TEXAS INSTRUMENTS

Linear Circuits

Voltage Regulators and Supervisors

Data Book
Volume 3

Data Book
Volume 3

Linear Circuits
Voltage Regulators and Supervisors

1989

1989

Linear Products

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TEXAS
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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed to provide highly-reliable power supply controllers and regulators, voltage references, and voltage converters for system operations.

TI voltage regulators and supervisory circuits represent processes from standard bipolar through BIDFET† and Schottky technologies.

This data book (Volume 3 of 3) provides information on the following types of products:

- Supervisory circuits
- Switched-capacitance voltage converters
- Shunt voltage regulators and voltage references
- Adjustable series-pass voltage regulators
- Switching power supply and pulse-width-modulated (PWM) controllers and regulators
- Fixed output series-pass voltage regulators (positive and negative)

These products provide critical functions for power conversion in analog and digital systems that:

- Utilize a wide range of voltages
- Require a constant output voltage regardless of changes in input voltage, output current, and ambient temperature
- Demand high input-output isolation where analog circuitry must be connected independent of digital ground
- Need low-voltage (battery) regulation.

New surface-mount packages (8 to 20 leads) include plastic chip carriers and the small-outline (D) plastic packages that optimize board density with minimum impact on power-dissipation capability. Test equipment with handlers and automated assembly bonders strengthens the production capabilities to provide a lower cost-to-performance ratio. TI continues to enhance quality and reliability of integrated circuits by improving materials, processes, test methods, and test equipment. In addition, specifications and programs are continuously updated. Quality and performance are monitored throughout all phases of manufacturing.

The alphanumeric listing in this data book includes all devices in Volumes 1, 2, and 3. Products in this data book are shown in **bold** type. The alphanumeric index provides a method of quickly locating the correct device type. The selection guide includes a functional description of each device providing key parameter information and packaging types. Ordering information and mechanical data are in the last section of the data book.

While this volume offers design and specification data only for voltage regulators and supervisory circuit components, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that the new 1989 Voltage Regulators and Supervisors data book will be a significant addition to your library of technical literature from Texas Instruments.

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process

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power supply supervisors

(Values specified for T_A = 25°C)

FUNCTION	SENSE INPUT SUPPLY		SENSE INPUT THRESHOLD (V TYP)	THRESHOLD TOLERANCE (%)	OUTPUT	TYPE	PACKAGE	PAGE NO.
	1 VSU	2 VSU						
Overvoltage Monitor	*	–	2.6	5	Open-Emitter	MC3423	D, JG, P	2-75
Undervoltage Monitor	*	–	2.53	1	Open-Collector	TL7702A	D, P	2-191
	5 V	–	4.55			TL7705A		
	9 V	–	7.6			TL7709A		
	12 V	–	10.8			TL7712A		
	15 V	–	13.5			TL7715A		
CMOS Undervoltage Monitor	*	–	1.2	1	Open-Drain	TLC7701	D, JG, P	3-15
					Push-Pull	TLC7721		
	5 V	–	4.55	1	Open-Drain	TLC7705		
					Push-Pull	TLC7725		
CMOS Undervoltage Monitor	5 V	*	4.55	1	Open-Collector	TL7780-5	D, N	2-205
	12 V	*	10.9			TL7780-12		
	15 V	*	13.64			TL7780-15		
Dual Undervoltage /Overvoltage*	5 V	*	4.55	1	Open-Collector	TL7770-5	DW, N	2-199
	12 V	*	10.9			TL7770-12		
	15 V	*	13.64			TL7770-15		

*Programmable

switched-capacitor voltage converters

(Values specified for T_A = 25°C)

CONTROL TOPOLOGY	OUTPUT SWITCH	SUPPLY VOLTAGE RANGE (V)	QUIESCENT CURRENT (NO LOAD)	MAXIMUM CONTINUOUS I OUT	MAXIMUM FREQUENCY (kHz)	TYPICAL CONVERSION EFFICIENCY (%)	TYPE	PACKAGE	PAGE NO.
Voltage Mode	Single	1.5–9	200 μA	50 mA	10	95	LTC1044	JG, L, P	2-59
		3.5–15	150 μA	300 mA	35	90	LT1054		3-5

shunt voltage regulators/references

(Values specified for T_A = 25°C)

REGULATOR VOLTAGE RANGE (V)	MINIMUM SHUNT CURRENT TO MAINTAIN REG	MAXIMUM SHUNT CURRENT	TOLERANCE (%)	TEMPERATURE COEFFICIENT (TYP)	DEVICE	PACKAGE	PAGE NO.
2.5 (Typ)	10 μA	20 mA	1	20 PPM/°C	LT1004	D, LD, LP	2-39
	20 μA		2		LM185-2.5	L	2-3
					LM385-2.5	D, LD, LP	
	400 μA		0.2	15 PPM/°C	LT1009		2-51
2.5 to 30	500 μA (Typ)	150 mA	4	120 PPM/°C	TL430	LP	2-107
2.5 to 36	270 μA (Typ)		2	30 PPM/°C	TL431	D, JG, LD, LP, P	2-111
			1		TL431A	D, LP, P	

adjustable series-pass voltage regulators **(Values specified over operating temperature range)**

OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT VOLTAGE RANGE (V)	TOLERANCE (%)	MAXIMUM ($V_I - V_O$) DIFFERENCE	DEVICE	PACKAGE	PAGE NO.
Postive Output	100 mA	1.2 to 32	5	35 V	TL317	D, JG, LP	2-101
	750 mA	1.25 to 125	5	125 V	TL783	KC	2-173
	1.5 A	1.2 to 37	5	40 V	LM217 LM317		2-9
Negative Output	1.5 A	−1.2 to −37	4	−40 V	LM237 LM337		2-17
Positive or Negative Output	150 mA	2 to 37	5	38 V	uA723	D, J, N, U	2-211
Positive Output	5 A	3 to 28	2	30 V	LT1084	KA, KK	3-11

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switching power supply controllers and regulators

(Values specified for T_A = 25°C)

CONTROL TOPOLOGY	SINGLE ENDED	FIXED PUSH-PULL	SINGLE SWITCH OUTPUTS	TOTEM-POLE OUTPUTS	OUTPUT CURRENT PER SWITCH (mA)	MAXIMUM FREQUENCY (kHz)	VOLTAGE REFERENCE TOLERANCE (%)	PULSE-BY-PULSE CURRENT LIMITING	OUTPUT STEERING CONTROL	PROGRAMMABLE OUTPUTS	DEAD-TIME CONTROL	UNDERVOLTAGE LOCKOUT	SOFT START	ON-BOARD AMPLIFIERS	CURRENT-SENSE AMPLIFIERS	50% MAXIMUM DUTY CYCLE	TYPE	PKG	PAGE NO.
Voltage-Mode Pulse-Width Modulated Controllers	X	—	X	—	250	200	5	—	—	—	X	—	—	2	—	—	MC34060	D, N	2-81
	—					300			—	X	X	—	—	2	X	—	TL493	D, J, N	2-123
									—	X	X	—	—	2	—	—	TL494		
									X	X	X	—	—	2	—	—	TL495	N	
		X	—						—	—	—	—	—	1	1	—	SG2524 SG3524	J, N	2-89
		—	X				1		—	X	X	X	—	2	—	—	TL594	D, N	2-143
									X	X	X	X	—	2	—	—	TL595		
		X	—	X	250	300	1	—	—	X	X	X	—	2	—	—	TL598	D, J, N	2-153
	X	—	Dual	—	21	500	4	—	—	—	X	X	—	—	X	—	TL1451A	D, N	2-185
Current Mode Pulse-Width Modulated Controllers	X	—	—	X	±1000	500	1	X	—	—	—	X	—	1	X	—	UC2842 UC2843 UC3842 UC3843	D, P	2-21
																X	UC2844 UC2845 UC3844 UC3845		2-21
	—	X	—	X	±1000	500	1	X	—	—	—	X	—	1	X	—	UC1846 UC1847	J	2-263
																	UC2846 UC2847 UC3846 UC3847	FN, N	
	X	—	X	—	5000	40	2	X	—	—	—	—	—	1	X	—	LT1070	KJ, KV	3-9
Fixed On-Time Voltage Mode	X	—	X	—	1200	40	10	—	—	—	—	—	—	1	—	—	TL496	D, P	2-131
							5	—	—	—	—	—	—	1	—	—	TL499A	P	3-13
					700	50	5	—	—	—	—	—	—	1	—	—	TL497A	D, J, N	2-135

X Applicable data
— Non-applicable data

positive fixed output series-pass voltage regulators

(Values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
2.6	100 mA	5	2	uA78L02A	D, JG, LP	2-229
		10		uA78L02		
5	100 mA	5		uA78L05A		
		5	0.6	LM2931-5AQ	D, KC, LP	2-37
		10	2	uA78L05	D, JG, LP	2-229
	150 mA	5	0.6	LM330	KC	2-21
		10		LM2930-5	KC, LP	2-29
		5		TL750L05	D, KC, LP, P	2-159
				TL751L05	D, P	
	500 mA		2	uA78M05	JG, KC	2-237
	750 mA	1	0.6	TL750M05	KC	2-163
				TL751M05		
	1.5 A	2	2	TL780-05		2-169
		5		uA7805		2-247
6	500 mA			uA78M06		2-237
6.2	100 mA	5		uA78L06A	D, JG, LP	2-229
		10		uA78L06		
	1.5 A	5		uA7806	KC	2-247
8	100 mA			uA78L08A	D, JG, LP	2-229
		10		uA78L08		
	150 mA		0.6	LM2930-8	KC, LP	2-29
		5		TL750L08	D, KC, LP, P	2-159
				TL751L08	D, P	2-159
	500 mA		2	uA78M08	KC	2-237
	750 mA	1	0.6	TL750M08		2-163
				TL751M08		
	1.5 A	5		uA7808		2-221
8.5				uA7885		2-221
9	100 mA		2	uA78L09A	D, JG, LP	2-229
		10		uA78L09		
	500 mA	5		uA78M09	KC	2-237
10	100 mA			uA78L10A	D, JG, LP	2-229
		10		uA78L10		
	150 mA	5	0.6	TL750L10	D, KC, LP, P	2-159
				TL751L10	D, P	2-159
	500 mA		2	uA78M10	KC	2-237
Dual 5	100 mA	4	2.2	LT1036	KJ, KV	3-3
Dual 12	3 A		3			

positive fixed output series-pass voltage regulators (continued)

(Values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
10	750 mA	1	0.6	TL750M10	KC	2-163
				TL751M10		
	1.5 A	5	2	uA7810		2-221
12	100 mA			uA78L12A	D, JG, LP	2-229
		10		uA78L12		
	150 mA	5	0.6	TL750L12	D, KC, LP, D	2-159
				TL751L12	D, P	2-159
	500 mA		2	uA78M12	JG, KC	2-237
	750 mA	1	0.6	TL750M12	KC	2-163
				TL751M12		
	1.5 A	2	2	TL780-12		2-169
		5		uA7812		2-221
15	100 mA			uA78L15A	D, JG, LP	2-229
		10		uA78L15		
	500 mA	5		uA78M15	JG, KC	2-237
	1.5 A	2		TL780-15	KC	2-169
		5		uA7815		2-221
18				uA7818		2-247
20	500 mA			uA78M20		2-237
24				uA78M24		
	1.5 A			uA7824		2-221

negative fixed output series-pass voltage regulators

(Values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
5	100 mA	5	1.7	MC79L05A	D, LP	2-77
		10		MC79L05		
	500 mA	5	2	uA79M05	JG, KC	2-253
	1.5 A			uA7905	KC	2-247
5.2				uA7952		
6	500 mA			uA79M06	JG, KC	2-253
	1.5 A			uA7906	KC	2-247
8	500 mA			uA79M08	JG, KC	2-253
	1.5 A			uA7908	KC	2-247
12	100 mA		1.7	MC79L12A	D, LP	2-77
		10		MC79L12		
	500 mA	5	2	uA79M12	JG, KC	2-253
	1.5 A			uA7912	KC	2-247
15	100 mA		1.7	MC79L15A	D, LP	2-77
		10		MC79L15		
	500 mA	5	2	uA79M15	JG, KC	2-253
	1.5 A			uA7915	KC	2-247
18				uA7918		
20	500 mA			uA79M20		2-253
24				uA79M24		
	1.5 A			uA7924		2-247

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	PAGE NO.
LM317	LM317	2-9
LM337	LM337	2-17
LM385-2.5	LM385-2.5	2-3
LT1004-2.5	LT1004-2.5	2-39
LT1009	LT1009	2-51
LT1036	LT1036	3-3
LT1070	LT1070	3-9
SG3524	SG3524	2-89
UC3846	UC3846	2-263
UC3847	UC3847	2-263

MOTOROLA	DIRECT TI REPLACEMENT	PAGE NO.
LM217, LM317	LM217, LM317	2-9
LM237, LM337	LM237, LM337	2-17
MC1723	UA723	2-211
MC3423	MC3423	2-75
MC34060	MC34060	2-81
MC78L00 Series	uA78L00 Series	2-229
MC78M00 Series	uA78M00 Series	2-237
MC79L00 Series	MC79L00 Series	2-77
TL431	TL431	2-111
TL431A	TL431A	2-111
TL494	TL494	2-123
TL495	TL495	2-123
TL780-5	TL780-5	2-169
TL780-12	TL780-12	2-169
TL780-15	TL780-15	2-169

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM217, LM317	LM217, LM317		2-9
LM237, LM337	LM237, LM337		2-17
LM317L	TL317		2-101
LM330	LM330		2-21
LM336-2.5		LT1009	2-51
LM385-2.5	LM385-2.5	LT1004-2.5	2-39
LM723	uA723		2-211
LM2930-5	LM2930-5		2-29
LM2930-8	LM2930-8		2-29
LM2931-5	LM2931-5A		2-37
LM3524	SG3524		2-89
LM7800 Series	uA7800 Series		2-221
LM78L00 Series	uA78L00 Series		2-229
LM78M00 Series	uA78M00 Series		2-237
LM7900 Series	uA7900 Series		2-247
LM79L00 Series	MC79L00 Series		2-77
LM79M00 Series	uA79M00 Series		2-253

SILICON GENERAL	DIRECT TI REPLACEMENT	PAGE NO.
SG3524	SG3524	2-89
SG3842/3/4/5	UC3842/3/4/5	3-21

SPRAGUE	DIRECT TI REPLACEMENT	PAGE NO.
ULN8194	TL594	2-143
ULN8195	TL595	2-143

UNITRODE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
TL431	TL431		2-111
UC317	LM317		2-9
UC337	LM337		2-17
UC494	TL494		2-123
UC494A	TL594		2-143
UC495	TL495		2-123
UC495A	TL595		3-143
UC2842/3/4/5	UC2842/3/4/5		3-21
UC3842/3/4/5	UC3842/3/4/5		3-21
UC3846/UC2846	UC3846/UC2846		2-263
UC3847/UC2847	UC3847/UC2847		2-263
UC7800 Series	uA7800 Series		2-221
UC7800A Series		TL780-00 Series	2-169
UC7900 Series	uA7900 Series		2-247

SERIES REGULATORS

Bias Current

The difference between input and output currents.
NOTE: This is sometimes referred to as quiescent current.

Current-Limit Sense-Voltage

The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry. This is the current-sense voltage at which current limiting occurs.

Dropout Voltage

The low input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage

The voltage that is a function of the output voltage and is used for feedback control of the regulator.

Input Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in input voltage from one level to another level.
NOTE: Sometimes this characteristic is normalized with respect to the input voltage change.

Output Noise Voltage

The rms output noise voltage, sometimes expressed as a percentage of the dc output voltage, with constant load and no input ripple.

Output Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in load current from one level to another level.

Output Voltage Change with Temperature

The percentage change in the output voltage for a change in temperature. This is the net change over the total temperature range.

Output Voltage Long-Term Drift

The change in output voltage over a long period of time.

Peak Output Current

The maximum output current that can be obtained from the regulator due to limiting circuitry within the regulator.

Reference Voltage

The voltage that is compared with the feedback sense voltage to control the regulator.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
NOTE: This is the reciprocal of ripple sensitivity.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage, sometimes expressed as a percentage of output voltage, to the peak-to-peak input ripple voltage.
NOTE: This is the reciprocal of ripple rejection.

Short-Circuit Output Current

The output current of the regulator with the output shorted to ground.

Standby Current

The input current drawn by the regulator with no output load and no reference voltage load.

Temperature Coefficient of Output Voltage (αVO)

The ratio of the change in output voltage, usually expressed as a percentage of output voltage, to the change in temperature. This is the average value for the total temperature change.

$$\alpha VO = \pm\left[\frac{V_O \text{ at } T_2 - V_O \text{ at } T_1}{V_O \text{ at } 25°C}\right]\left[\frac{100\%}{T_2 - T_1}\right]$$

SHUNT REGULATORS

NOTE: These terms and symbols are based on JEDEC and IEC standards for voltage regulator diodes.

Anode

The electrode to which the regulator current flows within the regulator when it is biased for regulation.

Cathode

The electrode from which the regulator current flows within the regulator when it is biased for regulation.

Dynamic Impedance $|z_{KA}|$

The quotient of a change in voltage across the regulator and the corresponding change in current through the regulator when it is biased for regulation.

Noise Voltage (V_{nz})

The rms noise voltage with the regulator biased for regulation and with no input ripple.

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)

The voltage at the reference input terminal with respect to the anode terminal.

Regulator Current (I_Z)

The dc current through the regulator when it is biased for regulation.

Regulator Current near Lower Knee of Regulation Range (I_{ZK})

The regulator current near the lower limit of the region within which regulation occurs; this corresponds to the breakdown knee of a regulator diode.

Regulator Current at Maximum Limit of Regulation Range (I_{ZM})

The regulator current above which the differential resistance of the regulator significantly increases.

Regulator Voltage (V_Z)

The dc voltage across the regulator.

Shunt Regulator

A device having a voltage-current characteristic similar to that of a voltage-regulator diode. It is normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) and develops across its terminals an essentially constant voltage throughout a specified current range.

Temperature Coefficient of Reference Voltage (αV_{ref})

The ratio of the change in reference voltage to the change in temperature. This is the average value for the total temperature change.

To obtain a value in ppm/°C:

$$\alpha V_{ref} = \left[\frac{V_{ref\ at\ T_2} - V_{ref\ at\ T_1}}{V_{ref\ at\ 25°C}}\right]\left[\frac{10^6}{T_2 - T_1}\right]$$

General Information 1

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Product Previews 3

Design Considerations 4

Mechanical Data 5

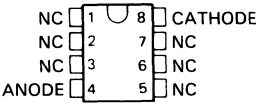
Contents

Supervisor Functions
Series-Pass Voltage Regulators
Shunt Regulators
Voltage References
DC-to-DC Converters
PWM Controllers

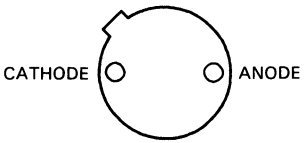
D3189, JANUARY 1989

- **Operating Current Range . . . 20 µA to 20 mA**
- **1.5% and 3% Initial Voltage Tolerance**
- **Reference Impedance . . .**
  LM185 . . . 0.6 Ω Max at 25°C
  LM385 . . . 1 Ω Max at 25°C
  All Devices . . . 1.5 Ω Max Over Full Temperature Range
- **Very Low Power Consumption**
- **Applications:**
  Portable Meter References
  Portable Test Instruments
  Battery-Operated Systems
  Current-Loop Instrumentation
  Panel Meters
- **Designed to be Interchangeable with National LM185-2.5, LM285-2.5, and LM385-2.5**

D PACKAGE
(TOP VIEW)

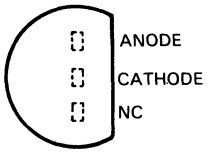


LD PACKAGE
(TOP VIEW)



The anode is in electrical contact with the case.

LP PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

description

These micropower terminal bandgap voltage references operate over a 20-µA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The LM185-2.5 series bandgap reference has low noise and good long-term stability.

Careful design of the LM185-2.5 series has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating temperature range allows its use with widely varying supplies with excellent regulation.

The extremely low-power drain of the LM185-2.5 series makes it useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current range allows them to replace older references with a tighter tolerance part.

The LM185-2.5 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM285-2.5 is characterized for operation from −40°C to 85°C. The LM385-2.5 and LM385B-2.5 are characterized for operation from 0°C to 70°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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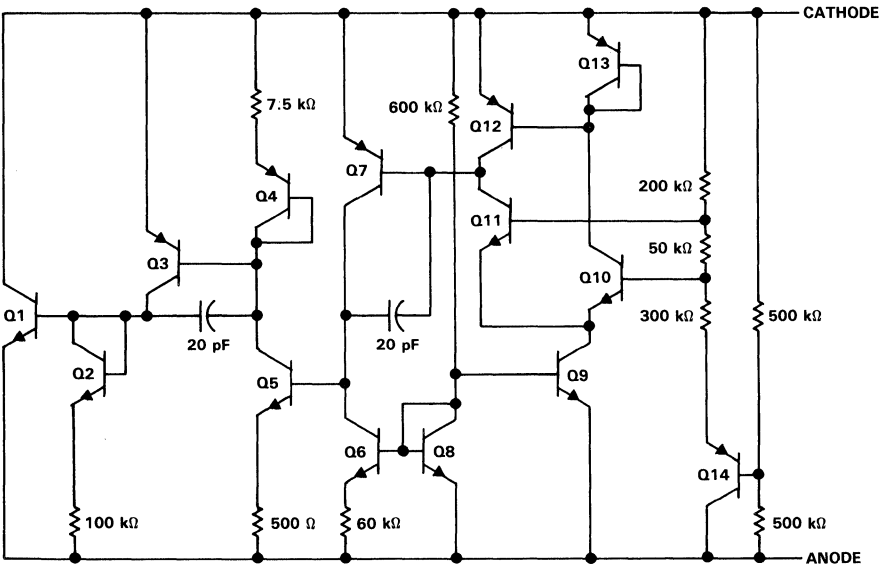
AVAILABLE OPTIONS

T_A	V_Z TOLERANCE	PACKAGE		
		SMALL OUTLINE (D)	METAL CAN (LD)	PLASTIC (LP)
0°C to 70°C	3%	LM385D-2.5		LM385LP-2.5
	1.5%	LM385BD-2.5		LM385BLP-2.5
−40°C to 85°C	1.5%	LM285D-2.5	LM285LD-2.5	LM285LP-2.5
−55°C to 125°C	1.5%		LM185LD-2.5	

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LM385DR-2.5).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current . . . . . 30 mA
Forward current . . . . . 10 mA
Operating free-air temperature range: LM185-2.5 . . . . . −55°C to 125°C
LM285-2.5 . . . . . −40°C to 85°C
LM385-2.5, LM385B-2.5 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: LD package . . . . . 300°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LM185-2.5, LM285-2.5			LM385-2.5			LM385B-2.5			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 20 µA to 20 mA	25°C	2.462	2.5	2.538	2.425	2.5	2.575	2.462	2.5	2.538	V
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 20 µA to 20 mA	25°C		±20			±20			±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 20 µA to 1 mA	25°C			1			2			2	mV
			Full range			1.5			2.5			2.5	
		I_Z = 1 mA to 20 mA	25°C			10			20			20	
			Full range			20			25			25	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA	25°C		±20			±20			±20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range		8	20		8	20		8	20	µA
Z_Z	Reference impedance	I_Z = 100 µA	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C		120			120			120		µV

† Full range is −55°C to 125°C for the LM185M-2.5, −40°C to 85°C for the LM285-2.5, and 0°C to 70°C for the LM385-2.5 and LM385B-2.5.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REVERSE CHARACTERISTICS

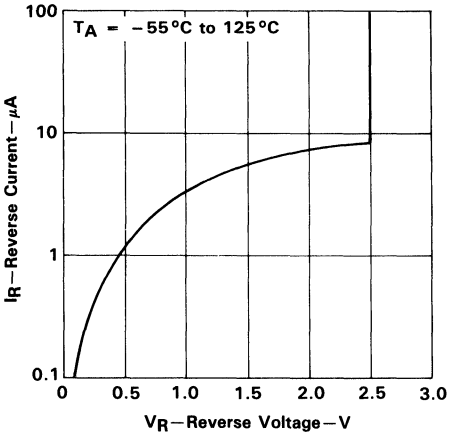


FIGURE 1

REFERENCE VOLTAGE CHANGE WITH REVERSE CURRENT

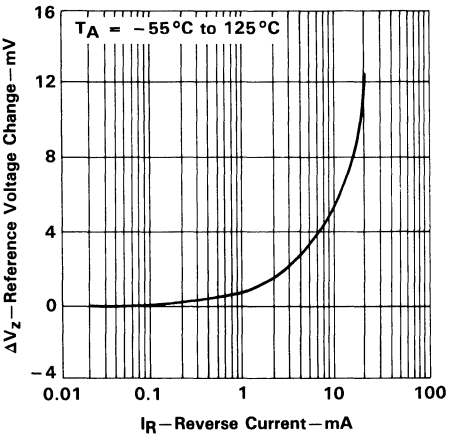


FIGURE 2

FORWARD CHARACTERISTICS

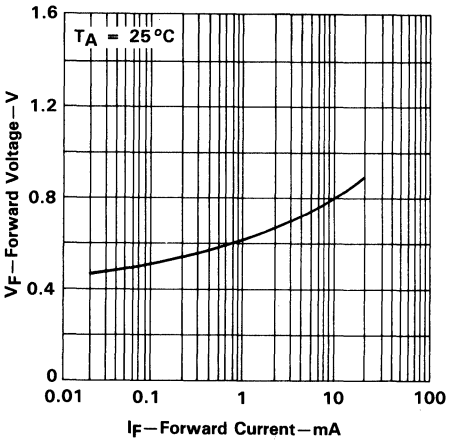


FIGURE 3

REFERENCE VOLTAGE VS FREE-AIR TEMPERATURE

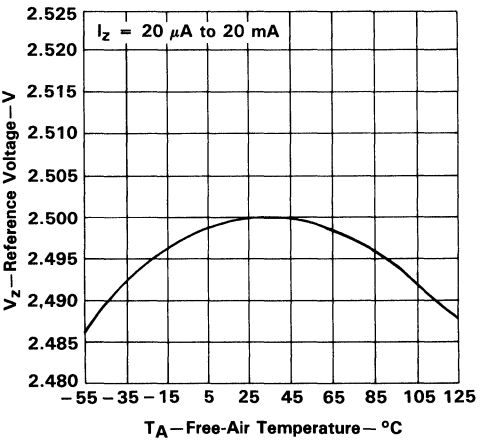


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

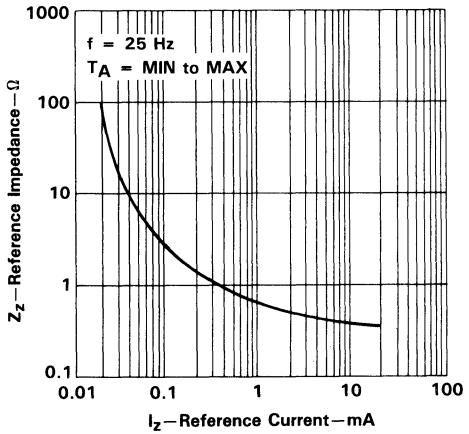


FIGURE 5

REFERENCE IMPEDANCE
vs
FREQUENCY

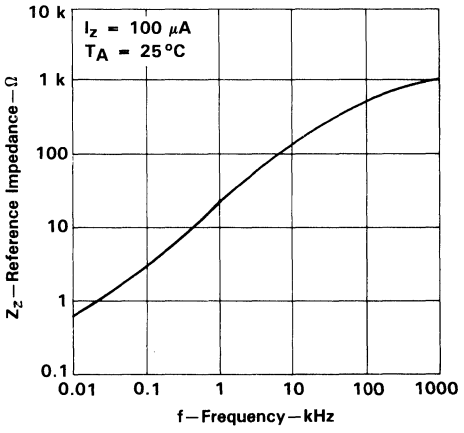


FIGURE 6

NOISE VOLTAGE
vs
FREQUENCY

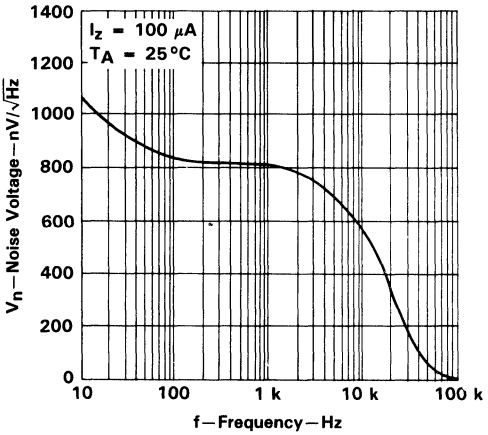


FIGURE 7

FILTERED RMS OUTPUT NOISE VOLTAGE
vs
FREQUENCY

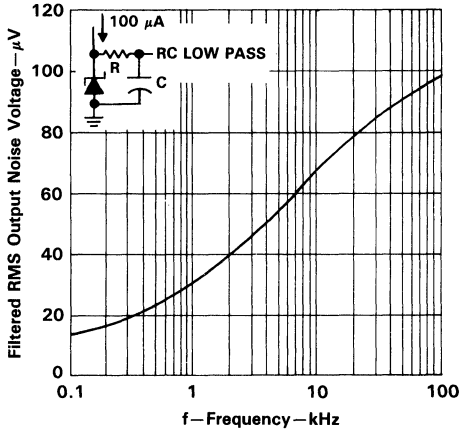


FIGURE 8

TYPICAL CHARACTERISTICS

TRANSIENT RESPONSE

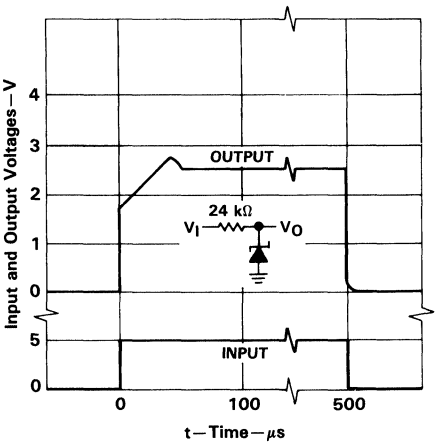


FIGURE 9

TYPICAL APPLICATION DATA

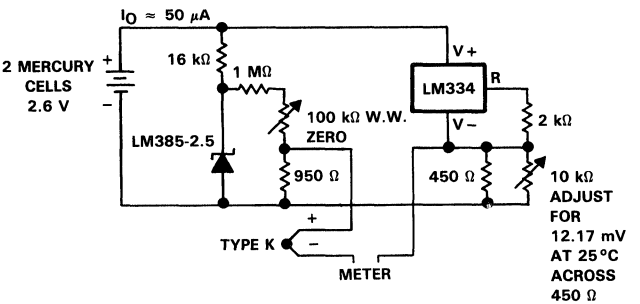


FIGURE 10. THERMOCOUPLE COLD-JUNCTION COMPENSATOR

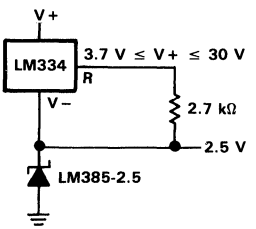


FIGURE 11. OPERATION OVER A WIDE SUPPLY RANGE

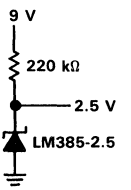


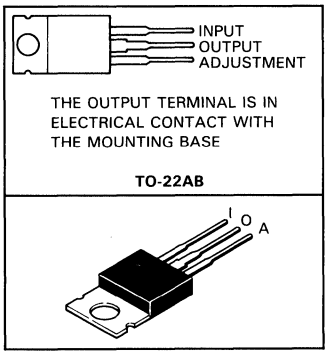
FIGURE 12. REFERENCE FROM A 9-V BATTERY

D2212, SEPTEMBER 1977—REVISED FEBRUARY 1988

- Output Voltage Range Adjustable from 1.2 V to 37 V
- Output Current Capability of 1.5 A Max
- Input Regulation Typically 0.01% Per Input-Volt Change
- Output Regulation Typically 0.1%
- Peak Output Current Constant Over Temperature Range of Regulator
- Popular 3-Lead TO-220AB Package
- Ripple Rejection Typically 80 dB
- Direct Replacement for National LM217 and LM317

terminal assignments

KC PACKAGE
(TOP VIEW)



description

The LM217 and LM317 are adjustable 3-terminal positive-voltage regulators capable of supplying 1.5 A over a differential voltage range of 3 V to 40 V. They are exceptionally easy to use and require only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The devices are packaged in a standard transistor package that is easily mounted and handled.

In addition to higher performance than fixed regulators, these regulators offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection, and safe-area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, these regulators are useful in a wide variety of other applications. The primary applications of each of these regulators is that of a programmable output regulator, but by connecting a fixed resistor between the adjustment terminal and the output terminal, each device can be used as a precision current regulator. Even though the regulator is floating and sees only the input-to-output differential voltage, use of these devices to regulate output voltages that would cause the maximum-rated differential voltage to be exceeded if the output became shorted to ground is not recommended. The TL783 is recommended for output voltages exceeding 37 V. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2 V where most loads draw little current.

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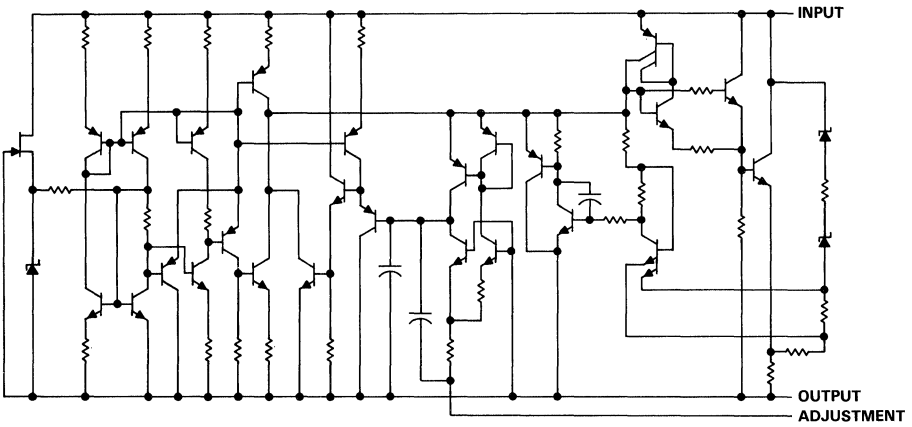
The LM217 and LM317 are characterized for operation from −25°C to 150°C and from 0°C to 125°C, respectively.

schematic



absolute maximum ratings over operating temperature range (unless otherwise noted)

	LM217	LM317	UNIT
Input-to-output differential voltage, $V_I - V_O$	40	40	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2000	2000	mW
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	20	15	W
Operating free-air, case, or virtual junction temperature range	−25 to 150	0 to 125	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 15 and 16. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	LM217		LM317		UNIT
	MIN	MAX	MIN	MAX	
Output current, I_O	5	1500	10	1500	mA
Operating virtual junction temperature, T_J	−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS†		LM217			LM317			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation (See Note 3)	$V_I - V_O$ = 3 V to 40 V, See Note 4	T_J = MIN to MAX		0.01	0.02		0.01	0.04	%/V
		I_O = 10 mA to 1.5 A		0.02	0.05		0.02	0.07	
Ripple rejection	V_O = 10 V,	f = 120 Hz		65			65		dB
	V_O = 10 V, 10-μF capacitor between ADJ and ground	f = 120 Hz,	66	80		66	80		
Output regulation	I_O = 10 mA to 1.5 A, T_J = 25°C, See Note 4	$V_O \leq 5$ V		5	15		5	25	mV
		$V_O > 5$ V		0.1	0.3		0.1	0.5	%
	I_O = 10 mA to 1.5 A, See Note 4	$V_O \leq 5$ V		20	50		20	70	mV
		$V_O > 5$ V		0.3	1		0.3	1.5	%
Output voltage change with temperature	T_J = MIN to MAX			1			1		%
Output voltage long-term drift (see Note 5)	After 1000 h at T_J = MAX and $V_I - V_O$ = 40 V			0.3	1		0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C			0.003			0.003		%
Minimum output current to maintain regulation	$V_I - V_O$ = 40 V			3.5	5		3.5	10	mA
Peak output current	$V_I - V_O \leq 15$ V		1.5	2.2		1.5	2.2		A
	$V_I - V_O \leq 40$ V, T_J = 25°C			0.4		0.15	0.4		
Adjustment-terminal current				50	100		50	100	μA
Change in adjustment-terminal current	$V_I - V_O$ = 2.5 V to 40 V, I_O = 10 mA to 1.5 A			0.2	5		0.2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O$ = 3 V to 40 V, I_O = 10 mA to 1.5 A, P ≤ 15 W		1.2	1.25	1.3	1.2	1.25	1.3	V

†Unless otherwise noted, these specifications apply for the following test conditions; $V_I - V_O$ = 5 V and I_O = 0.5 A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.
3. Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.
4. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
5. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA

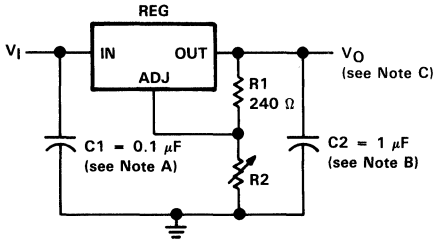


FIGURE 1. ADJUSTABLE VOLTAGE REGULATOR

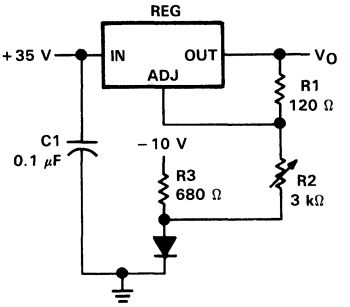
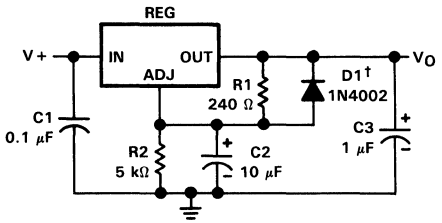


FIGURE 2. 0-V to 30-V REGULATOR CIRCUIT



†D1 discharges C2 if output is shorted to ground.

FIGURE 3. ADJUSTABLE REGULATOR CIRCUIT WITH IMPROVED RIPPLE REJECTION

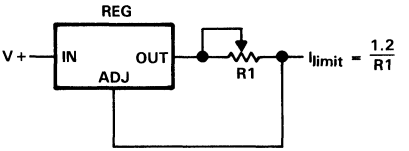


FIGURE 4. PRECISION CURRENT LIMITER CIRCUIT

NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.
B. Use of an output capacitor improves transient response but is optional.
C. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$
V_{ref} equals the difference between the output and adjustment terminal voltages.

TYPICAL APPLICATIONS

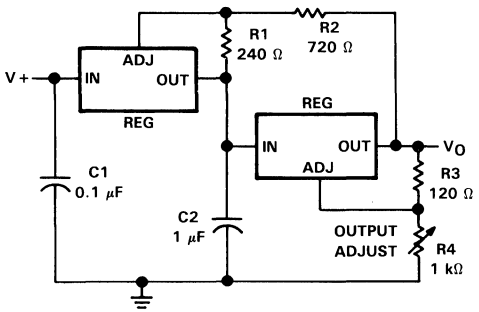


FIGURE 5. TRACKING PREREGULATOR CIRCUIT

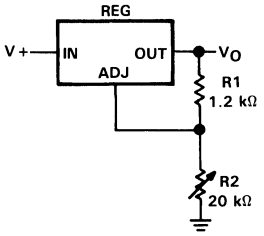


FIGURE 6. 1.2 to 20-V REGULATOR CIRCUIT WITH MINIMUM PROGRAM CURRENT

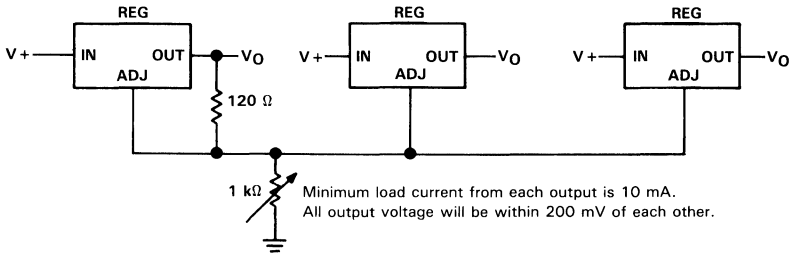
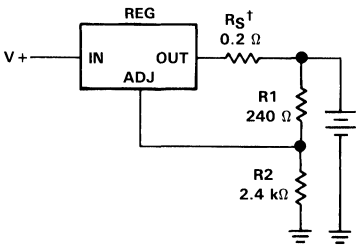


FIGURE 7. ADJUSTING MULTIPLE ON-CARD REGULATORS WITH A SINGLE CONTROL



†R_S controls output impedance of charger

$$Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$$

The use of R_S allows low charging rates with a fully-charged battery.

FIGURE 8. BATTERY CHARGER CIRCUIT

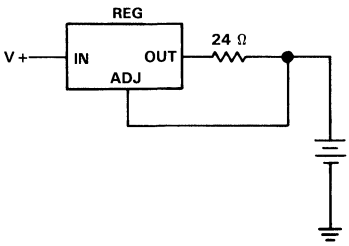


FIGURE 9. 50-mA CONSTANT-CURRENT BATTERY CHARGER CIRCUIT

TYPICAL APPLICATIONS

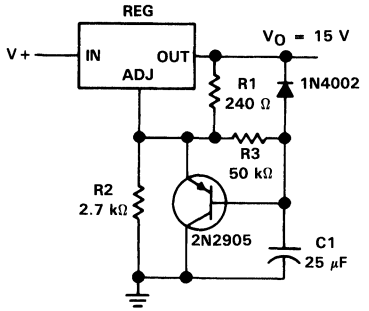


FIGURE 10. SLOW-TURN-ON 15-V REGULATOR CIRCUIT

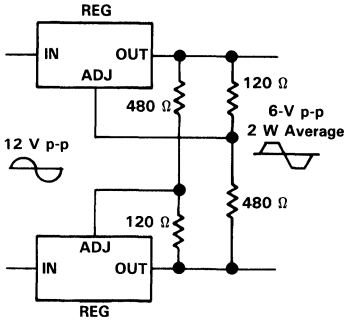
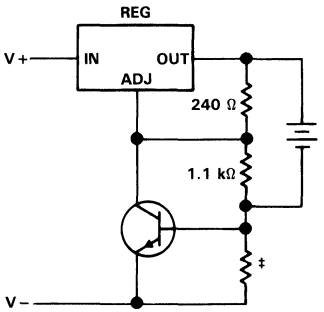


FIGURE 11. A-C VOLTAGE REGULATOR CIRCUIT



‡This resistor sets peak current (0.6 A for 1 Ω)

FIGURE 12. CURRENT-LIMITED 6-V CHARGER

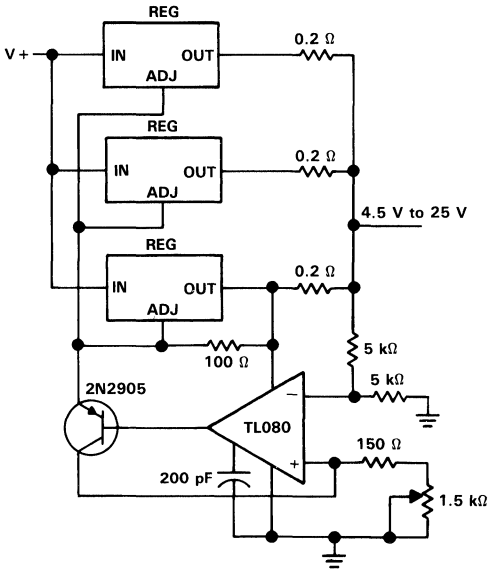


FIGURE 13. ADJUSTABLE 4-A REGULATOR

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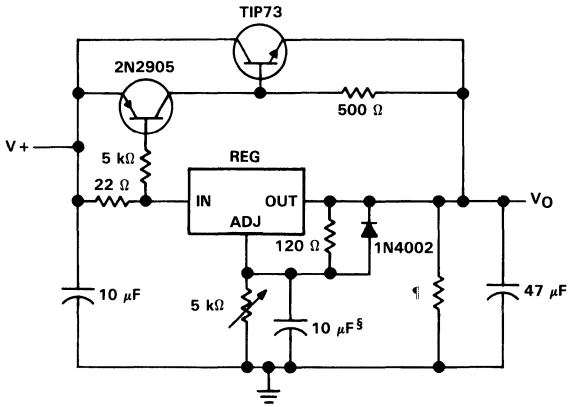
TYPICAL APPLICATIONS



¶Minimum load current is 30 mA.
§Optional capacitor improves ripple rejection

FIGURE 14. HIGH-CURRENT ADJUSTABLE REGULATOR

THERMAL INFORMATION

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

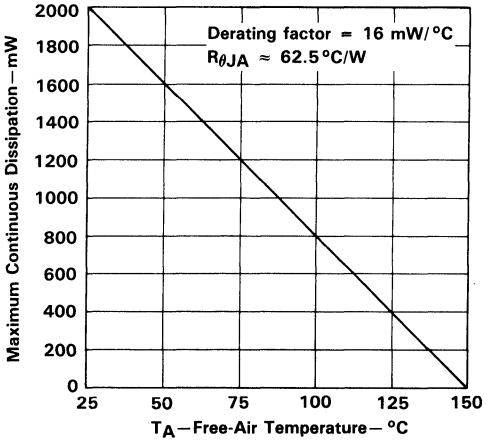


FIGURE 15

CASE TEMPERATURE DISSIPATION DERATING CURVE

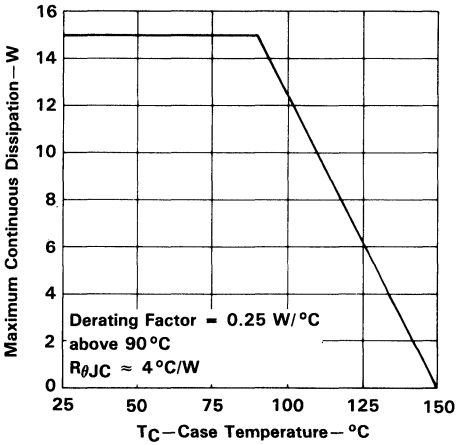
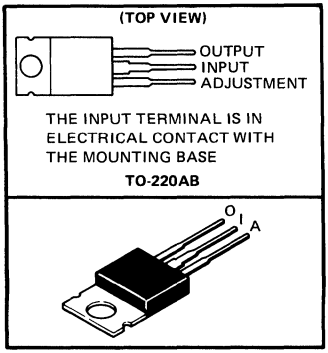


FIGURE 16

D2640, NOVEMBER 1981 – REVISED FEBRUARY 1988

- **Output Voltage Range Adjustable from −1.2 V to −37 V**
- **I_O Capability of 1.5 A Max**
- **Input Regulation Typically 0.01% per Input-Volt Change**
- **Output Regulation Typically 0.3%**
- **Peak Output Current Constant Over Temperature Range of Regulator**
- **Ripple Rejection Typically 77 dB**
- **Direct Replacement for National Semiconductor LM237, LM337**

LM237, LM337 . . . KC PACKAGE
(TOP VIEW)

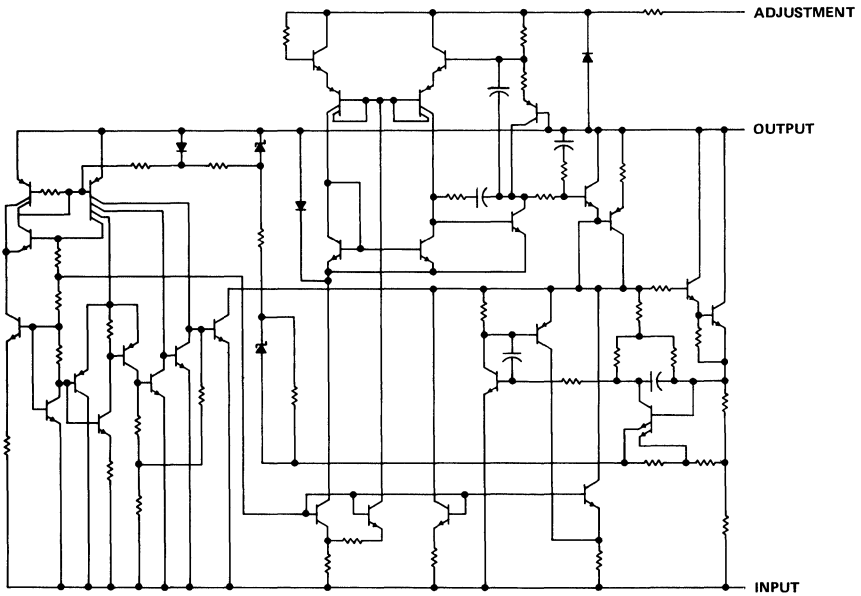


description

The LM237 and LM337 are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of −1.5 A over an output voltage range of −1.2 V to −37 V. They are exceptionally easy to use, requiring only two external resistors to set the output voltage and one output capacitor for frequency compensation. The current design has been optimized for excellent regulation and low thermal transients. In addition, the LM237 and LM337 feature internal current limiting, thermal shutdown, and safe-area compensation, making them virtually immune to blowout by overloads.

The LM237 and LM337 serve a wide variety of applications including local on-card regulation, programmable output voltage regulation, or precision current regulation. They are ideal complements to the LM217 and LM317 adjustable positive-voltage regulators.

schematic diagram



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absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ . . . . . −40 V
Continuous total dissipation at 25°C free-air temperature (see Note 1) . . . . . 2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 15 W
Operating free-air, case, or virtual junction temperature range: LM237 . . . . . −25°C to 150°C
LM337 . . . . . 0°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

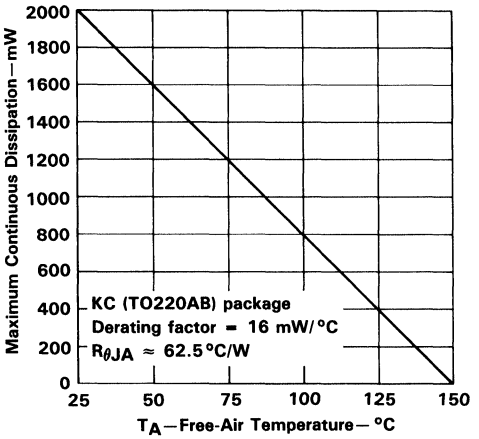

FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

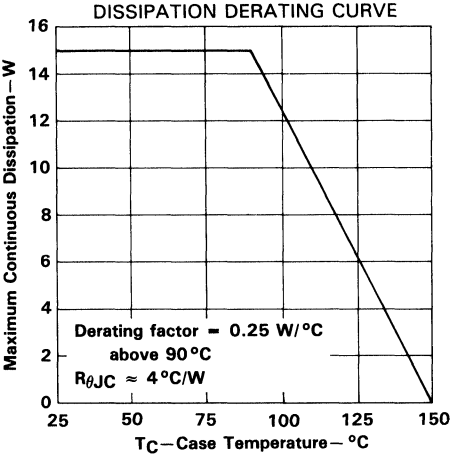

FIGURE 2

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recommended operating conditions

		LM237		LM337		UNIT
		MIN	MAX	MIN	MAX	
Output current, I_O	$\lvert V_I - V_O \rvert \leq 40$ V, $P \leq 15$ W	10	1500	10	1500	mA
	$\lvert V_I - V_O \rvert \leq 10$ V, $P \leq 15$ W	6	1500	6	1500	
Operating virtual junction temperature, T_J		−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

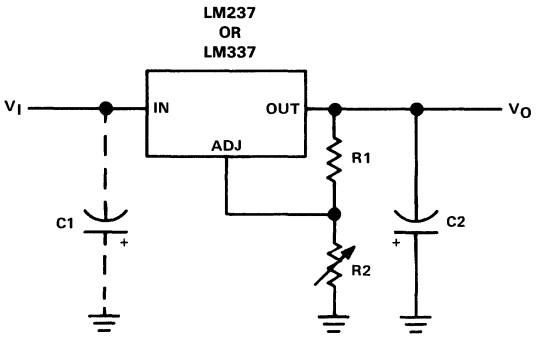
PARAMETER	TEST CONDITIONS†		LM237			LM337			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation‡	$V_I - V_O = -3$ V to −40 V	$T_J = 25$°C		0.01	0.02		0.01	0.04	%/V
		T_J = MIN to MAX		0.02	0.05		0.02	0.07	
Ripple rejection	$V_O = -10$ V,	f = 120 Hz		60			60		dB
	$V_O = -10$ V, $C_{ADJ} = 10\ \mu$F	f = 120 Hz	66	77		66	77		
Output regulation	I_O = 10 mA to 1.5 A, $T_J = 25$°C	$\lvert V_O \rvert \leq 5$ V			25			50	mV
		$\lvert V_O \rvert \geq 5$ V			0.5			1	%
	I_O 10 mA to 1.5 A	$\lvert V_O \rvert \leq 5$ V			50			70	mV
		$\lvert V_O \rvert \geq 5$ V			1			1.5	%
Output voltage change with temperature	T_J = MIN to MAX			0.6			0.6		%
Output voltage long-term drift (see Note 2)	After 1000 h at T_J = MAX and $V_I - V_O = -40$ V			0.3	1		0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz,	$T_J = 25$°C		0.003			0.003		%
Minimum output current to maintain regulation	$\lvert V_I - V_O \rvert \leq 40$ V			2.5	5		2.5	10	mA
	$\lvert V_I - V_O \rvert \leq 10$ V			1.2	3		1.5	6	
Peak output current	$\lvert V_I - V_O \rvert \leq 15$ V		1.5	2.2		1.5	2.2		A
	$\lvert V_I - V_O \rvert \leq 40$ V,	$T_J = 25$°C	0.24	0.4		0.15	0.4		
Adjustment-terminal current				65	100		65	100	μA
Change in adjustment terminal current	$V_I - V_O = -2.5$ V to −40 V, I_O = 10 mA to MAX,	$T_J = 25$°C		2	5		2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = -3$ to −40 V, I_O = 10 mA to 1.5 A, $P \leq$ rated dissipation	$T_J = 25$°C	−1.225	−1.250	−1.275	−1.213	−1.25	−1.287	V
		T_J = MIN to MAX	−1.2	−1.25	−1.3	−1.2	−1.25	−1.3	
Thermal regulation	Initial $T_J = 25$°C,	10-ms pulse		0.002	0.02		0.003	0.04	%/W

†Unless otherwise noted, these specifications apply for the following test conditions $\lvert V_I - V_O \rvert$ = 5 V and I_O = 0.5 A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

NOTE 2: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA



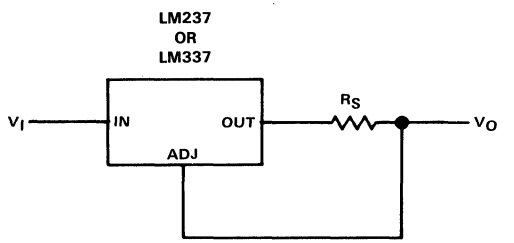
R1 is typically 120 Ω.

$$R2 = R1\left(\frac{-V_O}{-1.25} - 1\right)$$ where V_O is the output in volts.

C1 is a 1-μF solid tantalum required only if the regulator is more than 10 cm (4 in.) from the power supply filter capacitor.

C2 is a 1-μF solid tantalum or 10-μF aluminum electrolytic required for stability.

FIGURE 3. ADJUSTABLE NEGATIVE-VOLTAGE REGULATOR



$$R_S = \frac{1.25\ V}{I_{LIMIT}}$$

FIGURE 4. CURRENT-LIMITING CIRCUIT

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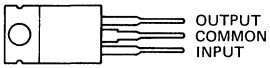
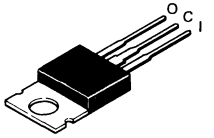
D2700, APRIL 1983—REVISED APRIL 1988

- **Input-Output Differential Less than 0.6 V**
- **Output Current of 150 mA**
- **Reverse Polarity Protection**
- **Line Transient Protection**
- **Internal Short-Circuit Current Limiting**
- **Internal Thermal Overload Protection**
- **Mirror-Image Insertion Protection**
- **Direct Replacement for National LM330T-5.0**

KC PACKAGE
(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE
TO-220AB



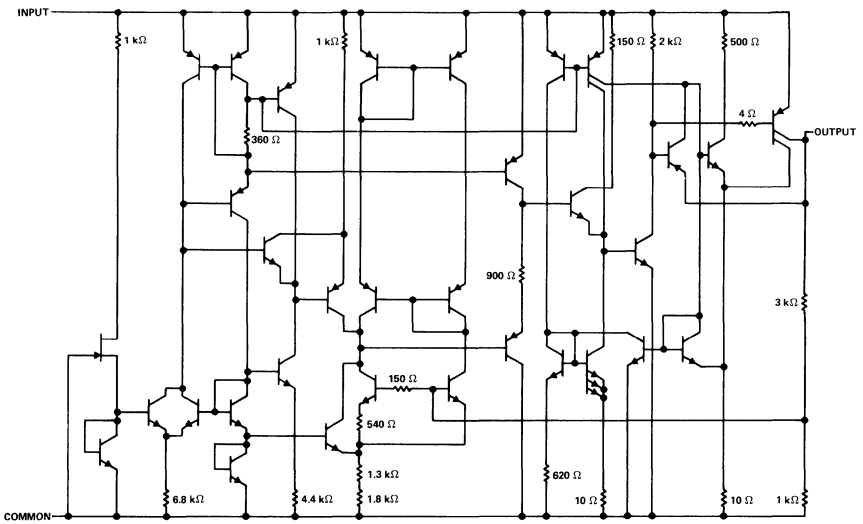
description

The LM330 3-terminal positive regulator features an ability to source 150 mA of output current with an input-output differential of 0.6 volt or less. Familar regulator features such as current limit and thermal overload protection are also provided.

The LM330 has low dropout voltage making it useful for certain battery applications. For example, since the low dropout voltage allows a longer battery discharge before the output falls out of regulation, a battery supplying the regulator input voltage may discharge to 5.6 V and still properly regulate the system and load voltage. The LM330 protects both itself and the regulated system from reverse installation of batteries.

Other protection features include line transient protection above 40 V, where the output actually shuts down to avoid damaging internal and external circuits. The LM330 regulator cannot be harmed by temporary mirror-image insertion.

schematic diagram



Resistor values shown are nominal.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage	26 V
Transient input voltage t = 1 s	40 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) case temperature (see Note 1)	15 W
Operating free-air, case, or virtual junction temperature	−55°C to 150°C
Storage temperature	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

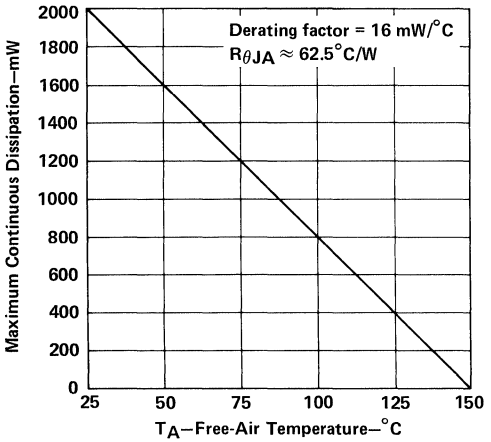

FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

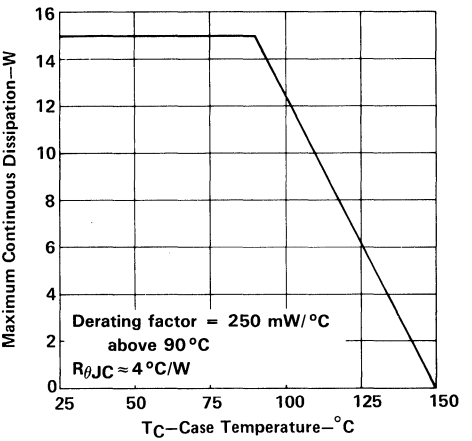

FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
I_O	Output current	5	150	mA
T_A	Operating virtual junction temperature	0	100	°C

electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETERS	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V,	I_O = 5 mA to 150 mA,	4.8	5	5.2	V
	T_J = 0°C to 100°C					
Input regulation		V_I = 9 V to 16 V		7	25	mV
		V_I = 6 V to 26 V		30	60	
Ripple rejection	f = 120 Hz			56		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 150°C			20		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			50		μV
Output voltage with input polarity reversed	R_L = 100 Ω	V_I = −30 V, t = 100 ms		> −0.3		V
		V_I = −12 V, DC		> −0.3		
Output voltage with input transient	V_I = 60 V,	t = 100 ms		<5.5		V
	V_I = 50 V,	t = 1 s		<5.5		
Bias current with input transient	R_L = 100 Ω	V_I = 40 V, t = 1 s		14		mA
		V_I = −6 V, t = 1 s		−80		
Overvoltage shutdown voltage			26	45		V
Output impedance	I_O = 100 mA, I_O = 10 mA (rms), f = 100 Hz to 10 kHz			200		mΩ
Bias current	I_O = 10 mA			3.5	7	mA
	I_O = 50 mA			5	11	
	I_O = 150 mA			18	40	
Bias current change	V_I = 6 V to 26 V			10		%
Peak output current			150	420	700	mA

† Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor across the output.

‡ Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

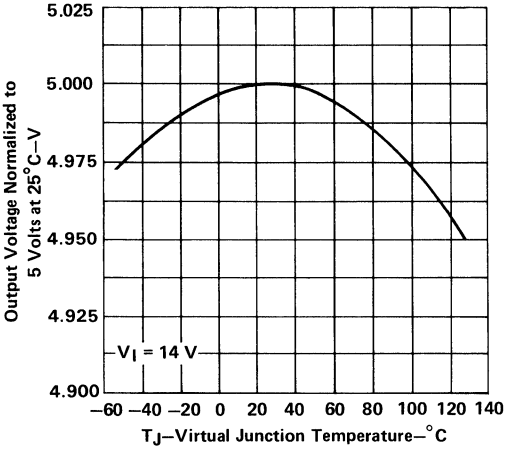

FIGURE 3

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

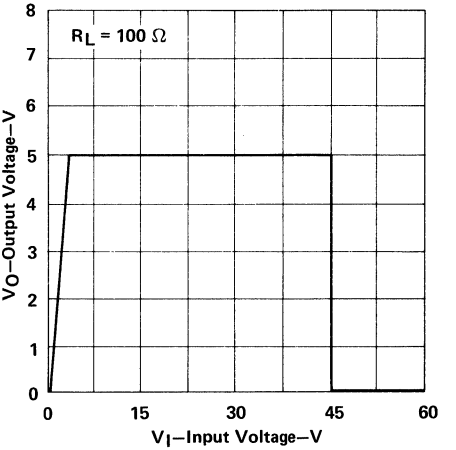

FIGURE 4

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

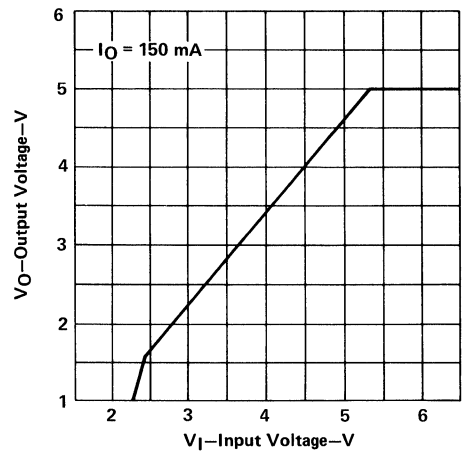

FIGURE 5

PEAK OUTPUT CURRENT
vs
INPUT VOLTAGE

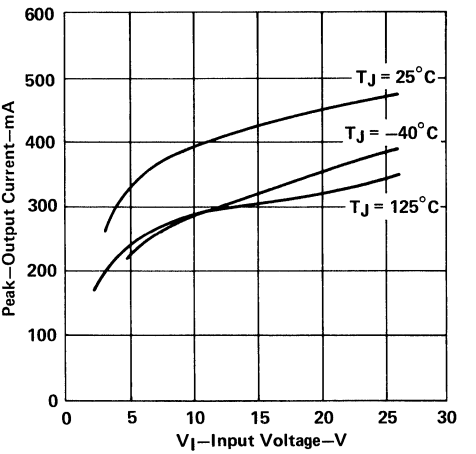

FIGURE 6

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TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

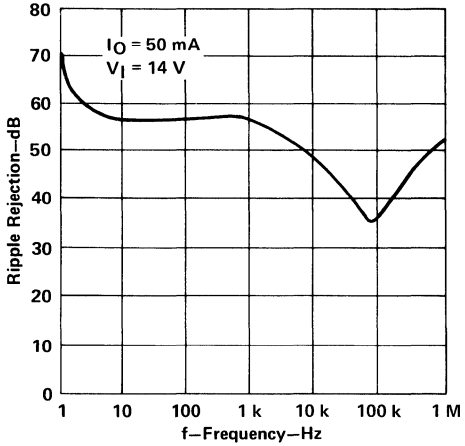

FIGURE 7

RIPPLE REJECTION
vs
OUTPUT CURRENT

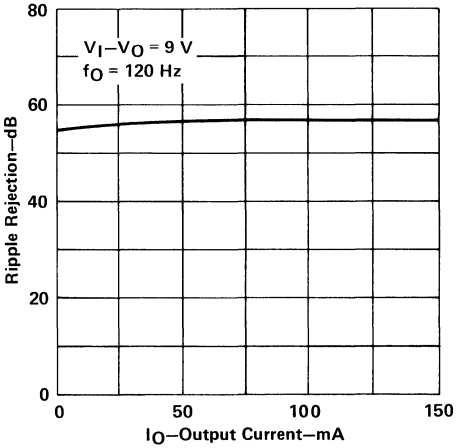

FIGURE 8

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

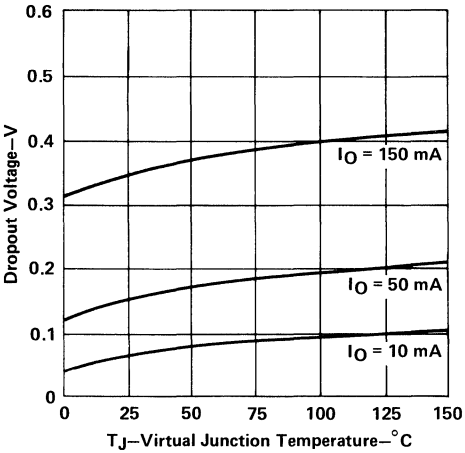

FIGURE 9

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

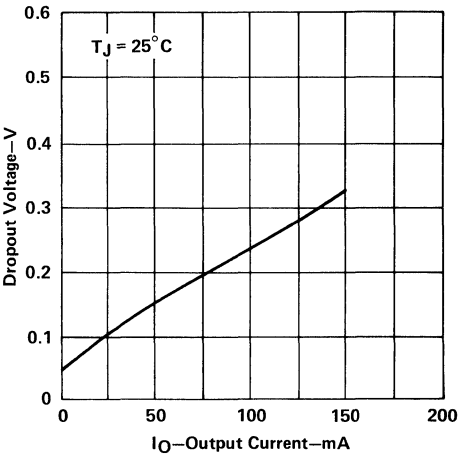

FIGURE 10

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

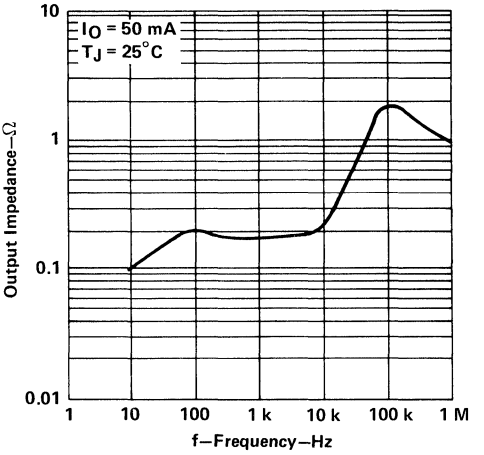

FIGURE 11

INPUT CURRENT
vs
INPUT VOLTAGE

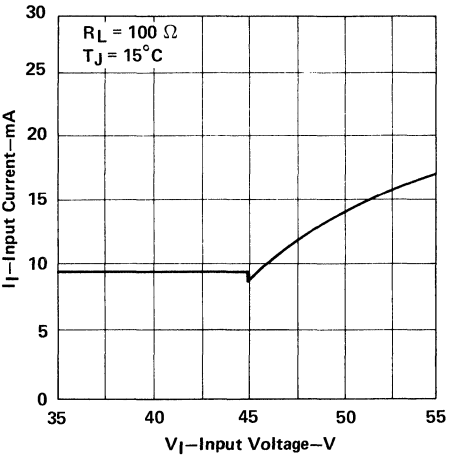

FIGURE 12

LINE TRANSIENT RESPONSE

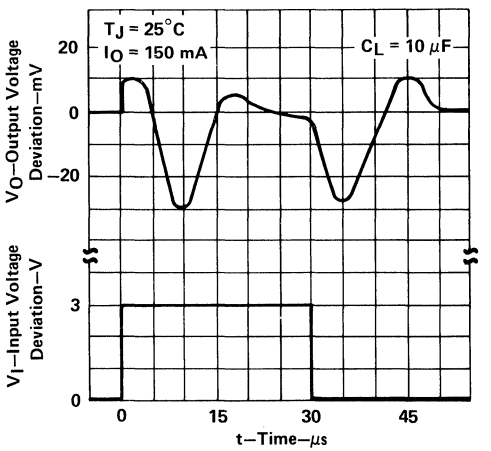

FIGURE 13

INPUT CURRENT
vs
REVERSE INPUT VOLTAGE

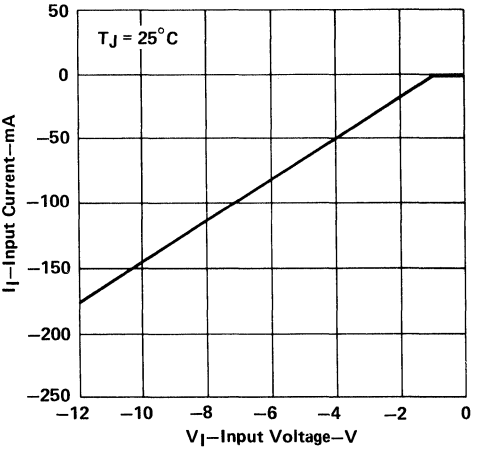

FIGURE 14

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
REVERSE INPUT VOLTAGE

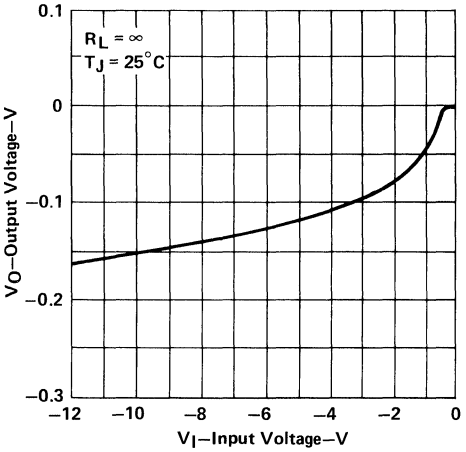


FIGURE 15

LOAD TRANSIENT RESPONSE

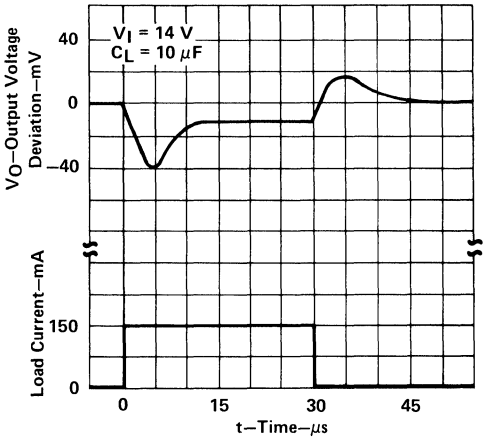


FIGURE 16

BIAS CURRENT
vs
OUTPUT CURRENT

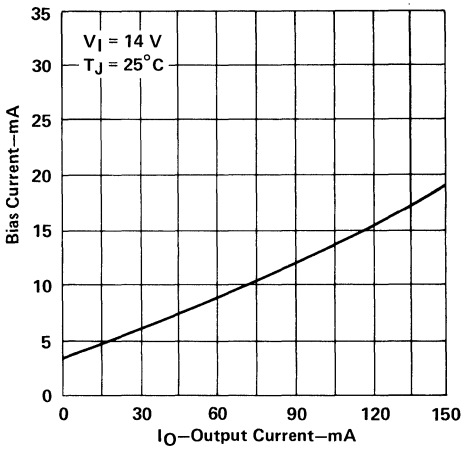


FIGURE 17

TYPICAL CHARACTERISTICS

BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

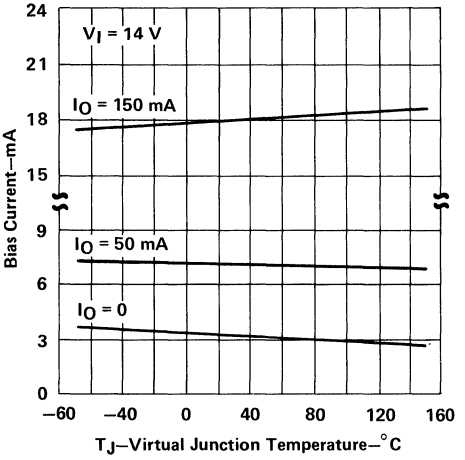


FIGURE 18

BIAS CURRENT
vs
INPUT VOLTAGE

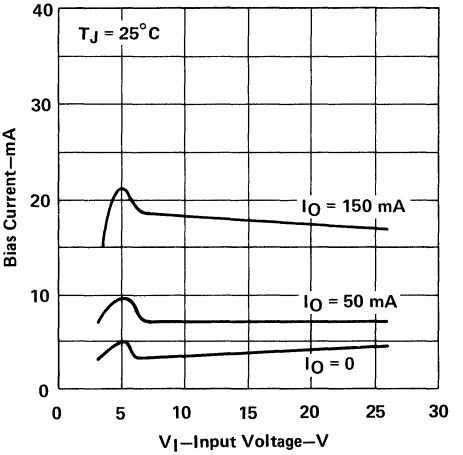
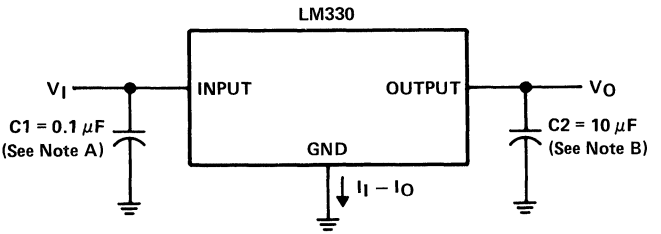


FIGURE 19

TYPICAL APPLICATION DATA



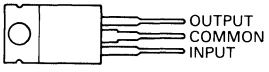
NOTES: A. Use of C1 is required if the regulator is not located in close proximity to the supply filter.
B. Capacitor C2 must be located as close as possible to the regulator and may be an aluminum or tantalum type capacitor. The minimum capacitance that will provide stability is 10-μF. The capacitor must be rated for operation at −40 °C to assure stability to that extreme.

FIGURE 20

D2733 APRIL 1983—REVISED JUNE 1988

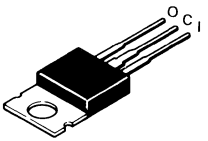
- **Input-Output Differential Less than 0.6 V**
- **Output Current of 150 mA**
- **Reverse Battery Protection**
- **Line Transient Protection**
- **40-V Load-Dump Protection**
- **Internal Short Circuit Current Limiting**
- **Internal Thermal Overload Protection**
- **Mirror-Image Insertion Protection**
- **Direct Replacement for National LM2930 Series**

KC PACKAGE
(TOP VIEW)

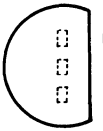


THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



LP
SILECT PACKAGE
(TOP VIEW)



TO-226AA

OCI

description

The LM2930-5 and LM2930-8 are 3-terminal positive regulators that provide fixed 5-V and 8-V regulated outputs. Each features the ability to source 150 mA of output current with an input-output differential of 0.6 V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

The LM2930 series has low voltage dropout making it useful for certain battery applications. For example, the low voltage dropout feature allows a longer battery discharge before the output falls out of regulation; the battery supplying the regulator input voltage may discharge to 5.6 V and still properly regulate the system and load voltage. Supporting this feature, the LM2930 series protects both itself and the regulated system from reverse battery installation or 2-battery jumps.

Other protection features include line transient protection for load-dump of up to 40 V. In this case, the regulator shuts down to avoid damaging internal and external circuits. The LM2930 series regulator cannot be harmed by temporary mirror-image insertion.

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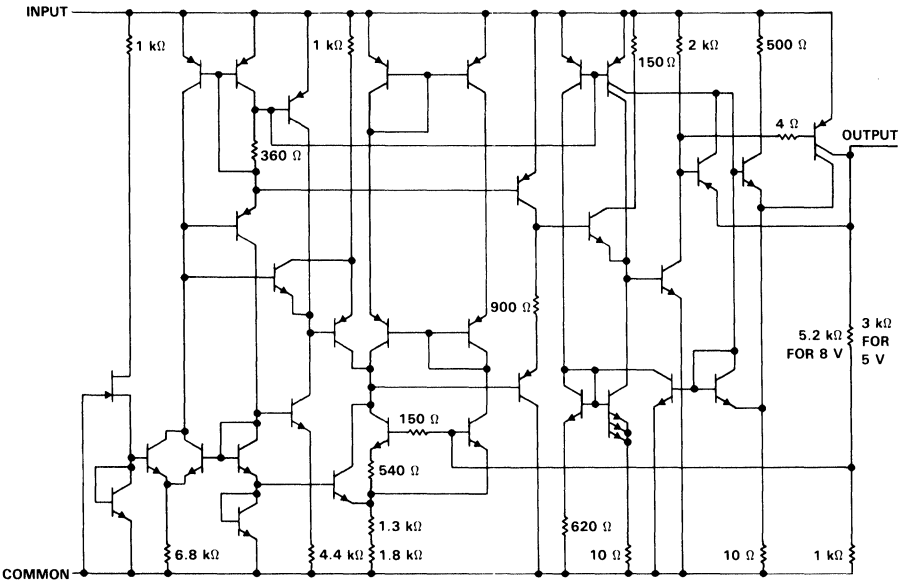
schematic diagram



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage	26 V
Transient input voltage: t = 1 s	40 V
Continuous reverse input voltage	−6 V
Transient reverse input voltage: t = 100 ms	−12 V
Continuous total dissipation (see Note 1)	See Dissipation Rating Table 1
Continuous total dissipation (see Note 1)	See Dissipation Rating Table 2
Operating free-air, case, or virtual junction temperature	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1—FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
KC	2000 mW	16 mW/°C	25°C	1280 mW
LP	775 mW	6.2 mW/°C	25°C	496 mW

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
KC	20 W	0.25 W/°C	70°C	6.25 W
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
I_O	Output current		150	mA
T_J	Operating virtual junction temperature	−40	125	°C

LM2930-5 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	4.5	5	5.5	V
Input regulation	I_O = 5 mA	V_I = 9 V to 16 V		7	25	mV
		V_I = 6 V to 26 V		30	80	
Ripple rejection	f = 120 Hz			56		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 125°C			20		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			60		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		5.5	V
Output impedance	I_O = 100 mA, I_O = 10 mA (rms), 100 Hz to 10 kHz			200		MΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor across the output.

‡Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is intended to be an engineering estimate of the average drift to be expected from lot to lot.

LM2930-8 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA, (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	7.2	8	8.8	V
Input regulation	I_O = 5 mA	V_I = 9.4 V to 16 V		12	50	mV
		V_I = 9.4 V to 26 V		50	100	
Ripple rejection	f = 120 Hz			52		dB
Output regulation	I_O = 5 mA to 150 mA			25	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 125°C			30		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			90		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		8.8	V
Output impedance	I_O = 100 mA, I_O = 10 mA (rms), f = 100 Hz to 10 kHz			300		MΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor across the output.

‡Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is intended to be an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

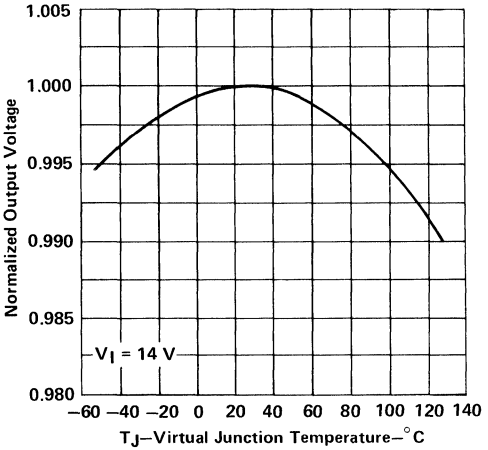


FIGURE 1

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

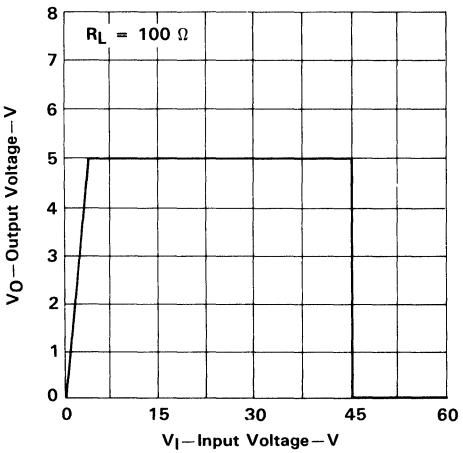


FIGURE 2

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TYPICAL CHARACTERISTICS

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

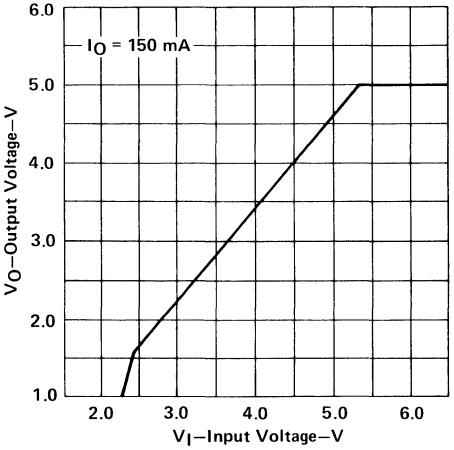

FIGURE 3

RIPPLE REJECTION
vs
FREQUENCY

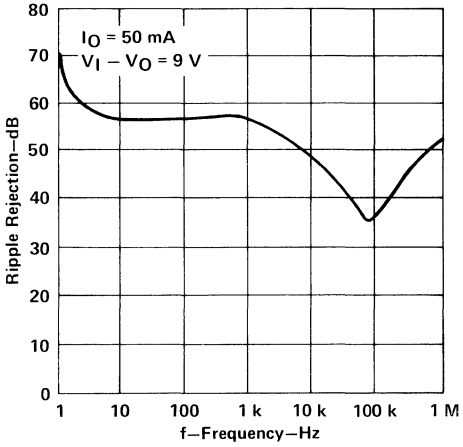

FIGURE 4

RIPPLE REJECTION
vs
OUTPUT CURRENT

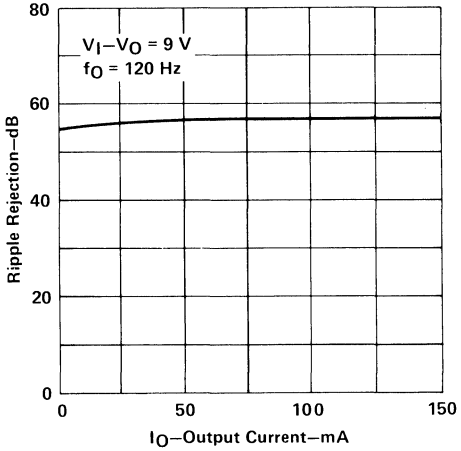

FIGURE 5

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

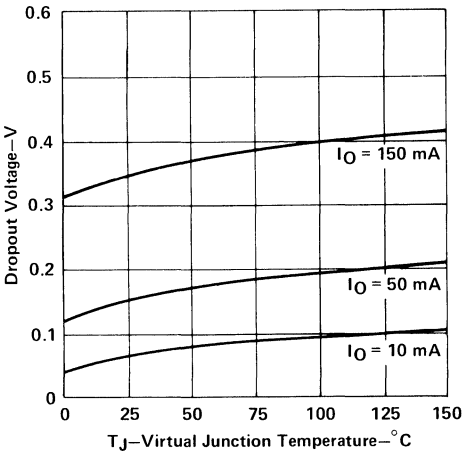

FIGURE 6

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

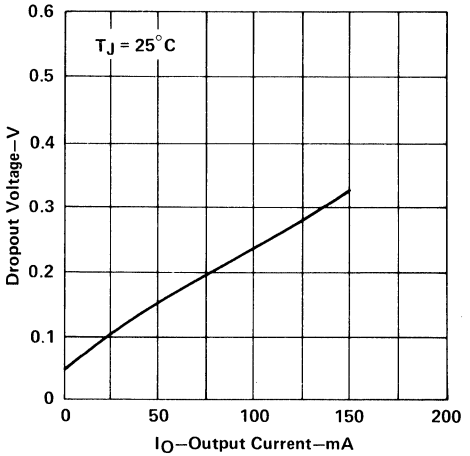

FIGURE 7

OUTPUT IMPEDANCE
vs
FREQUENCY

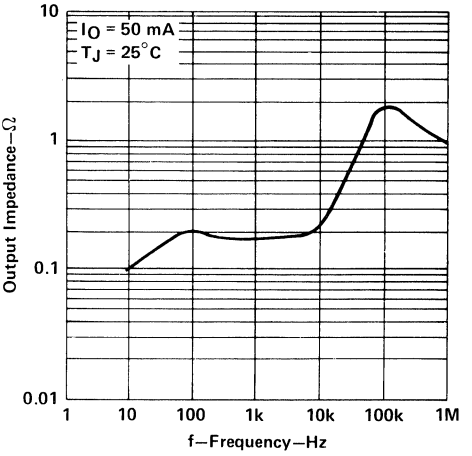

FIGURE 8

INPUT CURRENT
vs
INPUT VOLTAGE

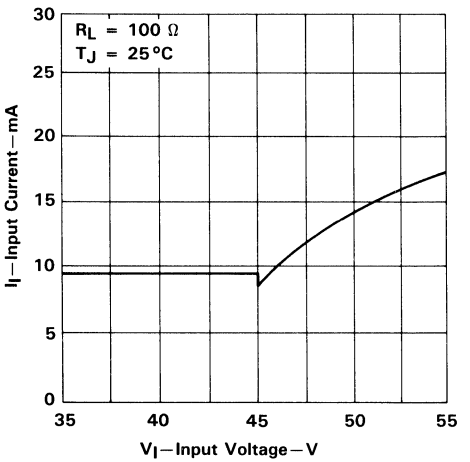

FIGURE 9

LINE TRANSIENT RESPONSE

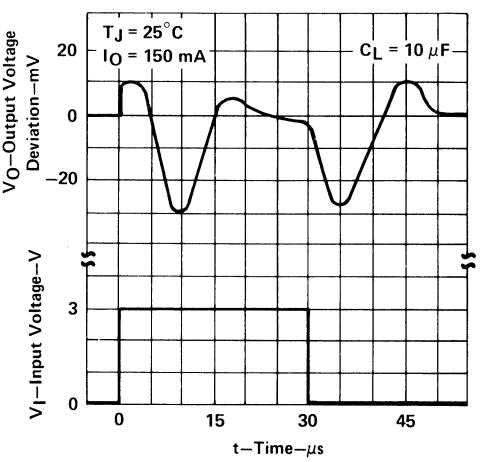

FIGURE 10

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
REVERSE INPUT VOLTAGE

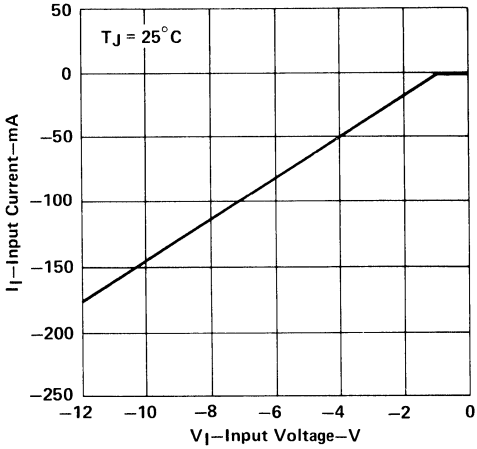


FIGURE 11

OUTPUT VOLTAGE
vs
REVERSE INPUT VOLTAGE

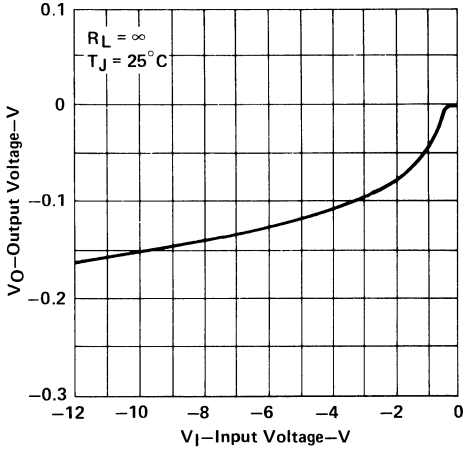


FIGURE 12

LOAD TRANSIENT RESPONSE

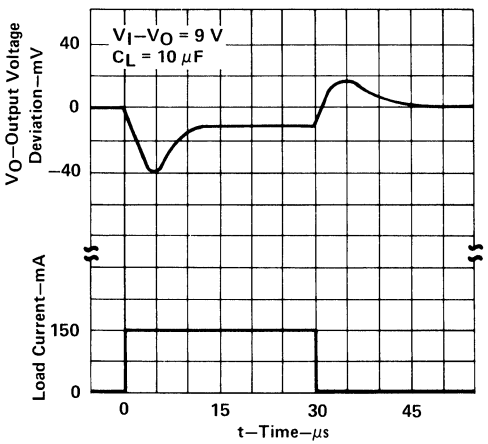


FIGURE 13

BIAS CURRENT
vs
OUTPUT CURRENT

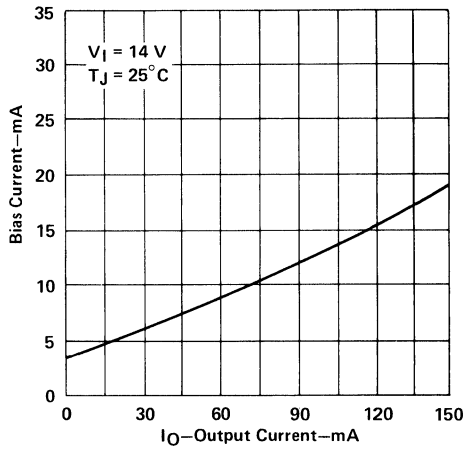


FIGURE 14

TYPICAL CHARACTERISTICS

BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

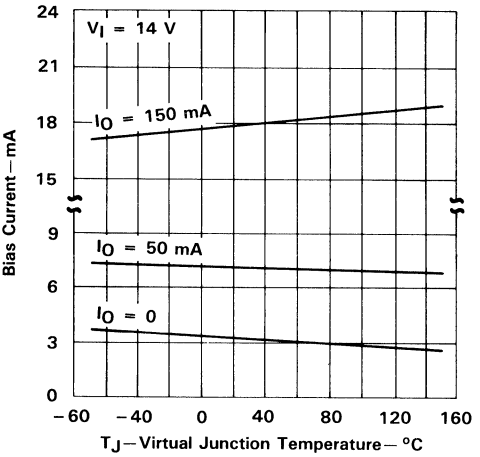


FIGURE 15

LM2905-5
BIAS CURRENT
vs
INPUT VOLTAGE

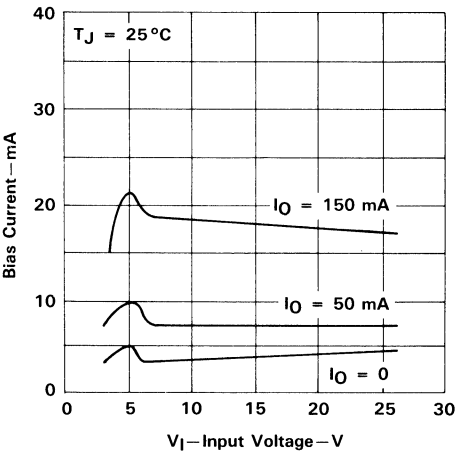
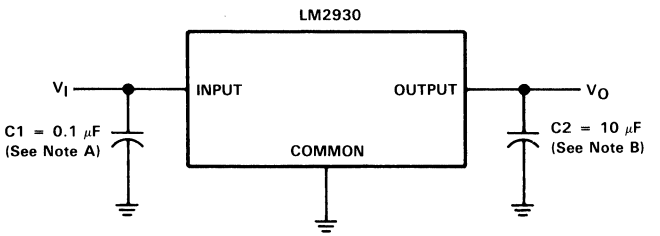


FIGURE 16

TYPICAL APPLICATION DATA



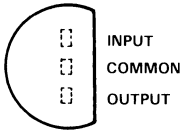
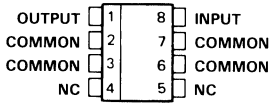
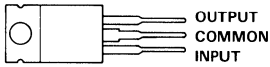
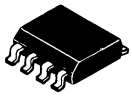
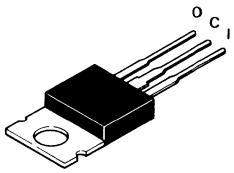
NOTES: A. Use of C1 is required if the regulator is not located in close proximity to the supply filter.
B. Capacitor C2 must be located as close as possible to the regulator and may be an aluminum or tantalum type capacitor. The minimum value required for stability is 10 μF. The capacitor must be rated for operation at −40°C to guarantee stability to that extreme.

FIGURE 17

LM2931-5AQ
3-TERMINAL POSITIVE VOLTAGE REGULATOR

D2828, AUGUST 1988—REVISED OCTOBER 1988

- Input-Output Differential Less than 0.6 V
- Output Current of 150 mA
- Reverse Battery Protection
- Very Low Quiescent Current
- 60-V Load-Dump Protection
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Mirror-Image Insertion Protection
- Reverse Transient Protection
- Direct Improved Replacement for National LM2931-5 and LM2931A-5

LP SILECT PACKAGE	D SMALL-OUTLINE PACKAGE	KC PACKAGE
(TOP VIEW)  TO-226AA	(TOP VIEW)  	(TOP VIEW)  THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE TO-220AB
 OCI		

description

The LM2931-5AQ is a 3-terminal positive voltage regulator that provides a 5-V regulated output. It features the ability to source 150 mA of output current with an input-output differential of 0.6 V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

This device also has a low dropout voltage making it useful for certain battery applications. For example, because the low dropout voltage allows a longer battery discharge before the output falls out of regulation, the battery supplying the regulator input voltage may discharge to 5.6 V and still properly regulate the 5-V load voltage. Supporting this feature, the LM2931-5AQ protects both itself and the regulated system from reverse battery installation or 2-battery jumps. The very low quiescent current feature is especially useful in battery-powered applications.

Other protection features include line transient protection from load-dump of up to 60 V. In this case, the regulator shuts down to avoid damaging internal and external circuits. The LM2931-5AQ regulator is virtually immune to temporary mirror-image insertion.

The Q suffix indicates that the device is characterized for operation from −40°C to 125°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating junction temperature range (unless otherwise noted)

Continuous input voltage . . . . . 26 V
Transient input voltage: t = 1 s . . . . . 60 V
Continuous reverse input voltage . . . . . −15 V
Transient reverse input voltage: t = 100 ms . . . . . −50 V
Continuous total dissipation (see Note 1) . . . . . See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 — FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
D	825 mW	6.6 mW/°C	165 mW
KC	2000 mW	16 mW/°C	400 mW
LP	775 mW	6.2 mW/°C	155 mW

DISSIPATION RATING TABLE 2 — CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.4 mW/°C	96°C	735 mW
KC	20 W	0.18 W/°C	39°C	4.5 W
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

	MIN	MAX	UNIT
Output current, I_O		150	mA
Operating virtual junction temperature, T_J	−40	125	°C

electrical characteristics at 25°C virtual junction temperature, V_I = 14 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, $I_O \leq$ 150 mA, T_J = −40°C to 125°C		4.75	5	5.25	V
Input regulation	I_O = 10 mA	V_I = 9 V to 16 V		2	10	mV
		V_I = 6 V to 26 V		4	30	
Ripple rejection	I_O = 10 mA, f = 120 hz		60	80		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	I_O = 10 mA, After 1000 h at T_J = 125°C			20		mV
Dropout voltage	I_O = 10 mA			0.05	0.2	V
	I_O = 150 mA			0.3	0.6	
Output noise voltage	I_O = 10 mA, f = 10 Hz to 100 kHz			500		μV rms
Bias current	V_I = 6 V to 26 V, I_O = 10 mA, T_J = = −40°C to 125°C			0.4	1	mA
	V_I = 14 V, I_O = 150 mA, T_J = 25°C			10	12	

† Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input to common and a 100-μF capacitor, with equivalent series resistance of less then 1 Ω, across the output to common.
‡ Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3190, JANUARY 1989

- **Initial Accuracy . . .**
  ±4 mV for LT1004-1.2
  ±20 mV for LT1004-2.5
- **Micropower Operation**
- **Operates Up to 20 mA**
- **Very Low Reference Impedance**
- **Applications:**
  Portable Meter References
  Portable Test Instruments
  Battery Operated Systems
  Current-Loop Instrumentation

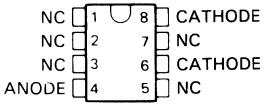
Description

The LT1004 micropower voltage references are two-terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimizing the key parameters in the design, processing, and testing of the devices results in specifications previously attainable only with selected units.

The LT1004 is a pin-for-pin replacement for the LM185 series of references with improved specifications. The LT1004 is an attractive device for use in systems in which accuracy was previously attained at the expense of power consumption and trimming.

The LT1004M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1004C is characterized for operation from 0°C to 70°C.

LT1004C . . . D PACKAGE
(TOP VIEW)



NC – No internal connection

LT1004M, LT1004C . . . LD PACKAGE
(TOP VIEW)

The anode is in electrical contact with the case.

LT1004C . . . LP PACKAGE
(TOP VIEW)

NC – No internal connection

symbol

AVAILABLE OPTIONS

T_A	NOM V_Z	PACKAGE		
		SMALL OUTLINE (D)	METAL CAN (LD)	PLASTIC (LP)
0°C to 70°C	1.2 V	LT1004CD-1.2	LT1004CLD-1.2	LT1004CLP-1.2
	2.5 V	LT1004CD-2.5	LT1004CLD-2.5	LT1004CLP-2.5
−55°C to 125°C	1.2 V		LT1004MLD-1.2	
	2.5 V		LT1004MLD-2.5	

The D package is available taped and reeled. Add suffix R to the device type (i.e., LT1004CDR0.

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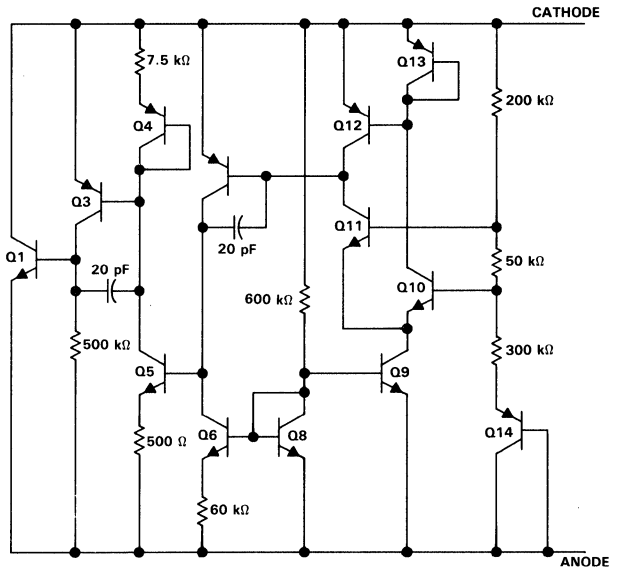
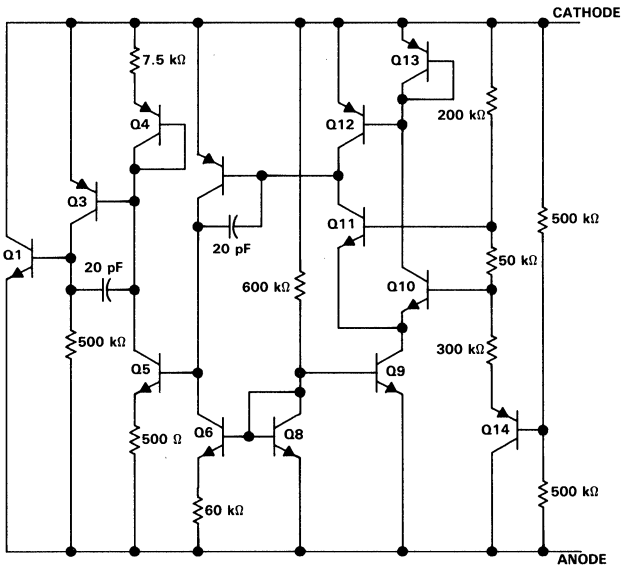
schematic

LT1004-1.2



LT1004-2.5



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current . . . . . 30 mA
Forward current . . . . . 10 mA
Operating free-air temperature range: LT1004M . . . . . −55°C to 125°C
LT1004C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: LD package . . . . . 300°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LT1004-1.2			LT1004-2.5			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 100 µA, See Note 1	25°C	1.231	1.235	1.239	2.48	2.5	2.52	V
			0°C to 70°C	1.225		1.245	2.47		2.53	
			−55°C to 125°C	1.22		1.245	2.46		2.535	
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 10 µA	25°C		20					ppm/°C
		I_Z = 20 µA						20		
ΔV_Z	Change in reference voltage with current	I_Z = 10 µA to 1 mA	25°C			1			1	mV
			Full range			1.5			1.5	
		I_Z = 1 mA to 20 mA	25°C			10			10	
			Full range			20			20	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 µA	25°C		20			20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range		8	10		12	20	µA
Z_Z	Reference impedance	I_Z = 100 µA	25°C		0.2	0.6		0.2	0.6	Ω
			Full range			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 µA, f = 10 Hz to 10 kHz	25°C		60			120		µV

† Full range is −55°C to 125°C for the LT1004M and 0°C to 70°C for the LT1004C.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.
NOTE 1: The 0°C to 70°C limits apply for both M- and C-suffix devices. The −55°C to 125°C limits apply only for M-suffix devices.

TYPICAL CHARACTERISTICS†

REVERSE CHARACTERISTICS

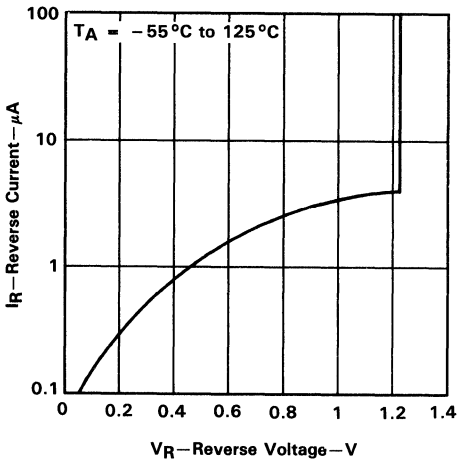


FIGURE 1

REFERENCE VOLTAGE CHANGE
vs
REVERSE CURRENT

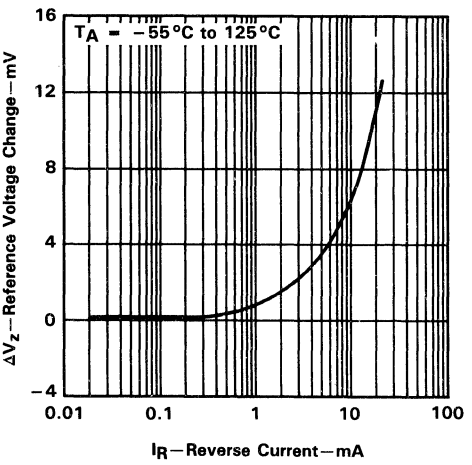


FIGURE 2

FORWARD CHARACTERISTICS

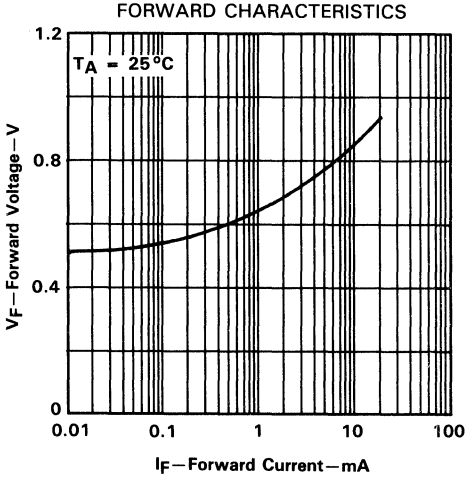


FIGURE 3

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

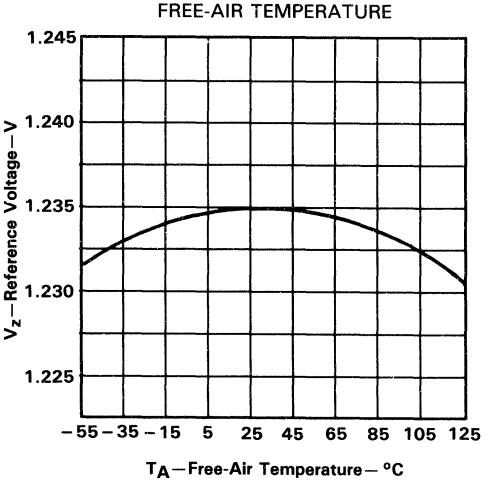


FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

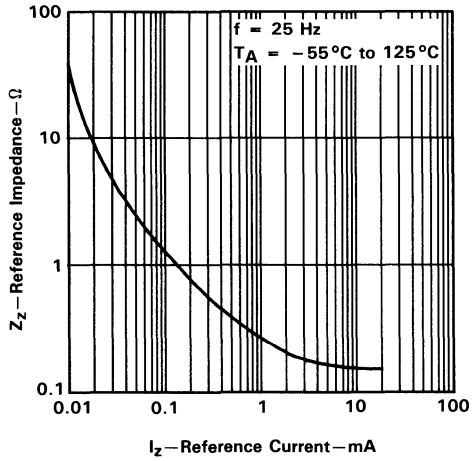


FIGURE 5

REFERENCE IMPEDANCE
vs
FREQUENCY

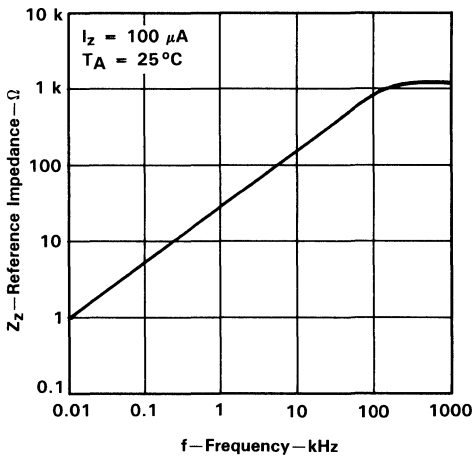


FIGURE 6

NOISE VOLTAGE
vs
FREQUENCY

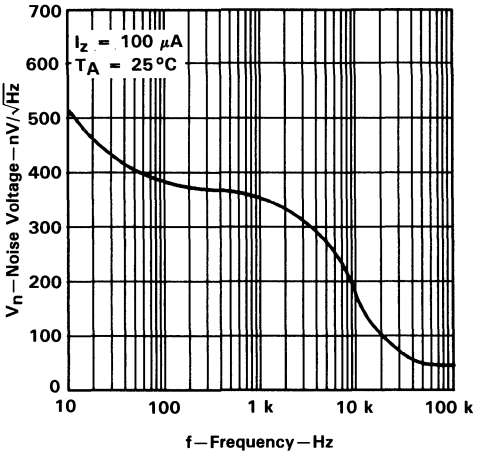


FIGURE 7

OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

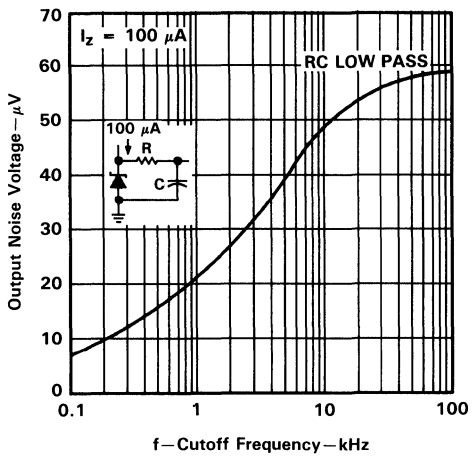


FIGURE 8

TYPICAL CHARACTERISTICS†

REVERSE CHARACTERISTICS

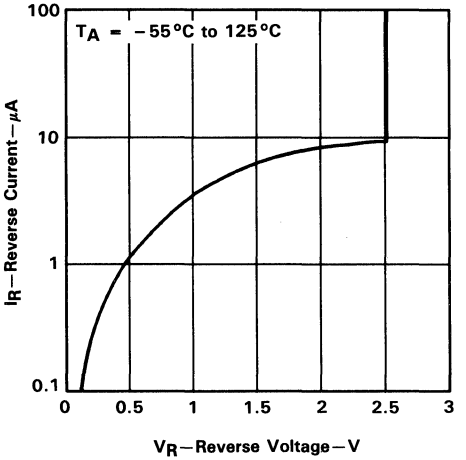


FIGURE 9

FORWARD CHARACTERISTICS

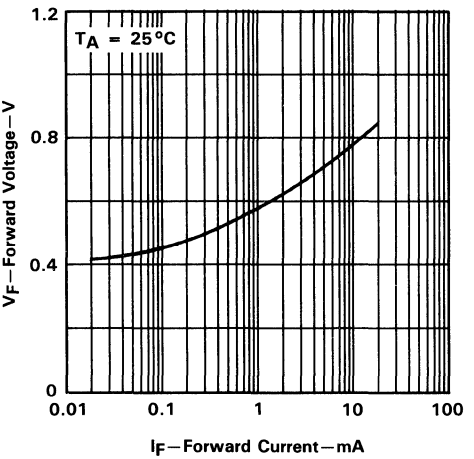


FIGURE 10

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

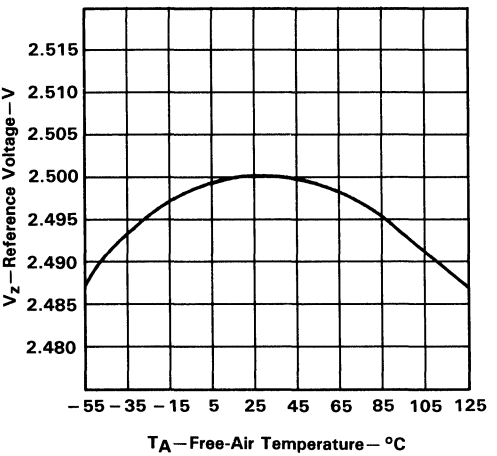


FIGURE 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

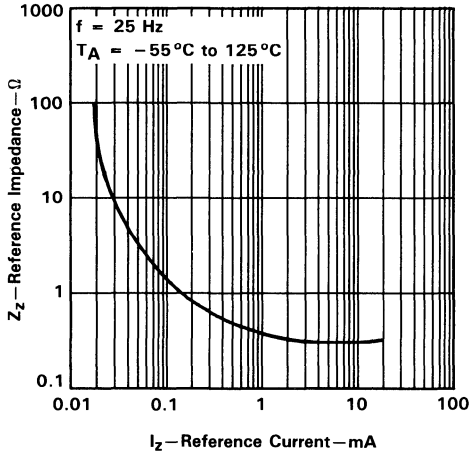


FIGURE 12

REFERENCE IMPEDANCE
vs
FREQUENCY

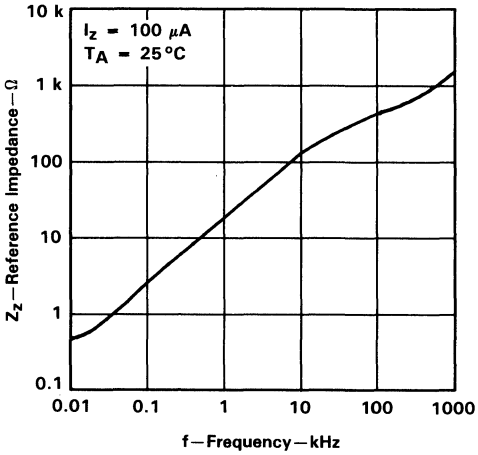


FIGURE 13

NOISE VOLTAGE
vs
FREQUENCY

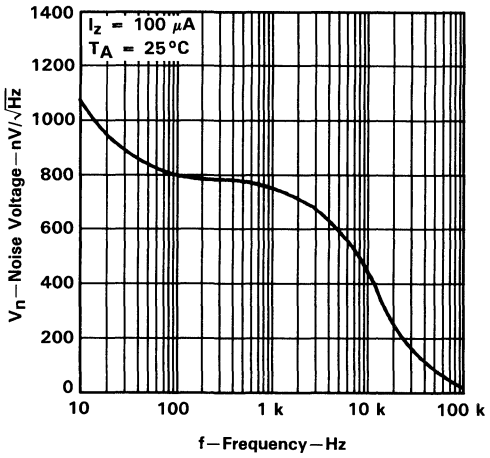


FIGURE 14

FILTERED OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

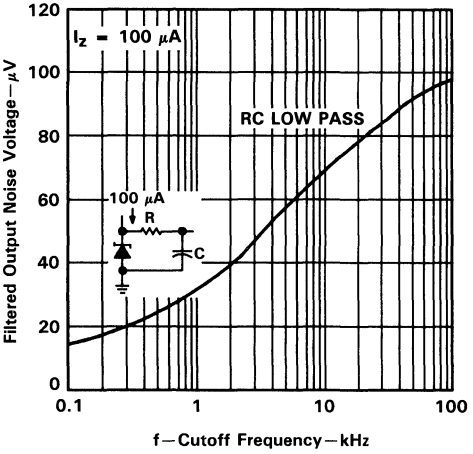


FIGURE 15

TYPICAL CHARACTERISTICS

LT1004-1.2
TRANSIENT RESPONSE

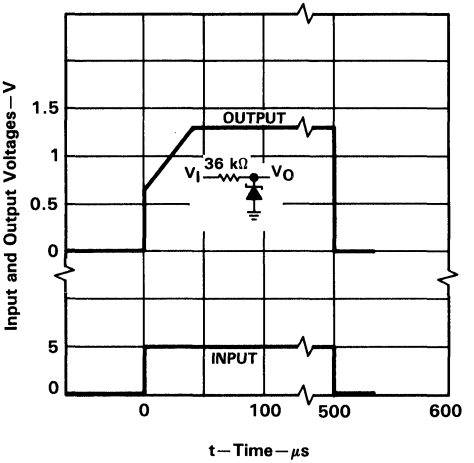


FIGURE 16

LT1004-2.5
TRANSIENT RESPONSE

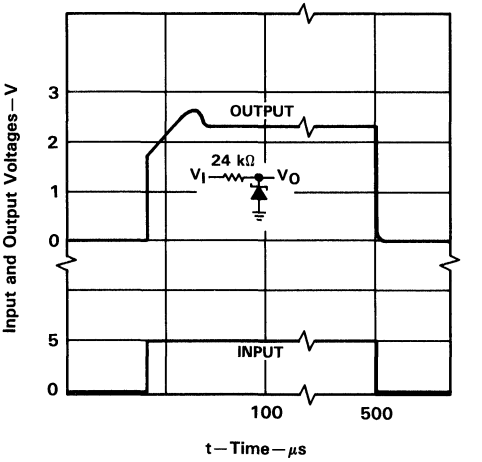
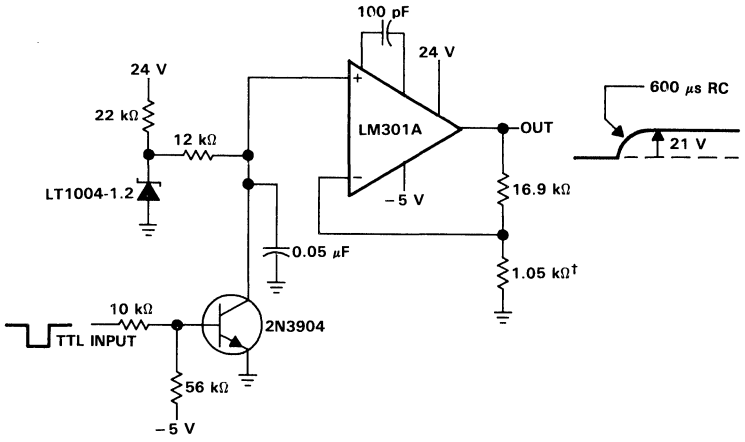


FIGURE 17

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA



† 1% metal film resistors

FIGURE 18. V_{PP} GENERATOR FOR EPROMS (NO TRIM REQUIRED)

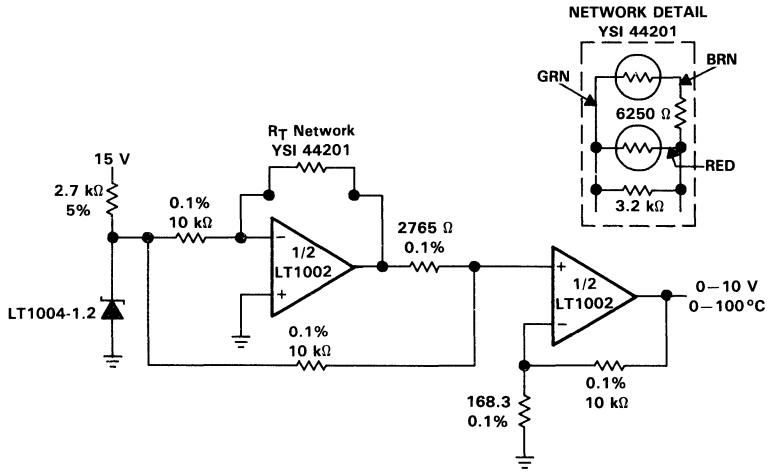


FIGURE 19. 0°C TO 100°C LINEAR OUTPUT THERMOMETER

TYPICAL APPLICATION DATA

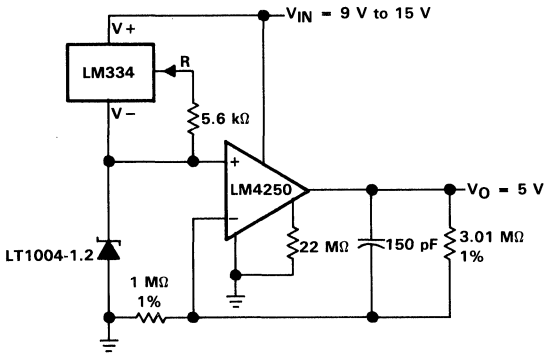


FIGURE 20. MICROPOWER 5-V REFERENCE

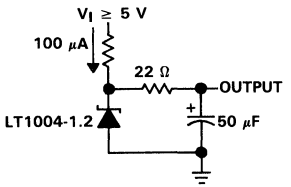


FIGURE 21. LOW-NOISE REFERENCE

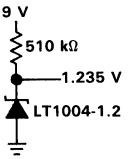
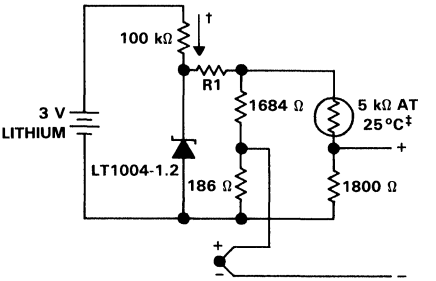


FIGURE 22. MICROPOWER REFERENCE FROM 9-V BATTERY



THERMOCOUPLE TYPE	R1
J	233 kΩ
K	299 kΩ
T	300 kΩ
S	2.1 MΩ

† Quiescent current ≅ 15 μA
‡ Yellow Springs Inst. Co., Part #44007
NOTE: This application compensates within ±1°C from 0°C to 60°C.

FIGURE 23. MICROPOWER COLD-JUNCTION COMPENSATION FOR THERMOCOUPLES

TYPICAL APPLICATION DATA

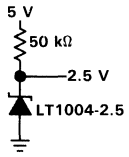


FIGURE 24. 2.5-V REFERENCE

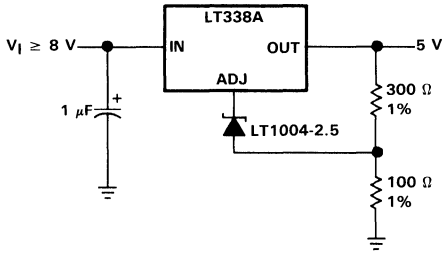
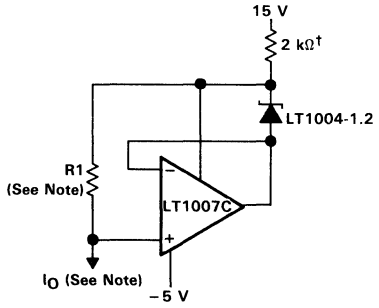


FIGURE 27. HIGH-STABILITY 5-V REGULATOR



† May be increased for small output currents.

NOTE: $R1 \approx \frac{2\ V}{I_O + 10\ \mu A}$, $I_O = \frac{1.235\ V}{R1}$.

FIGURE 25. GROUND-REFERENCED CURRENT SOURCE

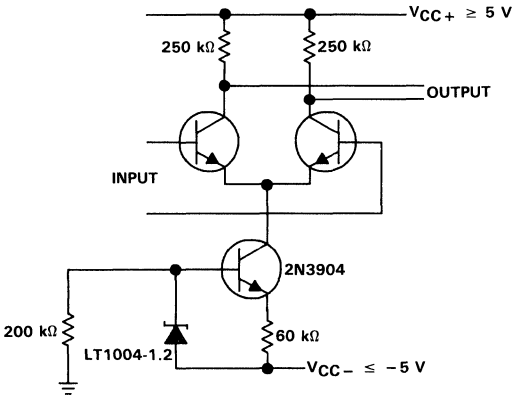
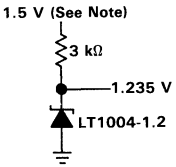
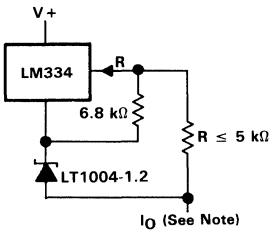


FIGURE 28. AMPLIFIER WITH CONSTANT GAIN OVER TEMPERATURE



NOTE: Output regulates down to 1.285 V for $I_O = 0$.

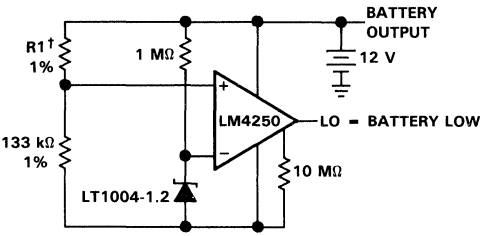
FIGURE 26. 1.2-V REFERENCE FROM 1.5-V BATTERY



NOTE: $I_O \approx \frac{1.3\ V}{R}$

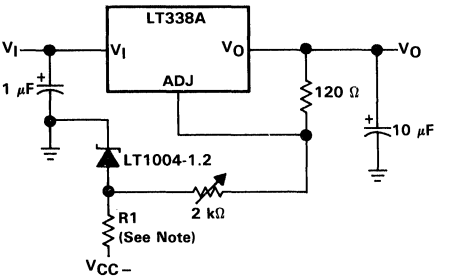
FIGURE 29. 2-TERMINAL CURRENT SOURCE WITH LOW TEMPERATURE COEFFICIENT

TYPICAL APPLICATION DATA



† R1 sets trip point, 60.4 kΩ per cell for 1.8 V per cell.

FIGURE 30. LEAD-ACID LOW-BATTERY-VOLTAGE DETECTOR



NOTE: $R1 \leq \frac{V_{CC} - 1\ V}{0.015}$

FIGURE 31. VARIABLE-VOLTAGE SUPPLY

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3191, MAY 1987—REVISED JANUARY 1989

- **Excellent Temperature Stability**
- **Initial Tolerance . . . 0.2% Max**
- **Dynamic Impedance . . . 0.6 Ω Max**
- **Wide Operating Current Range**
- **Directly Interchangeable with LM136**
- **Needs No Adjustment for Minimum Temperature Coefficient**

description

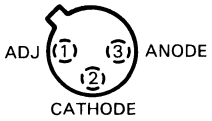
The LT1009 is a precision trimmed 2.5-V shunt regulator featuring a maximum initial tolerance of only ±5 mV, low dynamic impedance, and a wide operating current range. The 0.2% reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient α_{VZ}.

Even though the LT1009 needs no adjustments, a third terminal allows the reference voltage to be adjusted 5% to eliminate system errors. In many applications, the LT1009 can be used as a pin-for-pin replacement for the LM136H-2.5, which eliminates the external trim network.

The uses of the LT1009 include a 5-V system reference, an 8-bit ADC and DAC reference, or a power supply monitor. The LT1009 can also be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1009C is characterized for operation from 0°C to 70°C.

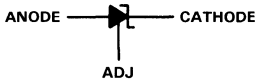
LT1009M, LT1009C . . . LD PACKAGE
(TOP VIEW)



The anode is in electrical contact with the case.

LT1009C . . . LP PACKAGE
(TOP VIEW)

symbol



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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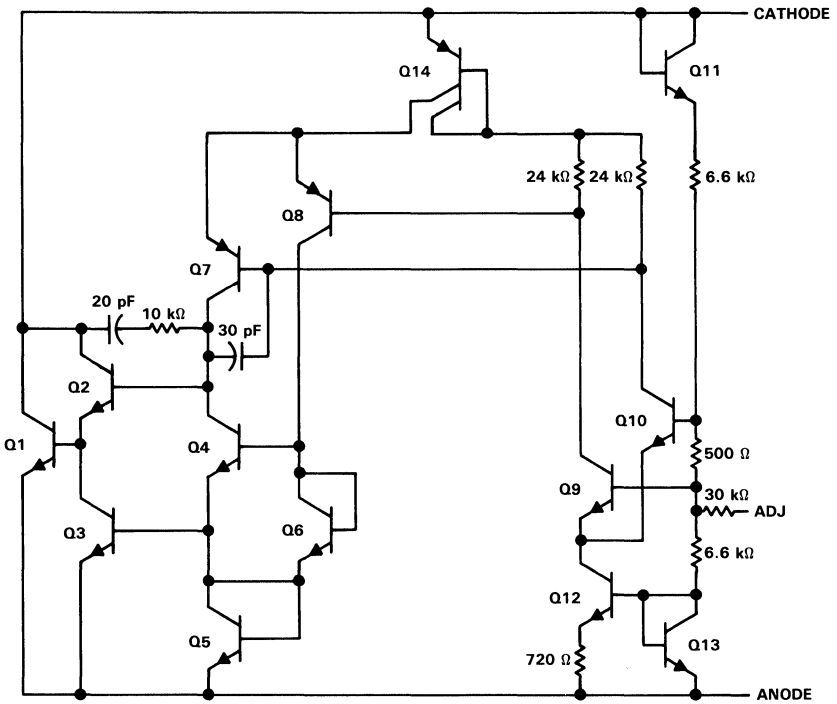
schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current . . . . . 20 mA
Forward current . . . . . 10 mA
Operating free-air temperature range: LT1009M . . . . . −55°C to 125°C
LT1009C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: LD package . . . . . 300°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LT1009M			LT1009C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	25°C	2.495	2.5	2.505	2.495	2.5	2.505	V
$\Delta V_{Z(temp)}$	Change in reference voltage with temperature		MIN to MAX			15			4	mV
α_{VZ}	Average temperature coefficient of reference voltage‡		0°C to 70°C		15	25		15	25	ppm/°C
			−55°C to 125°C		25	35				
ΔV_Z	Change in reference voltage with current	I_Z = 400 μA to 10 mA	25°C		2.6	6		2.6	10	mV
			Full range			10			12	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 1 mA	25°C		20			20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA	25°C		0.3	0.6		0.3	1	Ω
			Full range			1			1.4	

† Full range is −55°C to 125°C for the LT1009M and 0°C to 70°C for the LT1009C.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

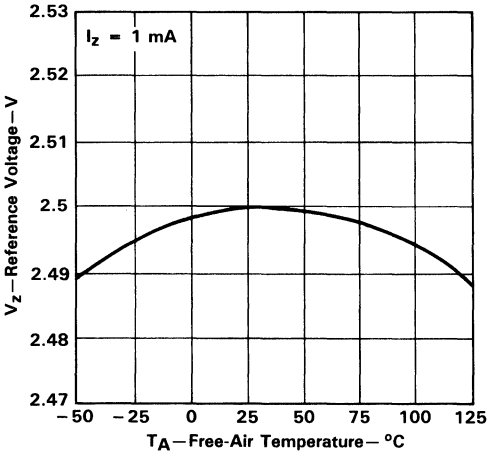


FIGURE 1

CHANGE IN REFERENCE VOLTAGE
vs
REFERENCE CURRENT

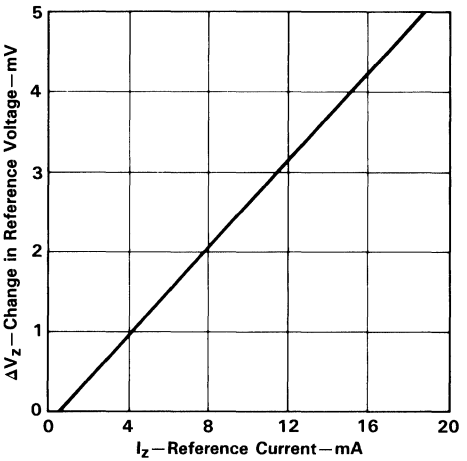


FIGURE 2

REVERSE CHARACTERISTICS

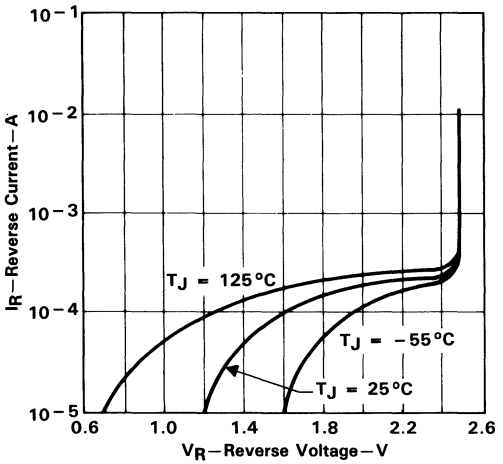


FIGURE 3

FORWARD CHARACTERISTICS

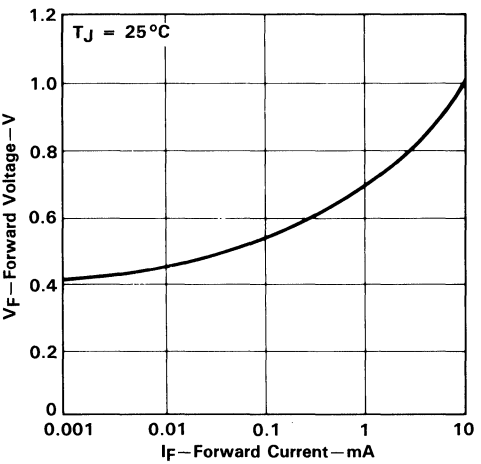


FIGURE 4

† Data at the high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

REFERENCE IMPEDANCE
vs
FREQUENCY

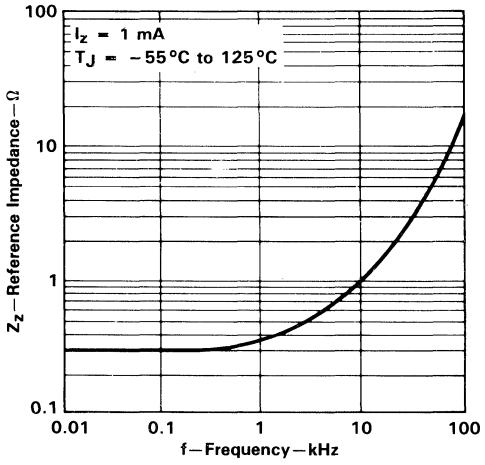


FIGURE 5

NOISE VOLTAGE
vs
FREQUENCY

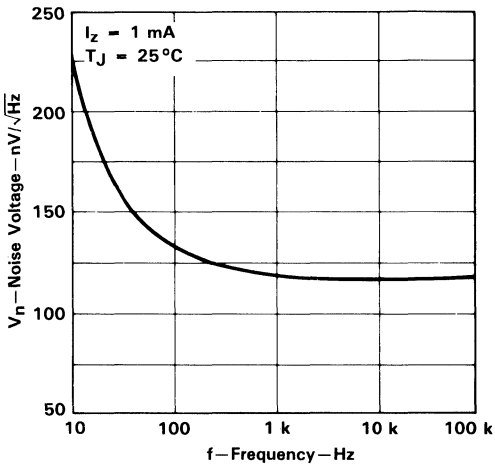


FIGURE 6

TRANSIENT RESPONSE

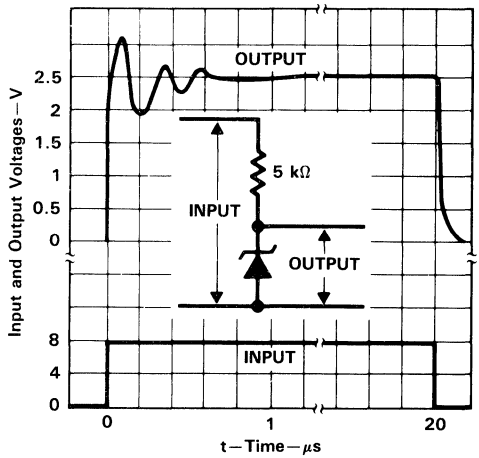
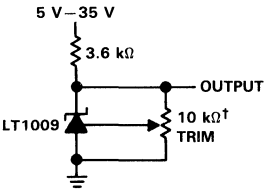


FIGURE 7

TYPICAL APPLICATION DATA



† Does not affect temperature coefficient. Provides ±5% trim range.

FIGURE 8. 2.5-V REFERENCE

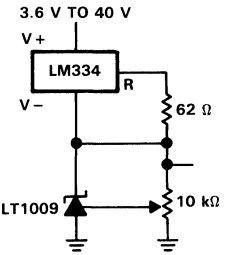


FIGURE 9. ADJUSTABLE REFERENCE WITH WIDE-SUPPLY RANGE

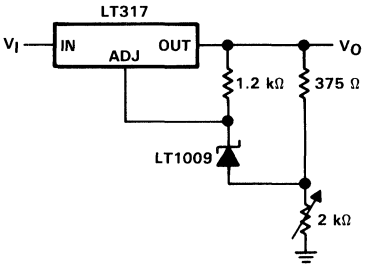


FIGURE 10. POWER REGULATOR WITH LOW TEMPERATURE COEFFICIENT

TYPICAL APPLICATION DATA

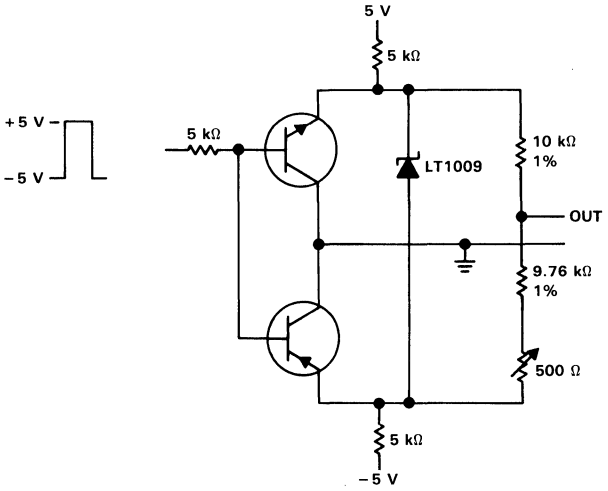


FIGURE 11. SWITCHABLE ±1.25-V BIPOLAR REFERENCE

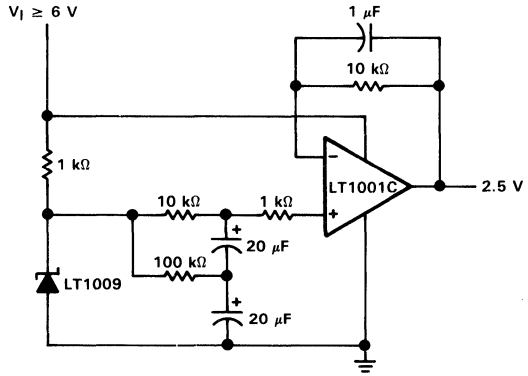
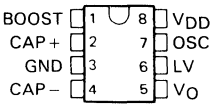


FIGURE 12. LOW-NOISE 2.5-V BUFFERED REFERENCE

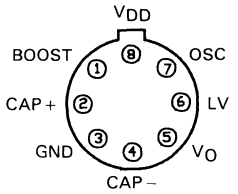
D3193, JANUARY 1989

- Plug-In Compatible with the 7660 with These Additional Features:
  - Operation to 9 V Over Full Temperature Range with No External Protection Diodes
  - Boost Pin for Higher Switching Frequency
  - 2 1/2 Times Lower Quiescent Power
  - Efficient Voltage Doubler
- No-Load Supply Current at 5 V . . . 200 μA Max
- Open-Circuit Voltage Conversion Efficiency . . . 97% Min
- Power Conversion Efficiency . . . 95% Min
- Operating Supply Voltage Range . . . 1.5 V to 9 V
- Commercial Device Operates from −40°C to 85°C

LTC1044M . . . JG PACKAGE
LTC1044C . . . D, JG, OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



description

The LTC1044 is a monolithic CMOS switched-capacitor voltage converter manufactured using CMOS silicon-gate technology. The LTC1044 provides several voltage conversion functions; the input voltage can be inverted ($V_O = -V_I$), doubled ($V_O = 2V_I$), divided ($V_O = V_I/2$), or multiplied ($V_O = \pm nV_I$).

Designed to be pin-for-pin and functionally compatible with the 7660, the LTC1044 offers significant new design and performance advantages while still maintaining compatibility with existing 7660 designs.

The LTC1044M is characterized for operation over the full military temperature range of −55°C to 125°C. The LTC1044C is characterized for operation from −40°C to 85°C.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{DD} . . . . . 9.5 V
Input voltage range (pins 1, 6, and 7, see Note 1) . . . . . −0.3 V to V_{DD} + 0.3 V
Input current, I_I (pin 6) . . . . . 20 μA
Duration of output short circuit ($V_{CC+} \leq 5.5$ V) . . . . . unlimited
Operating free-air temperature range: LTC1044M . . . . . −55°C to 125°C
LTC1044C . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
L package . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		LTC1044M		LTC1044C		UNIT
		MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage (R_L = 10 kΩ, see Note 1)	1.5	9	1.5	9	V
V_I	Input voltage (pins 1, 6, and 7, see Note 2)	−0.3	V_{DD}+0.3	−0.3	V_{DD}+0.3	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 1. The LTC1044 operates with alkaline, mercury, or NiCad 9-V batteries, even when the initial battery voltage is slightly higher than 9 V.
2. Connecting any input terminal to voltages substantially greater than V_{DD} or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted, see Figure 1)

PARAMETER		TEST CONDITIONS	T_A†	LTC1044M			LTC1044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
r_o	Output resistance	I_O = 20 mA, f_{osc} = 5 kHz	25°C			100			100	Ω
			Full range			150			130	
		V_{DD} = 2 V, I_L = 3 mA, f_{osc} = 1 kHz	Full range			400			325	
f_{osc}	Oscillator frequency	V_{DD} = 5 V, C_{osc} = 1 pF, See Note 3	Full range	5			5			kHz
		V_{DD} = 2 V, C_{osc} = 1 pF, See Note 3		1			1			
η_P	Power efficiency	R_L = 5 kΩ, f_{osc} = 5 kHz	25°C	95	98		95	98		%
η_{VO}	Voltage conversion efficiency	R_L = ∞	25°C	97	99.9		97	99.9		%
I_{osc}	Oscillator sink or source current	V_{osc} = 0 or V_{DD}, Pin 1 at 0 V	Full range			3			3	μA
		V_{osc} = 0 or V_{DD}, Pin 1 at V_{DD}				20			20	
I_{DD}	Supply current	R_L = ∞, Pins 1 and 7 no connection	25°C		60	200		60	200	μA
		R_L = ∞, Pins 1 and 7 V_{DD} = 3 V			20			20		

† Full range is −55°C to 125°C for the LTC1044M and −40°C to 85°C for the LTC1044C.

NOTE 3: f_{osc} is tested with C_{osc} at 100 pF to minimize the effects of test fixture capacitance loading. The 1-pF frequency is correlated to this 100-pF test point and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

PARAMETER MEASUREMENT INFORMATION

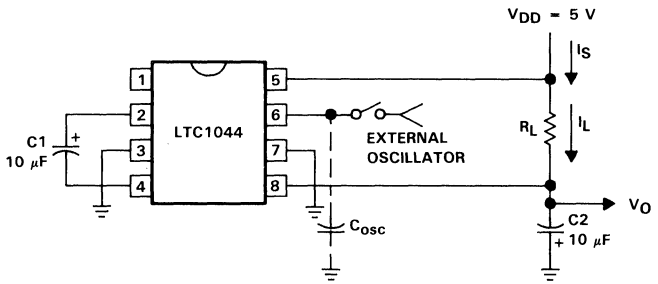

FIGURE 1. TEST CIRCUIT

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

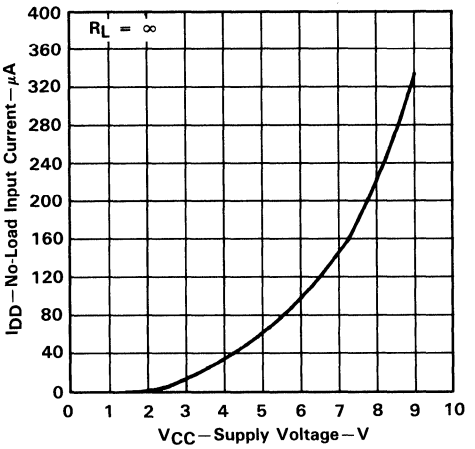

FIGURE 2

OUTPUT RESISTANCE
vs
SUPPLY VOLTAGE

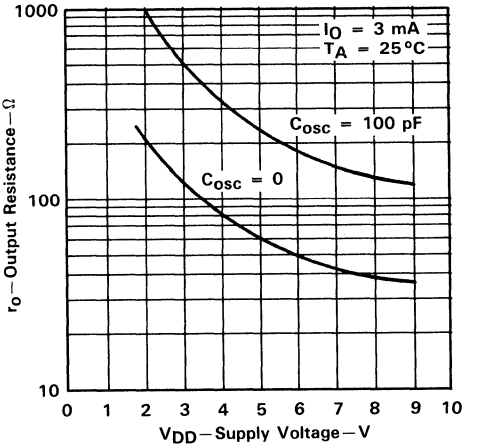

FIGURE 3

OUTPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

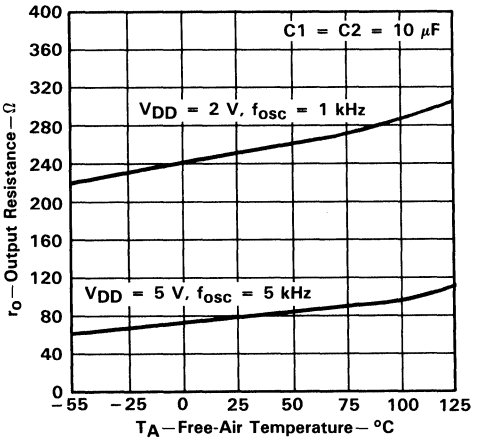

FIGURE 4

OUTPUT RESISTANCE
vs
OSCILLATOR FREQUENCY

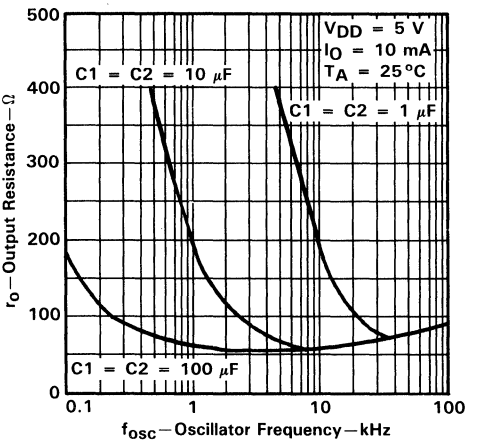

FIGURE 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the two devices.

TYPICAL CHARACTERISTICS†

OSCILLATOR FREQUENCY
vs
EXTERNAL CAPACITOR

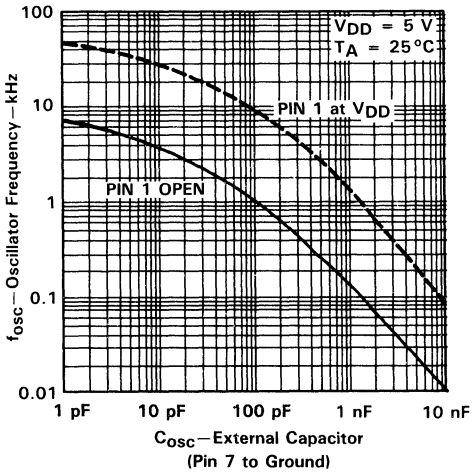

FIGURE 6

OSCILLATOR FREQUENCY
vs
SUPPLY VOLTAGE

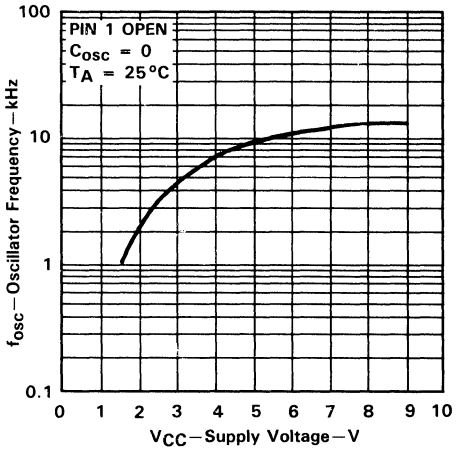

FIGURE 7

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

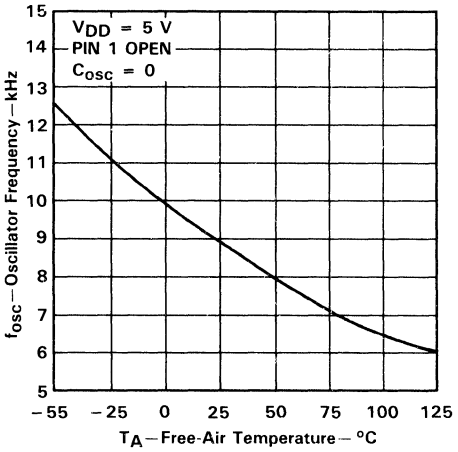

FIGURE 8

POWER CONVERSION EFFICIENCY
vs
OSCILLATOR FREQUENCY

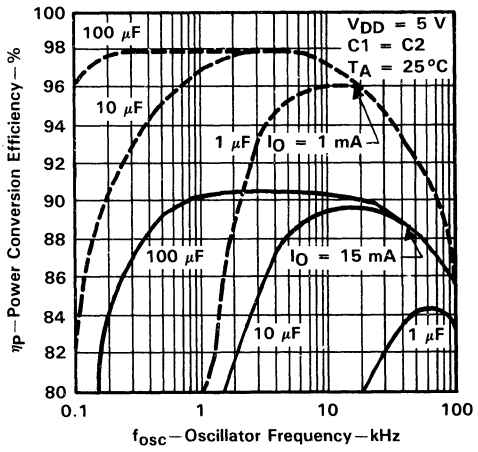

FIGURE 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the two devices.

TYPICAL CHARACTERISTICS

POWER CONVERSION EFFICIENCY and SUPPLY CURRENT vs OUTPUT CURRENT

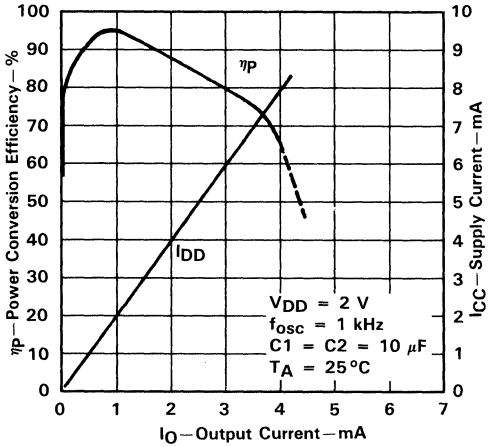

FIGURE 10

POWER CONVERSION EFFICIENCY and SUPPLY CURRENT vs OUTPUT CURRENT

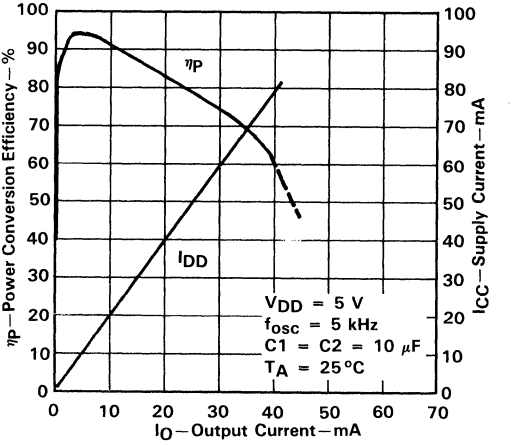

FIGURE 11

OUTPUT VOLTAGE vs OUTPUT CURRENT

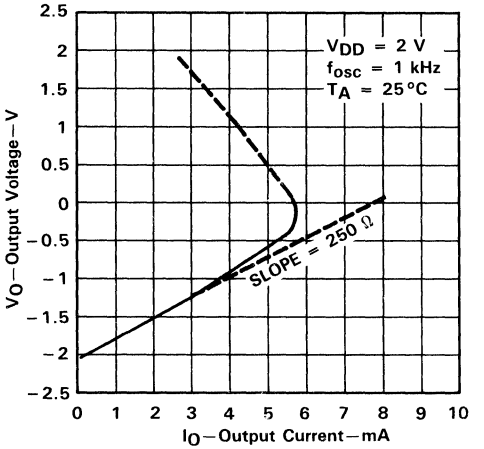

FIGURE 12

OUTPUT VOLTAGE vs OUTPUT CURRENT

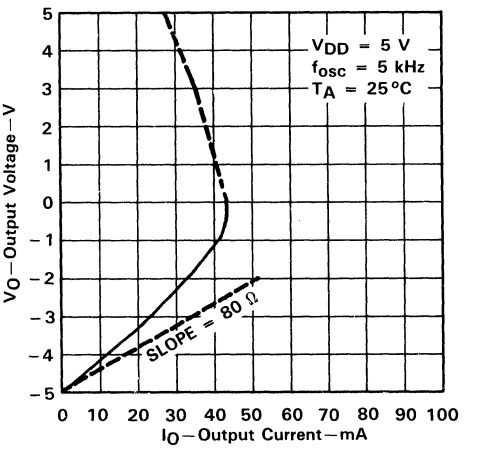

FIGURE 13

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TYPICAL APPLICATION DATA

theory of operation

To understand the theory of operation of the LTC1044, a review of a basic switched-capacitor building block is helpful. In Figure 14, when the switch is in the left position, capacitor C1 charges to voltage V1. The total charge on C1 is q1 = C1 • V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1 • V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is calculated as follows:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is calculated as follows:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{eq}}$$

where R_{eq} is defined as $R_{eq} = 1/fC1$. The equivalent circuit for the switched-capacitor network is shown in Figure 15.

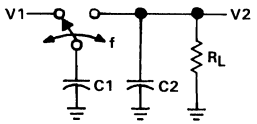

FIGURE 14. SWITCHED-CAPACITOR BUILDING BLOCK

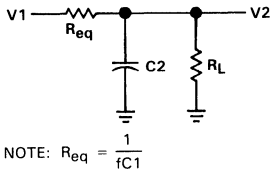

FIGURE 15. SWITCHED-CAPACITOR EQUIVALENT CIRCUIT

Examination of Figure 16 shows that the LTC1044 has the same switching action as the basic switched-capacitor building block, with the addition of finite switch on-state resistance and output voltage ripple.

The simple theory, although not exact, helps illustrate how the device operates. For example, it explains how the LTC1044 behaves in Figure 9. The loss, and hence the efficiency, is determined by the output impedance. As frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term, and power efficiency drops. Figure 9 shows this effect for various capacitor values.

Note also that power efficiency decreases as frequency increases. This is caused by internal switching losses that occur because some finite charge is lost in each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant, and the power efficiency starts to decrease.

TYPICAL APPLICATION DATA

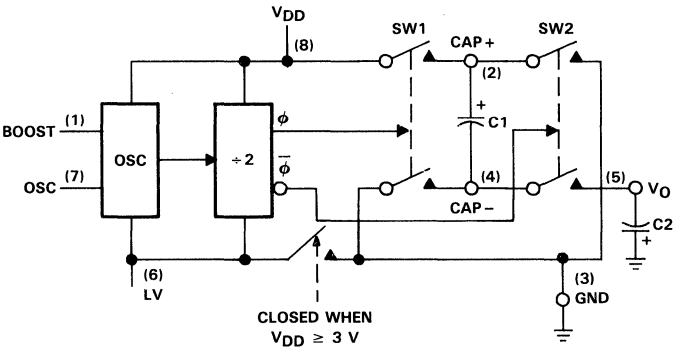

FIGURE 16. LTC1044 SWITCHED-CAPACITOR VOLTAGE CONVERTER BLOCK DIAGRAM

LV (pin 6)

The internal logic of the LTC1044 runs between V_{DD} and LV (pin 6). For $V_{DD} \geq 3$ V, an internal switch shorts LV to GND (pin 3). The LV pin can be tied to ground or left floating. For $V_{DD} \leq 3$ V, the LV pin should be tied to GND.

OSC (pin 7) and BOOST (pin 1)

The switching frequency can be raised, lowered, or driven from an external source. Figure 17 shows a functional diagram of the oscillator circuit. By connecting the boost pin (pin 1) to V_{DD}, the charge and discharge current is increased, thereby increasing the frequency by a factor of approximately 7. Increasing the frequency decreases output impedance and ripple for higher load currents. Loading pin 7 with more capacitance lowers the frequency. Using the boost pin (pin 1) in conjunction with external capacitance on pin 7 allows the user to select the frequency over a wide range.

Driving the LTC1044 from an external frequency source can easily be achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 18. The output current from pin 7 is small, typically 0.5 μA, so a logic gate can drive this current. Using a CMOS logic gate is preferable because it can operate over a wide supply voltage range (3 V to 15 V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 17. For 5-V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 18).

TYPICAL APPLICATION DATA

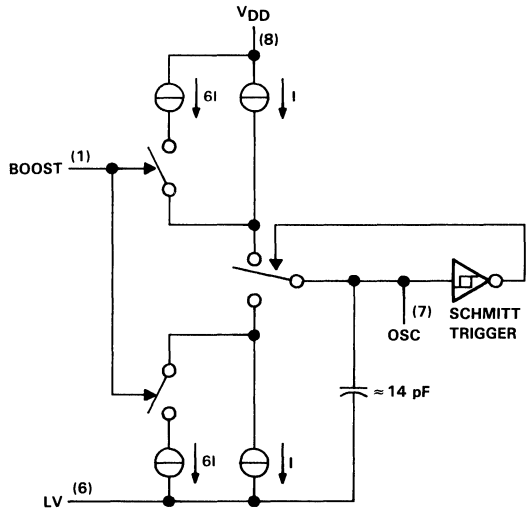

FIGURE 17. OSCILLATOR

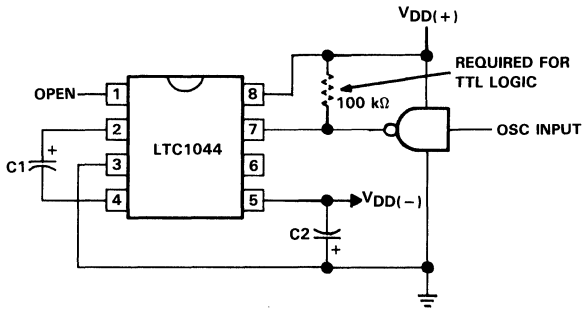

FIGURE 18. EXTERNAL CLOCKING

external diode (D_X)

Previous circuits of this type have required a diode between V_O (pin 5) and the external capacitor C2 for voltages above 6.5 V (5 V for military temperature range). The improvements in the LTC1044 circuit design and Texas Instruments LinCMOS™ silicon-gate process have eliminated the need for this diode. The LTC1044 operates from 1.5 V to 9 V without the protection diode over all temperature ranges. The LTC1044 will operate without any problems in existing LTC7660 designs that use the protection diode as long as the maximum recommended supply voltage of 9 V is not exceeded.

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TYPICAL APPLICATION DATA

capacitor selection

External capacitors C1 and C2 are not critical. They do not have to be high quality or have tight tolerance, nor is matching required. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

negative voltage converter

Figure 19 shows a typical connection that provides a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges without the need for external diodes. The LV pin (pin 6) is shown grounded, but for $V_{DD} \geq 3$ V, it may be floated, since LV is internally switched to ground (pin 3) for $V_{DD} \geq 3$ V.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80-Ω resistor. The 80-Ω output impedance is composed of two terms – the equivalent switched-capacitor resistance (see Theory of Operation) and a term related to the on-state resistance of the MOS switches. At an oscillator frequency of 10 kHz and C1 = 10 µF, the first term is:

$$R_{eq} = \frac{1}{(f_{osc}/2) \times C1} = \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\ \Omega$$

Notice that the equation for R_{eq} is not a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term. While the exact expression for output impedance is extremely complex, the dominant effect of the capacitor is clearly shown in the typical curves of output impedance and power efficiency versus frequency. For C1 = C2 = 10 µF, the output impedance goes from 60 Ω at f_{osc} = 10 kHz to 200 Ω at f_{osc} = 1 kHz. As the 1/fC term becomes large compared to the switch on-state resistance term, the output resistance is determined by 1/fC only.

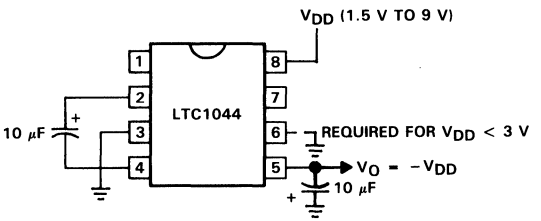

FIGURE 19. NEGATIVE VOLTAGE CONVERTER

voltage doubling

Figure 20 illustrates two methods of voltage doubling. In Figure 20(a), doubling is achieved by simply rearranging the connection of the two external capacitors. When the input voltage is less than 3 V, an external 1-MΩ resistor is required to ensure that the oscillator starts; it is not required for higher input voltages.

In this application, the ground input (pin 3) is taken above V_{DD} (pin 8) during power-on, making it prone to latch-up. The latch-up, while not destructive, prevents the circuit from doubling. Resistor R1 is added to eliminate this problem; in most cases, 200 Ω is sufficient. It may be necessary in a particular application to increase this value to guarantee start-up. The voltage drop across R1 is $V_{R1} = 2 \times I_O \times R2$. If this voltage exceeds two diode drops (1.4 V for silicon, 0.8 V for Schottky), the circuit in Figure 20(a) is recommended because it will never have a start-up problem.

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TYPICAL APPLICATION DATA

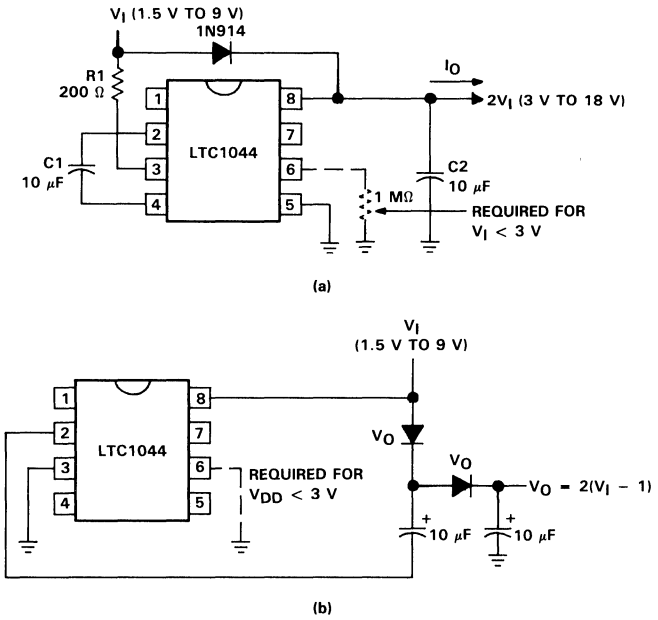
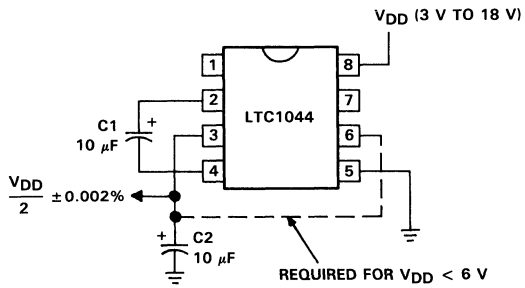


FIGURE 20. VOLTAGE DOUBLER

ultra-precision voltage divider

An ultra-precision voltage divider is shown in Figure 21. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100 nA. However, with a slight loss in accuracy, the load current can be increased.



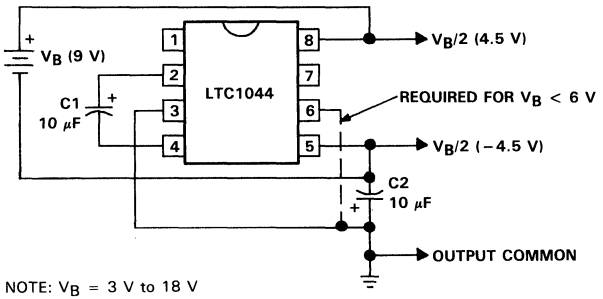
NOTE: T_A = MIN to MAX, $I_O \leq 100$ nA

FIGURE 21. ULTRA-PRECISION VOLTAGE DIVIDER

TYPICAL APPLICATION DATA

battery splitter

Obtaining positive and negative supplies from a single battery or single power supply is a common need in many systems. Where current requirements are small, the circuit shown in Figure 22 is a simple solution. It provides symmetrical positive and negative output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6 V, pin 6 should also be connected to pin 3, as shown by the dashed line.

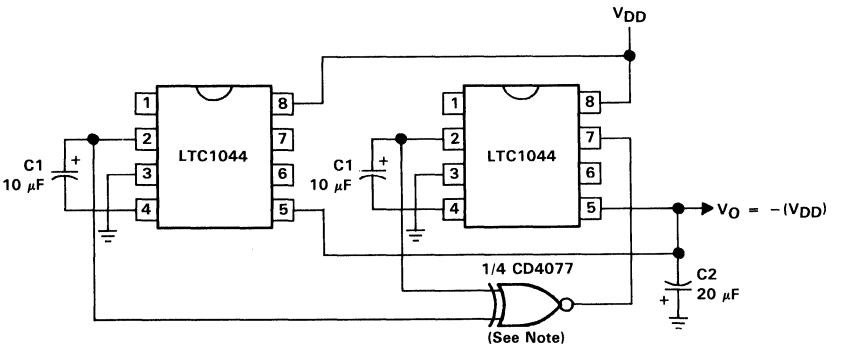


NOTE: V_B = 3 V to 18 V

FIGURE 22. BATTERY SPLITTER

paralleling for lower output resistance

Figures 23, 24, and 25 illustrate the flexibility of the LTC1044. Figure 23 shows two LTC1044s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the size of C1 or increasing the frequency is more beneficial than the paralleling circuit shown.



NOTE: The exclusive NOR gate synchronizes both LTC1044s to minimize ripple.

FIGURE 23. PARALLELING FOR LOWER OUTPUT RESISTANCE

TYPICAL APPLICATION DATA

Figures 24 and 25 "stack" two LTC1044s to provide even higher voltages. As shown schematically in Figure 24, a negative voltage doubler or tripler can be achieved depending upon how pin 8 of the second LTC1044 is connected. Figure 25 illustrates a similar circuit that can be used to obtain positive tripling, or even quadrupling [the doubler circuit appears in Figure 20(a)]. In both of these circuits, the available output current is a function of the product of the individual power conversion efficiencies and the voltage step-up ratio.

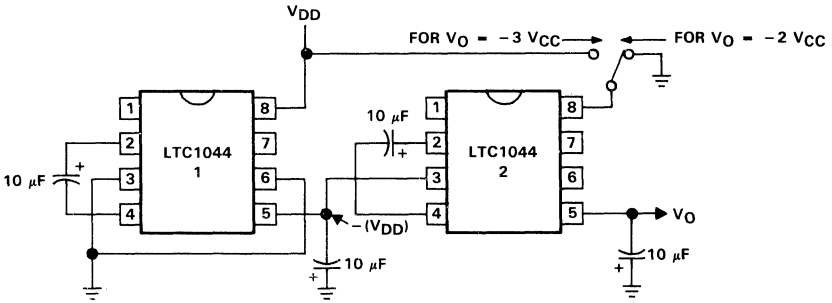
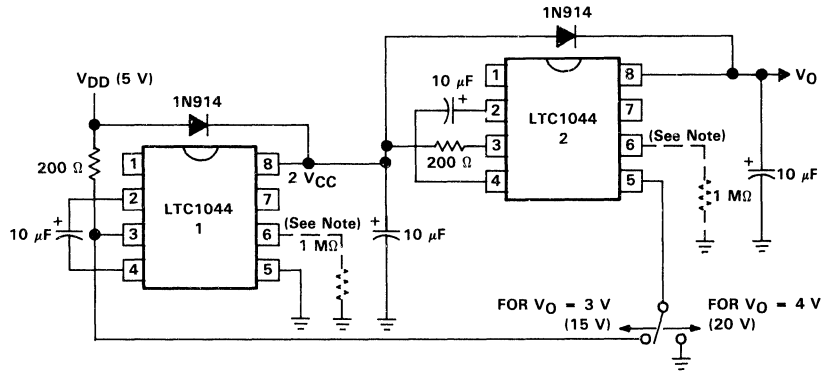


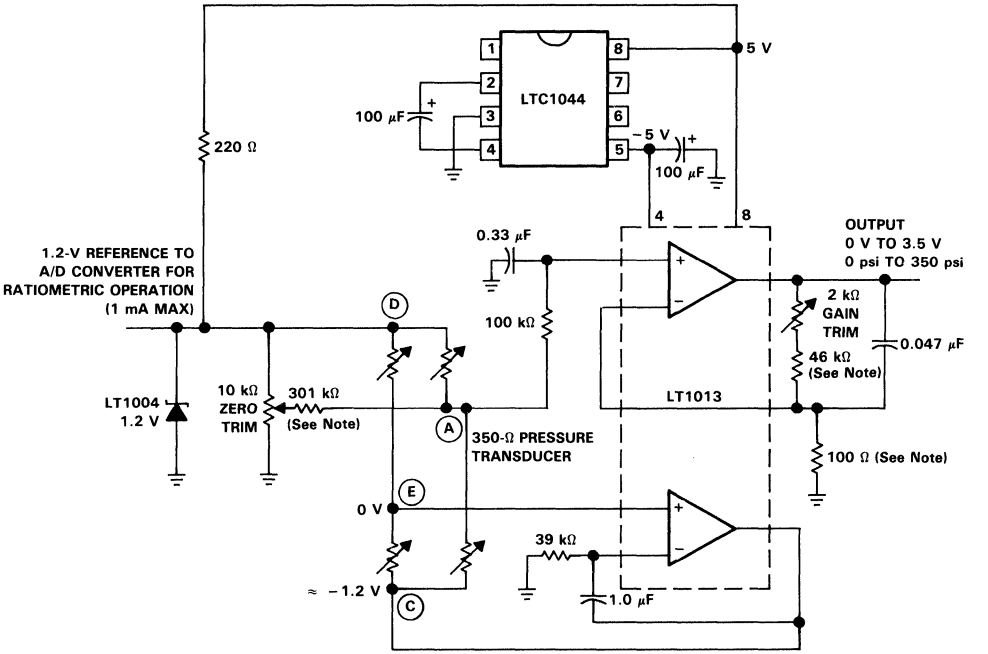
FIGURE 24. STACKING FOR HIGHER VOLTAGE



NOTE: Required for V_{DD} < 3 V

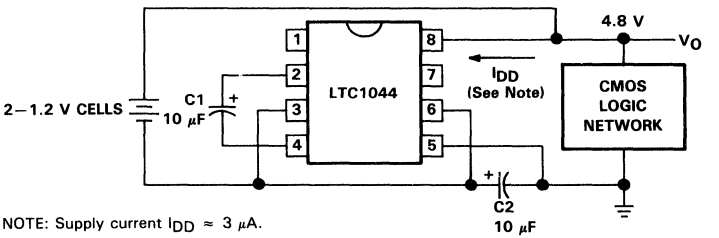
FIGURE 25. VOLTAGE TRIPLER/QUADRUPLER

TYPICAL APPLICATION DATA



NOTE: 1% film resistor pressure transducer BLH/DHF-350 (Circled letter is pin number)

FIGURE 26. SINGLE 5-V STRAIN GAUGE BRIDGE SIGNAL CONDITIONER



NOTE: Supply current $I_{DD} \approx 3\ \mu A$.

FIGURE 27. GENERATING CMOS LOGIC SUPPLY FROM 2 MERCURY BATTERIES

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TYPICAL APPLICATION DATA

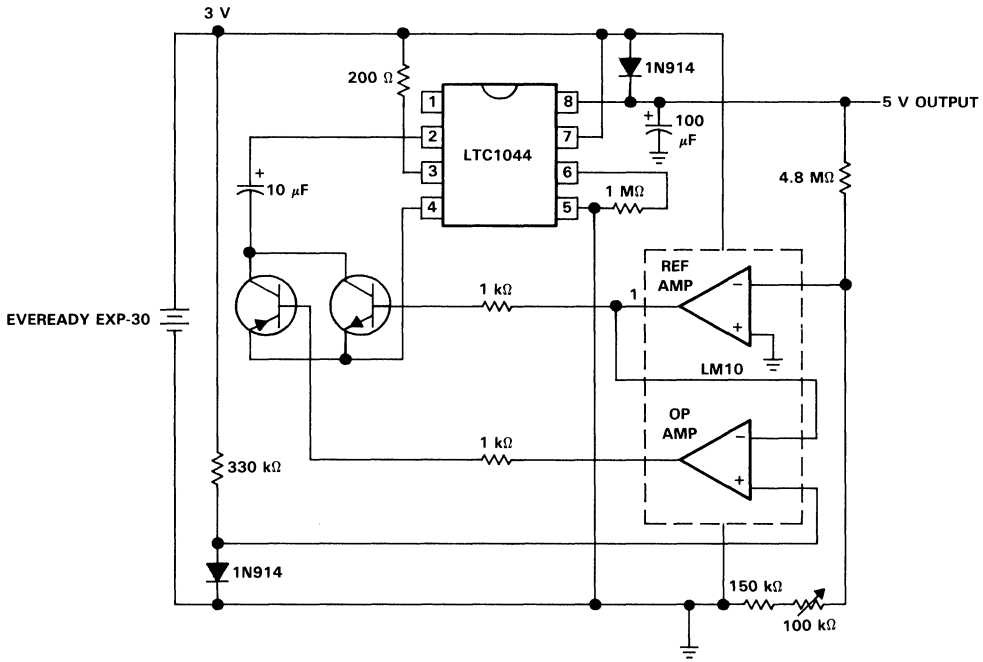
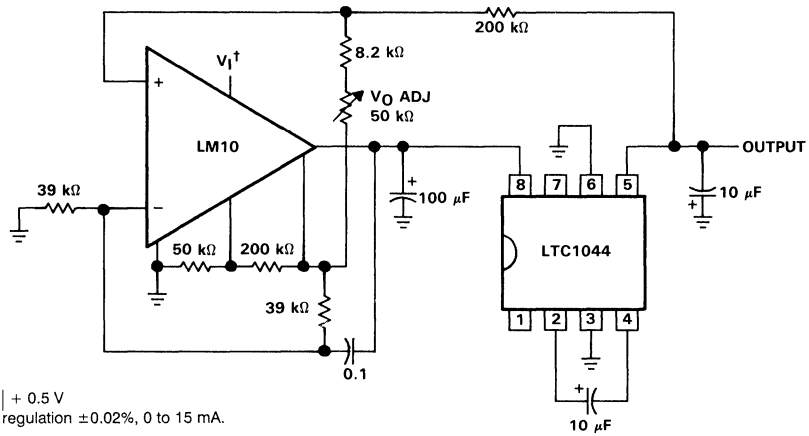


FIGURE 28. REGULATED OUTPUT 3-V TO 5-V CONVERTER



†$V_I \geq |-V_O| + 0.5$ V
NOTE: Load regulation ±0.02%, 0 to 15 mA.

FIGURE 29. LOW-OUTPUT-IMPEDANCE VOLTAGE CONVERTER

TYPICAL APPLICATION DATA

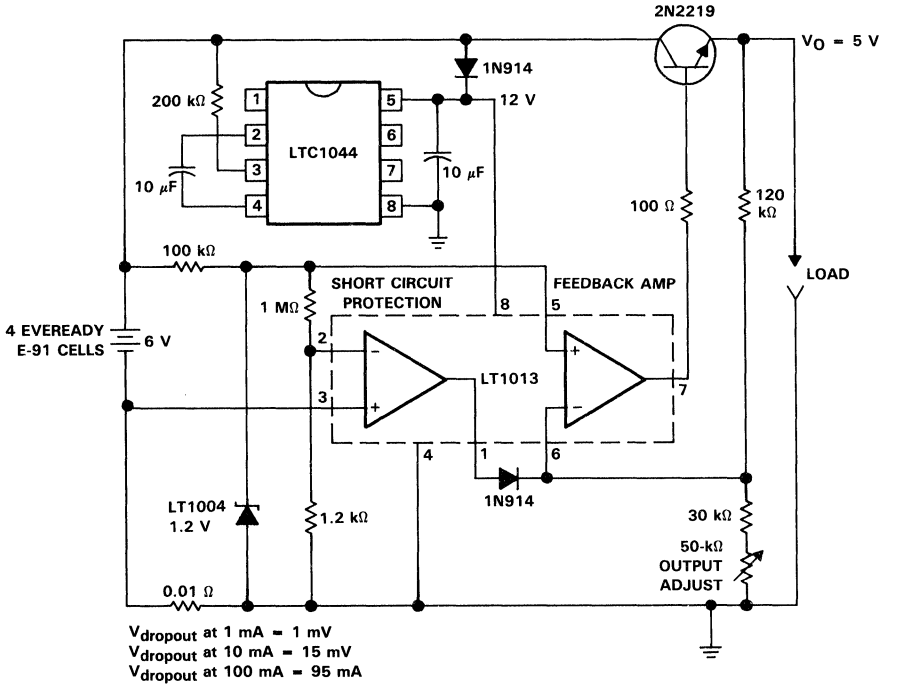
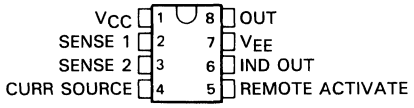


FIGURE 30. LOW-DROPOUT 5-V REGULATOR

D2439, APRIL 1978—REVISED MARCH 1988

- **Separate Outputs for "Crowbar" and Logic Circuitry**
- **Programmable Time Delay to Eliminate Noise Triggering**
- **TTL-Level Activation Isolated from Voltage-Sensing Inputs**
- **2.6-Volt Internal Voltage Reference with Temperature Coefficient Typically 0.08%/°C**

D, JG, OR P PACKAGE
(TOP VIEW)

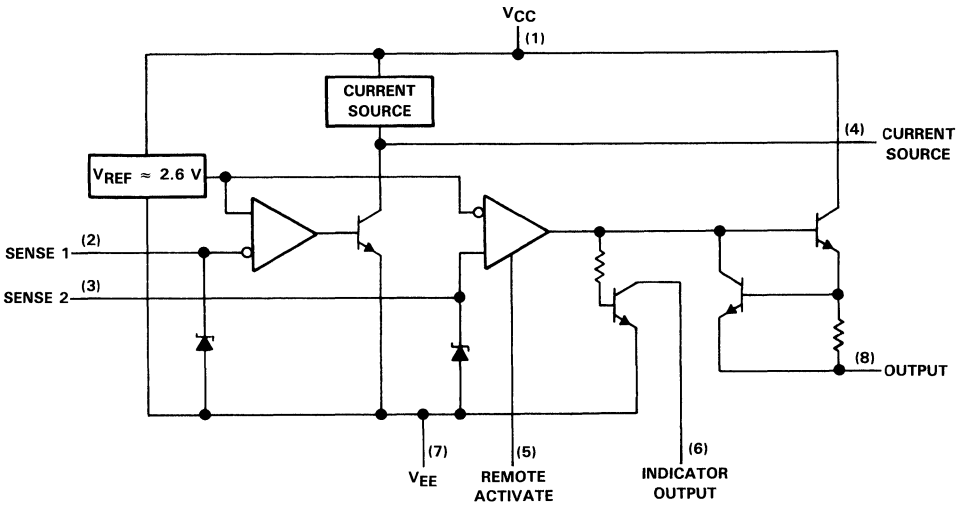


description

The MC3423 overvoltage-sensing circuit is designed to protect sensitive electronic circuitry by monitoring the supply rail and triggering an external "crowbar" SCR in the event of a voltage transient or loss of regulation. The protective mechanism may be activated by an overvoltage condition at the Sense 2 input or by application of a TTL high level to the Remote Activate terminal. Separate outputs are available to trigger the crowbar circuit and to provide a logic pulse to indicator or power supply control circuitry. The Sense 2 input provides a direct control of the output circuitry. The Sense 1 input controls an internal current source that may be utilized to implement a delayed trigger by connecting its output to an external capacitor and the Sense 2 input. This protects against false triggering due to noise at the Sense 1 input.

The MC3423 is characterized for operation from 0°C to 70°C.

functional block diagram



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absolute maximum ratings

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Sense 1 voltage . . . . . 6.5 V
Sense 2 voltage . . . . . 6.5 V
Remote activate input voltage . . . . . 7 V
Output current, I_O . . . . . 300 mA
Continuous total dissipation: . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTE 1: Voltage values are measured with respect to the V_{EE} terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	40	V
High-level input voltage, remote activate input	2		V
Low-level input voltage, remote activate input		0.5	V

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V to 36 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	Remote Activate at 2 V, I_O = 100 mA	$V_{CC}-2.2$	$V_{CC}-1.8$		V
Indicator low-level output voltage	Remote Activate at 2 V, I_O = 1.6 mA		0.1	0.4	V
Threshold voltage of either sense input	T_A = 25°C	2.45	2.6	2.75	V
Temperature coefficient of input threshold voltage			0.06		%/°C
Source current (pin 4)	Sense 1 at 3 V, Pin 4 at 1.3 V	0.1	0.22	0.3	mA
High-level input current, Remote Activate input	V_{CC} = 5 V, V_I = 2 V		5	40	μA
Low-level input current, Remote Activate input	V_{CC} = 5 V, V_I = 0.8 V		−120	−180	μA
Supply current	Outputs open		6	10	mA
Propagation delay time, Remote Activate input to output	T_A = 25°C		0.5		μs
Output current rate of rise	T_A = 25°C		400		mA/μs

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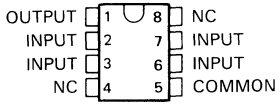
D2565, OCTOBER 1982—REVISED APRIL 1988

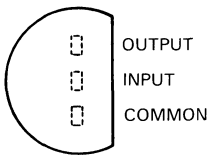
- 3-Terminal Regulators
- Output Current Up to 100 mA
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Direct Replacement for Motorola MC79L00 Series
- Available in 5% or 10% Selections

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
−5 V	MC79L05AC	MC79L05C
−12 V	MC79L12AC	MC79L12C
−15 V	MC79L15AC	MC79L15C

D PACKAGE
(TOP VIEW)



LP SILECT PACKAGE
(TOP VIEW)

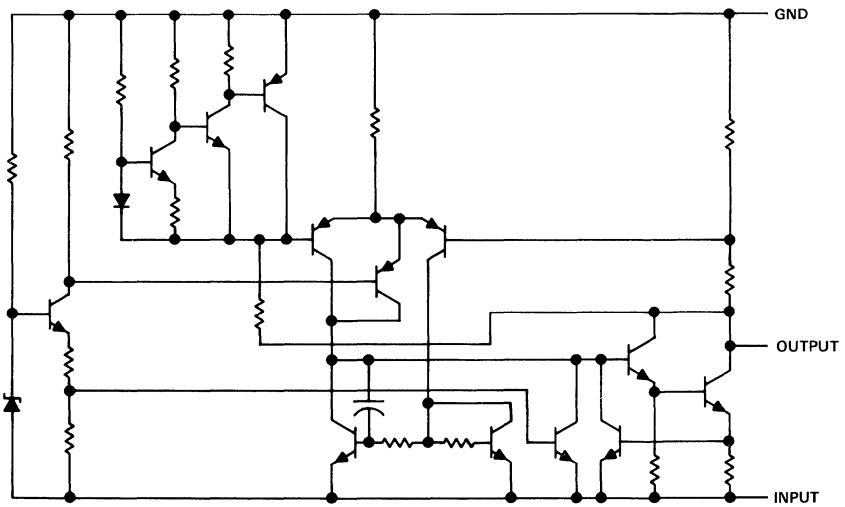


NC-No internal connection

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features make them essentially immune to overload. When used as a replacement for a Zener-diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude and lower bias current.

schematic



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	MC79L05	MC79L12 MC79L15	UNIT
Input voltage	−30	−35	V
Continuous total dissipation	See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range	0 to 150	0 to 150	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

DISSIPATION RATING TABLE 1—FREE AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	825 mW	6.6 mW/°C	25°C	528 mW
LP†	775 mW	6.2 mW/°C	25°C	496 mW

†The LP package dissipation rating is based on thermal resistance measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.0 mW/°C	95°C	725 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	MC79L05	−7	−20	V
	MC79L12	−14.5	−27	
	MC79L15	−17.5	−30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J		0	125	°C

MC79L05 electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L05C			MC79L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−4.6	−5	−5.4	−4.8	−5	−5.2	V
	V_I = −7 V to −20 V, I_O = 1 mA to 40 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
	V_I = −10 V, I_O = 1 mA to 70 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
Input regulation	V_I = −7 V to −20 V	25°C			200			150	mV
	V_I = −8 V to −20 V				150			100	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			60			60	mV
	I_O = 1 mA to 40 mA				30			30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6			6	mA
		125°C			5.5			5.5	
Bias current change	V_I = −8 V to −20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

MC79L12 electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L12C			MC79L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−11.1	−12	−12.9	−11.5	−12	−12.5	V
	V_I = −14.5 V to −27 V, I_O = 1 mA to 40 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
	V_I = −19 V, I_O = 1 mA to 70 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −27 V	25°C			250			250	mV
	V_I = −16 V to −27 V				200			200	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			100			100	mV
	I_O = 1 mA to 40 mA				50			50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −16 V to −27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

†All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

MC79L15 electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MC79L15C			MC79L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−13.8	−15	−16.2	−14.4	−15	−15.6	V
	V_I = −17.5 V to −30 V, I_O = 1 mA to 40 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
	V_I = −23 V, I_O = 1 mA to 70 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C			300			300	mV
	V_I = −20 V to −30 V				250			250	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			150			150	mV
	I_O = 1 mA to 40 mA				75			75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −20 V to −30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

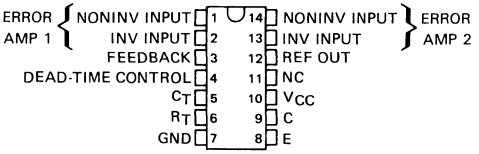
†All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

D2714, MARCH 1983—REVISED FEBRUARY 1988

- **Complete PWM Power Control Circuitry**
- **Uncommitted Output for 200-mA Sink or Source Current**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply**
- **Circuit Architecture Provides Easy Synchronization**
- **Direct Replacement for Motorola MC34060**

D OR N PACKAGE
(TOP VIEW)



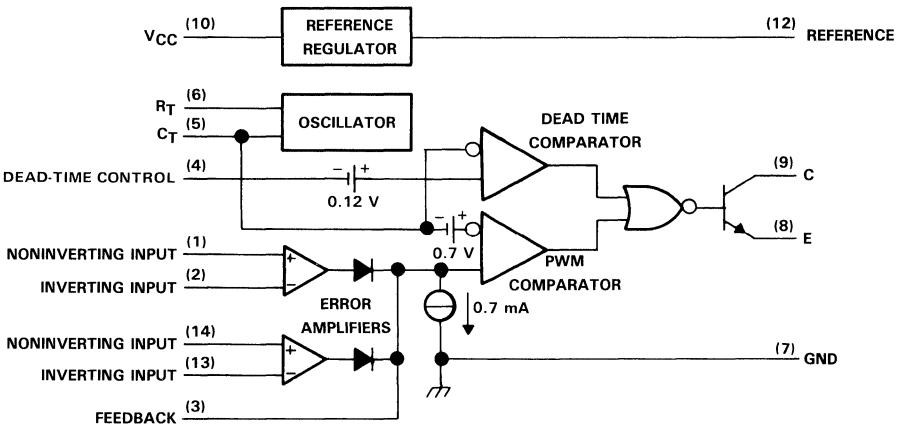
NC—No internal connections

description

The MC34060 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the device contains an on-chip 5-V regulator, two error amplifiers, an adjustable oscillator, and a dead-time control comparator. The uncommitted output transistor provides either common-emitter or emitter-follower output capability. The internal amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} − 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common MC34060 circuitry and provide a sawtooth input for associated control circuitry in multiple rail power supplies.

The MC34060 is characterized for operation from 0°C to 70°C.

functional block diagram



All voltage and current values shown are nominal.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

		UNIT
Supply voltage, V_{CC} (see Note 1)	42	V
Amplifier input voltages	$V_{CC}+0.3$	V
Collector output voltage	42	V
Collector output current	250	mA
Continuous total dissipation	See Dissipation Rating Table	
Operating free-air temperature range	0 to 70	°C
Storage temperature range	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260	°C

NOTE 1: All voltage values except differential voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	900 mW	7.6 mW/°C	31 °C	608 mW
N	1000 mW	9.2 mW/°C	41 °C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40	V
Collector output current (each transistor)		200	mA
Reference output current		10	mA
Current into feedback terminal		0.3	mA
Timing capacitor, C_T	0.47	10000	nF
Timing resistor, R_T	1.8	500	kΩ
Oscillator frequency	1	200	kHz
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 25 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Output voltage (V_{ref})	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25	mV
Output regulation	I_{IO} = 1 to 10 mA, T_A = 25°C		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		0.2%	2.6%	
Short-circuit output current§	V_{ref} = 0, T_A = 25°C		35		mA

oscillator section

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency	C_T = 0.001 μF, R_T = 47 kΩ		25		kHz
Standard deviation of frequency¶	C_T = 0.001 μF, R_T = 47 kΩ		3%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%		
Frequency change with temperature	C_T = 0.001 μF, R_T = 47 kΩ, ΔT_A = MIN to MAX			±2%	

dead-time control-section (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V			−2	−10	μA
Maximum duty cycle	$V_{I\ (pin\ 4)}$ = 0	C_T = 0.1 μF, R_T = 12 kΩ	90%	96%	100%	
		C_T = 0.001 μF, R_T = 47 kΩ		92%	100%	
Input threshold voltage (pin 4)	Zero duty cycle			3	3.3	V
	Maximum duty cycle		0			

error-amplifier sections

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	$V_{O\ (pin\ 3)}$ = 2.5 V		2	10	mV
Input offset current	$V_{O\ (pin\ 3)}$ = 2.5 V		25	250	nA
Input bias current	$V_{O\ (pin\ 3)}$ = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V			−0.3 to V_{CC} − 2	V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Phase margin at unity gain	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Common-mode rejection ratio	V_{CC} = 40 V	65	80		dB
Output sink current (pin 3)	V_{ID} = −15 mV to −5 V, $V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V, $V_{(pin\ 3)}$ = 3.5 V	−2			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for "change with temperature" characteristics are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N-1}}$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 25 kHz (unless otherwise noted) (continued)

output section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V, I_E = −200 mA		1.5	2.5	

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA

total device

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	$V_{(pin\ 4)}$ = 2 V, C_T = 0.001 μF,	R_T = 47 kΩ, See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time			40	100	ns

†All typical values are at T_A = 25°C.

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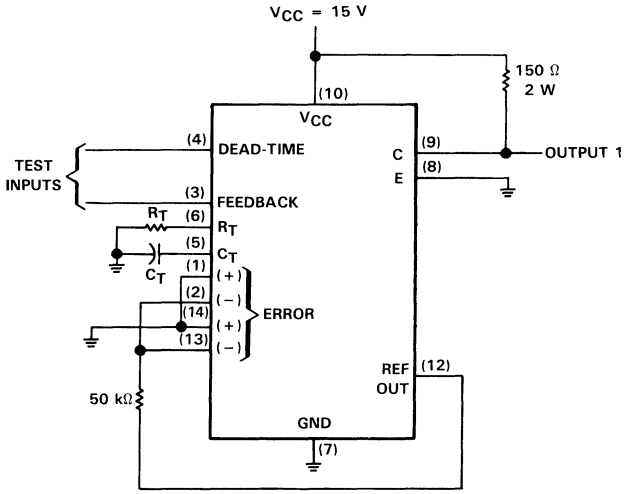
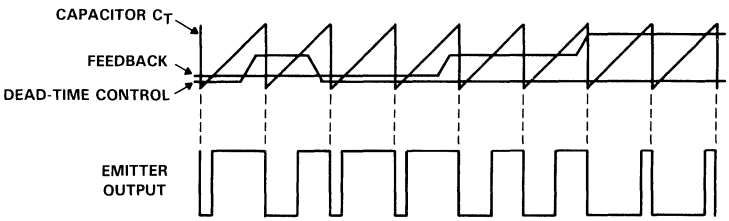
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



TIMING WAVEFORMS

FIGURE 1. DEAD-TIME AND FEEDBACK CONTROL

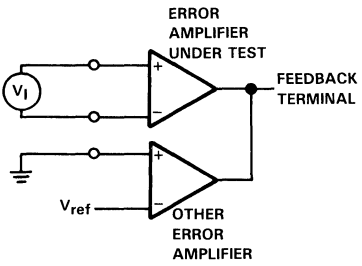
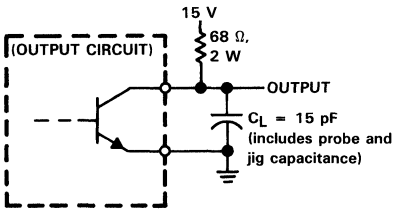
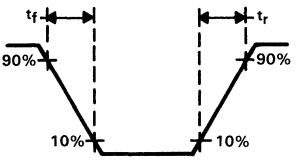


FIGURE 2. ERROR-AMPLIFIER CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

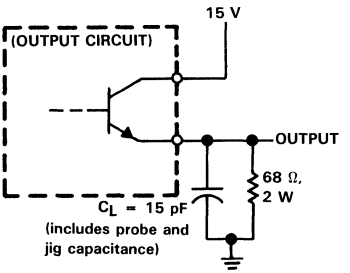


TEST CIRCUIT

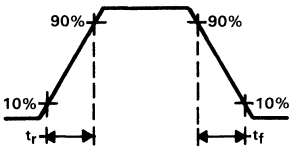


OUTPUT VOLTAGE WAVEFORM

FIGURE 3. COMMON-EMITTER CONFIGURATION



TEST CIRCUIT



OUTPUT VOLTAGE WAVEFORM

FIGURE 4. EMITTER-FOLLOWER CONFIGURATION

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TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY and FREQUENCY VARIATION† vs TIMING RESISTANCE

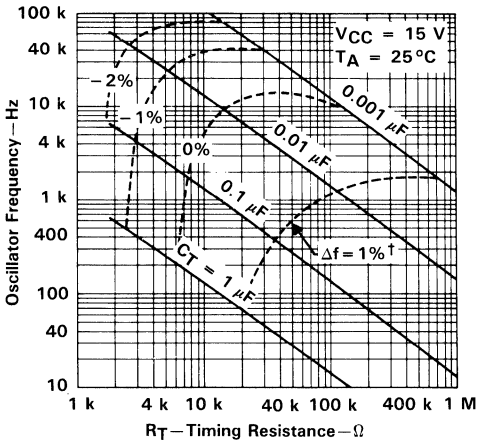


FIGURE 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

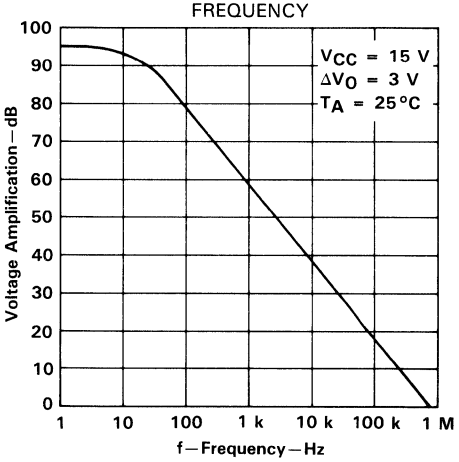


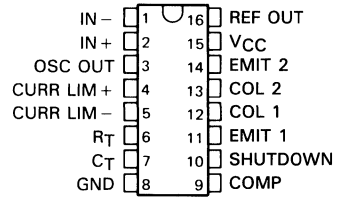
FIGURE 6

†Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D2294, APRIL 1977—REVISED OCTOBER 1988

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable with Silicon General SG2524 and SG3524**

J OR N PACKAGE
(TOP VIEW)

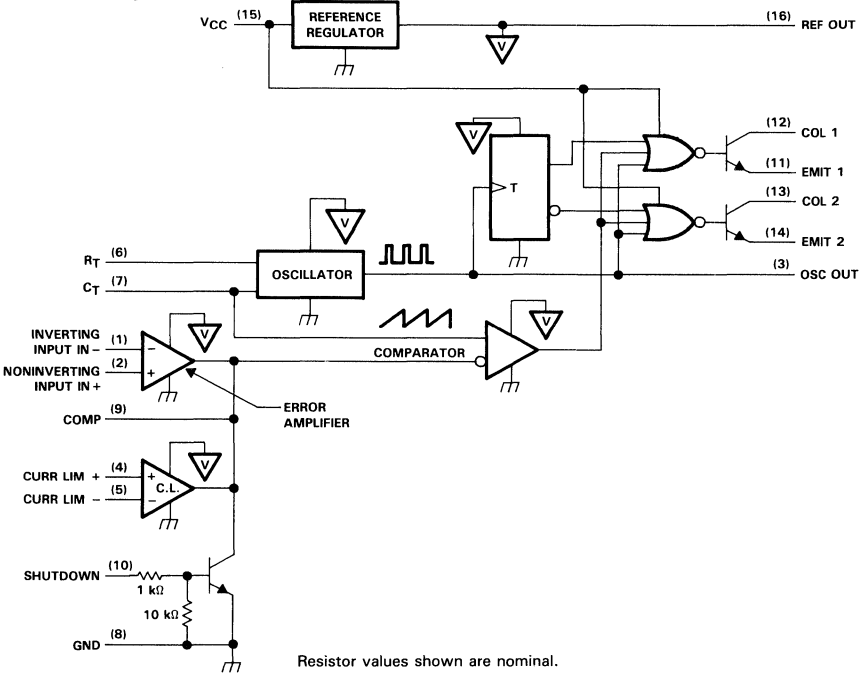


description

The SG2524 and SG3524 incorporate on single monolithic chips all the functions required in the construction of a regulating power supply, inverter, or switching regulator. They can also be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

The SG2524 is characterized for operation from −25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

functional block diagram



Resistor values shown are nominal.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 40 V
Collector output current . . . . . 100 mA
Reference output current . . . . . 50 mA
Current through C_T terminal . . . . . −5 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SG2524 . . . . . −25°C to 85°C
SG3524 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
J	1000 mW	8.2 mW/°C	28°C	656 mW	533 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

	SG2524		SG3524		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	8	40	8	40	V
Reference output current	0	50	0	50	mA
Current thru C_T terminal	−0.03	−2	−0.03	−2	mA
Timing resistor, R_T	1.8	100	1.8	100	kΩ
Timing capacitor, C_T	0.001	0.1	0.001	0.1	μF
Operating free-air temperature	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.6	5	5.4	V
Input regulation	V_{CC} = 8 to 40 V		10	20		10	30	mV
Ripple rejection	f = 120 Hz		66			66		dB
Output regulation	I_O = 0 to 20 mA		20	50		20	50	mV
Output voltage change with temperature	T_A = MIN to MAX		0.3	1		0.3	1	%
Short-circuit output current§	V_{ref} = 0		100			100		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values, except output voltage change with temperature, are at T_A = 25°C.
§Duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

oscillator section

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency	C_T = 0.001 μF, R_T = 2 kΩ		450		kHz
Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant		5		%
Frequency change with voltage	V_{CC} = 8 to 40 V, T_A = 25°C			1	%
Frequency change with temperature	T_A = MIN to MAX			2	%
Output amplitude at pin 3	T_A = 25°C		3.5		V
Output pulse duration (width) at pin 3	C_T = 0.01 μF, T_A = 25°C		0.5		μs

error amplifier section

PARAMETER	TEST CONDITIONS	SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10	mV
Input bias current	V_{IC} = 2.5 V		2	10		2	10	μA
Open-loop voltage amplification		72	80		60	80		dB
Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4			V
Common-mode rejection ratio			70			70		dB
Unity-gain bandwidth			3			3		MHz
Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	V

output section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Collector-emitter breakdown voltage		40			V
Collector off-state current	V_{CE} = 40 V		0.01	50	μA
Collector-emitter saturation voltage	I_C = 50 mA		1	2	V
Emitter output voltage	V_C = 20 V, I_E = −250 μA	17	18		V
Turn-off voltage rise time	R_C = 2 kΩ		0.2		μs
Turn-on voltage fall time	R_C = 2 kΩ		0.1		μs

comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Maximum duty cycle, each output		45			%
Input threshold voltage at pin 9	Zero duty cycle		1		V
	Maximum duty cycle		3.5		
Input bias current			−1		μA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values, except for temperature coefficients, are at T_A = 25°C.
§Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

current limiting section

PARAMETER	TEST CONDITIONS	SG2524			SG3524			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Input voltage range (either input)		−1 to +1			−1 to +1			V
Sense voltage at T_A = 25°C	$V_{(pin\ 2)} - V_{(pin\ 1)} \geq 50$ mV, $V_{(pin\ 9)}$ = 2 V	190	200	210	180	200	220	mV
Temperature coefficient of sense voltage			0.2			0.2		mV/°C

total device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby current	V_{CC} = 40 V, Pins 1,4,7,8,9,11,14 gronded, Pin 2 at 2 V, All other inputs and outputs open		8	10	mA

†All typical values, except for temperature coefficients, are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

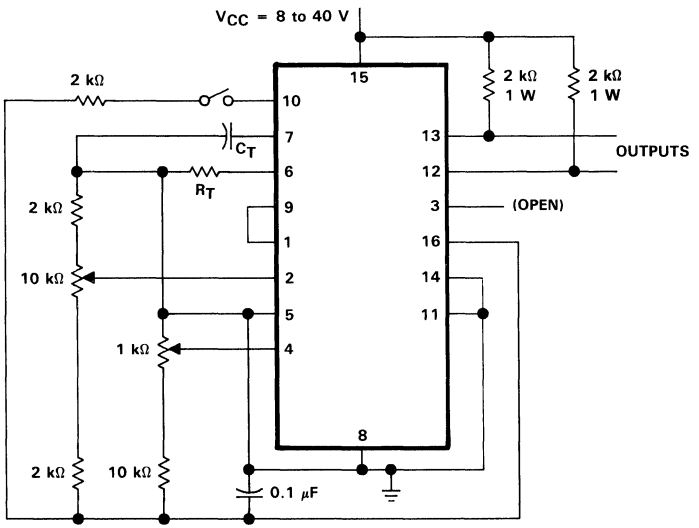

FIGURE 1. GENERAL TEST CIRCUIT

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PARAMETER MEASUREMENT INFORMATION

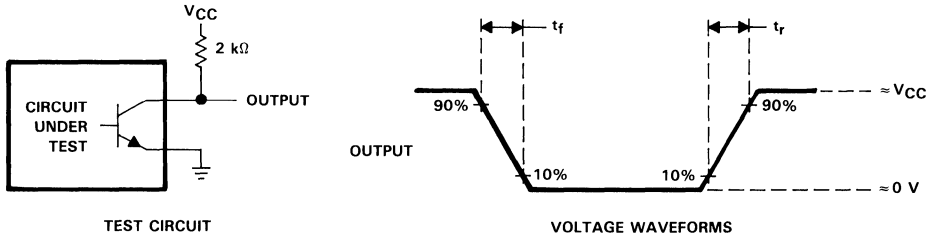


FIGURE 2. SWITCHING TIMES

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION
OF ERROR AMPLIFIER
vs
FREQUENCY

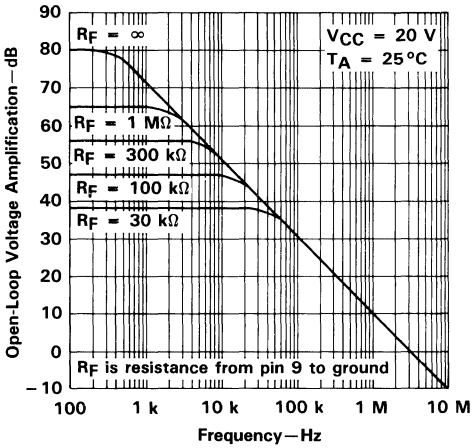


FIGURE 3

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

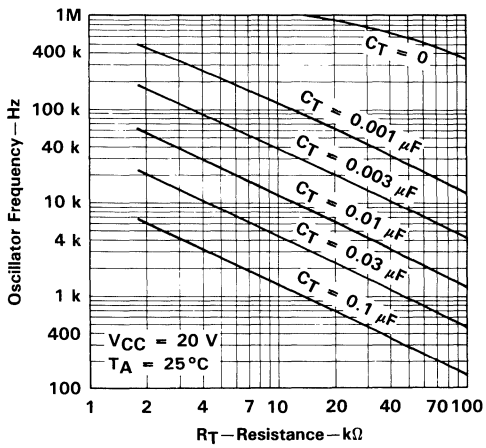


FIGURE 4

TYPICAL CHARACTERISTICS

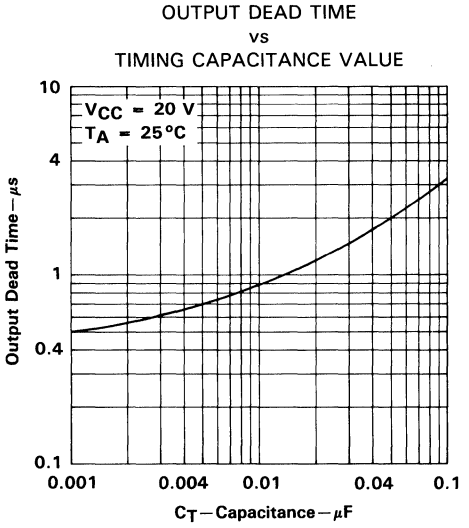


FIGURE 5

PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor R_T and one timing capacitor C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an on-board 5-V regulator that serves as a reference as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference may be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate the error amplifier, or to provide additional control to the regulator.

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

TYPICAL APPLICATION DATA†

oscillator

The oscillator controls the frequency of the SG2524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.15}{R_T C_T}$$

where R_T is in kΩ
C_T is in μF
f is in kHz

Practical values of C_T fall between 0.001 and 0.1 μF. Practical values of R_T fall between 1.8 and 100 kΩ. This results in a frequency range typically from 140 Hz to 500 kHz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse duration may still be maintained by applying a shunt capacitance from pin 3 to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more SG2524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other SG2524s operate. In this application, the C_T R_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and will subsequently reset the slave regulators.

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

TYPICAL APPLICATION DATA†

voltage reference

The 5-V internal reference may be employed by use of an external resistor divider network to establish a reference within the error amplifiers common-mode voltage range (1.8 to 3.4 V) as shown in Figure 6, or an external reference may be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference may be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.

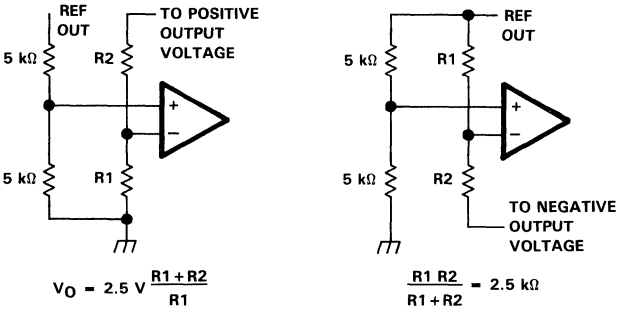


FIGURE 6. ERROR AMPLIFIER BIAS CIRCUITS

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (pin 9) is a high-impedance node (R_L = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})\ R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from pin 9 to ground. Refer to Figure 3 for data.

compensation

Pin 9, as discussed above, is made available for compensation. Since most output filters will introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from pin 9 to ground in the range of 50 kΩ and 0.001 μF. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

shut-down circuitry

Pin 9 can also be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and thus disable the SG2524.

In addition to constant-current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. Pin 5 may also be grounded to convert pin 4 into an additional shut-down terminal.

†Throughout these discussions, references to the SG2524 also apply to the SG3524.

TYPICAL APPLICATION DATA†

current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV and must be applied in the ground line since the voltage range of the inputs is limited to +1 V to −1 V. Caution should be taken to ensure the −1 V limit is not exceeded by either input, otherwise damage to the device may result.

Fold-back current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.

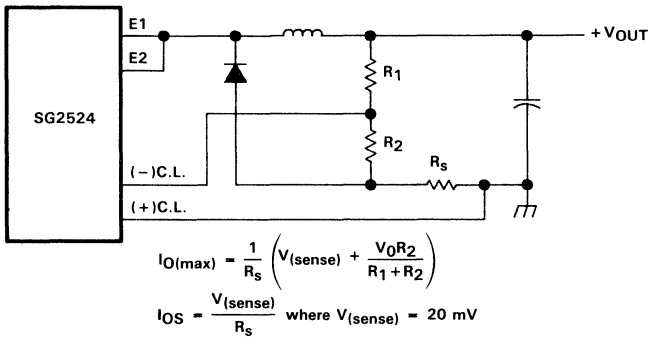


FIGURE 7. FOLDBACK CURRENT LIMITING FOR SHORTED OUTPUT CONDITIONS

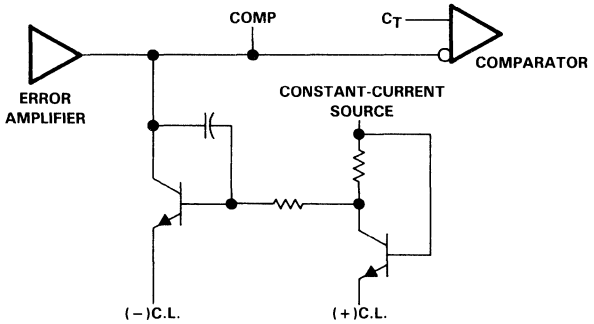


FIGURE 8. CURRENT-LIMIT SCHEMATIC

output circuitry

The SG2524 contains two identical n-p-n transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

†Throughout these discussions, references to the SG2524 also apply to the SG3524.

TYPICAL APPLICATION DATA†

general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

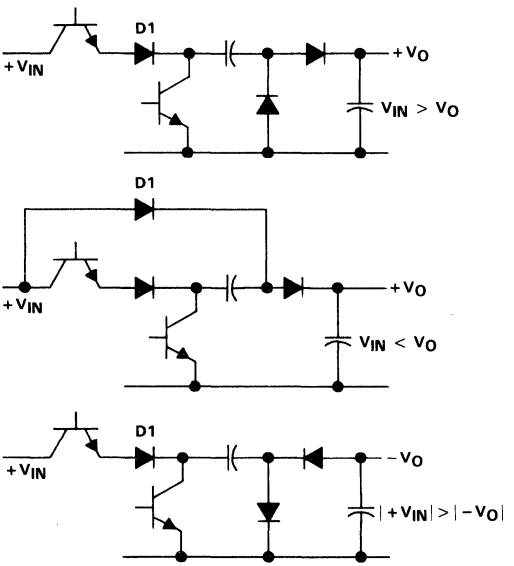


FIGURE 9. CAPACITOR-DIODE-COUPLED VOLTAGE-MULTIPLIER OUTPUT STAGES

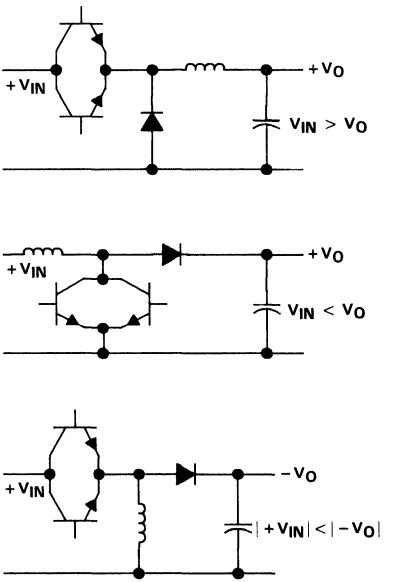
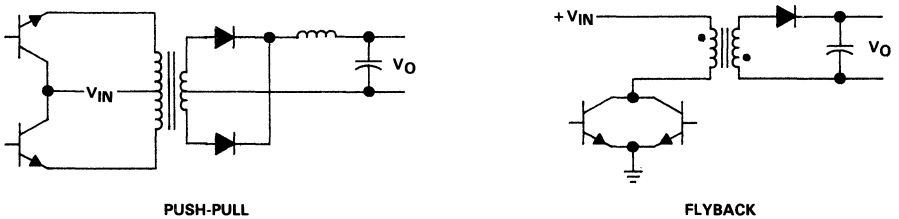


FIGURE 10. SINGLE-ENDED INDUCTOR CIRCUIT



PUSH-PULL FLYBACK

FIGURE 11. TRANSFORMER-COUPLED OUTPUTS

†Throughout these discussions, references to the SG2524 also apply to the SG3524.

TYPICAL APPLICATION DATA†

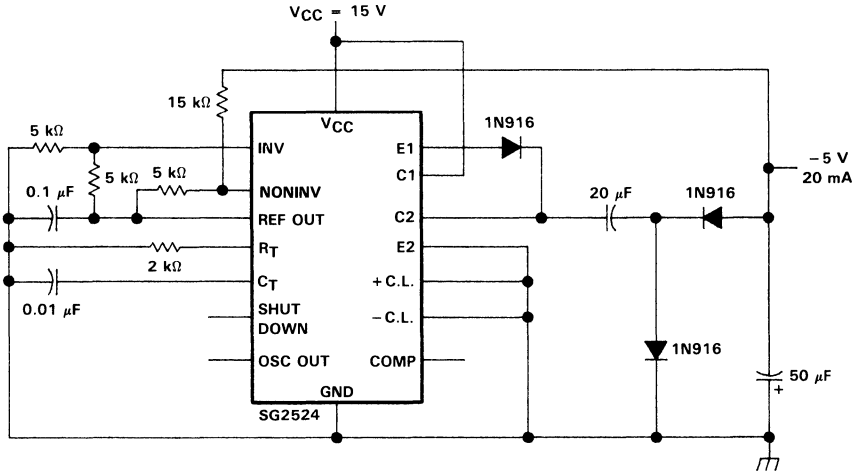


FIGURE 12. CAPACITOR-DIODE OUTPUT CIRCUIT

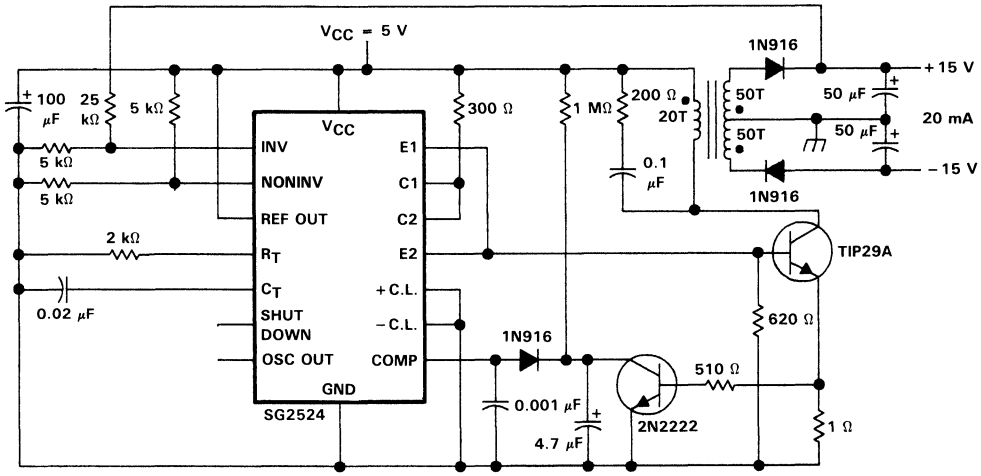


FIGURE 13. FLYBACK CONVERTER CIRCUIT

†Throughout these discussions, references to the SG2524 also apply to the SG3524.

TYPICAL APPLICATION DATA†

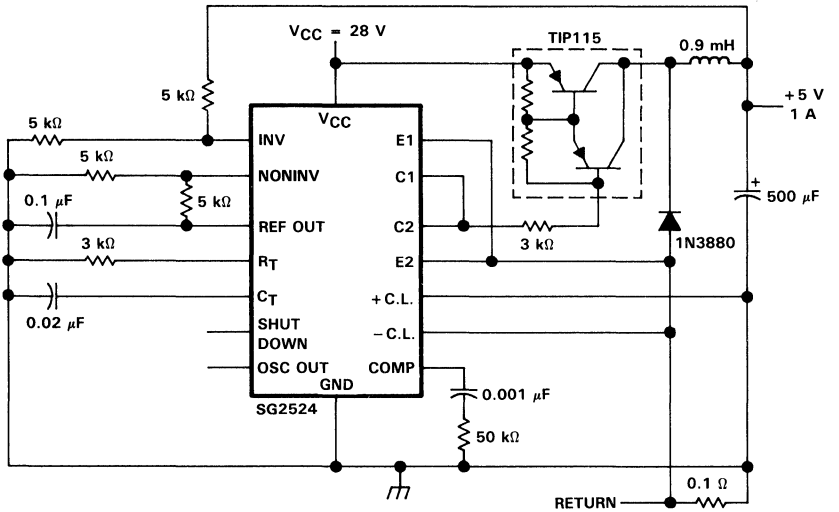


FIGURE 14. SINGLE-ENDED LC CIRCUIT

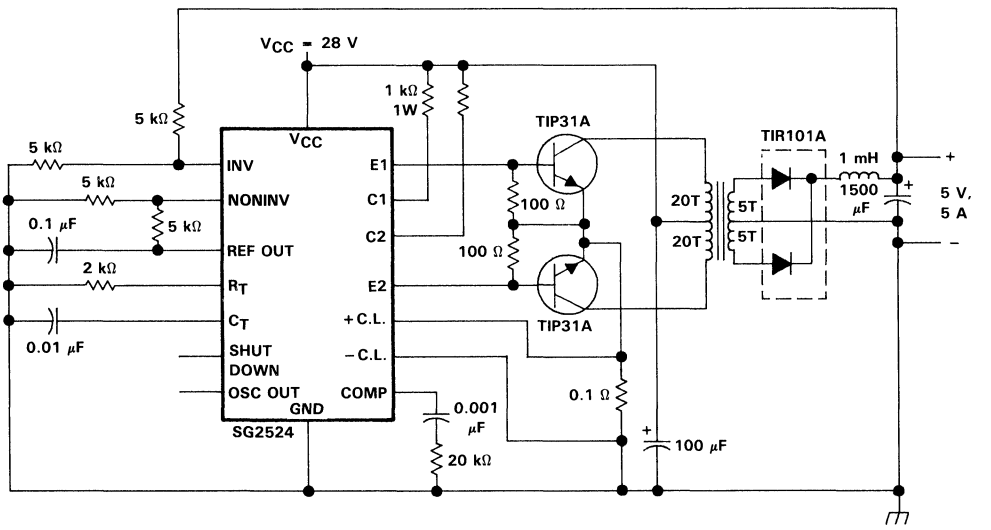


FIGURE 15. PUSH-PULL TRANSFORMER-COUPLED CIRCUIT

†Throughout these discussions, references to the SG2524 also apply to the SG3524.

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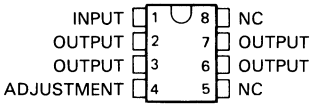
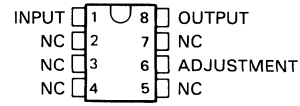
D2527, APRIL 1979—REVISED MAY 1988

- **Output Voltage Range Adjustable from 1.2 V to 32 V**
- **Output Current Capability of 100 mA**
- **Input Regulation Typically 0.01% Per Input-Volt Change**
- **Output Regulation Typically 0.5%**
- **Ripple Rejection Typically 80 dB**

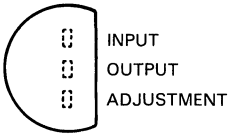
TL317C . . . D PACKAGE
(TOP VIEW)



TL317M . . . JG PACKAGE
(TOP VIEW)



TL317C . . . LP SILECT PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL317 is an adjustable 3-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The device is packaged in standard packages that are easily mounted and handled.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current limiting and thermal overload protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

In addition to replacing fixed regulators, the TL317 regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between the adjustment terminal and the output terminal, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, programming the output to 1.2 V where most loads draw little current.

The TL317M is characterized for operation over the full military temperature range from −55 °C to 125 °C. The TL317C is characterized for operation from 0 °C to 125 °C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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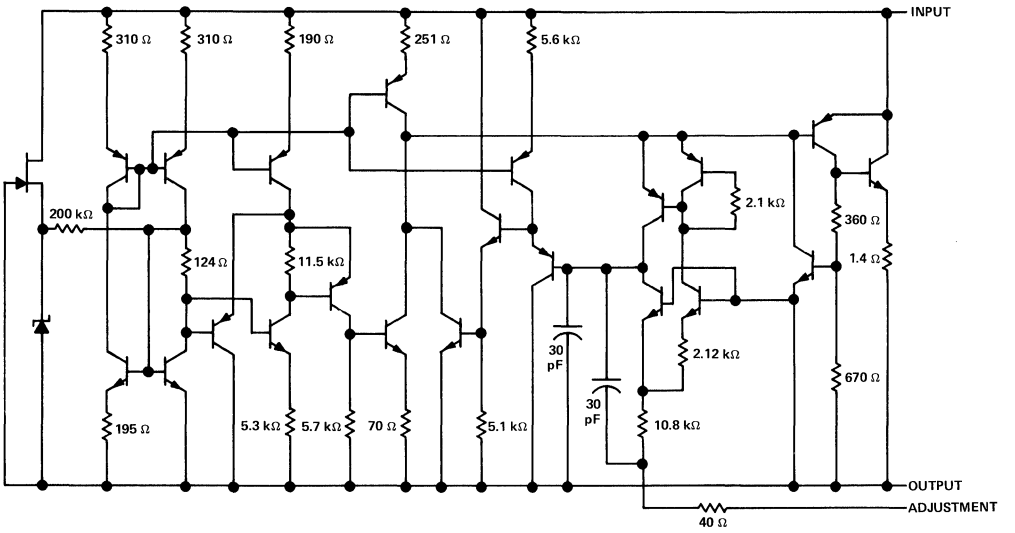
schematic



All component values shown are nominal

absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ . . . . . 35 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air, case, or virtual junction temperature range: TL317M . . . . . −55°C to 150°C
TL317C . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package . . . . . 260°C

DISSIPATION RATING TABLE 1—FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	145 mW
JG	1050 mW	8.4 mW/°C	210 mW
LP†	775 mW	6.2 mW/°C	155 mW

†The LP package dissipation rating is based on thermal resistance measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.6 mW/°C	96°C	740 mW
JG	1600 mW	38.4 mW/°C	108°C	960 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

	TL317M		TL317C		UNIT
	MIN	MAX	MIN	MAX	
Output current, I_O	2.5	100	2.5	100	mA
Operating virtual junction temperature, T_J	−55	125	0	125	°C

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Input regulation (see Note 2)	$V_I - V_O$ = 3 V to 35 V	T_J = 25°C		0.01	0.02	%/V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple rejection	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-μF capacitor between ADJ and ground	f = 120 Hz,	66	80		
Output regulation	I_O = 2.5 mA to 100 mA, T_J = 25°C,	$V_O \leq$ 5 V		25		mV
		$V_O \geq$ 5 V		0.5		%
	I_O = 2.5 mA to 100 mA,	$V_O \leq$ 5 V		50		mV
		$V_O \geq$ 5 V		1		%
Output voltage change with temperature	T_J = 0°C to 125°C			1		%
Output voltage long-term drift (see Note 3)	After 1000 h at T_J = 125°C and $V_I - V_O$ = 35 V			0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		0.003		%
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \leq$ 35 V		100	200		mA
Adjustment-terminal current				50	100	μA
Change in adjustment-terminal current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O$ = 3 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.

NOTES: 2. Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

3. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL APPLICATION DATA

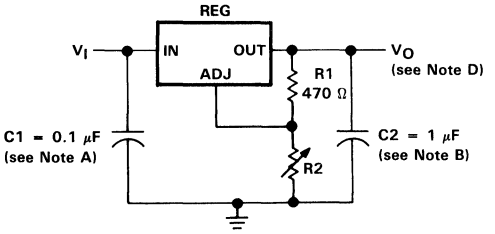


FIGURE 1. ADJUSTABLE VOLTAGE REGULATOR

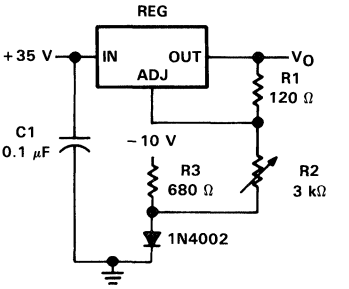
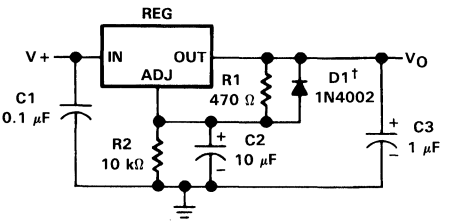


FIGURE 2. 0-V TO 30-V REGULATOR CIRCUIT



† D1 discharges C2 if output is shorted to ground.

FIGURE 3. ADJUSTABLE REGULATOR CIRCUIT WITH IMPROVED RIPPLE REJECTION

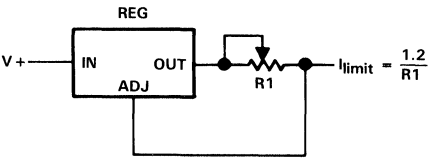


FIGURE 4. PRECISION CURRENT LIMITER CIRCUIT

NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.
B. Use of an output capacitor improves transient response but is optional.
C. V_{ref} equals the difference between the output and adjustment terminal voltages.
D. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$

TYPICAL APPLICATION DATA

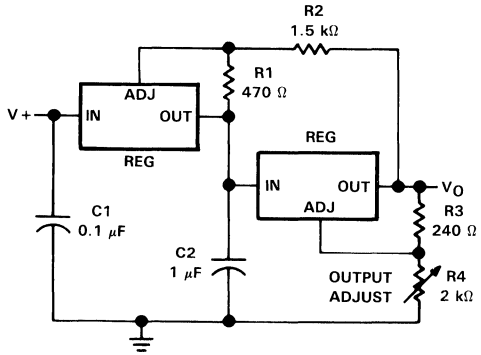


FIGURE 5. TRACKING PREREGULATOR CIRCUIT

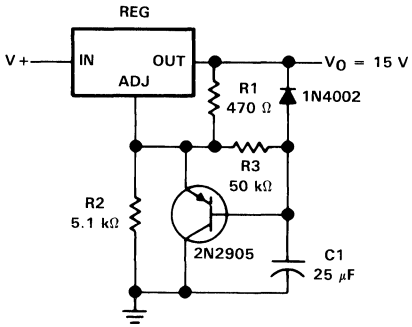


FIGURE 6. SLOW-TURN-ON 15-V REGULATOR CIRCUIT

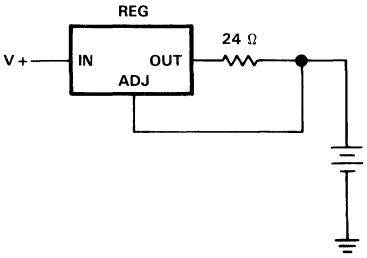
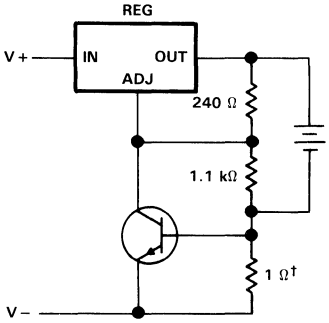


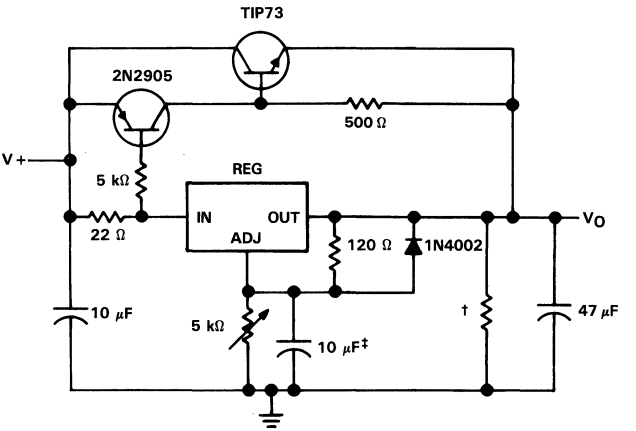
FIGURE 7. 50-mA CONSTANT-CURRENT BATTERY CHARGER CIRCUIT



†This resistor sets peak current (100 mA for 6 Ω).

FIGURE 8. CURRENT-LIMITED 6-V CHARGER

TYPICAL APPLICATION DATA



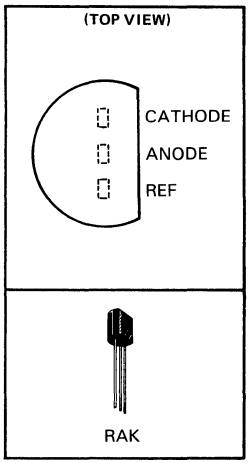
†Minimum load current is 30 mA.
‡Optional capacitor improves ripple rejection

FIGURE 9. HIGH-CURRENT ADJUSTABLE REGULATOR

D2165, JUNE 1976—REVISED MARCH 1988

- **Temperature Compensated**
- **Programmable Output Voltage**
- **Low Output Resistance**
- **Low Output Noise**
- **Sink Capability to 100 mA**

LP
SILECT PACKAGE
(TOP VIEW)

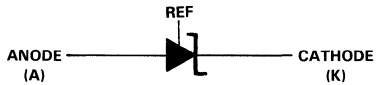


description

The TL430 is a three-terminal adjustable shunt regulator featuring excellent temperature stability, wide operating current range, and low output noise. The output voltage may be set by two external resistors to any desired value between 3 volts and 30 volts. The TL430 can replace zener diodes in many applications providing improved performance.

The TL430I is characterized for operation from −40°C to 85°C, and the TL430C is characterized for operating from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Regulator voltage (see Note 1) . . . . . 30 V
Continuous regulator current . . . . . 150 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 775 mW
Operating free-air temperature range: TL430I . . . . . −40°C to 85°C
TL430C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

	MIN	MAX	UNIT
Regulator voltage, V_Z	V_{ref}	30	V
Regulator current, I_Z	2	100	mA

Notes: 1. All voltage values are with respect to the anode terminal.
2. For operation above 25°C free-air temperature, derate at 6.2 mW/°C.

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electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		TL430I MIN	TL430I TYP	TL430I MAX	TL430C MIN	TL430C TYP	TL430C MAX	UNIT
V_{ref}	Reference input voltage	1	$V_Z = V_{ref}$, I_Z = 10 mA		2.6	2.75	2.9	2.5	2.75	3	V
αV_{ref}	Temperature coefficient of reference input voltage	1	$V_Z = V_{ref}$, I_Z = 10 mA, T_A = 0°C to 70°C			120	200		120		ppm/°C
I_{ref}	Reference input current	2	I_Z = 10 mA, R1 = 10 kΩ, R2 = ∞			3	10		3	10	μA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{ref}$			0.5	2		0.5	2	mA
I_{ZM}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{ref}$		50			50			mA
		2	V_Z = 5 V to 30 V, See Note 3		100			100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{ref}$, ΔI_Z = (52 − 2) mA			1.5	3		1.5	3	Ω
V_{nz}	Noise voltage	2	f = 0.1 Hz to 10 Hz	V_Z = 3 V		50			50		μV
				V_Z = 12 V		200			200		
				V_Z = 30 V		650			650		

NOTES: 3. The average power dissipation, $V_Z \cdot I_Z$ • duty cycle, must not exceed the maximum continuous rating in any 10-ms interval.
4. The regulator resistance for $V_Z > V_{ref}$, r_z, is given by:

$$r_z' = r_z \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

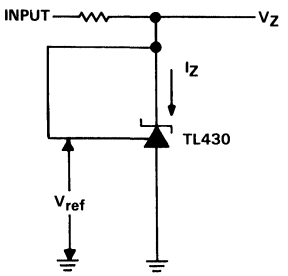
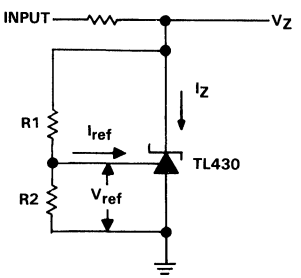


FIGURE 1. TEST CIRCUIT FOR $V_Z = V_{ref}$



$$V_Z = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \cdot R1$$

FIGURE 2. TEST CIRCUIT FOR $V_Z > V_{ref}$

TYPICAL CHARACTERISTICS

SMALL-SIGNAL REGULATOR IMPEDANCE
vs
FREQUENCY

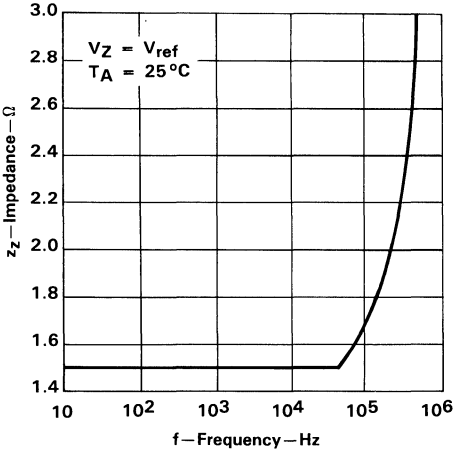


FIGURE 3

CURRENT
vs
VOLTAGE

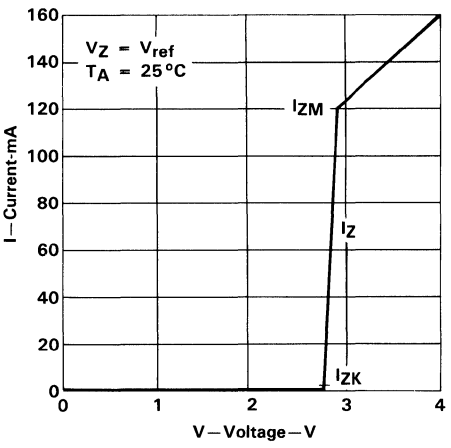


FIGURE 4

TYPICAL APPLICATION DATA

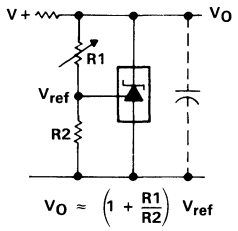


FIGURE 5. SHUNT REGULATOR

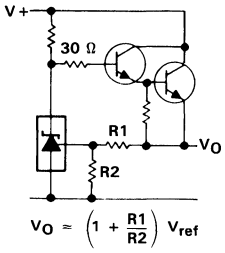


FIGURE 6. SERIES REGULATOR

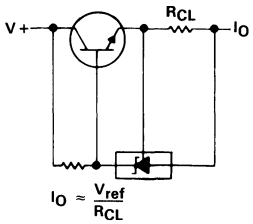


FIGURE 7. CURRENT LIMITER

TYPICAL APPLICATION DATA

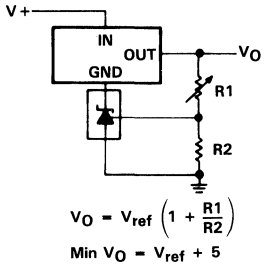


FIGURE 8. OUTPUT CONTROL OF A THREE-THERMAL FIXED REGULATOR

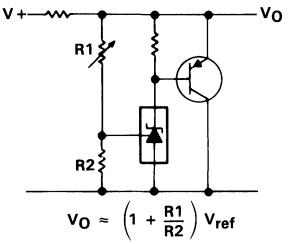


FIGURE 9. HIGHER-CURRENT APPLICATIONS

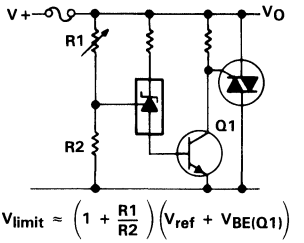


FIGURE 10. CROW BAR

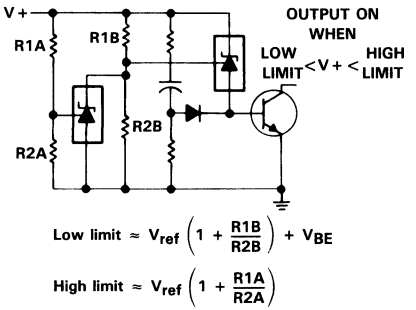


FIGURE 11. OVER-VOLTAGE/ UNDER-VOLTAGE PROTECTION CIRCUIT

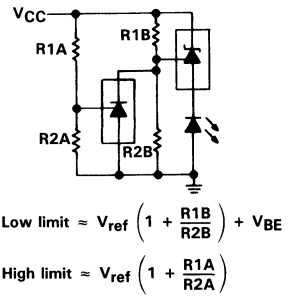


FIGURE 12. V_{CC} MONITOR

D2410, JULY 1978—REVISED AUGUST 1988

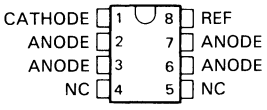
- **Equivalent Full-Range Temperature Coefficient . . . 30 ppm/°C**
- **Temperature Compensated for Operation Over Full Rated Operating Temperature Range**
- **Adjustable Output Voltage**
- **Fast Turn-On Response**
- **Sink Current Capability . . . 1 mA to 100 mA**
- **Low (0.2 Ω Typ) Dynamic Output Impedance**
- **Low Output Noise**

description

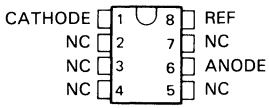
The TL431 and TL431A are three-terminal adjustable shunt regulators with specified thermal stability over applicable industrial and commercial temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes in many applications.

The TL431M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL431I and TL431AI are characterized for operation from −40°C to 85°C, and the TL431C and TL431AC are characterized for operation from 0°C to 70°C.

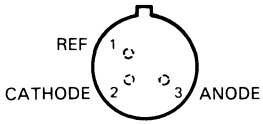
TL431I, TL431AI, TL431C, TL431AC . . . D PACKAGE
(TOP VIEW)



TL431M . . . JG PACKAGE
(TOP VIEW)

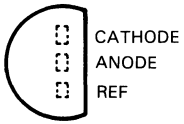


TL431M . . . LD PACKAGE
(TOP VIEW)

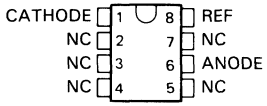


THE ANODE IS IN ELECTRICAL CONTACT WITH THE CASE.

TL431I, TL431AI, TL431C, TL431AC . . . LP PACKAGE
(TOP VIEW)

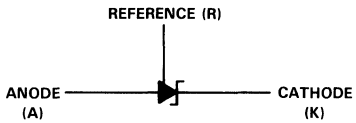


TL431I, TL431AI, TL431C, TL431AC . . . P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



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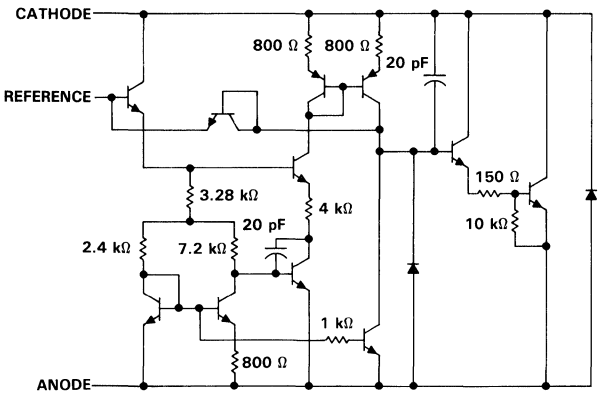
schematic



Component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Cathode voltage (see Note 1) . . . . . 37 V
Continuous cathode current range . . . . . −100 mA to 150 mA
Reference input current range . . . . . −50 μA to 10 mA
Continuous power dissipation . . . . . See Dissipation Rating Tables 1 and 2
Operating free-air temperature range: TL431C, TL431AC . . . . . 0°C to 70°C
TL431I, TL431AI . . . . . −40°C to 85°C
TL431M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: LD or JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, LP, or P package . . . . . 260°C

NOTE 1: Voltage values are with respect to the anode terminal unless otherwise noted.

DISSIPATION RATING TABLE 1—FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	825 mW	6.6 mW/°C	528 mW	429 mW	
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LD	275 mW	2.2 mW/°C	176 mW	143 mW	55 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 125°C$ POWER RATING
LD	1550 mW	12.4 mW/°C	310 mW

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	36	V
Cathode current, I_K (for regulation)	1	100	mA

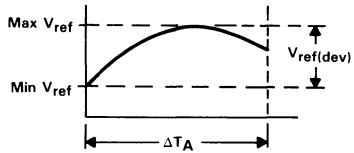
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431M			TL431I			TL431C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2400	2495	2600	2440	2495	2550	2440	2495	2550	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†			22			5	30		4	17	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−3		−1.4	−2.7		−1.4	−2.7	$\frac{mV}{V}$
				ΔV_{KA} = 36 V − 10 V		−1	−2.3		−1	−2		−1	−2	
I_{ref}	Reference input current	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	8		2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			1			0.8	2.5		0.4	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	1.5		0.4	1		0.4	1	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	3		0.1	1		0.1	1	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.9		0.2	0.5		0.2	0.5	Ω

† Full temperature range is −55°C to 125°C for the TL431M, −40°C to 85°C for the TL431I, and 0°C to 70°C for the TL431C.

‡ The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$|\alpha V_{ref}| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ @\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device,

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature (see Figure 8).

Example: Max V_{ref} = 2496 mV @ 30°C, Min V_{ref} = 2492 mV @ 0°C, V_{ref} = 2495 mV @ 25°C, ΔT_A = 70°C for TL431C

$$|\alpha V_{ref}| = \frac{\left(\frac{4\ mV}{2495\ mV}\right) \times 10^6}{70°C} \approx 23\ ppm/°C$$

Because minimum V_{ref} occurs at the lower temperature, the coefficient is positive.

§ The dynamic impedance is defined as:

$$|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operated with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

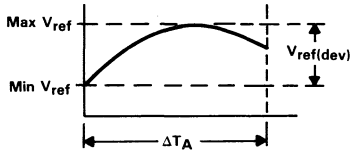
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431AI MIN	TL431AI TYP	TL431AI MAX	TL431AC MIN	TL431AC TYP	TL431AC MAX	UNIT
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2470	2495	2520	2470	2495	2520	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†			5	25		4	15	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−2.7		−1.4	−2.7	$\frac{mV}{V}$
				ΔK_{VA} = 36 V − 10 V		−1	−2		−1	−2	
I_{ref}	Reference input current	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			0.8	2.5		0.8	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	0.7		0.4	0.6	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5		0.1	0.5	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.5		0.2	0.5	Ω

†Full temperature range is −40°C to 85°C for TL431AI and 0°C to 70°C for TL431AC.

‡The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$|\alpha V_{ref}| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ @\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

§The dynamic impedance is defined as: $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors, see figure 2, the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I}, \text{ which is approximately equal to } |z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

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PARAMETER MEASUREMENT INFORMATION

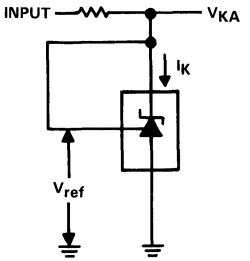


FIGURE 1. TEST CIRCUIT FOR $V_{KA} = V_{ref}$

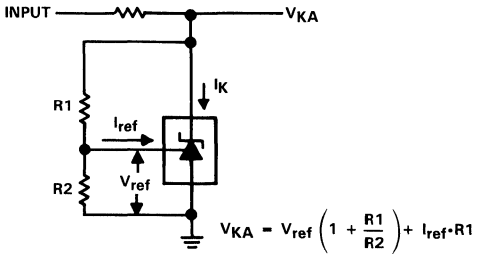


FIGURE 2. TEST CIRCUIT FOR $V_{KA} > V_{ref}$

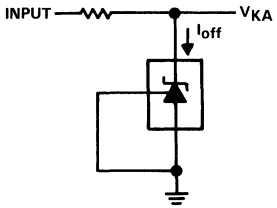


FIGURE 3. TEST CIRCUIT FOR I_{off}

TYPICAL CHARACTERISTICS

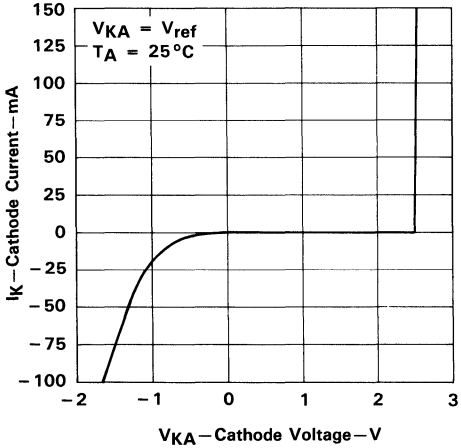


FIGURE 4

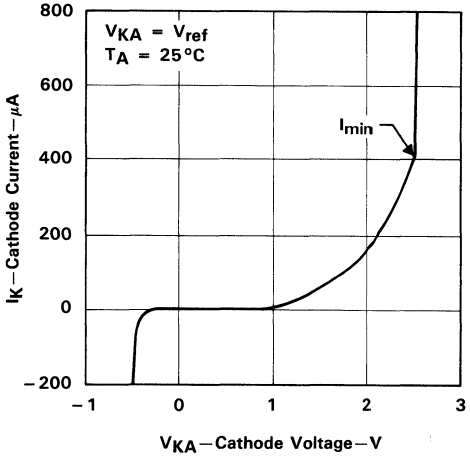


FIGURE 5

TYPICAL CHARACTERISTICS

OFF-STATE CATHODE CURRENT
vs
FREE-AIR TEMPERATURE†

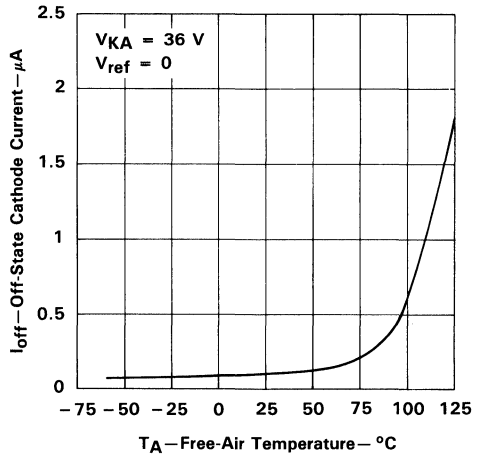


FIGURE 6

NOISE VOLTAGE
vs
FREQUENCY

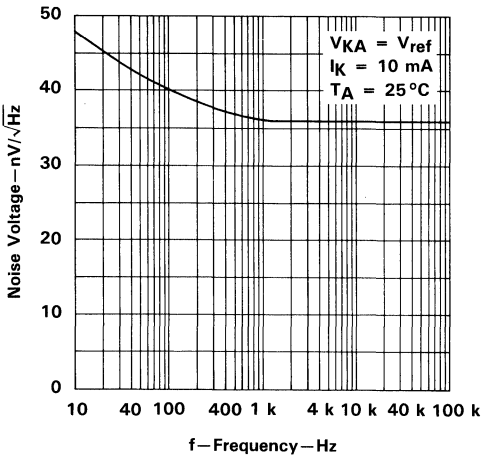


FIGURE 7

REFERENCE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

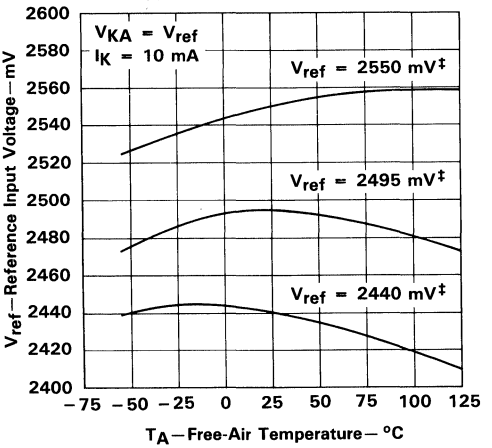


FIGURE 8

REFERENCE INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

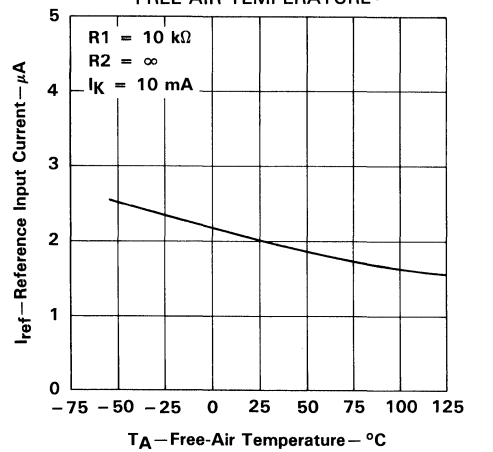


FIGURE 9

†For TL431I, TL431AI, TL431C, and TL431AC, the data applies only for the portions of the curves that lie within their recommended operating temperature ranges.
‡Data is for devices having the indicated value of V_{ref} at I_K = 10 mA, T_A = 25°C.

TYPICAL CHARACTERISTICS

CHANGE IN REFERENCE INPUT VOLTAGE
vs
CATHODE VOLTAGE

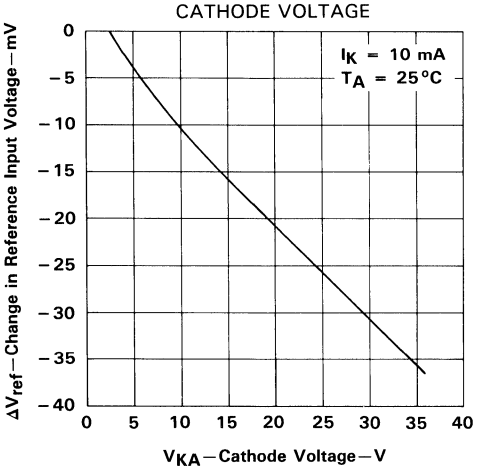


FIGURE 10

DYNAMIC IMPEDANCE
vs
FREE-AIR TEMPERATURE†

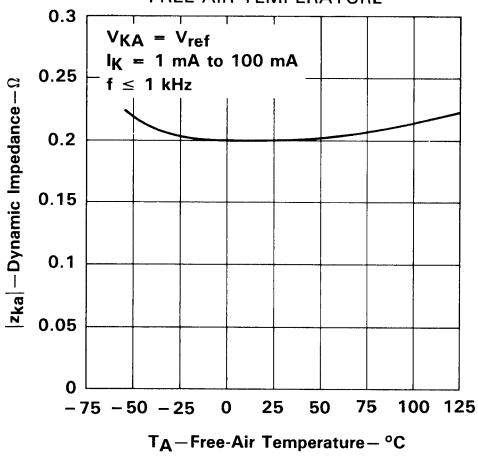
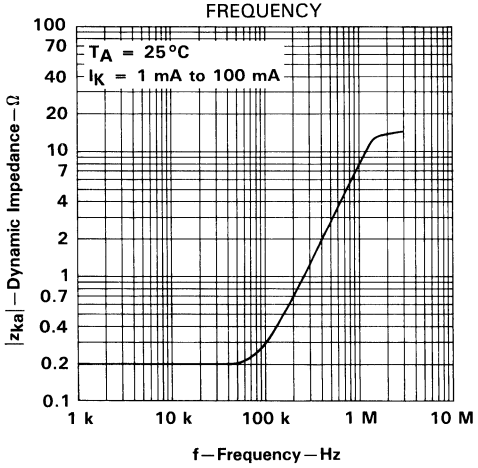
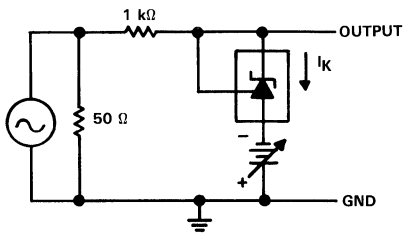


FIGURE 11

DYNAMIC IMPEDANCE
vs
FREQUENCY



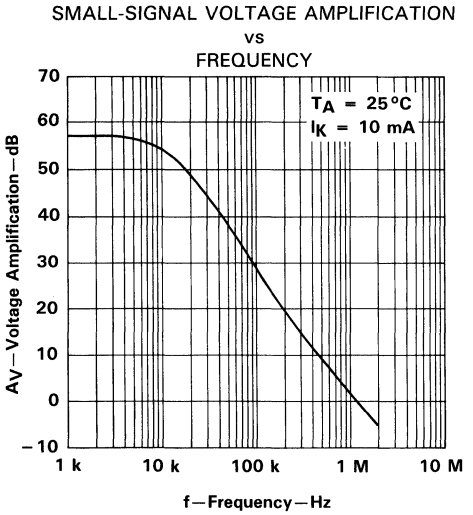


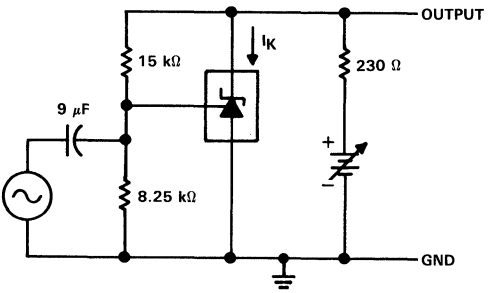
TEST CIRCUIT FOR DYNAMIC IMPEDANCE

FIGURE 12

†For TL431I, TL431AI, TL431C, and TL431AC, the data applies only for the portions of the curves that lie within their recommended operating temperature ranges.

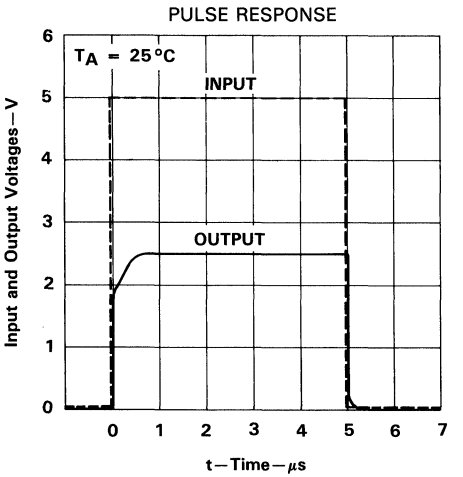
TYPICAL CHARACTERISTICS

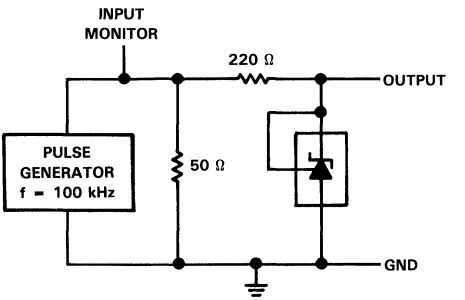




TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

FIGURE 13

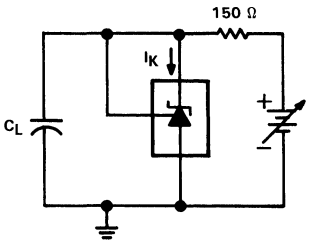




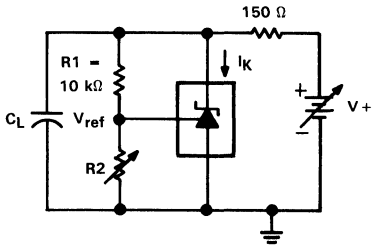
TEST CIRCUIT FOR PULSE RESPONSE

FIGURE 14

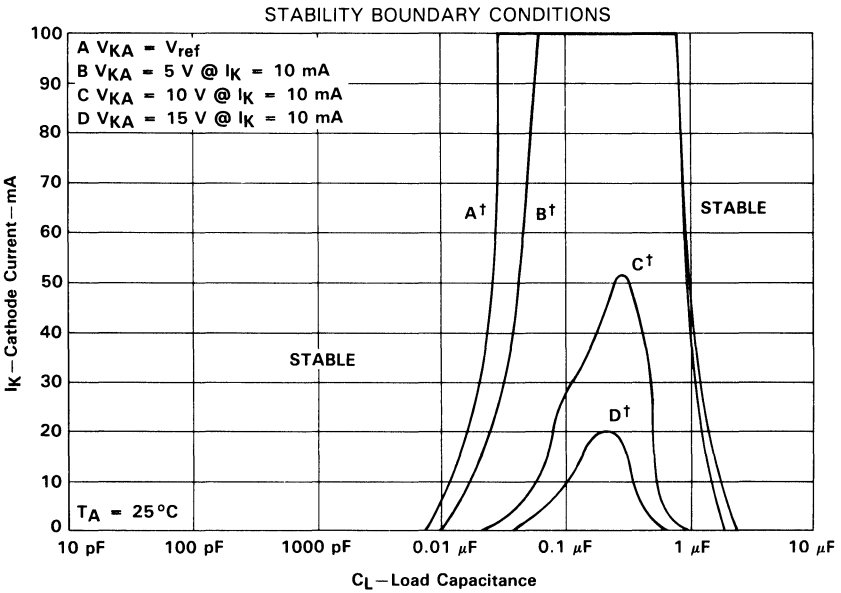
TYPICAL CHARACTERISTICS



TEST CIRCUIT FOR CURVE A BELOW



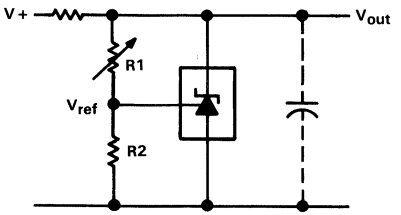
TEST CIRCUIT FOR CURVES B, C, AND D BELOW



† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V+ and C_L were then adjusted to determine the ranges of stability.

FIGURE 15

TYPICAL APPLICATIONS



$$V_{out} \approx \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 16. SHUNT REGULATOR

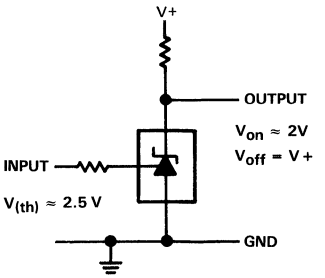
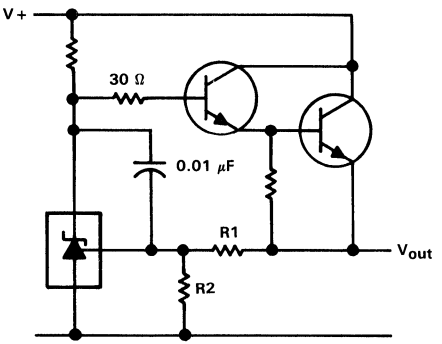
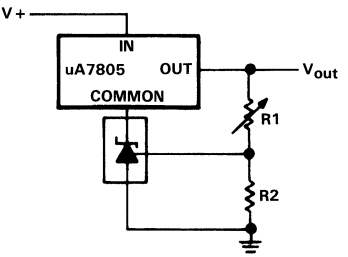


FIGURE 17. SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



$$V_{out} \approx \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 18. SERIES REGULATOR

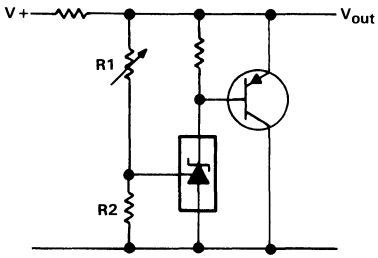


$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

$$\text{Min } V_{out} = V_{ref} + 5\text{ V}$$

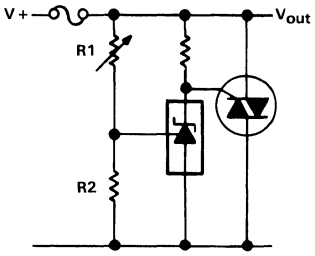
FIGURE 19. OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR

TYPICAL APPLICATIONS



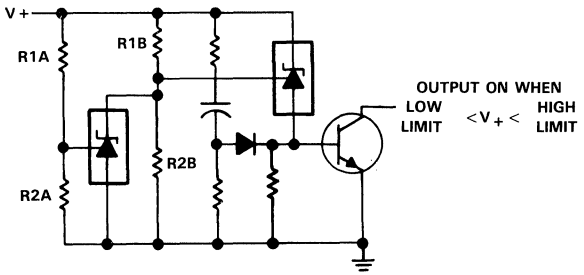
$$V_{out} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 20. HIGHER-CURRENT SHUNT REGULATOR



$$V_{limit} \approx \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 21. CROW BAR

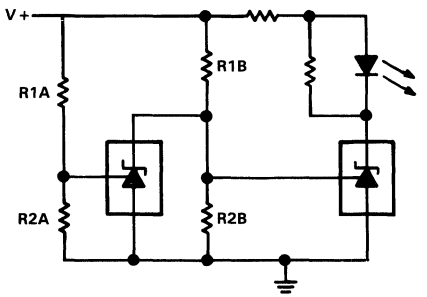


$$\text{Low limit} \approx V_{ref}\left(1 + \frac{R1B}{R2B}\right) + V_{BE}$$

$$\text{High limit} \approx V_{ref}\left(1 + \frac{R1A}{R2A}\right)$$

FIGURE 22. OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION CIRCUIT

TYPICAL APPLICATIONS

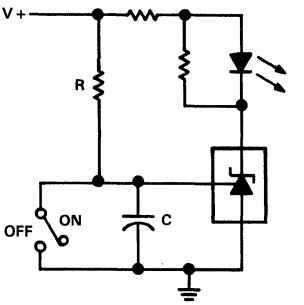


$$\text{Low limit} \approx V_{ref}\left(1 + \frac{R1B}{R2B}\right)$$

$$\text{High limit} \approx V_{ref}\left(1 + \frac{R1A}{R2A}\right)$$

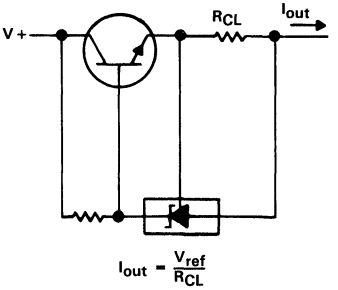
LED ON WHEN LOW LIMIT $< V+ <$ HIGH LIMIT

FIGURE 23. VOLTAGE MONITOR



$$\text{Delay} = R \cdot C \cdot \ln \frac{V+}{(V+) - V_{ref}}$$

FIGURE 24. DELAY TIMER



$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

FIGURE 25. CURRENT LIMITER OR CURRENT SOURCE

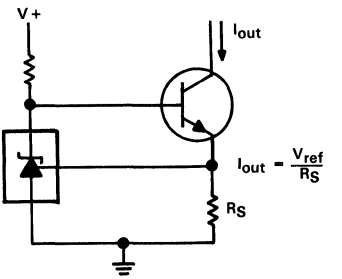


FIGURE 26. CONSTANT-CURRENT SINK

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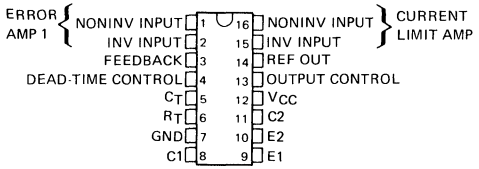
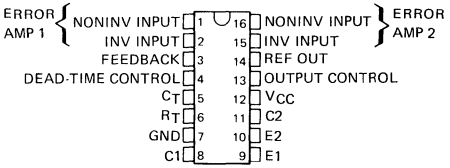
D2535, JANUARY 1983—REVISED OCTOBER 1988

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, 5%**
- **Circuit Architecture Allows Easy Synchronization**
- **TL493 has Output Current-Limit Sensing**
- **TL495 has On-Chip 39-V Zener and External Control of Output Steering**

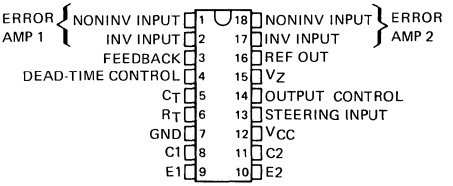
TL493C . . . D OR N PACKAGE
(TOP VIEW)



TL494I, TL494C . . . D, J, OR N PACKAGE
(TOP VIEW)



TL495C . . . N PACKAGE
(TOP VIEW)



description

The TL493, TL494, and TL495 each incorporate on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to his application.

The TL493 contains an error amplifier, current-limiting amplifier, an on-chip adjustable oscillator, a dead-time control comparator, pulse-steering control flip-flop, a 5-volt, 5%-precision regulator, and output-control circuits.

The error amplifier exhibits a common-mode voltage range from -0.3 volts to $V_{CC} - 2$ volts. The current-limit amplifier exhibits a common-mode voltage range from -0.3 volts to 3 volts with an offset voltage of approximately 80 millivolts in series with the inverting input to ease circuit design requirements. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common circuits in synchronous multiple-rail power supplies.

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL493	TL494	TL495
TL49—I	*	D,J,N	*
TL49—C	D,N	D,J,N	N

*These combinations are not defined by this data sheet.

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT (TL495 only)	
V_I = 0	Open	Single-ended or parallel output
$V_I = V_{ref}$	Open	Normal push-pull operation
$V_I = V_{ref}$	V_I = 0	PWM Output at Q1
$V_I = V_{ref}$	$V_I = V_{ref}$	PWM Output at Q2

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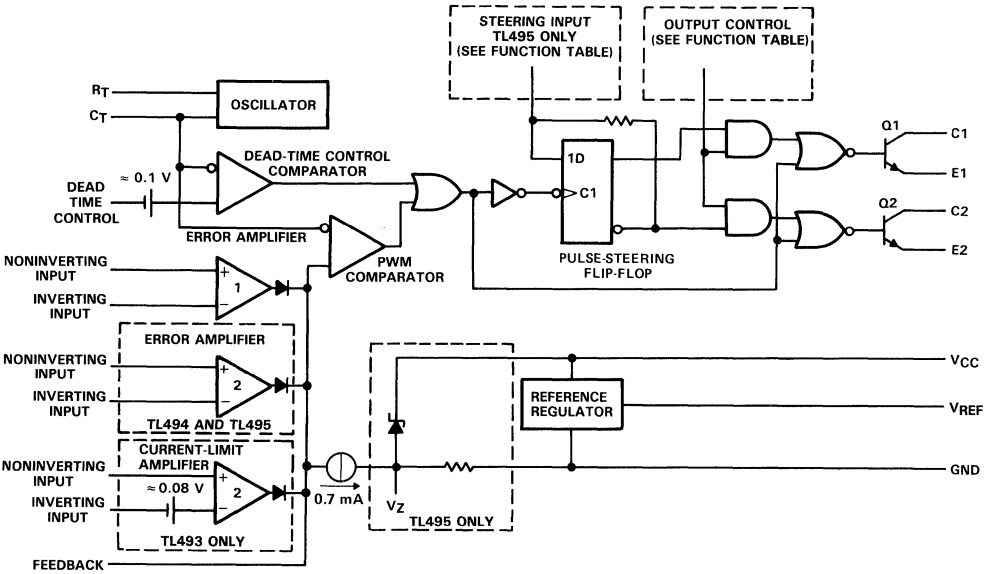
description (continued)

The uncommited output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL493 and TL494 are similar except that an additional error amplifier is included in the TL494 instead of a current-limiting amplifier. The TL495 provides the identical functions found in the TL494. In addition, it contains an on-chip 39-volt diode for high-voltage applications where V_{CC} is greater than 40 volts, and an output-steering control that overrides the internal control of the pulse-steering flip-flop.

The TL494I is characterized for operation from −25°C to 85°C. The TL493C, TL494C, and TL495C are characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL494I	TL493C TL494C	TL495C	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	41	V
Amplifier input voltage	$V_{CC}+0.3$	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	41	41	41	V
Collector output current	250	250	250	mA
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−25 to 85	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260	260	260	°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	900	7.6 mW/°C	25°C	608 mW	494 mW
J	1000	8.2 mW/°C	28°C	656 mW	533 mW
N	1000	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

	TL494I		TL493C TL494C TL495C		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10 000	0.47	10 000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	kHz
Operating free-air temperature, T_A	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL493C, TL494I, TL494C, TL495C			UNIT
		MIN	TYP‡	MAX	
Output voltage (V_{ref})	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		0.2%	1%	
Short-circuit output current§	V_{ref} = 0		35		mA

oscillator section (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL493C, TL494I, TL494C, TL495C			UNIT
		MIN	TYP‡	MAX	
Frequency	C_T = 0.01 μF, R_T = 12 kΩ		10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, and T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%		
Frequency change with temperature#	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = MIN to MAX			1%	

amplifier sections (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	Error	V_O (pin 3) = 2.5 V		2	10	mV
	Current-limit (TL493 only)			80		
Input offset current		V_O (pin 3) = 2.5 V		25	250	nA
Input bias current		V_O (pin 3) = 2.5 V		0.2	1	μA
Common-mode input voltage range	Error	V_{CC} = 7 V to 40 V	−0.3 to V_{CC}−2			V
	Current limit (TL493 only)		−0.3 to 3			
Open-loop voltage amplification	Error	ΔV_O = 3 V, R_L = 2 kΩ V_O = 0.5 V to 3.5 V	70	95		dB
	Current-limit (TL493 only)			90		
Unity-gain bandwidth		V_O = 0.5 V to 3.5 V R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	Error	ΔV_O = 40 V, T_A = 25°C	65	80		dB
	Current-limit (TL493 only)			70		
Output sink current (pin 3)		V_{ID} = −15 mV to −5 V, $V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA
Output source current (pin 3)		V_{ID} = 15 mV to 5 V, $V_{(pin\ 3)}$ = 3.5 V	−2			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$
# Temperature coefficient of timing capacitor and timing resistor not taken into account.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS	TL493C, TL494I, TL494C, TL495C			UNIT
			MIN	TYP†	MAX	
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter-follower	V_C = 15 V, I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5	mA

dead-time control-section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	V_I (pin 4) = 0, C_T = 0.1 μF, R_T = 12 kΩ		45%		
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA

steering control (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Input current	V_I = 0.4 V		−200	μA
	V_I = 2.4 V		200	

zener-diode circuit (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Breakdown voltage	V_{CC} = 41 V, I_Z = 2 mA		39		V
Sink current	$V_{I(pin\ 15)}$ = 1 V		0.3		mA

total device

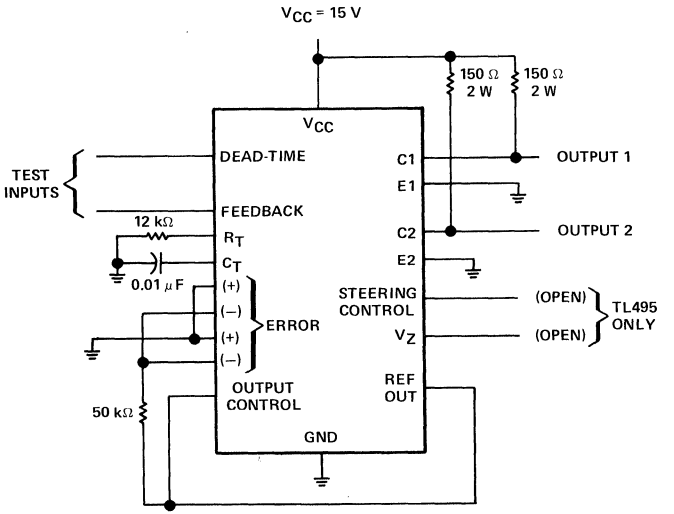
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		6	10	mA
		V_{CC} = 40 V		9	15	
Average supply current	$V_{I(pin\ 4)}$ = 2 V,	See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

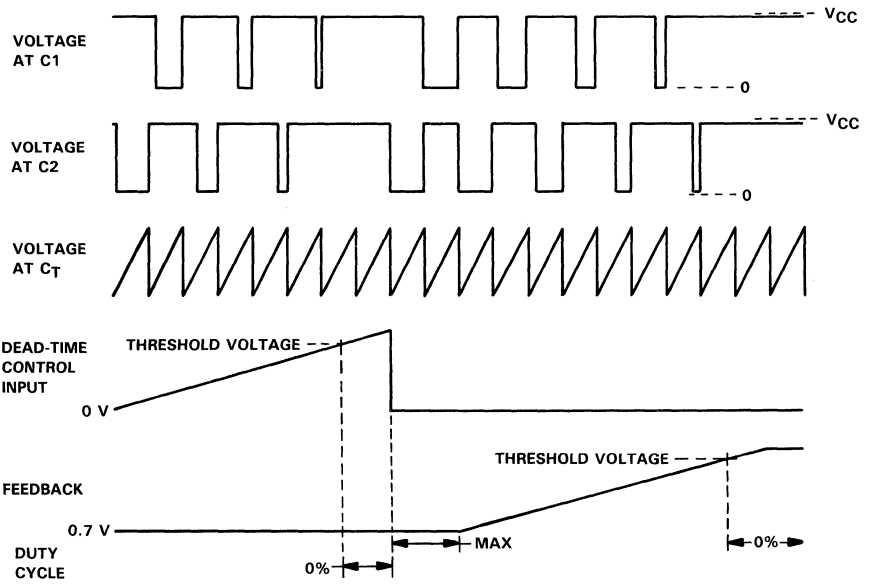
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time			40	100	ns

†All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1. OPERATIONAL TEST CIRCUIT AND WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION

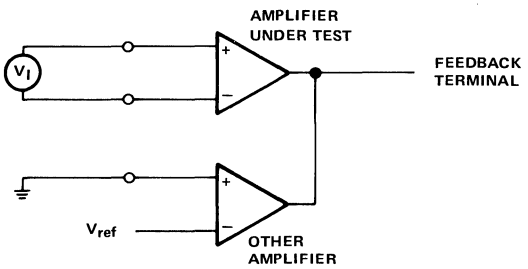


FIGURE 2. AMPLIFIER CHARACTERISTICS

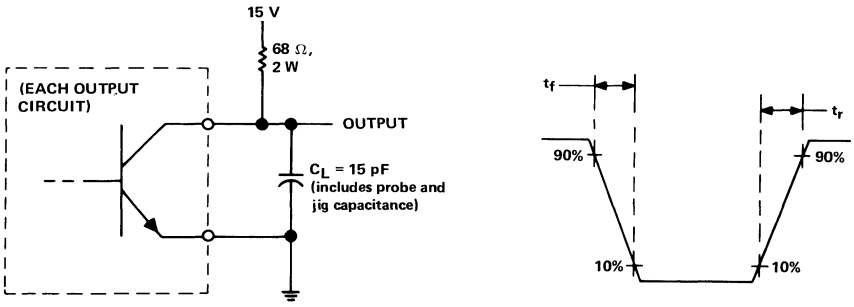


FIGURE 3. COMMON-EMITTER CONFIGURATION

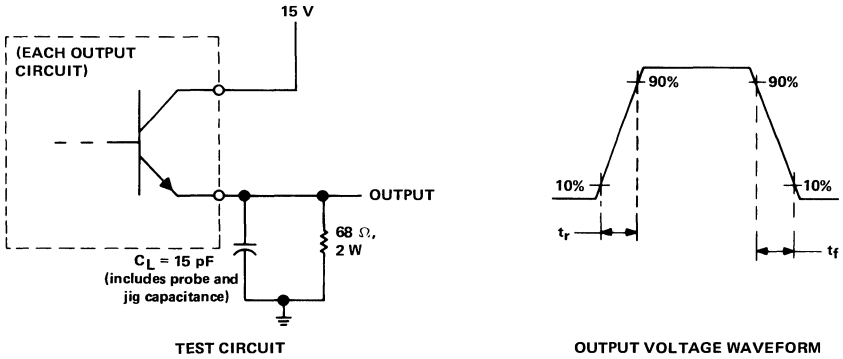


FIGURE 4. EMITTER-FOLLOWER CONFIGURATION

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND
FREQUENCY VARIATION† vs
TIMING RESISTANCE

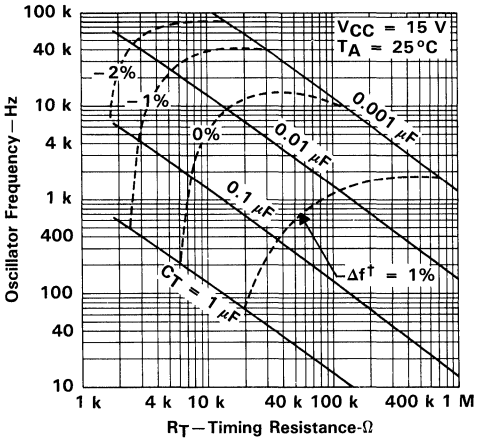


FIGURE 5

AMPLIFIER VOLTAGE AMPLIFICATION
vs
FREQUENCY

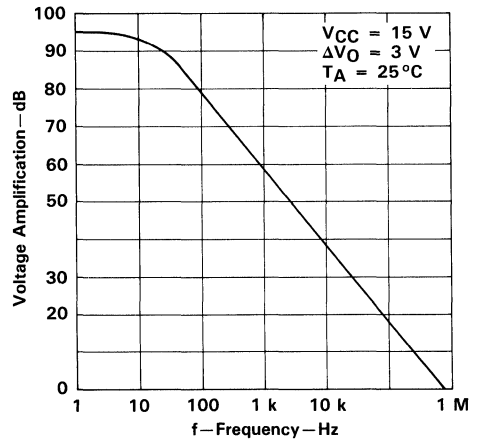


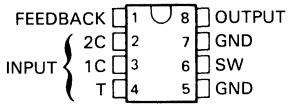
FIGURE 6

†Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D2486, AUGUST 1978—REVISED FEBRUARY 1988

- **Internal Step-Up Switching Regulator**
- **Fixed 9-Volt Output**
- **Charges Battery Source During Transformer-Coupled-Input Operation**
- **Minimum External Components Required (1 Inductor, 1 Capacitor, 1 Diode)**
- **1- or 2-Cell-Input Operation**

D OR P PACKAGE
(TOP VIEW)



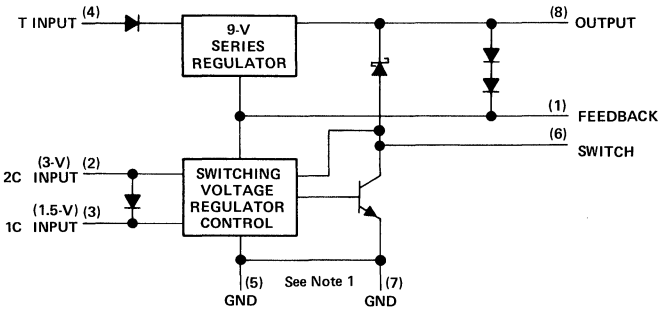
Pins 5 and 7 are connected together internally.

description

The TL496 power supply control circuit is designed to provide a 9-volt regulated supply from a variety of input sources. Operable from a 1- or 2-cell battery input, the TL496 performs as a switching regulator with the addition of a single inductor and filter capacitor. When ac coupled with a step-down transformer, the TL496 operates as a series regulator to maintain the regulated output voltage and, with the addition of a single catch diode, time shares to recharge the input batteries.

The design of the TL496 allows minimal supply current drain during stand-by operation (125 μA typical). With most battery sources this allows a constant bias to be maintained on the power supply. This makes power instantly available to the system thus eliminating power-up sequencing problems.

functional block diagram



NOTE 1: Pins 5 and 7, though connected together internally, must both be terminated to ground to ensure proper circuit operation.

absolute maximum ratings

Input voltage:
- Pin 2 . . . . . 3.5 V
- Pin 3 . . . . . 2.5 V
- Pin 4 . . . . . 20 V

Output voltage (Pin 6) . . . . . 12 V
Diode reverse voltage (Pin 8) . . . . . 12 V
Switch current (Pin 6) . . . . . 1.2 A
Diode current (Pin 8) . . . . . 1.2 A
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

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DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, one-cell operation (pins 2 and 3 to ground)	1.1	1.5	V
Input voltage, two-cell operation (pin 2 to ground)	2.3	3	V
Input voltage, one-cell or two-cell operation (pin 4 to ground)	V_O+2	20	V

electrical characteristics at 25°C free-air temperature

series regulator section (input is pin 4)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage	V_I = 5 V, I_O = −50 mA			1.5	2	V
Regulated output voltage	V_I = 20 V	I_O = −50 μA	9.5	10.1	11.2	V
		I_O = −80 mA	9.0	10.0	11.0	
	V_I = 20 V, Pin 1 shorted to pin 8	I_O = −50 μA	8.5	9.0	9.7	
		I_O = −80 mA	6.7	8.6	9.5	
Standby current (pin 4)	V_I = 20 V, Pin 8 at 12 V				400	μA
Reverse current thru pin 4	V_I = −1.5 V, 1 mA into pin 8				−25	μA

output switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MAX
$V_{CE(sat)}$	Collector-emitter saturation voltage	800 mA into pin 6, Pin 2 at 2.25 V		0.35	0.6	V

diode (pin 6 to pin 8)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward voltage	I_F = 1.5 A		1.6	2.5	V
I_R	Reverse current thru pin 6	Pin 6 at 0 V, 1 mA into pin 8			−20	μA

control section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On-state current (pin 2)	Pins 1 and 8 at 0 V, Pin 2 at 3 V		60	100	mA
Standby current (pin 1)	Pin 1 at 8.65 V, Pins 2 and 6 at 3 V			40	μA
Standby current (pin 2 and 6)	Pin 1 at 8.65 V, Pins 2 and 6 at 3 V			400	μA
Start-up current (current into pin 6 to initiate cycle)	Pins 1, 2, 6 and 8 at 2.25 V	16			mA

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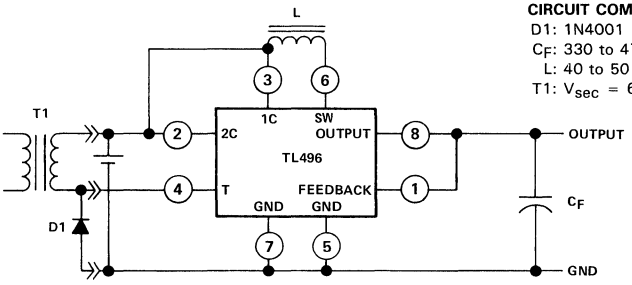
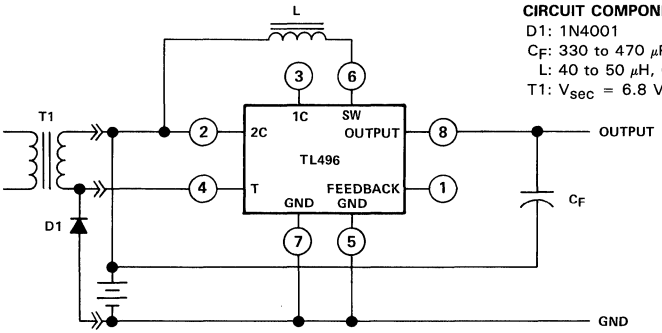
TYPICAL APPLICATION DATA



CIRCUIT COMPONENT INFORMATION
D1: 1N4001
C_F: 330 to 470 μF, 10 V, electrolytic
L: 40 to 50 μH, Q $\approx$ 3, R < 0, 15 Ω
T1: V_{sec} = 6.8 V RMS typ., R_{sec} = 11 Ω typ.

FIGURE 1. ONE-CELL OPERATION



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L: 40 to 50 μH, Q $\approx$ 3, R < 0, 15 Ω
T1: V_{sec} = 6.8 V RMS typ., R_{sec} = 11 Ω typ.

FIGURE 2. TWO-CELL OPERATION

typical electrical characteristics for circuits above

PARAMETER		ONE-CELL OPERATION (FIGURE 1)	TWO-CELL OPERATION (FIGURE 2)
Input current	No load	125 uA	125 uA
	R_L = 120 Ω	525 mA	405 mA
Output voltage	Without T1	7.2 V	8.6 V
	With T1	8.6 V	10 V
Output current capability		40 mA	80 mA
Efficiency		66%	66%
Battery life (AA NiCad) no load		60 days	166 days

functional description

The TL496 is designed to operate from either a single-cell or two-cell source. To operate the device from a single-cell (1.1 V to 1.5 V) the source must be connected to both inputs 1C and 2C as shown in Figure 1. For two-cell operation (2.3 V to 3.0 V), the input is applied to the 2C input only and the 1C input is left open (see Figure 2).

battery operation

The TL496 operates as a switching regulator from a battery input. The cycle is initiated when a low voltage condition is sensed by the internal feedback (the thresholds at pin 1 and pin 8 are approximately 7.2 and 8.6 volts respectively). An internal latch is set and the output transistor is turned "on." This causes the current in the external inductor (L) to increase linearly until it reaches a peak value of approximately 1 ampere. When the peak current is sensed the internal latch is reset and the output transistor is turned "off." The energy developed in the inductor is then delivered to the output storage capacitor through the blocking diode. The latch remains in the off state until the feedback signal indicates the output voltage is again deficient.

transformer-coupled operation

The TL496 operates on alternate half cycles of the ac input during transformer-coupled operation to, first, sustain the output voltage and, second, recharge the batteries. The TL496 performs like a series regulator to supply charge to the output filter/storage capacitor during the first half cycle. The output voltage of the series regulator is slightly higher voltage than that created by the switching circuit; this maintains the feedback voltage above the switching regulator control circuit threshold. This effectively inhibits the switching control circuitry. During the second half cycle an external diode (1N4001) is used to clamp the negative going end of the transformer secondary to ground thus allowing the positive-going end (end connected to V+side of battery) to pump charge into the stand-by batteries.

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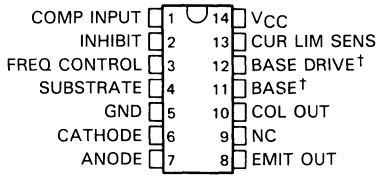
D2225, JUNE 1976—REVISED OCTOBER 1988

- **High Efficiency . . . 60% or Greater**
- **Output Current . . . 500 mA**
- **Input Current Limit Protection**
- **TTL Compatible Inhibit**
- **Adjustable Output Voltage**
- **Input Regulation . . . 0.2% Typ**
- **Output Regulation . . . 0.4% Typ**
- **Soft Start-up Capability**

TL497AM . . . J PACKAGE
TL497AI, TL497AC . . . D, J, OR N PACKAGE
(TOP VIEW)



NC—No internal connection

† The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

description

The TL497A incorporates on a single monolithic chip all the active functions required in the construction of a switching voltage regulator. It can also be used as the control element to drive external components for high-power-output applications. The TL497A was designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

The TL497A is a fixed-on-time variable-frequency switching voltage regulator control circuit. The on-time is programmed by a single external capacitor connected between the frequency control pin and ground. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC}, thus the one time remains constant over the specified range of input voltage (5 to 12 V). Typical on-times for various values of C_T are as follows:

TIMING CAPACITOR, C_T (pF)	200	250	350	400	500	750	1000	1500	2000
ON-TIME (μs)	19	22	26	32	44	56	80	120	180

The output voltage is controlled by an external resistor ladder network (R1 and R2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 V (relative to the substrate pin) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T. The internal transistor may be used directly for switching currents up to 500 mA. Its collector and emitter are uncommitted and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor is also available for blocking or commutating purposes. The TL497A also has on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL}, connected between pin 14 and pin 13. The current-limit circuitry is activated when 0.7 V is developed across R_{CL}. External gating is provided by the inhibit input. When the inhibit input is high, the output is turned off.

Simplicity of design is a primary feature of the TL497A. With only six external components (three resistors, two capacitors, and one inductor), the TL497A will operate in numerous voltage conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497A replaces the TL497 in all applications.

The TL497AM is characterized for operation over the full military temperature range of −55°C to 125°C, the TL497AI is characterized for operation from −25°C to 85°C, and the TL497AC from 0°C to 70°C.

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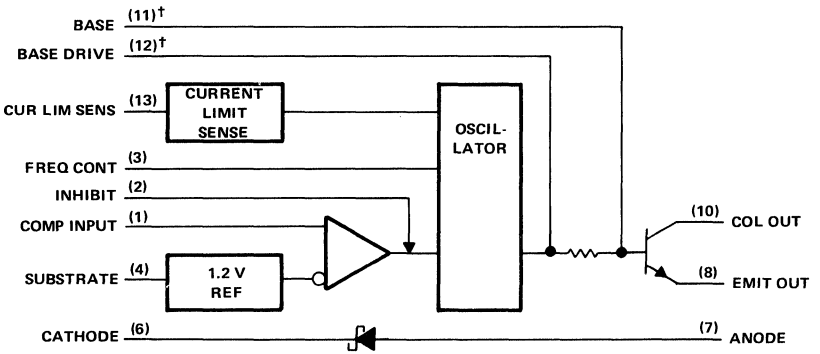
functional block diagram



† The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage, V_{CC} (see Note 1) . . . . . 15 V
Output voltage . . . . . 35 V
Comparator input voltage . . . . . 5 V
Inhibit input voltage . . . . . 5 V
Diode reverse voltage . . . . . 35 V
Power switch current . . . . . 750 mA
Diode forward current . . . . . 750 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL497AM . . . . . −55°C to 125°C
TL497AI . . . . . −25°C to 85°C
TL497AC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1. All voltage values except diode voltages are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW	
J (TL__AM)	1000 mW	11.0 mW/°C	59°C	880 mW	715 mW	275 mW
J (TL__AI)	1000 mW	8.2 mW/°C	28°C	656 mW	533 mW	
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW	

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

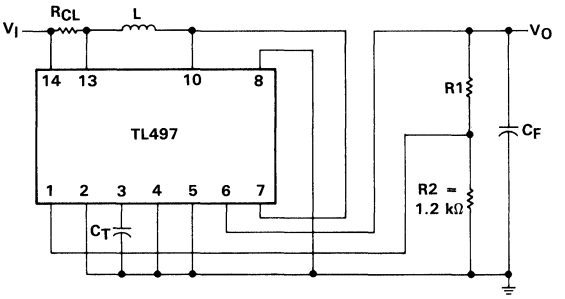
		MIN	MAX	UNIT
Input voltage, V_I		4.5	12	V
High-level inhibit input voltage, V_{IH}		2.5		V
Low-level inhibit input voltage, V_{IL}			0.8	V
Output voltage	Step-up configuration (see Figure 1)	$V_I + 2$	30	V
	Step-down configuration (see Figure 2)	V_{ref}	$V_I - 1$	
	Inverting regulator (see Figure 3)	$-V_{ref}$	-25	
Power switch current			500	mA
Diode forward current			500	mA

electrical characteristics at specified free-air temperature, V_I = 6 V (unless otherwise noted)

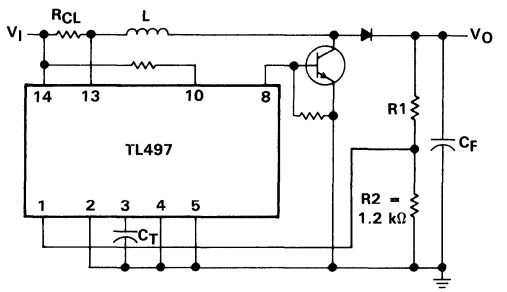
PARAMETER	TEST CONDITIONS†		TL497AM, TL497AI			TL497AC			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level inhibit input current	$V_{I(I)}$ = 5 V	Full range		0.8	1.5		0.8	1.5	mA
Low-level inhibit input current	$V_{I(I)}$ = 0 V	Full range		5	20		5	10	μA
Comparator reference voltage	V_I = 4.5 V to 6 V	Full range	1.14	1.20	1.26	1.08	1.20	1.32	V
Comparator input bias current	V_I = 6 V	Full range		40	100		40	100	μA
Switch on-state voltage	V_I = 4.5 V, I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
	V_I = 4.5 V, I_O = 500 mA	Full range			1			0.85	
Switch off-state current	V_I = 4.5 V, V_O = 30 V	25°C		10	50		10	50	μA
		Full range			500			200	
Current-limit sense voltage	V_I = 6 V	25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA	Full range		0.75	0.95		0.75	0.85	V
	I_O = 100 mA	Full range		0.9	1.1		0.9	1	
	I_O = 500 mA	Full range		1.33	1.75		1.33	1.55	
Diode reverse voltage	I_O = 500 μA	Full range	30						V
	I_O = 200 μA	Full range				30			
On-state supply current		25°C		11	14		11	14	mA
		Full range			16			15	
Off-state supply current		25°C		6	9		6	9	mA
		Full range			11			10	

† Full range for TL497AM is −55°C to 125°C, for TL497AI is −25°C to 85°C, and for TL497AC is 0°C to 70°C.
‡ All typical values are at T_A = 25°C.

TYPICAL APPLICATION DATA



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\, I_O \text{ max} \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\, t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T(pF) \approx 12\, t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s)\ \frac{\left[\frac{V_I}{V_O}\, I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

FIGURE 1. POSITIVE REGULATOR, STEP-UP CONFIGURATIONS

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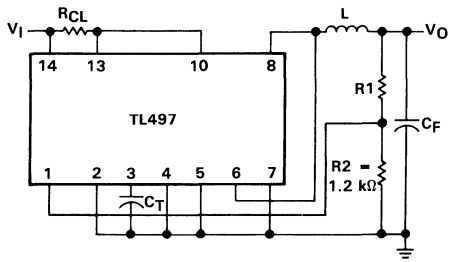
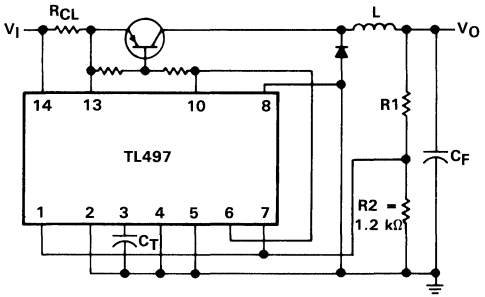
TYPICAL APPLICATION DATA



BASIC CONFIGURATION
I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

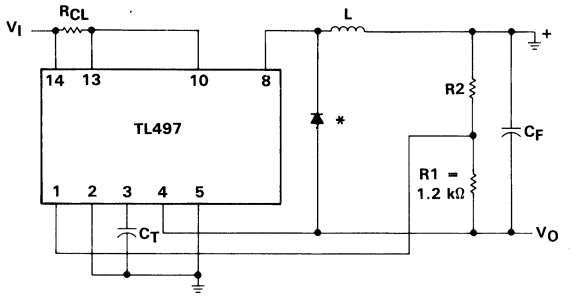
- $I_{PK} = 2\ I_O$ max
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{PK}}\ t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

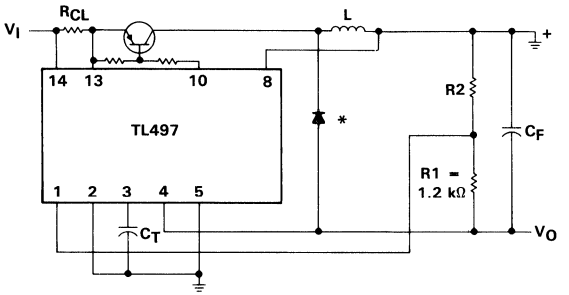
- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \dfrac{0.5\ V}{I_{PK}}$
- $C_F(\mu F) \approx t_{on}(\mu s)\ \dfrac{\left[\dfrac{V_I}{V_O} I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

FIGURE 2. POSITIVE REGULATOR, STEP-DOWN CONFIGURATIONS

TYPICAL APPLICATION DATA



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

- $I_{PK} = 2\ I_O\ max \left[1 + \frac{|V_O|}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\ t_{on}(\mu s)$

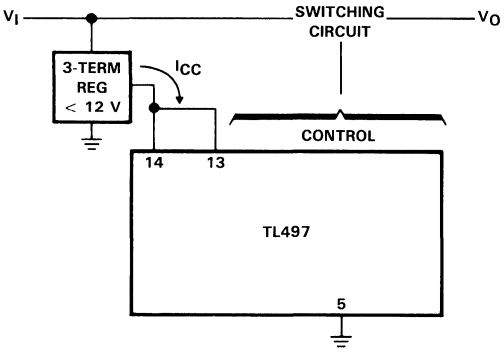
Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R2 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s)\ \frac{\left[\frac{V_I}{V_O}\ I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

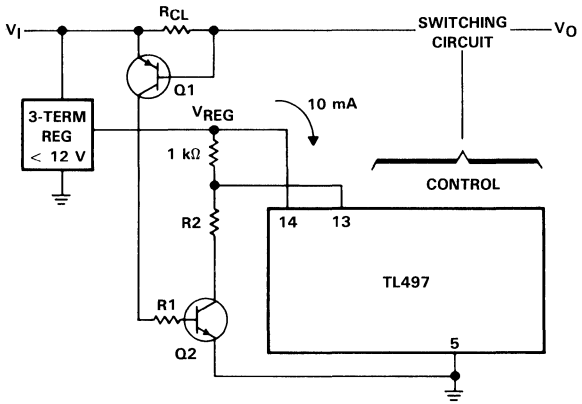
*Use external catch-diode, e.g., 1N4001, when building an inverting supply with the TL497A.

FIGURE 3. INVERTING APPLICATIONS

TYPICAL APPLICATION DATA



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

DESIGN EQUATIONS

$$R_{CL} = \frac{V_{BE(Q1)}}{I_{limit\ (PK)}}$$

$$R1 = \frac{V_I}{I_{B(Q2)}}$$

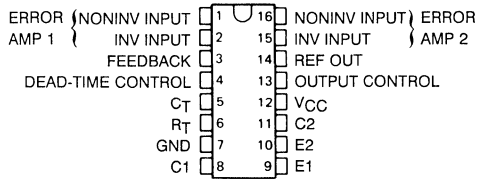
$$R2 = (V_{reg} - 1)\ 10\ k\Omega$$

FIGURE 4. EXTENDED INPUT VOLTAGE RANGE (V_I > 15 V)

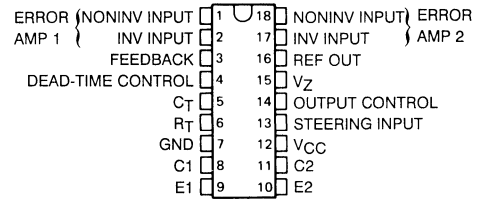
D2712, APRIL 1983—REVISED OCTOBER 1988

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture allows Easy Synchronization**
- **Under-Voltage Lockout for Low V_{CC} Conditions**
- **TL595 has On-Chip 39-V Zener and External Control of Output Steering**

TL594I, TL594C . . . D, J, OR N PACKAGE
(TOP VIEW)



TL595C . . . N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL594 and TL595 devices each incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to his application.

The TL594 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control comparator, pulse-steering control flip-flop, 5-V regulator with a precision of 1%, an under-voltage lockout control circuit, and output control circuitry.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common circuitry in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation with selection by

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT (TL595 ONLY)	
$V_I \le 0$	Open	Single-ended or parallel output
$V_I \ge V_{ref}$	Open	Normal push-pull operation
$V_I \ge V_{ref}$	$V_I < 0$	PWM Output at Q1
$V_I \ge V_{ref}$	$V_I \ge V_{ref}$	PWM Output at Q2

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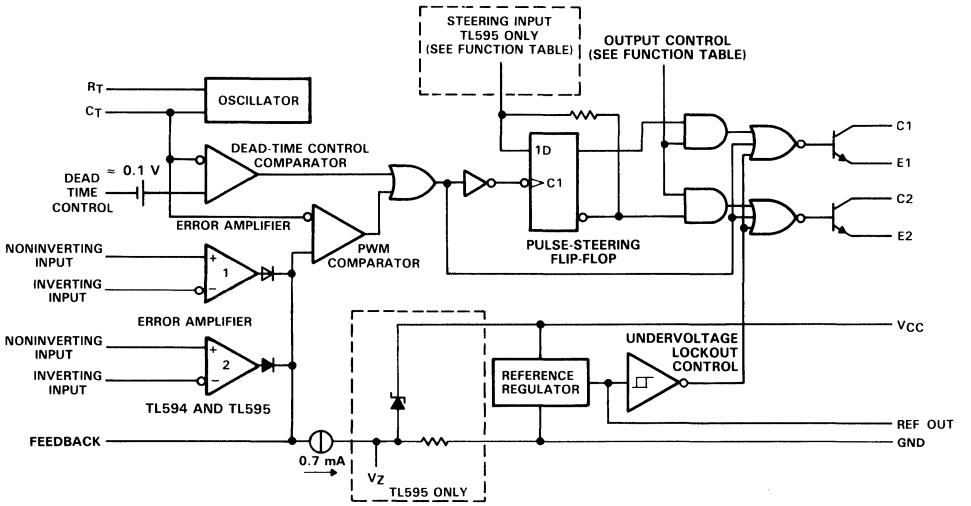
description (continued)

means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

The TL595 provides the identical functions found in the TL594. In addition, the TL595 also contains an on-chip 39-V zener diode for high-voltage applications where V_{CC} is greater than 40 V, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

The TL594I is characterized for operation from −25°C to 85°C. The TL594C and TL595C are characterized for operation from 0°C to 70°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL594I	TL594C TL595C	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	V
Amplifier input voltages	V_{CC}+0.3	V_{CC}+0.3	V
Collector output voltage	41	41	V
Collector output current	250	250	mA
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260	260	°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW
J	1000 mW	8.2 mW/°C	28°C	656 mW	533 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

	TL594I		TL594C TL595C		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	V_{CC}−2	−0.3	V_{CC}−2	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10 000	0.47	10 000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	kHz
Operating free-air temperature, T_A	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Output voltage (V_{ref})	I_O = 1 mA,	T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	25	mV
Output regulation	I_O = 1 to 10 mA,	T_A = 25°C		14	35	mV
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2%	1%	
Short-circuit output current§	V_{ref} = 0		10	35	50	mA

oscillator section (see Figure 2)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Frequency				10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant			10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V,	T_A = 25°C		0.1%		
Frequency change with temperature	ΔT_A = MIN to MAX				12%	

amplifier sections (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Input offset voltage, error amplifier	Feedback pin at 2.5 V			2	10	mV
Input offset current	Feedback control at 2.5 V			25	250	nA
Input bias current	Feedback control at 2.5 V			0.2	1	µA
Common-mode input voltage range, error amplifier	V_{CC} = 7 V to 40 V		−0.3 to V_{CC}−2			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V, R_L = 2 kΩ	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ		800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V,	T_A = 25°C	65	80		dB
Output sink current (pin 3)	V_{ID} = −15 mV to −5 V,	Feedback control at 0.5 V	0.3	0.7		mA
Output cource current (pin 3)	V_{ID} = 15 mV to 5 V,	Feedback at 3.5 V	−2			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N - 1}}$$

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	Dead-time control at 0 V	45%			
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

output section

		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
		V_C = 15 V, V_{CC} = 1 to 3 V, Dead-time and output control pins at 0 V	V_E = 0 V,		4	200	
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter-follower	V_C = 15 V,	I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}				3.5	mA

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.5 V	0.3	0.7		mA

under-voltage lockout section (see Figure 2)

PARAMETER	TEST CONDITION‡	MIN	MAX	UNIT
Threshold voltage	T_A = 25°C		6	V
	ΔT_A = MIN to MAX	3.5	6.9	
Hysteresis§		100		mV

total device (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	Dead-time Control at 2 V, See Figure 2			12.4		mA

† All typical values except for parameter changes with temperature are at T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration,		100	200	ns
Output voltage fall time	See Figure 3		30	100	
Output voltage rise time	Emitter-follower configuration,		200	400	ns
Output voltage fall time	See Figure 4		45	100	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

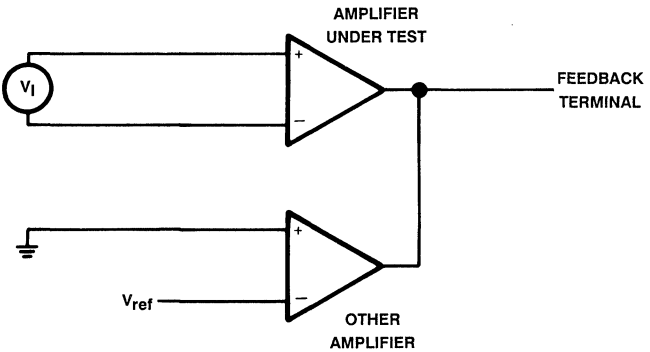

FIGURE 1. AMPLIFIER CHARACTERISTICS

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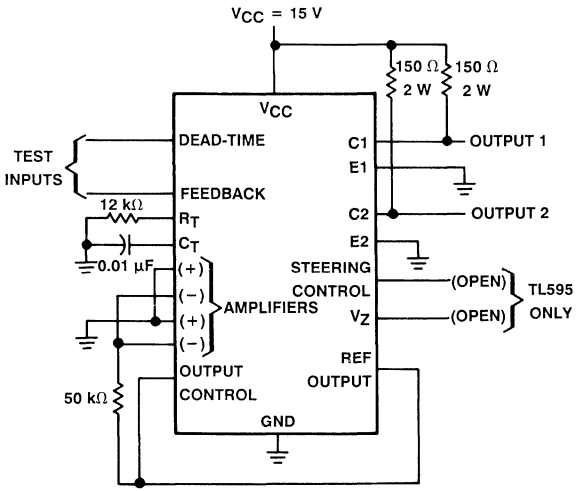
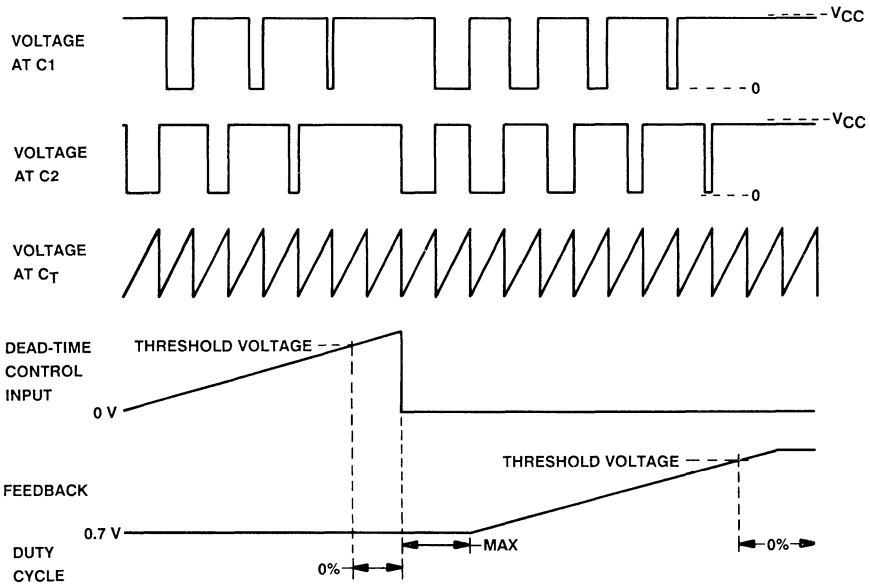
PARAMETER MEASUREMENT INFORMATION



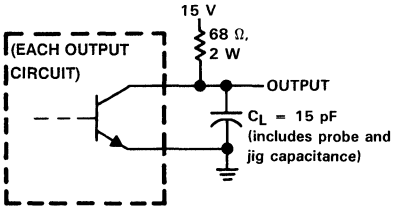
TEST CIRCUIT



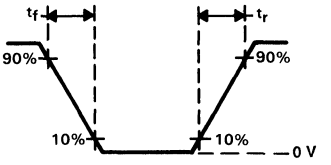
VOLTAGE WAVEFORMS

FIGURE 2. OPERATIONAL TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

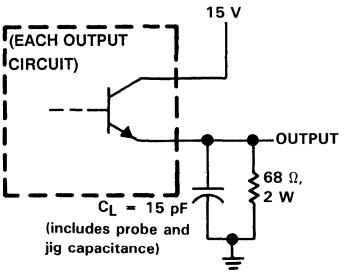


TEST CIRCUIT

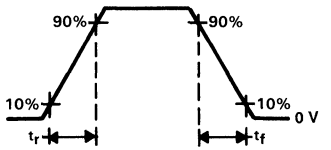


OUTPUT VOLTAGE WAVEFORM

FIGURE 3. COMMON-EMITTER CONFIGURATION



TEST CIRCUIT



OUTPUT VOLTAGE WAVEFORM

FIGURE 4. EMITTER-FOLLOWER CONFIGURATION

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY and FREQUENCY VARIATION† vs TIMING RESISTANCE

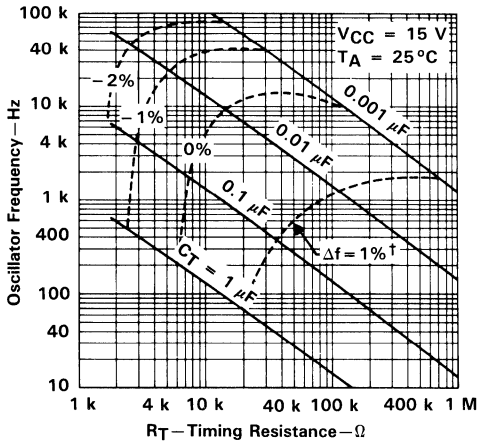


FIGURE 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

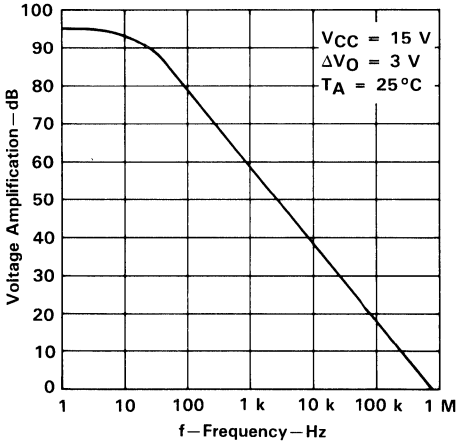


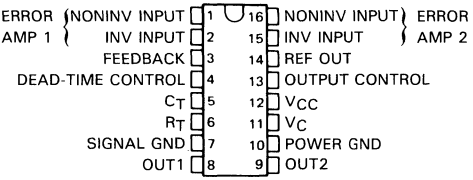
FIGURE 6

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D3026, FEBRUARY 1988—REVISED OCTOBER 1988

- Complete PWM Power Control Function
- Totem-Pole Outputs for 200-mA Sink or Source Current
- Output Control Selects Parallel or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance
- On-Board Output Current-Limiting Protection
- Under-Voltage Lockout for Low V_{CC} Conditions
- Independent Power and Signal Grounds
- TL598Q Has Extended Temperature Range . . . −40°C to 125°C

D, J, OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUT	
OUTPUT CONTROL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

2 Data Sheets

description

The TL598 incorporates all the functions required in the construction of pulse-width-modulated controlled systems on a single monolithic chip. Designed primarily for power supply control, the TL598 provides the systems engineer with the flexibility to tailor the power supply control circuits to a specific application.

The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control comparator, a pulse-steering flip-flop, a 5-V precision reference, an under-voltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise and fall time performance for power FET control. The outputs are designed with the collectors sharing a common source supply and common power grounds and are independent of V_{CC} and signal ground.

The error amplifier has a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. Synchronous multiple supply operation may be achieved by connecting pin 6 to the reference output and providing a sawtooth input to pin 5.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation.

The TL598Q is characterized for operation from −40°C to 125°C. The TL598C is characterized for operation from 0°C to 70°C.

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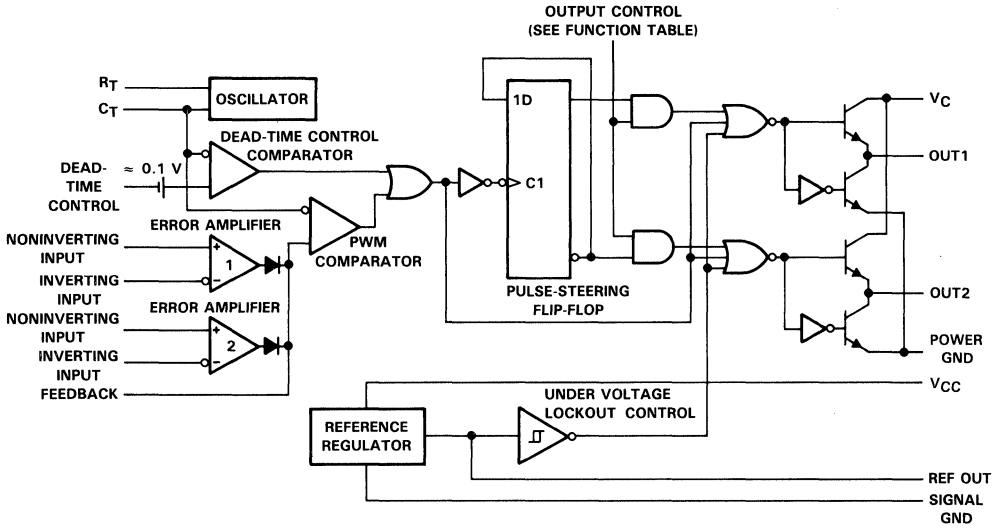
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 41 V
Amplifier input voltage, V_I . . . . . V_{CC} + 0.3 V
Collector voltage . . . . . 41 V
Output current (each output), sink or source, I_O . . . . . 250 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J: TL598Q . . . . . −40°C to 150°C
TL598C . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	190 mW
N	1200 mW	13 mW/°C	58°C	1040 mW	325 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		−0.3	V_{CC} − 2	V
Collector voltage			40	V
Output current (each output), sink or source, I_O			200	mA
Current into feedback terminal, I_{IL}			0.3	mA
Timing capacitor, C_T		0.00047	10	μF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Free-air temperature, T_A	TL598Q	−40	125	°C
	TL598C	0	70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted), see Note 2

reference section

PARAMETER	TEST CONDITIONS†		TL598Q			TL598C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (V_{ref})	I_O = 1 mA,	T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	22		2	25	mV
Output regulation	I_O = 1 to 10 mA,	T_A = 25°C		1	15		1	15	mV
		T_A = MIN to MAX			80				
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2	1		0.2	1	%
Short-circuit output current§	V_{ref} = 0		−10	−35		−10	−35		mA

oscillator section (see Figure 1) C_T = 0.001 μF, R_T = 12 kΩ

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		10		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1	1	%
Frequency change with temperature#	ΔT_A = MIN to MAX		2	5	%

error amplifier section

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Input offset voltage	Feedback pin at 2.5 V			2	10	mV
Input offset current	Feedback pin at 2.5 V			25	250	nA
Input bias current	Feedback pin at 2.5 V			0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V		−0.3 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (pin 3) = 3 V,	V_O (pin 3) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth				800		kHz
Common-mode rejection ratio	V_{CC} = 40 V,	ΔV_{IC} = 36.5 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	Feedback pin at 0.5 V		0.3	0.7		mA
Output source current (pin 3)	Feedback pin at 3.5 V		−2			mA
Phase margin at unity gain	Feedback pin = 0.5 V to 3.5 V, R_L = 2 kΩ			65°		
Supply voltage rejection ratio	Feedback pin at 2.5 V,	ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - X)^2}{N-1}}$
# Effects of temperature on external R_T and C_T are not taken into account.

NOTE 2: Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted), see Note 2

under-voltage lockout section

PARAMETER	TEST CONDITIONS†	TL598Q		TL598C		UNIT
		MIN	MAX	MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	4	6	V
	ΔT_A = MIN to MAX	3.8	6.9	3	6.9	
Hysteresis‡	T_A = 25°C	100		100		mV
	T_A = MIN to MAX	30		50		

output section

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Collector off-state current	V_{CE} = 40 V, V_{CC} = 40 V, Dead-time pin is connected to REF			2	100	μA
High-level output voltage	V_{CC} = 15 V,	I_O = −200 mA	12			V
	V_C = 15 V,	I_O = −20 mA	13			
Low-level output voltage	V_{CC} = 15 V,	I_O = 200 mA			2	V
	V_C = 15 V,	I_O = 20 mA			0.4	
Output control input current	V_I = V_{ref}				3.5	mA
	V_I = 0.4 V				100	μA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL598Q			TL598C			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−25		−2	−10	μA
Maximum duty cycle, each output	Dead-time control at 0 V	45			45			%
Input threshold voltage (pin 4)	Zero duty cycle		3	3.2		3	3.3	V
	Maximum duty cycle	0			0			

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.5 V	0.3	mA

total device (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open	V_{CC} = 15 V		15	21	mA
		V_{CC} = 40 V		17	23	
Average supply current	Dead-time control at 2 V			15		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
§All typical values except for parameter changes with temperature are at T_A = 25°C
NOTE 2: Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage rise time	C_L = 1500 pF,			100	150	ns
Output voltage fall time	V_C = 15 V,	V_{CC} = 15 V, See Figure 2		50	75	ns

PARAMETER MEASUREMENT INFORMATION

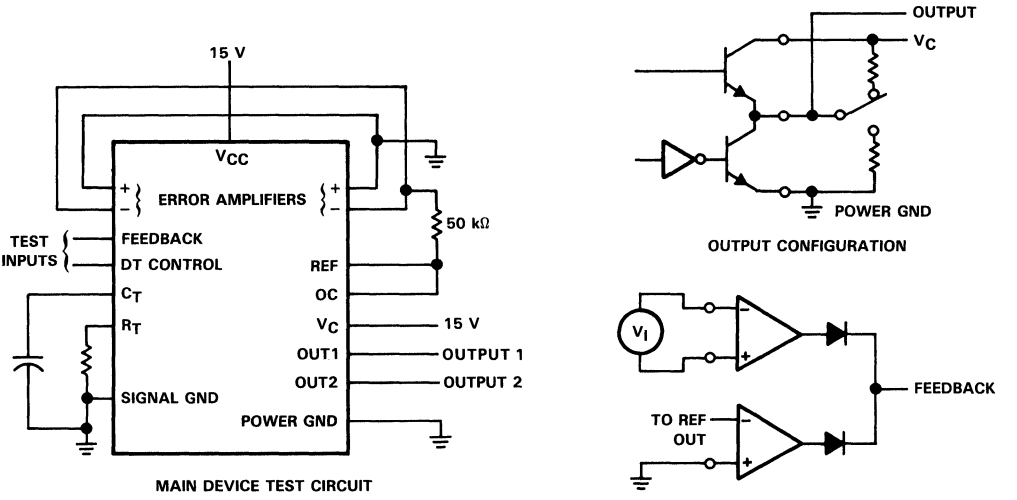

FIGURE 1. TEST CIRCUITS

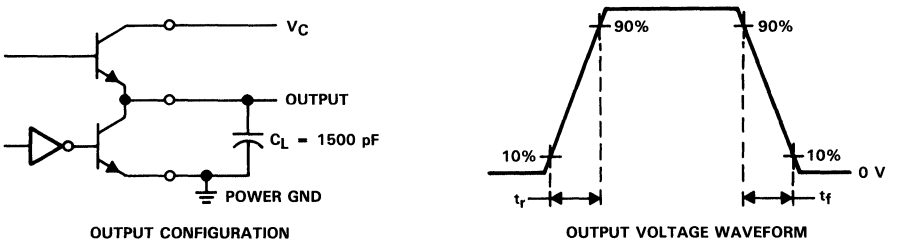

FIGURE 2. SWITCHING OUTPUT CONFIGURATION AND VOLTAGE WAVEFORM

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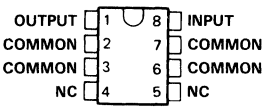
D3017, SEPTEMBER 1987—REVISED FEBRUARY 1988

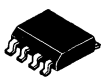
- Very Low Dropout Voltage, Less than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable On TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection to −50 V
- Internal Thermal Overload Protection
- Over-Voltage Protection
- Internal Over-Current Limiting Circuitry

terminal assignments

TL750L . . . D
SMALL OUTLINE PACKAGE

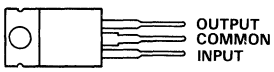
(TOP VIEW)





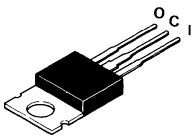
TL750L . . . KC
HEAT-SINK-MOUNTED PACKAGE

(TOP VIEW)



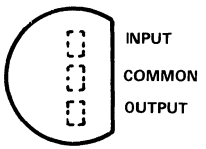
THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



TL750L . . . LP
SILECT™ PACKAGE

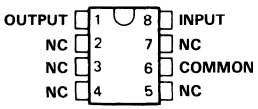
(TOP VIEW)



TO-226AA

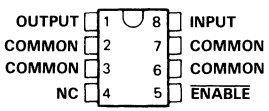
TL750L . . . P
DUAL-IN-LINE PACKAGE

(TOP VIEW)



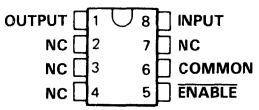
TL751L . . . D
SMALL OUTLINE PACKAGE

(TOP VIEW)



TL751L . . . P
DUAL-IN-LINE PACKAGE

(TOP VIEW)



NC—No internal connection
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description

The TL750L and TL751L series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750L and the TL751L incorporate over-voltage and current-limiting protection circuitry along with internal reverse-battery protection circuitry to protect both itself and the regulated system. Both series are fully protected against 60-volt load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes the TL750L and TL751L series ideal for standby power systems.

The TL750L series of fixed-output voltage regulators offer 5-volt, 8-volt, 10-volt, and 12-volt options. They are available in TO-226AA (formerly TO-92) (LP) packages, TO-220AB (KC) packages, 8-pin "small outline" plastic packages (D), and 8-pin plastic dual-in-line packages (P).

The TL751L series of fixed-output voltage regulators also offer 5-volt, 8-volt, 10-volt, and 12-volt options with the addition of an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. This series is offered in the 8-pin "small outline" plastic package and the 8-pin plastic dual-in-line package.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)

		TL750L	TL751L	UNIT
Continuous input voltage		26	26	V
Transient input voltage, T_A = 25°C (see Note 1)		60	60	V
Continuous reverse input voltage		−15	−15	V
Transient reverse input voltage: t ≤ 100 ms		−50	−50	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1):	D package	825	825	mW
	KC package	2000		
	LP package	775		
	P package	1000	1000	
Operating virtual junction temperature range		−40 to 150	−40 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds		260	260	°C

NOTES: 1. The transient input voltage rating applies for the waveform described in Figure 1.
2. For operation above 25°C free-air temperature, linearly derate the D package at the rate of 6.6 mW/°C, the KC package at 15.2 mW/°C, the LP package at 6.2 mW/°C, and the P package at 8 mW/°C.

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNITS
Input voltage, V_I	TL75_L05	6	26	V
	TL75_L08	9	26	
	TL75_L10	11	26	
	TL75_L12	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}	TL751L	2	15	V
Low-level $\overline{\text{ENABLE}}$ voltage, V_{IL}†	TL751L	−0.3	0.8	V
Output current, I_O	TL75_L	0	150	mA
Operating virtual junction temperature, T_J	TL75_L_C	0	125	°C
	TL75_L_Q	−40	125	

†The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL750L05 and TL751L05 electrical characteristics at 25 °C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V,	T_J = 25°C	4.80	5	5.2	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	4.75		5.25	
Input regulation	V_I = 9 V to 16 V			5	10	mV
	V_I = 6 V to 26 V			6	30	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz	60	65		dB
Output regulation	I_O = 5 mA to 150 mA			20	50	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 6 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

TL750L08 and TL751L08 electrical characteristics at 25 °C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V,	T_J = 25°C	7.8	8	8.2	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	7.6		8.4	
Input regulation	V_I = 10 V to 17 V			10	20	mV
	V_I = 9 V to 26 V			25	50	
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz	60	65		dB
Output regulation	I_O = 5 mA to 150 mA			40	80	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 9 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

TL750L10 and TL751L10 electrical characteristics at 25 °C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V,	T_J = 25°C	9.75	10	10.25	V
	I_O = 0 to 150 mA	T_J = T_J min to 125°C	9.50		10.50	
Input regulation	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V,	f = 120 Hz	60	65		dB
Output regulation	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V,	I_O = 10 mA, T_J = T_J min 125°C		1	2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 ohm, across the output.

TL750L12 and TL751L12 electrical characteristics at 25 °C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.7	12	12.3	V
		T_J = T_J min to 125°C	11.4		12.6	
Input regulation	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V,	I_O = 10 mA, T_J = T_J min to 125°C		1	2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 ohm, across the output.

ABSOLUTE MAXIMUM RATINGS

TRANSIENT INPUT VOLTAGE
vs
TIME

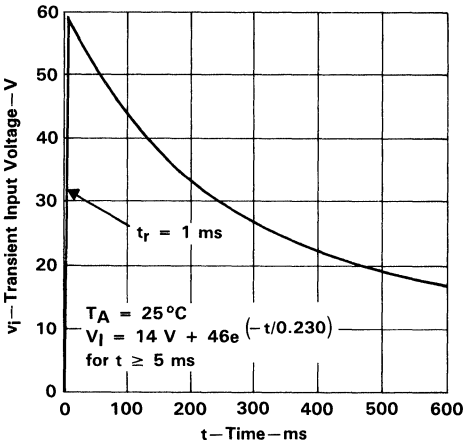


FIGURE 1

D3017, JANUARY 1988—REVISED OCTOBER 1988

- **Very Low Dropout Voltage, Less than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **60-V Load-Dump Protection**
- **Over-Voltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Over-Current Limiting Circuitry**

description

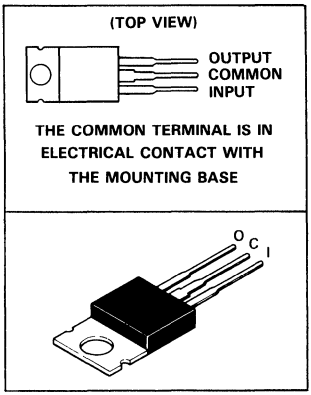
The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M incorporate on-board over-voltage and current-limit protection circuitry to protect both themselves and the regulated system. Both series are fully protected against 60-V load-dump and reverse battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options available in 3-lead KC (TO-220AB) plastic packages.

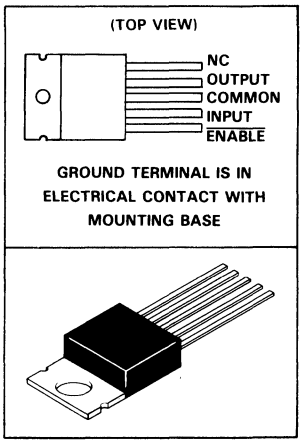
The TL751M series of fixed-output voltage regulators also offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input gives the designer complete control over power-up, allowing for sequential power-up or emergency shutdown. When taken high, the enable input places the regulator output in a high-impedance state. It is completely TTL- and CMOS-compatible. The TL751M series is offered in 5-lead KC plastic packages.

The TL750M and TL751M series are characterized for operation from −40°C to 125°C free-air temperature.

3-LEAD KC (TO-220AB) PACKAGE



5-LEAD KC PACKAGE



2 Data Sheets

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage . . . . . 26 V
Transient input voltage (see Figure 1) . . . . . 60 V
Continuous reverse input voltage . . . . . −15 V
Transient reverse input voltage: t = 100 ms . . . . . −50 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 20 W
Operating free-air, case, or virtual junction temperature . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

Note 1: For operation above 25°C free-air temperature, refer to Figures 2 and 3. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions over recommended operating free-air temperature range (unless otherwise noted)

	DEVICE	MIN	MAX	UNITS
Input voltage range, V_I	TL75_M05	6	26	V
	TL75_M08	9	26	
	TL75_M10	11	26	
	TL75_M12	13	26	
High-level ENABLE input voltage, V_{IH}	TL751M_	2	15	V
Low-level ENABLE input voltage, V_{IL} (see Note 2)	TL751M_	−0.3	0.8	
Output current range, I_O	TL75_M		750	mA
Operating virtual junction temperature range, T_J	TL75_M_C	0	125	°C
	TL75_M_Q	−40	125	

Note 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL750M05 and TL751M05 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M05 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	4.95	5	5.05	V
		T_A = T_J min to 125°C	4.9		5.1	
Input regulation	V_I = 9 V to 16 V, I_O = 250 mA			10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA			12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz			55		dB
Output regulation	I_O = 5 mA to 750 mA			20	50	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	

NOTE 3: Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL750M08 and TL751M08 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M08 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	7.92	8	8.08	V
		T_A = T_J min to 125°C	7.84		8.16	
Input regulation	V_I = 10 V to 17 V, I_O = 250 mA			12		mV
	V_I = 9 V to 26 V, I_O = 250 mA			15		
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz			55		dB
Output regulation	I_O = 5 mA to 750 mA			24		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	

TL750M10 and TL751M10 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M10 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	9.9	10	10.1	V
		T_A = T_J min to 125°C	9.8		10.2	
Input regulation	V_I = 12 V to 18 V, I_O = 250 mA			15		mV
	V_I = 11 V to 26 V, I_O = 250 mA			20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55	60		dB
Output regulation	I_O = 5 mA to 750 mA			30		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	

TL750M12 and TL751M12 electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12 (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 3)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 750 mA	T_A = 25°C	11.88	12	12.12	V
		T_A = T_J min to 125°C	11.76		12.24	
Input regulation	V_I = 14 V to 19 V, I_O = 250 mA			15		mV
	V_I = 13 V to 26 V, I_O = 250 mA			20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55	60		dB
Output regulation	I_O = 5 mA to 750 mA			30		mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	

NOTE 3: Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL751Mxx electrical characteristics at 25°C free-air temperature, V_I = 14 V, I_O = 300 mA

PARAMETER	MIN	TYP	MAX	UNIT
Response time, $\overline{\text{ENABLE}}$ to output		50		μs

MAXIMUM RATINGS

TRANSIENT INPUT VOLTAGE
vs
TIME

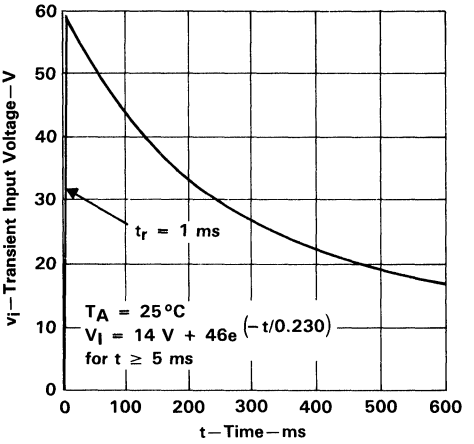


FIGURE 1

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

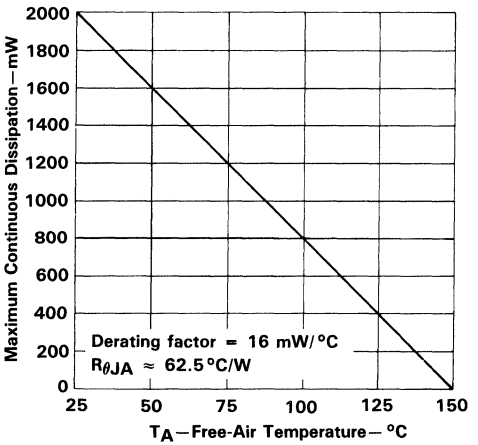


FIGURE 2

CASE TEMPERATURE
DISSIPATION DERATING CURVE

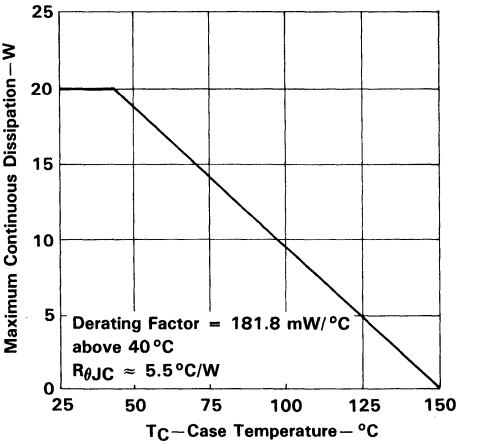
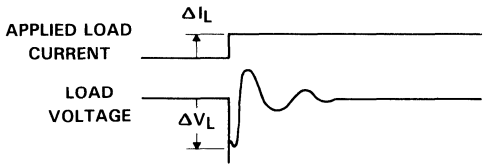


FIGURE 3

TRANSIENT RESPONSE



EQUIVALENT SERIES RESISTANCE OF OUTPUT CAPACITOR
vs
LOAD CURRENT RANGE

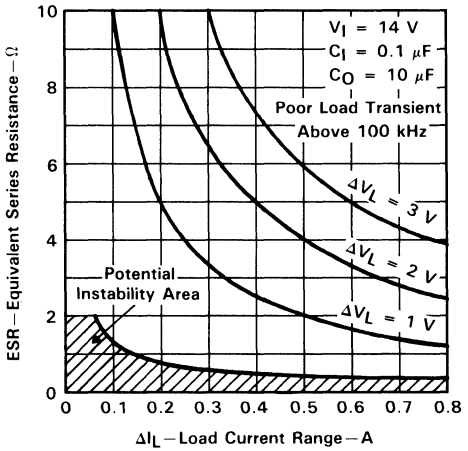


FIGURE 4

2 Data Sheets

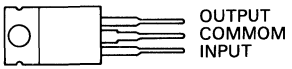
D2643, APRIL 1981 – REVISED AUGUST 1988

- ±1% Output Tolerance at 25°C
- ±2% Output Tolerance Over Full Operating Range
- Thermal Shutdown
- Internal Short-Circuit Current Limiting
- Pinout Identical to uA7800 Series
- Improved Version of uA7800 Series

NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	TL780-05C
12 V	TL780-12C
15 V	TL780-15C

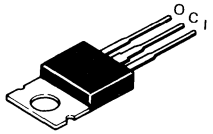
KC PACKAGE

(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

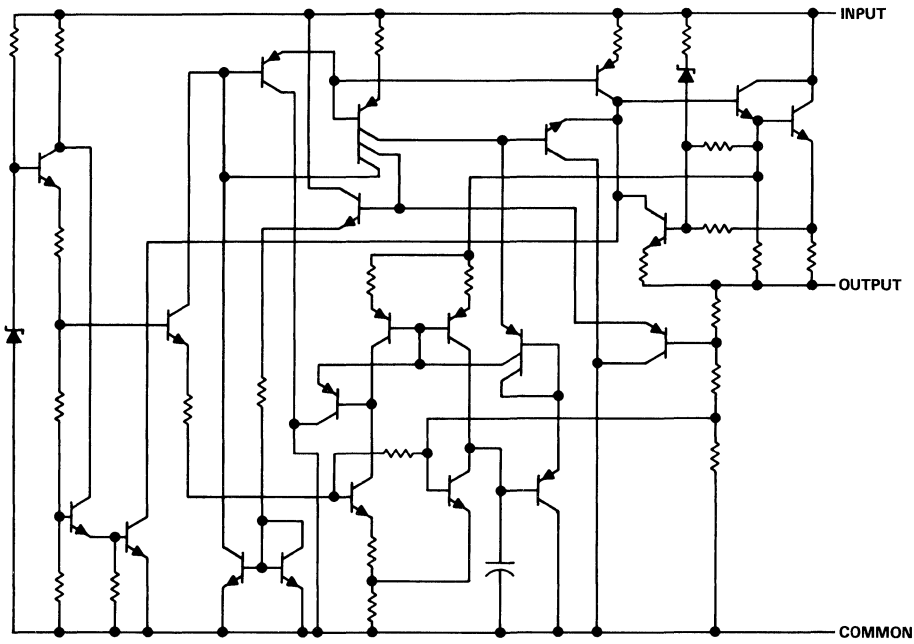
TO-220AB



description

Each fixed-voltage precision regulator in this series is capable of supplying 1.5 amperes of load current. A unique temperature-compensation technique coupled with an internally trimmed bandgap reference has resulted in improved accuracy when compared to other three-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current limiting and thermal shutdown features make the devices essentially immune to overload.

schematic



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absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage . . . . . 35 V
Continuous total dissipation at 25°C free-air temperature (see Note 1) . . . . . 2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 15 W
Operating free-air, case, or virtual junction temperature range . . . . . 0 to 150°C
Storage temperature range . . . . . −65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

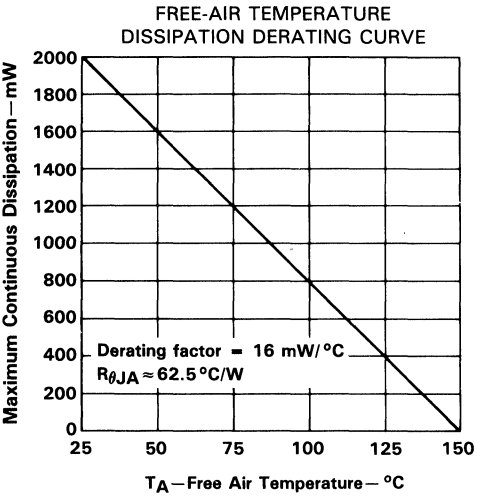


FIGURE 1

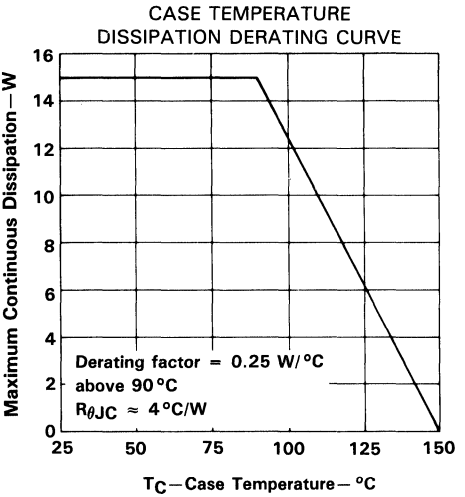


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL780-05C	7	25	V
	TL780-12C	14.5	30	
	TL780-15C	17.5	30	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

TL780-05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1A, P ≤ 15 W,	25°C	4.95	5	5.05	V
	V_I = 7 V to 20 V	0°C to 125°C	4.9		5.1	
Input regulation	V_I = 7 V to 25 V	25°C		0.5	5	mV
	V_I = 8 V to 12 V			0.5	5	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	70	85		db
Output regulation	I_O = 5 mA to 1.5 A	25°C		4	25	mV
	I_O = 250 mA to 750 mA			1.5	15	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C		0.7	1.3	mA
	I_O = 5 mA to 1 A			0.003	0.5	
Short-circuit output current	V_I = 35 V	25°C		750		mA
Peak output current		25°C		2.2		A

TL780-12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,	25°C	11.88	12	12.12	V
	V_I = 14.5 V to 27 V	0°C to 125°C	11.76		12.24	
Input regulation	V_I = 14.5 V to 30 V	25°C		1.2	12	mV
	V_I = 16 V to 22 V			1.2	12	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	65	80		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		6.5	60	mV
	I_O 250 mA to 750 mA			2.5	36	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		180		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current	V_I = 35 V	25°C		350		mA
Peak output current		25°C		2.2		A

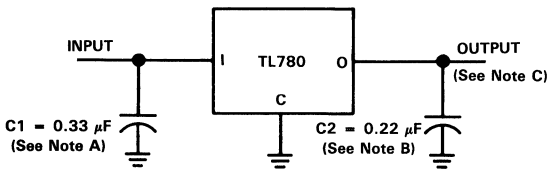
†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with 0.33 μF capacitor across the input and a 0.22 μF capacitor across the output.

TL780-15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,	25°C	14.85	15	15.15	V
	V_I = 17.5 V to 30 V	0°C to 125°C	14.7		15.3	
Input regulation	V_I = 17.5 V to 30 V	25°C		1.5	15	mV
	V_I = 20 V to 26 V			1.5	15	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	60	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		7	75	mV
	I_O = 250 mA to 750 mA			2.5	45	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		225		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.02	0.5	
Short-circuit output current	V_I = 35 V	25°C		230		mA
Peak output current		25°C		2.2		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33 μF capacitor across the input and a 0.22 μF capacitor across the output.

TYPICAL APPLICATION DATA



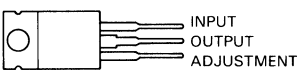
Notes: A. C1 required if regulator is far from power supply filter.
B. C2 not required for stability, however transient response is improved.
C. Permanent damage can occur if output is pulled below ground.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2659, SEPTEMBER 1981 – REVISED SEPTEMBER 1988

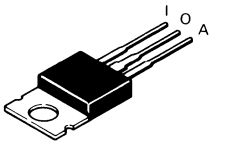
- **Output Adjustable from 1.25 V to 125 V**
- **700-mA Output Current**
- **Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection**
- **0.001 %/V Typical Input Regulation**
- **0.15% Typical Output Regulation**
- **76-dB Typical Ripple Rejection**
- **Standard TO-220AB Package**

KC PACKAGE
(TOP VIEW)



THE OUTPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



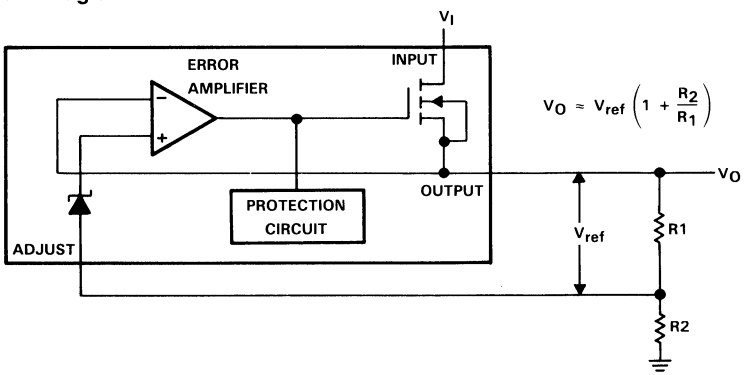
description

The TL783C is an adjustable three-terminal positive-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications . . . superior to those of most bipolar regulators . . . are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783C combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually assoicated with bipolar outputs, the TL783C maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if the adjustment pin is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, will improve transient response and protection from instantaneous output short-circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

functional block diagram



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ . . . . . 125 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 20 W
Operating free-air, case, or virtual junction temperature range . . . . . 0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

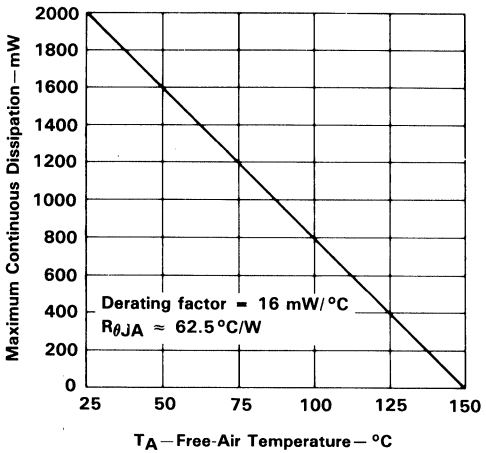

FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVES

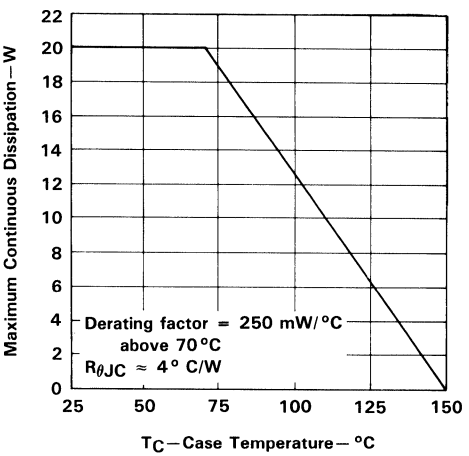

FIGURE 2

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 0°C$ to $125°C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Input regulation‡	$V_I - V_O = 20$ V to 125 V,	P ≤ rated dissipation	$T_J = 25°C$		0.001	0.01	%/V
			$T_J = 0°C$ to $125°C$		0.004	0.02	
Ripple rejection	$\Delta V_{I(p-p)} = 10$ V,	$V_O = 10$ V,	f = 120 Hz	66	76		dB
Output regulation	$I_O = 15$ mA to 700 mA,	$T_J = 25°C$	$V_O \leq 5$ V		7.5	25	mV
			$V_O \geq 5$ V		0.15	0.5	%
	$I_O = 15$ mA to 700 mA,	P ≤ rated dissipation	$V_O \leq 5$ V		20	70	mV
			$V_O \geq 5$ V		0.3	1.5	%
Output voltage change with temperature					0.4		%
Output voltage long-term drift	1000 h at $T_J = 125°C$, See Note 2	$V_I - V_O = 125$ V,			0.2		%
Output noise voltage	f = 10 Hz to 10 kHz,	$T_J = 25°C$			0.003		%
Minimum output current to maintain regulation	$V_I - V_O = 125$ V					15	mA
Peak output current	$V_I - V_O = 25$ V,	t = 1 ms			1100		mA
	$V_I - V_O = 15$ V,	t = 30 ms			715		
	$V_I - V_O = 25$ V,	t = 30 ms		700	900		
	$V_I - V_O = 125$ V,	t = 30 ms		100	250		
Adjustment-terminal current					83	110	μA
Change in adjustment-terminal current	$V_I - V_O = 15$ V to 125 V,	$I_O = 15$ mA to 700 mA,	P ≤ rated dissipation		0.5	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = 10$ V to 125 V,	$I_O = 15$ mA to 700 mA,	P ≤ rated dissipation	1.2	1.27	1.3	V

† Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

NOTE 2: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

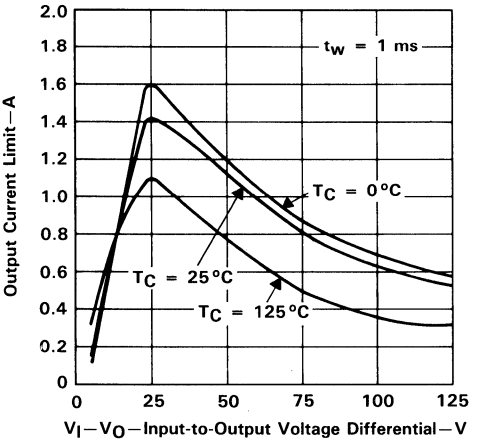

FIGURE 3

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

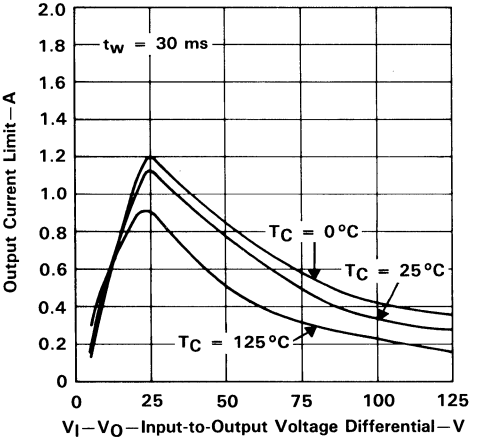

FIGURE 4

OUTPUT CURRENT LIMIT
vs
TIME

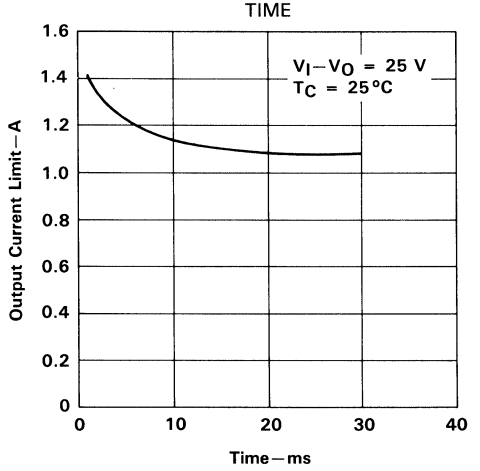

FIGURE 5

RIPPLE REJECTION
vs
OUTPUT VOLTAGE

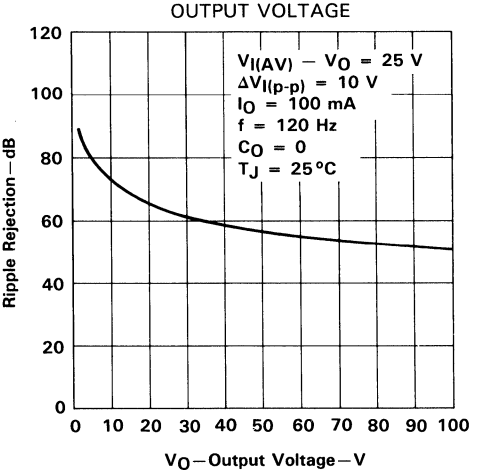

FIGURE 6

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
OUTPUT CURRENT

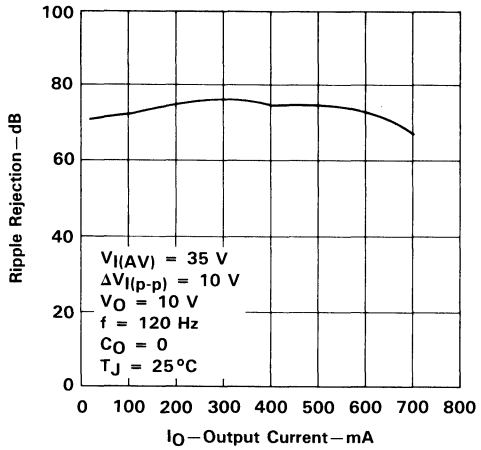

FIGURE 7

RIPPLE REJECTION
vs
FREQUENCY

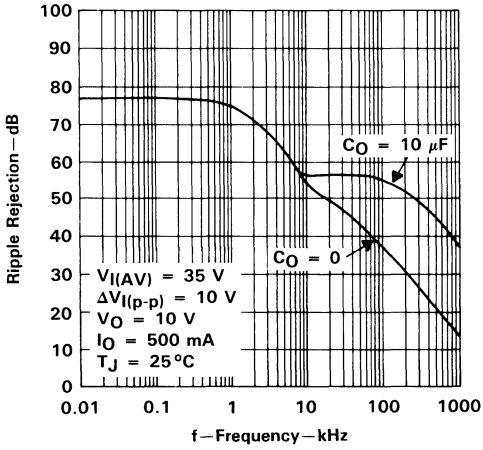

FIGURE 8

OUTPUT IMPEDANCE
vs
FREQUENCY

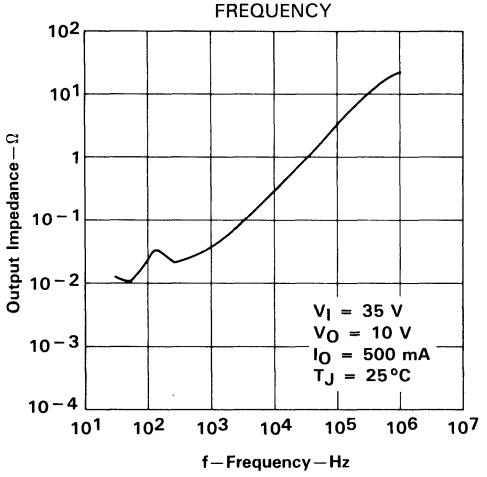

FIGURE 9

REFERENCE VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

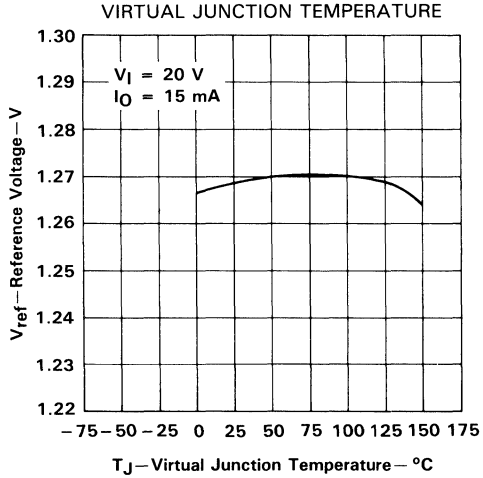

FIGURE 10

TYPICAL CHARACTERISTICS

ADJUSTMENT-TERMINAL CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

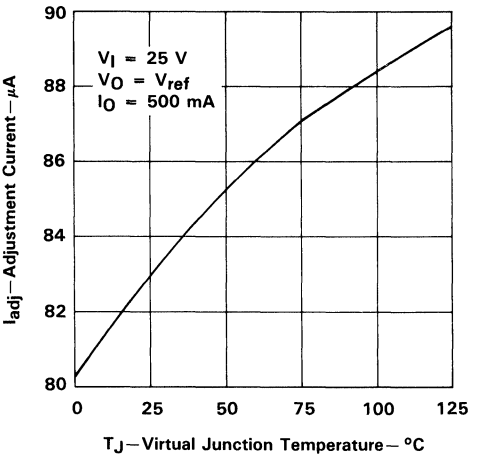

FIGURE 11

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

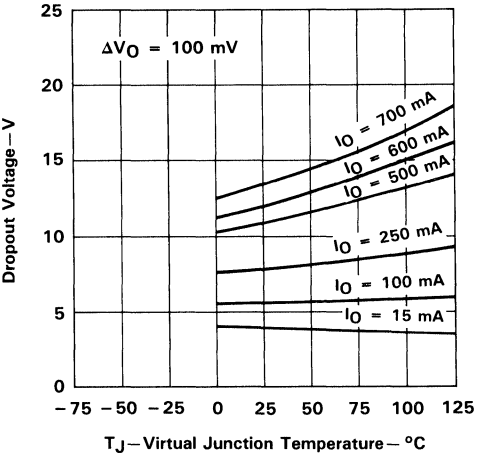

FIGURE 12

LOAD REGULATION
vs
VIRTUAL JUNCTION TEMPERATURE

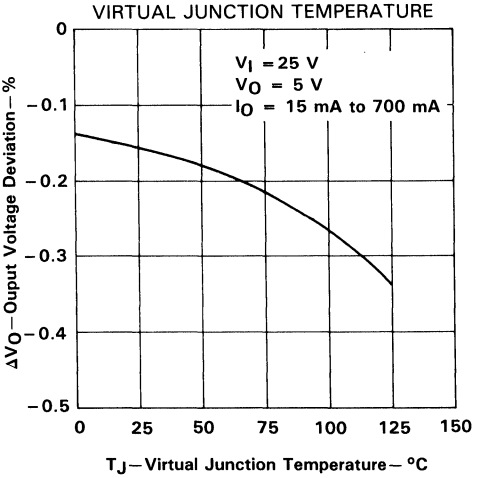

FIGURE 13

MINIMUM OUTPUT CURRENT
TO MAINTAIN REGULATION
vs
INPUT VOLTAGE

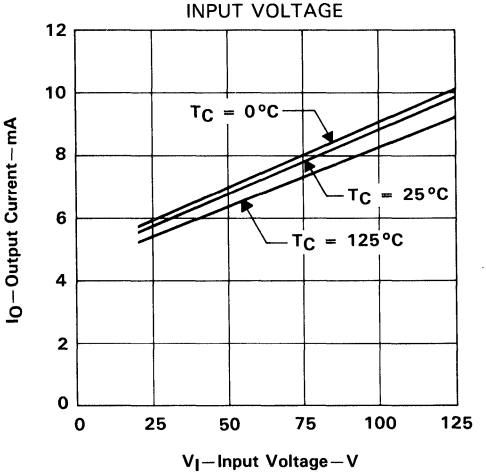

FIGURE 14

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

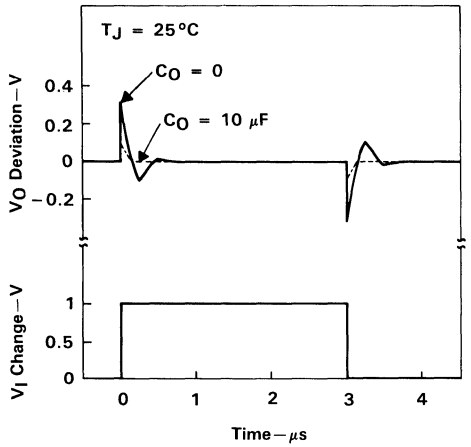


FIGURE 15

LOAD TRANSIENT RESPONSE

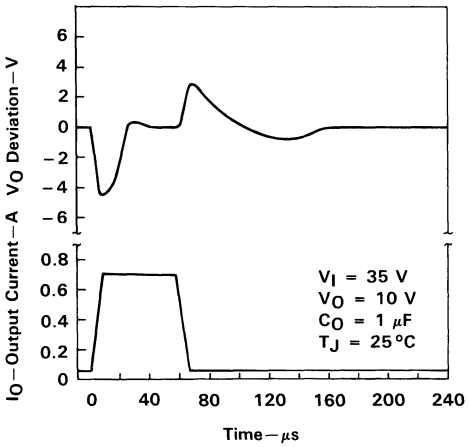


FIGURE 16

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) is used to generate 1.25 V nominal (V_{ref}) between the output and adjustment terminals. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref}\,(1+R2/R1) + I_{adj}\,(R2)$$

or

$$V_O \sim V_{ref}\,(1+R2/R1).$$

The TL783C was designed to minimize I_{adj} and maintain consistency over line and load variations, thereby minimizing the I_{adj} (R2) error term.

To maintain I_{adj} at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω will provide a minimum load current of 15 mA. Larger values may be used if the input-to-output differential voltage is less than 125 V (see minimum operating current curve) or if the load will sink some portion of the minimum current.

bypass capacitors

The TL783C regulator is stable without bypass capacitors; however, any regulator will become unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-μF tantalum or electrolytic capacitor is usually sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783C because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage drop-out may occur under large load transient conditions. Addition of an output bypass capacitor will greatly enhance load transient response as well as prevent drop-out. For most applications, it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_O\ (\mu F) = 15/V_O$$

Larger values will provide proportionally better transient response characteristics.

protection circuitry

The TL783C regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits are meant to protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783C will protect the device up to maximum rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, if rise times in excess of 10 V/ns are applied to the input, a parasitic n-p-n transistor in parallel with the DMOS output can be turned on causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as a tantalum or electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater will usually provide adequate damping to suppress ringing. Normally, no problems will occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, if an instantaneous short circuit is applied to the outputs, both ringing and excessive fall times can result. A tantalum or electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I. A protective diode (see Figure 17) is required only for capacitance values greater than

$$C_O\ (\mu F) = 3 \times 10^4/(V_O)^2.$$

Care should always be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

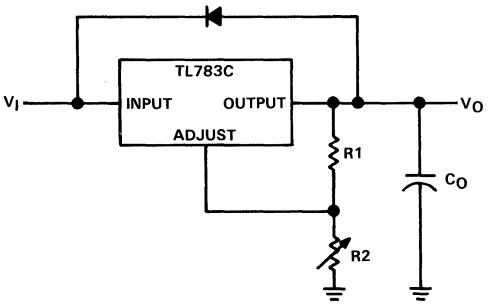


FIGURE 17. REGULATOR WITH PROTECTIVE DIODE

load regulation

The current set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R1 and R2 to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

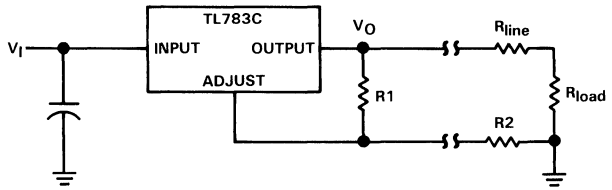
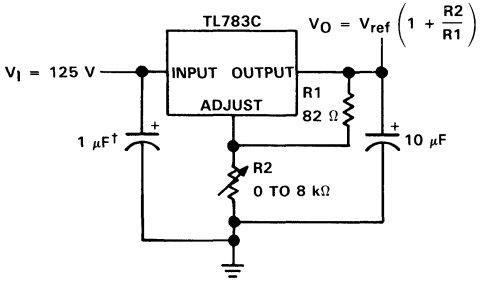


FIGURE 18. REGULATOR WITH CURRENT-SET RESISTOR

TYPICAL APPLICATION DATA



†NEEDED IF DEVICE IS MORE THAN 4 INCHES FROM FILTER CAPACITOR

FIGURE 19. 1.25-V TO 115-V ADJUSTABLE REGULATOR

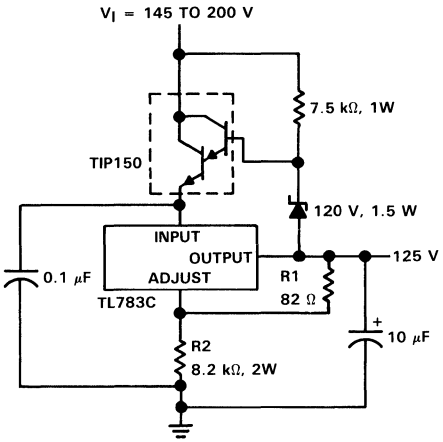


FIGURE 20. 125-V SHORT-CIRCUIT-PROTECTED OFF-LINE REGULATOR

TYPICAL APPLICATION DATA

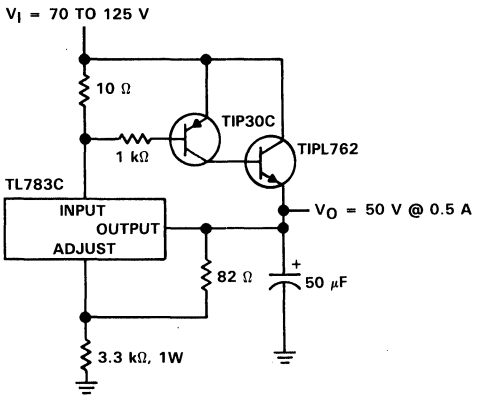


FIGURE 21. 50-V
REGULATOR WITH CURRENT BOOST

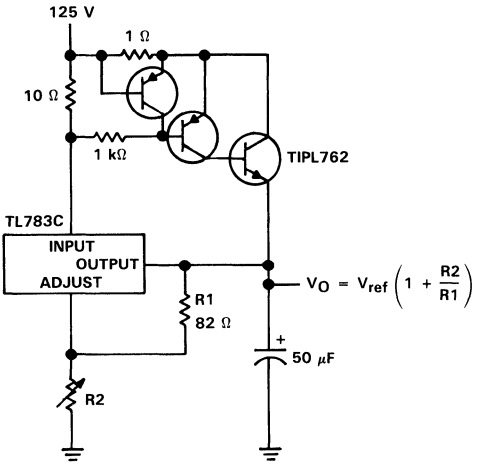


FIGURE 22. ADJUSTABLE
REGULATOR WITH CURRENT BOOST
AND CURRENT LIMIT

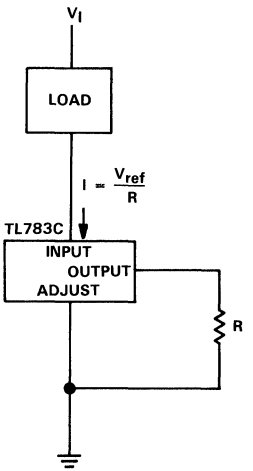


FIGURE 23. CURRENT-SINKING REGULATOR

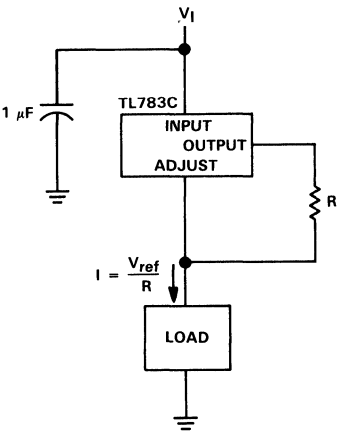


FIGURE 24. CURRENT SOURCING REGULATOR

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TYPICAL APPLICATION DATA

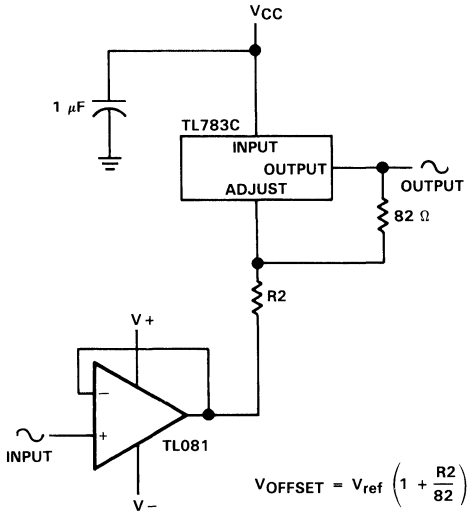


FIGURE 25. HIGH-VOLTAGE UNITY-GAIN OFFSET AMPLIFIER

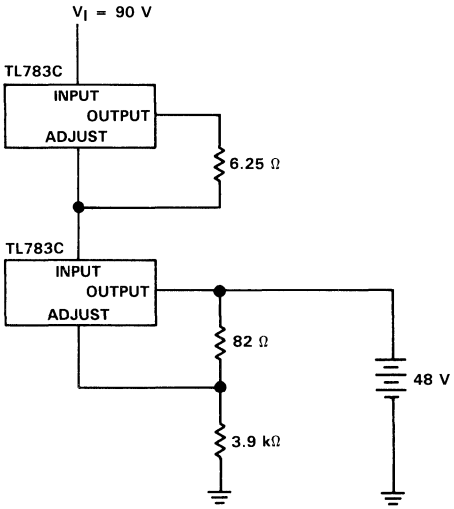
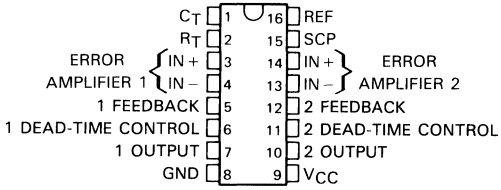


FIGURE 26. 48-V, 200-mA FLOAT CHARGER

D2730, FEBRUARY 1983 – REVISED OCTOBER 1988

- Complete PWM Power Control Circuitry
- Completely Synchronized Operation
- Internal Undervoltage Lockout Protection
- Wide Supply Voltage Range
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 500 kHz Max
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 2.5-V Reference Supply

D OR N PACKAGE
(TOP VIEW)



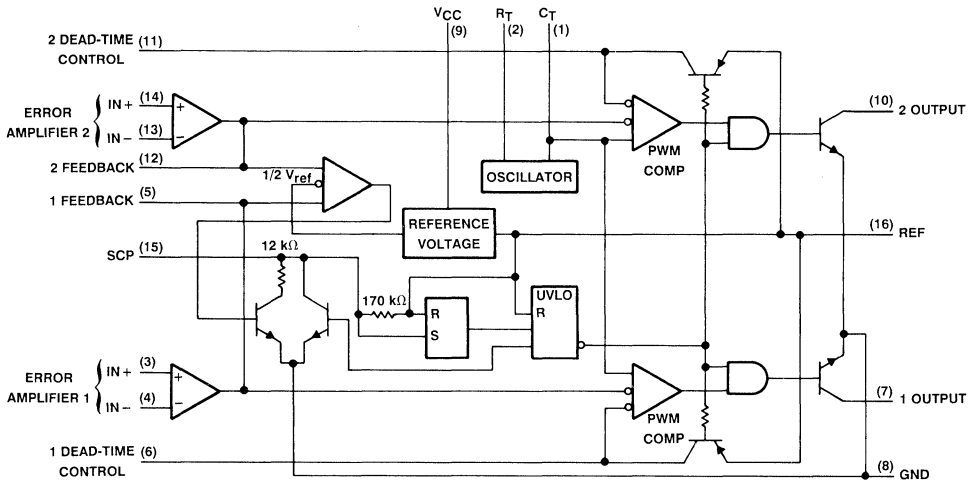
description

The TL1451AC incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation control circuits. Designed primarily for power supply control, the TL1451AC contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control comparator has no offset unless externally altered and may be used to provide 0% to 100% dead time. The on-chip oscillator may be operated by terminating R_T (pin 2) and C_T (pin 1). During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from −20°C to 85°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 41 V
Amplifier input voltage . . . . . 20 V
Collector output voltage . . . . . 51 V
Collector output current . . . . . 21 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	4.0 mW/°C	320 mW	260 mW
N	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	40	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		50	V
Collector output current		20	mA
Current into feedback terminal		45	μA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (pin 16)	I_O = 1 mA	2.4	2.5	2.6	V
Output voltage change with temperature	T_A = −20°C to 25°C		−0.1%	±1%	
	T_A = 25°C to 85°C		−0.2%	±1%	
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output regulation	I_O = 0.1 mA to 1 mA		1	7.5	mV
Short-circuit output current	V_O = 0	3	10	30	mV

undervoltage lockout section

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Upper threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.72		V
Lower threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C		2.6		V
Hysteresis (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	80	120		mV
Reset threshold voltage (pin 9)	I_{Oref} = 0.1 mA,	T_A = 25°C	1.5	1.8		V

† All typical values are at T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

protection control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 15)	T_A = 25°C	0.65	0.7	0.75	V
Standby voltage (pin 15)	No pullup	140	185	230	mV
Latched input voltage (pin 15)	No pullup		60	120	mV
Input (source) current	V_I = 0.7 V, T_A = 25°C	−10	−15	−20	µA
Comparator threshold voltage (pins 5 and 12)			1.18		V

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	C_T = 330 pF, R_T = 10 kΩ		200		kHz
Standard deviation of frequency	C_T = 330 pF, R_T = 10 kΩ		10%		
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1%		
Frequency change with temperature	T_A = −20°C to 25°C		−0.4%	±2%	
	T_A = 25°C to 85°C		−0.2%	±2%	

dead-time control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pins 6 and 11)				1	µA
Latch mode (source) current (pins 6 and 11)	T_A = 25°C	−80	−145		µA
Latched input voltage (pins 6 and 11)	I_O = 40 µA	2.3			V
Input threshold voltage at f = 10 kHz (pins 6 and 11)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

error-amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pins 5 and 12) = 1.25 V			±6	mV
Input offset current	V_O (pins 5 and 12) = 1.25 V			±100	nA
Input bias current	V_O (pins 5 and 12) = 1.25 V		160	500	nA
Common-mode input voltage range	V_{CC} = 3.6 V to 40 V	1.05 to 1.45			V
Open-loop voltage amplification	R_F = 200 kΩ	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		V_{ref}−0.1			V
Negative output voltage swing				1	V
Output (sink) current (pins 5 and 12)	V_{ID} = −0.1 V, V_O = 1.25 V	0.5	1.6		mA
Output (source) current (pins 5 and 12)	V_{ID} = 0.1 V, V_O = 1.25 V	−45	−70		µA

† All typical values are at T_A = 25°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

output section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current	V_O = 50 V			10	µA
Output saturation voltage	I_O = 10 mA		1.2	2	V
Short-circuit output current	V_O = 6 V		90		mA

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage at f = 10 kHz (pins 5 and 12)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		
Input (sink) current (pins 5 and 12)	V_I = 1.25 V	0.5	1.6		mA
Input (source) current (pins 5 and 12)	V_I = 1.25 V	−45	−70		µA

total device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	R_T = 10 kΩ		1.7	2.4	mA

† All typical values are at T_A = 25°C.

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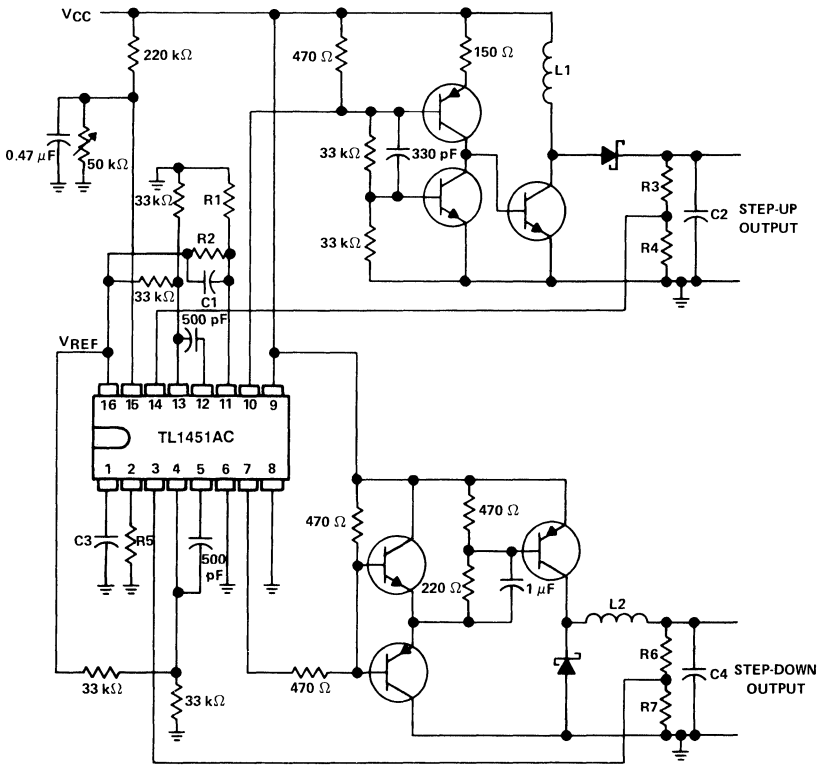
TYPICAL APPLICATION DATA

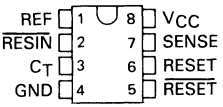


Values for R1 through R7, C1 through C4, and L1 and L2 depend upon inidividual application.

D2722, APRIL 1983—REVISED OCTOBER 1988

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply Voltage Range . . . 3 V to 18 V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Width**

D OR P PACKAGE
(TOP VIEW)



description

The TL7702A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. To ensure that the microcomputer system has reset, the TL7702A series initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external capacitor connected to the C_T input (pin 3).

$$t_d = 1.3 \times 10^4 \times C_T$$

Where: C_T is in farads (F) and t_d is in seconds(s)

During power-up, the outputs are undefined until the supply voltage V_{CC} reaches a minimum value of 3.6 V. During power-down, with the SENSE input below the threshold voltage, the outputs remain active until the supply voltage V_{CC} falls below a maximum of 2 V after which the outputs are undefined. See Timing Diagram. Suggested circuits to eliminate undefined states are shown in Figures 3 and 4.

In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 μF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7702AI series is characterized for operation from −25°C to 85°C; the TL7702AC series is characterized from 0°C to 70°C.

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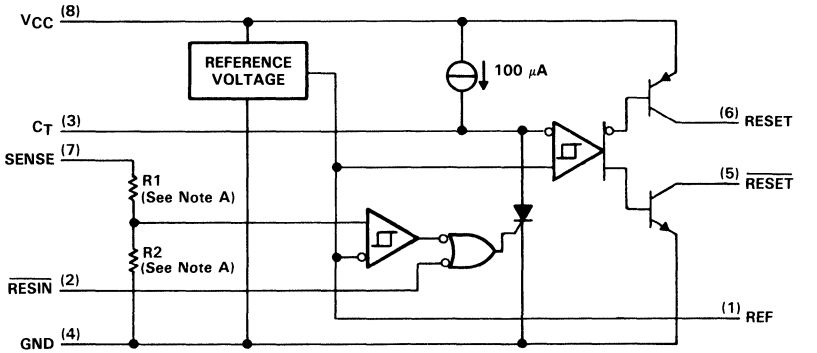
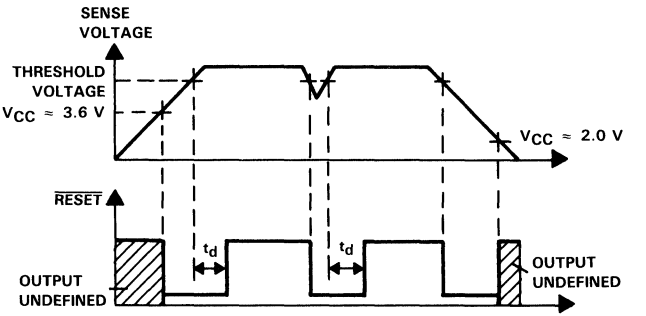
functional block diagram



NOTE A: TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range at $\overline{RESIN}$ . . . . . −0.3 V to 20 V
Input voltage at SENSE: TL7702A (see Note 2) . . . . . −0.3 V to 6 V
TL7705A . . . . . −0.3 V to 10 V
TL7709A . . . . . −0.3 V to 15 V
TL7712A . . . . . −0.3 V to 20 V
TL7715A . . . . . −0.3 V to 20 V
High-level output current at $\overline{RESET}$ . . . . . −30 mA
Low-level output current at $\overline{RESET}$ . . . . . 30 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL77_I . . . . . −25°C to 85°C
TL77_C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.6		18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2			V
Low-level input voltage at $\overline{RESIN}$, V_{IL}				0.6	V
Voltage at SENSE, V_I	TL7702A	0	See Note 2		V
	TL7705A	0		10	
	TL7709A	0		15	
	TL7712A	0		20	
	TL7715A	0		20	
High-level output current at RESET, I_{OH}				−16	mA
Low-level output current at $\overline{RESET}$, I_{OL}				16	mA
Operating free-air temperature range, T_A	TL77_I	−25		85	°C
	TL77_C	0		70	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} − 1 V or 6 V, whichever is less.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage at RESET		I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage at $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_{T-}	Negative-going threshold voltage at SENSE input	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis‡ at SENSE input	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current at $\overline{\text{RESIN}}$ input		V_I = 2.4 V to V_{CC}			20	μA
			V_I = 0.4 V			−100	
I_I	Input current at SENSE input	TL7702A	$V_{ref} < V_I < V_{CC}$ −1.5 V		0.5	2	μA
I_{OH}	High-level output current at $\overline{\text{RESET}}$		V_O = 18 V			50	μA
I_{OL}	Low-level output current at RESET		V_O = 0			−50	μA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

†All electrical characteristics are measured with 0.1-μF capacitors connected at pins 1, 3, and 8 to GND.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
$t_{wS(min)}$	Minimum pulse duration at SENSE input to switch outputs	V_{IH} = V_{T-} +200 mV, V_{IL} = V_{T-} −200 mV			2	μs
t_{pd}	Propagation delay time from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	V_{CC} = 5 V		1.5		μs
t_r	RESET	V_{CC} = 5 V, See Note 3			0.2	μs
	$\overline{\text{RESET}}$				3.5	
t_f	$\overline{\text{RESET}}$				0.2	μs
	RESET				3.5	

§All switching characteristics are measured with 0.1-μF capacitors connected at pins 1 and 8 to GND.
NOTE 3: The rise and fall times are measured with a 4.7-kΩ load resistor at $\overline{\text{RESET}}$ (pin 5) and RESET (pin 6).

PARAMETER MEASUREMENT INFORMATION

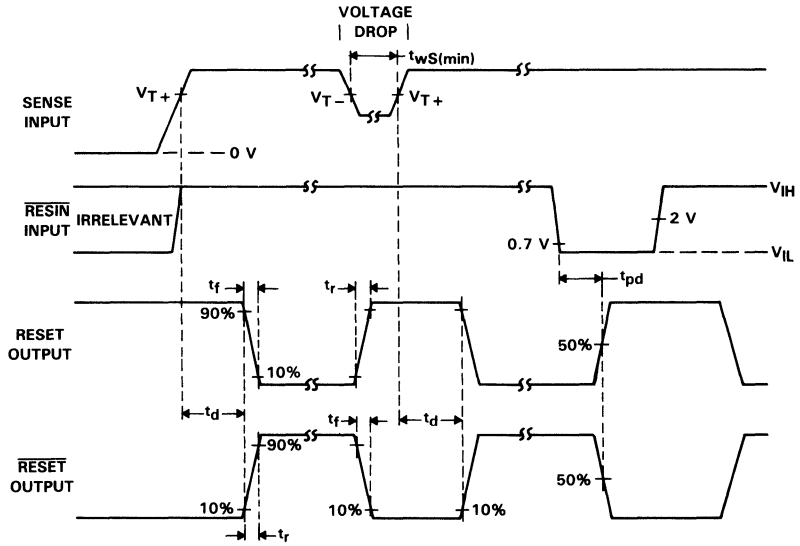


FIGURE 1. SWITCHING DIAGRAM

TYPICAL APPLICATION DATA

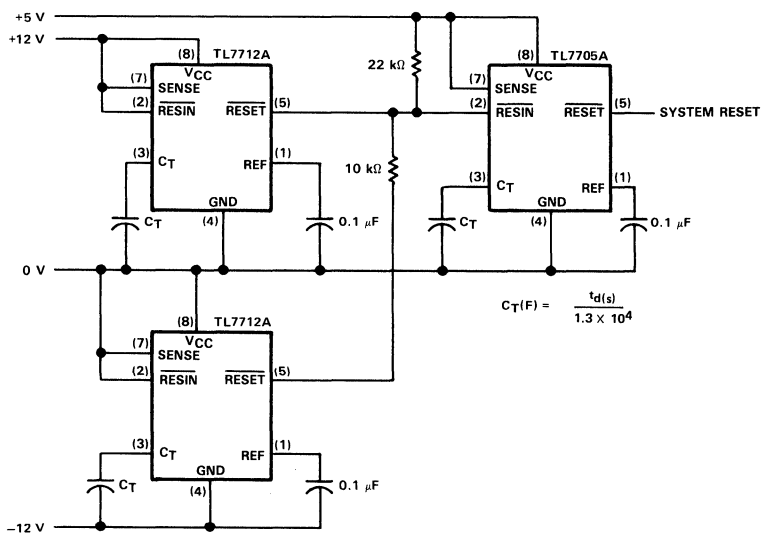


FIGURE 2. MULTIPLE POWER SUPPLY SYSTEM RESET GENERATION

TYPICAL APPLICATION DATA

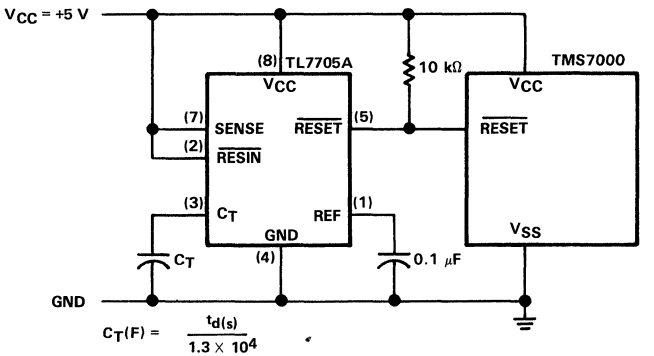


FIGURE 3. RESET CONTROLLER FOR TMS7000 SYSTEM

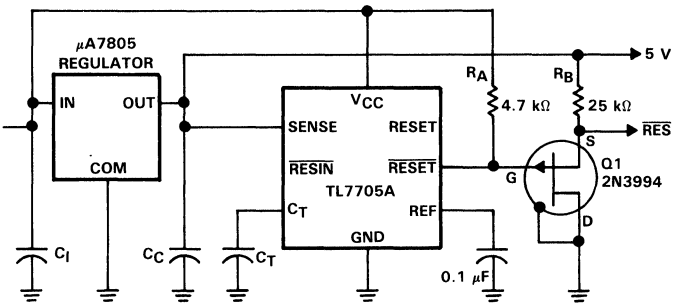


FIGURE 4. ELIMINATING UNDEFINED STATES USING A P-CHANNEL JFET

TYPICAL APPLICATION DATA

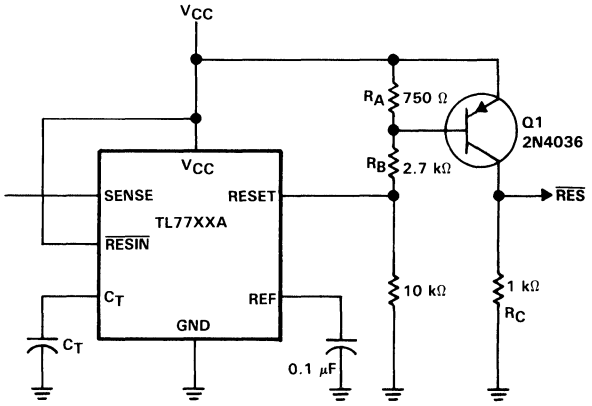
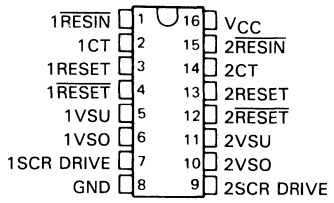


FIGURE 5. ELIMINATING UNDEFINED STATES USING A P-N-P TRANSISTOR

D3035, OCTOBER 1987—REVISED MAY 1988

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- $\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V
- Wide Supply Voltage Range . . . 3.5 V to 18 V
- Precision Overvoltage and Undervoltage Sensing
- 250-mA Peak Output Current for Driving SCR Gates
- 2-mA Active-Low SCR Gate Drive for False Trigger Protection
- Temperature-Compensated Voltage Reference
- True and Complementary Reset Outputs
- Externally Adjustable Output Pulse Duration

DW OR N PACKAGE
(TOP VIEW)



description

The TL7770 is a monolithic integrated circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU pins, respectively. When V_{CC} attains the minimum voltage of 1 V during power-up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the delay timer function activates latching RESET and $\overline{\text{RESET}}$ active (high and low respectively) for a time delay, t_d, after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low will activate the time delay function, RESET and $\overline{\text{RESET}}$, during normal system voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value V_{T+} for a time delay, t_d, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

The overvoltage-detection circuit is programmable for a wide range of user designs. During an overvoltage condition, an internal SCR is triggered, providing 250 mA peak instantaneous current and 25 mA continuous current to the SCR gate drive pin, which can be used to drive an external high-current SCR gate or an overvoltage warning circuit.

The TL7770Q series is characterized for operation from −40°C to 125°C. The TL7770C series is characterized for operation from 0°C to 70°C.

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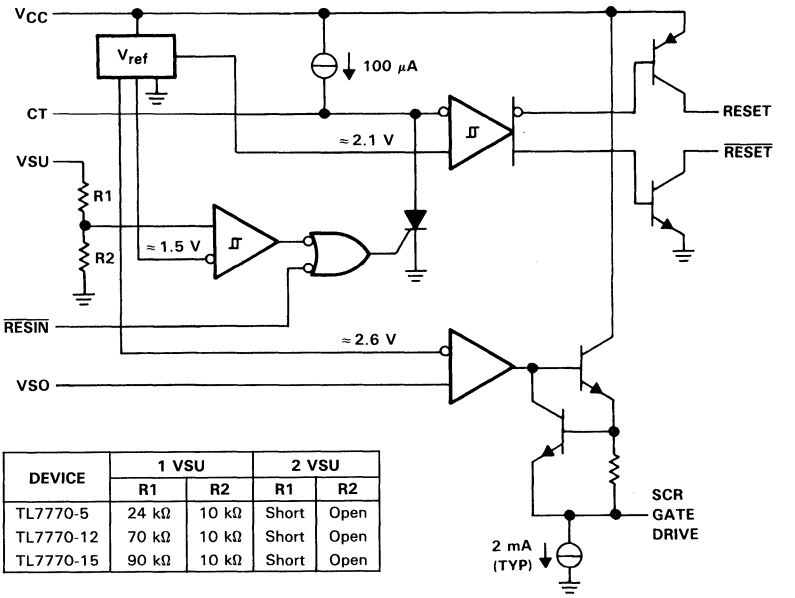
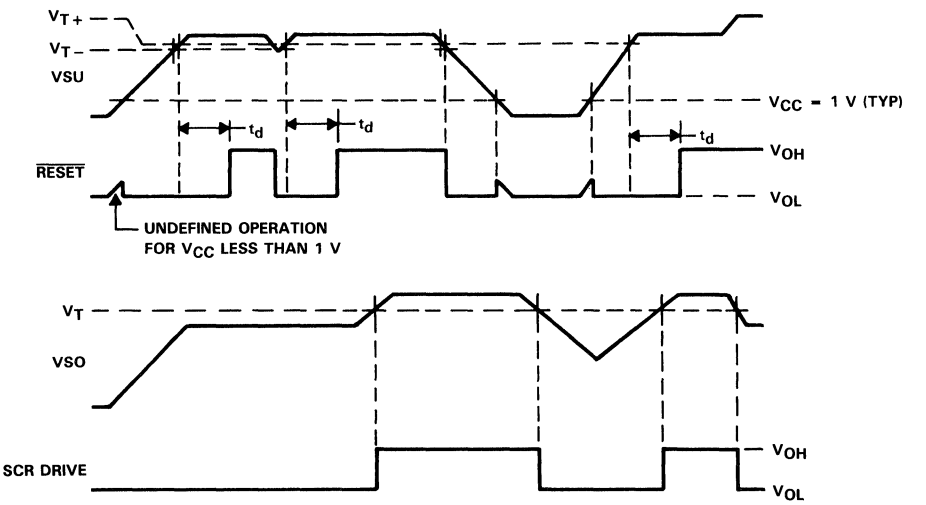
logic diagram (each channel)



DEVICE	1 VSU		2 VSU	
	R1	R2	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open
TL7770-15	90 kΩ	10 kΩ	Short	Open

typical timing diagram



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range, V_I: 1$\overline{VSU}$, 2VSU, 1$\overline{VSO}$, and 2VSO . . . . . −0.3 V to 18 V
Low-level output current (1$\overline{RESET}$ and 2$\overline{RESET}$), I_{OL} . . . . . 20 mA
High-level output current (1RESET and 2RESET), I_{OH} . . . . . −20 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range (see Note 2) . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1000 mW	8.2 mW/°C	25°C	656 mW	205 mW
N	1000 mW	12.4 mW/°C	69°C	992 mW	310 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 2)	1$\overline{RESIN}$, 2$\overline{RESIN}$, 1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage (1CT and 2CT), V_O			5	V
Output sink current (1CT and 2CT), I_O			50	μA
High-level output current (1RESET and 2RESET), I_{OH}			−16	mA
Low-level output current (1$\overline{RESET}$ and 2$\overline{RESET}$), I_{OL}			16	mA
Continuous output current (1SCR GATE DRIVE and 2SCR GATE DRIVE), I_O			25	mA
Operating free-air temperature, T_A	TL7770Q Series	−40	125	°C
	TL7770C Series	0	70	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH} High-level output voltage	RESET	I_{OH} = −15 mA	V_{CC}−1.5			V
	SCR GATE DRIVE	I_{OH} = −20 mA	V_{CC}−1.5			
V_{OL} Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{T-} Undervoltage threshold (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
	TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
	TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
	TL7770-5 (5-V sense, 1VSU)		4.46		4.64	
	TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
	TL7770-15 (15-V sense, 1VSU)		13.36		13.91	
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.47		1.53	
V_T Overvoltage threshold	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
		T_A = MIN to MAX	2.48		2.68	
V_{hys} Hysteresis ($V_{T+} - V_{T-}$) at VSU	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
	TL7770-12 (12-V sense, 1VSU)			36		
	TL7770-15 (15-V sense, 1VSU)			45		
	TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
I_I Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			−10	μA
	VSO	V_I = 2.4 V		0.5	2	
I_{OH} High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	μA
I_{OL} Low-level output current	RESET	V_O = 0			−50	μA
I_{OH} Peak output current	SCR GATE DRIVE	Duration = 1 ms	250			mA

total device

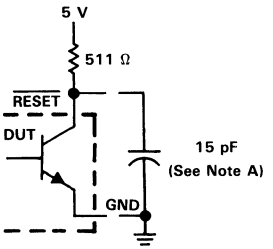
PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
I_{CC} Supply current	1VSU and 2VSU at > V_{T+}, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
		T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

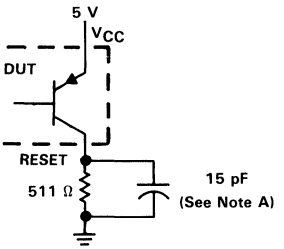
switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	RESET	See Figure 1		270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	RESET			270	500	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
t_r	Rise time		RESET				75	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{RESET}$			75		ns
t_f	Fall time						50	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{RESIN}$		See Figure 2(a)		150		ns
		VSU		See Figure 2(b)		100		

PARAMETER MEASUREMENT INFORMATION



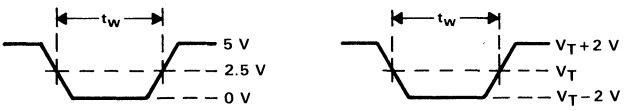
$\overline{\text{RESET}}$ OUTPUT CONFIGURATION



RESET OUTPUT CONFIGURATION

NOTE A: Includes jig and probe capacitance.

FIGURE 1. RESET AND $\overline{\text{RESET}}$ OUTPUT CONFIGURATIONS



(a) $\overline{\text{RESIN}}$ (b) VSU

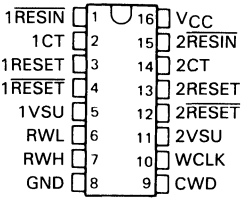
WAVEFORMS

FIGURE 2. INPUT PULSE DEFINITION

D3016, NOVEMBER 1988

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Wide Supply Voltage Range . . . 3.5 V to 18 V
- Dual Precision Undervoltage Comparators
- Temperature-Compensated Voltage Reference
- True and Complementary Reset Outputs
- Externally Adjustable Pulse Duration
- Outputs Valid When V_{CC} Exceeds 1 V
- Precision Watchdog Function
- Externally Set Timing Window
- Externally Set Delay

D OR N PACKAGE
(TOP VIEW)



description

The TL7780 is a monolithic integrated circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power supply systems. This device contains two independent supply-voltage supervisors and one watchdog function. The voltage supervisors monitor the supply voltages at the VSU pins. When V_{CC} attains the minimum voltage of 1 V during power-up, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the outputs remain active after the voltage at VSU exceeds the threshold value V_{T+} for a time delay (t_d) determined by an external timing capacitor such that:

t_d = (constant to be determined) X capacitance

where t_d is in seconds and capacitance is in farads

The "watchdog" function monitors the system activity by sensing the positive edge of a programmer-generated signal at WCLK. An on-board current source generates a voltage ramp v_{cwd} across the external capacitor connected to CWD, which is compared to a timing window (set by external resistors connected to RWL and RWH) at the instant of the occurrence of the positive edge of the programmer-generated signal WCLK. If the positive edge of WCLK occurs before v_{cwd} reaches the voltage at RWL or after v_{cwd} reaches the voltage at RWH, then 1RESET and $\overline{\text{1RESET}}$ become active, resetting the system for a period t_d. A precision current source, which tracks with the CWD charging current, allows RWL and RWH to be set by external resistors, creating a temperature-compensated "watchdog" window.

To set up the required frequency window for WCLK, the following conditions must exist:

1) $C_{WD} > 100$ pF, $R_{WL} > 10$ kΩ, $R_{WH} > 40$ kΩ

2) $f_L = \frac{1}{R_{WH}} \times C_{WD}$, $f_H = \frac{1}{R_{WL}} \times C_{WD}$

The TL7780Q series is characterized for operation from −40°C to 125°C. The TL7780C series is characterized for operation from 0°C to 70°C.

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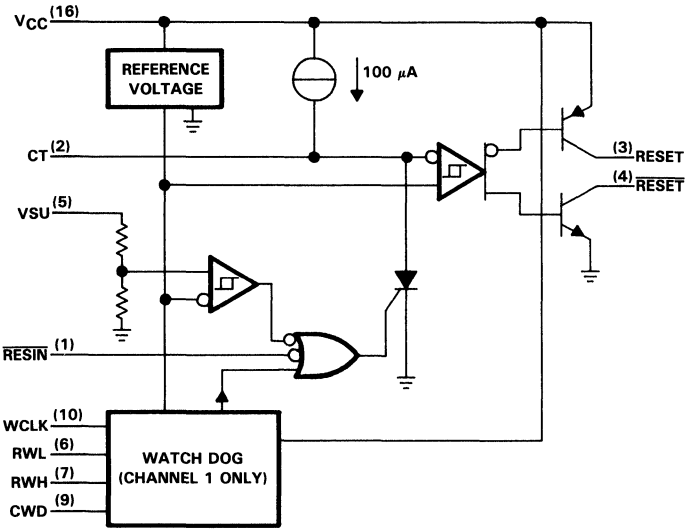
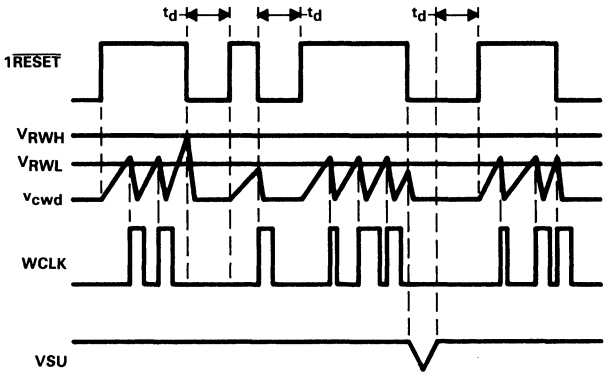
logic diagram (each channel)†



† Pin numbers for channel 1 are shown; pin 16 is common to both channels.

functional timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range 1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$, 1VSU, 2VSU) . . . . . −0.3 V to V_{CC}
High-level output current 1RESET and 2RESET, I_{OH}: . . . . . −20 mA
Low-level output current 1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$, I_{OL}: . . . . . 20 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	190 mW
N	1000 mW	12.5 mW/°C	1000 mW	312 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage, V_I	1$\overline{\text{RESIN}}$, 2$\overline{\text{RESIN}}$, 1VSU, 2VSU, V_I, See Note 2	−0.3	18	V
Output voltage (1CT and 2CT), V_O			5	V
Output sink current (1CT and 2CT), I_O			50	µA
High-level output current (1RESET and 2RESET), I_{OH}			−16	mA
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL}			16	mA
Operating free-air temperature, T_A	TL7780Q Series	−40	125	°C
	TL7780C Series	0	70	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for input voltage levels and temperature only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and operating free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	RESET	I_{OH} = −15 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{T-}	Undervoltage threshold (negative-going)	TL7780-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
		TL7780-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7780-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7780-5, TL7780-12, TL7780-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
		TL7780-5 (5-V sense, 1VSU)		4.46		4.64	
		TL7780-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7780-15 (15-V sense, 1VSU)		13.36		13.91	
		TL7780-5, TL7780-12, TL7780-15 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis (V_{T+} − V_{T-}) at VSU	TL7780-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7780-12 (12-V sense, 1VSU)			36		
		TL7780-15 (15-V sense, 1VSU)			45		
		TL7780-5, TL7780-12, TL7780-15 (programmable sense, 2VSU)			5		
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			−10	µA
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	µA
I_{OL}	Low-level output current	RESET	V_O = 0			−50	µA

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and operating free-air temperature, Ct at 0.1 µF to GND (unless otherwise noted)

"watchdog" section

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_T	Input threshold voltage	WCLK	V_{CC} = 3.5 V to 18 V	0.4		1.8	V
I_I	Input current	WCLK	V_I = 2.4 V			100	µA
			V_I = 0.4 V			200	
	Charging current	CWD	V_{CC} = 3.5 V to 18 V	45		55	µA
I_O	Output current	RWL and RWH	V_{CC} = 3.5 V to 18 V	45		55	µA

total device

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	VSU and $\overline{\text{RESIN}}$ at V_{CC}	T_A = 25°C			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.

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switching characteristics, V_{CC} = 5 V, Cr open, T_A = 25°C (see Figure 1)

supply supervisor section

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	1$\overline{\text{RESIN}}$	1RESET	C_L = 15 pF		100	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	2$\overline{\text{RESIN}}$	2RESET			100	500	ns
t_{PLH}	Propagation delay time, low-to-high-level output	2$\overline{\text{RESIN}}$	2$\overline{\text{RESET}}$			100	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	1$\overline{\text{RESIN}}$	1$\overline{\text{RESET}}$			100	500	ns
t_r	Rise time	1RESET or 2RESET					75	ns
t_f	Fall time						50	
t_r	Rise time	1$\overline{\text{RESET}}$ or 2$\overline{\text{RESET}}$					75	ns
t_f	Fall time						50	

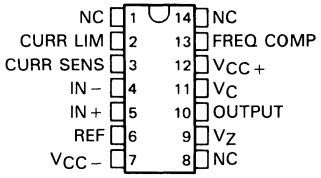
"watchdog" section

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	WCLK	1RESET	C_L = 15 pF,		100	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	WCLK	1RESET	R_{WL} = 60 kΩ,		100	500	ns
t_{PLH}	Propagation delay time, low-to-high-level output	WCLK	1$\overline{\text{RESET}}$	R_{WH} = 60 kΩ,		100	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	WCLK	1$\overline{\text{RESET}}$	CWD = 2 V		100	500	ns
t_{PLH}	Propagation delay time, low-to-high-level output	WCLK	CWD	C_{WD} = 15 pF		100	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	WCLK	CWD	(probe capacitance)		100	500	ns

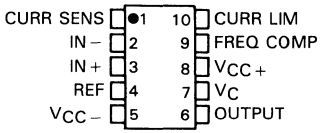
D1063, AUGUST 1972—REVISED OCTOBER 1988

- **150-mA Load Current Without External Power Transistor**
- **Typically 0.02% Input Regulation and 0.03% Load Regulation (uA723M)**
- **Adjustable Current Limiting Capability**
- **Input Voltages to 40 V**
- **Output Adjustable from 2 to 37 V**
- **Direct Replacement for Fairchild μA723M and μA723C**

uA723M . . . J PACKAGE
uA723C . . . D, J, OR N PACKAGE
(TOP VIEW)



uA723M . . . U PACKAGE
(TOP VIEW)



NC—No internal connection

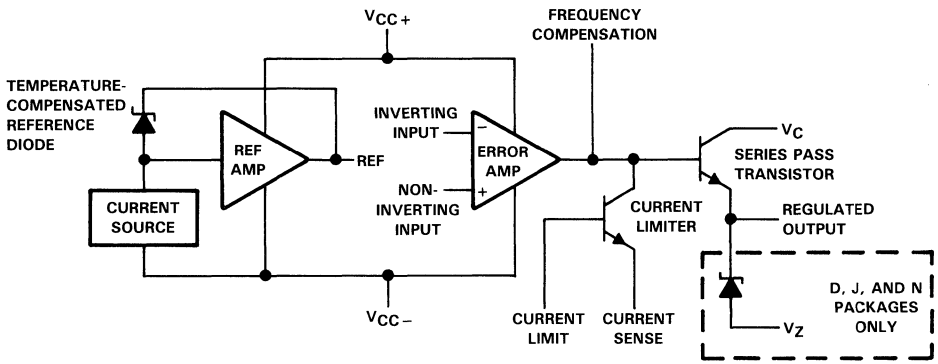
description

The uA723M and uA723C are monolithic integrated circuit voltage regulators featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference voltage amplifier, an error amplifier, a 150-mA output transistor, and an adjustable output current limiter.

The uA723M and uA723C are designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements may be connected as shown in Figures 4 and 5.

The uA723M is characterized for operation over the full military temperature range of −55°C to 125°C. The uA723C is characterized for operation from 0°C to 70°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Peak voltage from V_{CC+} to V_{CC-} ($t_w \leq 50$ ms) . . . . . 50 V
Continuous voltage from V_{CC+} to V_{CC-} . . . . . 40 V
Input-to-output voltage differential . . . . . 40 V
Differential input voltage to error amplifier . . . . . ±5 V
Voltage between noninverting input and V_{CC-} . . . . . 8 V
Current from V_Z . . . . . 25 mA
Current from REF . . . . . 15 mA
Continuous total dissipation (see Note 1) . . . . . See Dissipation Rating Table
Operating free-air temperature range: uA723M Circuits . . . . . −55°C to 125°C
uA723C Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or U package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: Power dissipation = $[I_{I(standby)} + I_{(ref)}] V_{CC} + [V_C - V_O] I_O$.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	
J (uA-M)	1000 mW	11.0 mW/°C	59°C	880 mW	275 mW
J (uA-C)	1000 mW	8.2 mW/°C	28°C	656 mW	
N	1000 mW	9.2 mW/°C	41°C	736 mW	
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA

electrical characteristics at specified free-air temperature (see Notes 2 and 3)

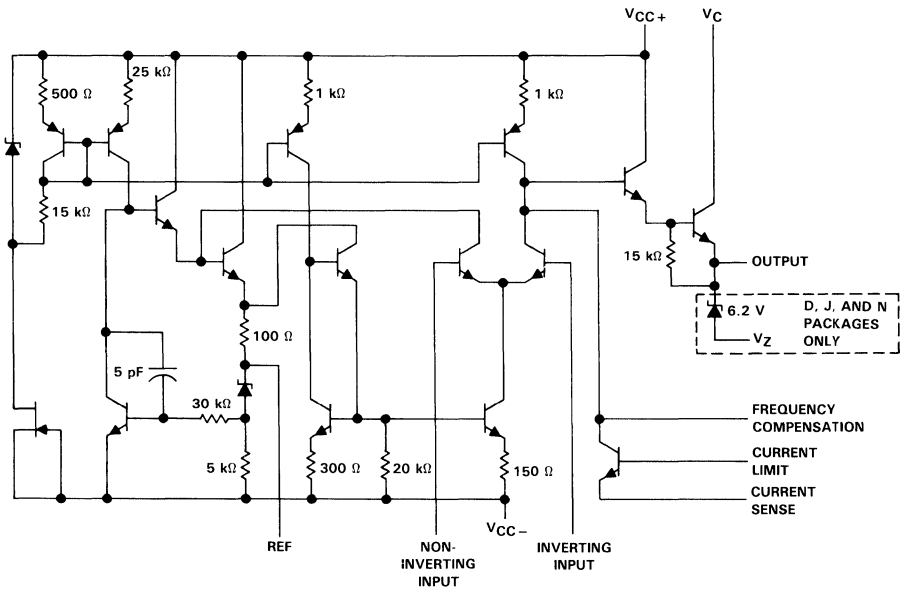
PARAMETER	TEST CONDITIONS†		uA723M			uA723C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V	25°C		0.01%	0.1%		0.01%	0.1%	
	V_I = 12 V to V_I = 40 V	25°C		0.02%	0.2%		0.1%	0.5%	
	V_I = 12 V to V_I = 15 V	Full range			0.3%			0.3%	
Ripple rejection	f = 50 Hz to 10 kHz, $C_{(ref)}$ = 0	25°C		74			74		dB
	f = 50 Hz to 10 kHz, $C_{(ref)}$ = 5 μF	25°C		86			86		
Output regulation	I_O = 1 mA to I_O = 50 mA	25°C		−0.03%	−0.15%		−0.03%	−0.2%	
		Full range			−0.6%			−0.6%	
Reference voltage, $V_{(ref)}$		25°C	6.95	7.15	7.35	6.8	7.15	7.5	V
Standby current	V_I = 30 V, I_O = 0	25°C		2.3	3.5		2.3	4	mA
Temperature coefficient of output voltage		Full range		0.002	0.015		0.003	0.015	%/°C
Short-circuit output current	R_{SC} = 10 Ω, V_O = 0	25°C		65			65		mA
Output noise voltage	BW = 100 Hz to 10 kHz, $C_{(ref)}$ = 0	25°C		20			20		μV
	BW = 100 Hz to 10 kHz, $C_{(ref)}$ = 5 μF	25°C		2.5			2.5		

†Full range for uA723M is −55°C to 125°C and for uA723C is 0°C to 70°C.

NOTES: 2. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier ≤ 10 kΩ. Unless otherwise specified, $V_I = V_{CC+} = V_C$ = 12 V, V_{CC-} = 0, V_O = 5 V, I_O = 1 mA, R_{SC} = 0, and $C_{(ref)}$ = 0.

3. Pulse testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

schematic



RESISTOR AND CAPACITOR VALUES SHOWN ARE NOMINAL.

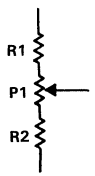
TYPICAL APPLICATION DATA

TABLE 1. RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 3)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 4)			OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 3)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 4)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	P2 (kΩ)			R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	P2 (kΩ)
+3.0	1,5,6,9,11, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	105	2.2	10	91
+3.6	1,5,6,9,11, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1,5,6,9,11, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (Note 5)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1,5,6,9,11, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2,4, (5,6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2,4, (5,6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.57	11.5	1.2	0.5	4.3
+15	2,4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2,4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	95.3	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

NOTES: 3. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use the figure numbers without parentheses. If the divider is across V_O, use the figure numbers in parentheses.

4. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown below.



ADJUSTABLE OUTPUT CIRCUIT

5. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

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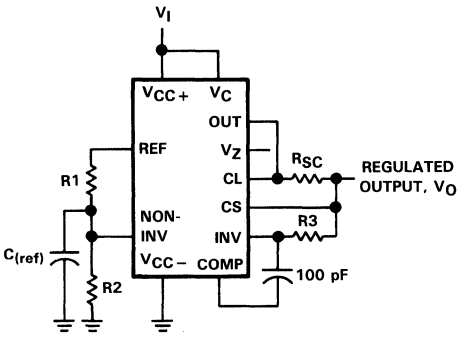
TYPICAL APPLICATION DATA

TABLE 2. FORMULAS FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 V [Figures 1,5,6,9, 11, 12, (4)] $V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	Outputs from +4 to +250 V (Figure 7) $V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1}$; $R3 = R4$	Current Limiting $I_{(limit)} \approx \frac{0.65\ V}{R_{SC}}$
Outputs from +7 to +37 V [Figures 2,4,(5,6,9, 11, 12)] $V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	Outputs from −6 to −250 V [Figures 3,8, 10] $V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$; $R3 = R4$	Foldback Current Limiting [Figure 6] $I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\ 0.65\ V}{R_{SC} R4}$; $I_{OS} \approx \frac{0.65\ V}{R_{SC}} \times \frac{R3 + R4}{R4}$

NOTES: 3. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$ and uses figures without parentheses, use figures with parentheses when the divider is across V_O.
4. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown at the right.
5. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

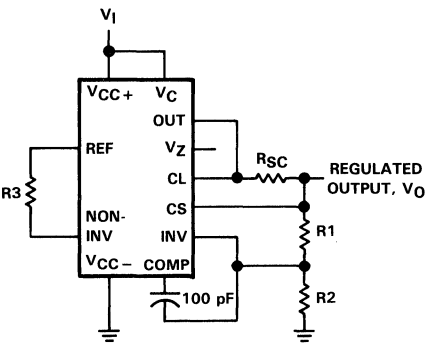
TYPICAL APPLICATION DATA



NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum αV_O.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 1. BASIC LOW-VOLTAGE REGULATOR (V_O = 2 TO 7 VOLTS)



NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum αV_O.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 2. BASIC HIGH-VOLTAGE REGULATOR (V_O = 7 TO 37 VOLTS)

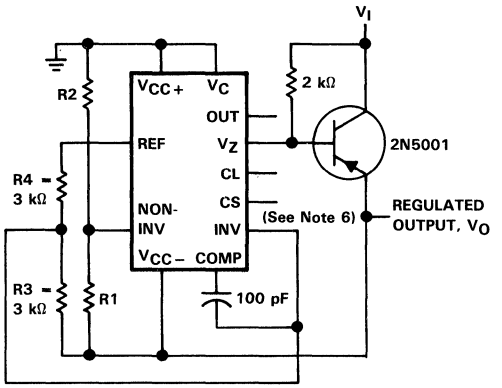


FIGURE 3. NEGATIVE-VOLTAGE REGULATOR

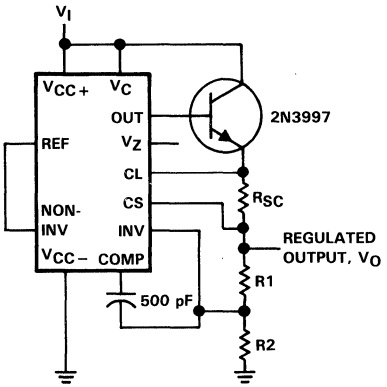


FIGURE 4. POSITIVE-VOLTAGE REGULATOR (EXTERNAL N-P-N PASS TRANSISTOR)

NOTE 6: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the OUT terminal.

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TYPICAL APPLICATION DATA

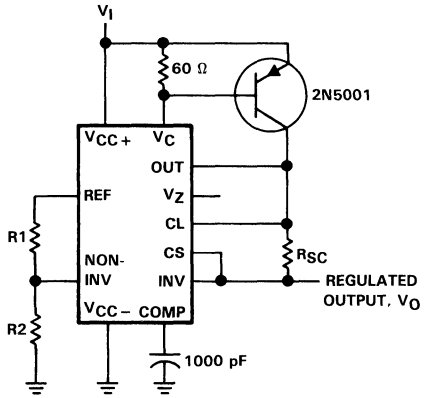

FIGURE 5. POSITIVE-VOLTAGE REGULATOR (EXTERNAL P-N-P PASS TRANSISTOR)

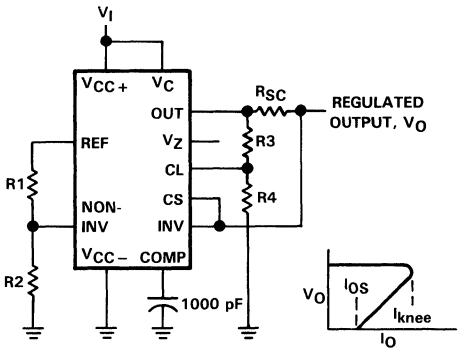

FIGURE 6. FOLDBACK CURRENT LIMITING

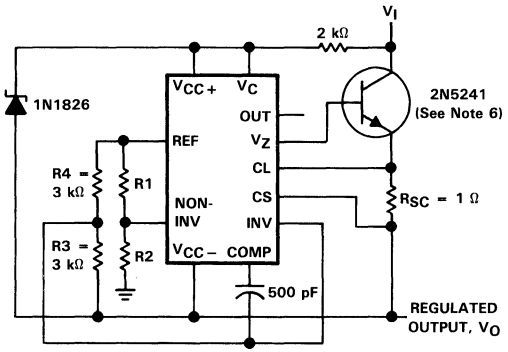

FIGURE 7. POSITIVE FLOATING REGULATOR

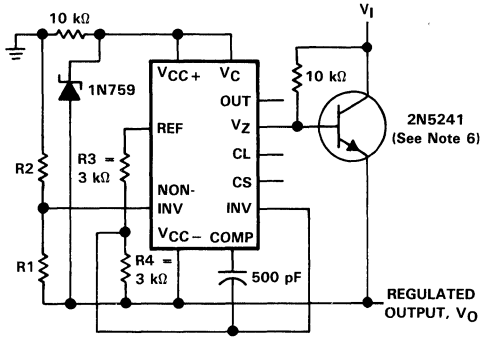

FIGURE 8. NEGATIVE FLOATING REGULATOR

NOTE 6: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the OUT terminal.

TYPICAL APPLICATION DATA

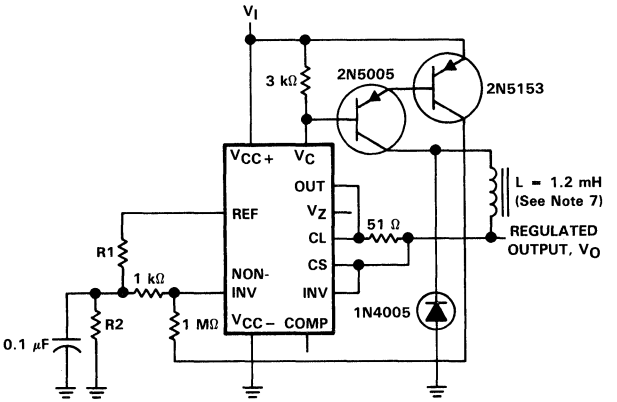

FIGURE 9. POSITIVE SWITCHING REGULATOR

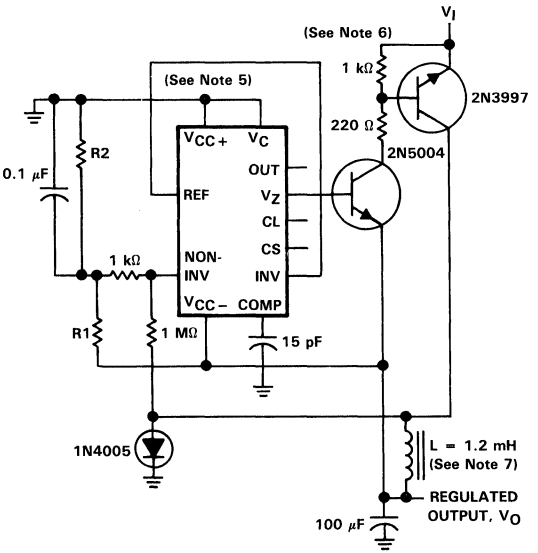

FIGURE 10. NEGATIVE SWITCHING REGULATOR

NOTES: 5. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

6. When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the OUT terminal.

7. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with an 0.009-inch air gap.

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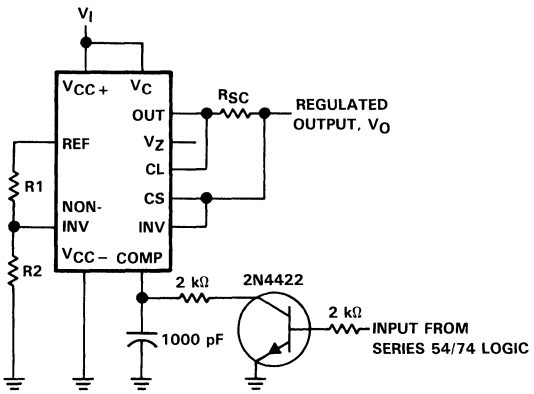
TYPICAL APPLICATION DATA



NOTE A: Current limit transistor may be used for shutdown if current limiting is not required.

FIGURE 11. REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

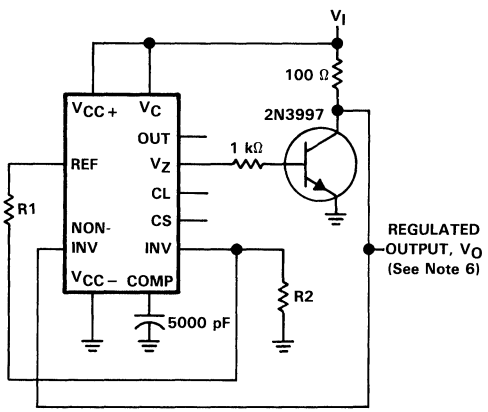


FIGURE 12. SHUNT REGULATOR

NOTE 6: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the OUT terminal.

D2154, MAY 1976—REVISED APRIL 1988

- 3-Terminal Regulators
- Output Current Up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μA7800 Series

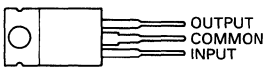
NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	uA7805C
6 V	uA7806C
8 V	uA7808C
8.5 V	uA7885C
10 V	uA7810C
12 V	uA7812C
15 V	uA7815C
18 V	uA7818C
24 V	uA7824C

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

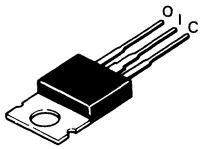
KC PACKAGE

(TOP VIEW)

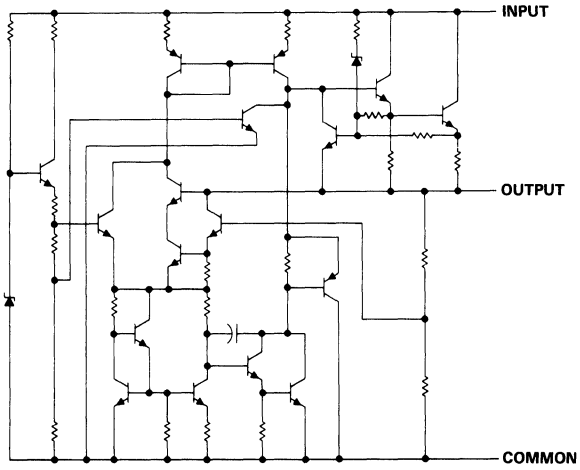


THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



schematic



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absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78__ __C	UNIT
Input voltage	uA7824C	40	V
	All others	35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)		2	W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	W
Operating free-air, case, or virtual junction temperature range		0 to 150	°C
Storage temperature range		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

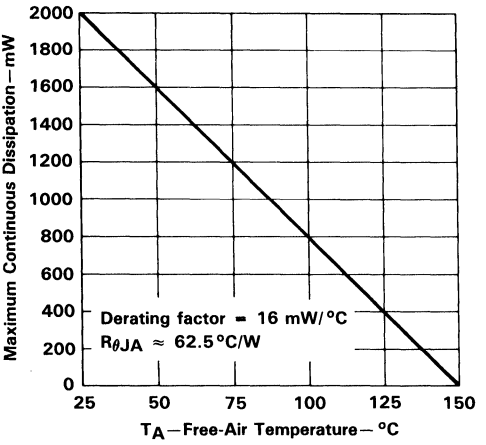

FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

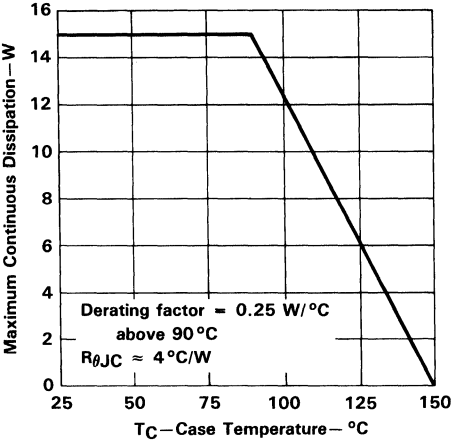

FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7805C	7	25	V
	uA7806C	8	25	
	uA7808C	10.5	25	
	uA7885C	10.5	25	
	uA7810C	12.5	28	
	uA7812C	14.5	30	
	uA7815C	17.5	30	
	uA7818C	21	33	
	uA7824C	27	38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

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uA7805C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7805C			UNIT
			MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, P ≤ 15 W	25°C	4.8	5	5.2	V
		0°C to 125°C	4.75		5.25	
Input regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	62	78		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	0°C to 125°C		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

uA7806C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7806C			UNIT
			MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 1 A, V_I = 8 V to 21 V, P ≤ 15 W	25°C	5.75	6	6.25	V
		0°C to 125°C	5.7		6.3	
Input regulation	V_I = 8 V to 25 V	25°C		5	120	mV
	V_I = 9 V to 13 V			1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	0°C to 125°C	59	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		14	120	mV
	I_O = 250 mA to 750 mA			4	60	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		45		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 8 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		550		mA
Peak output current		25°C		2.2		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7808C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7808C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	7.7	8	8.3	V
	I_O = 5 mA to 1 A, V_I = 10.5 V to 23 V, P ≤ 15 W	0°C to 125°C	7.6		8.4	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	160	mV
	V_I = 11 V to 17 V			2	80	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	55	72		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	160	mV
	I_O = 250 mA to 750 mA			4	80	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		52		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

uA7885C electrical characteristics at specified virtual junction temperature, V_I = 15 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7885C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	8.15	8.5	8.85	V
	I_O = 5 mA to 1 A, V_I = 11 V to 23.5 V, P ≤ 15 W	0°C to 125°C	8.1		8.9	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	170	mV
	V_I = 11 V to 17 V			2	85	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	170	mV
	I_O = 250 mA to 750 mA			4	85	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		55		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA7810C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7810C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	9.6	10	10.4	V
	I_O = 5 mA to 1 A, V_I = 12.5 V to 25 V, $P \leq 15$ W	0°C to 125°C	9.5	10	10.5	
Input regulation	V_I = 12.5 V to 28 V	25°C		7	200	mV
	V_I = 14 V to 20 V			2	100	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	200	mV
	I_O = 250 mA to 750 mA			4	100	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 12.5 V to 28 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

uA7812C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7812C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	11.5	12	12.5	V
	I_O = 5 mA to 1 A, V_I = 14.5 V to 27 V, $P \leq 15$ W	0°C to 125°C	11.4		12.6	
Input regulation	V_I = 14.5 V to 30 V	25°C		10	240	mV
	V_I = 16 V to 22 V			3	120	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	240	mV
	I_O = 250 mA to 750 mA			4	120	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7815C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7815C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	14.4	15	15.6	V
	I_O = 5 mA to 1 A, V_I = 17.5 V to 30 V, P ≤ 15 W	0°C to 125°C	14.25		15.75	
Input regulation	V_I = 17.5 V to 30 V	25°C		11	300	mV
	V_I = 20 V to 26 V			3	150	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	300	mV
	I_O = 250 mA to 750 mA			4	150	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.4	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

uA7818C electrical characteristics at specified virtual junction temperature, V_I = 27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7818C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	17.3	18	18.7	V
	I_O = 5 mA to 1 A, V_I = 21 V to 33 V, P ≤ 15 W	0°C to 125°C	17.1		18.9	
Input regulation	V_I = 21 V to 33 V	25°C		15	360	mV
	V_I = 24 V to 30 V			5	180	
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz	0°C to 125°C	53	69		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	360	mV
	I_O = 250 mA to 750 mA			4	180	
Output resistance	f = 1 kHz	0°C to 125°C		0.022		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.0		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		110		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.5	8	mA
Bias current change	V_I = 21 V to 33 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		200		mA
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7824C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7824C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	23	24	25	V
	I_O = 5 mA to 1 A, V_I = 27 V to 38 V, P ≤ 15 W	0°C to 125°C	22.8		25.2	
Input regulation	V_I = 27 V to 38 V	25°C		18	480	mV
	V_I = 30 V to 36 V			6	240	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	0°C to 125°C	50	66		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	480	mV
	I_O = 250 mA to 750 mA			4	240	
Output resistance	f = 1 kHz	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		170		μV
Dropout voltage	I_O = 1 A	25°C		2.0		V
Bias current		25°C		4.6	8	mA
Bias current change	V_I = 27 V to 38 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

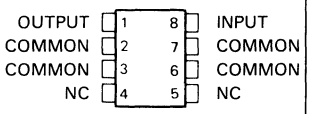
D2203, JANUARY 1976—REVISED FEBRUARY 1988

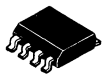
- 3-Terminal Regulators
- Output Current Up to 100 mA
- No External Components
- Internal Thermal Overload Protection
- Internal Short-Circuit Limiting
- Direct Replacement for Fairchild μA78L00 Series

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
2.6 V	uA78L02AC	uA78L02C
5 V	uA78L05AC	uA78L05C
6.2 V	UA78L06AC	uA78L06C
8 V	uA78L08AC	uA78L08C
9 V	uA78L09AC	uA78L09C
10 V	uA78L10AC	uA78L10C
12 V	uA78L12AC	uA78L12C
15 V	uA78L15AC	uA78L15C

D
"SMALL OUTLINE" PACKAGE

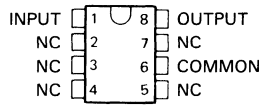
(TOP VIEW)





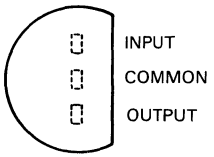
JG
DUAL-IN-LINE PACKAGE

(TOP VIEW)



LP
SILECT PACKAGE

(TOP VIEW)



TO-226AA

OCI

NC—No internal connection

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained together with lower-bias current.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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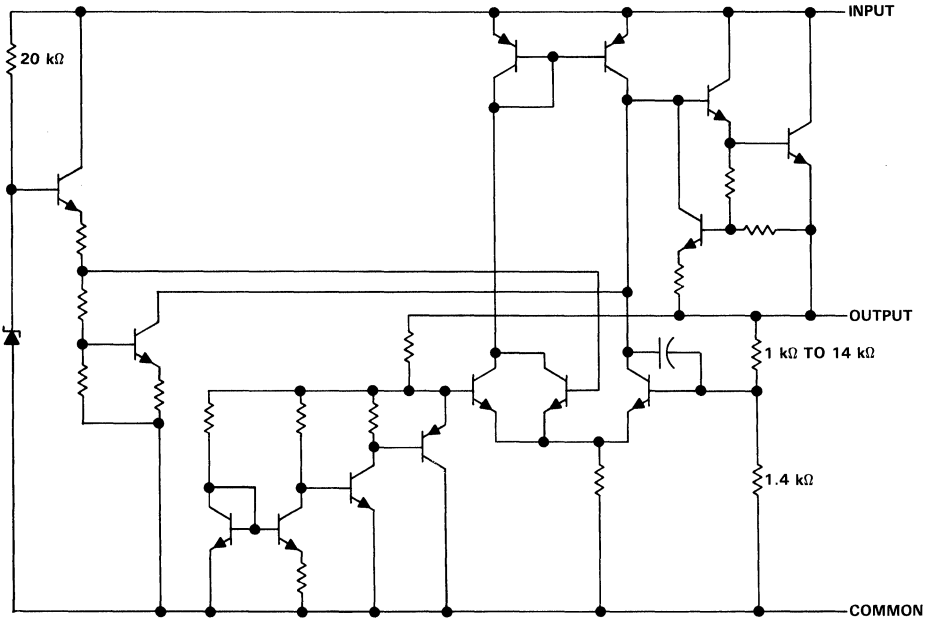
schematic



Resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating temperature range (unless otherwise noted)

	uA78L02AC, uA78L02C THRU uA78L10AC, uA78L10C	uA78L12AC, uA78L12C uA78L15AC, uA78L15C	UNIT
Input voltage	30	35	V
Continuous total dissipation (see Note 1)	See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range	0 to 150	0 to 150	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 — FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	825 mW	5.8 mW/°C	25°C	464 mW
JG	825 mW	6.6 mW/°C	25°C	528 mW
LP†	775 mW	6.2 mW/°C	25°C	496 mW

†The LP package dissipation rating is based on thermal resistance $R_{\theta JA}$ measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in) above the socket.

DISSIPATION RATING TABLE 2 — CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	19.6 mW/°C	65°C	490 mW
JG	1600 mW	17.2 mW/°C	57°C	430 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78L02C, uA78L02AC	4.75	20	V
	uA78L05C, uA78L05AC	7	20	
	uA78L06C, uA78L06AC	8.5	20	
	uA78L08C, uA78L08AC	10.5	23	
	uA78L09C, uA78L09AC	11.5	24	
	uA78L10C, uA78L10AC	12.5	25	
	uA78L12C, uA78L12AC	14.5	27	
	uA78L15C, uA78L15AC	17.5	30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J		0	125	°C

uA78L02AC, uA78L02C electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L02AC			uA78L02C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	2.5	2.6	2.7	2.4	2.6	2.8	V
	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	0°C to	2.45		2.75	2.35		2.85	
	I_O = 1 mA to 70 mA	125°C	2.45		2.75	2.35		2.85	
Input regulation	V_I = 4.75 V to 20 V	25°C		20	100		20	125	mV
	V_I = 5 V to 20 V			16	75		16	100	
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz	25°C	43	51		42	51		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		12	50		12	50	mV
	I_O = 1 mA to 40 mA			6	25		6	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30			30		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.6	6		3.6	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	0°C to			2.5			2.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

uA78L05AC, uA78L05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L05AC			uA78L05C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	4.8	5	5.2	4.6	5	5.4	V
	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	0°C to	4.75		5.25	4.5		5.5	
	I_O = 1 mA to 70 mA	125°C	4.75		5.25	4.5		5.5	
Input regulation	V_I = 7 V to 20 V	25°C		32	150		32	200	mV
	V_I = 8 V to 20 V			26	100		26	150	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	41	49		40	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		15	60		15	60	mV
	I_O = 1 mA to 40 mA			8	30		8	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78L06AC, uA78L06C electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L06AC			uA78L06C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	5.95	6.2	6.45	5.7	6.2	6.7	V
	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	0°C to	5.9		6.5	5.6		6.8	
	I_O = 1 mA to 70 mA	125°C	5.9		6.5	5.6		6.8	
Input regulation	V_I = 8.5 V to 20 V	25°C		35	175		35	200	mV
	V_I = 9 V to 20 V			29	125		29	150	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	40	48		39	48		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		16	80		16	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

uA78L08AC, uA78L08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L08AC			uA78L08C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	7.7	8	8.3	7.36	8	8.64	V
	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	0°C to	7.6		8.4	7.2		8.8	
	I_O = 1 mA to 70 mA	125°C	7.6		8.4	7.2		8.8	
Input regulation	V_I = 10.5 V to 23 V	25°C		42	175		42	200	mV
	V_I = 11 V to 23 V			36	125		36	150	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	37	46		36	46		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		18	80		18	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 11 V to 23 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78L09AC, uA78L09C electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L09AC			uA78L09C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	8.6	9	9.4	8.3	9	9.7	V
	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	0°C to	8.55		9.45	8.1		9.9	
	I_O = 1 mA to 70 mA	125°C	8.55		9.45	8.1		9.9	
Input regulation	V_I = 12 V to 24 V	25°C		45	175		45	225	mV
	V_I = 13 V to 24 V			40	125		40	175	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	38	45		36	45		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		19	90		19	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		58			58		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 13 V to 24 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

uA78L10AC, uA78L10C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L10AC			uA78L10C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	9.6	10	10.4	9.2	10	10.8	V
	V_I = 13 V to 25 V, I_O = 1 mA to 40 mA	0°C to	9.5		10.5	9		11	
	I_O = 1 mA to 70 mA	125°C	9.5		10.5	9		11	
Input regulation	V_I = 13 V to 25 V	25°C		51	175		51	225	mV
	V_I = 14 V to 25 V			42	125		42	175	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	37	44		36	44		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		20	90		20	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		62			62		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.2	6		4.2	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 14 V to 25 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78L12AC, uA78L12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L12AC			uA78L12C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	11.5	12	12.5	11.1	12	12.9	V
	V_I = 14 V to 27 V, I_O = 1 mA to 40 mA	0°C to	11.4		12.6	10.8		13.2	
	I_O = 1 mA to 70 mA	125°C	11.4		12.6	10.8		13.2	
Input regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			49	200		49	200	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	37	42		36	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		22	100		22	100	mV
	I_O = 1 mA to 40 mA			13	50		13	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

uA78L15AC, uA78L15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L15AC			uA78L15C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	14.4	15	15.6	13.8	15	16.2	V
	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	0°C to	14.25		15.75	13.5		16.5	
	I_O = 1 mA to 70 mA	125°C	14.25		15.75	13.5		16.5	
Input regulation	V_I = 17.5 V to 30 V	25°C		65	300		65	300	mV
	V_I = 20 V to 30 V			58	250		58	250	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	25°C	34	39		33	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		25	150		25	150	mV
	I_O = 1 mA to 40 mA			15	75		15	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	V_I = 10 V to 30 V	0°C to			1.5			1.5	mA
	I_O = 1 mA to 40 mA	125°C			0.1			0.2	

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

D2214, JUNE 1976—REVISED APRIL 1988

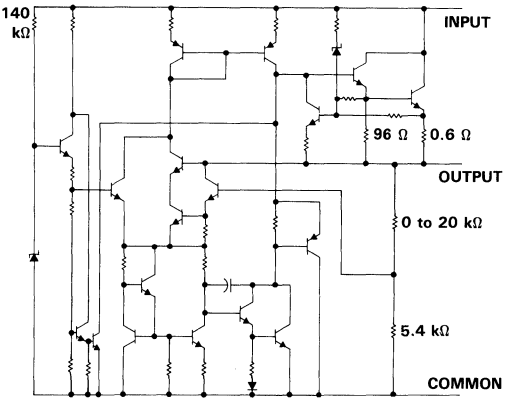
- 3-Terminal Regulators
- Output Current Up to 500 mA
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Direct Replacements for Fairchild μA78M00 Series

NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
5 V	uA78M05M	uA78M05C
6 V		uA78M06C
8 V		uA78M08C
9 V		uA78M09C
10 V		uA78M10C
12 V	uA78M12M	uA78M12C
15 V	uA78M15M	uA78M15C
20 V		uA78M20C
24 V		uA78M24C
PACKAGES	JG	KC

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

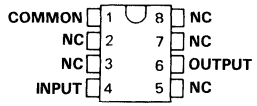


Resistor values shown are nominal.

terminal assignments

uA78M_M . . . JG PACKAGE

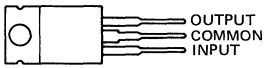
(TOP VIEW)



NC — No internal connection.

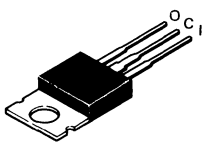
uA78M_C . . . KC PACKAGE

(TOP VIEW)



THE COMMON TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



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absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78M05M uA78M12M uA78M15M	uA78M05C THRU uA78M24C	UNIT
Input voltage	uA78M20, uA78M24		−40	V
	All others	35	35	
Continuous total dissipation (see Note 1)		See Dissipation Rating Tables 1 and 2		
Operating free-air, case or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	KC package		260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1—FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
JG	1050 mW	8.4 mW/°C	672 mW
KC	2000 mW	16 mW/°C	1280 mW

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \leq 50°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 50°C$	$T_C = 125°C$ POWER RATING
KC	20 W	200 mW/°C	5 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78M05M, uA78M05C	7	25	V
	uA78M06C	8	25	
	uA78M08C	10.5	25	
	uA78M09C	11.5	26	
	uA78M10C	12.5	28	
	uA78M12M, uA78M12C	14.5	30	
	uA78M15M, uA78M15C	17.5	30	
	uA78M20C	23	35	
	uA78M24C	27	38	
Output current, I_O	All devices		500	mA
Operating virtual junction temperature, T_J	uA78M05M thru uA78M15M	−55	150	°C
	uA78M05C thru uA78M24C	0	125	

uA78M05M, uA78M05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M05M			uA78M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	4.8	5	5.2	4.8	5	5.2	V
	I_O = 5 mA to 350 mA	V_I = 8 V to 20 V	−55°C to 150°C	4.7		5.3				
		V_I = 7 V to 20 V	0°C to 125°C				4.75		5.25	
Input regulation	I_O = 200 mA	V_I = 7 V to 25 V	25°C		3	50		3	100	mV
		V_I = 8 V to 20 V			1	25				
		V_I = 8 V to 25 V						1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	62						dB
			0°C to 125°C				62			
		I_O = 300 mA	25°C	62	80		62	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	50		20	100	mV
	I_O = 5 mA to 200 mA				10	25		10	50	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 25°C			−2				mV/°C
			25°C to 150°C			−1.5				
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40	200		40	200	μV
Dropout voltage			25°C		2	2.5		2	2.5	V
Bias current			25°C		4.5	7		4.5	6	mA
Bias current change	I_O = 200 mA, V_I = 8 V to 25 V		−55°C to 150°C			0.8				mA
			0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		300	600		300		mA
Peak output current			25°C	0.5	0.7	1.4		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M06C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage‡			25°C	5.75	6	6.25	V
	I_O = 5 mA to 350 mA	V_I = 8 V to 21 V	0°C to 125°C	5.7		6.3	
Input regulation	I_O = 200 mA	V_I = 8 V to 25 V	25°C		5	100	mV
		V_I = 9 V to 25 V			1.5	50	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	59			dB
		I_O = 300 mA	25°C	59	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	120	mV
	I_O = 5 mA to 200 mA				10	60	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		45		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.5	6	mA
Bias current change	I_O = 200 mA,	V_I = 9 V to 25 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		270		mA
Peak output current			25°C		0.7		A

uA78M08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage‡			25°C	7.7	8	8.3	V
	I_O = 5 mA to 350 mA	V_I = 10.5 V to 23 V	0°C to 125°C	7.6		8.4	
Input regulation	I_O = 200 mA	V_I = 10.5 V to 25 V	25°C		6	100	mV
		V_I = 11 V to 25 V			2	50	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	56			dB
		I_O = 300 mA	25°C	56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	160	mV
	I_O = 5 mA to 200 mA				10	80	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		52		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.6	6	mA
Bias current change	I_O = 200 mA,	V_I = 10.5 V to 25 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		250		mA
Peak output current			25°C		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA78M09C electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage ‡			25°C	8.6	9	9.4	V
	I_O = 5 mA to 350 mA	V_I = 11.5 V to 24 V	0°C to 125°C	8.5		9.5	
Input regulation	I_O = 200 mA	V_I = 11.5 V to 26 V	25°C		6	100	mV
		V_I = 12 V to 26 V			2	50	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	56			dB
		I_O = 300 mA	25°C	56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	180	mV
	I_O = 5 mA to 200 mA				10	90	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		58		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.6	6	mA
Bias current change	I_O = 200 mA,	V_I = 11.5 V to 26 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA					0.5	
Short-circuit output current	V_I = 35 V		25°C		250		mA
Peak output current			25°C		0.7		A

uA78M10C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage‡			25°C	9.6	10	10.4	V
	I_O = 5 mA to 350 mA	V_I = 12.5 V to 25 V	0°C to 125°C	9.5		10.5	
Input regulation	I_O = 200 mA	V_I = 12.5 V to 28 V	25°C		7	100	mV
		V_I = 14 V to 28 V			2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	59			dB
		I_O = 300 mA	25°C	55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	200	mV
	I_O = 5 mA to 200 mA				10	100	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		64		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.7	6	mA
Bias current change	I_O = 200 mA	V_I = 13.5 V to 28 V	0°C to 125°C			0.8	mA
		V_I = 12.5 V to 28 V					
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		245		mA
Peak output current			25°C		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M12M, uA78M12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M12M			uA78M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 350 mA	V_I = 15.5 V to 27 V	25°C	11.5	12	12.5	11.5	12	12.5	V
		V_I = 14.5 V to 27 V	−55°C to 150°C	11.4		12.6				
			0°C to 125°C				11.4		12.6	
Input regulation	I_O = 200 mA	V_I = 14.5 V to 30 V	25°C		8	60		8	100	mV
		V_I = 16 V to 25 V			2	30				
		V_I = 16 V to 30 V						2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	55						dB
			0°C to 125°C				55			
		I_O = 300 mA	25°C	55	80		55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	120		25	240	mV
	I_O = 5 mA to 200 mA				10	60		10	120	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 25°C			−4.8				mV/°C
			25°C to 150°C			−3.6				
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		75	480		75		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.8	7		4.8	6	mA
Bias current change	I_O = 200 mA	V_I = 15 V to 30 V	−55°C to 150°C			0.8				mA
		V_I = 14.5 V to 30 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240	600		240		mA
Peak output current			25°C	0.5	0.7	1.4		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA78M15M, uA78M15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M15M			uA78M15C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	14.4	15	15.6	14.4	15	15.6	V
	I_O = 5 mA to 350 mA	V_I = 18.5 V to 30 V	−55°C to 150°C	14.25		15.75				
		V_I = 17.5 V to 30 V	0°C to 125°C				14.25		15.75	
Input regulation	I_O = 200 mA	V_I = 17.5 V to 30 V	25°C		10	60		10	100	mV
		V_I = 20 V to 30 V			3	30		3	50	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	54						dB
			0°C to 125°C				54			
		I_O = 300 mA	25°C	54	70		54	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	150		25	300	mV
	I_O = 5 mA to 200 mA				10	75		10	150	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 25°C			−6				mV/°C
			25°C to 150°C			−4.5				
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		90	600		90		μV
Dropout voltage			25°C		2	2.5		2		V
Bias current			25°C		4.8	7		4.8	6	mA
Bias current change	I_O = 200 mA	V_I = 18.5 V to 30 V	−55°C to 150°C			0.8				mA
		V_I = 17.5 V to 30 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240	600		240		mA
Peak output current			25°C	0.5	0.7	1.4		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M20C electrical characteristics at specified virtual junction temperature, V_I = 29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage ‡			25°C	19.2	20	20.8	V
	I_O = 5 mA to 350 mA	V_I = 23 V to 35 V	0°C to 125°C	19		21	
Input regulation	I_O = 200 mA	V_I = 23 V to 35 V	25°C		10	100	mV
		V_I = 24 V to 35 V			5	50	
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	53			dB
		I_O = 300 mA	25°C	53	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	400	mV
	I_O = 5 mA to 200 mA				10	200	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		110		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.9	6	mA
Bias current change	I_O = 200 mA,	V_I = 23 V to 35 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA					0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA78M24C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Output voltage‡			25°C	23	24	25	V
	I_O = 5 mA to 350 mA	V_I = 27 V to 38 V	0°C to 125°C	22.8		25.2	
Input regulation	I_O = 200 mA	V_I = 27 V to 38 V	25°C		10	100	mV
		V_I = 28 V to 38 V			5	50	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				dB
			0°C to 125°C	50			
		I_O = 300 mA	25°C	50	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	480	mV
	I_O = 5 mA to 200 mA				10	240	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.2		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		170		μV
Dropout voltage			25°C		2		V
Bias current			25°C		5	6	mA
Bias current change	I_O = 200 mA,	V_I = 27 V to 38 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

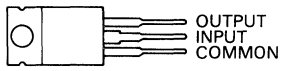
D2215, JUNE 1976—REVISED AUGUST 1983

- 3-Terminal Regulators
- Output Current Up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Essentially Equivalent to National LM320 Series

NOMINAL OUTPUT VOLTAGE	REGULATOR
−5 V	uA7905C
−5.2 V	uA7952C
−6 V	uA7906C
−8 V	uA7908C
−12 V	uA7912C
−15 V	uA7915C
−18 V	uA7918C
−24 V	uA7924C

KC PACKAGE

(TOP VIEW)



THE INPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

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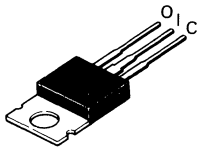
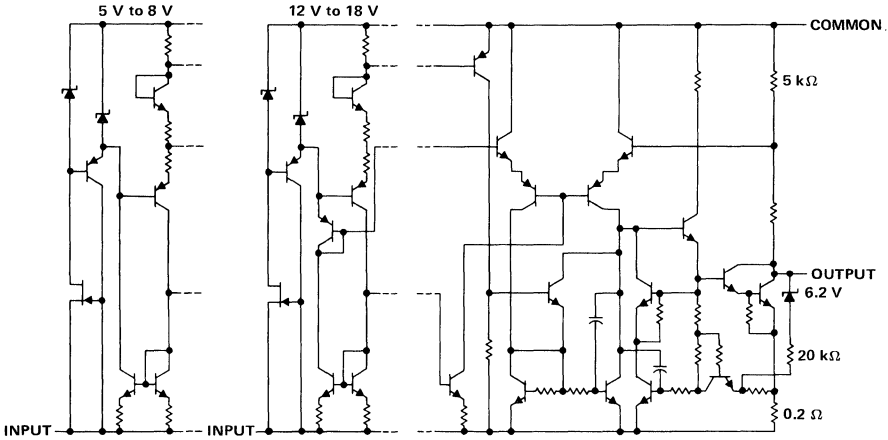


description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA7800 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic



All component values are nominal.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA7905C THRU uA7924C	UNIT
Input voltage	uA7924C	−40	V
	All others	−35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)		2	W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	W
Operating free-air, case, or virtual junction temperature range		0 to 150	°C
Storage temperature range		−65 to 150	°C
Lead temperature 3.2 mm (1/8 inch) from case for 10 seconds		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

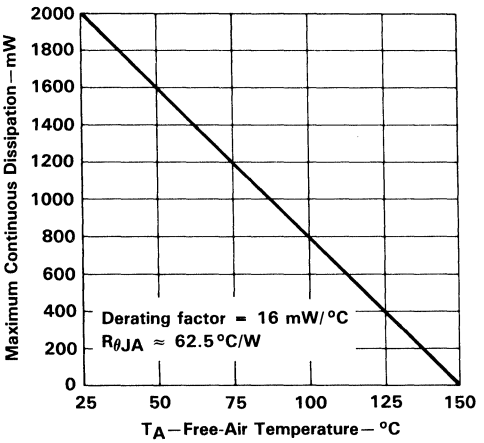

FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

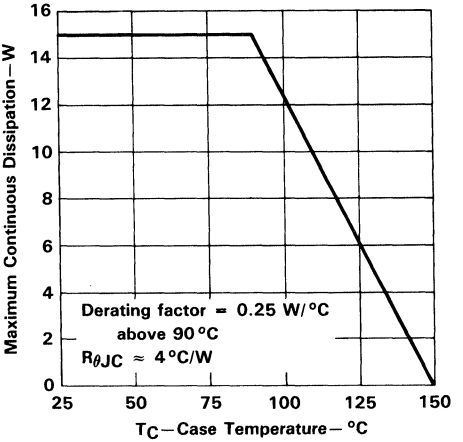

FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7905C	−7	−25	V
	uA7952C	−7.2	−25	
	uA7906C	−8	−25	
	uA7908C	−10.5	−25	
	uA7912C	−14.5	−30	
	uA7915C	−17.5	−30	
	uA7918C	−21	−33	
	uA7924C	−27	−38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

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uA7905C electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7905C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−4.8	−5	−5.2	V
	I_O = 5 mA to 1 A, V_I = −7 V to −20 V, P ≤ 15 W	0°C to 125°C	−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V	25°C		12.5	50	mV
	V_I = −8 V to −12 V			4	15	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7 V to −25 V	0°C to 125°C		0.15	0.5	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

uA7952C electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7952C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−5	−5.2	−5.4	V
	I_O = 5 mA to 1 A, V_I = −7.2 V to −20 V, P ≤ 15 W	0°C to 125°C	−4.95		−5.45	
Input regulation	V_I = −7.2 V to −25 V	25°C		12.5	100	mV
	V_I = −8.2 V to −12 V			4	50	
Ripple rejection	V_I = −8.2 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7.2 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7906C electrical characteristics at specified virtual junction temperature, V_I = −11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7906C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−5.75	−6	−6.25	V
	I_O = 5 mA to 1 A, V_I = −8 V to −21 V, P ≤ 15 W	0°C to 125°C	−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V	25°C		12.5	120	mV
	V_I = −9 V to −13 V			4	60	
Ripple rejection	V_I = −9 V to −19 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	120	mV
	I_O = 250 mA to 750 mA			5	60	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		150		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −8 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

uA7908C electrical characteristics at specified virtual junction temperature, V_I = −14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7908C			UNIT
			MIN	TYP	MAX	
Output voltage ‡		25°C	−7.7	−8	−8.3	V
	I_O = 5 mA to 1 A, V_I = −10.5 V to −23 V, P ≤ 15 W	0°C to 125°C	−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V	25°C		12.5	160	mV
	V_I = −11 V to −17 V			4	80	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	160	mV
	I_O = 250 mA to 750 mA			5	80	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		200		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −10.5 V to −25 V	0°C to 125°C		0.15	1	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7912C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7912C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−11.5	−12	−12.5	V
	I_O = 5 mA to 1 A, V_I = −14.5 V to −27 V, P ≤ 15 W	0°C to 125°C	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V	25°C		5	80	mV
	V_I = −16 V to −22 V			3	30	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		300		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −14.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

uA7915C electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7915C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−14.4	−15	−15.6	V
	I_O = 5 mA to 1 A, V_I = −17.5 V to −30 V, P ≤ 15 W	0°C to 125°C	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C		5	100	mV
	V_I = −20 V to −26 V			3	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		375		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −17.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7918C electrical characteristics at specified virtual junction temperature, V_I = −27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7918C			UNIT
			MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 1 A, V_I = −21 V to −33 V, P ≤ 15 W	25°C	−17.3	−18	−18.7	V
		0°C to 125°C	−17.1		−18.9	
Input regulation	V_I = −21 V to −33 V	25°C		5	360	mV
	V_I = −24 V to −30 V			3	180	
Ripple rejection	V_I = −22 V to −32 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		30	360	mV
	I_O = 250 mA to 750 mA			10	180	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		450		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −21 V to −33 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

uA7924C electrical characteristics at specified virtual junction temperature, V_I = −33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA7924C			UNIT
			MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 1 A, V_I = −27 V to −38 V, P ≤ 15 W	25°C	−23	−24	−25	V
		0°C to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V	25°C		5	480	mV
	V_I = −30 V to −36 V			3	240	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		85	480	mV
	I_O = 250 mA to 750 mA			25	240	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		600		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −27 V to −38 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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D2216, JUNE 1976—REVISED APRIL 1988

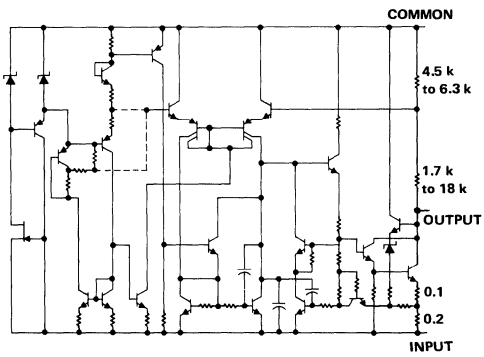
- **3-Terminal Regulators**
- **Output Current Up to 500 mA**
- **No External Components**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA79M00 Series**

NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
−5 V	uA79M05M	uA79M05C
−6 V	uA79M06M	uA79M06C
−8 V	uA79M08M	uA79M08C
−12 V	uA79M12M	uA79M12C
−15 V	uA79M15M	uA79M15C
−20 V		uA79M20C
−24 V		uA79M24C
PACKAGE	JG	KC

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA78M00 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

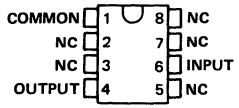


Resistor values shown are nominal and in ohms.

terminal assignments

uA79M_M. . .JG PACKAGE

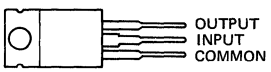
(TOP VIEW)



NC—No internal connection

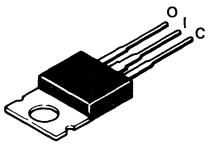
uA79M_C. . .KC PACKAGE

(TOP VIEW)



THE INPUT TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING BASE

TO-220AB



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absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA79M05M THRU uA79M15M	uA79M05C THRU uA79M24C	UNIT
Input voltage	uA79M20, uA79M24		−40	V
	All others	−35	−35	
Continuous total dissipation (see Note 1)		See Dissipation Rating Tables 1 and 2		
Operating free-air, case or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	KC package		260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1—FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
JG	1050 mW	8.4 mW/°C	672 mW
KC	2000 mW	16 mW/°C	1280 mW

DISSIPATION RATING TABLE 2—CASE TEMPERATURE

PACKAGE	$T_C \leq 50°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 50°C$	$T_C = 125°C$ POWER RATING
KC	20 W	200 mW/°C	5 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA79M05M, uA79M05C	−7	−25	V
	uA79M06M, uA79M06C	−8	−25	
	uA79M08M, uA79M08C	−10.5	−25	
	uA79M12M, uA79M12C	−14.5	30	
	uA79M15M, uA79M15C	−17.5	−30	
	uA79M20C	−23	−35	
	uA79M24C	−27	−38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J	uA79M05M thru uA79M15M	−55	150	°C
	uA79M05C thru uA79M24C	0	125	

uA79M05M, uA79M05C electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M05M			uA79M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−4.8	−5	−5.2	−4.8	−5	−5.2	V
	I_O = 5 mA to 350 mA, V_I = −7 V to −25 V		−55°C to 150°C	−4.75		−5.25				
			0°C to 125°C				−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V		25°C		7	50		7	50	mV
	V_I = −8 V to −18 V				3	30		3	30	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	100		75	100	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C			−1.5				mV/°C
			0°C to 125°C					−0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		125	400		125		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −8 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current			25°C	0.5	0.65	1.4		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M06M, uA79M06C electrical characteristics at specified virtual junction temperature, V_I = −11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M06M			uA79M06C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−5.75	−6	−6.25	−5.75	−6	−6.25	V
	I_O = 5 mA to 350 mA, V_I = −8 V to −25 V		−55°C to 150°C	−5.7		−6.3				
			0°C to 125°C				−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V		25°C		7	60		7	60	mV
	V_I = −9 V to −19 V				3	40		3	40	
Ripple rejection	V_I = −9 V to −19 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		80	120		80	120	mV
	I_O = 5 mA to 350 mA				55			55		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C			−1.5				mV/°C
			0°C to 125°C					−0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		150	480		150		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −9 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current			25°C	0.5	0.65	1.4		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M08M, uA79M08C electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M08M			uA79M08C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−7.7	−8	−8.3	−7.7	−8	−8.3	V
	I_O = 5 mA to 350 mA, V_I = −10.5 V to −25 V		−55°C to 150°C	−7.6		−8.4				
			0°C to 125°C				−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V		25°C		8	80		8	80	mV
	V_I = −11 V to −21 V				4	50		4	50	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120 Hz	V = 100 mA	155°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA		25°C		90	160		90	160	mV
	I_O = 5 mA to 350 mA				60			60		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C			−2.4				mV/°C
			0°C to 125°C					−0.6		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		200	640		200		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −10.5 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current			25°C	0.5	0.65	1.4		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M12M, uA79M12C electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M12M			uA79M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−11.5	−12	−12.5	−11.5	−12	−12.5	V
	I_O = 5 mA to 350 mA, V_I = −14.5 V to −30 V		−55°C to 150°C	−11.4		−12.6				
			0°C to 125°C				−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V		25°C		9	80		9	80	mV
	V_I = −15 V to −25 V				5	50		5	50	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C			−3.6				mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		300	960		300		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −14.5 V to −30 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current			25°C	0.5	0.65	1.4		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M15M, uA79M15C electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M15M			uA79M15C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−14.4	−15	−15.6	−14.4	−15	−15.6	V
	I_O = 5 mA to 350 mA, V_I = −17.5 V to −30 V		−55°C to 150°C	−14.25		−15.75				
			0°C to 125°C				−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V		25°C		9	80		9	80	mV
	V_I = −18 V to −28 V				7	50		7	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C			−4.5				mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		375	1200		375		μV
Dropout voltage			25°C		1.1	2.3		1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −17.5 V to −30 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short-circuit output current	V_I = −30 V		25°C			600		140		mA
Peak output current			25°C	0.5	0.65			0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M20C electrical characteristics at specified virtual junction temperature, V_I = −29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M20C			UNIT
				MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 350 mA, V_I = −23 V to −35 V		25°C	−19.2	−20	−20.8	V
			0 to 125°C	−19		−21	
Input regulation	V_I = −23 V to −35 V		25°C		12	80	mV
	V_I = −24 V to −34 V				10	70	
Ripple rejection	V_I = −24 V to −34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		500		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −23 V to −35 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA79M24C electrical characteristics at specified virtual junction temperature, V_I = −33 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M24C			UNIT
				MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 350 mA, V_I = −27 V to −38 V		25°C	−23	−24	−25	V
			0 to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V		25°C		12	80	mV
	V_I = −28 V to −38 V				12	70	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		600		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −27 V to −38 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

†Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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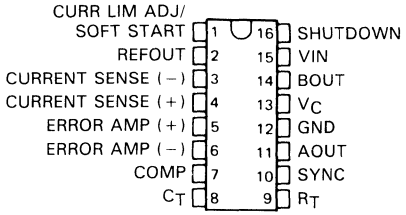
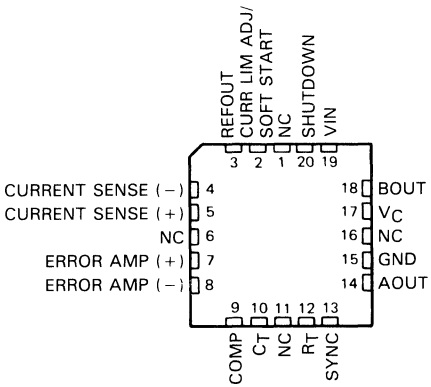
- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-Pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current-Sense Amplifier with Wide Common-Mode Range
- Double-Pulse Suppression
- 200-mA Totem-Pole Outputs
- ±1% Bandgap Reference
- Under-Voltage Lockout
- Soft-Start Capability
- Shutdown Terminal
- 500-kHz Operation

UC1846, UC1847 . . . J PACKAGE
UC2846, UC2847, UC3846, UC3847 . . . N PACKAGE
(TOP VIEW)



UC2846, UC2847, UC3846, UC3847 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This family of control ICs provides all of the necessary features to implement fixed frequency, current-mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current-limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limiting in addition to soft-start capability. A shutdown function is also available that can initiate either a complete shutdown with automatic restart, or latch the supply off.

Other features include fully-latched operation, double-pulse suppression, deadtime adjustment capability, and a ±1% trimmed bandgap reference.

In the off state, the UC1846 outputs are low and the UC1847 outputs are high.

The UC1846 and UC1847 are characterized for operation over the full military temperature range of −55°C to 125°C, the UC2846 and UC2847 are characterized for operation from −25°C to 85°C, and the UC3846 and UC3847 are characterized for operation from 0°C to 70°C.

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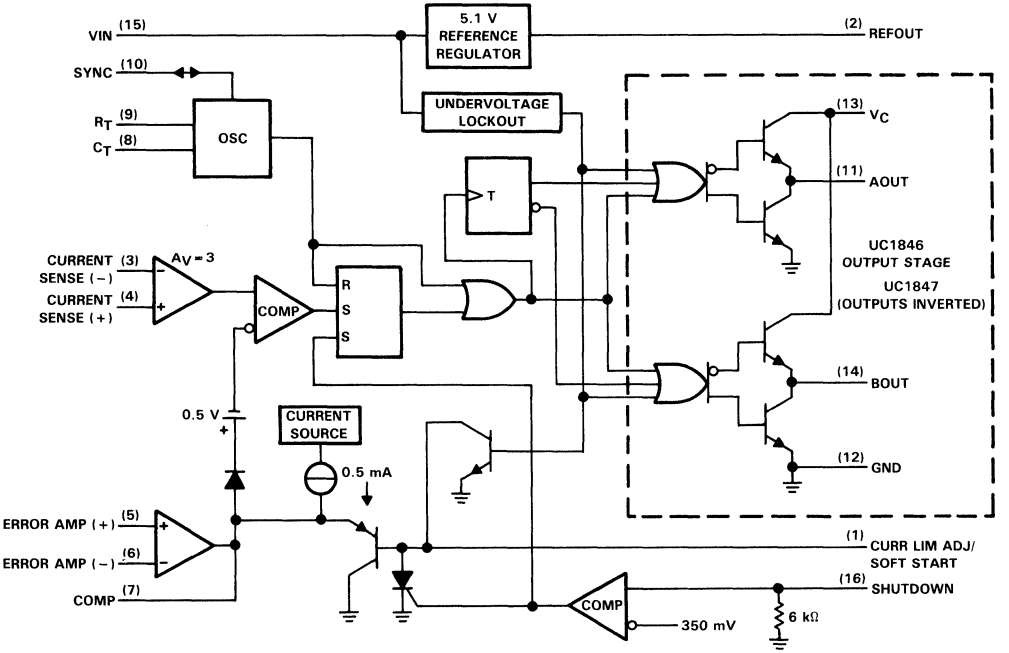
functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{IN} (see Note 1) . . . . . 40 V
Collector supply voltage, V_C . . . . . 40 V
Output current, source or sink, I_O . . . . . 500 mA
Analog input voltage (CURRENT SENSE (−), CURRENT SENSE (+), ERROR AMP (+), ERROR AMP (−), or SHUTDOWN) . . . . . −0.3 V to V_{IN}
Reference output current . . . . . −30 mA
SYNC output current . . . . . −5 mA
Error amplifier output current . . . . . −5 mA
Soft-start sink current . . . . . 50 mA
Oscillator charging current . . . . . 5 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: UC1846, UC1847 . . . . . −55°C to 125°C
UC2846, UC2847 . . . . . −25°C to 85°C
UC3846, UC3847 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW	728 mW	280 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	

recommended operating conditions

	UC1846, UC1847		UC2846, UC2847		UC3846, UC3847		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
High-level input voltage, V_{IH} (Oscillator Section)	3.9		3.9		3.9		V
Low-level input voltage, V_{IL} (Oscillator Section)		2.5		2.5		2.5	V
Supply voltage operating range, V_{IN}	8	40	8	40	8	40	V
Operating free-air temperature, T_A	−55	125	−25	85	0	70	°C

electrical characteristics over operating free-air temperature range, V_{IN} = 15 V, R_T = 10 kΩ, C_T = 4.7 nF (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output voltage	I_O = 1 mA, T_A = 25°C	5.05	5.1	5.1	5	5.1	5.2	V
	Line regulation	V_{IN}(pin 15) = 8 V to 40 V		5	20		5	20	mV
	Load regulation	I_{IL} = 1 mA to 10 mA		3	15		3	15	mV
α_{VO}	Temperature coefficient of output voltage			0.4			0.4		mV/°C
	Total output variation		5		5.2	4.95		5.25	V
	Output noise voltage	f = 1 kHz to 10 kHz, T_A = 25°C			100			100	μV
	Output voltage long-term drift	t = 1000 hours, T_A = 25°C		5			5		mV
I_{OS}	Short-circuit output current (REFOUT)	V_{REF} = 0	−10	−45		−10	−45		mA

oscillator section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Initial accuracy	T_A = 25°C	39	43	47	39	43	47	kHz
	Frequency change with voltage	V_{IN}(pin 15) = 8 V to 40 V		−1%	±2%		−1%	±2%	
	Frequency change with temperature			−1%			−1%		
V_T	Threshold voltage (SYNC)		2.5		3.9	2.5		3.9	V
V_{OH}	High-level output voltage (SYNC)		3.9			3.9			V
V_{OL}	Low-level output voltage (SYNC)				2.5			2.5	V
I_I	Input current (SYNC)	Sync voltage = 5.25 V, C_T at 0 V		1.3	1.5		1.3	1.5	mA

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electrical characteristics over operating free-air temperature range, V_{IN} = 15 V, R_T = 10 kΩ, C_T = 4.7 nF (unless otherwise noted) (continued)

error amplifier section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			0.5	5		0.5	5	mV
I_{IO}	Input offset current			40	250		40	250	nA
I_{IB}	Input bias current			−0.6	−1		−0.6	−1	μA
V_{OH}	High-level output voltage	$R_{L(COMP)}$ = 15 kΩ	4.3	4.6		4.3	4.6		V
I_{OH}	High-level output current	V_{ID} = 15 mV to 5 V, COMP at 2.5 V	−0.4	−0.5		−0.4	−0.5		mA
V_{OL}	Low-level output voltage	$R_{L(COMP)}$ = 15 kΩ		0.7	1		0.7	1	V
I_{OL}	Low-level output current	V_{ID} = −15 mV to −5 V, COMP at 1.2 V	2	6		2	6		mA
V_{ICR}	Common-mode input voltage range	V_{IN} = 8 V to 40 V	0 to V_{IN}−2			0 to V_{IN}−2			V
A_{VD}	Open-loop voltage amplification	ΔV_O = 1.2 V to 3 V, V_{IC} = 2 V	80	105		80	105		dB
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 38 V, V_{IN} = 40 V	75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio	V_{IN} = 8 V to 40 V	80	105		80	105		dB

current-sense amplifier section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	CURR LIM ADJ/SOFT START at 0.5 V, COMP open, See Note 3		5	25		5	25	mV
I_{IO}	Input offset current			0.08	1		0.08	1	μA
I_{IB}	Input bias current			−2.5	−10		−2.5	−10	μA
A_V	Voltage amplification	CURRENT SENSE (−) at 0 V, CURR LIM ADJ/SOFT START open, See Notes 2 and 3	2.5	2.75	3	2.5	2.75	3	V
V_{ICR}	Common-mode input voltage range		0 to V_{IN}−3			0 to V_{IN}−3			V
	Maximum usable differential input signal	CURR LIM ADJ/SOFT START open, $R_{L(COMP)}$ = 15 kΩ, See Note 2	1.1	1.3		1.1	1.2		V
CMRR	Common-mode rejection ratio	V_{IC} = 1 V to 12 V	60	83		60	83		dB
k_{SVR}	Supply-voltage rejection ratio	V_{IN} = 8 V to 40 V	60	84		60	84		dB
t_d	Input-to-output delay time	T_A = 25°C		200	600		200	600	ns

NOTES: 2. This parameter is measured at the trip point of the latch with ERROR AMP (+) at V_{REF}, ERROR AMP (−) at 0 V.

3. Amplifier gain is defined as:

$$AV = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$$

Where:

$\Delta V_{PIN\ 4}$ = 0 V to 1.0 V

electrical characteristics over operating free-air temperature range, V_{IN} = 15 V, R_T = 10 kΩ, C_T = 4.7 nF (unless otherwise noted) (continued)

current limit adjustment section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	CURRENT SENSE (−) at 0 V, CURRENT SENSE (+) at 0 V, COMP open, See Note 3	0.45	0.5	0.55	0.45	0.5	0.55	V
I_{IB}	Input bias current	ERROR AMP (+) at V_{REF}, ERROR AMP (−) at 0 V		−10	−30		−10	−30	μA

shutdown terminal section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Differential-input threshold voltage		250	350	400	250	350	400	mV
V_I	Input voltage range		0 to V_{IN}			0 to V_{IN}			V
	Minimum latching current (CURR LIM ADJ/SOFT START)	See Note 4	0.8	1.5	3	0.8	1.5	3	mA
	Output delay	T_A = 25°C		300	600		300	600	ns

output section

PARAMETER		TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CE}$	Collector-emitter breakdown voltage		40			40			V
I_{CEX}	Collector-emitter off-state current	V_{CE} = 40 V, See Note 5			200			200	μA
V_{OH}	High-level output voltage (AOUT and BOUT)	I_{OH} = −20 mA	13	13.5		13	13.5		V
		I_{OH} = −100 mA	12	13.5		12	13.5		
V_{OL}	Low-level output voltage (AOUT and BOUT)	I_{OL} = 20 mA		0.1	0.4		0.1	0.4	V
		I_{OL} = 100 mA		0.4	2.1		0.4	2.1	
t_r	Rise time (AOUT and BOUT)	C_L = 1 nF, T_A = 25°C		50	300		50	300	ns
t_f	Fall time (AOUT and BOUT)			50	300		50	300	ns

under-voltage lockout section

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Startup threshold			7.7	8		7.7	8	V
Threshold hysteresis			0.75			0.75		V

NOTES: 3. This parameter is measured at the trip point of the latch with ERROR AMP (+) at V_{REF} and ERROR AMP (−) at 0 V.
4. This is the lowest current into Pin 1 that will latch the circuit in the shutdown state.
5. This applies for UC1846, UC2846, and UC3846 only (due to polarity of outputs).

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electrical characteristics over operating free-air temperature range, V_{IN} = 15 V, R_T = 10 kΩ, C_T = 4.7 nF (unless otherwise noted) (continued)

total device

PARAMETER	TEST CONDITIONS	UC1846, UC1847 UC2846, UC2847			UC3846, UC3847			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply current			17	21		17	21	mA

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER AMPLIFICATION AND PHASE
vs
FREQUENCY

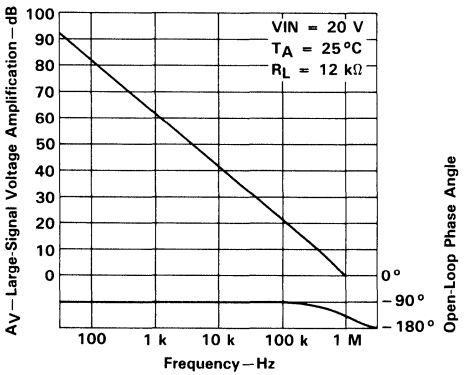


FIGURE 1

ERROR AMPLIFIER LARGE-SIGNAL DC AMPLIFICATION
vs
LOAD RESISTANCE

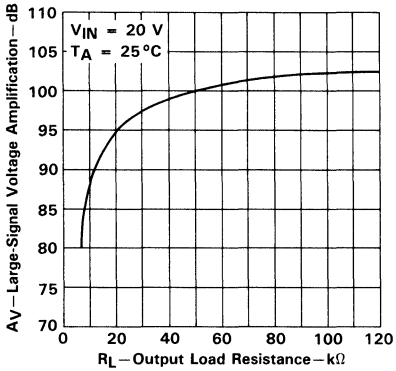
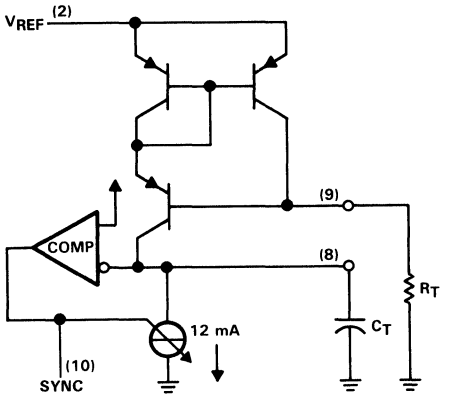
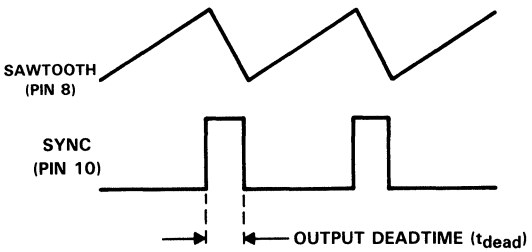


FIGURE 2

TYPICAL APPLICATION DATA



OSCILLATOR CIRCUIT



OSCILLATOR WAVEFORMS

NOTE: Oscillator frequency is approximated by the formula: $f_T \approx \frac{2.2}{R_T C_T}$

Output deadtime is determined by the size of the external capacitor, C_T, according to the following formula:

$$t_{dead} = 145\ C_T \left(\frac{12}{12 - \frac{3.6}{R_T\ (k\Omega)}} \right)$$

For large values of R_T, $t_{dead} \approx 145\ C_T$

FIGURE 3. OSCILLATOR CIRCUIT

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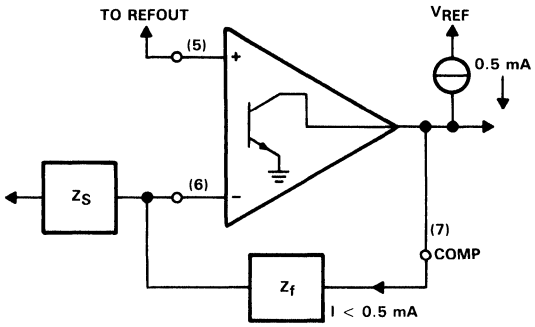
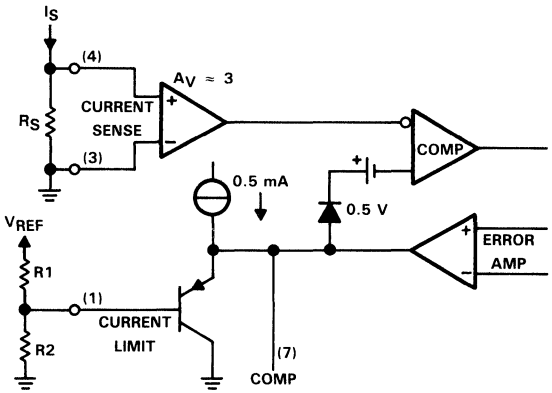
TYPICAL APPLICATION DATA



NOTE: Error Amplifier can source up to 0.5 mA.

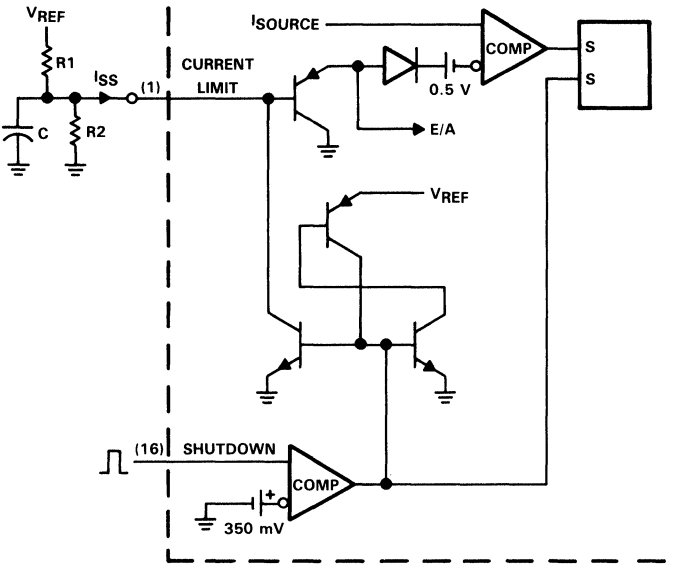
FIGURE 4. ERROR AMPLIFIER OUTPUT CONFIGURATION



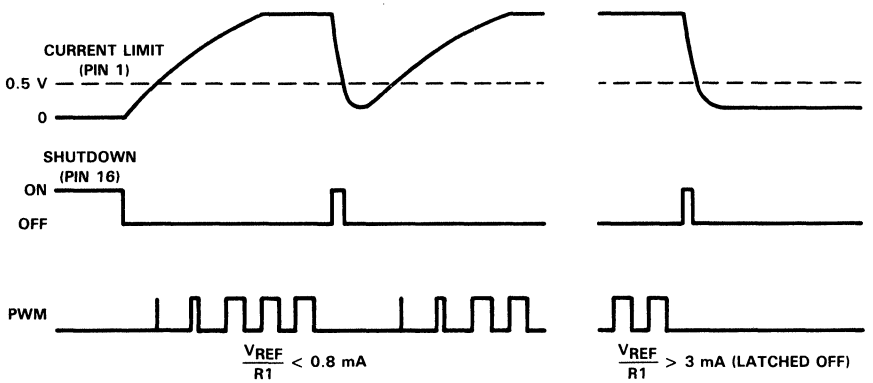
NOTE: Peak Current (I_S) is determined by the formula: $I_S = \dfrac{\frac{R2\ V_{REF}}{R1 + R2} - 0.5\ V}{3R_S}$

FIGURE 5. PULSE-BY-PULSE CURRENT LIMITING

TYPICAL APPLICATION DATA



SOFT START AND SHUTDOWN/RESTART CIRCUIT



NOTE: If $\frac{V_{REF}}{R1} < 0.8$ mA, the shutdown latch will commutate when $I_{SS} = 0.8$ mA and a restart cycle will be initiated.

SHUTDOWN WITH AUTO-RESTART

NOTE: If $\frac{V_{REF}}{R1} > 3$ mA, the device will latch off until power is cycled.

SHUTDOWN WITHOUT AUTO-RESTART (LATCHED)

FIGURE 6. SOFT START AND SHUTDOWN/RESTART FUNCTIONS

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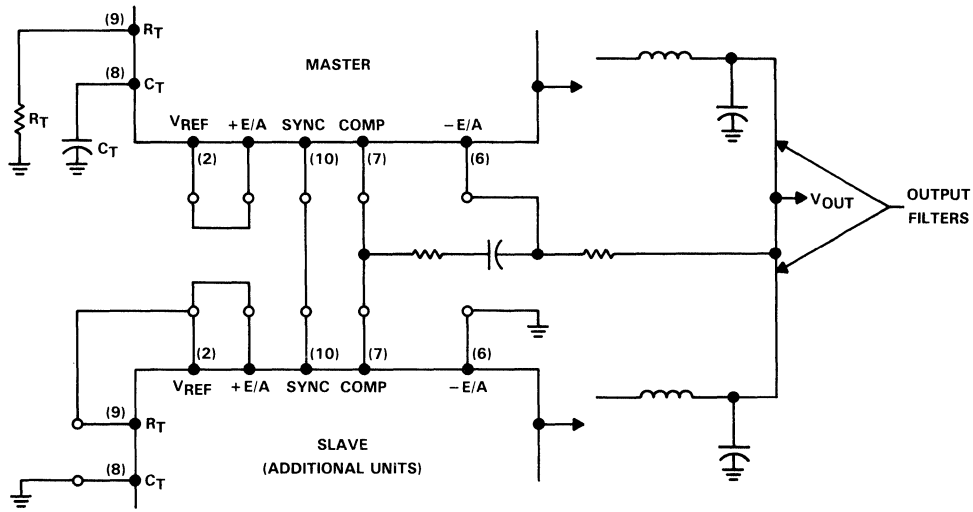
TYPICAL APPLICATION DATA



NOTE: Slaving allows parallel operation of two or more units with equal current sharing.

FIGURE 7. PARALLEL OPERATION

General Information 1

Data Sheets 2

Product Previews 3

Design Considerations 4

Mechanical Data 5

D3219, JULY 1988—REVISED JANUARY 1989

- **Two Regulated Outputs**
  +12 V at 3 A
  +5 V at 75 mA
- **2% Output Voltage Tolerance**
- **60-dB Ripple Rejection**
- **0.7% Output Regulation**
- **100% Thermal-Limit Burn-In**
- **TTL and CMOS Compatible Logic Control**

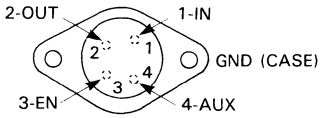
description

The LT1036 contains two positive regulators in the same package. The 12-V main regulator supplies current up to 3 A and the auxiliary 5-V regulator supplies up to 75 mA. The 12-V main regulator has an additional feature that allows a logic signal to control its operation. When the enable input is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0 V. The auxiliary regulator at this time is unaffected and continues to provide a 5-V output.

The 12-V main output has current and power limiting combined with thermal shutdown to make it very reliable. The 5-V auxiliary output is not affected by the thermal shutdown circuits or the state of the 12-V main output. This allows it to be used as a back-up in case of overloads on the main supply. The logic enable input of the LT1036 has a 1.6-V threshold and can be driven by most logic families including TTL and CMOS.

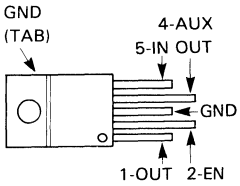
Typical applications include power supply sequencing, remote on/off power control, selective system power during emergency power operation, and power supply with back-up.

KJ PACKAGE
(TOP VIEW)



4 LEAD TO-3

KV PACKAGE
(TOP VIEW)



5 LEAD TO-220

AVAILABLE OPTIONS

T_J	PACKAGE	
	4 LEAD TO-3 KJ	5 LEAD TO-220 KV
0°C to 125°C	LT1036CKJ	LT1036CKV
−55°C to 150°C	LT1036MKJ	

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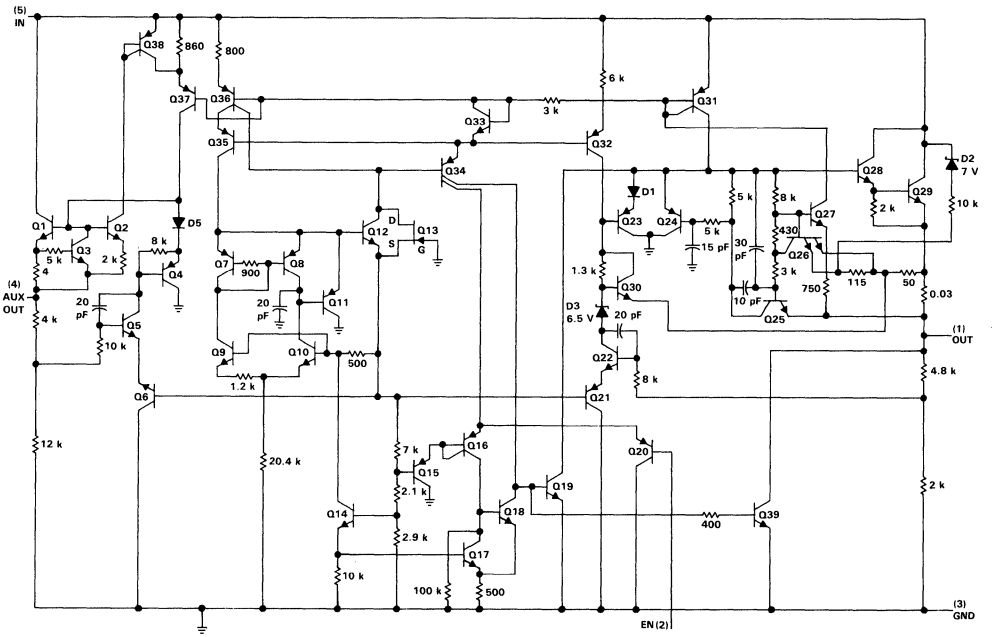
schematic diagram



All resistor values are nominal and in ohms.

absolute maximum ratings over operating virtual-junction temperature range (unless otherwise noted)

Input voltage, V_I . . . . . 30 V
Enable voltage, V_{EN} . . . . . 30 V
Continuous power dissipation, P_D . . . . . 24 W
Power dissipation under fault conditions . . . . . Internally self-limited
Operating virtual junction temperature range: LT1036M . . . . . −55°C to 150°C
LT1036C . . . . . 0°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: KJ package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: KV package . . . . . 260°C

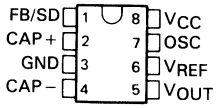
recommended operating conditions

		MIN	MAX	UNIT
Output current, I_O			3	A
Operating junction temperature, T_J	LT1036M	−55	150	°C
	LT1036C	0	125	°C

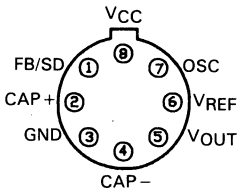
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin Compatible with the LTC1044/7660**

JG AND P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE		
	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	LT1054CJG	LT1054CL	LT1054CP
−55°C to 125°C	LT1054MJG	LT1054ML	N/A

description

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100 mA output current is typically 1.1 V. This holds true over the full supply voltage range of 3.5 V to 15 V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shut down is less than 100 μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such as the LTC1044/7660.

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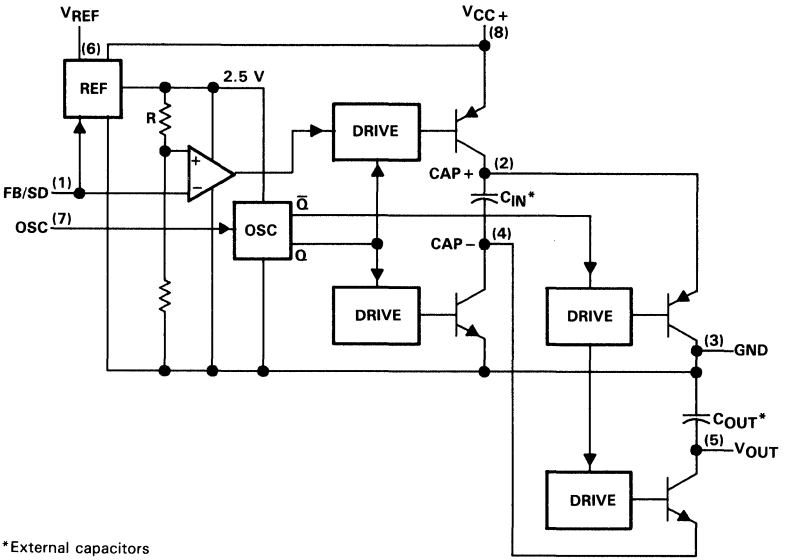
functional block diagram



*External capacitors

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 16 V
Input voltage, FB/SD terminal . . . . . 0 V to $V_{CC}+$
Input voltage, OSC terminal . . . . . 0 V to V_{ref}
Junction temperature (see Note 2): LT1054C . . . . . 125°C
LT1054M . . . . . 150°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package . . . . . 300°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. The absolute maximum supply voltage rating of 16 V is for unregulated circuits. For regulation mode circuits with $V_O \leq 15$ V, this rating may be increased to 20 V.
2. The devices are functional up to the absolute maximum junction temperature.

TEXAS INSTRUMENTS
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recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.5	15	V
T_A	Operating free-air temperature	LT1054C	0	70	°C
		LT1054M	−55	125	

electrical characteristics

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Regulated output voltage, V_O	V_{CC} = 7 V, T_J = 25°C, See Note 3		25°C	−4.7	−5	−5.2	V
Input regulation	V_{CC} = 7 V to 12 V, See Note 3		Full range		5	25	mV
Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 3		Full range		10	50	mV
Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = μF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
		I_O = 100 mA	Full range		1.1	1.6	
Output resistance	ΔI_O = 10 mA to 100 mA, See Note 5		Full range		10	15	Ω
Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
Reference voltage, V_{ref}	I_{ref} = 60 μA, T_J = 25°C		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
Maximum switch current			25°C		300		mA
Supply current, I_{CC}	I_O = 0	V_I = 3.5 V	Full range		2.5	3.5	mA
		V_I = 15 V	Full range		3	4.5	
Supply current in shutdown	$V_{FB/SD}$ = 0 V		Full range		100	150	μV

†Full range is −55°C to 125°C for the LT1054M and 0°C to 70°C for the LT1054C. For the LT1054C, the specifications apply up to a junction temperature of 100°C.

NOTES: 3. All regulation specifications are for a device connected as a positive to negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, C1 = 10 μF (tantalum), and C_O = 100 μF (tantalum).

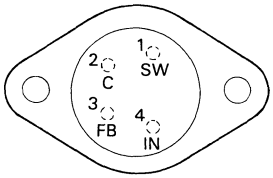
4. For voltage-loss tests, the device is connected as a voltage inverter, with pins 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations.

5. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents of less than 10 mA due to the characteristics of the switch transistors.

D3222, OCTOBER 1988

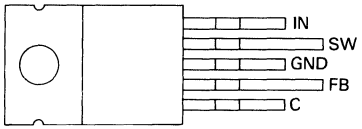
- **Wide Supply Voltage Range:**
  LT1070HV . . . 3 V to 60 V
  LT1070 . . . 3 V to 40 V
- **Low Quiescent Current . . . 6 mA Typ**
- **Internal 5-A Switch**
- **Very Few External Parts Required**
- **Self-Protected Against Overloads**
- **Operates in Nearly All Switching Topologies**
- **Low Shutdown-Mode Supply Current**
- **Fully Floating Outputs in Flyback-Regulated Mode**
- **Available in Standard KV and KJ Packages**
- **Can be Externally Synchronized**

KJ PACKAGE
(TOP VIEW)



CASE IS GND

KV PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_J	MAX INPUT VOLTAGE	KJ PACKAGE	KV PACKAGE
0°C to 100°C	60 V	LT1070HVCKJ	LT1070HVCKV
	40 V	LT1070CKJ	LT1070CKV
−55°C to 150°C	60 V	LT1070HVMKJ	
	40 V	LT1070MKJ	

description

The LT1070 is a monolithic, high-power switching regulator. It can be operated in all standard switching configurations including: buck, boost, flyback, forward, inverting, and Ćuk†. A high-current, high-efficiency switch is included in the package along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070 to be built in a standard 5-pin KV package and the 4-pin case-ground KJ power package. This makes it extremely easy to use and provides bust-proof operation similar to that obtained with 3-pin linear regulators.

The LT1070 operates with supply voltages from 3 V to 40 V. The LT1070HV, a high-voltage version of the LT1070, operates with supply voltages from 3 V to 60 V. These devices draw only 6-mA quiescent current, deliver load power up to 100 W with no external power devices, and by utilizing current-mode switching techniques, they provide excellent ac and dc input and output regulation.

The LT1070 is much easier to use than the low-power control chips that are presently available and has many unique features that are not found on these chips. It uses an adaptive saturation-preventing switch drive to allow very-wide-ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070, without the need for optocouplers or extra transformer windings.

†Boost-buck-derived regulator circuit patented by Slobodan Ćuk.

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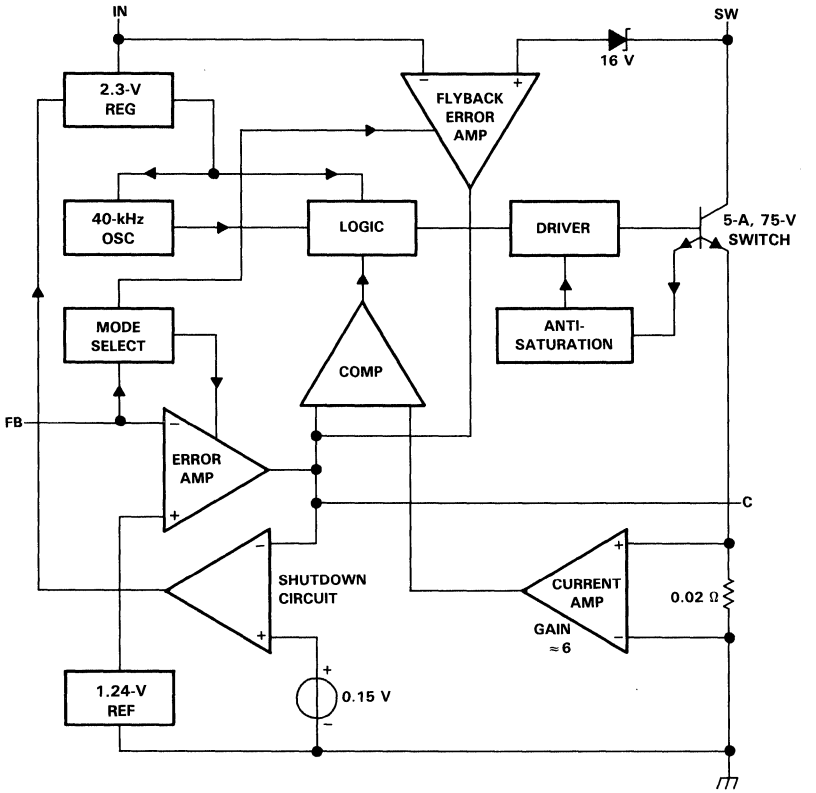
functional block diagram



absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Input voltage, V_I (see Note 1): LT1070 . . . . . 40 V
LT1070HV . . . . . 60 V
Switch output voltage: LT1070 . . . . . 65 V
LT1070HV . . . . . 75 V
Feedback pin voltage, V_{FB} (transient, 1 ms) . . . . . ±15 V
Operating virtual junction temperature range:
LT1070C, LT1070HVC (normal operation) . . . . . 0°C to 100°C
LT1070C, LT1070HVC (short-circuit operation) . . . . . 0°C to 125°C
LT1070M, LT1070HVM . . . . . −55°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds: . . . . . 300°C

NOTE 1: Minimum switch-on time for the LT1070 in current limit is ≈1 μs. This limits the maximum input voltage during short-circuit conditions, in the buck and inverting modes only, to ≈35 V. Normal (unshorted) conditions are not affected. If the LT1070 is being operated in the buck or inverting mode at high input voltages and short-circuit conditions are expected, a resistor must be placed in series with the inductor.

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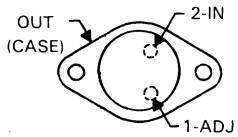
D3118, JULY 1988—REVISED JANUARY 1989

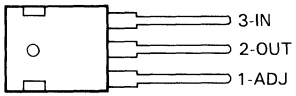
- **Adjustable Output . . . 1 V to 35 V**
- **5-A Output Capability**
- **Dropout Voltage . . . 5 V Max**
- **Input Regulation . . . 0.015% Typ**
- **Output Regulation . . . 0.01% Typ**
- **100% Thermal Limit Burn-In**

KA PACKAGE
(TOP VIEW)



TO-3

KK PACKAGE
(TOP VIEW)



description

The LT1084 is a 3-terminal adjustable positive regulator that operates with higher efficiency than currently available devices with output loads up to 5 A. Internal circuitry is designed to operate with a small input-to-output differential voltage of 1.3 V (typical) and all dropout voltages are specified as a function of output current. Dropout voltage reaches a maximum of 1.5 V at maximum output currents. On-chip circuitry holds the reference voltage constant to within 1%. Current limiting is used to minimize the stress on both the regulator and power source circuits under overload conditions.

The LT1084 is pin compatible with older 3-terminal regulators. A 10-μF output capacitor is required, as in most regulator designs. In P-N-P regulators, up to 10% of the output current is lost as bias (quiescent) current, but LT1084 bias current flows into the load, which improves power efficiency.

Typical applications include high-efficiency linear regulators, post regulators for switching power supplies, constant-current regulators, and battery chargers.

AVAILABLE OPTIONS

T_J	PACKAGE	
	METAL TO-3 KA	PLASTIC KK
0°C to 125°C	LT1084CKA	LT1084CKK
−55°C to 150°C	LT1084MKA	

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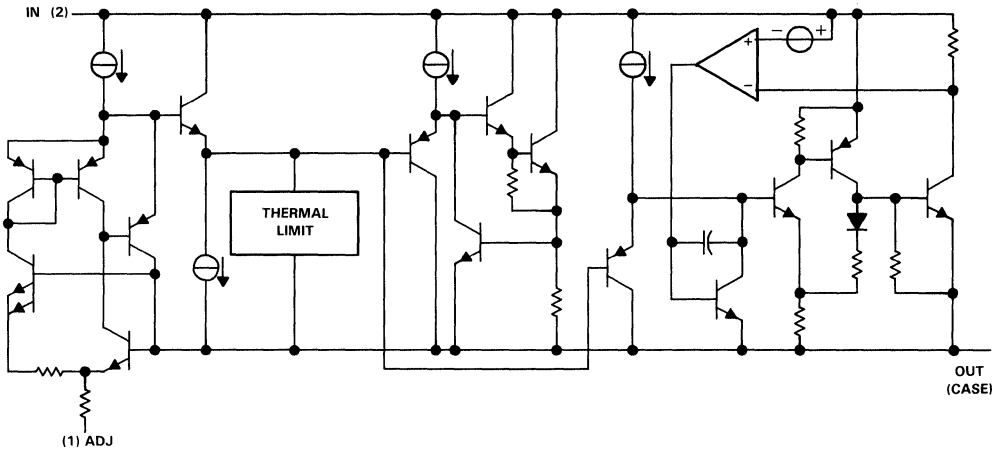
functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage: LT1084M . . . . . 35 V
LT1084C . . . . . 30 V
Power dissipation . . . . . Internally self-limited
Operating virtual-junction temperature range: LT1084M Control section . . . . . −55°C to 150°C
LT1084M Power transistor . . . . . −55°C to 200°C
LT1084C Control section . . . . . 0°C to 125°C
LT1084C Power transistor . . . . . 0°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: KA package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: KK package . . . . . 260°C

recommended operating conditions

		MIN	MAX	UNIT
Output current, I_O			5	A
Operating virtual-junction temperature, T_J	LT1084M Control section	0	125	°C
	LT1084M Power transistor	0	150	
	LT1084C Control section	0	125	
	LT1084C Power transistor	0	150	

TEXAS INSTRUMENTS
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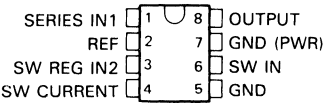
D2762, JANUARY 1984—REVISED FEBRUARY 1989

- **Internal Series-Pass and Step-Up Switching Regulator**
- **Output Adjustable from 2.9 V to 30 V**
- **1-V to 10-V Input for Switching Regulator**
- **4.5-V to 32-V Input for Series Regulator**
- **Externally Controlled Switching Current**
- **No External Rectifier Required**

D OR P PACKAGE
(TOP VIEW)



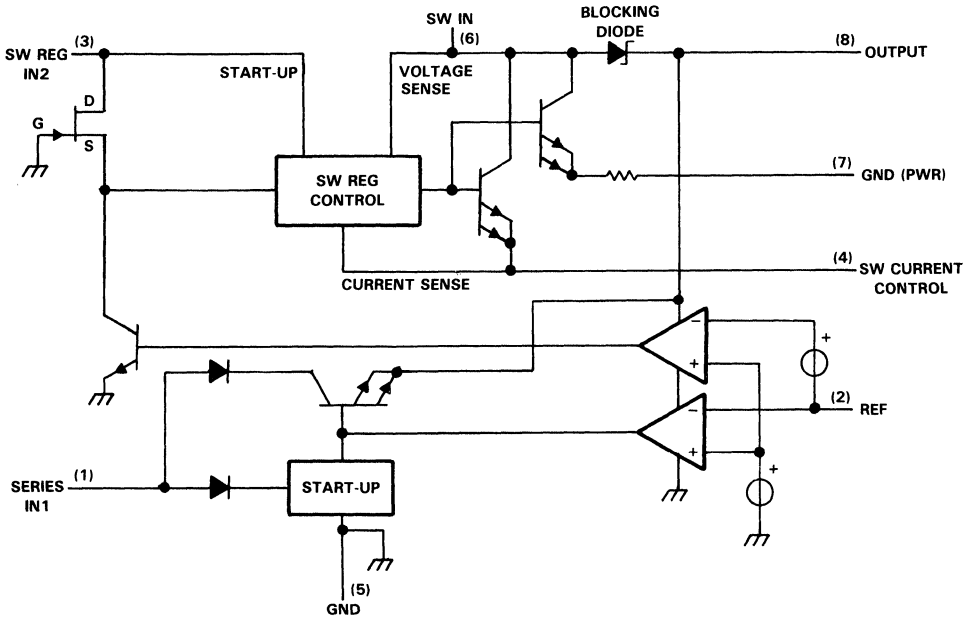
description

The TL499A is a monolithic integrated circuit designed to provide a wide range of adjustable regulated supply voltages. The regulated output voltage is adjustable from 2.9 V to 30 V by adjusting two external resistors. When the TL499A is ac coupled to line power through a step-down transformer, it operates as a series dc voltage regulator to maintain the regulated output voltage. With the addition of a backup battery of from 1.1 V to 10 V, an inductor, a filter capacitor, and two resistors, the TL499A will operate as a step-up switching regulator during an ac-line failure.

The adjustable regulated output voltage makes the TL499A useful for a wide range of applications. Providing backup power during an ac-line failure makes the TL499A extremely useful as backup power in microprocessor memory applications.

The TL499A is characterized for operation from −20°C to 85°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Output voltage, V_O . . . . . 35 V
Input voltage, series regulator, V_{I1} . . . . . 35 V
Input voltage, switching regulator, V_{I2} . . . . . 10 V
Diode (blocking) reverse voltage . . . . . 35 V
Diode (blocking) forward current . . . . . 1 A
Power switch current (at SW IN, pin 6) . . . . . 1 A
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	825 mW	6.6 mW/°C	429 mW
P	1000 mW	8 mW/°C	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Output voltage, V_O	2.9		30	V
Input voltage, series regulator, V_{I1}	4.5		32	V
Input voltage, switching regulator, V_{I2}	1.1		10	V
Input-to-output differential voltage, switching regulator, $V_O - V_{I2}$ (see Note 2)	1.2		28.9	V
Continuous output current, I_O			100	mA
Power switch current (at SW IN, pin 6)			500	mA
Current limiting resistor, R_{CL}	150		1000	Ω
Capacitor, filter	100		470	μF
Capacitor, pass		0.1		μF
Inductor, L ($r_{in} \leq 0.1$ Ω)	50		150	μH
Operating free-air temperature, T_A	−20		85	°C

NOTE 2. When operating temperature range is $T_A \leq 70°C$, $\Delta V \geq 1.2V$. When operating temperature range is $T_A \leq 85°C$, $\Delta V \geq 1.9V$. $\Delta V = V_O - V_{I2}$.

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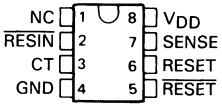
D3221, JANUARY 1989

- **Power-On and Supply Drop-Out Reset Generator**
- **Low Supply Current . . . Maximum 80 μA**
- **Reset Outputs Defined from 1-V Supply Voltage**
- **Wide Supply Voltage Range . . . 3 V to 16 V**
- **Precision Temperature-Compensated Threshold Voltage**
- **True and Complement Open-Drain or Push-Pull Outputs**
- **Externally Adjustable Pulse Duration**
- **Pin-Compatible Improved Low-Power Versions of TL7702A and TL7705A**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

description

The LinCMOS™ TLC77__ series of supply voltage supervisors (SVS) are low-power integrated circuits designed for use as reset controllers in microprocessor and logic systems. During system power-up, the SVS tests the supply voltage level via the SENSE input. If it is below the nominal value, the RESET and $\overline{\text{RESET}}$ outputs are held high and low, respectively. The reset outputs reach their active reset levels when the power supply voltage to the SVS has increased to 1 V.

To ensure a full reset period after the monitored supply voltage reaches its nominal value, the SVS delays the return of the RESET and $\overline{\text{RESET}}$ outputs to their low and high levels, respectively, by an internal time delay t_d. This time delay is determined by an external capacitor connected from the CT input to GND and is of duration $t_d = 275 \times C_T$ μs, where C_T is in nF.

If at any time the supply voltage drops below its nominal value, the reset outputs will immediately become, and remain, in the reset active state until the supply voltage has returned to its nominal value and the reset period has elapsed.

Holding the $\overline{\text{RESIN}}$ input low keeps the reset outputs in their active (reset) states. The $\overline{\text{RESIN}}$ input can be used to provide a debounced input for a reset switch or a cascade input for the wired-OR reset outputs of several SVSs in multiple supply systems.

To prevent functional failures, these devices have internal electrostatic discharge (ESD) protection circuits rated at 2 kV. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

These devices are characterized for operation from −40°C to 85°C.

DEVICE FEATURES

Threshold voltage	1.3 V	4.55 V
Open-drain outputs	TLC7701	TLC7705
Push-pull outputs	TLC7721	TLC7725

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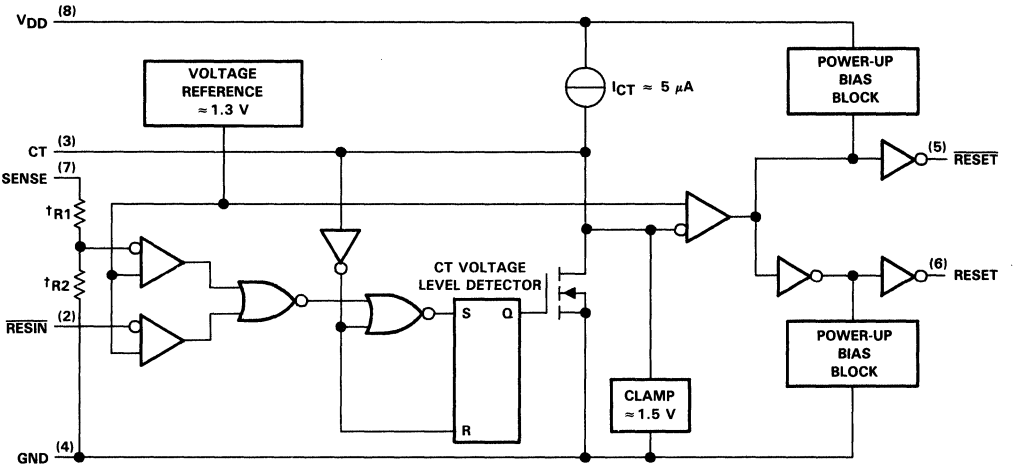
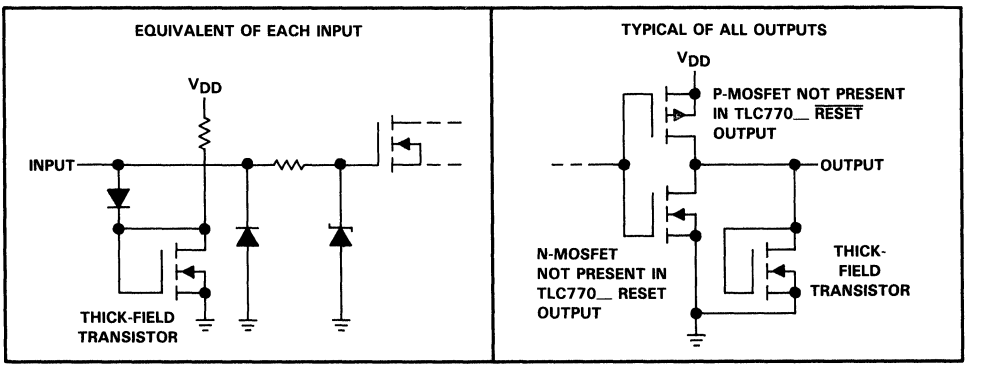
functional block diagram



†TLC7701, TLC7721: R1 = 0 Ω NOM, R2 = Open.
TLC7705, TLC7725: R1 = 1.37 MΩ NOM, R2 = 545 kΩ NOM.

schematics of inputs and outputs



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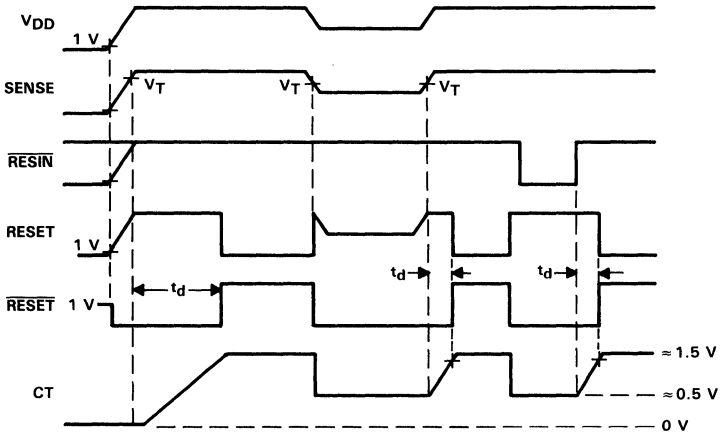
typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range at $\overline{RESIN}$ and SENSE . . . . . −0.3 V to V_{DD}
High-level output current at $\overline{RESET}$ . . . . . −5 mA
Low-level output current at $\overline{RESET}$ . . . . . 5 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°CC to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
JG	825 mW	6.6 mW/°C	429 mW
P	1000 mW	8.0 mW/°C	520 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}† (see Note 2)	3	16	V
High-level input voltage at $\overline{RESIN}$, V_{IH}‡	2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}‡		0.6	V
Input voltage at SENSE input, V_I	0	V_{DD}	V
High-level output current at RESET, I_{OH}		−2	mA
Low-level output current at $\overline{RESET}$, I_{OL}		4	mA
Operating free-air temperature range, T_A	−40	85	°C

†Outputs are in a reset state above a V_{DD} of 1 V.
‡An unused $\overline{RESIN}$ input should be tied to V_{DD}.
NOTE 2: The minimum operating supply voltage will be equal to the voltage at the SENSE input for the TLC77_5.

electrical characteristics over ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage RESET		I_{OH} = 2 mA	$V_{DD}-1.5$			V
			I_{OH} = 20 μA	$V_{DD}-0.1$			
V_{OL}	Low-level output voltage $\overline{RESET}$		I_{OH} = 4 mA			0.4	V
			I_{OH} = 20 μA			0.1	
$V_{OH(ST)}$	High-level output voltage at RESET defined at start-up		V_{DD} = 1 V to 3 V, R_L = 500 kΩ to GND§	$V_{DD}-0.1$			V
$V_{OL(ST)}$	Low-level output voltage at $\overline{RESET}$ defined at start-up		V_{DD} = 1 V to 3 V, R_L = 4.7 kΩ to V_{DD}§			0.8	V
V_T	Threshold voltage at SENSE input	TLC77_1	V_{DD} = 3 V to 16 V, T_A = 25°C	1.290	1.303	1.316	V
		TLC77_5	V_{DD} = 5 V to 16 V, T_A = 25°C	4.505	4.55	4.59	
		TLC77_1	V_{DD} = 3 V to 16 V	1.277	1.303	1.329	
		TLC77_5	V_{DD} = 5 V to 16 V	4.46	4.55	4.64	
V_{hys}	Hysteresis at SENSE input (see Note 3)	TLC77_1	V_{DD} = 3V to 16 V, T_A = 25°C		5		mV
		TLC77_5			15		
I_I	Input current at $\overline{RESIN}$		V_I = 0 to V_{DD}		0.5	2	μA
I_I	Input current at SENSE	TLC77_1	V_I = 0 to V_{DD}		0.5	2	μA
		TLC77_5	V_I = 5 V			5	
I_{OH}	High-level output current at $\overline{RESET}$	TLC77_5	V_{DD} = 16 V, V_O = 16 V, V_I = V_{DD}			1	μA
I_{OL}	Low-level output current at RESET	TLC77_5	V_{DD} = 16 V, V_O = 0, V_I = V_{DD}			−1	μA
I_{DD}	Supply current		All inputs at V_{DD}, No load		25	80	μA

switching characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
t_{w1}	Pulse duration, SENSE		V_{IH} = V_{Ttyp}×1.08, V_{IL} = V_{Ttyp}×0.92	500			ns
t_{w2}	Pulse duration, $\overline{RESIN}$		V_{IH} = 4.8 V, V_{IL} = 0.4 V	400			ns
t_d	Time delay, SENSE high to reset outputs inactive		C_T = 1 nF, T_A = 25°C, See Note 4		0.35		ns
t_{pd1}	Propagation delay, SENSE to reset active		V_{DD} = 5 V, R_L = 4.7 kΩ, C_L = 100 pF			0.6	μs
t_{pd2}	Propagation delay, $\overline{RESIN}$ to reset active		C_T = 1 nF, T_A = 25°C			0.4	μs
t_{r1}	Rise time, RESET and $\overline{RESET}$	TLC7721, TLC7725	V_{DD} = 5 V, R_L = 4.7 kΩ, C_L = 100 pF			200	ns
t_{f1}	Fall time, RESET and $\overline{RESET}$	TLC7721, TLC7725				200	ns
t_{r2}	Rise time, RESET	TLC7701, TLC7705				200	ns
t_{f2}	Fall time, RESET	TLC7701, TLC7705			1	2	μs
t_{r3}	Rise time, $\overline{RESET}$	TLC7701, TLC7705			1	2	μs
t_{f3}	Fall time, $\overline{RESET}$	TLC7701, TLC7705				200	ns

†All characteristics are at 10 nF between CT and GND.
‡All typical values are at T_A = 25°C.
§Supply voltage slew rate should not exceed 30 V/μs.

NOTES: 3. Hysteresis is the difference between the positive-going input threshold voltage (V_{T+}) and the negative-going input threshold voltage (V_{T-}).
4. This parameter is measured in normal operation after the initial power-up reset. See typical operating sequence.

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PARAMETER MEASUREMENT INFORMATION

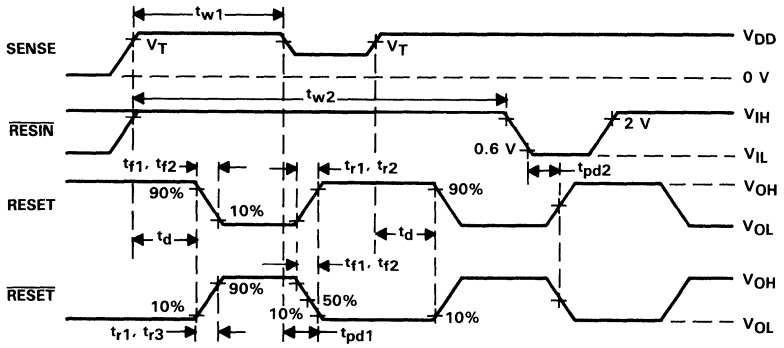

FIGURE 1. SWITCHING VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

The internal configuration, shown in the functional block diagram, comprises a precision SENSE input comparator, a precision voltage reference, a current source, a discharge NMOS transistor, an RS latch, and an output comparator that drives the reset outputs. Logic input $\overline{\text{RESIN}}$ feeds the input of another comparator.

The SENSE input comparator is used to monitor a chosen supply voltage. The reset outputs of TLC77__5 trip at an input voltage threshold level, preset by an internal high-impedance potential divider, equalling a 10% drop in a 5-V supply. The reset outputs of TLC77__1 trip at any user-defined supply voltage threshold level set by an external potential divider connected directly to the input of the SENSE comparator. The TLC77__1 SENSE comparator has a threshold level at its input set by the internal reference voltage of nominally 1.3 V (see electrical characteristics table values).

The current source, discharge NMOS transistor, and RS latch provide the retriggerable reset timing function with an external capacitor connected between CT and GND. The internal output comparator monitors the capacitor voltage and controls the state of the reset outputs.

The TLC770__ RESET and $\overline{\text{RESET}}$ outputs are open drain and require resistors to define the non-reset condition by pulling-up to V_{DD} or pulling-down to GND, respectively. Open-drain reset outputs allow the TLC770__ to be used in applications where wired-AND/OR is required. An example is microprocessors with reset inputs that also act as system reset outputs under software control. When this is not required, the push-pull outputs of TLC772__ are more appropriate. These use internal PMOS and NMOS transistors, respectively, on RESET and $\overline{\text{RESET}}$ outputs to define an active non-reset condition, saving an external pull-up resistor.

In operation, when the monitored supply voltage has reached the SVS threshold level V_T, an internal 5-μA current source starts to charge the external capacitor C_T. The reset outputs remain in their active reset state until the voltage across C_T reaches an internal 1.3-V reference voltage. The output comparator then returns the reset outputs to their non-reset states. The internal current source continues to charge C_T until a clamp level of 1.5 V is reached. Supply voltage drop-outs that make the SENSE input fall below V_T cause capacitor C_T to be discharged via the NMOS transistor. The input of the output comparator then falls below its reference level and the reset outputs are switched to an active reset state. A full reset timing pulse duration is ensured by discharging C_T to the same voltage level irrespective of the input SENSE

PRINCIPLES OF OPERATION

pulse duration above the minimum specified. This is achieved by detecting the C_T capacitor voltage level and only releasing the RS latch when the capacitor has reached 0.5 V. A feedback action maintains this value. At power-up, when C_T is fully discharged, the reset pulse duration (t_W) is approximately twice the duration of a reset pulse duration obtained when V_{DD} is established and TLC77__ is in normal operation.

Setting the $\overline{\text{RESIN}}$ input low has the same effect as the SENSE input falling below V_T. If the $\overline{\text{RESIN}}$ input is unused, it should be tied to V_{DD}. The $\overline{\text{RESIN}}$ input uses a comparator with a nominal threshold voltage of 1.3 V, and can be used to monitor supply voltages with an external potential divider in the manner of the TLC77__1 SENSE input but with less accuracy. For greater precision, the wired-OR $\overline{\text{RESET}}$ outputs of several TLC770__ devices used to monitor a systems multiple supply voltages can be fed into the $\overline{\text{RESIN}}$ input of a master SVS whose output provides the overall system reset function.

When their supply voltage approaches the nominal TTL threshold of 1.4 V during power-up, most logic devices start to become internally biased. Special bias circuits have been added to the TLC77__ RESET and $\overline{\text{RESET}}$ output transistor to ensure that these outputs are reset active when V_{DD} reaches 1 V. The $\overline{\text{RESET}}$ output will not exceed the lower TTL input threshold of 0.8 V. The only limitation is the initial rate of rise of supply voltage, which if greater than 30 V/μs may not allow sufficient time for the RESET and $\overline{\text{RESET}}$ MOS output transistors to be fully turned on. This is caused by their gate circuit time-constants being initially higher at very low supply voltages. The effect is for the $\overline{\text{RESET}}$ output to follow the supply voltage increase for several ns. This is not a problem in practice because power supplies usually assume a current sourcing mode at start-up that, when feeding into an output smoothing capacitor, limits the rate of rise of output voltage.

When using the TLC77__1, low-power applications require high-value external resistors to provide a user-defined external threshold level. To achieve minimum propagation delay, it may be necessary to provide compensation by means of a capacitor across the series resistor (the input capacitance of the SENSE comparator is typically 8 pF). Care should be taken that over compensation, which would cause triggering on noise, does not occur. Conversely, if it is desired to reduce susceptibility to noise, a capacitor can be placed across the input. For the TLC77__5, a low-value resistor in series with the SENSE input is required to achieve this function.

Capacitor C_T should have a leakage current substantially below the 5-μA charge current. This may rule out the use of electrolytic capacitors.

TLC77__ internal parameter values referred to in this description are nominal design values.

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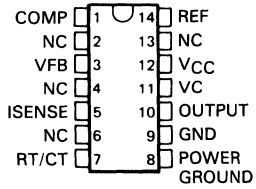
D3175, JANUARY 1989

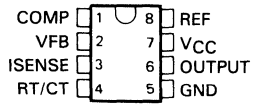
- **Optimized for Off-Line and DC-to-DC Converters**
- **Low Start-Up Current (< 1 mA)**
- **Automatic Feed-Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load-Response Characteristics**
- **Undervoltage Lockout with Hysteresis**
- **Double Pulse Suppression**
- **High-Current Totem-Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Error Amplifier with Low Output Resistance**
- **Designed to be Interchangable with Unitrode UC2842 and UC3842 Series**

D PACKAGE
(TOP VIEW)



NC—No internal connection

P PACKAGE
(TOP VIEW)



description

The UC2842 and UC3842 series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes with a minimum number of external components. Internally implemented circuits include: undervoltage lockout (UVLO) featuring a start-up current of less than 1 mA, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator (which also provides current-limit control), and a totem-pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

The primary difference between the UC2842-series devices and the UC3842-series devices is the ambient operating temperature range. The UC2842-series devices operate between −25°C and 85°C; the UC3842-series devices operate between 0°C and 70°C. Major differences between members of these series are the undervoltage lockout (UVLO) thresholds and maximum duty cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the UC__842 and UC__844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the UC__843 and UC__845 devices are 8.4 V on and 7.6 V off. The UC__842 and UC__843 devices can operate to duty cycles approaching 100%. A duty cycle range of 0 to 50% is obtained by the UC__844 and UC__845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage (see Note 1) (I_{CC} <30 mA) . . . . . Self Limiting
Analog input voltage (VFB and ISENSE terminals) . . . . . −0.3 V to 6.3 V
Voltage on output pin . . . . . 35 V
Voltage on VC pin (14-pin package) . . . . . 35 V
Supply current, I_{CC} . . . . . 30 mA
Output current . . . . . ±1 A
Error amplifier output sink current . . . . . 10 mA
Continuous power dissipation . . . . . see Dissipation Rating Table
Output energy (capacitive load) . . . . . 5 μJ
Storage temperature range . . . . . −65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the device GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	UC284_			UC384_			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} and VC			30			30	V
Average output current, I_O			200			200	mA
Reference output current			−20			−20	mA
Frequency range			500			500	kHz
Operating free-air temperature, T_A	−25		85	0		70	°C

electrical characteristics, V_{CC} = 15 V (see Note 2), R_T = 10 kΩ, C_T = 3.3 nF, T_A = full range (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	I_O = 1 mA, T_J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25		6	25	mV
Temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage with worst-case variation	V_{CC} = 12 V to 25 V, I_O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C		50			50		μV
Output voltage long-term drift	After 1000 h at T_A = 125°C		5	25		5	25	mV
Short-circuit output current		−30	−100	−180	−30	−100	−180	mA

NOTE 2: Adjust V_{CC} above the start threshold before setting it to 15 V.

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Voltage Regulator Circuits

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Basic Regulator Theory

The function of every voltage regulator is to convert a dc input voltage into a specific, stable, dc output voltage and maintain that voltage over a wide range of load current and input voltage conditions. To accomplish this, the typical voltage regulator (Figure 1) consists of:

1. A reference element that provides a known stable voltage level, (V_{REF})
2. A sampling element to sample the output voltage level
3. An error-amplifier element for comparing the output voltage sample to the reference and creating an error signal.
4. A power control element to provide conversion of the input voltage to the desired output level over varying load conditions as indicated by the error signal.

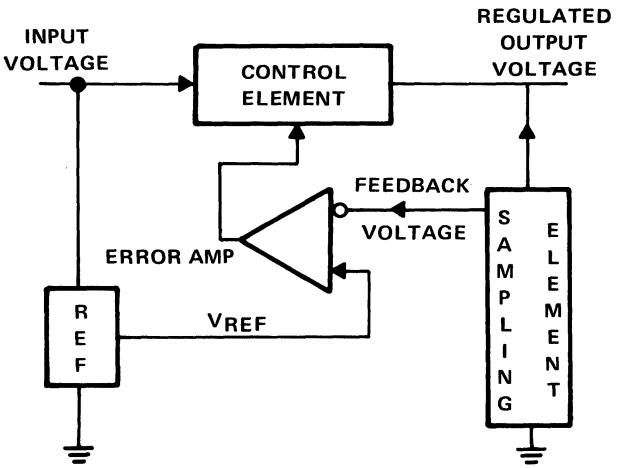


Figure 1. Basic Regulator Block Diagram

Although actual circuits may vary, the three basic regulator types are series, shunt, and switching. The four basic functions listed above exist in all three regulator types.

Voltage Regulator Components

Reference Element

The reference element forms the foundation of all voltage regulators since output voltage is directly controlled by the reference voltage. Variations in the reference voltage

will be interpreted as output voltage errors by the error amplifier and cause the output voltage to change accordingly. To achieve the desired regulation, the reference must be stable for all variations in supply voltages and junction temperatures. There are several common techniques which can be used to solve design problems using integrated circuit regulators. Many of these techniques are discussed in the section of the text that outlines error contributions.

Sampling Element

The sampling element monitors the output voltage and converts it into a level equal to the reference voltage. A variation in the output voltage causes the feedback voltage to change to a value which is either greater or less than the reference voltage. This voltage difference is the error voltage which directs the regulator to make the appropriate response and thus correct the output voltage change.

Error Amplifier

The error amplifier of an integrated circuit voltage regulator monitors the feedback voltage for comparison with the reference. It also provides gain for the detected error level. The output of the error amplifier drives the control circuit to return the output to the preset level.

Control Element

All the previous elements discussed remain virtually unaltered regardless of the type regulator circuit. The control element, on the other hand, varies widely, depending upon the type of regulator being designed. It is the element that determines the classification of the voltage regulator; series, shunt, or switching. Figure 2 illustrates the three basic control element configurations, each of which is discussed in detail. These elements contribute an insignificant amount of error to the regulator's performance. This is because the sampling element monitors the output voltage beyond the control element and

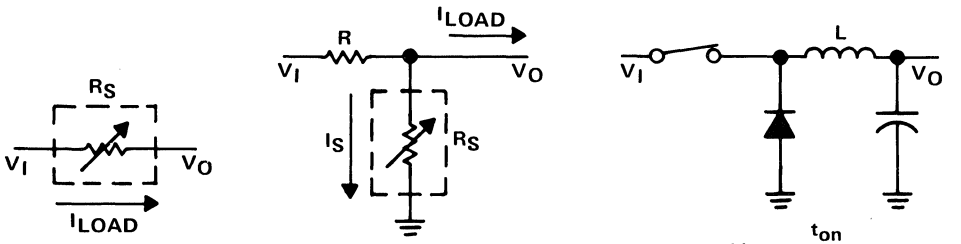


Figure 2. Control Element Configurations

compensates for its error contributions. However, the control element directly affects parameters such as minimum input-to-output voltage differential, circuit efficiency, and power dissipation.

Regulator Classifications

Series Regulator

The series regulator derives its name from its control element. The output voltage, V_O, is regulated by modulating an active series element, usually a transistor, that functions as a variable resistor. Changes in the input voltage, V_I, will result in a change in the equivalent resistance of the series element identified as R_S. The product of the resistance, R_S, and the load current, I_L creates a changing input-to-output differential voltage, $V_I - V_O$, that compensates for the changing input voltage. The basic series regulator is illustrated in Figure 3, and the equations describing its performance are listed below.

$$\begin{aligned} V_O &= V_I - (V_I - V_O) \\ (V_I - V_O) &= I_L R_S \\ V_O &= V_I - I_L R_S \end{aligned}$$

The change in R_S for a changing input voltage is:

$$\Delta R_S = \frac{\Delta V_I}{I_L}$$

The change in R_S for a changing load current:

$$\Delta R_S = \frac{\Delta I_L R_S}{I_L + \Delta I_L}$$

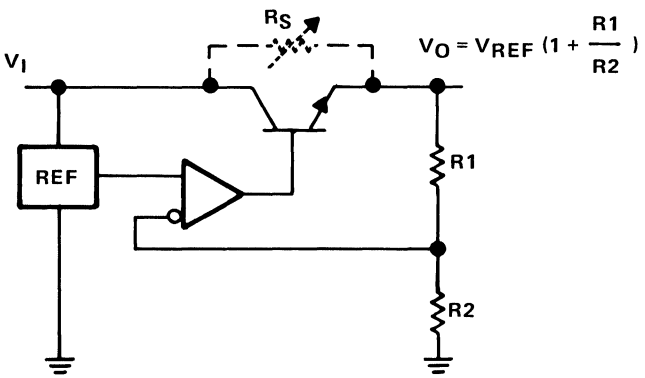


Figure 3. Basic Series Regulator

Series regulators provide a simple, inexpensive way to obtain a source of regulated voltage. In high-current applications, however, the voltage drop which is maintained across the control element will result in substantial power loss and a much lower efficiency regulator.

Shunt Regulator

The shunt regulator employs a shunt control element in which the current is controlled to compensate for varying input voltage or changing load conditions. The basic shunt regulator is illustrated in Figure 4.

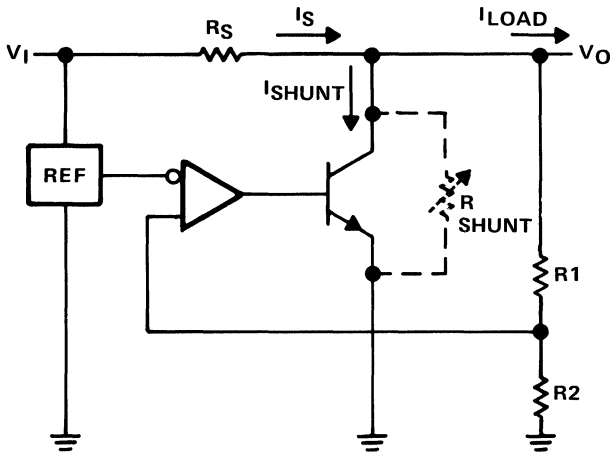


Figure 4. Basic Shunt Regulator

The output voltage, V_O as with the series regulator, is held constant by varying the voltage drop across the series resistor, R_S, by varying the current I_S. I_S may vary because of I_L changes or it may vary because of current, $I_{(shunt)}$, through the shunt control element. For example, as I_L increases, $I_{(shunt)}$ decreases to adjust the voltage drop across R_S. In this fashion V_O is held constant.

$$V_O = V_I - I_S R_S$$
$$I_S = I_L + I_{(shunt)}$$
$$V_O = V_I - R_S[I_L + I_{(shunt)}]$$

The change in shunt current for a changing load current is:

$$\Delta I_{(shunt)} = -\Delta I_L$$

The change in shunt current for a changing input voltage is:

$$\Delta I_{(shunt)} = \frac{\Delta V_I}{R_S}$$

$$I_{(shunt)} = \frac{V_O}{R_{(shunt)}}$$

Even though it is usually less efficient than series or switching regulators, a shunt regulator may be the best choice for some applications. The shunt regulator is less sensitive to input voltage transients; does not reflect load current transients back to the source, and is inherently short-circuit proof.

Switching Regulator

The switching regulator employs an active switch as its control element. This switch is used to chop the input voltage at a varying duty cycle based on the load requirements. A basic switching regulator is illustrated in Figure 5.

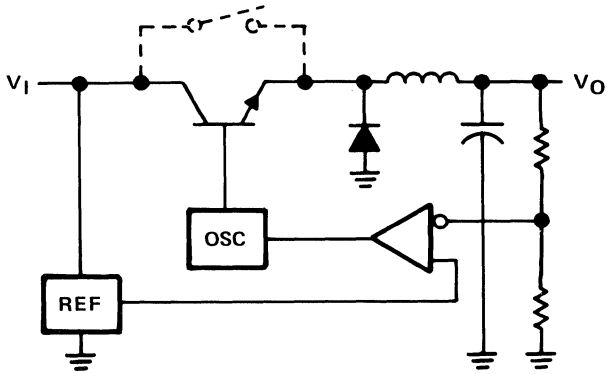


Figure 5. Basic Switching Regulator (Step-Down Configuration)

A filter, usually an LC filter, is then used to average the voltage present at its input and deliver that voltage to the output load. Because the pass transistor is either on (saturated) or off, the power dissipated in the control element is minimal. The switching regulator is therefore more efficient than the series or shunt type. For this reason, the switching regulator becomes particularly advantageous for applications involving large input-to-output differential voltages or high load-current requirements. In the past, switching voltage regulators were discrete designs. However, recent advancements in integrated circuit

technology have resulted in several monolithic switching regulator circuits that contain all of the necessary elements to design step-up, step-down, or inverting voltage converters. The duty cycle may be varied by:

1. maintaining a constant on-time, varying the frequency
2. maintaining a constant off-time, varying the frequency
3. maintaining a constant frequency, varying the on/off times

Major Error Contributors

The ideal voltage regulator maintains constant output voltage despite varying input voltage, load current, and temperature conditions. Realistically, these influences affect the regulator's output voltage. In addition, the regulator's own internal inaccuracies affect the overall circuit performance. This section discusses the major error contributors, their effects, and suggests some possible solutions to the problems they create.

Regulator Reference Techniques

There are several reference techniques employed in integrated circuit voltage regulators. Each provides its particular level of performance and problems. The optimum reference depends on the regulator's requirements.

Zener Diode Reference

The zener diode reference, as illustrated in Figure 6, is the simplest technique. The zener voltage itself, V_Z, forms the reference voltage, V_{REF}.

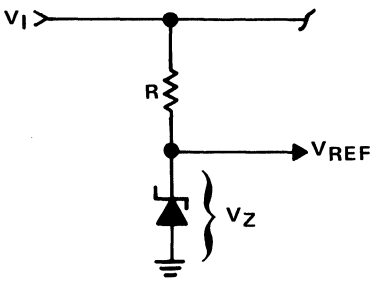


Figure 6. Basic Zener Reference

This technique is satisfactory for relatively stable supply-voltage and load-current applications. The changing zener current results in a change in the zener diode's reference voltage, V_Z. This zener reference model is illustrated in Figure 7.

Constant-Current Zener Reference

The zener reference can be refined by the addition of a constant-current source as its supply. Driving the zener diode with a constant current minimizes the effect of zener

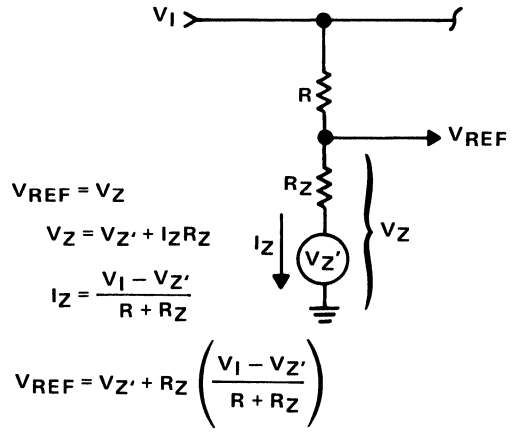


Figure 7. Zener Reference Model

impedance on the overall stability of the zener reference. An example of this technique is illustrated in Figure 8. The reference voltage of this configuration is relatively independent of changes in supply voltage and load current.

$$V_{REF} = V_Z + V_{BE(Q1)}$$

$$I_Z = \frac{V_{BE(Q1)}}{R_{CS}} + I_{B(Q1)}$$

In addition to superior supply voltage independence, the circuit illustrated in Figure 8 yields improved temperature stability. The reference voltage, V_{REF}, is the sum of the zener voltage (V_Z) and the base-emitter voltage of Q1[$V_{BE(Q1)}$]. A low temperature

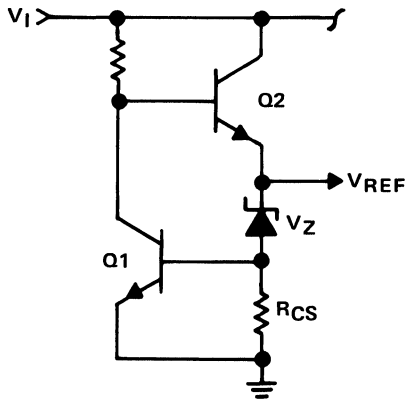


Figure 8. Constant-Current Zener Reference

coefficient can be achieved by balancing the positive temperature coefficient of the zener with the negative temperature coefficient of the base-emitter junction of Q1.

Band-Gap Reference

Another popular reference is the band-gap reference, which developed from the highly predictable emitter-base voltage of integrated transistors. Basically, the reference voltage is derived from the energy-band-gap voltage of the semiconductor material [$V_{go(silicon)}$ = 1.204 V]. The basic band-gap configuration is illustrated in Figure 9. The reference voltage, V_{REF}, in this case is:

$$V_{REF} = V_{BE(Q3)} + I_2 R_2$$

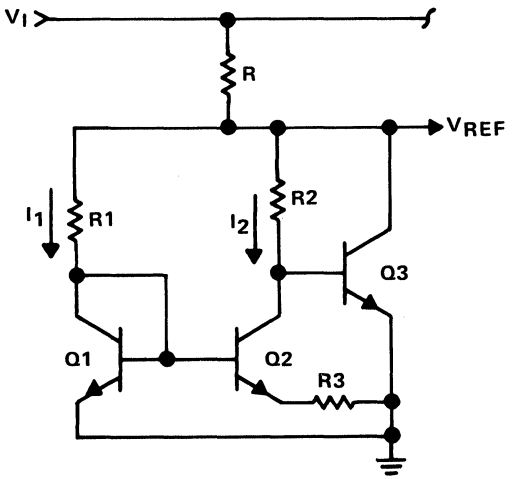


Figure 9. Band-Gap Reference

The resistor values of R1 and R2 are selected in such a way that the current through transistors Q1 and Q2 are significantly different ($I_1 = 10I_2$). The difference in current through transistors Q1 and Q2 also results in a difference in their respective base-emitter voltages. This voltage differential [$V_{BE(Q1)} - V_{BE(Q2)}$] will appear across R3. Application of transistors with sufficiently high gain results in current I_2 passing through R3. In this instance, I_2 is equal to:

$$\frac{V_{BE(Q1)} - V_{BE(Q2)}}{R3}$$

$$\therefore V_{REF} = V_{BE(Q3)} + \left[\left(V_{BE(Q1)} - V_{BE(Q2)}\right)\frac{R2}{R3}\right]$$

By analyzing the effect of temperature on V_{REF} it can be shown that the difference between two similar transistors' emitter-base voltages, when operated at different currents is:

$$V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q} \ln \frac{I_1}{I_2}$$

where

k = Boltzmann's constant
T = absolute temperature – degrees K
q = charge of an electron
I = current

The base-emitter voltage of Q3 can also be expressed as:

$$V_{BE(Q3)} = V_{go}\left[1 - \frac{T}{T_O}\right] + V_{BEO}\left[\frac{T}{T_O}\right]$$

where

V_{go} = band-gap potential
V_{BEO} = emitter-base voltage at T_O

V_{REF} can then be expressed as:

$$V_{REF} = V_{go}\left[1 - \frac{T}{T_O}\right] + V_{BEO}\left[\frac{T}{T_O}\right] + \frac{R2}{R3} \quad \frac{kT}{q} \ln \frac{I_1}{I_2}$$

Differentiating with respect to temperature yields

$$\frac{dV_{REF}}{dT} = -\frac{V_{go}}{T_O} + \frac{V_{BEO}}{T_O} + \frac{R2}{R3} \frac{k}{q} \ln \frac{I_1}{I_2}$$

If R2, R3, and I_1 are appropriately selected such that

$$\frac{R2}{R3} \ln \frac{I_1}{I_2} = [V_{go} - V_{BEO(Q3)}]\ C$$

where

$$C = \frac{q}{kT_O}$$

and

$$V_{go} = 1.2\ V$$

the resulting

$$\frac{dV_{REF}}{dT} = 0$$

The reference is temperature-compensated.

Band-gap reference voltage is particularly advantageous for low-voltage applications (V_{REF} = 1.2 V) and it yields a reference level that is stable even with variations in supply and temperature.

Sampling Element

The sampling element used on most integrated circuit voltage regulators is an R1/R2 resistor divider network (Figure 10), which can be determined by the output-voltage-to-reference-voltage ratio.

$$\frac{V_O}{V_{REF}} = 1 + \frac{R1}{R2}$$

Since the feedback voltage is determined by ratio and not absolute value, proportional variations in R1 and R2 have no effect on the accuracy of the integrated circuit voltage regulator. When proper attention is given to the layout of these resistors in an integrated circuit, their contribution to the error of the voltage regulator will be minimal. The initial accuracy is the only parameter affected.

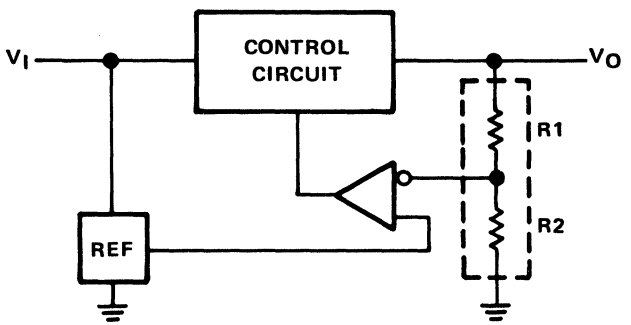


Figure 10. R1/R2 Ladder Network Sampling Element

Error Amplifier Performance

If a stable reference and an accurate output sampling element exist, the error amplifier becomes the primary factor determining the performance of the voltage regulator. Typical amplifier performance parameters such as offset, common-mode and supply-rejection ratios, output impedance, and temperature coefficient affect the accuracy and regulation of the voltage regulator. These amplifier performance parameters will affect the accuracy of the regulator due to variations in supply, load, and ambient temperature conditions.

Offset Voltage

Offset voltage is viewed by the amplifier as an error signal, as illustrated in Figure 11, and will cause the output to respond accordingly.

$$V_O = A_V V_I$$

$$V_I = V_{REF} - V_{IO} - V_{FB}$$

$$V_{FB} = V_O \left[\frac{R2}{R1 + R2} \right]$$

$$V_O = \frac{V_{REF} - V_{IO}}{\frac{1}{A_V} + \left[\frac{R2}{R1 + R2} \right]}$$

If A_V is sufficiently large

$$V_O = (V_{REF} - V_{IO}) \left[1 + \frac{R1}{R2} \right]$$

V_{IO} represents an initial error in the output of the integraged circuit voltage regulator. The simplest method of compensating for this error is to adjust the output voltage sampling element R1/R2.

Offset Change with Temperature

The technique discussed above compensates for the amplifier's offset voltage and yields an accurate regulator, but only at a specific temperature. In most amplifiers, the offset voltage change with temperature is proportional to the initial offset level. Trimming the output voltage sampling element, does not reduce the offset voltage but merely counteracts it. At a different ambient tmperature, the offset voltage changes and, thus, error is again introduced into the voltage regulator. Monolithic integrated circuit regulators use technology that essentially eliminates offset in integrated circuit amplifiers. With minimal offset voltage, drift caused by temperature variations will have little consequence.

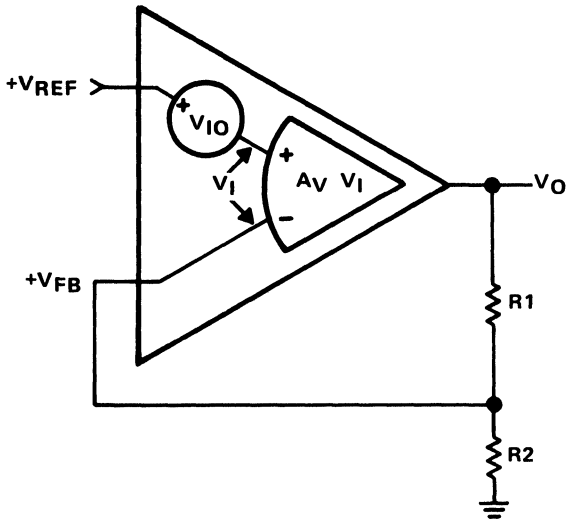


Figure 11. Amplifier Model Showing Input Offset Voltage Effect

Supply Voltage Variations

The amplifier's power supply and common-mode rejection ratios are the primary contributors to regulator error which has been introduced by an unregulated input voltage. In an ideal amplifier, the output voltage is a function of the differential input voltage only. Realistically, the common-mode voltage of the input also influences the output voltage. The common-mode voltage is the average input voltage, referenced from the amplifier's virtual ground (see Figure 12 and the following equations).

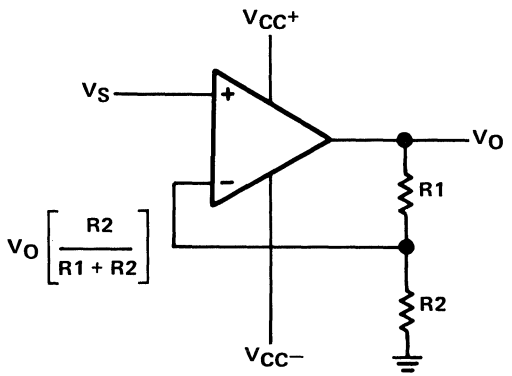


Figure 12. Amplifier Model Showing Common-Mode Voltage

$$\text{Virtual ground} = \frac{V_{CC+} + V_{CC-}}{2}$$

$$V_{I(av)} = \frac{V_S + V_O\left[\frac{R2}{R1+R2}\right]}{2}$$

$$V_{CM} = \frac{1}{2}\left[V_S + V_O\left(\frac{R2}{R1+R2}\right) - \left(V_{CC+} + V_{CC-}\right)\right]$$

From this relation, it can be seen that unequal variations in either power supply bus rail will result in a change in the common-mode voltage. The common-mode voltage rejection ration (CMRR) is the ratio of the amplifier's differential voltage amplification to the common-mode voltage amplification.

$$CMRR = \frac{A_{VD}}{A_{VCM}}$$

$$A_{VCM} = \frac{A_{VD}}{CMRR}$$

That portion of output which is voltage contributed by the equivalent common-mode input voltage is:

$$V_O = V_{CM}A_{VCM} = \frac{A_{VD}V_{CM}}{CMRR}$$

The equivalent error introduced then is:

$$\text{COMMON-MODE ERROR} = \frac{V_{CM}}{CMRR}$$

The common-mode error represents an offset voltage to the amplifier. Neglecting the actual offset voltage, the output voltage of the error amplifier then becomes:

$$V_O = \left(V_{REF} + \frac{V_{CM}}{CMRR}\right)\left(1 + \frac{R1}{R2}\right)$$

Using constant-current sources in most integrated circuit amplifiers, however, yields a high power-supply (common-mode) rejection ratio. This power-supply rejection ratio is of such a large magnitude that the common-mode voltage effect on V_O can usually be neglected.

Regulator Design Considerations

Various types of integrated circuit voltage regulators are available, each having its own particular characteristics, giving it advantages in various applications. The type of regulator used depends primarily upon the designer's needs and trade-offs in performance and cost.

Positive vs Negative Regulators

This classification of voltage regulators is easily understood; a positive regulator is used to regulate a positive voltage, and a negative regulator is used to regulate a negative voltage. However, what is positive and negative may vary, depending upon the ground reference.

Figure 13 illustrates conventional positive and negative voltage regulator applications employing a continuous and common ground. For systems operating on a single supply, the positive and negative regulators may be interchanged by floating the ground reference to the load or input. This approach to design is recommended only where ground isolation serves as an advantage to overall system performance.

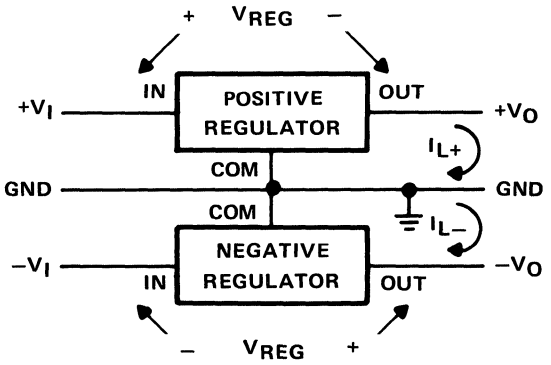


Figure 13. Conventional Positive/Negative Regulator

Figures 14 and 15 illustrate a positive regulator in a negative configuration and a negative regulator in a positive configuration, respectively.

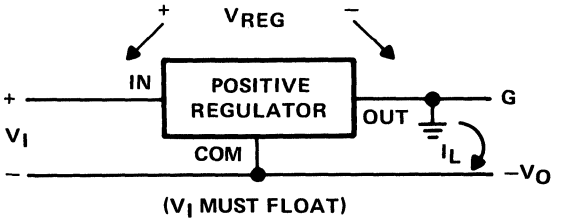


Figure 14. Positive Regulator in Negative Configuration

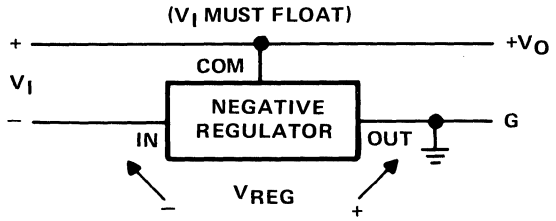


Figure 15. Negative Regulator in Positive Configuration

Fixed vs Adjustable Regulators

Many fixed three-terminal voltage regulators are available in various current ranges from most major integrated circuit manufacturers. These regulators offer the designer a simple, inexpensive method to establish a regulated voltage source. Their particular advantages are:

1. Ease of use
2. Few external components required
3. Reliable performance
4. Internal thermal protection
5. Short-circuit protection.

There are disadvantages. The fixed three-terminal voltage regulators cannot be precisely adjusted because their output voltage sampling elements are internal. The initial accuracy of these devices may vary as much as ±5% from the nominal value; also the output voltages available are limited.

Current limits are based on the voltage regulator's applicable current range and are not adjustable. Extended range operation (increasing I_{LOAD}) is cumbersome and requires complex external circuitry.

The adjustable regulator may be well suited for those applications requiring higher initial accuracy. This depends on the complexity of the adjustable voltage regulator. Additionally, all adjustable regulators use external feedback, which allows the designer a precise and infinite voltage selection.

The output sense may also be referred to a remote point. This allows the designer to not only extend the range of the regulator (with minimal external circuitry), but also to compensate for losses in a distributed load or external pass components. Additional features found on many adjustable voltage regulators are: adjustable short-circuit current limiting, access to the voltage reference element, and shutdown circuitry.

Dual-Tracking Regulator

The dual-tracking regulator (Figure 16) provides regulation for two power supply buses, usually one positive and one negative. The dual-tracking feature assures a balanced supply system by monitoring the voltage on both power supply buses. If either of the voltages sags or goes out of regulation, the tracking regulator will cause the other voltage to vary accordingly (A 10% sag in the positive voltage will result in a 10% sag in the negative voltage.). These regulators are, for the most part, restricted to applications such as linear systems where balanced supplies offer a definite performance improvement.

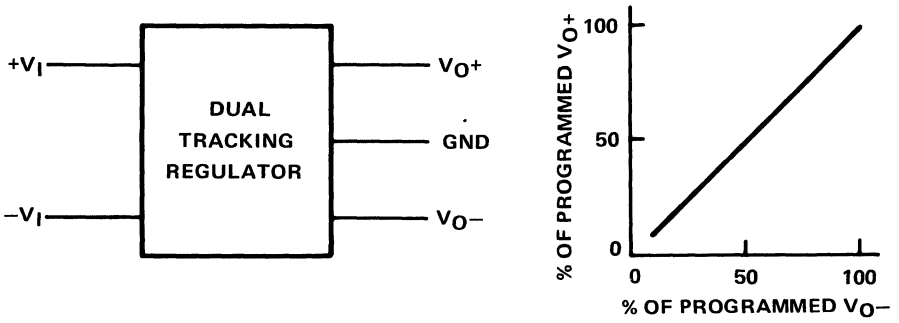


Figure 16. Dual-Tracking Regulator

Series Regulator

The series regulator is well suited for medium current applications with nominal voltage differential requirements. Modulation of a series pass control element to maintain a well-regulated, prescribed, output voltage is a straightforward design technique. Safe-operating-area protection circuits such as overvoltage, fold-back current limiting, and short-circuit protection are additional functions that series regulators can supply. The primary disadvantage of the series regulator is its power consumption. The amount of power a series regulator (Figure 17) will consume depends on the load current being drawn from the regulator and is proportional to the input-to-output voltage differential. The amount

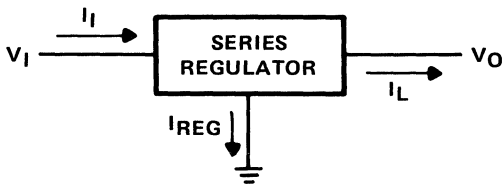


Figure 17. Series Regulator

of power consumed becomes considerable with increasing load or differential voltage requirements. This power loss limits the amount of power that can be delivered to the load because the amount of power that can be dissipated by the series regulator is limited.

The equations that describe these conditions are listed below. P_{REG} is the power lost in the regulator, I_I is the input current, I_{REG} is the regulator current and I_L is the load current. The differential voltage across the regulator is $(V_I - V_O)$.

$$P_{REG} = V_I I_I - V_O I_L$$

$$I_I = I_{REG} + I_L$$

Since I_L is much greater than I_{REG}

$$I_I = I_L$$

$$P_{REG} = I_L (V_I - V_O)$$

Floating Regulator

The floating regulator (Figure 18) is a variation of the series regulator. The output voltage remains constant by changing the input-to-output voltage differential for varying input voltage. The floating regulator's differential voltage is modulated such that its output voltage when referenced to its common terminal $V_{O(reg)}$ is equal to its internal reference (V_{REF}). The voltage developed across the output-to-common terminal is equal to the voltage developed across R1(V_{R1}).

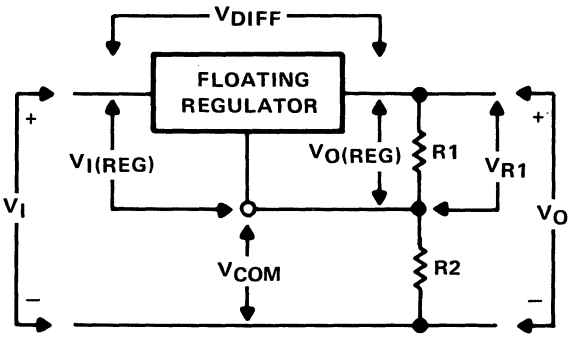


Figure 18. Floating Regulator

$$V_{O(reg)} = V_{REF} = V_{R1}$$

$$V_{R1} = V_O \left[\frac{R1}{R1+R2}\right]$$

$$V_O = V_{REF}\left[1+\frac{R2}{R1}\right]$$

The common-terminal voltage is:

$$V_{COM} = V_O - V_{R1} = V_O - V_{REF}$$

The input voltage seen by the floating regulator is:

$$V_{I(reg)} = V_I - V_{COM}$$

$$V_{I(reg)} = V_I - V_O + V_{REF}$$

$$V_{I(reg)} = V_{DIFF} + V_{REF}$$

Since V_{REF} is fixed, the only limitation on the input voltage is the allowable differential voltage. This makes the floating regulator especially suited for high-voltage applications ($V_I > 40$ V). Practical values of output voltage are limited to practical ratios of output-to-reference voltages.

$$\frac{R2}{R1} = \frac{V_O}{V_{REF}} - 1$$

The floating regulator exhibits power consumption characteristics similar to that of the series regulator from which it is derived, but unlike the series regulator, it can also serve as a current regulator as shown in Figure 19.

$$V_O = V_{REF}\left[1+\frac{R_L}{R_S}\right]$$

$$V_O = V_L + V_{O(reg)}$$

$$V_{O(reg)} = V_{REF}$$

$$V_L = V_{REF}\left[1+\frac{R_L}{R_S}\right] - V_{REF}$$

$$V_L = V_{REF}\left[\frac{R_L}{R_S}\right]$$

$$I_L = \frac{V_{LOAD}}{R_L}$$

$$I_{LOAD} = \frac{V_{REF}}{R_S}$$

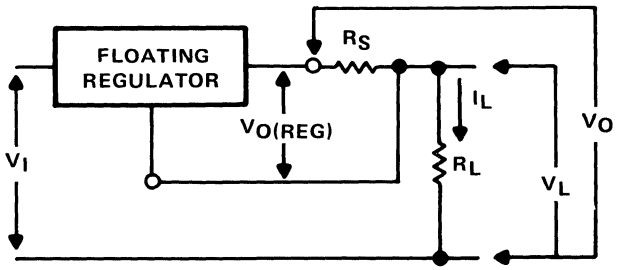


Figure 19. Floating Regulator as a Constant-Current Regulator

Shunt Regulator

The shunt regulator, illustrated in Figure 20, is the simplest of all regulators. It employs a fixed resistor as its series pass element. Changes in input voltage or load current requirements are compensated by modulating the current which is shunted to ground through the regulator.

For changes in V_I: $\Delta I_Z = \frac{\Delta V_I}{R_S}$

For changes in I_L: $\Delta I_Z = -\Delta I_L$

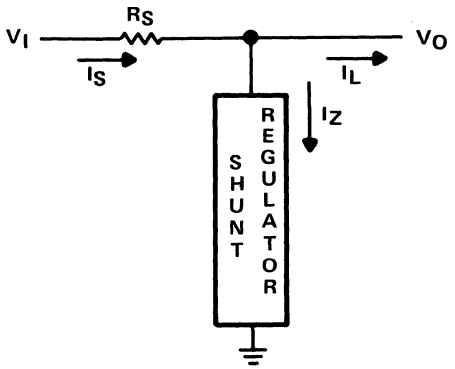


Figure 20. Shunt Regulator

The inherent short-circuit-proof feature of the shunt regulator makes it particularly attractive for some applications. The output voltage will be maintained until the load current required is equal to the current through the series element (see Figure 21). Since the shunt regulator cannot supply any current, additional current required by the load will result in reducing the output voltage to zero.

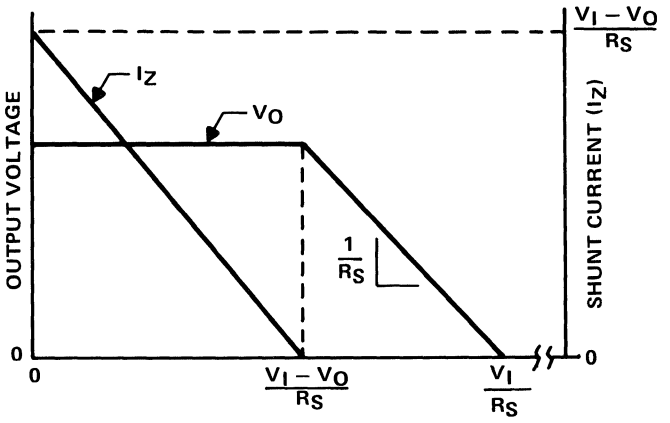


Figure 21. Output Voltage vs Shunt Current of a Shunt Regulator

$$V_O = V_I - I_L R_S$$

The short-circuit current of the shunt regulator then becomes:

$$V_O = 0$$

$$I_{SC} = \frac{V_I}{R_S}$$

Switching Regulator

The switching regulator lends itself primarily to the higher power applications or those applications where power supply and system efficiency are of the utmost concern. Unlike the series regulator, the switching regulator operates its control element in an on- or off-mode. Switching regulator control element modes are illustrated in Figure 22.

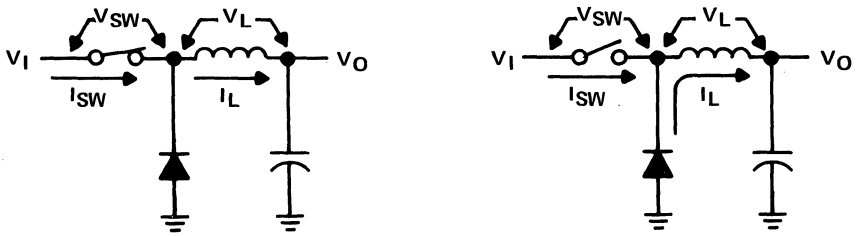


Figure 22. Switching Voltage Regulator Modes

In this manner, the control element is subjected to a high current at a very low voltage or a high differential voltage at a very low current. In either case, power dissipation in the control element is minimal. Changes in the load current or input voltage are compensated for by varying the on-off ratio (duty cycle) of the switch without increasing the internal power dissipated in the switching regulator. See Figure 23(a).

For the output voltage to remain constant, the net charge in the capacitor must remain constant. This means the charge delivered to the capacitor must be dissipated in the load.

$$I_C = I_{L'} - I_L$$

$$I_C = -I_L \text{ for } I_{L'} = 0$$

$$I_C = I_{L(pk)} - I_L \text{ for } I_{L'} = I_{L(pk)}$$

The capacitor current waveform then becomes that illustrated in Figure 23(b). The charge delivered to the capacitor and the charge dissipated by the load are equal to the areas under the capacitor current waveform.

$$\Delta Q+ = \frac{1}{2}\frac{(I_{L(pk)} - I_L)^2}{I_{L(pk)}} t \left(\frac{V_I}{V_C}\right)$$

$$\Delta Q- = I_L \left[t_{period} - \frac{1}{2} t \left(\frac{V_I}{V_C}\right) - \frac{1}{2} t \left(\frac{I_{L(pk)} - I_L}{I_{L(pk)}}\right)\left(\frac{V_I}{V_C}\right)\right]$$

By setting $\Delta Q+$ equal to $\Delta Q-$, the relationship of I_L and $I_{L(pk)}$ for $\Delta Q = 0$ can be determined;

$$I_L = \frac{1}{2} I_{L(pk)} \left[\frac{V_I}{V_C} \frac{t}{t_{period}}\right]$$

As this demonstrates, the duty cycle t/t_{period} can be altered to compensate for input voltage changes or load variations.

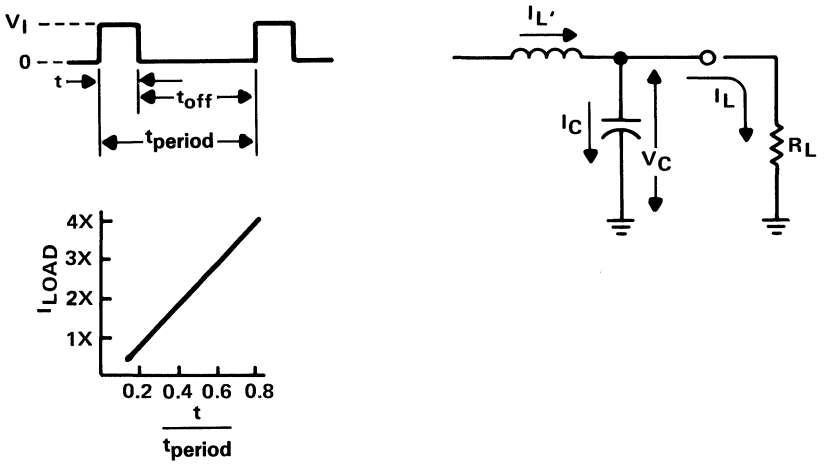
The duty cycle t/t_{period} can be altered a number of different ways.

$t = t_{on}$ (inductor charge time)

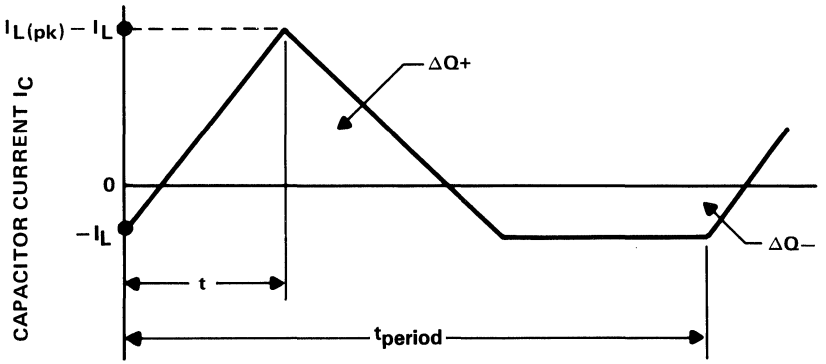
t_{period} = Total time ($t_{on} + t_{off} + t_I$) where t_I is the time from t_{off} until the start of the next charge cycle.

Knowing t_{period} then:

$$f = \frac{1}{t_{period}}$$



(a) CHANGES IN THE LOAD CURRENT WITH DUTY CYCLE



(b) CAPACITOR CURRENT WAVEFORM

Figure 23. Variation of Pulse Width vs Load

Fixed-On-Time, Variable Frequency

One technique of voltage regulation is to maintain a fixed or predetermined "on" time (t), the time the input voltage is being applied to the LC filter and vary the duty cycle by varying the frequency (f). This method makes voltage conversion applications design easier (step-up, step-down, invert) since the energy stored in the inductor of the LC filter during the on-time (which is fixed) determines the amount of power deliverable to the load. Thus calculation of the inductor is fairly straightforward.

$$L = \frac{V}{I} t$$

where

L = value of inductance in microhenrys
V = differential voltage in volts
I = required inductor current defined by the load in amps
t = on-time in microseconds

The fixed-on-time approach is also advantageous from the standpoint that a consistent amount of energy is stored in the inductor during the fixed on-time period. This simplifies the design of the inductor by defining the operating parameters to which the inductor is subjected. The operating characteristic of a fixed-on-time switching voltage regulator is a varying frequency, which changes directly with changes in the load. This can be seen in Figure 24.

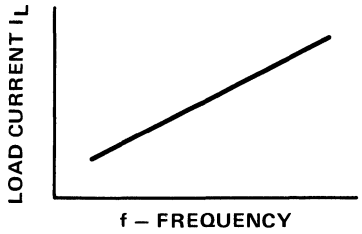


Figure 24. Frequency vs Load Current for Fixed On-Time SVR

Fixed-Off-Time, Variable Frequency

In the fixed-off-time switching voltage regulator, the average dc voltage is varied by changing the on time (t) of the switch while maintaining a fixed off-time (t_{off}). The fixed-off-time switching voltage regulator behaves in a manner opposite that of the fixed-on-time regulator.

As the load current increases, the on time is made to increase, thus decreasing the operating frequency; this is illustrated in Figure 25. This approach provides the capability to design a switching voltage regulator that will operate at a well-defined minimum frequency under full-load conditions.

The fixed-off-time approach also allows a dc current to be established in the inductor under increased load conditions, thus reducing the ripple current while maintaining the same average current. The maximum current experienced in the inductor under transient load conditions is not as well defined as that found in the fixed-on-time regulator. Thus, additional precautions should be taken to ensure that the inductor does not saturate.

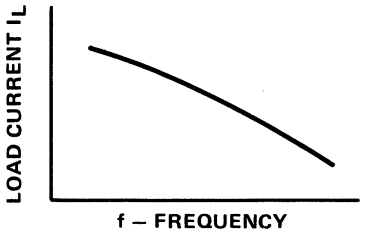


Figure 25. Frequency vs Load Current for Fixed Off-Time SVR

Fixed-Frequency, Variable Duty Cycle

The fixed-frequency switching regulator varies the duty cycle of the pulse train in order to change the average power. The fixed-frequency concept is particularly advantageous for systems employing transformer-coupled output stages. The fixed frequency permits efficient design of the associated magnetics. Transformer coupling also has advantages in single and multiple voltage-conversion applications. The fixed-frequency regulator will establish a dc current through the inductor (for increased load conditions) to maintain the required load current with minimal ripple current. The single-ended and transformer-coupled configurations are illustrated in Figure 26.

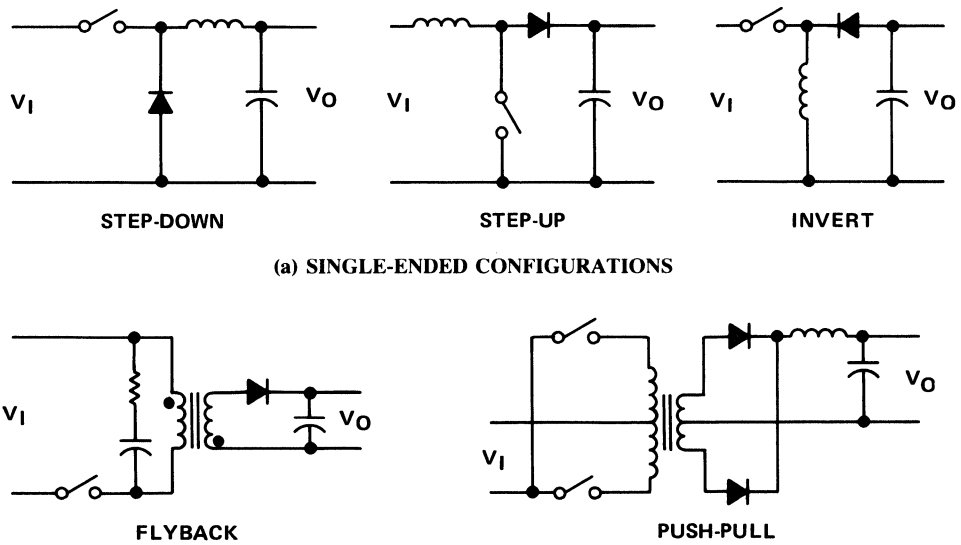


Figure 26. Switching Voltage Regulator Configurations

These types of switching regulators can thus be operated with high efficiency to provide low-voltage, regulated outputs from a high-voltage, unregulated supply or vice versa. The switching frequency should be established at the optimum value for the switching components of the supply (transformer, switching transistor, inductor, and filter capacitor). High-frequency operation is distinctly advantageous because the cost, weight, and volume of both L and C filter elements are reduced. However, the frequency at which the effective series resistance of the filter capacitor equals its capacitive reactance is the maximum allowable frequency.

Operation above 20 kHz is desirable to eliminate the possibility of audible noise. Choosing an operating frequency that is too high will result in power switching transistor losses as well as "catch" diode losses. The higher cost of these high performance components must be balanced against the reduced cost, size, and weight of the L and C components when determining the optimum frequency for a specific application.

Regulator Safe Operating Area

The safe operating area (SOA) is a term used to define the input and output voltage range and load current range within which any device is designed to operate reliably. Exceeding these limits will result in a catastrophic failure or will render the device temporarily inoperative, depending upon the device and its performance characteristics. Integrated circuit voltage regulators with internal current limiting, thermal and short-circuit protection will merely shut down. External components, such as pass transistors on the other hand, may respond with catastrophic failure.

Regulator SOA Considerations

Although particular design equations depend upon the type of integrated circuit voltage regulator used and its application, there are several boundaries that apply to all regulator circuits for safe, reliable performance.

Input Voltage

The limits on the input voltage are derived from three considerations:

V_{Imax}
The absolute maximum rated input voltage as referenced to the regulator's ground. This is a safe operating area (SOA) destruct limit.

$(V_I - V_O)_{min}$
The input-to-output differential voltage also referred to as the dropout voltage, at which the regulator ceases to function properly. This is a functional limit.

$(V_I - V_O)_{max}$
The maximum input-to-output differential voltage. Usually, the regulator's power dissipation is exceeded prior to the $(V_I - V_O)_{max}$ limit. This is an SOA level that can be limited by the allowable power dissipation (P_{Dmax}).

Load Current

I_{Lmax}

The maximum load current deliverable from the integrated circuit regulator. If internal current limiting is not provided, external protection should be provided. This is a functional limit that may be further limited by P_{Dmax}.

Power Dissipation

P_{Dmax}

The maximum power that can be dissipated within the regulator. Power dissipation is the product of the input-to-output differential voltage and the load current, and is normally specified at or below a given case temperature. This rating is usually based on a 150 °C junction temperature limit. The power rating is an SOA limit unless the integrated circuit regulator provides an internal thermal protection.

Output Voltage of an Adjustable-Voltage Regulator

V_{Omin}

The minimum output voltage a regulator is capable of regulating. This is usually a factor of the regulator's internal reference and is a functional limit.

V_{Omax}

The maximum output voltage a regulator is capable of regulating. This is largely dependent on the input voltage and is a functional limit.

External Pass Transistor

For applications requiring additional load current, integrated circuit voltage regulator capabilities may be boosted with the addition of an external pass transistor. When employed, the external pass transistor, in addition to the voltage regulator, must be protected against operation outside its safe operating area. Operation outside the safe operating area is catastrophic to most discrete transistors.

I_{Cmax}

The maximum current the transistor is capable of sustaining. I_{Cmax} now becomes the maximum current the regulator circuit is capable of delivering to the load. Associated with I_{Cmax} is a collector-emitter voltage ($V_{CE} = V_I - V_O$). If the product ($V_I - V_{Omax}$) I_{Cmax} exceeds the SOA then I_{Cmax} will have to be derated. This will then become a functional limit instead of a catastrophic limit. I_{Cmax} is related to power dissipation and junction or case temperature. I_{Cmax} must again be derated if the thermal or power ratings at which it is specified are exceeded. The resulting derated I_{Cmax} should continue to be considered as a catastrophic limit. Actual I_{Cmax} limits and derating information will appear on the individual transistor specification.

V_{CEmax}
The maximum collector-emitter voltage that can be applied to the transistor in the off-state. Exceeding this limit can be catastrophic.

P_{Dmax}
The maximum power that can be dissipated by the transistor. This is usually specified at a specific junction or case temperature. If the transistor is operated at higher temperatures, the maximum power must be derated in accordance with the operating rules specified in the transistor's applicable specification. Prolonged operation above the transistor's maximum power rating will result in degradation or destruction of the transistor.

Safe Operating Protection Circuits

Selection of the proper integrated circuit voltage regulators and external components will result in a reliable design in which all devices can operate well within their respective safe operating areas. Fault conditions (such as a short-circuit or excessive load) may cause components in the regulator circuit to exceed their safe operating area operation. Because of this situation, as well as protection for the load, certain protection circuits should be considered.

Reverse Bias Protection

A potentially dangerous condition may occur when a voltage regulator becomes reverse biased. For example, if the input supply were crowbarred to protect either the supply itself or additional circuitry, the filter capacitor at the output of the regulator circuit would maintain the regulator's output voltage and the regulator circuit would be reverse biased. If the regulated voltage is large enough (greater than 7 V), the regulator circuit may be damaged. To protect against this, a diode can be used as illustrated in Figure 27.

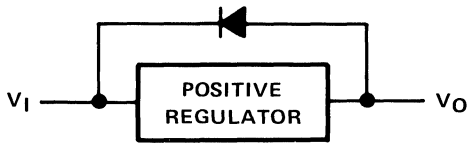


Figure 27. Reverse Bias Protection

Current Limiting Techniques

The type of current limiting used depends primarily on the safe operating area of the pass element used. The three basic current limiting techniques are series resistor, constant current, and fold-back current limiting.

Series Resistor

This is the simplest method for short-circuit protection. The short-circuit current is determined by the current-limiting resistor R_{CL}, illustrated in Figure 28.

$$V_O = V_{O(reg)} - I_L R_{CL}$$

A short-circuit condition occurs when $V_O = 0$, thus:

$$I_{SC} = I_L \text{ @ } (V_O = 0) = \frac{V_{O(reg)}}{R_{CL}}$$

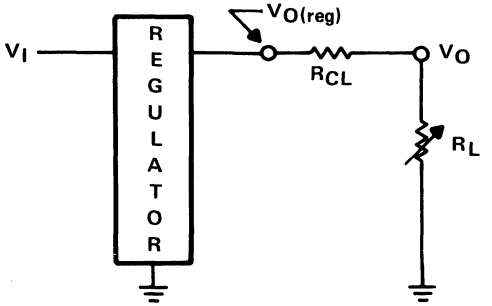


Figure 28. Series Resistance Current Limiter

The primary drawback of this technique is error introduced by the voltage dropped across R_{CL} under varying load condtions. The % error, as illustrated by the following equations, depends on the R_{CL} and R_L values.

$$I_L = \frac{V_O}{R_L}$$

$$V_O = \frac{V_{O(reg)}}{1 + \frac{R_{CL}}{R_L}}$$

$$\% \text{ ERROR} = \frac{V_{O(reg)} - V_O}{V_{O(reg)}}$$

$$\% \text{ ERROR} = \frac{R_{CL}}{R_L + R_{CL}}$$

Maintaining R_{CL} at a level which is an order of magnitude less than the nominal load impedance minimizes this effect.

$$R_{CL} = \frac{1}{10} R_L \qquad \% \text{ ERROR} = 9.1\%$$

This also yields a short-circuit current that is an order of magnitude greater than the normal operating load current.

$$I_{L(norm)} = \frac{V_{O(reg)}}{R_{CL} + R_{L(norm)}}$$

$$I_{SC} = \frac{V_{O(reg)}}{R_{CL}}$$

$$I_{SC} = 11\ I_{L(norm)}$$

This technique is obviously inefficient since it requires using a regulator or pass element with current capabilities in excess (11X) of its normal operating capabilities. The performance characteristics of a series resistance current limited regulator are illustrated in Figure 29.

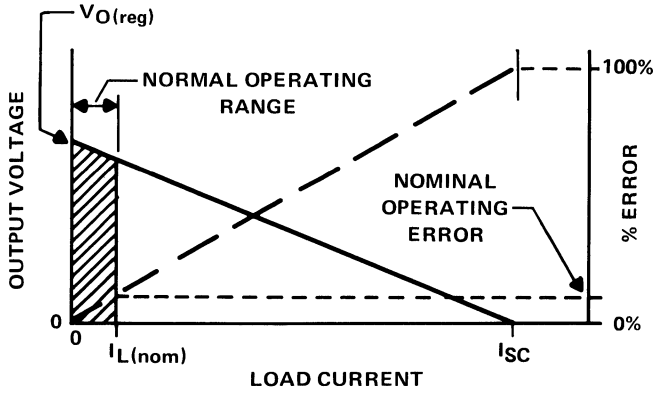


Figure 29. Performance Characteristics of a Series Resistance Current-Limited Regulator

Constant-Current Limiting

Constant-current limiting is the most popular current-limiting technique in low-power, low-current regulator circuits. The basic configuration is illustrated in Figure 30. Note that this method requires access to the control element and remote voltage sense capabilities. By sensing the output voltage beyond the current limiting resistor, the circuit allows the regulator to compensate for the voltage changes across R_{CL}.

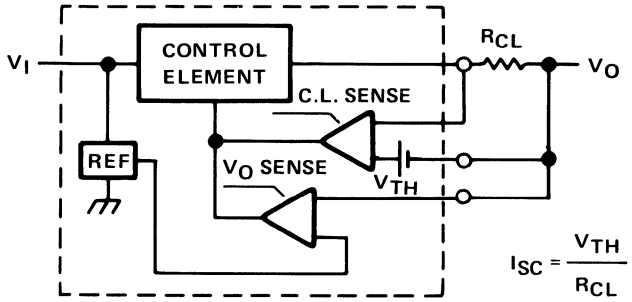


Figure 30. Constant-Current Limit Configuration

If an external pass transistor is used, its base current may be starved to accomplish constant-current limiting, as illustrated in Figure 31. Current limiting takes effect as the voltage drop across R_{CL} approaches the potential required to turn on transistor Q1. As Q1 is biased on, the current supplying the base of Q2 is diverted, thus decreasing the drive current to Q3, the regulator's pass transistor. The performance characteristics of a constant-current limited regulator are illustrated in Figure 32.

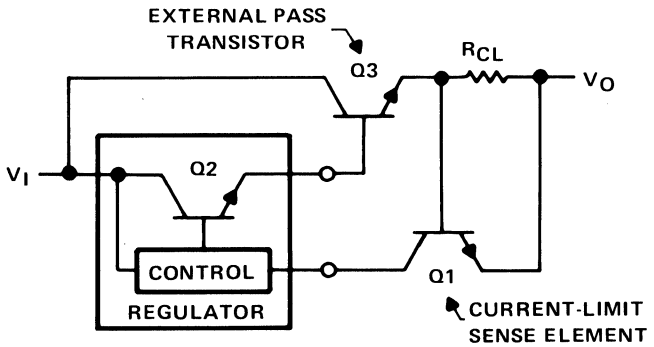


Figure 31. Constant Current Limiting for External Pass Transistor Applications

It should be noted that short-circuit conditions are the worst conditions that can be imposed on the pass transistor since it has to survive not only the short-circuit current, but it has to withstand the full input voltage across its collector and emitter terminals.

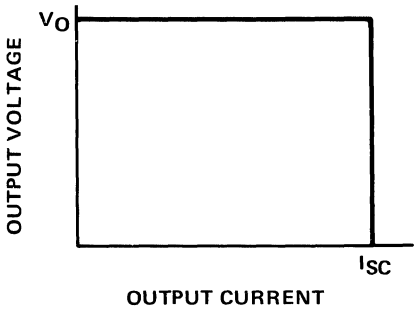


Figure 32. Constant-Current Limiting

This normally requires the use of a pass transistor with power handling capabilities much greater than those required for normal operation i.e.:

$V_I = 20\ V \quad V_O = 12\ V \quad I_O = 700\ mA$

NOMINAL $P_D = (20\ V - 12\ V) \times 0.7\ A = 5.6\ W$

For $I_{SC} = 1\ A (150\%\ I_{OUT})$:

SHORT-CIRCUIT $P_D = 20\ V \times 1\ A = 20\ W$

This requirement may be reduced by the application of fold-back current limiting.

Fold-Back Current Limiting

Fold-back current limiting is used primarily for high-current applications where the normal operating requirements of the regulator dictate the use of an external power transistor. The performance characteristics of a fold-back current limiting regulator are illustrated in Figure 33. The principle of fold-back current limiting provides limiting at a predetermined current (I_K). At this predetermined current, feedback reduces the load current as the load continues to increase (R_L decreasing) and causes the output voltage to decay.

The fold-back current-limiting circuit of Figure 34, behaves in a manner similar to the constant-current limit circuit illustrated in Figure 31. In Figure 34, the potential developed across the current limit sense resistor (R_{CL}) must not only develop the base-emitter voltage required to turn on Q1, but it must develop sufficient potential to overcome the voltage across resistor R1.

$$V_{BE(Q1)} = R_{CL}I_L - \frac{V_O + R_{CL}I_L}{R1 + R2} \times R1$$

$$\therefore I_K = \frac{V_{BE(Q1)}\,(R1 + R2) + V_O R1}{R_{CL}R2}$$

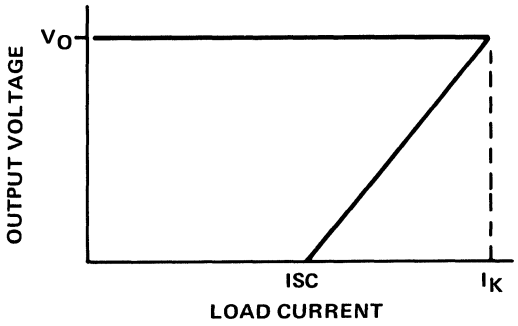


Figure 33. Fold-Back Current Limiting

As the load current requirement increases above I_K, the output voltage (V_O) decays. The decreasing output voltage results in a proportional decrease in voltage across R1. Thus, less current is required through R_{CL} to develop sufficient potential to maintain the forward-biased condition of Q1. This can be seen in the above expression for I_K. As V_O decreases, I_K decreases. Under short-circuit conditions, ($V_O = 0$) I_K becomes:

$$I_{SC} = I_K \text{ @ } (V_O = 0) = \frac{V_{BE(Q1)}}{R_{CL}} \left[1 + \frac{R1}{R2} \right]$$

The approach illustrated in Figure 34 allows a more efficient design because the collector current of the pass transistor is less during short-circuit conditions than it is during normal operation. This means that during short-circuit conditions, when the voltage across the pass transistor is maximum, the collector-emitter current is reduced. As illustrated in Figure 35, fold-back current limiting fits closer to the typical performance characteristics of the transistor, thus allowing a better design match of the pass transistor to the regulator.

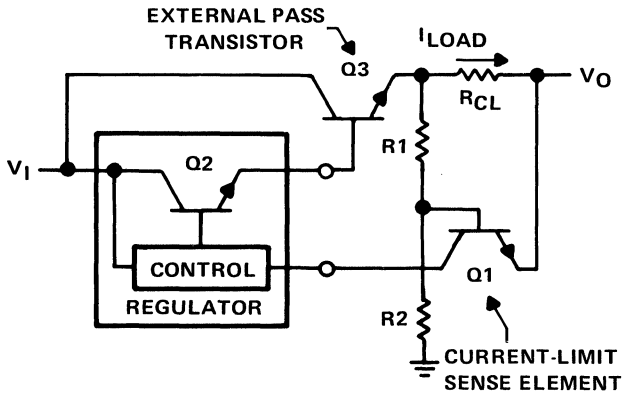


Figure 34. Fold-Back Current Limit Configuration

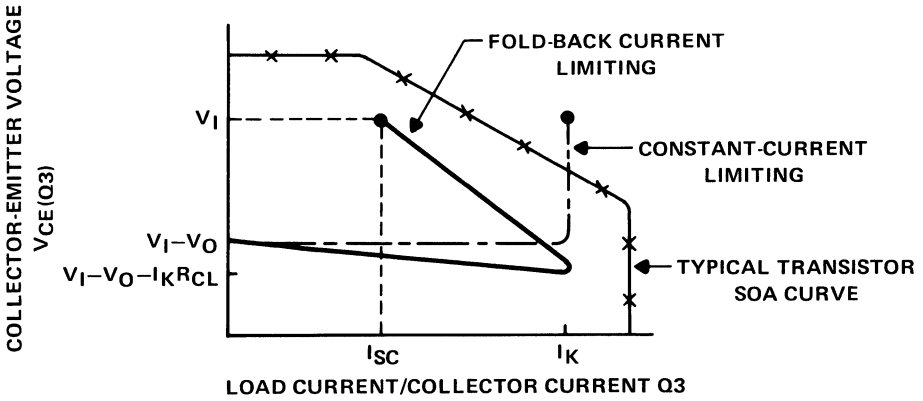


Figure 35. Fold-Back Current Limit Safe Operating Area

Three-Terminal Regulators

Three-terminal IC regulators have been especially useful to the designer of small, regulated power supplies or on-card regulators. Three-terminal regulators are popular because they are small and require a minimum number of external components.

Stabilization

Mounting and using three-terminal regulators usually presents no problem, however, there are several precautions that should be observed. Positive regulators, in general, use n-p-n emitter follower output stages whereas negative regulators use n-p-n common-emitter stages with the load connected to the collector. The emitter follower output stage configuration is not used in negative regulators because monolithic p-n-p series-pass transistors are more difficult to make. Due to their output stage configuration, positive regulators are more stable than negative regulators. Therefore, the practice of bypassing positive regulators may be omitted in some applications. It is good practice, however, to use bypass capacitors at all times.

For a positive regulator, a 0.33-μF bypass capacitor should be used on the input terminals. While not necessary for stability, an output capacitor of 0.1 μF may be used to improve the transient response of the regulator. These capacitors should be on or as near as possible to the regulator terminals. See Figure 36.

When using a negative regulator, bypass capacitors are a must on both the input and output. Recommended values are 2 μF on the input and 1 μF on the output. It is considered good practice to include a 0.1-μF capacitor on the output to improve the transient response (Figure 37). These capacitors may be mylar, ceramic, or tantalum, provided that they have good high frequency characteristics.

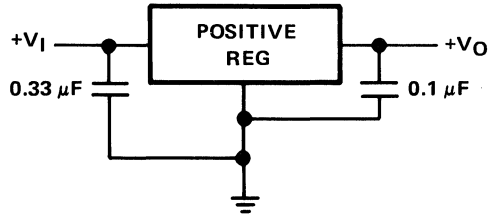


Figure 36. Positive Regulator

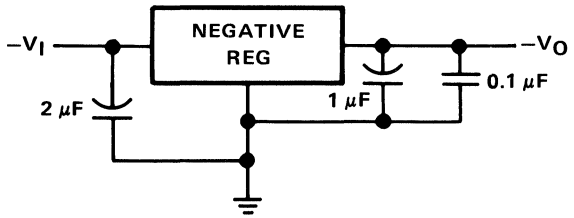


Figure 37. Negative Regulator

Fixed Dual Regulators

When building a dual power supply with both a positive and a negative regulator, extra precautions should be taken. If there is a common load between the two supplies, latch-up may occur. Latch-up occurs because a three-terminal regulator does not tolerate a reverse voltage of more than one-diode drop. To prevent this latch-up problem, it is good design practice to place reversed-biased diodes across each output of a dual supply. While the diodes should not be necessary if the dual regulator outputs are referenced to ground, latch-up may occur at the instant power is turned on, especially if the input voltage to one regulator rises faster than the other. This latch-up condition usually affects the positive regulator rather than the negative regulator. These diodes prevent reverse voltage to the regulator and prevent parasitic action from taking place when the power is turned on. The diodes should have a current rating of at least half the output current. A recommended circuit for a dual 15-V regulated supply is illustrated in Figure 38.

In Figure 38, 1N4001 diodes are placed directly across the regulators, input to output. When a capacitor is connected to the regulator output, if the input is shorted to ground, the only path for discharging the capacitor normally is back through the regulator. This could be (and usually is) destructive to the regulator. The diodes across the regulator divert any discharge current, thus protecting the regulator.

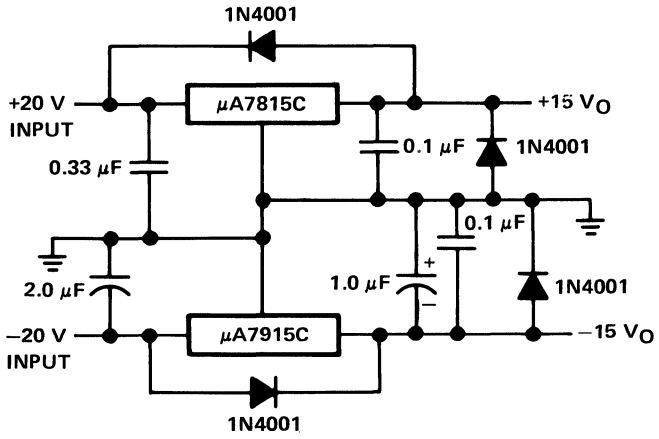


Figure 38. Regulated Dual Supply

Series Adjustable Regulator

Figure 39 illustrates a typical circuit for an LM317 adjustable positive regulator with the output adjustable from 1.2 V to 17 V and up to 1.5 A of current. (A typical input supply uses a 25.2-V transformer and a full-wave bridge rectifier.)

Stabilization, as described earlier for fixed three-terminal regulators, is usually not required. Although the LM317 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This effect occurs with values between 500 pF and 5000 pF. Using a 10-μF aluminum electrolytic on the output swamps this effect and ensures stability.

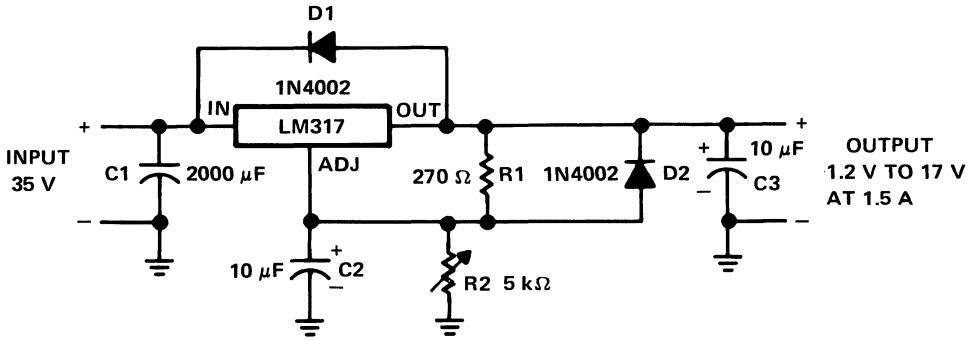


Figure 39. Positive Adjustable Series Regulator

C1 is the power supply filter capacitor following the rectifier section and should be connected close to the regulator input for maximum stability. If the input were to be shorted, D1 would divert the discharge current around the regulator, protecting it. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes. In general, a diode should be used in the position occupied by D1 on all positive regulators to prevent reverse biasing. This becomes more important at higher output voltages since the energy stored in the capacitors is larger. Bypassing the adjustment terminal (C2) improves ripple rejection. Output capacitor C3 is added to improve the transient response of the regulator.

In both the negative (LM337) and the positive (LM317) series adjustable regulators, there is an internal diode from the input to the output. If the total output capacitance is less than 25 μF, D1 may be omitted.

Layout Guidelines

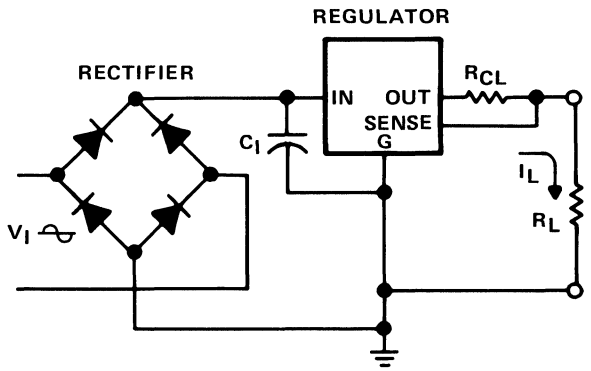
As implied in the previous sections, component layout and orientation plays an important, but often overlooked, role in the overall performance of the regulator. The importance of this role depends upon such things as power level, the type of regulator, the overall regulator circuit complexity, and the environment in which the regulator operates. The general layout rules, as well as remote voltage sensing, and component layout guidelines are discussed in the following text.

Layout Design Factors

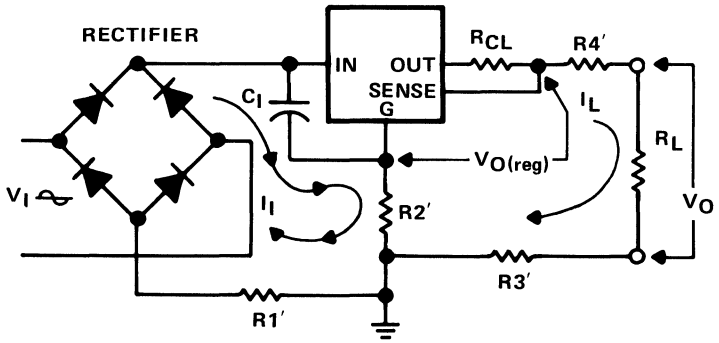
Most integrated circuit regulators use wide-band transistors to optimize their response. These regulators must be compensated to ensure stable closed-loop operation. This compensation can be counteracted by a layout which has excess external stray capacitance and line inductance. For this reason, circuit lead lengths should be held to a minimum. Lead lengths associated with external compensation or pass transistor elements are of primary concern. These components, especially, should be located as close as possible to the regulator control circuit. In addition to affecting a regulator's susceptibility to spurious oscillation, the layout of the regulator also affects its accuracy and performance.

Input Ground Loop

Improper placement of the input capacitor can induce unwanted ripple on the output voltage. Care should be taken to ensure that currents in the input circuit do not flow in the ground line that is in common with the load return. This would cause an error voltage resulting from the peak currents of the filter capacitor flowing through the line resistance of the load return. See Figure 40 for an illustration of this effect.



(a) TYPICAL LAYOUT



(b) LAYOUT ERROR CONTRIBUTIONS

Figure 40. Circuit Layout Showing Error Contributions

Output Ground Loop

Similar in nature to the problem discussed on the input, excessive lead length in the ground return line of the output results in additional error. Because the load current flows in the ground line, an error equivalent to the load current multiplied by the line resistance (R3′) will be introduced in the output voltage.

Remote Voltage Sense

The voltage regulator should be located as close as possible to the load. This is true especially if the output voltage sense circuitry is internal to the regulator's control device. Excessive lead length will result in an error voltage developed across the line resistance (R4').

$$V_O = V_{O(reg)} - (R2' + R3' + R4')\, I_L + R2'\, I_{reg}$$

$$\text{ERROR} = I_L(R3' + R4') - I_{reg}R2'$$

If the voltage sense is available externally, the effect of the line resistance can be minimized. By referencing the low current external voltage sense input to the load, losses in the output line are compensated. Since the current in the sense line is very small, error introduced by its line resistance is negligible (Figure 41).

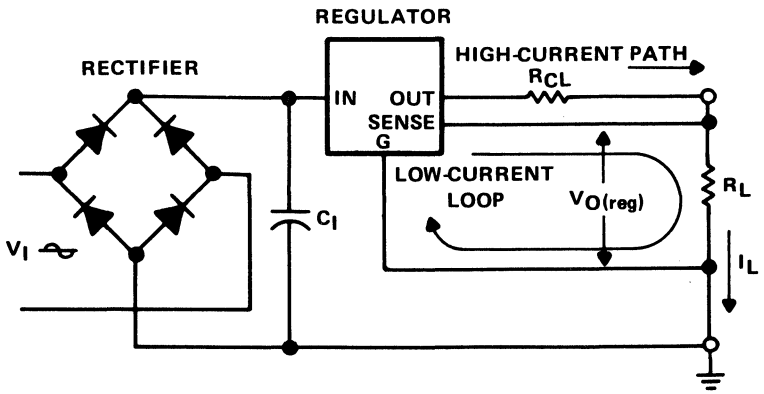


Figure 41. Proper Regulator Layout

Input Supply Design

When the power source is an ac voltage, the transformer, rectifier, and input filter design are as important as the regulator design itself for optimum system performances. This section presents input supply and filter design information for designing a basic capacitor input supply.

Transformer/Rectifier Configuration

The input supply consists of three basic sections: (1) input transformer, (2) rectifier, and (3) filter as illustrated in Figure 42. The first two sections, the transformer and the rectifier, are partially dependent upon each other because the structure of one depends upon that of the other. The most common transformer configurations and their associated rectifier circuits are illustrated in Figure 43.

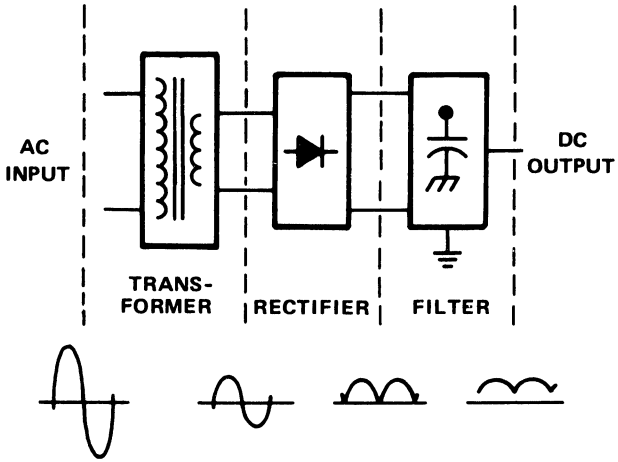
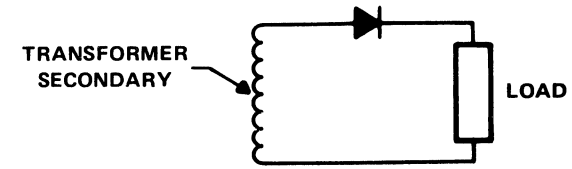
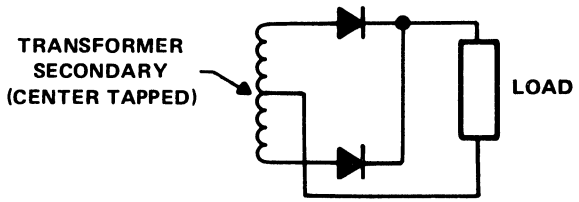


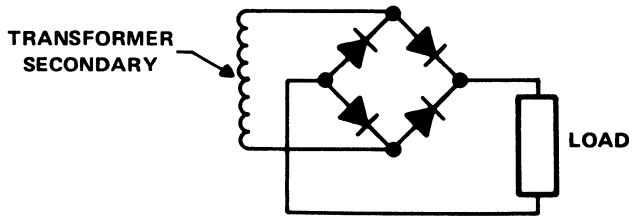
Figure 42. Input Supply



(a) SINGLE-PHASE HALF-WAVE



(b) SINGLE-PHASE CENTER-TAPPED FULL-WAVE



(c) SINGLE-PHASE FULL-WAVE BRIDGE

Figure 43. Input Supply Transformer/Rectifier Configurations

The particular configuration used depends upon the application. The half-wave circuit [Figure 43(a)] is used in low-current applications. This is because the single rectifier diode experiences the total load current and its conversion efficiency is less than 50%. The full-wave configurations [Figure 43(b) and 43(c)] are used for higher current application. The characteristic output voltage waveforms of these configurations are illustrated in Figure 44.

Figure 44. Rectifier Output-Voltage Waveforms

Before the input supply and its associated filter can be designed, the voltage, current, and ripple requirements of its load must be fully defined. The load, as far as the input supply is concerned, is the regulator circuit. Therefore, the input requirements of the regulator itself become the governing conditions. Because the input requirements of the regulator control circuit govern the input supply and filter design, it is easiest to work backwards from the load to the transformer primary.

Capacitor Input Filter Design

The most practical approach to a capacitor-input filter design remains the graphical approach presented by O.H. Schade[1] in 1943. The curves illustrated in Figures 45 through 48 contain all of the design information required for full-wave and half-wave rectifier circuits.

Figures 45 and 46 illustrate the ratio of the dc-output voltage developed (V_C) to the applied peak input voltage ($V_{(PK)}$), as a function of ωCR_L for half-wave and full-wave rectified signals, respectively. For a full-wave rectified application, the voltage reduction is less than 10% for $\omega CR_L > 10$ and $R_S/R_L < 0.5\%$. As illustrated, the voltage reduction decreases as ωCR_L increases or the R_S/R_L ratio decreases. Minimizing the reduction rate, contrary to initial impressions, may prove to be detrimental to the optimum circuit design. Further reduction requires a reduction in the series to load resistance ratio (R_S/R_L) for any given ωCR_L. This will result in a higher peak-to-average current ratio

[1]O.H. Schade, "Analysis of Rectifier Operation", *Proc. IRE.*, VOL. 31, 343, 1943.

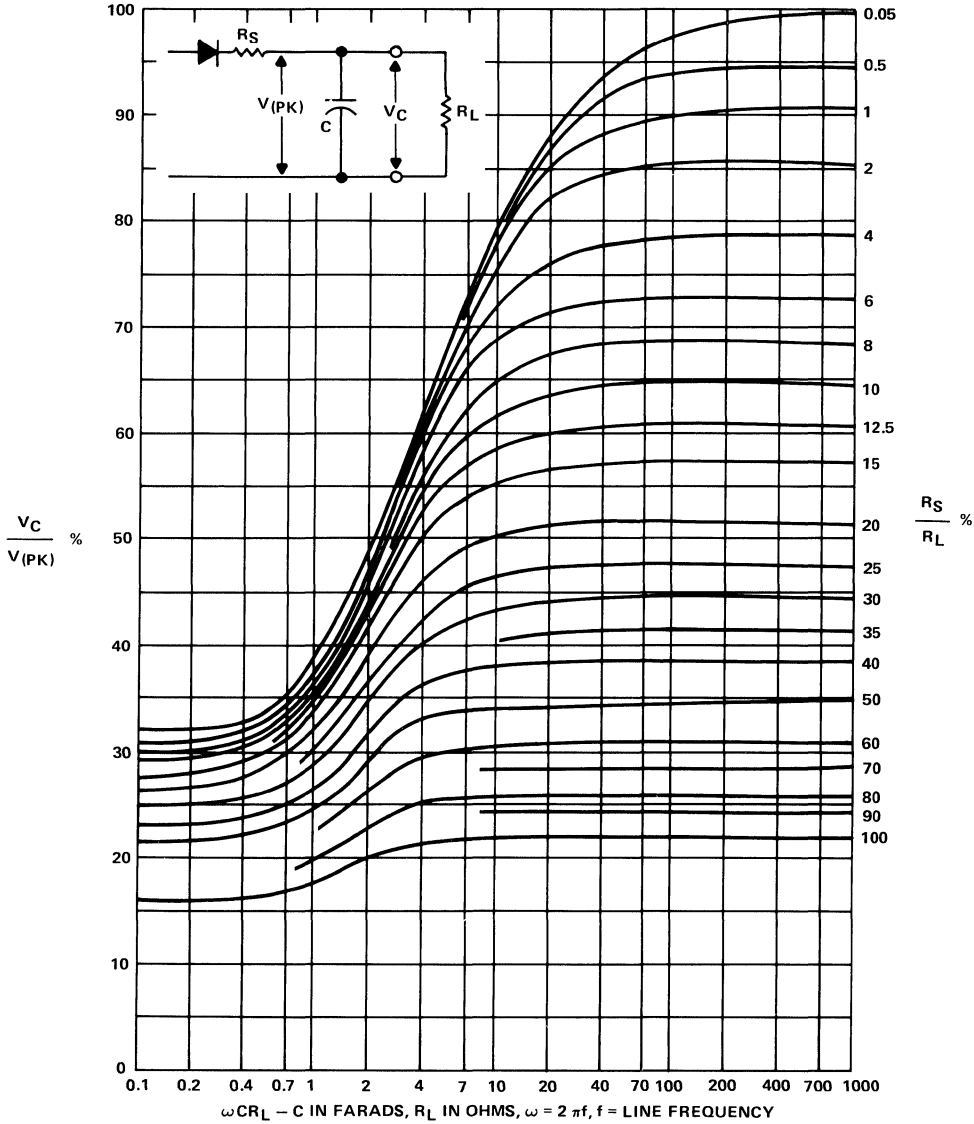


Figure 45. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits (From O.H. Schade, *Proc. IRE*, Vol. 31, p. 343, 1943)

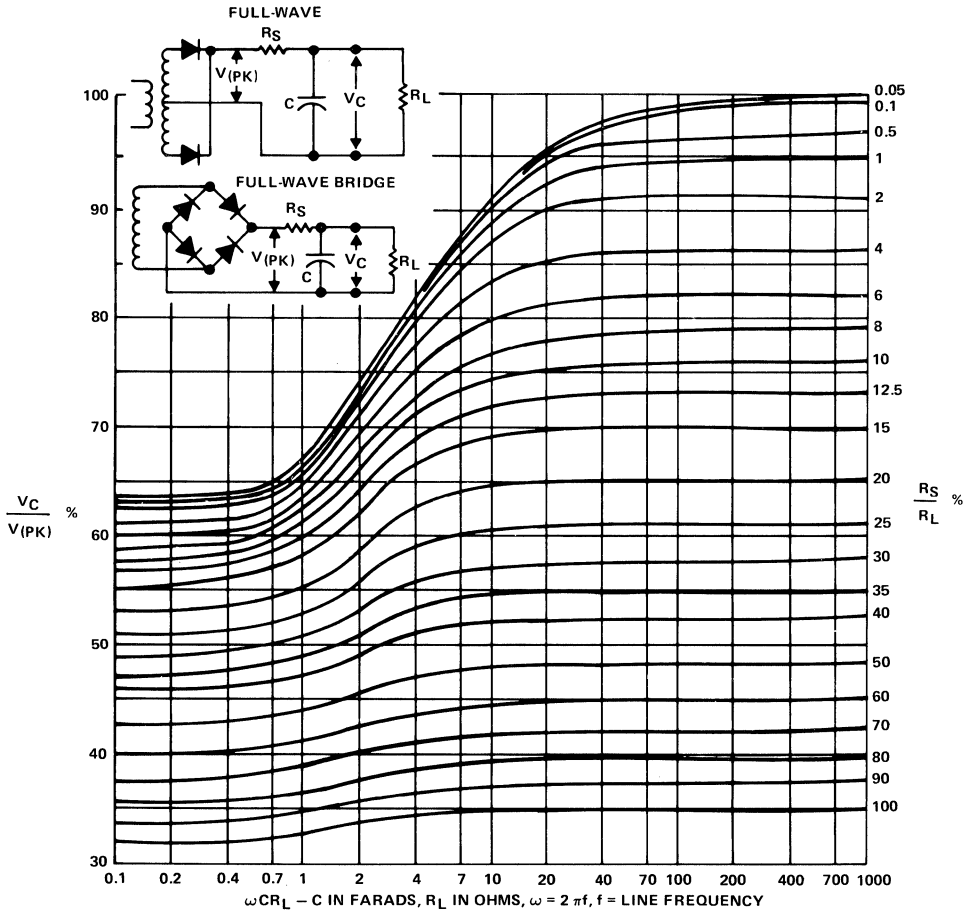
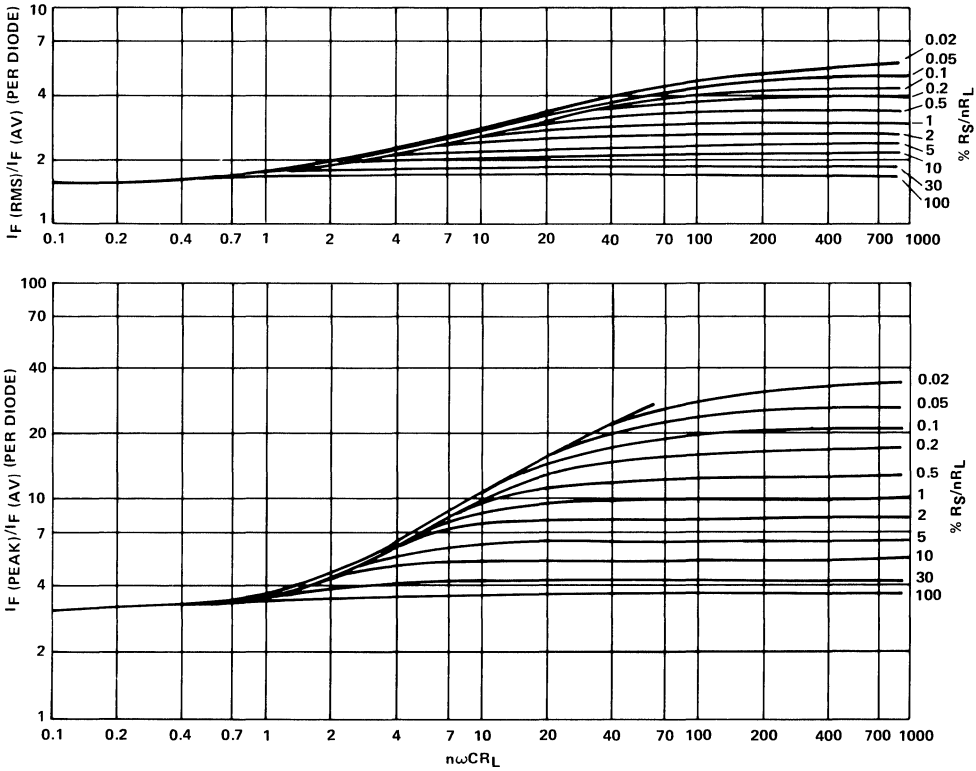


Figure 46. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full-Wave Capacitor-Input Circuits (From O.H. Schade, *Proc. IRE*, Vol. 31, p. 344, 1943)

through the rectifier diodes (see Figure 47). In addition, and probably of more concern, this increases the surge current experienced by the rectifier diodes during turn-on of the supply. It is important to realize that the surge current is limited only by the series resistance R_S.

$$I_{SURGE} = \frac{V_{SEC(PK)}}{R_S}$$



n = 1 (FOR HALF-WAVE SINGLE PHASE RECTIFIER CIRCUITS) or
n = 2 (FOR FULL-WAVE SINGLE PHASE RECTIFIER CIRCUITS)
$\omega = 2\pi f$ = LINE FREQUENCY

C IN FARADS
R_L IN OHMS
R_S = RMS EQUIVALENT SOURCE RESISTANCE

Figure 47. Relation of RMS and Peak-to-Average Diode Current in Capacitor-Input Circuits (From O.H. Schade, *Proc. IRE*, Vol. 31, p. 345, 1943)

In order to control the surge current, additional resistance is often required in series with each rectifier. It is evident that a compromise must be made between the voltage reduction and the rectifier current ratings. The maximum instantaneous surge current is $V_{(pk)}/R_S$. The time constant (τ) of capacitor C is $\tau \cong R_S C$. As a rule of thumb, the surge current will not damage the diode if: $I_{SURGE} < I_{F(SURGE)max}$ and $\tau < 8.3$ ms

Figure 48 illustrates the relationships between the ripple factor r_f, ωCR_L, and R_S/R_L. The ripple factor is the ratio of the rms value of the ripple component of the output voltage, expressed as a percent of the nominal dc output voltage.

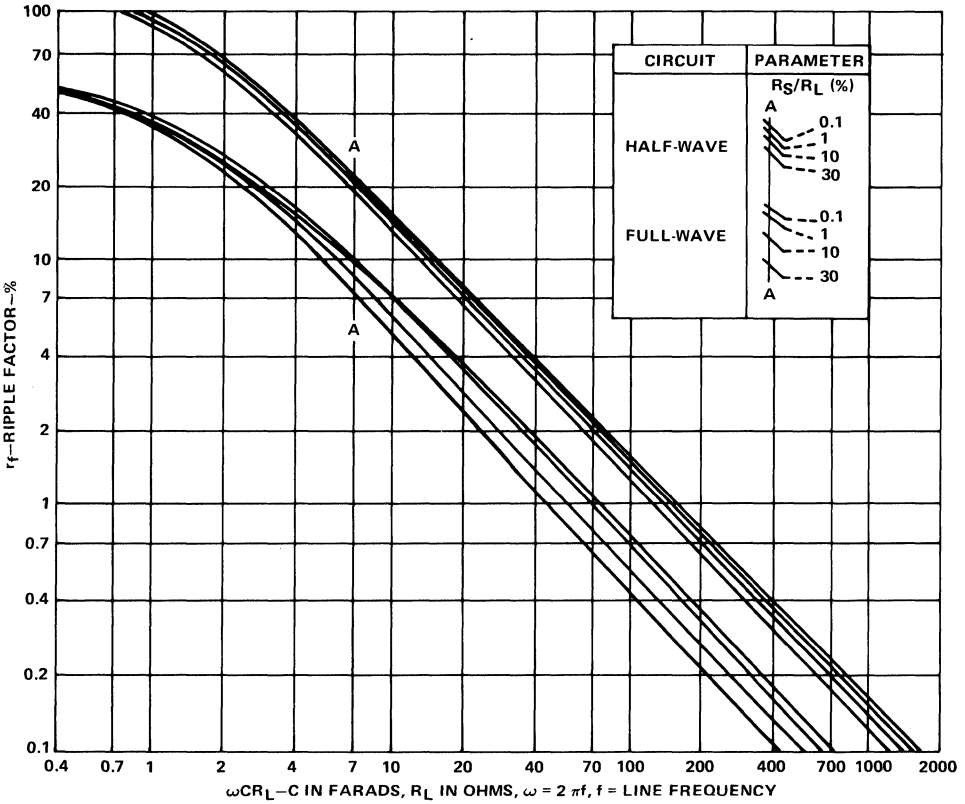


Figure 48. Root-Mean-Square Ripple Voltage for Capacitor-Input Circuits (From O.H. Schade, *Proc. IRE*, Vol. 31, p. 346, 1943)

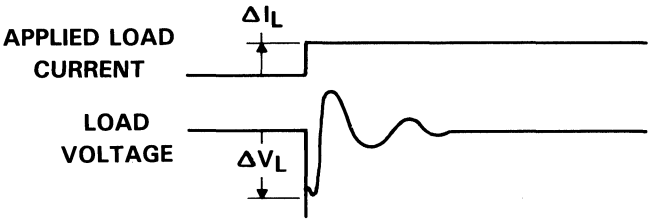
Low Drop-Out Voltage Regulator Design Considerations

Low drop-out (LDO) regulators have increased in popularity during the past five years. This design consideration discusses the special requirements that LDO applications users should consider to obtain optimum operations.

The LDO regulator design is characterized by a large geometry PNP output transistor that is used to conduct the power from input to output. This configuration places the collector at the output while reducing the overhead voltage required to drive the output transistor. Since the output impedance of the collector is several thousand ohms, a high open loop gain must be maintained to reach the necessary MΩ requirements of a voltage regulator. In addition, the high-impedance collector reactive-load elements can introduce low-frequency-phase shifts and control-loop instability. The LDO control loop is designed to accept a minimum capacitive loading (approximately 10 μF) for complete stablization for the low-power LDO (TL750LXX series) regulators. The medium-power regulators TL750MXX series introduced additional requirements because of the wide range of restistive loading (5 Ω to infinity) that have resulted in a broad frequency swing in loop-phase shift and restrictions in the value of the load capacitor. Some assumptions have been made on the range of the Equivalent Series Resistance (ESR) the load capacitor should exhibit in certain applications. The ESR would cancel the phase shift at some of the higher frequencies and allow the regulator design to have internal fixed-stability compensation. This compensation allows the load capacitor value to vary from the minimum to a greater than value. The assumed ESR is approximately 0.5 Ω (polarized solid tantalum to be used in this range) derived from studies of the ESR of the standard available capacitors at the minimum value. Actual response curves for the TL750MXX series are shown in Figure 49. To justify these assumptions, the following conditions must be stated:

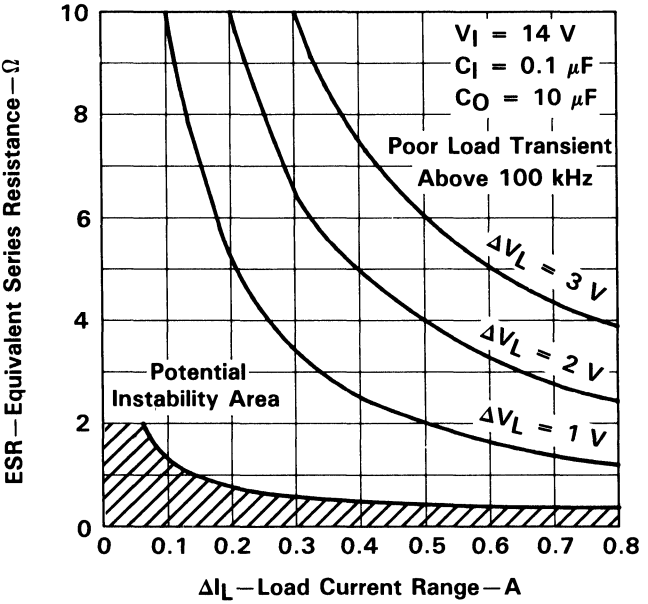
1. The ESR of the capacitor is directly related to the application (wiring resistance of regulator and load increases the ESR).
2. The loop will become unstable if the ESR is forced too low.
3. The stability will improve with an increase in load-capacitor value.

Caution must be exercised in some medium-power LDO applications that require stable regulation over a large load range because mV-level oscillations may be exhibited at the higher load-resistance ranges. To eliminate the oscillations, a larger capacitor value (approximately 100-μF maximum) should be selected or the ESR value should be increased (to approximately 2 Ω). The circuit bandwidth is decreased by the larger value capacitor and the loop bandwidth is increased with the higher ESR. This provides a faster transient load response and offsets some of the loss from the capacitor ESR.



(a) TYPICAL LOAD TRANSIENT RESPONSE

EQUIVALENT SERIES RESISTANCE OF OUTPUT CAPACITOR
VS
LOAD CURRENT RANGE



(b) ESR vs LOAD CURRENT

Figure 49. Typical Response Curves for the TL750MXX Series

Thermal Considerations in Design of Power Supplies

Introduction

Power supply circuit designers place emphasis on suppressing transients, improving regulation, and increasing efficiency, yet concentrate minimum effort toward thermal considerations and packaging of the power supply. Serious efforts must be given to thermal design and packaging to minimize power supply failures in the field. If sufficient attention is given to the important parameters supplied by the semiconductor manufacturers (e.g., maximum junction temperature, junction-to-case, and junction-to-ambient thermal resistance), proper heat removal can be achieved. Thermal resistance is the temperature difference between two points divided by the power dissipation, normally stated in °C/W. The reference temperature can be the ambient temperature or the temperature of a heat sink that the integrated circuit (IC) package is attached to.

Heat can be transferred from the transistor or integrated circuit package by three methods; conduction, convection, and radiation.

Conduction is transmission of energy by a medium not involving movement of the medium itself. This method is predominate in junction to the case or from the case to a heat sink heat transfer from the semiconductor. Length, cross-section, and temperature differential of the medium are key parameters that determine conduction.

Convection is transmission of energy or mass by a medium involving movement of the medium itself. This method predominates in the transfer of heat from the case to ambient or a heat sink to ambient. Surface conditions, convecting fluids, velocity, and temperature difference are dominant factors in convection.

Radiation is the emission and propagation of waves transmitting energy through space or some medium. This method is important in heat transfer from the cooling-fin surface of a heat sink. Thermal emissivity, surface-area, and temperature difference between radiating and adjacent mediums are key factors that determine radiation.

Basic Thermal Circuit and Symbols

Figure 50 illustrates the various heat flow paths, temperatures, and thermal resistances of a steady-state thermal model using a KC package with formed leads. A popular concept is to display this thermal model as a network of series resistors as shown on Figure 51, comparing the thermal circuit analogy to an electric circuit. Extending this Ohm's-law concept of this thermal circuit, temperature is analogus to voltage and thermal resistance to ohmic resistance. Inspection of Figure 51 will provide an expression for:

$$T_J = T_A + P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (1)$$

or $T_J = T_A + P_D(R_{\theta JA})$ for a regulator without external heat sink

where

T_J = junction temperature in °C
T_A = ambient air temperature in °C
$R_{\theta JC}$ = thermal resistance, junction-to-case in °C/W
$R_{\theta CS}$ = thermal resistance, case-to-heat sink °C/W
$R_{\theta SA}$ = thermal resistance, heat sink-to-ambient in °C/W
$R_{\theta JA}$ = thermal reaistance, junction to ambient °C/W
P_D = power dissipated by semiconductor device in W

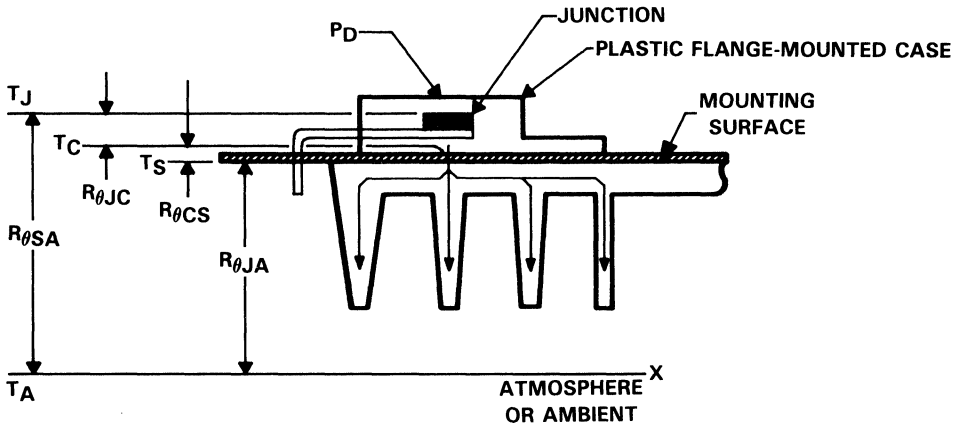


Figure 50. Semiconductor Thermal Model

The junction-to-ambient thermal resistance $R_{\theta JA}$ can be expressed as a sum of thermal resistances listed below:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (2)$$

Equation 2 is applicable only when an external heat sink is used. If only a mounting (internal) heat sink is used, or the device does not have a heat sink, the $R_{\theta JA}$ is equal to the $R_{\theta JA}$ specified on the product data sheet. $R_{\theta JC}$ normally will be given on the data sheet also, and the junction-to-case thermal resistance is a function of the material, and size of the package, die area and thickness, and integrity of the die bond to the case, lead frame, or chip carrier. $R_{\theta CS}$ depends on the package, heat-sink-interface (mounting of the regulator to the heat sink) area, and integrity of the contact surface. Typical values for $R_{\theta CS}$ for different packages are shown in Table 1.

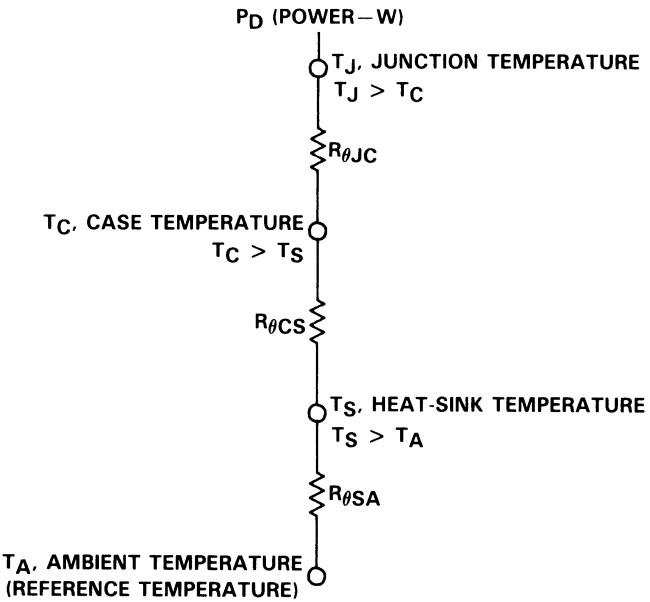


Figure 51. Basic Semiconductor Heat Sink Steady State Thermal Circuit

Table 1. $R_{\theta CS}$ for Different Types of Packages and Mounting Conditions

PACKAGE	METAL TO METAL	METAL-TO-METAL WITH THERMAL COMPOUND	CONTACT WITH MICA WASHER AND THERMAL COMPOUND†
TO-3	0.52 °C/W	0.14 °C/W	0.36 °C/W
KC (TO-220)	1.1 °C/W	1.0 °C/W	1.7 °C/W

†Typical values extracted from heat-sink manufacturer's curves

The $R_{\theta SA}$ found on the heat sink data sheets depends on the attributes of the heat sink and the ambient conditions. Convection and radiation are heat flow methods affecting the heat sink to ambient thermal resistance.

Typically, the ambient temperature (T_A), maximum junction temperature (T_J), power dissipation (P_D), thermal resistance from junction-to-case ($R_{\theta JC}$), and thermal resistance from junction to ambient air ($R_{\theta JA}$) are known. To ensure safe operations of any semiconductor, the device junction temperature must be maintained below the maximum value given on the product data sheet. As with any semiconductor component, these devices have thermal and electrical limitations that must be adhered to if desired performance and service time are to be achieved. In addition, improved reliability can be obtained by selecting conservative operating procedures and thermal ranges. Normally, the electrical and thermal characteristics are interrelated with the actual operating ranges that are heavily dependent on the component application.

Thermal Design Examples

The following examples are given to illustrate the design procedure in:

1. Ascertaining the maximum allowable power dissipation of a semiconductor device
2. Determining the maximum junction-to-ambient air temperature ($T_A$max) using a mounting (internal) heat sink, or regulator without internal heat sink
3. Selecting an external heat sink by calculating the heat sink-to-ambient thermal resistance ($R_{\theta SA}$).

To ascertain the maximum allowable power dissipation of a semiconductor device, use equation 3:

$$P_D = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \tag{3}$$

$$P_D = \frac{150\,°C - 75\,°C}{121.95\,°C/W} = 0.62\ W$$

where

$T_{Jmax} = 150\,°C$ (design limit)
$T_A = 75\,°C$
$R_{\theta JA}$ = 1/derating value = 1/8.2 mW/°C (DW package) = 121.95 °C/W
$T_{Jmax} = T_A + P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$

To ascertain the maximum T_A for an uA78M12C regulator with an internal heat sink, use equation 4:

$$T_J = T_A + P_D(R_{\theta JA}) \tag{4}$$
$$T_A = T_J - P_D(R_{\theta JA})$$
$$T_A = 125 - (0.8 \times 62.5)$$
$$T_A = 75\,°C$$

where

$P_D = 0.8$ W
$T_J = 125\,°C$
$R_{\theta JA}$ = 1/derating factor $= 1/0.016 = 62.5\,°C/W$
Derating factor of KC (TO-220) package is 16 mW/°C (from uA78M12C data sheet)

To ascertain the heat sink-to-ambient thermal resistance ($R_{\theta SA}$) for selection of external heat sink using the uA7915C regulator, the heat sink should be mounted metal-to-metal using thermal compound.

$$R_{\theta SA} = \frac{T_J - T_A}{P_D} - R_{\theta JC} - R_{\theta CS} \qquad (5)$$

$$R_{\theta SA} = \frac{125 - 75}{3} - 4 - 1 = 11.7\,°C/W$$

where

$P_D = 3$ W
$T_J = 125\,°C$
$T_A = 75\,°C$
$R_{\theta JC} = 4\,°C/W$ (from the uA7915C data sheet)
$R_{\theta CS} = 1\,°C/W$ from Table 1 (KC or TO-220 case).

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

A Thermalloy 7019 or Staver V3-5 heat sink will meet the desired requirements (see Table 3).

Table 2. Available Heat Sinks for TO-3 Packages

$R_{\theta SA}$ RANGE† °C/W	MANUFACTURER‡	
	STAVER	THERMALLOY
3 to 5	V3-5-2	6004,6053,6054,6214,6216
5 to 8	V3-3-2	6002, 6003, 6015, 6016, 6052, 6060, 6061, 6213
8 to 13	V1-3,V1-5,V3-3,V3-5,V3-7-96	6001, 6013, 6014, 6051

†All values are typical as determined from characteristic curves received from manufacturers.
‡This table is a representative of two heat sink manufacturers, many others are available.

Table 3. Available Heat Sinks for KC (TO-220) Packages

$R_{\theta SA}$ RANGE† °C/W	MANUFACTURER‡	
	STAVER	THERMALLOY
3 to 5	V3-5-2	6072/6071
5 to 8	V3-3-2	6072, 7021, 7025
8 to 13	V3-3, V3-5	6021, 6030, 6032, 7019, 7020

†All values are typical as determined from characteristic curves received from manufacturers.
‡This table is a representative of two heat sink manufacturers, many others are available.

General Suggestions for Efficient Thermal Management

Suggestions are as follows:

1. Place regulator components away from heat-dissipating components and mount hardware in an area that provides a good heat-dissipation path for the regulator.
2. For applications requiring electrical insulation of the heat-sink from the regulator use a thin (0.003 inch) mica washer. A thermal lubricant must be placed on both sides of the washer.
3. If a heat sink with fins is used with the regulator, align the fins in a vertical plane for a more efficient transfer of heat.
4. Select heat sink with a mounting surface that has a finish and flatness comparable to the regulator package. Use thermal compounds to minimize voids, scratches, and imperfections between the mating surfaces. Use of thermal compounds with an insulating washer is more significant than with a metal-to-metal contact.
5. Attach regulator heat sink to the regulator before soldering and mounting on the PC board. Maximum lead temperatures are 260 °C for ten seconds with plastic packages or 300 °C for sixty seconds for cermanic packages at a distance of 1/16th inches from case.

Conclusion

Thermal considerations in the design of power supplies are straight-forward, and with emphasis on heat reduction and conservative operating techniques, more efficient and reliable designs will be realized. The design parameters are normally under the control of the circuit designer and, with compromises, the variables can be controlled to achieve a product that will experience fewer failures in the field. On the other hand, if the thermal design considerations are overlooked or minimized, many of the power supply failures in the field may result from an inadequate thermal design approach.

Switching Power Supply Design

TEXAS INSTRUMENTS

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Introduction

Modern electronic equipment usually requires one or more dc power sources. The usual method of supplying dc power is a power supply which converts ac power to dc power. The two types of dc power supplies in common use are classified by the type of regulator employed; linear regulator and switching regulator.

Linear power supplies consist of a power transformer, rectifier and filter circuits, and a linear regulator. Switching power supplies do not require line transformers; the ac input is rectified and filtered, chopped by a high frequency transistor switch/transformer combination, then rectified and filtered again.

Switching power supplies have been used for some time in the military and space industry due to their smaller size and higher efficiency. In 1975, switching power supplies were more cost effective than linear power supplies from approximately the 500-W power level. Now the breakeven point is down to approximately 5 W.

Basic Operation of Switching Regulators

Figure 1 is a block diagram of a typical switching power supply which consists of four basic circuits:

1. Input rectifier and filter
2. High frequency inverter
3. Output rectifier and filter
4. Control circuit.

The ac line voltage is applied to an input rectifier and filter circuit. The dc voltage output from the rectifier and filter circuit is switched to a higher frequency (typically 25 kHz to 100 kHz) by the transistor switch in the high frequency inverter circuit. This circuit contains either a high frequency transformer or inductor, depending on the output voltage required.

Output from the high frequency inverter circuit is applied to the output rectifier and filter circuit. The circuit is monitored and controlled by the control circuit which attempts to keep the output at a constant level.

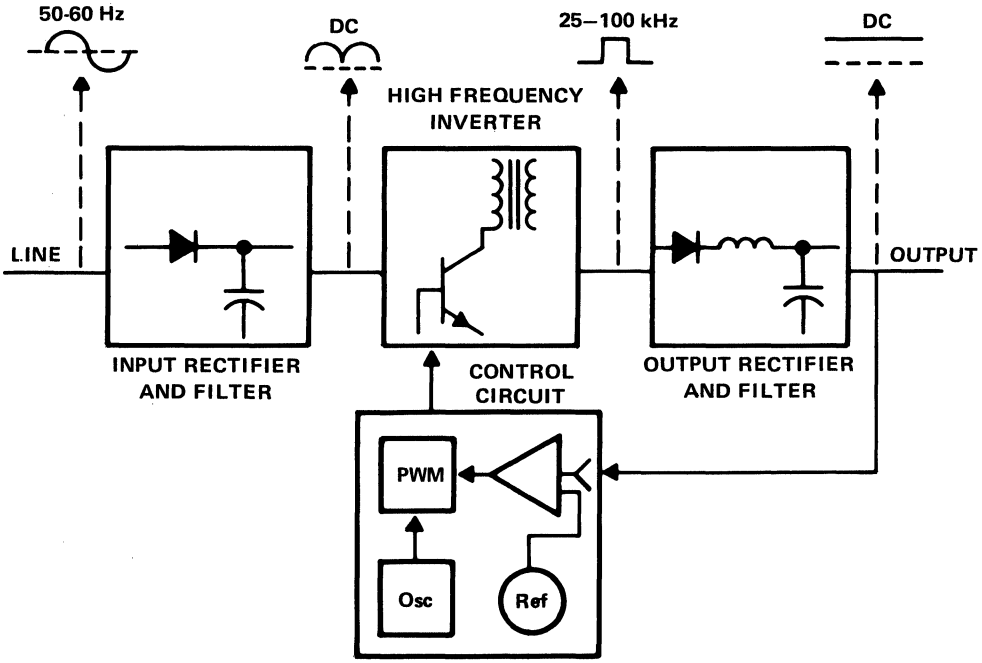


Figure 1. Basic Switching Regulator Block Diagram

The control circuit consists of an oscillator driving a pulse-width modulator, an error amplifier, and a precision voltage reference. The error amplifier compares the input reference voltage with a sample of the voltage from the output rectifier and filter circuit. As the load increases, the output voltage drops. The error amplifier senses this drop and causes the pulse-width modulator to remain on for a longer period of time, delivering wider control pulses to the transistor switch.

The width of the pulse determines how long the transistor switch allows current to flow through the high frequency transformer and, ultimately, how much voltage is available at the output. If the load decreases, narrower control pulses are delivered to the switching transistor until the output voltage remains at a constant value.

Advantages of a Switching Regulator

The primary advantages of switching regulators are higher efficiency and smaller size. Conventional linear series and shunt regulators operate in a continuous conduction mode, dissipating relatively large amounts of power. The efficiency of linear regulators is typically around 40% to 50%. When the input-to-output voltage differential is large, the resultant efficiency is much lower than 40%.

Switching regulators have typical efficiencies of 60% to 90%; much higher than either the linear series or shunt regulator. Switching regulators achieve their higher efficiency as a result of three factors:

1. The power-transistor switch is always turned completely on or off, except when it is switching between these two states, resulting in either low voltage or low current during most of its operation.
2. Good regulation can be achieved over a wide range of input voltage.
3. High efficiency can be maintained over wide ranges in load current.

Switching regulators use the on-off duty cycle of the transistor switch to regulate the output voltage and current. By using a frequency much higher than the line frequency (typically 20 kHz to 500 kHz), the transformers, chokes, capacitors, and other filter elements can be made smaller, lighter, and less costly. The smaller elements used in switching regulators result in smaller power losses than the larger components used in linear regulators. The highest cost elements of a switching power supply are the transistor switches. The remaining costs, in descending order, are due to the magnetic components, capacitors, and rectifiers.

Disadvantages of a Switching Regulator

Switching regulators can generate some electromagnetic and radio frequency interference (EMI/RFI) noise due to high switching currents and short rise and fall times. EMI/RFI noise, which is generated at higher frequencies (100 kHz to 500 kHz), is easily filtered. In those applications where a large series impedance appears between the supply and the regulator, the rapid changes in current also generate a certain amount of noise. These problems may be overcome or significantly reduced by one or more of the following steps:

1. Reducing the series impedance
2. Increasing the switching time
3. Filtering the input and output of the regulator.

Switching regulators with a fixed frequency are easier to filter than regulators with a variable frequency because the noise is at only one frequency. Variable frequency regulators with a fixed "on" time increase or decrease the switching frequency in proportion to load changes, presenting a more difficult filtering problem.

Basic Switching Regulator Architecture

There are three basic switching regulator configurations from which the majority of present day circuits are derived:

1. Step-down or "buck" regulator
2. Step-up or "boost" regulator
3. Inverting or "flyback" regulator (which is a variation of the "boost" regulator).

The Step-Down Regulator

Figure 2 illustrates the basic step-down or "buck" regulator. The output voltage of this configuration is always less than the input voltage. In the buck circuit, a semiconductor switch is placed in series with the dc input from the input rectifier/filter circuit. The switch interrupts the dc input voltage providing a variable-width pulse to a simple averaging LC filter. When the switch is closed, the dc input voltage is applied across the filter and current flows through the inductor to the load. When the switch is open, the energy stored in the field of the inductor maintains the current through the load. In the buck circuit, peak-switching current is proportional to the load current. The output voltage is equal to the input voltage times the duty cycle.

$$V_O = V_I \times \text{Duty Cycle}$$

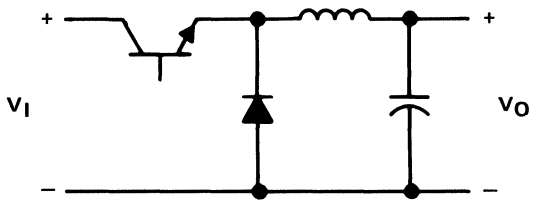


Figure 2. Step-Down or "Buck" Switching Regulator Circuit

The Step-Up Regulator

Another basic switching regulator configuration is the step-up or "boost" regulator (Figure 3). In this type of circuit, the output voltage is always greater than the input voltage. The boost circuit first stores energy in the inductor and then delivers this stored energy along with the energy from the dc input voltage to the load. When the switch is closed, current flows through the inductor and the switch, charging the inductor but delivering no current to the load. When the switch is open, the voltage across the load equals the dc input voltage plus the charge stored in the inductor. The inductor discharges, delivering current to the load.

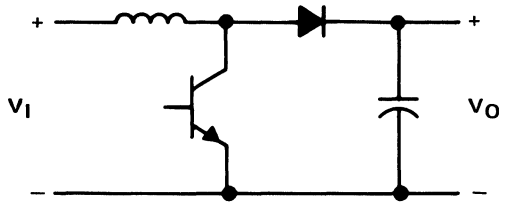


Figure 3. Step-Up or "Boost" Switching Regulator Circuit

The peak switching current in the boost circuit is not related to the load current. The power output of a boost regulator can be determined by the following equation:

$$P_{OUT} = \frac{LI^2f}{2}$$

where:

P_{OUT} = power output
L = inductance
I = peak current
f = operating frequency

The Inverting Regulator

The third switching regulator configuration is the inverting or "flyback" regulator. This circuit is a variation of the step-up or "boost" circuit discussed previously. The flyback circuit is illustrated in Figure 4. Flyback regulators, which evolved from "boost" regulators, deliver only the energy stored by the inductor to the load. This type of circuit can step the input voltage up or down. When the switch is closed, the inductor is charged, but no current is delivered to the load because the diode is reverse biased. When the switch is open, the blocking diode is forward biased and the energy stored in the inductor is transferred through it to the load.

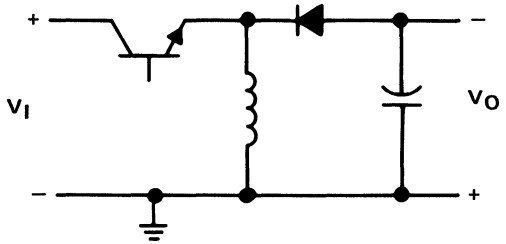


Figure 4. Inverting or "Flyback" Switching Regulator Circuit

The flyback circuit delivers a fixed amount of power to the load regardless of load impedance. It is widely used in photo flash, capacitor-discharge ignition circuits, and battery chargers.

To determine the output voltage of an electronic equipment supply, the load (R_L) must be known. If the load is known, the output voltage may be calculated using the following equation:

$$V_O = \sqrt{P_O R_L} = I\sqrt{\frac{LfR_L}{2}}$$

where:

V_O = voltage output
P_O = power out
R_L = load resistance
I = inductor current
f = operating frequency

The inductor current is proportional to the "on time" (duty cycle) of the switch and regulation is achieved by varying the duty cycle. However, the output also depends on the load resistance (which was not true with the step-down circuit).

Transient response to abrupt changes in the load is difficult to analyze. Practical solutions include limiting the minimum load and using the proper amount of filter capacitance to give the regulator time to respond to this change. Flyback type circuits are used at power levels of up to 100 W.

Forward Converters

The forward converter family, which includes the push-pull and half-bridge circuits, evolved from the step-down or "buck" type of regulator. A typical forward converter circuit is illustrated in Figure 5. When the transistor switch is turned on, the transformer delivers power to the load through diode D1 and the LC filter. When the switch is turned off, diode D2 is forward biased and maintains current to the load.

Without the third winding and diode D3, the converter would lose efficiency at higher frequencies. The function of this winding is to return energy stored in the transformer to the line and reset the transformer core after each cycle of operation. This is a popular low-power (up to about 200 W) converter and is almost immune to transformer saturation problems.

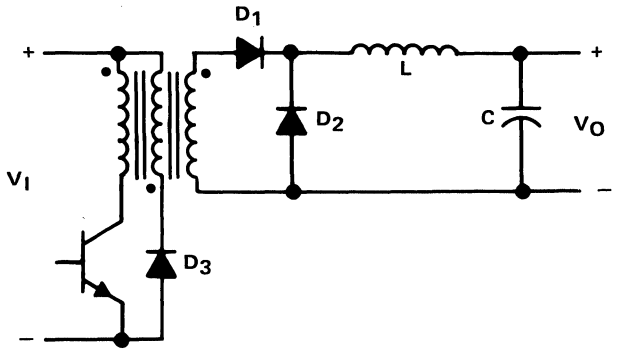


Figure 5. Forward Converter Switching Regulator

Push-Pull Converter

The push-pull converter is probably one of the oldest switching regulator type circuits. It was first used in the 1930s with mechanical vibrators functioning as the switch. When transistors became available, push-pull converters were used as free-running oscillators in the primary of many automobile communication converters. Some recreational vehicles still use this free-running type of oscillator converter in dc-to-dc converters as well as in dc-to-ac inverters. A typical push-pull converter circuit is shown in Figure 6.

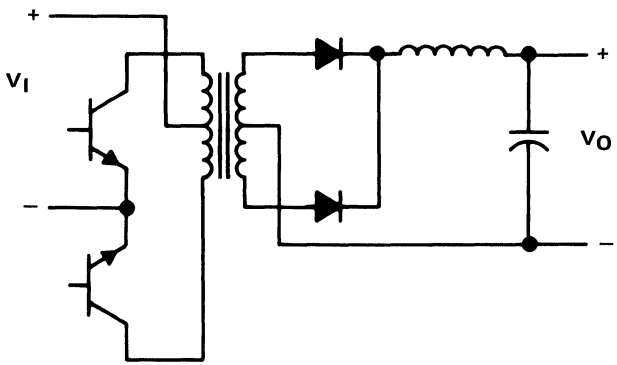


Figure 6. Basic Push-Pull Converter Circuit

Half-Bridge Converter

The most popular type of high-power converter is the half-bridge circuit illustrated in Figure 7. The half-bridge converter has several advantages over the push-pull circuit. First, the midpoint between the capacitors (point A) can be charged to $V_I/2$. This allows

the use of transistors with lower breakdown voltage. Second, because the primary is driven in both directions (push-pull), a full-wave rectifier and filter are used which allows the transformer core to be more effectively utilized.

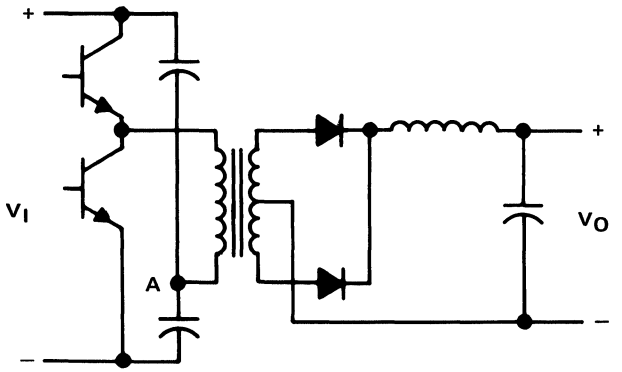


Figure 7. Half-Bridge Converter Circuit

Full-Bridge Converter

In contrast to the half-bridge, the full-bridge (or H-Bridge) converter uses four transistors as shown in Figure 8. In a full-bridge circuit, the diagonally opposite transistors (Q1/Q2 or Q3/Q4) are turned on during alternate half cycles. The highest voltage any transistor is subjected to is V_I, rather than 2 × V_I as is the case in the push-pull converter circuit. The full-bridge circuit offers increased reliability because less voltage and current stress is placed on the transistors. The disadvantage of this circuit is the space required by the four transistors and the cost of the two additional transistors.

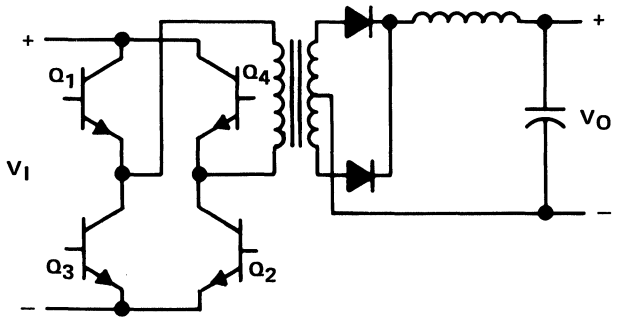


Figure 8. Full-Bridge Converter Circuit

TL493 Floppy Disk Power Supply

The TL493 incorporates, on a single monolithic chip, all the functions required for a pulse-width modulation control circuit. The TL493 is similar to the TL594, from which it was derived, except that the TL493 includes a current-limit amplifier instead of a second-error amplifier.

The current-limit amplifier of the TL493 has an offset voltage of approximately 80 mV in series with the inverting input (pin 15). This makes it easier to design the current-limit portion of the power supply and also requires fewer components. With 80 mV on the inverting input, it is only necessary to apply an 80-mV control voltage to the noninverting input (pin 16). This is easily accomplished by taking the voltage across a resistor in series with the load.

The floppy disk power supply schematic is shown in Figure 9. The power supply uses a pair of TIP34 p-n-p transistors in a push-pull configuration. The oscillation frequency is set at 25 kHz and −5 V at 500 mA by the .01-μF capacitor on pin 5 and the 5-kΩ resistor on pin 6.

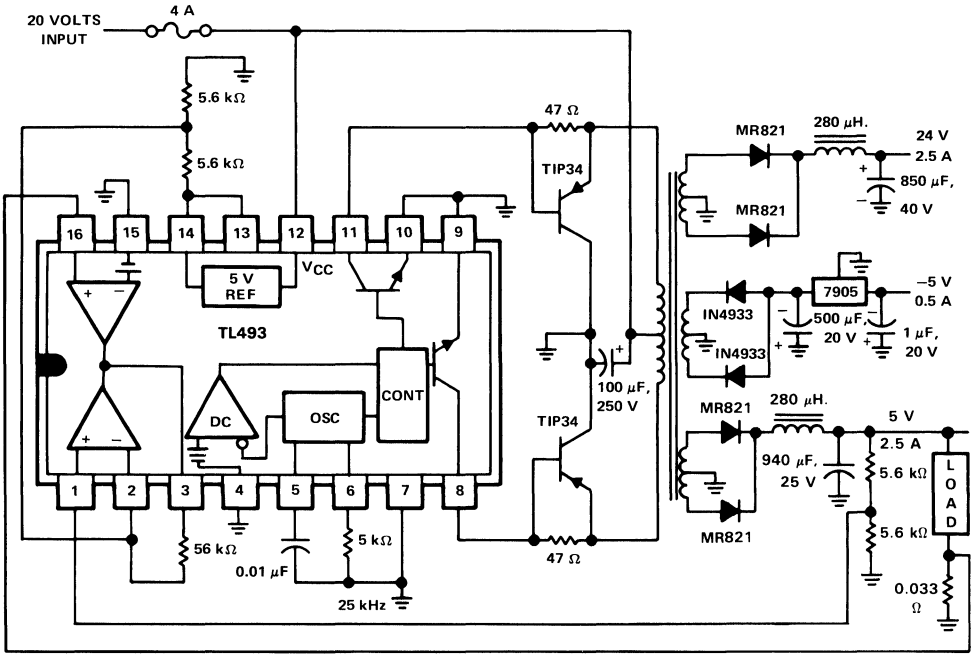


Figure 9. TL493 Floppy Disk Power Supply

The center connection of the two 5.6-kΩ resistors on pins 13 and 14 establishes a 2.5-V reference voltage on pin 2, which is the inverting input of the voltage control error amplifier. The voltage feedback to pin 1, the noninverting input, comes from the center connection of the two 5.6-kΩ resistors located on the 5-V/2.5-A power supply output terminal. Because this voltage supplies the logic circuits, it requires closer regulation.

The 24-V winding, on the other hand, is not critical as it furnishes voltage for the stepping motor. The −5-V supply is regulated separately with a uA7905 three-terminal regulator. In choosing components for this circuit, the same precautions taken in the construction of any switching power supply should be observed; be careful of layout, ground loops, and heatsinking of the power transistors. In the output section, where high-frequency rectifiers are needed, either Schottky or fast recovery diodes should be used. For output capacitors, low equivalent series resistance (ESR) types should be considered. The output ripple depends more on this resistance than on the capacitor value.

Transformer Construction

The transformer for this circuit was wound on a toroid core. The core used was 3C8 ferrite material (F-42908-TC). The winding layout is shown in Figure 10.

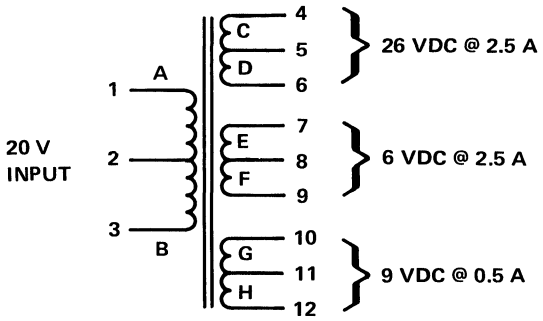


Figure 10. Transformer Winding Layout

Transformer Winding Data

Primary A + B = 20 turns bifilar #20 HNP
Secondary C + D = 28 turns bifilar #20 HNP over A+B
Secondary E + F = 6 turns bifilar #20 HNP over C+D
Secondary G + H = 10 turns bifilar #26 HNP over E+F
NOTE: All windings to be center tapped.

DC Resistance

Winding 1 - 3 = 0.11 Ω
Winding 4 - 6 = 0.11 Ω
Winding 7 - 9 = 0.025 Ω
Winding 10 - 12 = 0.15 Ω

TL594 12-V to 5-V Step-Down Regulator

The TL594 switching voltage regulator operates as a step-down converter in a discontinuous mode. When the output current falls below a specified minimum value, the inductor current becomes discontinuous. The advantages of a step-down converter in this mode of operation are:

1. The ripple voltage at the output can be kept low, even in high-current designs.
2. The ratio of peak current in the switching device to output current is determined by the inductor value and is typically low. For a specific output current requirement, the current rating for the switching transistor can be lower than for a transistor operating in a continuous mode.
3. Pulse-width modulation occurs with input voltage variations. Load variations are compensated for by modulation of the dc current level in the inductor, as well as by pulse-width modulation. This allows high efficiency to be maintained over the entire load range (from I_O max to I_O min).

The disadvantages of this type of converter are:

1. The size of the inductor used may result in a high-inductance value.
2. Transient response is impaired by high-inductance values.
3. Although peak current in the rectifier is reduced, losses due to reverse recovery current are increased.

The complete circuit for the TL594 step-down regulator is shown in Figure 11. For this application, the two switching transistors operate in phase with each other by grounding the output control, pin 13. The switching transistors supply input to the inductor, L for part of the oscillator cycle. For the remaining part of the oscillator cycle, the voltage across the inductor reverses and diode D1 starts conducting, maintaining current flow in the inductor while the transistors are off (see Figure 12).

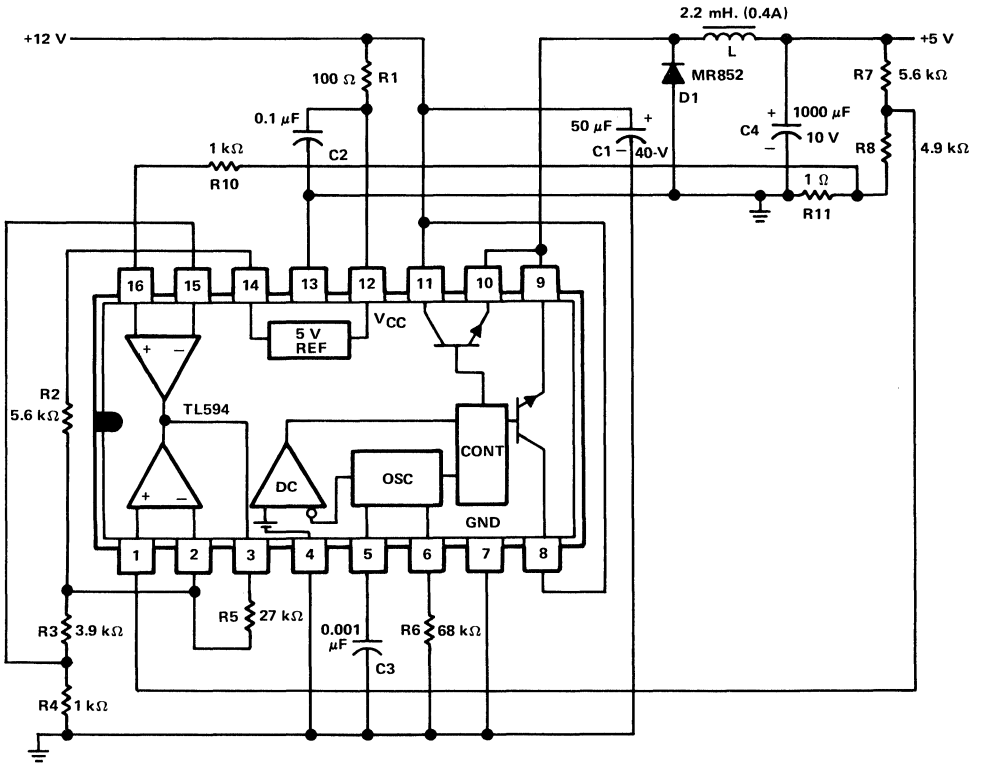


Figure 11. TL594 12-V to 5-V Step-Down Regulator

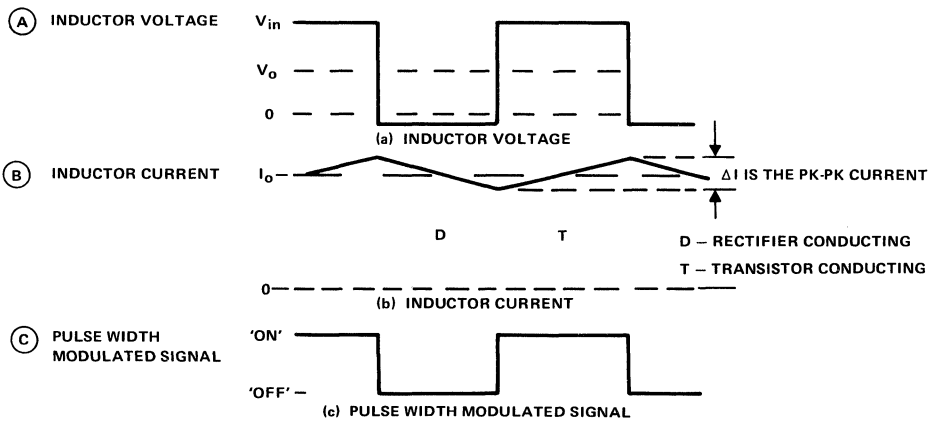


Figure 12. 12-V to 5-V Series Switching Regulator Waveforms

The input supply through R1 to pin 12 is decoupled by capacitor C2. Capacitor C4 filters the output voltage. The timing components C3 and R6 set the oscillator frequency to 15 kHz. The 2.2-mH inductor can be made on an RM7 ferrite core with 94 turns of #28 transformer wire.

Output-current limiting of 500 mA is provided by sensing the overcurrent level with R11 and feeding the resultant error voltage to the positive input of the current error amplifier on pin 16. The negative input to this error amplifier is biased to 500 mV from reference divider R2, R3, and R4. This resistor network also furnishes about 2.3-V bias to the voltage control error amplifier. An output error voltage signal is taken from the junction of R7 and R8 and fed to the positive input of the voltage control error amplifier. The voltage control loop gain is set by feedback resistor R5.

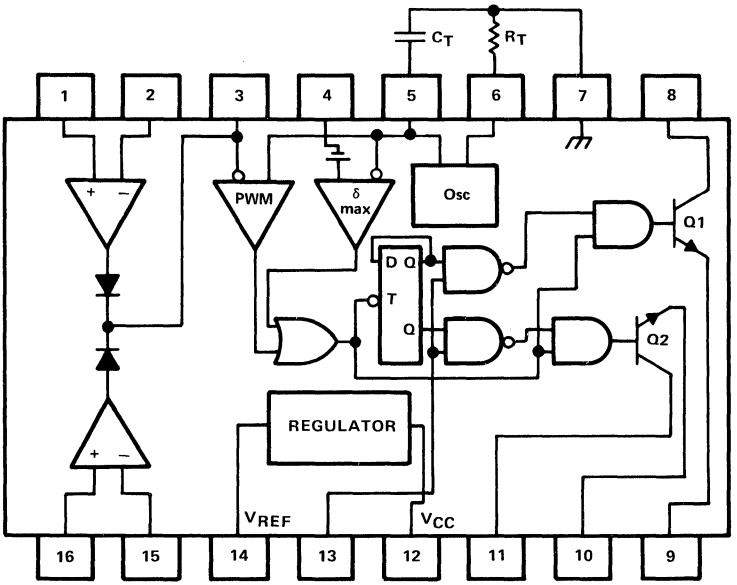
Specifications

Input Voltage	12 V nominal (10 V to 15 V)
Output Voltage	5 V ± 10%
Output Ripple	50 mV_{pp}
Output Current	400 mA
Output Power	2 W at 5-V output
Short Circuit Protection	500-mA constant current
Efficiency	typically 70%

The TL594 Control Circuit

The TL594 is a fixed frequency pulse-width-modulation control for switching power supplies and voltage converters. The TL594 includes an adjustable oscillator, a pulse-width modulator, and an error amplifier. Additional functions include over-current detection, independent dead-time control, a precision 5-V reference regulator, and output control logic which allows single-ended or push-pull operation of the two switching transistors. Figure 13 shows a block diagram of the TL594.

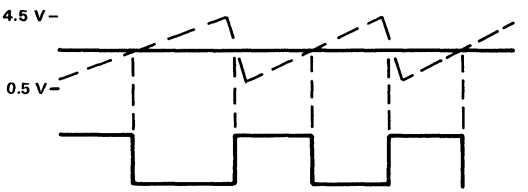
Modulation of the output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on timing capacitor C_T to either of two control signals. The output stage is enabled when the sawtooth voltage is greater than the voltage of the control signal. See Figure 14. As the control signals increase, the output pulse width decreases. The control signals are derived from two sources: the dead-time control and the error amplifiers. The dead-time comparator has a fixed offset of 10 mV which provides a preset dead time of about 5%. This is the minimum dead time that can be programmed with pin 4 grounded.



PIN ASSIGNMENT

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1.	ERROR AMP. 1, NONINVERTING INPUT	9.	DRIVE TRANSISTOR 1, EMITTER
2.	ERROR AMP. 1, INVERTING INPUT	10.	DRIVE TRANSISTOR 2, EMITTER
3.	COMPENSATION INPUT	11.	DRIVE TRANSISTOR 2, COLLECTOR
4.	DEAD TIME CONTROL INPUT	12.	INPUT SUPPLY
5.	OSCILLATOR TIMING CAPACITOR	13.	OUTPUT MODE CONTROL
6.	OSCILLATOR TIMING RESISTOR	14.	STABILIZED REFERENCE VOLTAGE
7.	GROUND	15.	ERROR AMP 2, INVERTING INPUT
8.	DRIVE TRANSISTOR 1, COLLECTOR	16.	ERROR AMP 2, NONINVERTING INPUT

Figure 13. TL594 Block Diagram



PWM CONTROL RANGE, PIN 3

RESULTANT OUTPUT PULSE WITH
PIN 3 VOLTAGE AS ABOVE PIN 13 WIRED FOR
SINGLE ENDED OPERATION

Figure 14. Output Pulses vs Sawtooth Control Voltage

The pulse-width-modulation (PWM) comparator generates the control difference signal created by the input from either of the error amplifiers. One error amplifier is used to monitor the output voltage and provide a change in control signal voltage. The other error amplifier monitors the output current and its change in control voltage provides current limiting.

Reference Regulator

The internal 5-V reference at pin 14 provides a stable reference for the control logic, pulse-steering flip-flop, oscillator, dead-time-control comparator and pulse-width-modulation circuitry. It is a band-gap circuit with short circuit protection and is internally programmed to an accuracy of ± 5%.

Oscillator

The internal oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison with the various control signals. The oscillator frequency is set by an external timing capacitor and resistor on pins 5 and 6. The oscillator frequency is determined by the equation:

$$f_{OSC} = \frac{1}{R_T C_T} \text{ (single-ended applications)}$$

The oscillator frequency is equal to the output frequency only for single-ended applications. The output frequency for push-pull applications is one-half the oscillator frequency as shown by the equation:

$$f_{OSC} = \frac{1}{2\ R_T C_T} \text{ (push-pull applications)}$$

There is a frequency variation of ± 5% between devices due to internal component tolerances. The oscillator charges the external timing capacitor, C_T, with a constant current which is determined by the external timing resistor, R_T. This circuit produces a linear ramp voltage waveform. When the voltage across the timing capacitor reaches 3 V, the circuit discharges and the charging cycle is initiated again.

Dead-Time and PWM Comparators

Both the dead-time and PWM comparator functions use a single logic comparator with parallel input stages. The comparator output is a pulse-width-modulated signal, whose width is determined by comparison with the oscillator ramp waveform. The comparator outputs drive the output control logic. A fixed 100-mV offset voltage input to the dead-time comparator allows a minimum dead time between output pulses to be maintained when the dead-time control input (pin 4) is grounded (Figure 15).

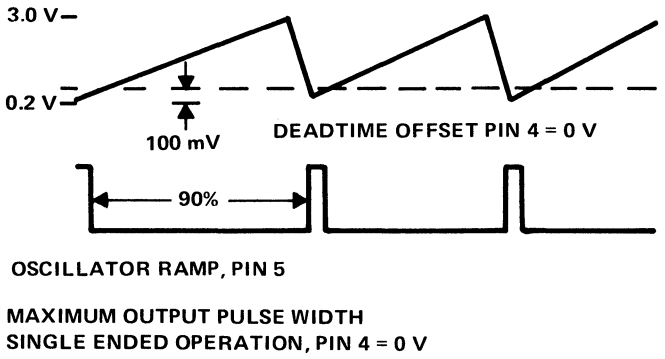


Figure 15. Deadtime Comparator Operation

The full range of pulse-width control (0% - 90%) is available when the dead-time control voltage (pin 4) is between 3.3 V and 0 V. The relationship between control voltage and maximum output pulse width is essentially linear. A typical application for this may be in a push-pull converter circuit where overlap of the conduction times of power transistors must be avoided.

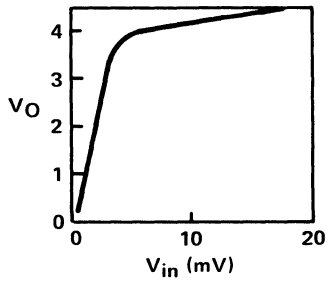
The PWM comparator input is coupled internally to the outputs of the two error amplifiers. This input is accessible on pin 3 for control loop compensation. The output pulse width varies from 90% of the period to zero as the voltage present at pin 3 varies from 0.5 V to 4.5 V (Figure 14).

Error Amplifiers

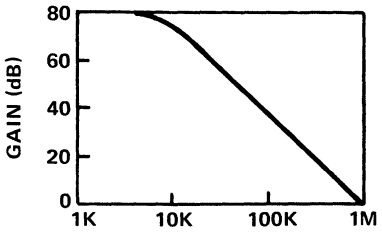
Both error amplifiers are high-gain amplifiers which operate as single-ended, single-supply amplifiers, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With the outputs ORed together, the amplifier with the higher output level dominates. The open-loop gain of these amplifiers is 60 dB. Both error amplifiers exhibit a response time of about 400 ns from their inputs to their outputs on pin 3. Figure 16 shows the amplifier transfer characteristics and a Bode plot of the gain curves.

Output Logic Control

The output control logic interfaces the pulse-width modulator to the output stages. In the single-ended mode (both outputs conducting simultaneously), the pulse-width-modulated signal is gated through to both output stages when the output control (pin 13) is connected to ground.



AMPLIFIER TRANSFER CHARACTERISTICS



AMPLIFIER BODE PLOT

Figure 16. Amplifier Performance Curves

For push-pull operation (each output stage conducting alternately), the output control (pin 13) is connected to the internal reference voltage (pin 14) enabling the pulse steering flip-flop. The flip-flop is toggled on the trailing edge of the pulse-width-modulated signal gating it to each of the outputs alternately; therefore, the switching frequency of each output is one-half the oscillator frequency. The output control (pin 13) must never be left open. It may be connected to the internal voltage reference (pin 14) or ground (pin 7).

The Output Driver Stages

The two identical Darlington output drivers may be operated in parallel or push-pull mode. Both the collector and emitter terminals are available for various drive configurations. $V_{CE(sat)}$ of each output at 200 mA is typically 1.1 V in common-emitter configuration and 1.5 V in common-collector configuration. These drivers are protected against overload but do not have sufficient current limiting to be operated as current source outputs.

Soft Start

Use of a soft-start protection circuit is recommended. This circuit prevents current surges during power-up and protects against false signals which might be created by the control circuit when power is applied. Implementing a soft-start circuit is relatively simple using the dead-time control input (pin 4). Figure 17 shows an example.

Initially, capacitor C_S forces the dead-time control input to follow the internal 5-V reference which disables both outputs (100% dead time). As the capacitor charges through R_S, the output pulse width increases until the control loop takes command.

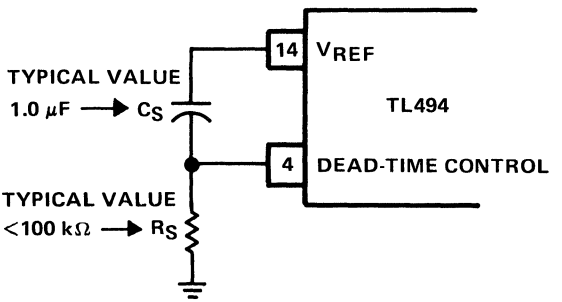


Figure 17. Soft-Start Circuit

Overvoltage Protection

The dead-time control input (pin 4) also provides a convenient input for over-voltage protection, which may be sensed as an output voltage condition, or input voltage protection as shown in Figure 18.

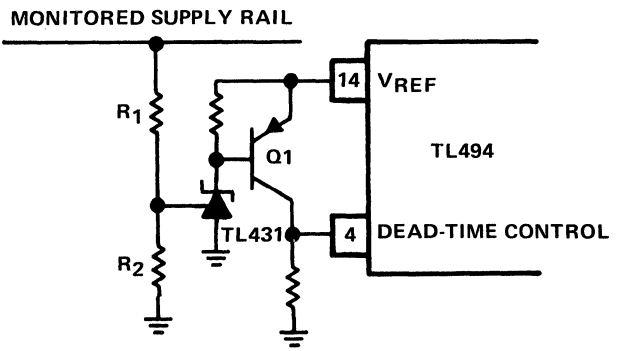


Figure 18. Overvoltage Protection Circuit

A TL431 is used as the sensing element. When the monitored supply rail voltage increases to the point that 2.5 V is developed across R2, the TL431 conducts, Q1 becomes forward biased, and the dead-time control is pulled up to the reference voltage which disables the output transistors.

Designing a Power Supply 5-V/10-A Output

Design Objective

This design uses the TL594 integrated circuit based on the following parameters:

V_O = 5 V
V_I = 32 V
I_O = 10 A
f = 20 kHz switching frequency
V_R = 100 mV peak-to-peak (V_{ripple})
ΔI_L = 1.5 A inductor current change

Input Power Source

The 32-V dc-power source for this supply uses a 120-V input, 24-V output transformer rated at 75 VA. The 24-V secondary winding feeds a full-wave bridge rectifier followed by a 0.3-Ω current limit resistor and two filter capacitors, as shown in Figure 19.

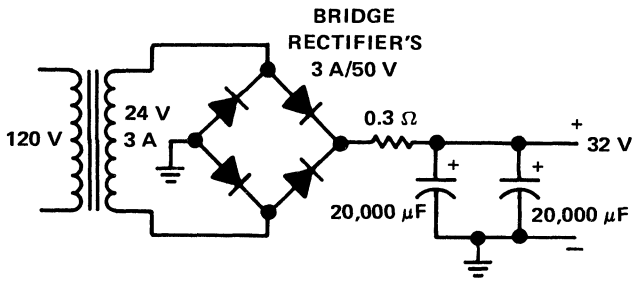


Figure 19. Input Power Source

The output current and voltage are determined by the following equations.

$$V_{rectifier} = V_{secondary} \times \sqrt{2} = 24\ V \times \sqrt{2} = 34\ V$$

$$I_{rectifier(avg)} \approx \left(\frac{V_O}{V_I}\right) \times I_O \approx \frac{5\ V}{32\ V} \times 10\ A \approx 1.6\ A$$

The 3-A/50-V full-wave bridge rectifier meets these calculated conditions. Figure 20 illustrates the switching and control section.

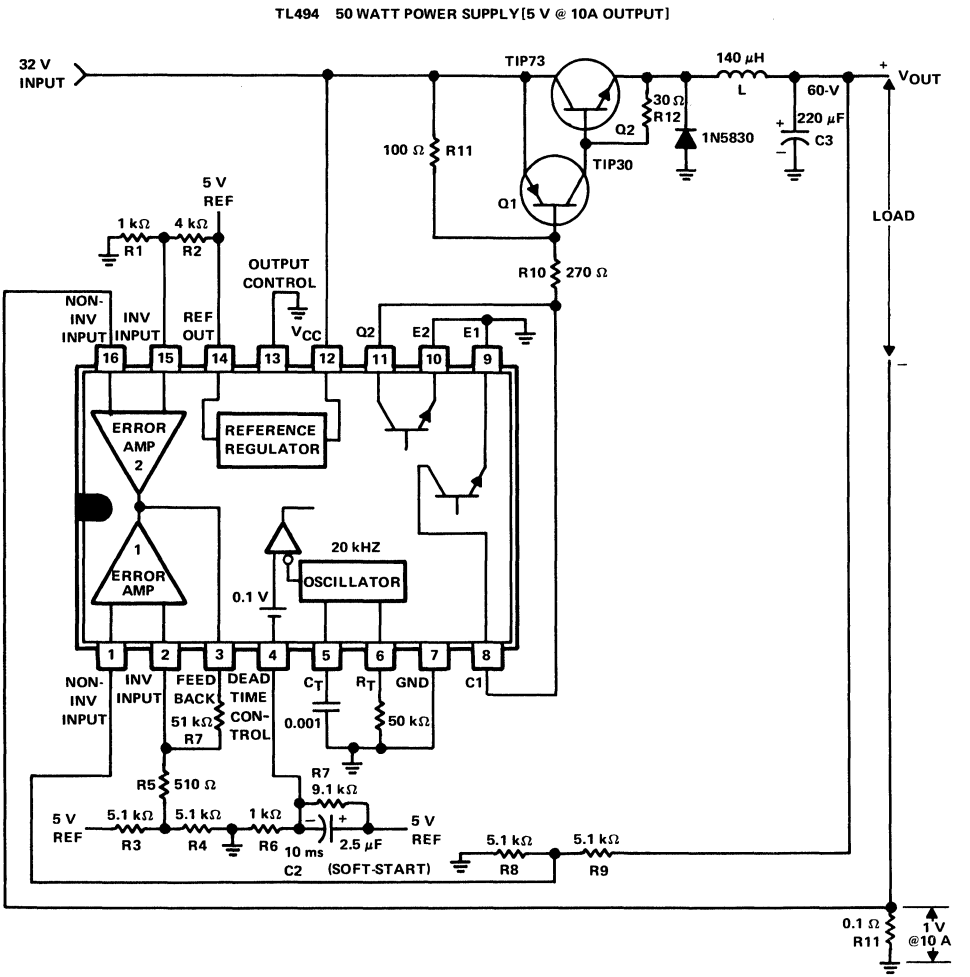


Figure 20. Switching and Control Section

Control Circuits

Oscillator

The TL594 oscillator frequency is controlled by connecting an external timing circuit consisting of a capacitor and resistor to pins 5 and 6. The oscillator is set to operate at 20 kHz using the component values calculated by the following equations.

$$f = \frac{1}{R_T C_T}$$

where:

R_T = Value of timing resistor
C_T = Value of timing capacitor

Choose C_T = 0.001 μF and calculate R_T.

$$R_T = \frac{1}{f \times C_T} = \frac{1}{20 \times 10^3 \times 0.001 \times 10^{-6}} = 50\ k\Omega$$

Error Amplifier

The error amplifier compares a sample of the 5-V output to a reference and adjusts the pulse-width modulator to maintain a constant output as shown in Figure 21. The TL594's internal 5-V reference (pin 14) is divided to 2.5 V by R3 and R4. The output voltage error signal is also divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5 V, a 10-kΩ potentiometer may be used in place of R8 to provide an adjustment control. To increase the stability of the error amplifier circuit, the output of the error amplifier is fed back to the inverting input through R7, reducing the gain to 100.

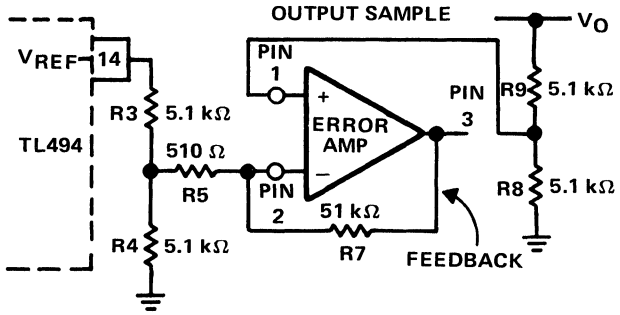


Figure 21. Error Amplifier Section

Current Limit Amplifier

The power supply was designed for a 10-A load current and an I_L swing of 1.5 A; therefore, the short circuit current should be

$$I_{SC} = I_O + \frac{I_L}{2} = 10.75\ A$$

The current limit portion of the circuit is shown in Figure 22. Resistors R1 and R2 set a reference of about 1 V on the inverting input of the current limit amplifier. Resistor R11, in series with the load, applies 1 V to the noninverting terminal of the current limit

amplifier when the load current reaches 10 A. The output-pulse width will be reduced accordingly. The value of R11 is calculated as follows:

$$R11 = \frac{1\ V}{10\ A} = 0.1\ \Omega$$

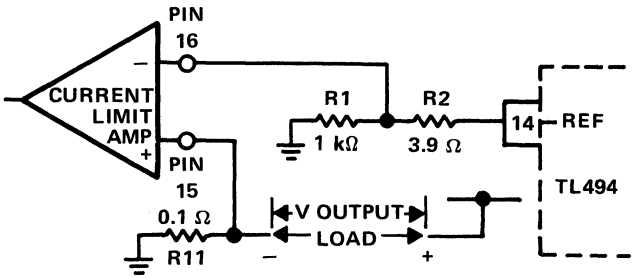


Figure 22. Current Limit Circuit

Soft Start and Dead Time

To reduce stress on the switching transistors at startup, the startup surge which occurs as the output filter capacitor charges must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit, as shown in Figure 23, relatively simple.

The "soft-start" circuit allows the pulse width at the output to increase slowly, as shown in Figure 23, by applying a negative slope waveform to the dead-time control input (pin 4). Initially, capacitor C2 forces the dead-time control input to follow the 5-V reference regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output-pulse width slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after startup will be 0.1 × 5 V or 0.5 V.

The soft-start time is generally in the range of 25 to 100 clock cycles. If we select 50 clock cycles at a 20-kHz switching rate, the soft-start time is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{20\ kHz} = 50\ \mu s \text{ per clock cycle}$$

The value of the capacitor is then determined by

$$C2 = \frac{\text{soft start time}}{R6} = \frac{50\ \mu s \times 50 \text{ cycles}}{1\ k\Omega} = 2.5\ \mu F$$

This helps to eliminate any false signals which might be created by the control circuit as power is applied.

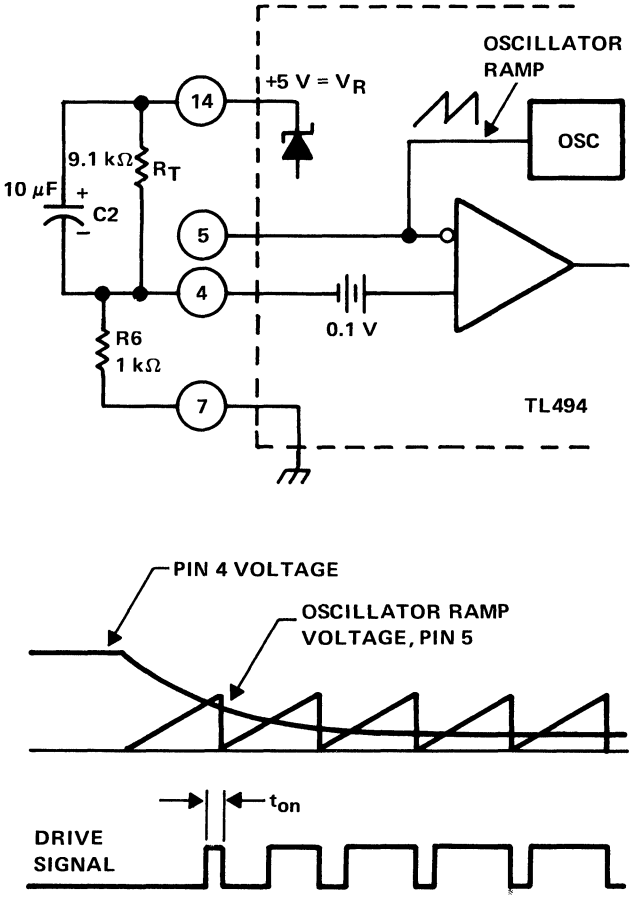


Figure 23. Soft-Start Circuit

Inductor Calculations

The switching circuit used is shown in Figure 24. The size of the inductor (L) required is calculated as follows:

$$d = \text{Duty Cycle} = \frac{V_O}{V_I} = \frac{5\ V}{32\ V} = 0.156$$

$$f = 20\ \text{kHz (Design Objective)}$$

$$t_{on} = \text{time on (S1 closed)} = \frac{1}{f} \times d = 7.8\ \mu s$$

$$t_{off} = \text{time off (S1 open)} = \frac{1}{f} - t_{on} = 42.2\ \mu s$$

$$L \approx \frac{(V_I - V_O) \times t_{on}}{\Delta IL} \approx \frac{(32\ V - 5\ V) \times 7.8\ \mu s}{1.5\ A} \approx 140.4\ \mu H$$

$$L \approx 140\ \mu H$$

INDUCTOR CALCULATIONS

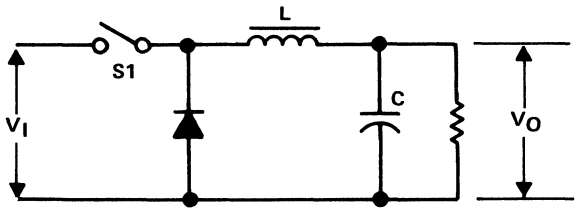


Figure 24. Switching Circuit

Output Capacitance Calculations

Once the filter inductance has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important; so, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and peak-to-peak ripple current.

$$ESR(max) = \frac{\Delta V_{O\ (ripple)}}{\Delta I_L} = \frac{0.1\ V}{1.5\ A} = 0.067\ \Omega$$

The minimum capacitance of C3 necessary to maintain the V_O ripple voltage at less than the 100-mV design objective was calculated according to the following equation.

$$C3 = \frac{\Delta I_L}{8\ f \Delta V_O} = \frac{1.5\ A}{8 \times 20 \times 10^3 \times 0.1\ V} = 94\ \mu F$$

A 220-µF, 60-V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8 A.

Transistor Power Switch Calculations

The transistor power switch was constructed with a TIP30 p-n-p drive transistor and a TIP73 n-p-n output transistor. These two power devices were connected in a p-n-p hybrid Darlington circuit configuration as shown in Figure 25. The hybrid Darlington must be saturated at a maximum output current of $I_O + \Delta I_L/2$ or 10.8 A. The Darlington h_{FE} at 10.8 A must be high enough not to exceed the 250-mA maximum output collector current of the TL594. Based on published TIP30 and TIP73 h_{FE} specifications, the required power switch minimum drive was calculated by the following equations to be 108 mA.

$h_{FE}(Q1)$ at I_C of 1.2 A = 10

$h_{FE}(Q2)$ at I_C of 12.0 A = 10

$$i_B \geq \frac{I_O + \frac{\Delta I_L}{2}}{h_{FE}(Q2) \times h_{FE}(Q1)} \geq 108 \text{ mA}$$

The value of R10 was calculated by the following equation.

$$R10 \leq \frac{V_I - (V_{BE}(Q1) + V_{CE}(TL594))}{i_B} = \frac{32 - (1.3 + 0.7)}{0.108}$$

$$R10 \leq 277\ \Omega$$

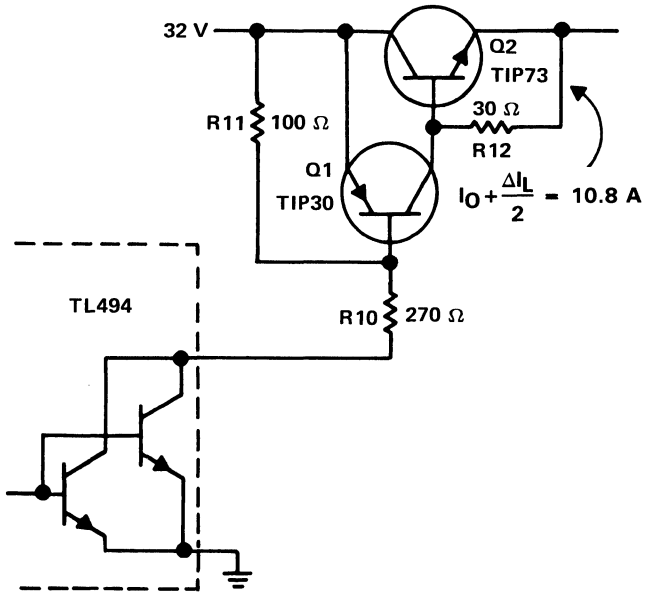
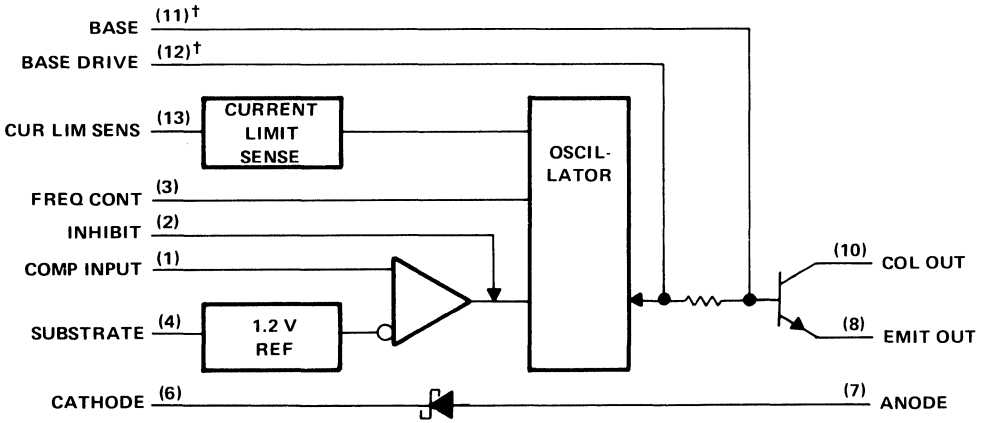


Figure 25. Power Switch Section

Used on these calculations, the nearest standard resistor value of 270 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in the switching transistors when they are turned off. The power supply described demonstrates the flexibility of the TL594 pulse-width-modulation control circuit. This power supply design demonstrates many of the power supply control methods provided by the TL594 as well as the versatility of the control circuit.

TL497A Switching Voltage Regulator

The TL497A is a fixed-on-time, variable-frequency voltage regulator controller. The block diagram of the TL497A is shown in Figure 26. The on-time is controlled by an external capacitor connected between the frequency control pin (pin 3) and ground. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and threshold vary proportionately with V_{CC}; thus, the on-time remains constant over the allowable input voltage range.



†The Base pin (#11) and Base Drive pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

Figure 26. TL497A Block Diagram

The output voltage is controlled by two series resistors in parallel with the supply output. The resistance ratios are calculated to supply 1.2 V to the comparator input (pin 1) at the desired output voltage. This feedback voltage is compared to the 1.2-V bandgap reference by the high-gain error amplifier. When the output voltage falls below the desired voltage, the error amplifier enables the oscillator circuit, which charges and discharges C_T.

The n-p-n output transistor is driven "on" during the charging cycle of C_T. The internal transistor can switch currents up to 500 mA. It is current driven to allow operation

from either the positive supply voltage or ground. An internal diode matched to the current characteristics of the output transistor is included on the chip and may be used for blocking or commutating purposes.

The TL497A also contains current-limiting circuitry which senses the peak currents in the switching regulator and protects the inductor against saturation and the output transistor against overstress. The current limit is adjustable and is set by a single-sense resistor between pins 13 and 14. The current-limit circuitry is activated when 0.5 V is developed across current-limit resistor R_{CL}.

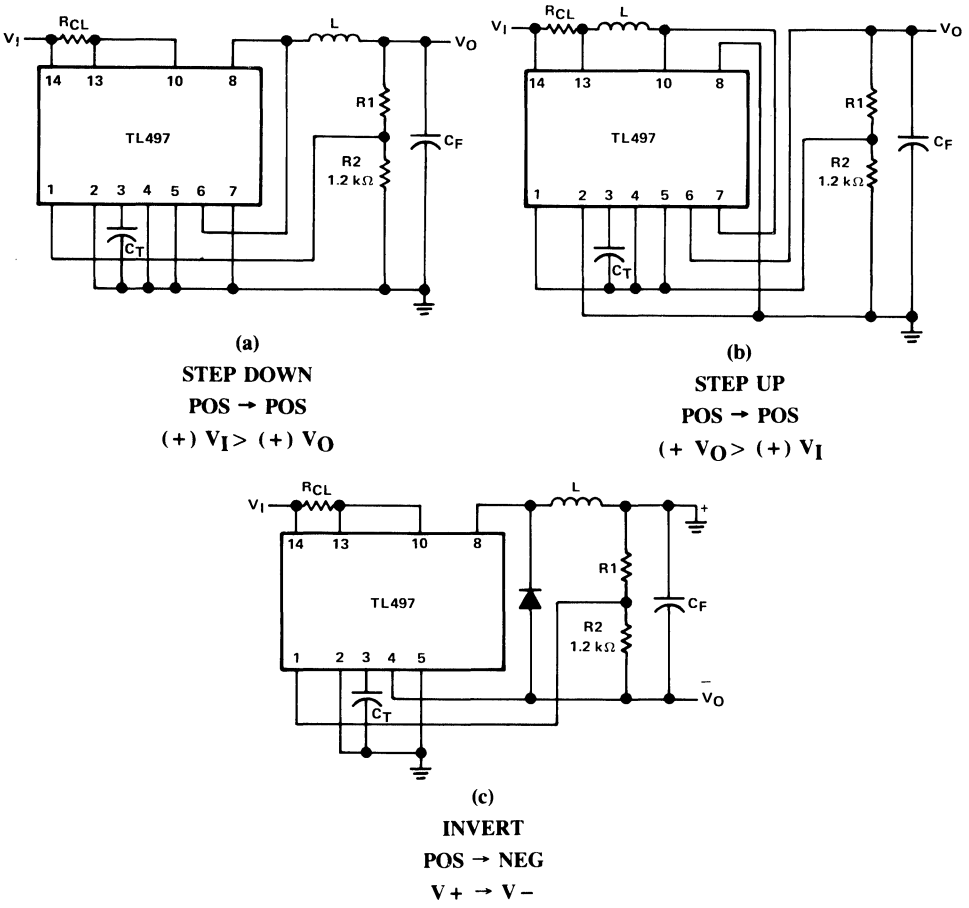


Figure 27. Basic Power Supply Configurations

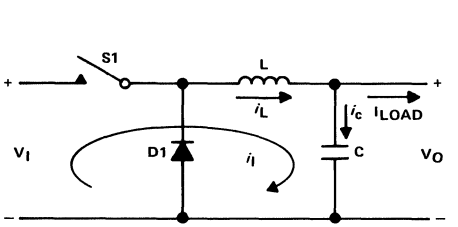
The TL497A contains all the active elements required for constructing a single-ended dc-to-dc converter. The output transistor and the rectifier are uncommitted allowing maximum flexibility in the choice of circuit configuration. The TL497A's primary feature is design simplicity. Using six external components; three resistors, two capacitors, and one inductor, the step-up, step-down, and inverting power supplies shown in Figure 27 may be constructed.

STEP-DOWN	STEP-UP	INVERTING
POS → POS	POS → POS	POS → NEG
$+V_I > +V_O$	$+V_O > +V_I$	$+V_I > -V_O$

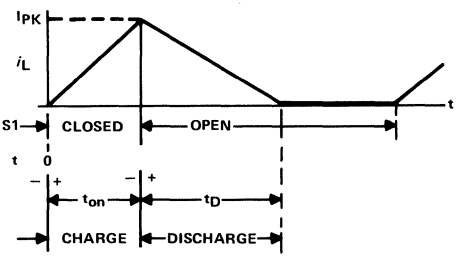
Step-Down Switching Regulator

The circuit in Figure 28(a) illustrates the basic configuration for a step-down switching regulator. When switch S1 is closed, the current in the inductor and the voltage across the capacitor start to build up. The current increases while switch S1 is closed as shown by the inductor waveform in Figure 28(b). The peak current in the inductor is dependent on the time S1 is closed (t_{on}).

When S1 opens, the current through the inductor is I_{pk}. Since the current cannot change instantaneously, the voltage across the inductor inverts, and the blocking diode (D1) is forward biased providing a current path for the discharge of the inductor into the load and filter capacitor. The inductor current discharges linearly as illustrated in Figure 28(b).



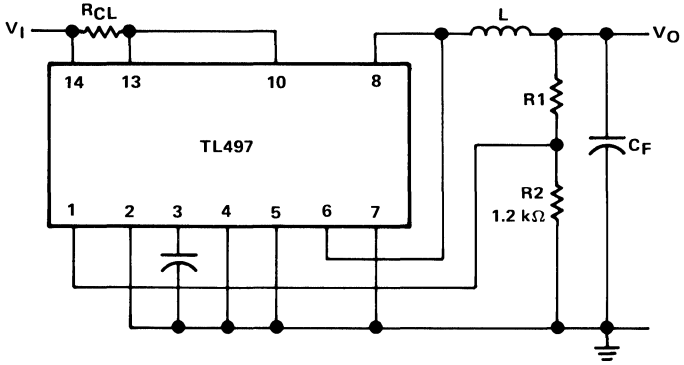
(a) BASIC STEP-DOWN REGULATOR



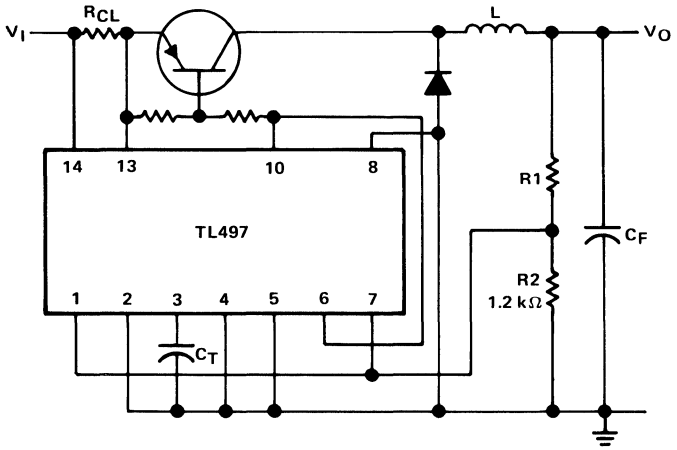
(b) INDUCTOR CURRENT WAVEFORM

Figure 28. Step-Down Switching Regulator

For the output voltage to remain constant, the net charge delivered to the filter capacitor must be zero. The charge delivered to the capacitor from the inductor must be dissipated in the load. Since the charge developed in the inductor is fixed (constant on-time), the time required for the load to dissipate that charge will vary with the load requirements. It is important to use a filter capacitor with minimal ESR. Note, however, some ripple voltage is required for proper operation of the regulator. Figure 29 shows a positive, step-down configuration both with and without an external pass transistor. Design equations for calculating the external components are included.



BASIC CONFIGURATION
(I_{PK} <500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\ I_{LOAD\ max}$
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{PK}}\ t_{on}\ (\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (20 to 150 μs)

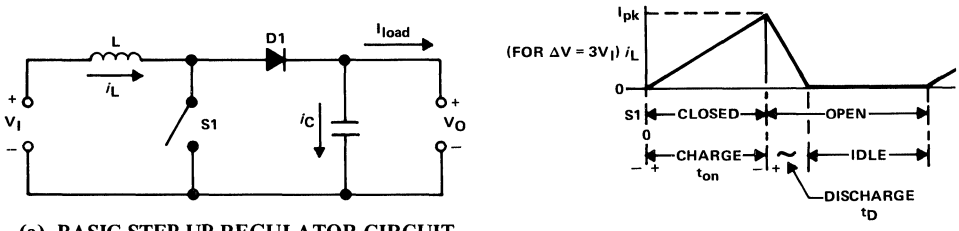
- $C_T\ (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \dfrac{0.5\ V}{I_{PK}}$
- $C_F = \dfrac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\ 2\ I_{PK}} \times \dfrac{t_{on}\ V_I}{V_O}$

Figure 29. Positive Regulator, Step-Down Configurations

Step-Up Switching Regulator

In the step-up regulator, the formulas change slightly. During the charging cycle (S1 closed), the inductor (L) is charged directly by the input potential. The peak current is not related to the load current as it was in the step-down regulator because, during the inductor charge cycle, the blocking diode D1 is reverse biased and no charge is delivered to the load.

The circuit in Figure 30(a) delivers power to the load only during the discharge cycle of the inductor (S1 open). The diode (D1) is forward biased and the inductor discharges into the load capacitor. Figure 31 shows a positive, step-down configuration both with and without an external pass transistor. Design equations are included.



(a) BASIC STEP-UP REGULATOR CIRCUIT

(b) INDUCTOR CURRENT WAVEFORM

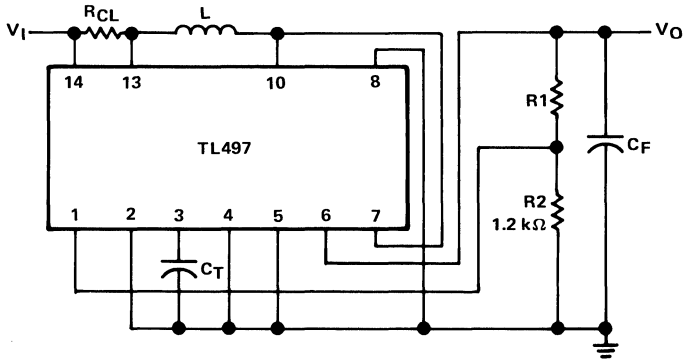
Figure 30. Step-Up Switching Regulator

Inverting Configuration

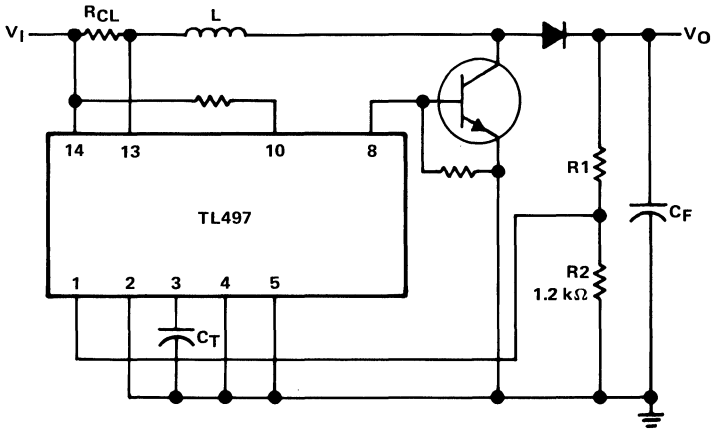
The inverting regulator is similar to the step-up regulator. During the charging cycle of the inductor, the load is isolated from the input. The only difference is in the potential across the inductor during its discharge. This can best be demonstrated by a review of the basic inverting regulator circuit (Figure 32).

During the charging cycle (S1 closed), the inductor (L) is charged only by the input potential, similar to the step-up configuration. In the inverting configuration, the input provides no contribution to the load current during the charging cycle. The maximum load current for discontinuous operation will be limited by the peak current, as observed in the step-up configuration. The inductor current waveform looks identical to the waveform demonstrated in the step-up configuration [see Figure 30(b)].

Figure 33 shows the inverting applications both with and without an external pass transistor. Design equations are also included. Note that in the inverting configuration, the internal diode is not used. An external diode must be used because pin 4 (substrate) must be the most negative point on the chip. The cathode of the internal diode is also the cathode of a diode connected to the substrate. When the cathodes are at the most negative voltage in the circuit, there will be conduction to the substrate resulting in unstable operation.



BASIC CONFIGURATION
(I_{PK} <500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\, I_{LOAD}$ max $1 + \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\ t_{on}\ (\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T\ (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F = \frac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\ 2\ I_{PK}} \times \frac{t_{on}\ V_I}{V_O}$

Figure 31. Positive Regulator, Step-Up Configurations

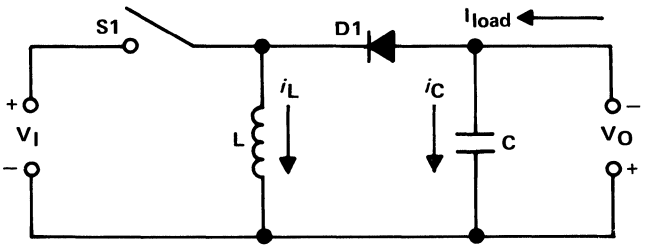


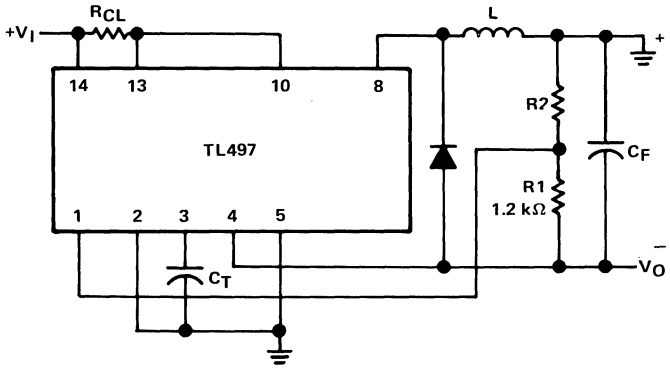
Figure 32. Basic Inverting Regulator Circuit

Design Considerations

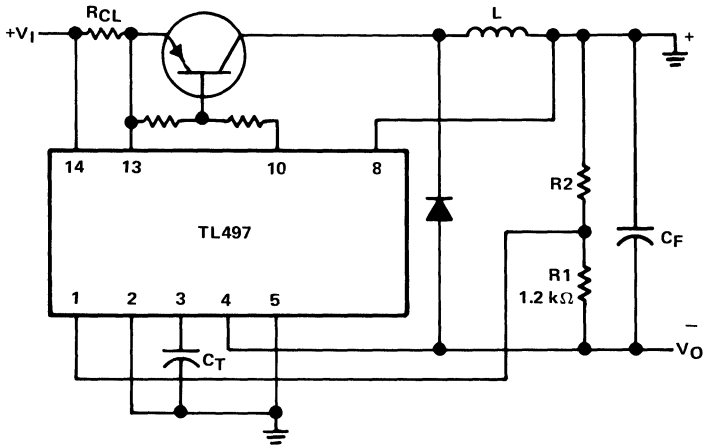
An oscilloscope is required when building a switching regulator. When checking the oscillator ramp on pin 3, the oscilloscope may be difficult to synchronize. This is a normal operating characteristic of this regulator and is caused by the asynchronous operation of the error amplifier to that of the oscillator. The oscilloscope may be synchronized by varying the input voltage or load current slightly from design nominals.

High frequency circuit layout techniques are imperative. Keep leads as short as possible and use a single ground point. Resistors R1 and R2 should be as close as possible to pin 1 to eliminate noise pick-up in the feedback loop. The TL497A type of circuits do not need "hi-Q" inductors. They are, in fact, not desirable due to the broad frequency range of operation. If the "Q" is too high, ringing will occur. If this happens, a shunt resistor (about 1-kΩ) may be placed across the coil to damp the oscillation.

While not necessary, it is highly desirable to use a toroidal inductor as opposed to a cylindrically wound coil. The toroidal type of winding helps to contain the flux closer to the core and in turn minimize radiation from the supply. All high current loops should be kept to a minimum length using copper connections that are as large as possible.



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\, I_{LOAD}\, \max\left[1 + \frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}}\ t_{on}\ (\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T\,(pF) \approx 12\, t_{on}\,(\mu s)$
- $R2 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F = \frac{(I_{PK} - I_{LOAD})^2}{(V_{ripple})\ 2\ I_{PK}} \times \frac{t_{on}\ V_I}{V_O}$

Figure 33. Inverting Applications

A Step-Down Switching Regulator Design Exercise with TL497A

The schematic of a basic step-down regulator is shown in Figure 34. This regulator will have the following design goals:

$$V_I = 15\ V$$

$$V_O = 5\ V$$

$$I_O = 200\ mA$$

$$V_{ripple} = < 1.0\%\ \text{or}\ 50\ mV\ (1.0\% \times 5\ V)$$

Calculations:

$$I_{PK} = 2\ I_L\ max = 400\ mA$$

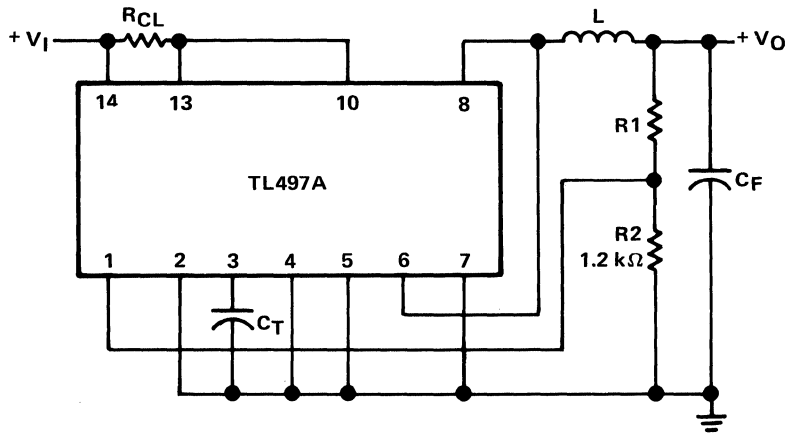


Figure 34. Basic Step-Down Regulator

For design margin, I_{PK} will be designed for 500 mA which is also the limit of the internal pass transistor and diode.

$$\therefore I_{PK} = 500\ mA$$

The next step will be to select t_{on}. You may select a timing capacitor to match an inductor you may already have. You may also assume an on-time and calculate the inductor value. We will assume an on-time of 20 μs.

$$t_{on} = 20\ \mu s$$

$$L(\mu H) = \frac{V_I - V_O}{I_{PK}} \times t_{on}\ \mu s = \frac{15 \times 5}{0.5} \times 20 = 400\ \mu H$$

$$L = 400\ \mu H$$

To set the TL497A for 5-V output:

$$R2 = 1.2\ k\Omega \text{ (fixed)}$$

$$R1 = (5 - 1.2)\ k\Omega = 3.8\ k\Omega$$

To set current limiting:

$$R_{CL} = \frac{0.5}{I_L} = \frac{0.5}{500 \times 10^{-3}} = 1\ \Omega$$

$$R_{CL} = 1\ \Omega$$

For the on-time chosen, C_T can be approximated:

$$C_T(pF) = 12\ t_{on}\ \mu s$$

$$C_T = 240\ pF$$

or it may be selected from a table in the data sheet.

To determine filter capacitor (C_F) for desired ripple voltage:

$$C_F = \frac{(I_{PK} - I_L)^2}{(V_{ripple})\ 2\ I_{PK}} \times \frac{t_{on}\ V_I}{V_O}$$

$$C_F = \frac{(0.5 - 0.2)^2}{(0.05)\ 2 \times 0.5} \times \frac{20 \times 10^{-6} \times 15}{5} = 108\ \mu F$$

We selected C_F to be 120 μF, the next higher standard value. Figure 35 illustrates the regulator with the calculated values applied to it.

A 150-μF filter capacitor may be used as a prefilter as well as a 0.01-μF disc capacitor to take care of any transients on the incoming V_I rail. For peak currents greater than 500 mA, it is necessary to use an external pass transistor and diode. Such a technique is illustrated in Figure 36, which is an automotive power supply. With a 12-V battery, this step-down regulator supplies 5 V at 2 A.

Figure 37 illustrates a basic step-up regulator. This design steps up the output voltage from 5 V to 15 V. The equations for determining the values of the external components are provided in Figure 31.

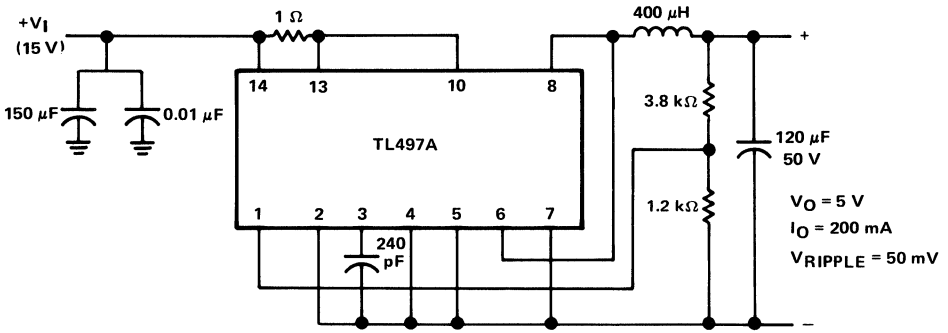


Figure 35. 15-V to 5-V Step-Down Regulator

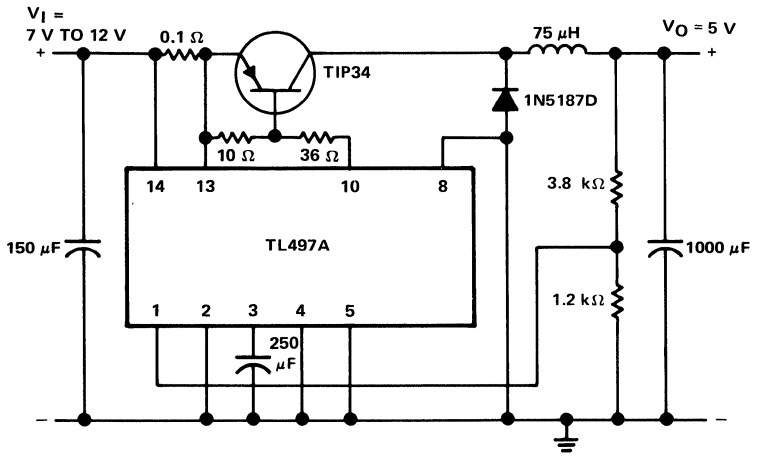


Figure 36. Step-Down Regulator

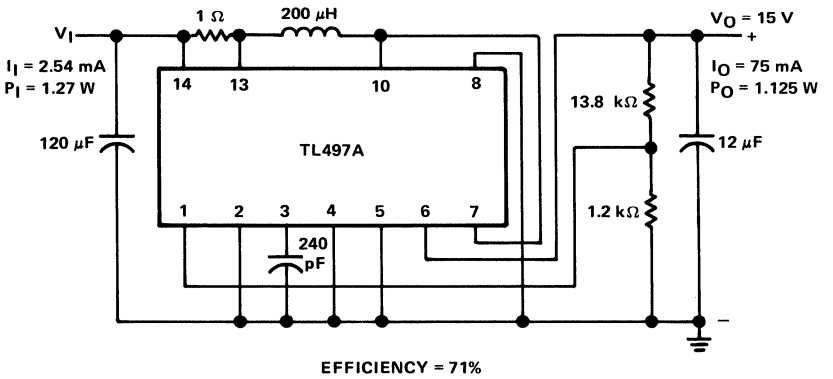


Figure 37. 5-V to 15-V Switching Regulator

Design and Operation of an Inverting Regulator Configuration

Figure 38 illustrates a basic inverting regulator designed to have −5-V output with +5-V input using the design equations in Figure 33.

Conditions:

$$V_I = 5\ V$$

$$V_O = -5\ V$$

$$I_O = 100\ mA$$

$$V_{ripple} = 1.0\%\ \text{or}\ 50\ mV\ (1\% \times 5\ V)$$

Calculations:

$$I_{PK} = 2\ I_{L(max)} \left(1 + \frac{|\ V_O\ |}{V_I}\right)$$

$$I_{PK} = 400\ mA\ \text{(for design margin use 500 mA)}$$

$$\text{Assume } t_{on} = 20\ \mu s$$

$$C_{T(pF)} = 12\ t_{on}\ \mu s$$

$$C_T = 240\ pF$$

$$L = \frac{V_I}{I_{PK}}\ t_{on} = \frac{5}{0.5} \times 20 = 200\ \mu H$$

To set the output voltage:

$$R2 = 1.2\ k\Omega$$

$$R1 = (5 - 1.2)\ k\Omega = 3.8\ k\Omega$$

To set the current limiting:

$$R_{CL} = \frac{0.5}{I_{PK}} = \frac{0.5}{0.5} = 1\ \Omega$$

$$R_{CL} = 1\ \Omega$$

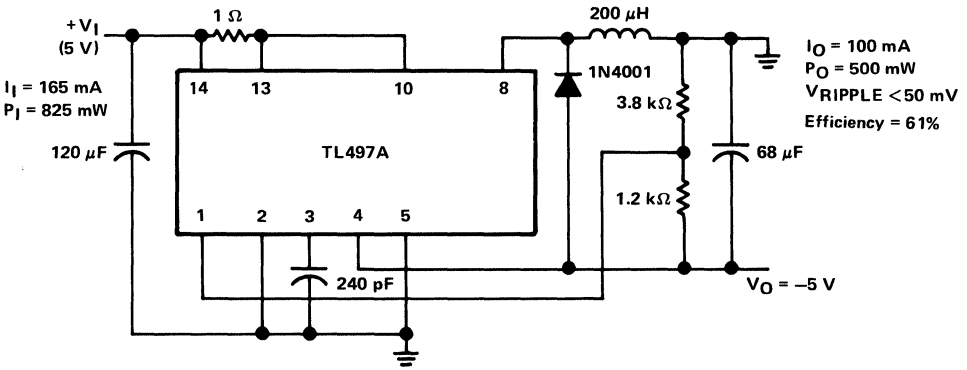
$$C_F = \frac{(I_{PK} - I_L)^2}{(V_{ripple})\ 2\ I_{PK}} \times \frac{t_{on}\ V_I}{V_O}$$

To determine C_{filter} for desired ripple voltage:

$$C_F = \frac{(I_{PK} - I_L)^2}{(V_{ripple})\,2\,I_{PK}} \times \frac{t_{on}\,V_I}{|\,V_O\,|}$$

$$= \frac{(0.5 - 0.1)^2}{(0.05)2 \times 0.5} \times \frac{20 \times 10^{-6} \times 5}{|\,-5\,|}$$

$$C_F = 64\ \mu F \text{ (nearest standard value } = 68\ \mu F)$$



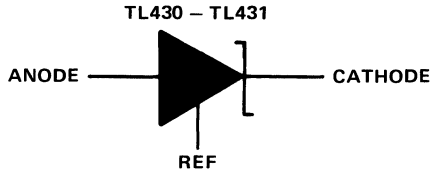
NOTE – Do not use internal diode (Pins 6, 7) on an inverting circuit.

Figure 38. +5-V to −5-V Switching Regulator

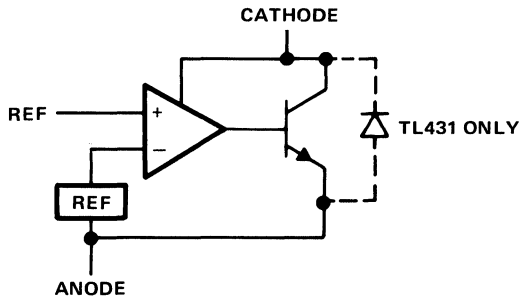
Adjustable Shunt Regulator TL430 - TL431

The TL430 and TL431 are three-terminal "programmable" shunt regulators. The devices are basically the same except the TL431 contains a diode connected between the emitter and collector of the output transistor. The standard symbol and block diagram are shown in Figure 39.

The circuit consists of a bipolar operational amplifier driving an n-p-n transistor. The reference on the TL430 is a band-gap reference (not temperature compensated). The TL431 has a true-temperature compensated band-gap reference and is more stable and accurate than other shunt regulators. The TL431 also has a diode across the emitter-collector of the n-p-n output transistor. If the cathode goes negative, the diode conducts around the transistor, emulating the performance characteristics of a normal zener diode. The basic operating characteristics are shown in Figure 40.



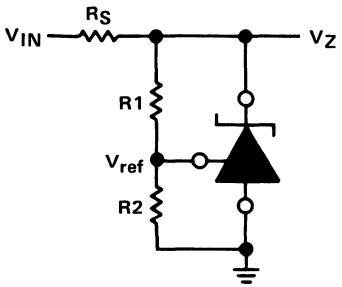
(a) SYMBOL

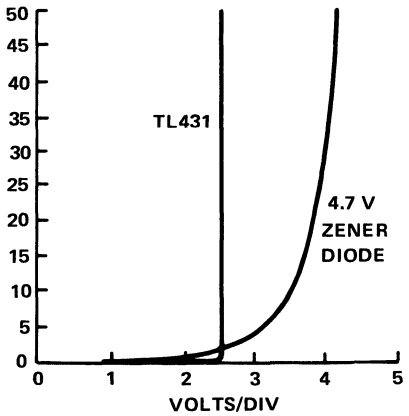


(b) BLOCK DIAGRAM

Figure 39. Tl430/TL431 Adjustable Shunt Regulators

TL430, TL431 PROGRAMMABLE ZENERS





- TEMPERATURE COMPENSATED
- LOW DYNAMIC IMPEDANCE
- TYPICAL V_{ref}
- REGULATES FROM 1.0 - 100 mA OVER ADJUSTABLE VOLTAGE RANGE

	TL430	TL431
	200 ppm/°C	100 ppm/°C
	1.5 OHMS	0.2 OHMS
	2.75 V	2.5 V
	2.75-30 V	2.5-36 V

Figure 40. Basic Operating Characteristics

Their excellent thermal stability make these devices extremely attractive as a replacement for high-cost, temperature-compensated zeners. As seen in Figure 41, the TL431 offers improved characteristics, even at low voltages. Since the TL431 operates as a shunt regulator, it can be used as either a positive or negative voltage reference. The TL431 has an equivalent full-range temperature coefficient of 50 ppm/°C (typical) and has low output noise voltage. Note in the graph (Figure 41) that for a nominal 2.495-V reference the curve is essentially flat from 0°C to 70°C. Depending upon the zener voltage, the TL431 also has an extremely low dynamic impedance of about 0.2 Ω, compared to a standard zener diode's dynamic impedance of about 30 to 60 Ω.

A 2.5-V reference voltage is developed across R2 as shown in Figure 42. I_{ref}, the current input at the reference terminal, is about 10 μA. To maintain a steady reference, it is advisable to allow 1 mA of current flow through series resistors R1 and R2. This will assure a stable reference voltage independent of I_{ref} variations. The TL431 is available in either the commercial temperature range of 0° - 70°C or the military temperature range of −55° to +125°C.

$$R = \frac{V_I - (V_{be} + V_O)}{I_R}$$

$$R = \frac{32 - (2 + 24)}{10\ mA} = 600\ \Omega$$

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$R1 = 21.4\ k\Omega$$

$$R2 = 2.5\ k\Omega$$

The circuit in Figure 43 uses a TL431 as a regulator to control the base drive to a TIP660 series pass transistor. For good reference stability, a current flow of about 1 mA (I_2) though the resistor divider is recommended. A 2.5-V reference voltage is developed across R2, and R1 will develop a voltage drop of 21.5 V. The Darlington power transistor is used because of the reduced base drive requirement of the TIP660 which has a V_{be} (max) of about 2 V. The h_{FE} at 2.5-A I_C is about 1000, so it would only require about 2.5 mA of base drive to produce 2.5 A of output current. In calculating the value of the current limit resistor, R3, we assume about 7.5 mA of current through the TL431. The value of R3, therefore, would be 600 Ω and the current about 10 mA, so a 1/2-W resistor will suffice. This is a simple method of designing a medium output current power supply using only four components plus the series pass transistor.

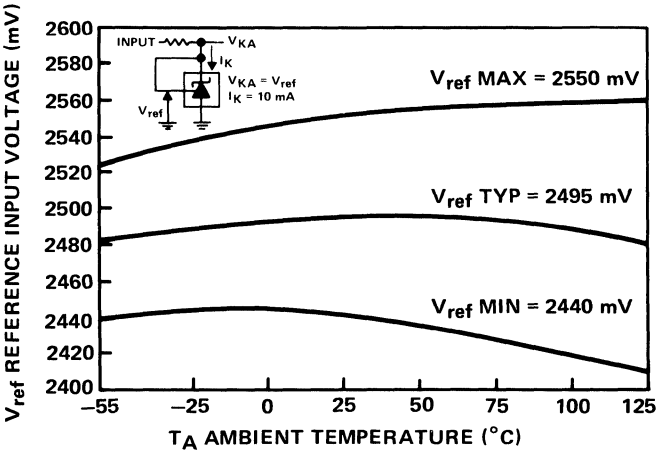


Figure 41. Reference Input Voltage vs Ambient Temperature

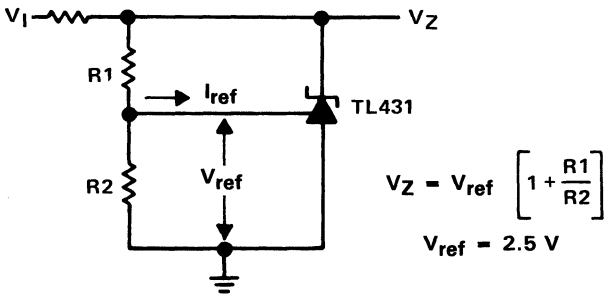


Figure 42. Basic Operational Circuit

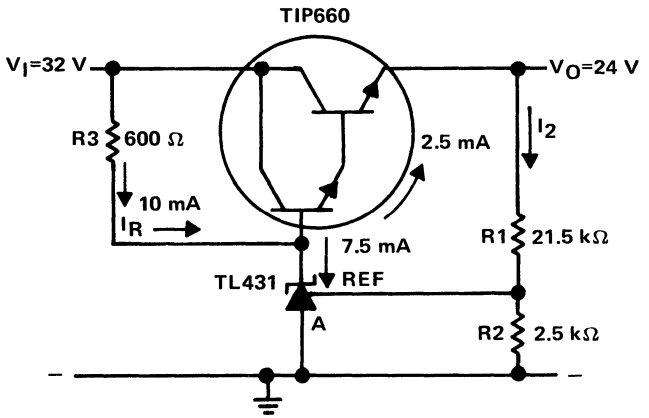


Figure 43. Series Regulator Circuit

Shunt Regulator Applications (Crowbar)

To protect solid-state electronic equipment from overvoltage due to a power-supply component failure, it is sometimes desirable to use a "crowbar" circuit. When a preset voltage is exceeded, the TRIAC turns on, shorting the output and blowing the fuse on the input side of the crowbar circuit. The circuit in Figure 44 is set to trip when V_O reaches 27 V. When that occurs, the reference voltage should be 2.5 V which turns on the TL431, thus biasing the SCR low. This turns the SCR on and immediately blows the safety fuse on the circuit input, thus protecting the equipment using this power supply.

$$V_L = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

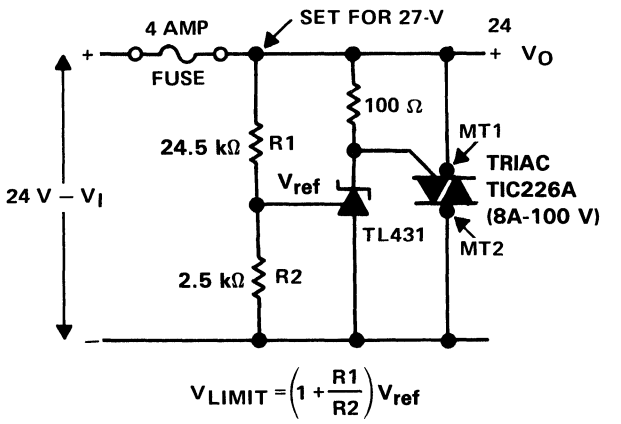


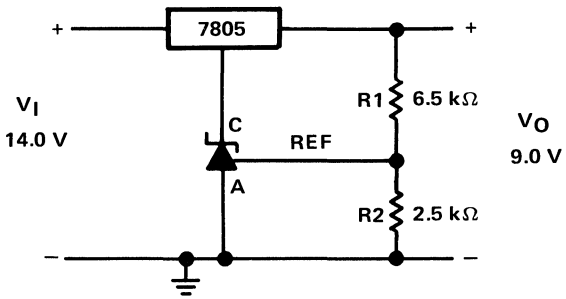
Figure 44. Shunt Regulator in Crowbar Circuit

Controlling V_O of a Fixed Output Voltage Regulator

Sometimes, it is necessary to have a regulated output voltage different from that for which the regulator is designed. This may be accomplished with any three-terminal regulator, although it should be noted that the lowest obtainable voltage will be 2.5 V for the TL431 plus the voltage of the three-terminal regulator. In the circuit in Figure 45, the lowest possible regulated voltage would be 7.5 V (2.5 V for the TL431 + 5 V for the 7805). This particular circuit provides 9-V output using a uA7805 three-terminal regulator.

Note: Minimum $V_O = V_{ref} + 5\ V$

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$



NOTE: MINIMUM $V_O = V_{ref} + 5.0\ V$

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 45. Fixed Output Shunt Regulator

Current Limiter

Figure 46 is an example of a current limiter designed to limit the current from a 12-V supply to 1.5 A using a TIP31 n-p-n transistor as the pass element. The value of R1 is calculated from the equation in Figure 46. The current through R1 is split almost equally in this circuit, with about 30 mA going to the TL431, and 30 mA for base drive to the TIP31. With a current load of 6 mA and an R1 value of 128 Ω, a 1/2-W resistor is sufficient. When the voltage across the current limit resistor (R_{CL}) reaches 2.5 V (TL431 reference voltage), the base drive to the TIP31 is reduced and the output current is limited to 1.5 A.

$$R1 = \frac{V_I - (V_{be} + V_{RCL})}{I_1} = \frac{12 - (1.8 + 2.5)}{0.06} = 128\ \Omega$$

$$R_{CL} = \frac{V_{ref}}{I_L} = \frac{2.5\ V}{1.5\ A} = 1.7\ \Omega$$

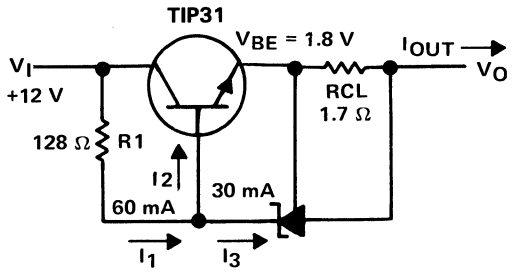
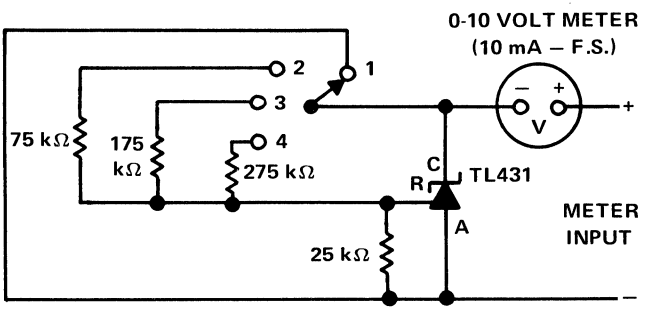


Figure 46. Current Limiter

Voltmeter Scaler

The circuit in Figure 47 is a voltmeter scaler (or multiplier) to extend the range of a 0- to 10-V voltmeter to 40 V. Most multiplier circuits extend the range with 0 V being the low reading on any given scale. This circuit actually divides the 40-V total range into 4 separate 10-V scales.

With the selector switch in position #1, the reference input of the TL431 is bypassed and the TL431 does not influence circuit operation. The meter is effectively connected directly to the voltage being measured. This scale would be the normal meter range of 0 to 10 V.



SWITCH POSITION	1	2	3	4
METER RANGE VOLTS	0-10	10-20	20-30	30-40

Figure 47. Voltmeter Scaler

When in position #2, a 75-kΩ and a 25-kΩ resistor are added in series across the anode and cathode of the TL431. The voltmeter will remain near zero until the input reaches 10 V. At this time, there is 2.5 V between the reference terminal and anode which causes the voltmeter to start reading at 10 V. It will continue reading on this scale until it reaches full scale, which is 20 V.

This sequence is repeated in 10-V steps until position #4 is reached. This circuit is very useful when expanded-scale voltmeter multiplication is required. The precision of the scaler depends upon the accuracy of the resistors.

Voltage-Regulated, Current-Limited Battery Charger for Lead-Acid Batteries

There are a number of approaches to recharging lead-acid batteries. Many will return the battery to service, but fail to fully rejuvenate the battery. To keep a battery fully charged, and attain maximum battery life, proper charging techniques must be observed.

The status of a cell is determined by the specific gravity of the electrolyte solution. A specific gravity of 1.280 (obtained by hydrometer reading) indicates a fully-charged cell. A reading of 1.250 or better is considered good. A fully-discharged cell exhibits a specific gravity of 1.150 or less.

Battery Charger Design

The battery charger design shown in Figure 48 is based on a charging voltage of 2.4 V per cell, in accordance with most manufacturers' recommendations. The battery charger circuit pulses the battery under charge with 14.4 V (6 cells × 2.4 V per cell) at a rate of 120 Hz.

The design provides current limiting to protect the charger's internal components while limiting the charging rate to prevent damaging severely discharged lead-acid batteries. The maximum recommended charging current is normally about one-fourth the ampere-hour rating of the battery. For example, the maximum charging current for an average 44 ampere-hour battery is 11 A.

If the impedance of the load requires a charging current greater than the 11-A current limit, the circuit will go into current limiting. The amplitude of the charging pulses is controlled to maintain a maximum peak charging current of 11 A (8 A average).

The charger circuit is composed of four basic sections:

1. Rectifier
2. Voltage Regulator
3. Current Limiting
4. Series-Pass Element

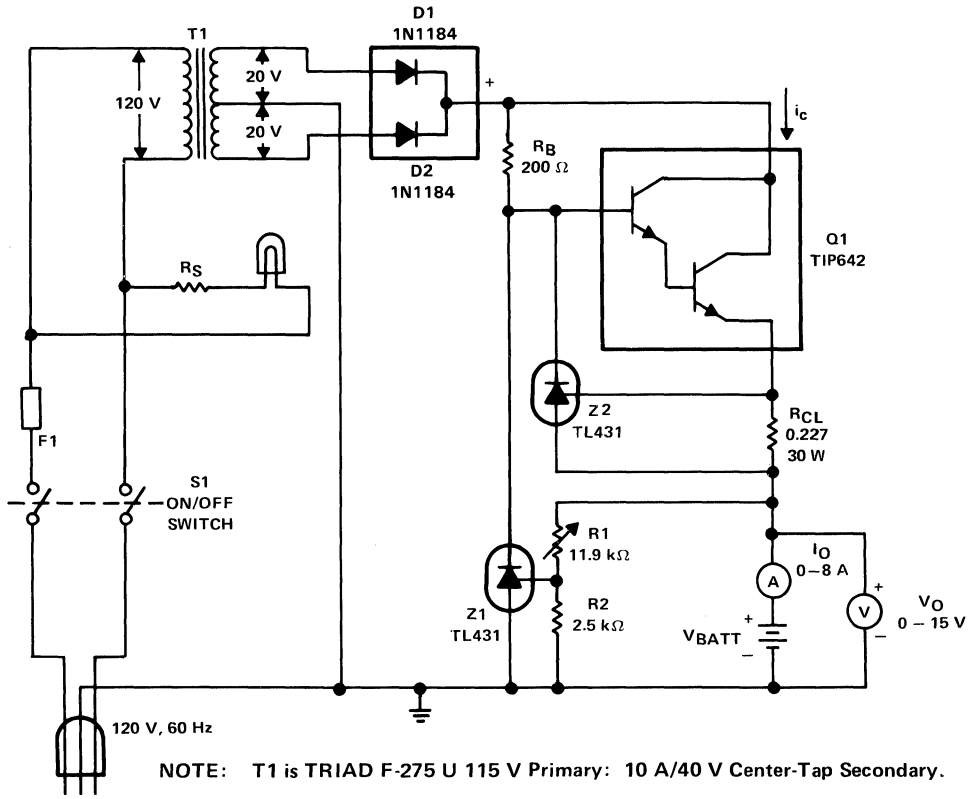


Figure 48. Current-Limited and Voltage-Regulated Battery Charger

Rectifier Section

A full-wave rectifier configuration with a center-tapped transformer (Figure 49) achieves maximum performance with minimum component count. The breakdown voltage requirement for the diode is:

$$VR > V_{secondary(pk)} - V_F(\text{rectifier drop})$$
$$\therefore VR > 20 \times 2.8 - 1 = 55 \text{ V}$$

This design is set to current limit at 11 A, therefore, a rectifier rating of 25 A is recommended to handle the maximum current drain plus any current surges. A pair of 1N1184 diodes was chosen (35-A/50-V rectifiers).

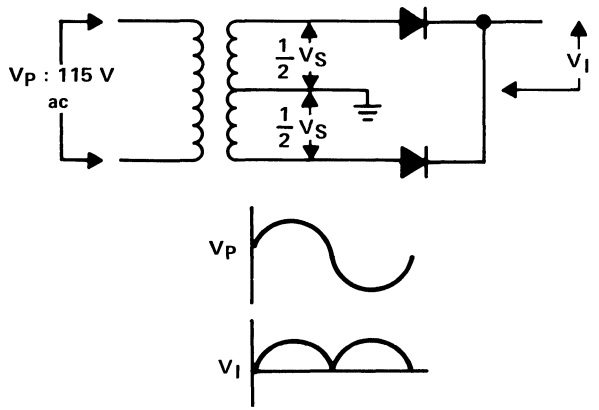


Figure 49. Full-Wave Rectifier Section of Circuit

Voltage Regulator Section

The components which make up the voltage regulator portion of the circuit are: Z1, Q1, R1, R2 and R_B as shown in Figure 50. Z1 is a TL431 programmable shunt regulator which serves as the control element, Q1 is the pass transistor, and R1 - R2 sense the output voltage providing feedback to Z1. R1 and R2 are chosen so that their node voltage is 2.5 V at the desired output voltage. This node voltage is applied to the TL431's error amplifier which compares it to the internal 2.5-V reference.

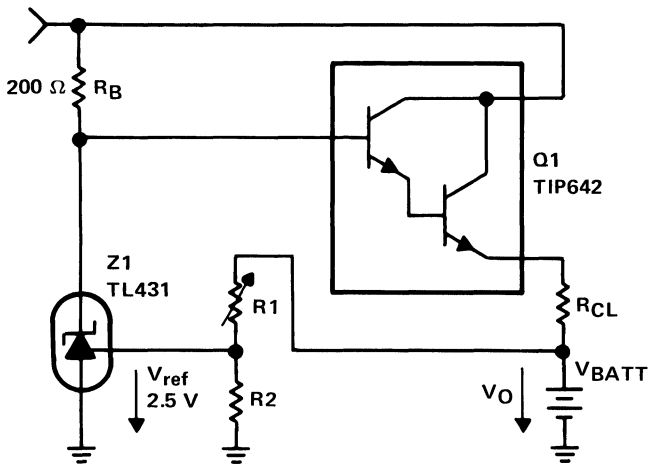


Figure 50. Voltage Regulator Section of Circuit

When the feedback voltage is less than the internal 2.5-V reference, the series impedance (anode-to-cathode) of the TL431 increases, decreasing the shunt current through the TL431. This increases the current available to the base of pass transistor Q1, increasing the output voltage. When the feedback voltage is greater than the internal 2.5-V reference, the series impedance of the TL431 decreases, increasing the shunt current through the TL431. This decreases the current available to the base of Q1, decreasing the output voltage. Because the feedback voltage is sensed at the output, the TL431 will compensate for any changes in the base-emitter drop of Q1 or the voltage dropped across R_{CL} for various currents.

Current Limiter Section

The components which make up the current-limit portion of this circuit are: Z2, Q1, and R_{CL} as shown in Figure 51. The value of the current-limit setting resistor, R_{CL}, is chosen so that 2.5 V will be developed across it at the desired limit current. The voltage across R_{CL} is sensed by a TL431 programmable shunt regulator (Z2). When the output current is less than the current limit, V_{ref} is less than 2.5 V and Z2 is a high impedance which does not affect the operation of Q1.

When the output current reaches maximum, V_{ref} is 2.5 V and the impedance of Z2 decreases, decreasing the current available at the base of Q1 and controlling the maximum output current. Under this condition, shunt regulator Z2 takes control of pass transistor Q1 and maintains a constant current, even into a short circuit.

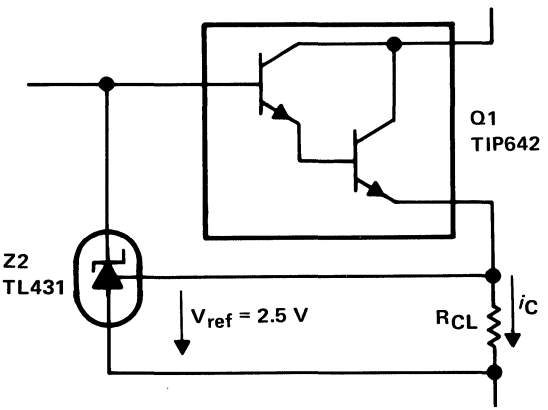


Figure 51. Current Limiter Section of Circuit

Series Pass Element

The series pass element used in this configuration is a conventional Darlington power transistor, whose control is derived from either Z1 or Z2 depending on the state of the battery being charged. See Figure 52.

The performance characteristics of Q1 are important in determining the circuit design and in the choice of the transformer to be used. This relationship is shown in the following section on the design of the battery charger.

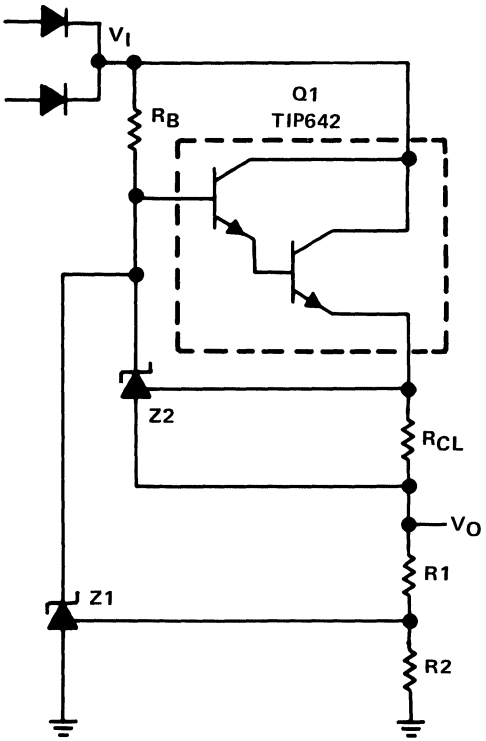


Figure 52. Series Pass Element

Design Calculations

The values of R1 and R2 set the output voltage level at 2.4 V per cell or 14.4 V for 6 cells. For optimum performance of Z1, 1 mA should flow through the R1 and R2 combination.

$$R1 + R2 = \frac{14.4\ V}{1\ mA} = 14.4\ k\Omega$$

$$R2 = \frac{2.5\ V}{1\ mA} = 2.5\ k\Omega$$

$$R1 = 14.4\ k\Omega - 2.5\ k\Omega = 11.9\ k\Omega$$

For ease of final adjustment, a 20-kΩ potentiometer may be used for R1.

Current limiting starts when 2.5 V is developed across R_{CL} at the desired current limit. For a 44-A hour battery, the maximum charge rate is 11 A.

$$R_{CL} = \frac{2.5\ V}{11\ A} = 0.227\ \Omega$$

The average current = 0.707 × 11 A = 7.777 A or ≈ 8A

The average power dissipation = $I^2R = 8^2 \times 0.227 = 14.5$ W

After the pass transistor has been selected, its base drive resistor, R_B, may be calculated. A TIP642 meets the requirements. From the data sheet:

h_{FE} @ 11 A = 500 (min)
$V_{CE} \approx 2$ V
$V_{BE} = 1.6$ V
$P_{max} = 160$ W @ 40°C TC
$I_B = 22$ mA @ 11-A peak-collector current

To calculate R_B, assume a worst case or short-circuit condition where:

$$R_B \approx \frac{V_I - V_{ref} - V_{BE(Q1)}}{I_{B(Q1)} + I_{SHUNT(Z_2)}}$$

$$R_B \approx \frac{27.28 - 2.5 - 1.6}{0.022 + 0.12} = 163\ \Omega$$

R_B must be small enough so that it does not limit the base current of Q1 at the desired I_{CHG} of 8 A, but large enough to limit the current during short circuit conditions. This value should be less than the sum of the base drive current required by Q1 and $I_{SHUNT(max)}$ Z2.

$$R_B \approx \frac{(V_I - 14.4\ V - 2.5\ V - V_{BE(Q1)})}{I_{CHG}/h_{FE(Q1)}}$$

$$= \frac{27.28 - 14.4 - 2.5 - 1.6}{8/500}$$

$$R_B \approx \frac{8.78}{0.016} = 548.7\ \Omega$$

A value of R_B within this range assures sufficient drive to Q1 for a charging rate of 8 A, yet allows total control of Q1 by Z2 during short-circuit conditions. R_B was selected to be 200 Ω.

Power Dissipation and Heat Sinking

To determine the power dissipation in the 1N1183 rectifier and the TIP642 Darlington, the RMS currents and voltages must be calculated. The voltage and current paths are shown in Figure 53.

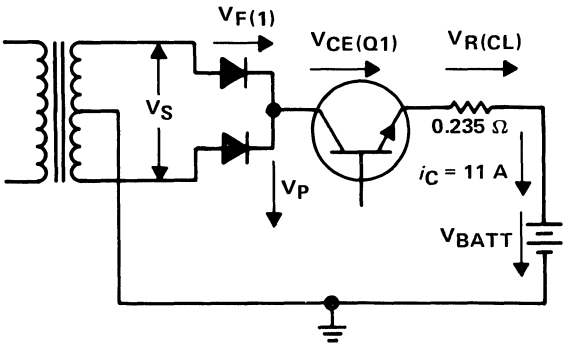


Figure 53. Voltage and Current Path

$$V_{CE(Q1)} = V_I - V_{BATT} - V_{RCL} = 27.78 - 14.4 - 2.5 = 10.88\ V$$
$$V_{CE(Q1)} = 10.9\ V$$

The transistor power dissipation is:

$$P_{Q1} = I_{(RMS)} \times V_{CE(RMS)} = (11\ A \times 0.707)(10.9\ V \times 0.707)$$
$$P_{Q1} = (7.78\ A)\ (7.7\ V)$$
$$P_{Q1} = 59.9\ W$$

The rectifier power dissipation is:

$$P_{(RECT)} = I_{(RMS)} \times V_F = (7.78\ A)\ (1.3\ V)$$
$$P_{(RECT)} = 10.1\ W \text{ total}$$

If the pass transistor and rectifiers are mounted on separate heat sinks, the sinks must be capable of dissipating the heat transferred by each device and maintain a surface temperature which satisfies the temperature requirement for each device. Mounted separately, the respective heat sink requirements are as follows:

PASS TRANSISTOR	RECTIFIERS
$R_{\theta CA} \leq \frac{150°C - 25°C}{59.9\ W}$	$R_{\theta CA} < \frac{140°C - 25°C}{10.1\ W}$
$R_{\theta CA} \leq 2.08°C/W$	$R_{\theta CA} < 11.4°C/W$

Depending on the mass of the heat sink and the type of cabinet, forced air cooling may be required.

Voltage Supply Supervisor Devices

Voltage supply supervisor devices deliver a digital output signal (high or low) if supply voltage (V_{CC}) falls below a predefined value. The digital output signal remains in its high or low state for a certain period of time (t delay) after V_{CC} returns to normal. These devices are used to sequentially initialize digital systems for proper operation at power-on or following a V_{CC} interruption.

The versatility, few external components, and accurate threshold voltage of the TL7700 series make these devices easy to use in digital systems requiring V_{CC} line supervision.

General Operation

At power-on, digital systems must normally be forced into a definite initial state. In simple microcomputer and microprocessor applications, an RC network connected to the RESET input pin will generally suffice. However, in more complex systems, a discrete component design as illustrated in Figure 54 may be used.

In this circuit, after V_{CC} reaches a specific value, defined by Z_D, the input voltage divider, and V_{BE}, the collector of Q2 becomes high and coupling capacitor C1 provides enough power to the RESET input pin of the digital system to execute the reset function.

The major deficiency with this type of circuit is that after power-on and the system is operating, low V_{CC} conditions and short drops in V_{CC} may not be recognized. A small decrease of V_{CC} below the recommended supply voltage can destroy the content of the memory and registers without activating the reset circuit. This may have catastrophic

consequences. Moreover, the circuit in Figure 54 contains an excessive number of components, one being Z_D, which has to be specially selected and is therefore relatively expensive.

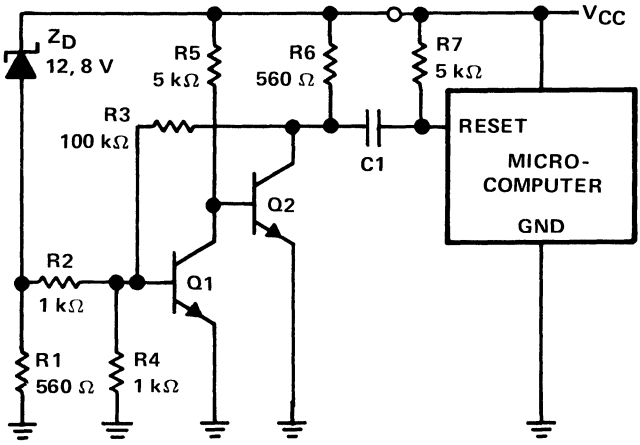


Figure 54. Discrete Solution of a Voltage Supply Supervisor

Several features are provided in larger computers to prevent some of the problems just mentioned. In some cases, the content of the memory is protected by a battery back-up. However, for most applications and in small microcomputer systems, these solutions are too expensive and generally not required. After any serious voltage drop, it is usually sufficient to force the microcomputer into a defined initial condition. To implement this function, while preventing the problems previously mentioned, a chip with the following features is required:

1. Accurate detection of a serious voltage drop
2. Generation of a continuous reset signal while the supply voltage is not in the operational range to prevent undefined operations.
3. Maintenance of the reset signal for a certain time after the supply voltage has returned to its nominal value to ensure a proper reset.

TL77XXA Series Supervisor Chips

A functional block diagram of the chip is illustrated in Figure 55. The most critical element of this chip is the reference voltage source, which consists of a very stable, temperature-compensated bandgap reference. An external capacitor (typically 0.1 μF) must be connected to the Reference (REF) voltage output to reduce the influence of fast transients in the supply voltage. The voltage at the SENSE INPUT pin is divided by resistors R1 and R2 and compared with the reference voltage. The divider is adjusted to achieve high accuracy at the probing operation during manufacture of the chip.

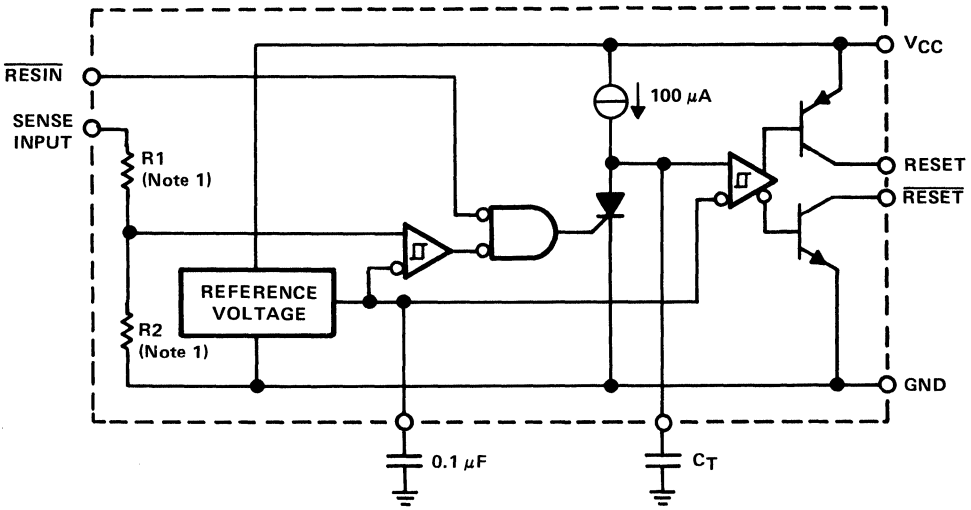


Figure 55. TL77XXA Series Function Block Diagram

When the sensed input voltage is lower than the threshold voltage, the thyristor is triggered discharging the timing capacitor C_T. It is also possible to fire the thyristor with a TTL logic level (active low) at the $\overline{\text{RESIN}}$ input. The thyristor is turned off again when the voltage at the SENSE INPUT (or $\overline{\text{RESIN}}$ input) increases beyond the threshold, or during short supply voltage drops when the discharge current of the capacitor becomes lower than the hold current of the thyristor. Capacitor C_T is recharged by a 100-μA current source; the charge time is calculated as follows:

t_d (internal time delay) = C_T (1.3×10^4)

A second comparator forces the output into the active state as long as the voltage at the capacitor is lower than the reference voltage. Figure 56 is a graph plotting C_T versus t_d. The SENSE INPUT pin is connected to V_{CC} in typical applications. Figure 57 shows the timing of the supply voltage and $\overline{\text{RESET}}$ signals.

The minimum supply voltage for which operation is guaranteed is 3 V. Between POWER-ON (0 V) and 3 V, the state of the outputs is not defined. In practical applications, this is not a limitation because the function of the reset inputs of the other devices is not guaranteed at such supply voltages.

Above 3 V, capacitor C_T is discharged and the outputs stay in the active state. When the input voltage exceeds the threshold voltage, V_S, the thyristor is turned off and

capacitor C_T is charged. After a delay of t_d, the voltage passes the trigger level of the output comparator and the outputs become inactive. The microcomputer is then set to a defined initial state and starts operation.

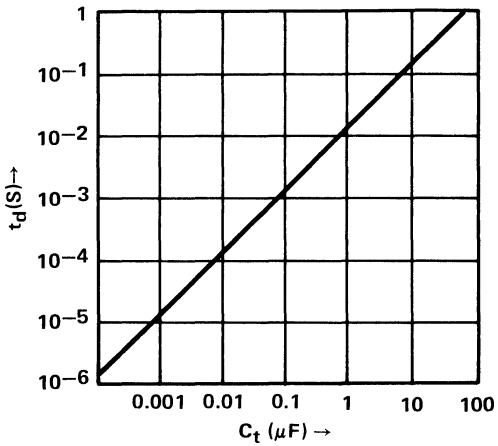


Figure 56. Graph for Calculation of C_T

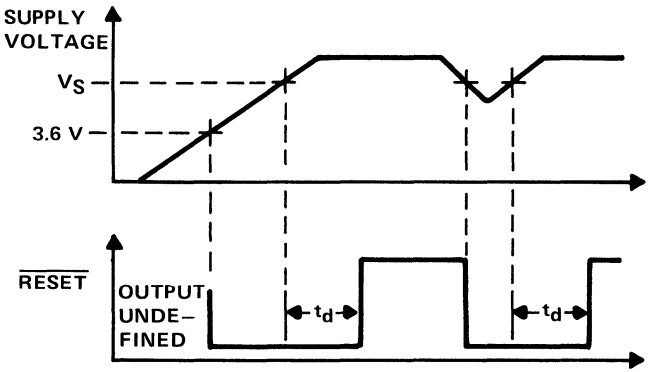


Figure 57. Timing Diagram

Operation During a Voltage Drop

The thyristor is triggered when the supply voltage drops below the minimum recommended value. After the supply returns to its required value, the output stays in the active state for the duration of t_d.

The delay time, t_d, is determined by the requirements of the computer system to be controlled. Typically, in TTL systems, a reset time of 20 to 50 ns is sufficient.

Microcomputers usually require a reset signal which lasts several machine cycles. The duration of the reset signal is dependent on the type of microcomputer, but is typically 10 to 200 μs. In most practical applications, t_d is determined by the characteristics of the power supply.

During and shortly after power-on make sure voltage fluctuations do not repetitively reset the system. Delay times of 10 to 20 ns will usually prevent this problem. Four versions of this device are available:

	Threshold Voltage	V_{CC}
TL7702A	2.53 V	3.0 — 18.0 V
TL7705A	4.55 V	5.0 V
TL7712A	10.8 V	12.0 V
TL7715A	13.5 V	15.0 V

The TL7702A may be used in applications where V_{CC} voltages up to 18 V are used. The required trigger level (2.5 V) may be set with a resistor divider network at the SENSE INPUT pin. The TL7705A, TL7712A, and TL7715A have an internal resistor divider network and operate on 5 V, 12 V, and 15 V, respectively.

TL77XXA Series Applications

Since, for most applications, the devices are already adjusted to the appropriate voltage levels, these chips are easy to use. Figure 58 illustrates an undervoltage protection circuit for a TMS370 microcomputer system with a 5-V power supply. External components are the 0.1-μF bypass capacitor at the REF terminal, which reduces transients from the supply voltage, and the C_T capacitor, which sets the time delay (t_d). The TL7705A devices do not have internal pull-up (or pull-down) resistors. An external 10-kΩ pull-up resistor is connected from the RESET pin to the 5-V V_{CC} to produce a high level. A similar application is illustrated in Figure 59.

This circuit utilizes a TL7715A as a protection device for a TMS1000 microcomputer system. The C_T and reference bypass capacitors are also used in this application. Note, however, the absence of the pull-up resistor used in Figure 58. This circuit has a required internal pull-down resistor at the INIT INPUT pin on the TMS1000 microcomputer chip.

In large systems, where several supply voltages are required (e.g., TMS8080, TMS9900), it is necessary to supervise all supply voltages that may cause dangerous conditions if a power failure or transient occurs. The circuit illustrated in Figure 60 uses two TL7712A devices to check the positive and negative 12-V supplies. A TL7705A is used to check a 5-V supply.

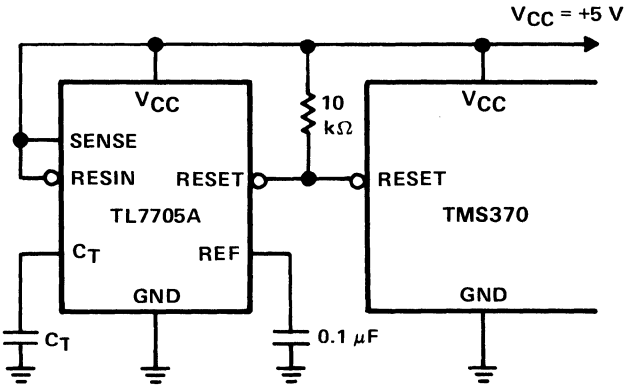


Figure 58. TL7705A in 5-V Microcomputer Application

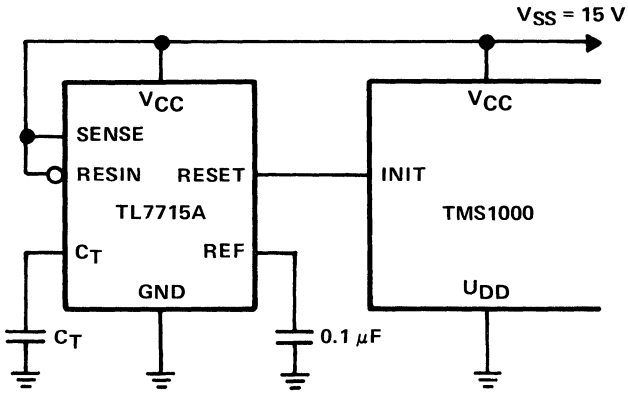


Figure 59. TL7715A in TMS1XXXNLP Application

The outputs of the two TL7712As are fed to the $\overline{\text{RESIN}}$ input of the TL7705A. The output of this device, a system-reset signal, becomes active when any one of the three supply voltages fail. The supply voltage supervisor devices were designed to detect very short voltage drops of 150 ns. In applications where this sensitivity is not required, the circuit may be delayed by adding an RC network ahead of the SENSE INPUT pin (Figure 61). To avoid influence on the threshold voltage of this input, the resistor should be less than 22 Ω. The capacitor C_d is then calculated to the required delay time (C_d = t/R).

Another application for the TL7705A is in battery-buffered memory systems. After a line-voltage failure, the content of the memory has to be protected against spikes on the write line. It is usually sufficient to switch the chip-select line into the inactive state; however, some memories also require that the write line be disabled. See Figure 62.

A switch, formed by transistor Q1 and diode D1, is inserted into the chip-select line of the memory. Under normal operation (line voltage present), the RESET output of the TL7705A is turned off (high), transistor Q2 is turned on, and transistor Q1 draws its base current through transistor Q2 and resistor R1. When the chip-select line is switched from high to low, transistor Q1 conducts and the CS input of the memory goes low. Because of the small dc load of resistor R2, the saturation voltage of the transistor is very small (typically 40 mV). When the chip-select line is switched high again, transistor Q1 is turned off and diode D1 conducts, charging the circuit capacitance.

In case of a power failure, the TL7705A is triggered and its RESET output becomes low, turning off transistor Q2 and the base current to transistor Q1. In this way, the CS input of the memory is separated from the chip-select line. In some cases, it is also recommended that memory be disabled during the system reset with the $\overline{\text{RESIN}}$ input. This protects the memory content against spikes on the write line during this time.

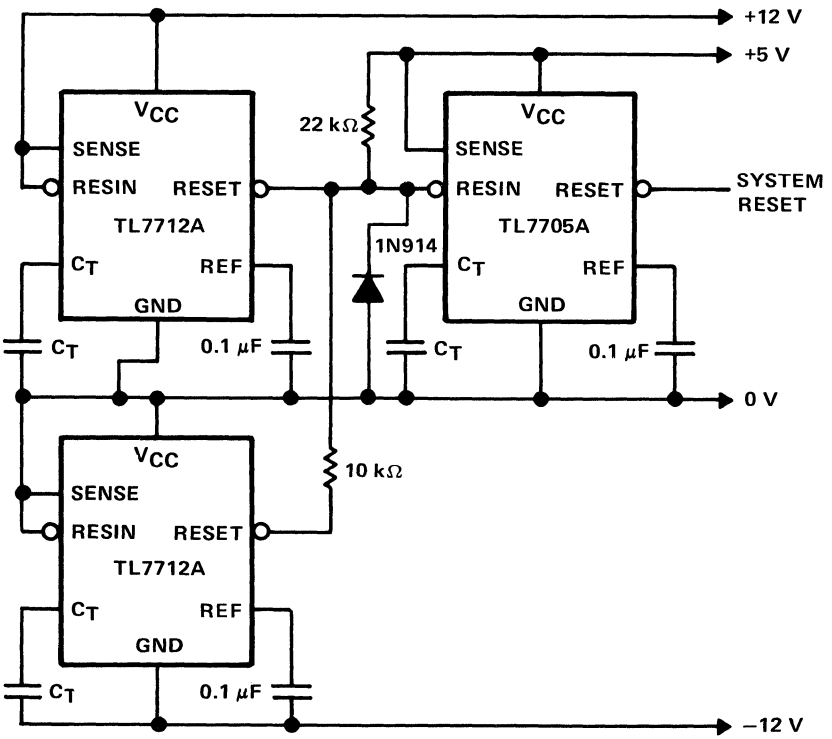


Figure 60. Voltage Supervision of a Multiple Power Supply

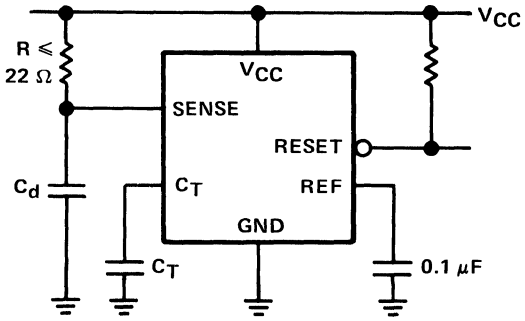


Figure 61. Delayed Triggering

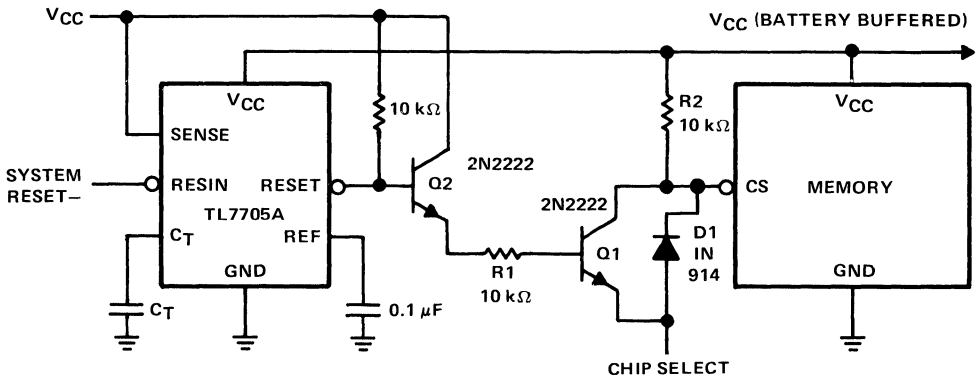


Figure 62. Circuit Diagram for Memory Protection

uA723 Precision Voltage Regulator

The uA723 monolithic integrated circuit voltage regulator is used extensively in power supply designs. The device consists of a temperature-compensated reference amplifier, an error amplifier, a 150-mA series-pass transistor, and current-limiting circuitry. See Figures 63 and 64 for the functional diagram and schematic.

Additional external n-p-n or p-n-p pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition, the device features low standby current drain, low-temperature drift and high-ripple rejection. The uA723 may be used with positive or negative supplies as a series, shunt, or floating regulator.

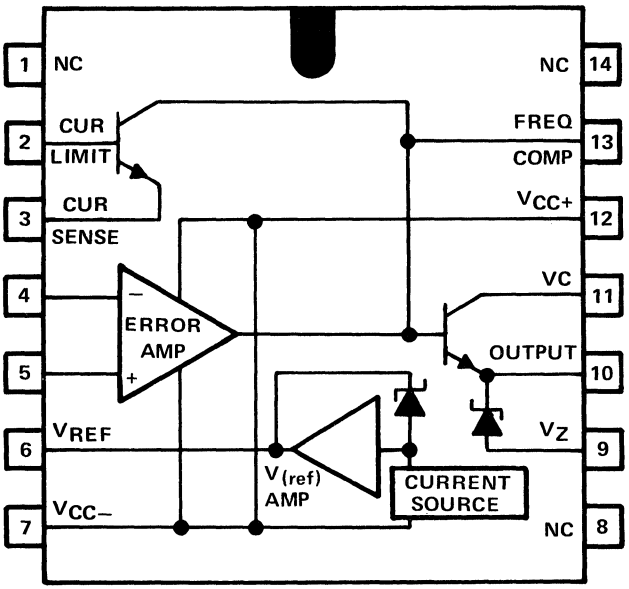


Figure 63. uA723 Functional Block Diagram

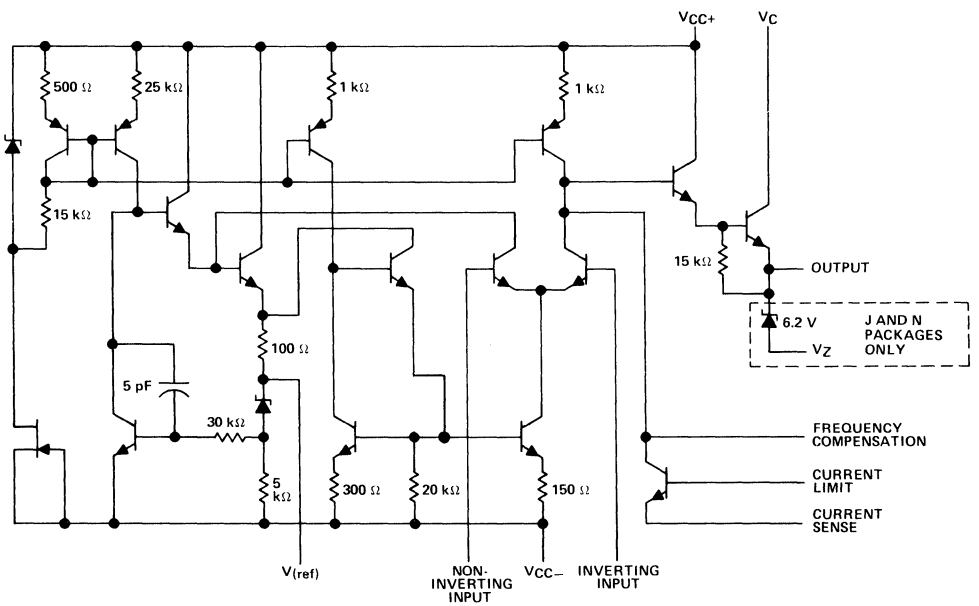


Figure 64. uA723 Schematic

When using an external series pass device, the 3-dB bandwidth of the uA723 must also be taken into consideration. Adequate uA723 compensation may be provided by connecting a 100- to 500-pF capacitor from the compensation terminal to the inverting input. Extra capacitance may be required at both the input and output of any power supply due to the inductive effects of long lines. Adding output capacitance provides the additional benefit of reducing the output impedance at high frequencies.

Typical Applications

The required output voltage and current limits for the applications shown in Figure 65 can be calculated from the equations given in Table 1. In all cases, the resulting resistor values are assumed to include a potentiometer as part of the total resistance. Table 2 affords a quick reference for many standard output voltage requirements.

Table 1. Formulas for Output Voltages

Outputs from 2 to 7 V
[Figures 65(a), (e), (f)]

$$V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$$

Outputs from 7 to 37 V
[Figures 65(b), (d), (e), (f)]

$$V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$$

Outputs from -6 to -250 V
[Figure 65(c)]

$$V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$$

$$R3 = R4$$

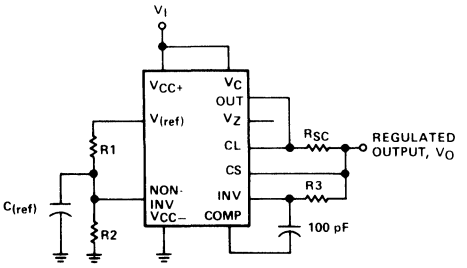
Current Limiting

$$I_{(limit)} \approx \frac{0.65\ V}{R_{SC}}$$

Foldback Current Limiting
[Figure 65(f)]

$$I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)0.65\ V}{R_{SC}\ R4}$$

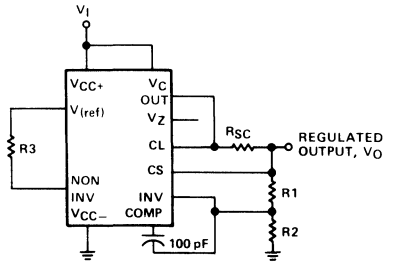
$$I_{OS} \approx \frac{0.65\ V}{R_{SC}} \times \frac{R3 + R4}{R4}$$



NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum αV_O.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

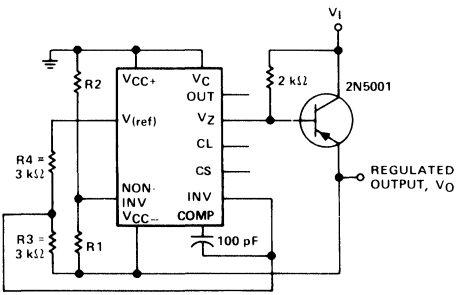
(a) BASE LOW-VOLTAGE REGULATOR (V_O = 2 to 7 V)



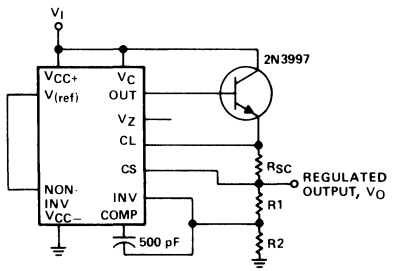
NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum αV_O.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

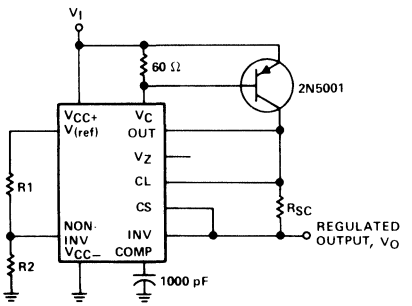
(b) BASIC HIGH-VOLTAGE REGULATOR (V_O = 7 to 37 V)



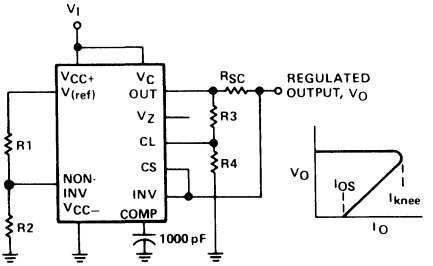
(c) NEGATIVE-VOLTAGE REGULATOR



(d) POSITIVE-VOLTAGE REGULATOR (EXTERNAL N-P-N PASS TRANSISTOR)



(e) POSITIVE-VOLTAGE REGULATOR (EXTERNAL P-N-P PASS TRANSISTOR)



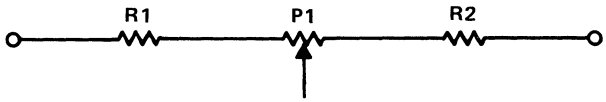
(f) FOLDBACK CURRENT LIMITING

Figure 65. Typical Applications

Table 2. Resistor Values for Standard Output Voltages

OUTPUT VOLTAGE (V)	APPLICABLE FIGURE (65) SEE NOTE 1	FIXED OUTPUT ± 5% kΩ		ADJUSTABLE OUTPUT ± 10% kΩ		
		R1	R2	R1	P1	R2
+5.0	a, e, f	2.15	4.99	0.75	0.5	2.2
+6.0	a, e, f	1.15	6.04	0.5	0.5	2.7
+9.0	b, d, e, f	1.87	7.15	0.75	1.0	2.7
+12.0	b, d, e, f	4.87	7.15	2.0	1.0	3.0
+15.0	b, d, e, f	7.87	7.15	3.3	1.0	3.0
−9.0	c (see note 2)	3.48	5.36	1.2	0.5	2.0
−12.0	c (see note 2)	3.57	8.45	1.2	0.5	3.3
−15.0	c (see note 2)	3.57	11.5	1.2	0.5	4.3

NOTES: 1. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown here.



2. For negative output voltages less than 9 V, $V_{CC}+$ and V_C must be connected to a level large enough to allow the voltage between $V_{CC}+$ and $V_{CC}-$ to be greater than 9 V.

General-Purpose Power Supply

The general-purpose power supply shown in Figure 66 may be used for supply output voltages from 1 to 35 V. The line transformer should be selected to give about 1.4 times the desired output voltage from the positive side of the filter capacitor, C1, to ground. R1 discharges the carriers in the base-emitter junction of the TIP31 when the drive is reduced. Its value is determined as follows:

$$R1 = \frac{\text{TIP31 voltage (at point of conduction)}}{\text{leakage current of TIP31 and uA723 output}}$$

where:

TIP31 voltage at point of conduction is 0.35 V, leakage current (collector-base) of the TIP31 plus the collector-emitter leakage of the uA723 output transistor (worst case = 200 μA).

therefore:

$$R1 = \frac{0.35\ V}{0.0002\ A} = 1750\ \Omega \text{ max}$$

$$R1 = 1.5\ k\Omega \text{ (standard value)}$$

Potentiometer R2 sets the output voltage to the desired value by adjusting the reference input voltage. It is connected between pin 6 (7.15-V reference) and ground. The center arm of R2, connected to pin 5, will select any point between zero and the 7.15-V reference.

Resistors R3 and R4 are connected in series across the supply output. The junction of these two resistors is connected to the inverting input (pin 4) of the error amplifier establishing an output voltage reference. This voltage reference is compared to the selected voltage at the noninverting input to the error amplifier (pin 5) to set the level of output voltage regulation. The values for R3 and R4 are listed in Note 1 of Figure 66. R_{SC} is the current limit set resistor. Its value is calculated as:

$$R_{SC} = \frac{0.65\ V}{I_L}$$

For example, if the maximum current output is to be 1 A, $R_{SC} = 0.65/1.0 = 0.65\ \Omega$.

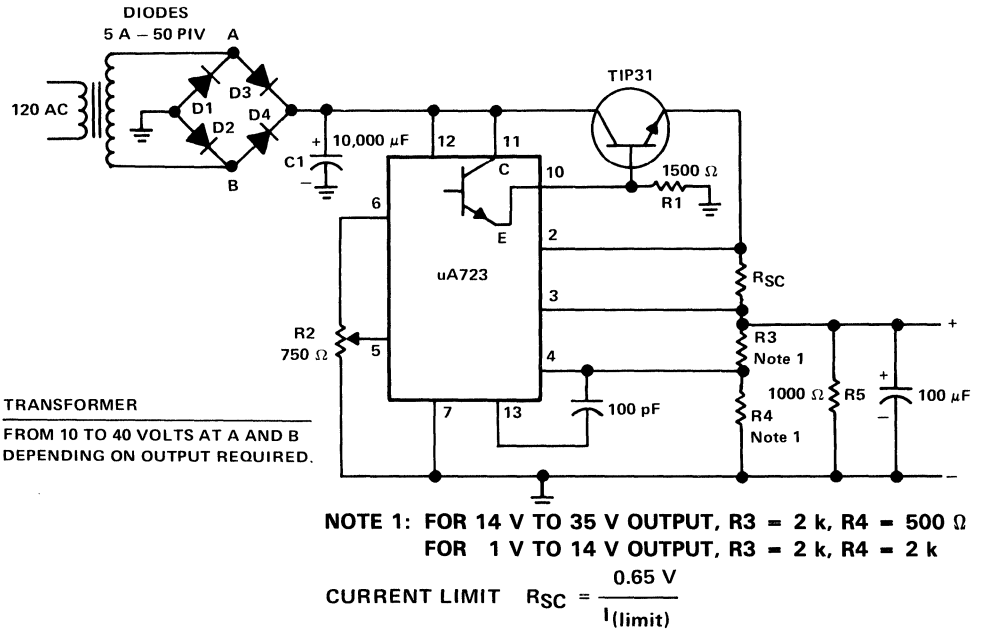


Figure 66. General-Purpose Power Supply

The 1-kΩ resistor, R_S, on the output is a light-load resistor designed to improve the no-load stability of the supply. The 100-μF electrolytic capacitor improves the overall output ripple voltage. A 100-pF capacitor from the compensation terminal (pin 13) to the inverting input (pin 4) allows for gain variations in the uA723 error amplifiers and for parasitic capacitances.

The output voltage and current of this supply must be restricted to the specifications of the TIP31 series pass transistor. Since it is rated at 2 W in free air at 25°C, sufficient heat sinking is necessary.

8-A Regulated Power Supply for Operating Mobile Equipment

It is often necessary to operate or test equipment used in automotive applications. This supply, as shown in Figure 67, provides up to 8 A at 13.8 V. The uA723 is used as the control element, furnishing drive current to series-pass transistors which are connected in a Darlington configuration. Two 2N3055 n-p-n transistors are used as the pass transistors, so proper heat sinking is necessary to dissipate the power.

This supply is powered by a transformer operating from 120 VAC on the primary and providing approximately 20 VAC on the secondary. Four 10-A diodes with a 100-PIV rating are used in a full-wave bridge rectifier. A 10,000-μF/36-VDC capacitor completes the filtering, providing 28 VDC.

The dc voltage is fed to the collectors of Darlington-connected 2N3055s. Base drive for the pass transistors is from pin 10 of the uA723 through a 200-Ω current limiting resistor, R1. The reference terminal (pin 6) is tied directly to the noninverting input of the error amplifier (pin 5), providing 7.15 V for comparison. The inverting input to the error amplifier (pin 4) is fed from the center arm of a 10-kΩ potentiometer connected across the output of the supply. This control is set for the desired output voltage of 13.8 V. Compensation of the error amplifier is accomplished with a 500-pF capacitor connected from pin 13 to pin 4.

The 1-kΩ resistor on the output is a light load to provide stability when the supply has a no load condition. The 100-μF/16-VDC electrolytic capacitor completes the filter action and reduces the ripple voltage. The current output of the supply is sampled through resistor R_{SC} between the output transistor and the output terminal. The resistor value for a 10-A maximum current is calculated from the formula:

$$R_{SC} = \frac{0.65\ V}{I_{(load\ max)}} = \frac{0.65}{10} = 0.065\ \Omega$$

If the power supply should exceed 8 A or develop a short circuit, the uA723 regulator will bias the transistors to cutoff and the output voltage will drop to near zero until the short circuit condition is corrected. This circuit features a no-load-to-full-load (8 A) voltage regulation of no more than 0.2-VDC variation (better than 2% regulation).

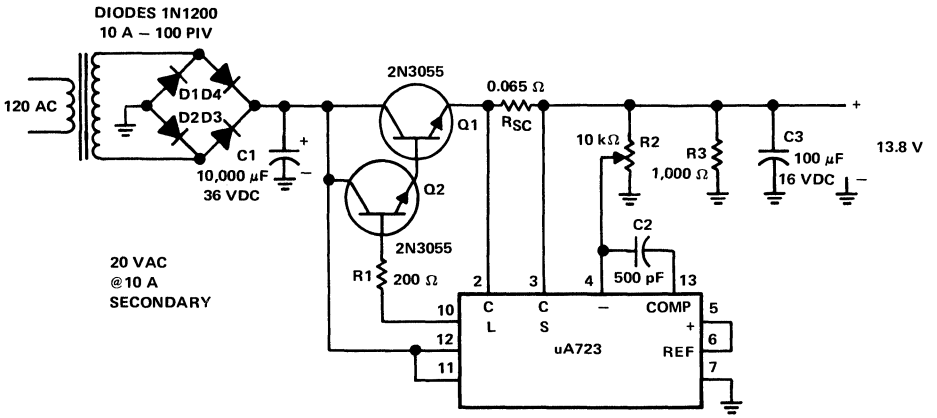


Figure 67. 8-A Regulated Power Supply

± 15 V at 1 A Regulated Power Supplies

When working with operational amplifiers, a common requirement is plus and minus supplies in the 15-V range. A positive 15-V supply is shown in Figure 68 and a negative 15-V supply is shown in Figure 69.

Positive Supply

The positive supply, shown in Figure 68, receives +20 VDC from the rectifier/filter section. This is applied to pins 11 and 12 of the uA723 as well as to the collector of the 2N3055 series-pass transistor. The output voltage is sampled through R1 and R2 providing about 7 V with respect to ground at pin 4.

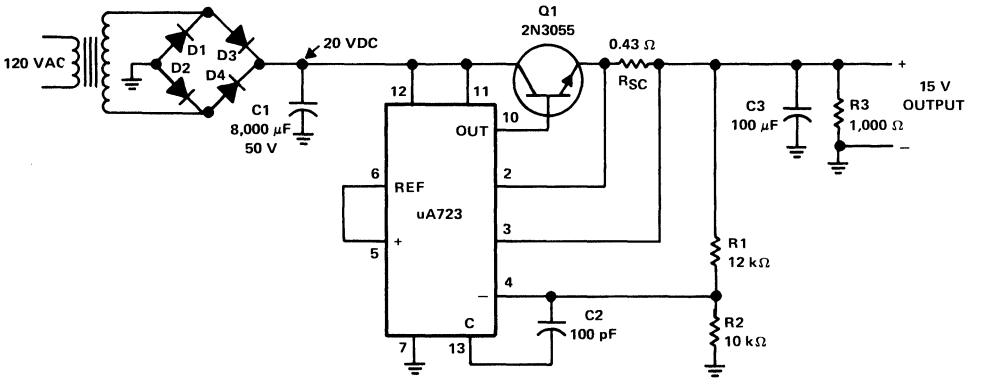


Figure 68. +15-V at 1-A Regulated Power Supply

The reference terminal (pin 6) is tied directly to pin 5, the noninverting input of the error amplifier. For fine trimming of the output voltage, a potentiometer may be installed between R1 and R2. A 100-pF capacitor from pin 13 to pin 4 furnishes gain compensation for the amplifier.

Base drive to the 2N3055 pass transistor is furnished by pin 10 of the uA723. Since the desired output of the supply is 1 A, maximum current limit is set to 1.5 A by resistor R_{SC} whose value is calculated as:

$$R_{SC} = \frac{0.65\ V}{I_{(max\ limit)}} = \frac{0.65}{1.5} = 0.433\ \Omega$$

A 100-μF electrolytic capacitor is used for ripple voltage reduction at the output. A 1-kΩ output resistor provides stability for the power supply under no-load conditions. The 2N3055 pass transistor must be mounted on an adequate heat sink since the 3.5-W, 25°C rating of the device would be exceeded at 1-A load current.

Negative Supply

The negative 15-V version of this power supply is shown in Figure 69. The supply receives −20 V from the rectifier/filter which is fed to the collector of the Darlington p-n-p pass transistor, a TIP105. A different uA723 configuration is required when designing a negative regulator.

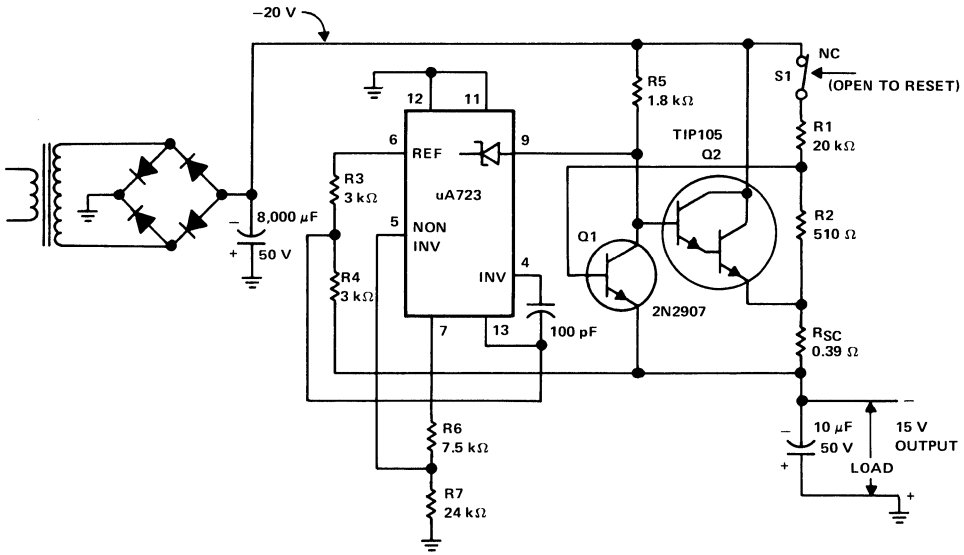


Figure 69. −15-V at 1-A Regulated Power Supply

The base drive to the TIP105 is supplied through resistor R5. The base of the TIP105 is driven from pin 9 (V_Z terminal), which is the anode of a 6.2-V zener diode that connects to the emitter of the uA723 output control transistor.

The method for providing the positive feedback required for foldback action is shown in Figure 69. This technique introduces positive feedback by increasing current flow through resistors R1 and R2 under short-circuit conditions. This forward biases the base-emitter junction of the 2N2907 sensing transistor, which reduces base drive to the TIP105.

The final percentage of foldback depends on the relative contributions of the voltage drop across R2 and R_{SC} to the base current of the 2N2907 sensing transistor. From the start of base-emitter conduction of the sense transistor to the full shut-off of the TIP105 pass transistor requires a 2-μA base current.

The latch condition, or 100% positive feedback, is generated by any change in the input voltage which increases the voltage drop across R2 turning on the sense transistor (2N2907). It can only be reset by breaking the positive feedback path with switch S1. This allows the series pass device to once more be driven in a normal fashion.

R3 and R4 are equal in value and divide the 7.15-V reference in half. The resulting 3.6-V reference is tied to the inverting input of the error amplifier. R6 and R7 are connected in series across the output of the power supply. The junction of R6 and R7 furnishes 3.6 V to the noninverting input of the error amplifier. At this point, the output is regulated at −15 V with respect to ground.

Resistors R1 and R2 are calculated as follows:

$$\begin{aligned} R1(k\Omega) &= V_I - {}^*V_{SENSE(V)} \\ &= 20 - 0.5 \\ &= 19.5\ k\Omega \end{aligned}$$

$$R1 = 20\ k\Omega \text{ (standard value)}$$

$$R2(k\Omega) = {}^*V_{SENSE(V)} = 0.5\ k \text{ or } 510\ \Omega \text{ (standard value)}$$

$$\text{Resistor R5} = (V_I - V_O - V_{BEQ2} - VR_{SC}) \times \frac{\text{(min beta Q2)}}{I_M \text{ (max load current)}}$$

$$R5 = (20 - 15 - 2.8 - 0.4) \times \frac{1000}{1} = 1800\ \Omega$$

$$R5 = 1.8\ k\Omega$$

*V_{SENSE} is defined as the base to emitter voltage needed to start turn-on of the 2N2907. From the data sheet this is about 0.5 V.

The current sense resistor R_{SC} is calculated as follows:

$$R_{SC} = \frac{V_O}{I_M}\left(\frac{V_{SENSE}}{V_I - V_{SENSE}}\right) = \frac{15}{1}\left(\frac{0.5}{20 - 0.5}\right) = 0.384\ \Omega$$

$$R_{SC} = 0.39\ \Omega$$

Foldback limiting, as used in this circuit, is advantageous where excessive pass transistor power dissipation is a problem. The TIP105 can tolerate only 2-W dissipation in free air at 25°C ambient, so adequate heat sinking is necessary.

Overvoltage Sensing Circuits

The use of SCR crowbar overvoltage protection (OVP) circuits is a popular method for providing protection from accidental overvoltage stress for a power supply load. The sensing function for this type of OVP circuit can be provided by a single IC, the MC3424, as shown in Figure 70.

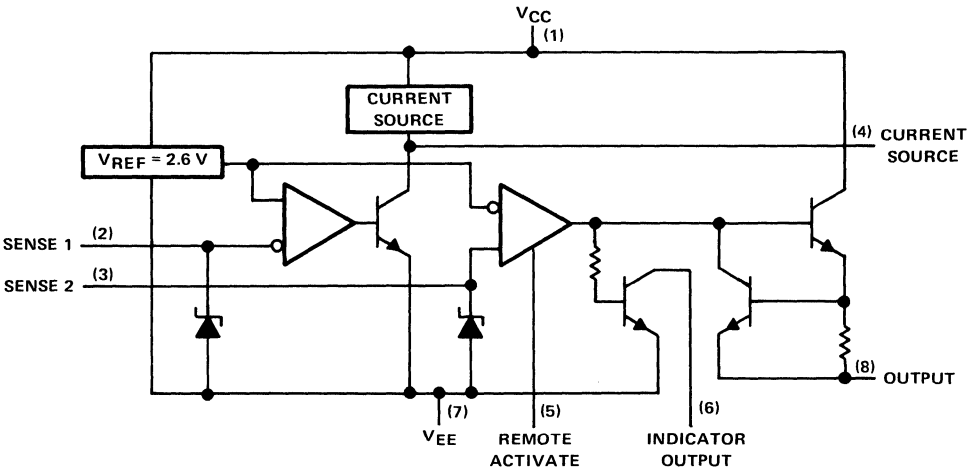


Figure 70. MC3423 Overvoltage Crowbar Sensing Circuit Block Diagram

The Crowbar Technique

One of the simplest and most effective methods of obtaining overvoltage protection is to use a crowbar SCR placed across the equipment's dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the input of the dc supply when an overvoltage condition is detected. A typical circuit configuration is shown in Figure 71.

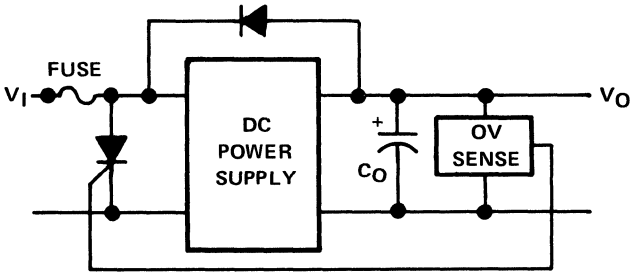


Figure 71. Typical Crowbar Circuit

The MC3423 operates from a V_{CC} minimum of 4.5 V to a maximum of 40 V. The input error amplifier has a 2.6-V reference between the noninverting input and V_{EE}. The inverting input is V_{sense1} (Pin 2) and is the point to which the output sense voltage is applied. This is usually done through a resistor voltage divider which sets the trip point (V_{ref}) at 2.6 V. The output of the device, pin 8, then triggers the gate drive terminal of the SCR. A basic OVP circuit is shown in Figure 72.

When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging capacitor C1 which is also connected to Pin 3. When triggered, pin 8 supplies gate drive through the current-limit resistor (RG) to the gate of the SCR. The minimum value of RG is given in Figure 73.

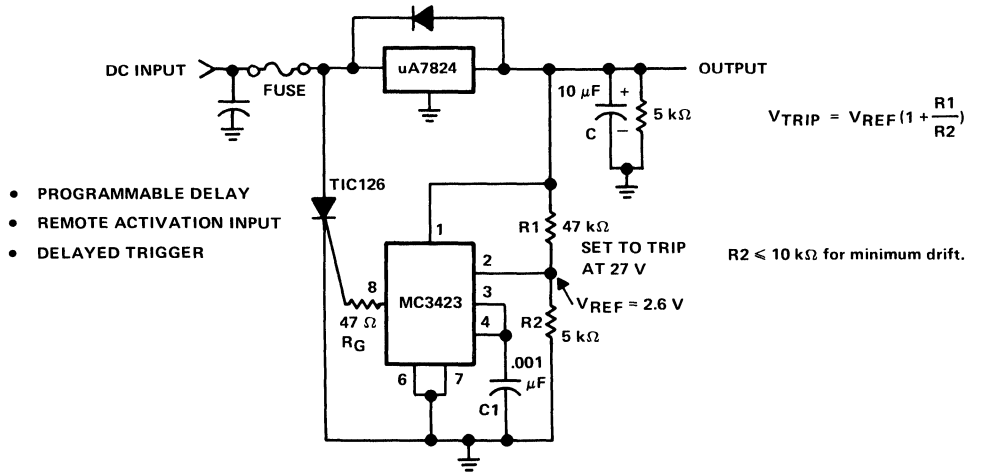


Figure 72. Overvoltage Protection Circuit

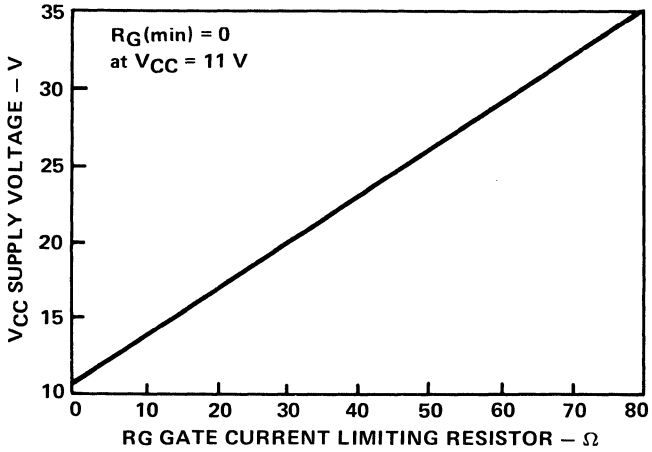


Figure 73. Minimum R_G vs Supply Voltage

The value of capacitor C determines the minimum duration of the overvoltage condition necessary to trip the OVP. The value of C can be determined from Figure 74. If the overvoltage condition disappears before C is charged, C discharges at a rate which is 10 times faster than the charging rate, and resets the timing feature until the next overvoltage condition occurs.

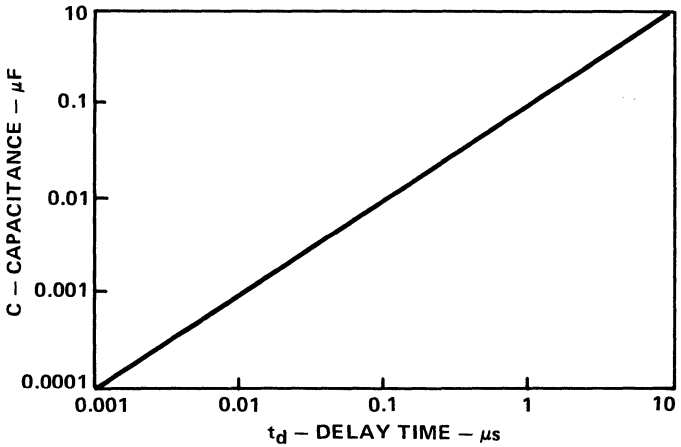


Figure 74. Capacitance vs Minimum Overvoltage Duration

Activation Indication Output

An additional output for use as an OV indicator is provided on the MC3423. This is an open-collector transistor which saturates when the OVP circuit is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V.

This output may also be used to clock an edge-triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This method of protection reduces or eliminates the heat-sinking requirements for the crowbar SCR.

Remote Activation Input

Another feature of the MC3423 is its remote activation input, pin 5, which has an internal pull-up current source. This input is CMOS/TTL compatible and, when held below 0.8 V, the MC3423 operates normally. However, if it is raised above 2 V, the OVP is activated regardless of whether an overvoltage condition is present. This feature may be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition.

TL77XXA Series
Supply Voltage Supervisors

TEXAS
INSTRUMENTS

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Introduction

The TL77XXA supply voltage supervisors are a series of monolithic integrated circuits that monitor the power supply status in digital and computer equipment and supply a reset signal when the supply voltage falls below the operational range. Each TL77XXA device performs all the functions required to monitor a voltage supply and generate complementary reset outputs whenever the voltage level being monitored falls below a defined operational range.

The reset outputs are maintained for a certain time delay after the supply voltage has returned to its nominal value. This allows the supply voltage to stabilize and prevents undefined operations. The amount of delay, t_d, is determined by an external timing capacitor C_T in accordance with the following formula:

$$t_d \approx 1.3 \times 10^4 \times C_T$$

where: t_d is in seconds
C_T is in farads

Theory of Operation

This section explains why a reset function is necessary in computer applications and how this function has been typically performed. It also explains why the TL77XXA supply voltage supervisors are a superior alternative to typical solutions, and provides a detailed description of TL77XXA performance.

Typical Reset Generators

A reset generator is required in most digital or computer applications where vital data is stored in volatile memory. Most digital or computer equipment uses discrete circuits that force the system into a defined state after power-on and when a supply voltage drop is detected.

Discrete Reset Generator 1

In a typical application (see Figure 1) for a digital or computer system, the reset input is connected to an RC (resistor-capacitor) reset network.

During power-up, the RC reset network maintains the reset signal until the charge on the capacitor reaches the threshold value. However, this network does not work well

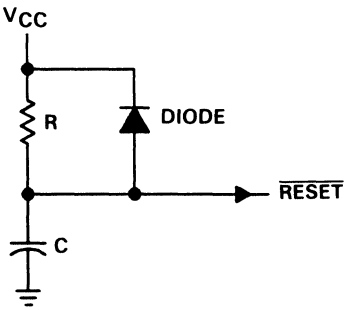

Figure 1. Discrete Reset Generator 1 in Typical System Application

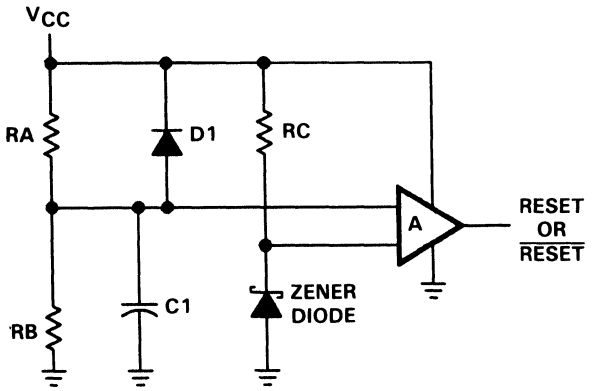

Figure 2. Discrete Reset Generator 2 in Typical System Application

during short voltage drops because the capacitor does not have enough time to discharge through the diode. This circuit is also characterized by a slow rise time and an uncertain reset time.

Discrete Reset Generator 2

Discrete reset generator 2 solves the problem of slow rise time (see Figure 2).

This circuit uses a zener diode to determine the threshold of the voltage being monitored, (V_{CC}). A reset signal is generated when V_{CC} drops to a level that causes the voltage at the junction of resistors RA and RB to fall below the zener diode breakdown voltage.

Either a high-active RESET or a low-active $\overline{\text{RESET}}$ output can be produced, depending on the connections to the inverting and noninverting inputs of the operational amplifier (op-amp).

For proper operation, V_{CC} for this circuit should never drop below the zener diode breakdown voltage or an undefined threshold point results.

Discrete Reset Generator 3

The circuit shown in Figure 3 provides a reset signal during power-up and detects short drops in the power supply.

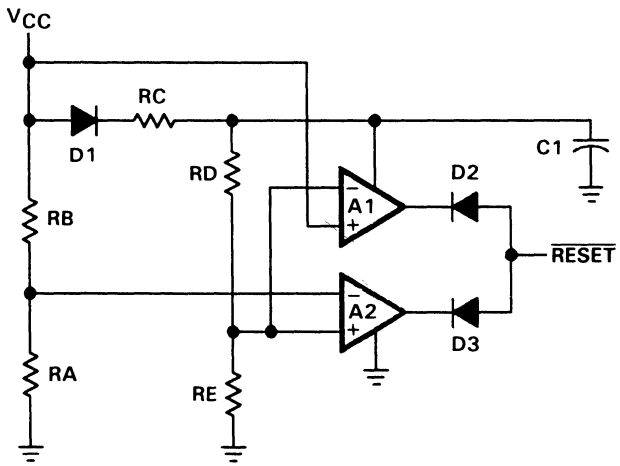

Figure 3. Discrete Reset Generator 3 in Typical System Application

This circuit generates a low-active pulse when one or both comparator outputs go low. This occurs when V_{CC} drops below the predefined threshold.

However, this circuit has two major disadvantages:

1. It does not generate accurate reset pulse durations.
2. It requires an excessive amount of components. The extra components add to the cost of the system and occupy more board space.

TL77XXA Performance

The TL77XXA series of supply voltage supervisors, with few external components, solves the problems associated with typical discrete reset generators. The TL77XXA supply voltage supervisors immediately detect low voltage conditions that

can cause a computer system to lose valuable data. Most discrete reset generators require a severe glitch before a fault is detected. However, the TL77XXA supervisors are sensitive to power drops of very small magnitude and duration.

In addition, fast rise and fall times are provided on the reset signal, which can be adjusted to ensure stable operating conditions.

To eliminate the need for an external inverter, two outputs, RESET and $\overline{\text{RESET}}$, are provided. These outputs remain active down to supply levels of 2 V during power-down, which would not be possible with an external inverter. Hysteresis is provided on the SENSE IN pin to improve the device performance by preventing oscillations around the threshold point.

Each TL77XXA circuit includes a very stable, temperature-compensated bandgap reference (see Figure 4), trimmed to 2.53 V (typically). In all but the TL7702A, a precision resistor-divider network (R1 and R2) reduces the voltage at SENSE IN for comparison with the internal reference voltage.

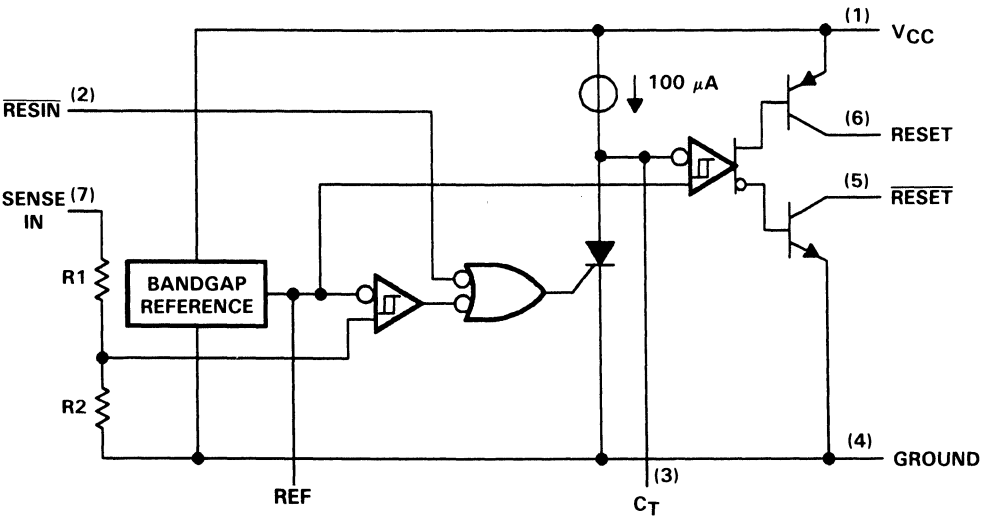

Figure 4. TL77XXA with Very Stable Temperature-Compensated Bandgap Reference

The typical resistance values of resistors R1 and R2 differ for the various supply voltage supervisors in the TL77XXA series. The nominal values of R1 and R2 for each are listed below.

	R1	R2
TL7702A	Short	Open
TL7705A	7.8 kΩ	10 kΩ
TL7709A	19.7 kΩ	10 kΩ
TL7712A	32.7 kΩ	10 kΩ
TL7715A	43.4 kΩ	10 kΩ

When the voltage being monitored at SENSE IN is within the operating range, SENSE IN voltage is greater than or equal to the threshold, the reset input ($\overline{\text{RESIN}}$) is high, the internal silicon-controlled rectifier (SCR) is off, and the external timing capacitor (CT) is charged to a value above the reference voltage. Both RESET and $\overline{\text{RESET}}$ outputs are inactive (low and high, respectively). Because both outputs are only active in one direction. RESET must be connected to a pull-down resistor and $\overline{\text{RESET}}$ to a pull-up resistor.

The TL77XXA outputs become active to generate a reset under various conditions.

When the SENSE IN voltage falls 10% below its operating value, the SCR is fired, the timing capacitor is discharged, and the outputs are forced into their active states.

With a low at the $\overline{\text{RESIN}}$ input, the SCR fires independently of the state of SENSE IN, so that an external system can generate a reset.

The SCR is turned off again after the voltages at SENSE IN and $\overline{\text{RESIN}}$ inputs increase above the respective thresholds.

In the TL7702A supply voltage supervisor, SENSE IN is tied directly to the input comparator, so that the threshold voltage can be programmed through an external voltage divider connected to SENSE IN.

For proper operation, the recommended voltage at SENSE IN should not exceed $V_{CC} - 1$ V. Voltage in excess of 6 V at this input will damage the internal circuit. With the exception of this feature, the performance of the TL7702A supply voltage supervisor is identical to that of the other circuits in the TL77XXA series.

During power-up, the outputs are undefined until the supply voltage (V_{CC}) to the TL77XXA reaches 3.6 V (see Figure 5). During power-down, with the voltage at SENSE IN below the threshold, the outputs remain active until the supply voltage to the TL77XXA falls below 2 V.

For proper operation in all TL77XXA applications, an external capacitor (0.1 μF minimum) must be connected from the REF pin to ground. The reference capacitor should be connected as close as possible to the TL77XXA. Using the reference output as a source for other circuits may result in erroneous operations.

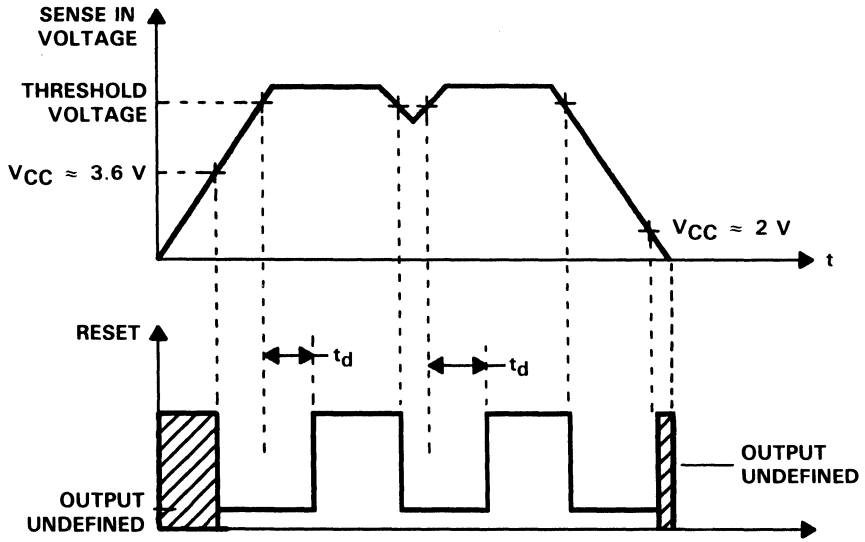

Figure 5. Circuit for Power-Up and Detection of Short Drops

TL77XXA Circuit Operation (see Figure 6)

Initialization

During power up, before the TL77XXA attains the minimum operating supply voltage value of 3.6 V, the bandgap reference circuit is inoperative, and both the RESET and $\overline{\text{RESET}}$ outputs are undefined. When V_{CC} exceeds 3.6 V, the reference circuit is ensured to be on by transistor Q32 and the 150-kΩ resistor, which form the start-up circuit. At this point, the reference voltage (pin 1) remains fixed at 2.53 V (typical) and is applied to the base of Q8, which is the inverting input of the comparator Q7-Q8. The noninverting input (the base of Q7) is the divided-down SENSE IN voltage from pin 7.

Low $\overline{\text{RESIN}}$

When $\overline{\text{RESIN}}$ (pin 2) is tied low, transistor Q19 is turned on and Q18 is turned off. With Q18 off, the base of Q17 is biased to the reference voltage, turning Q17 on. This activates the current mirror Q5-Q6, regardless of the state of Q8. Also with Q17 on, Q16 turns on causing Q12 to be shunted. This causes current mirror Q11-Q12 to be

inactive. Even though Q5 is on, there is no collector current flowing into Q11. Therefore, all the collector current of Q5 flows into the base of Q10 (SCR gate). This current flow allows both Q10 and Q9 to turn on and remain on even if the gate drive is removed.

With Q10-Q9 on, the timing capacitor CT (pin 3) and the base of Q21 (inverting input of comparator Q21-Q22) are shorted to ground. This turns on transistor Q22, which activates current mirror Q23, Q24, Q25, Q26, and Q27. With collector current flowing from Q26 and Q27,transistors Q28 and Q turn on, which causes the outputs (RESET and $\overline{\text{RESET}}$, respectively) to become active.

High $\overline{\text{RESIN}}$

When $\overline{\text{RESIN}}$ (pin 2) is tied high, transistor Q17 draws very little current, and Q16 is off. The state of the SCR (Q10-Q9) now depends only on the output of comparator Q7-Q8, which is determined by the SENSE IN voltage.

If the SENSE IN voltage is lower than the threshold, Q7 is off, disabling current mirror Q1, Q2, Q3, and Q4. In addition, Q8 is on, causing current mirror Q5-Q6 to be active. With Q4 off, no current flows into Q12 and mirror Q11-Q12 is disabled. Collector current from Q5 again flows into the SCR gate (Q10 base) to turn it on. CT discharges. This turns on Q22 allowing base current to flow into Q28 and Q29 and turning the outputs on (active).

Outputs Inactive

If the voltage at SENSE IN is greater than the threshold (with $\overline{\text{RESIN}}$ still tied high), Q7 turns on and Q8 is shut off. This activates mirror Q1, Q2, Q3, and Q4 and disables mirror Q5-Q6. With collector current flowing from Q4 into Q12, current mirror Q11-Q12 is on. Since Q5 is off, Q11 pulls current from the gate of the SCR and forces the SCR to turn off (gate turn off).

With Q9 off, collector current from Q3 charges CT to a value above the base voltage of Q22, after the time delay t_d. At this point, Q22 turns off, disabling mirror Q23, Q24, Q25, Q26, and Q27. This removes the base drive from Q28 and Q29 and places the outputs at their inactive (off) state.

Figure 6. (a)
TL77XXA Schematic Diagram

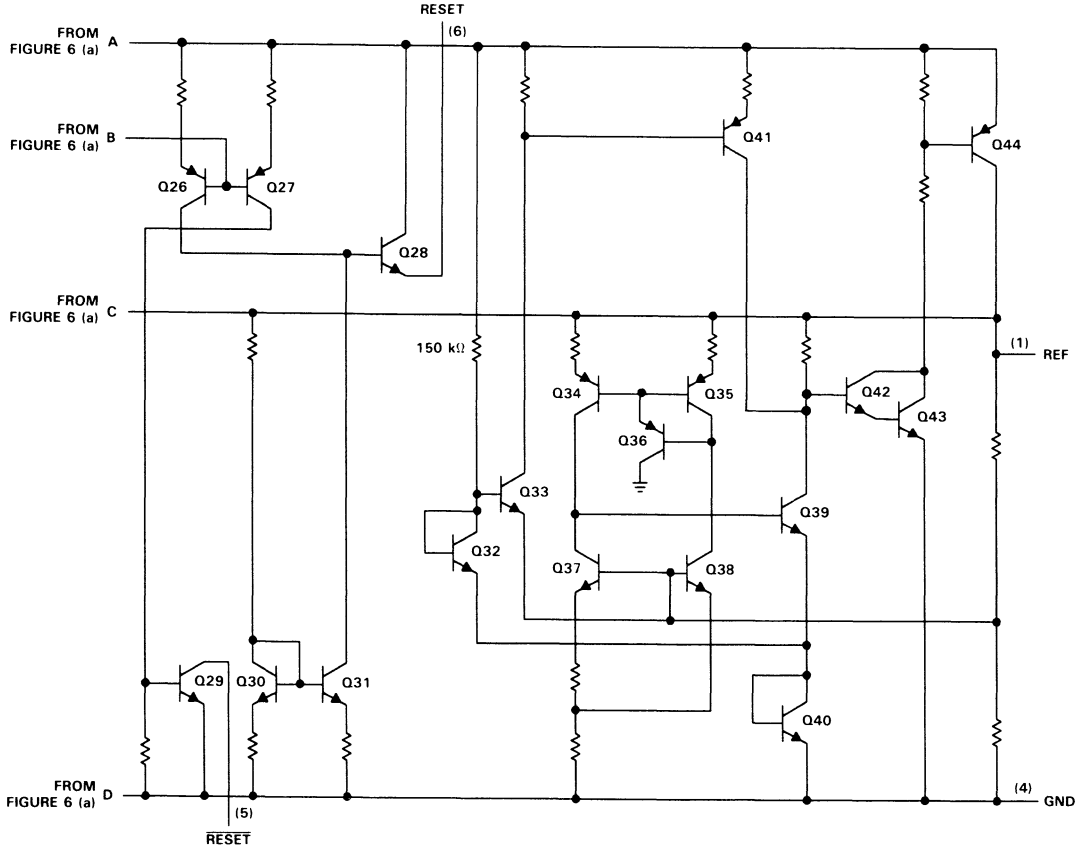

Figure 6. (b)
TL77XXA Schematic Diagram

TL77XXA ELECTRICAL SPECIFICATIONS

The TL77XXA supply voltage supervisors offer accurate, reliable performance over a wide range of operating conditions. The TL77XXA maximum allowable ratings, recommended operating conditions, and electrical characteristics are presented in the following tables.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range at $\overline{RESIN}$ . . . . . −0.3 V to 20 V
Input voltage at SENSE: TL7702A (see Note 2) . . . . . −0.6 V to 6 V
TL7705A . . . . . −0.3 V to 10 V
TL7709A . . . . . −0.3 V to 15 V
TL7712A . . . . . −0.3 V to 20 V
TL7715A . . . . . −0.3 V to 20 V
High-level output current at $\overline{RESET}$ . . . . . −30 mA
Low-level output current at $\overline{RESET}$ . . . . . 30 mA
Operating free-air temperature range: TL77XXAI . . . . . −25°C to 85°C
TL77XXAC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For the TL7702A, the voltage applied to the SENSE terminal must never exceed V_{CC}.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}			0.8	V
Input voltage at SENSE, V_I	TL7702A	0	†	V
	TL7705A	0	10	
	TL7709A	0	15	
	TL7712A	0	20	
	TL7715A	0	20	
High-level output current at $\overline{RESET}$, I_{OH}			−16	mA
Low-level output current at $\overline{RESET}$, I_{OL}			16	mA
Operating free-air temperature range, T_A	TL77XXAI	−25	85	°C
	TL77XXAC	0	70	

† For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} − 1 V or 6 V, whichever is less.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	RESET		I_{OH} = −16 mA	V_{CC}−1.5			V
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage			T_A = 25°C	2.48	2.53	2.58	V
V_T	Threshold voltage	SENSE	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C	2.48	2.53	2.58	V
			TL7705A		4.5	4.55	4.6	
			TL7709A		7.5	7.6	7.7	
			TL7712A		10.6	10.8	11	
			TL7715A		13.2	13.5	13.8	
$V_{T+}-V_{T-}$	Hysteresis‡	SENSE	TL7702A	V_{CC} = 3.6 V to 18 V, T_A = 25°C		10		mV
			TL7705A			15		
			TL7709A			20		
			TL7712A			35		
			TL7715A			45		
I_I	Input current	RESIN		V_I = 2.4 V to V_{CC}			20	µA
				V_I = 0.4 V			−100	
		SENSE	TL7702A	V_I = V_{ref} to V_{CC} − 1.5 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$		V_O = 18 V			50	µA
I_{OL}	Low-level output current	RESET		V_O = 0			−50	µA
I_{CC}	Supply current			All inputs and outputs open		1.8	3	mA

† All typical values are at T_A = 25°C.

‡ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{w1} Pulse duration, SENSE	V_{IH}‡ = V_{Tmax} + 300 mV, V_{IL}‡ = V_{Tmin} − 300 mV		0.5		µs
t_{w2} Pulse duration at RESET and $\overline{\text{RESET}}$	C_T = 0.1 µF		1.3		ms
t_{pd} Propagation delay from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	V_I‡ = 5 V, C1 = 100 pF		5		µs
t_r Rise time, RESET and $\overline{\text{RESET}}$	V_I‡ = 5 V, C1 = 100 pF, R1 = 4.7 kΩ		1		µs
t_f Fall time, RESET and $\overline{\text{RESET}}$	V_I‡ = 5 V, C1 = 100 pF, R1 = 4.7 kΩ		1		µs

† All typical values are at T_A = 25°C.
‡ Voltages listed are at the SENSE input.

Application Examples

This section describes several sample applications for the TL77XXA series of supply voltage supervisors. The sample applications are as follows:

1. Generating a Reset
2. Generating Dual Reset Signals
3. TL77XXA Supply Voltage Supervisors in Multiple Supplies
4. Speeding Up TL77XXA Output
5. Slowing the SENSE IN Glitch Response
6. Connecting a TL77XXA as an Oscillator
7. Building a Watchdog Circuit
8. The TL77XXA as a Retriggerable One-Shot Circuit
9. Connecting V_{CC} of the TL77XXA to a High Voltage Line
10. Monitoring AC and Unregulated DC Voltages
11. TL7705A in a Battery-Buffered Memory System
12. Eliminating Undefined States of TL77XXA Outputs
13. Sensing Different Voltage Thresholds
14. Preventing Voltage Above V_{CC} −1 at SENSE IN of the TL77XXA

Generating a Reset

The simplest application of a TL77XXA supply voltage supervisor is its use as a reset generator. A reset signal must be generated in microcomputer or microprocessor systems to properly initialize the system to a known state during power-on and protect the system memory when the system power supply is below the operational range.

The TL77XXA supply voltage supervisor can be used in microcomputer or microprocessor equipment to generate a reset. By connecting the RESET output of the TL77XXA to the RESET input of the microcomputer or microprocessor system, an accurate reset pulse is generated when fault conditions occur in the power supply being monitored.

Microprocessor Applications

The microprocessors with which the TL77XXA can interface fall into two categories according to whether they interface directly or indirectly with the TL77XXA. The following table lists examples of microprocessors in each category.

Direct Interfacing	Indirect Interfacing
MC6800	MC68000
R6502	Intel 8088
TMS7040	Intel 80286
Intel 8085	TMS320
Intel 80188	
Z-80	

Interfacing the TL77XXA supply voltage supervisor directly with a microprocessor is a relatively straightforward process. Interfacing it indirectly with a microprocessor is similar, but requires an additional consideration.

Direct Interfacing

Microprocessors in the first category, such as the MC6800, can be directly interfaced with the TL77XXA supply voltage supervisors as shown in Figure 7. Both the V_{CC} and SENSE IN inputs are tied to the microprocessor system supply line, so that the voltage being monitored at SENSE IN is the system supply voltage. The $\overline{\text{RESIN}}$ input is also tied to the supply line.

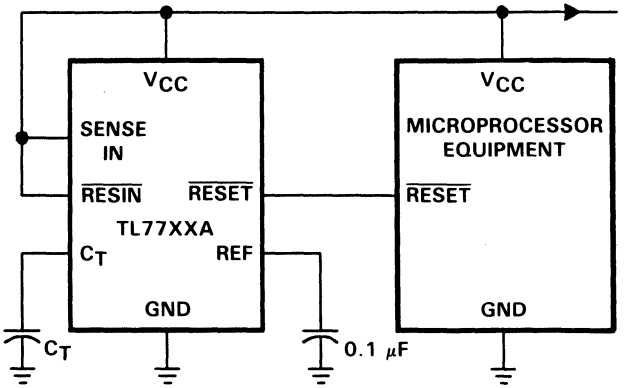

Figure 7. Microprocessor to TL77XXA Direct Interface

A small capacitor connected from the REF output to ground is required to minimize the effects of system noise, and provide a stable reference. Another capacitor C_T determines the delay between the end of the fault condition and the return of the $\overline{\text{RESET}}$ output to its inactive state.

The system is forced into a defined state when a high-to-low transition is detected on the $\overline{\text{RESET}}$ input of the microprocessor.

Indirect Interfacing

The microprocessors in the second category, such as the 68000, the 8088, etc., cannot be interfaced directly with the TL77XXA supply voltage supervisor because a clock generator precedes the microprocessor as shown in Figure 8.

The clock generator must generate the proper logic-reset signal (with a low external pulse) during power-fault conditions. The high-to-low transition of the clock

generator RESET output must be synchronized to the system clock. When the clock generator $\overline{\text{RESET}}$ input is low, the RESET output goes high after a one to two clock cycle delay, due to the synchronization of RESET to the system clock.

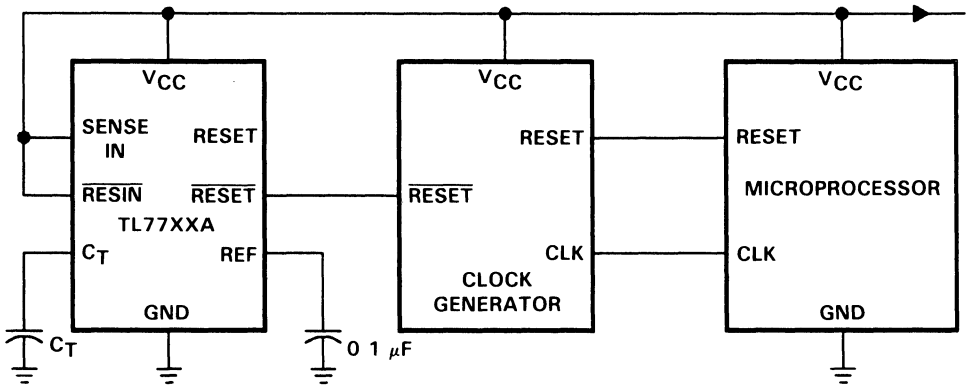

Figure 8. Indirect Interfacing

Generating Dual Reset Signals

A TL77XXA supply voltage supervisor can be used in a system that requires both low-active and high-active reset signals. Figure 9 shows a circuit that uses a TL7705A to send interrupt signals to a microcomputer and to read-only-memory (ROM). When a

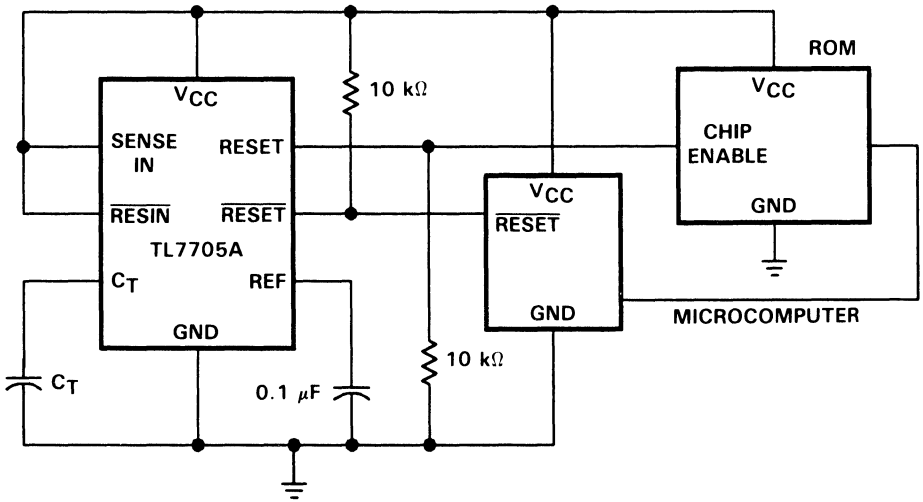

Figure 9. TL7705A Interrupt to Microprocessor and ROM

power failure occurs, RESET goes high and $\overline{\text{RESET}}$ goes low. $\overline{\text{RESET}}$ resets the microcomputer; RESET sets the ROM to a standby mode. The microcomputer output is also used to generate a signal during a reset. This signal is sent to the ROM.

TL77XXA Supply Voltage Supervisors in Multiple Supplies

Several TL77XXA supply voltage supervisors can be used in systems that have various supplies and that require monitoring of the supplies for proper operation. Figure 10 shows a circuit that uses two TL7712A supply voltage supervisors and one TL7705A to monitor 12 V, −12 V, and 5 V supplies.

The $\overline{\text{RESET}}$ outputs of both TL7712A supervisors are sent to the $\overline{\text{RESIN}}$ input of the TL7705A, which is high during normal operation. SENSE IN of the TL7705A is tied to the 5-V line. The $\overline{\text{RESET}}$ output of the TL7705A serves as the system interrupt signal. When one of the three supervisors detects a fault, an interrupt signal is generated.

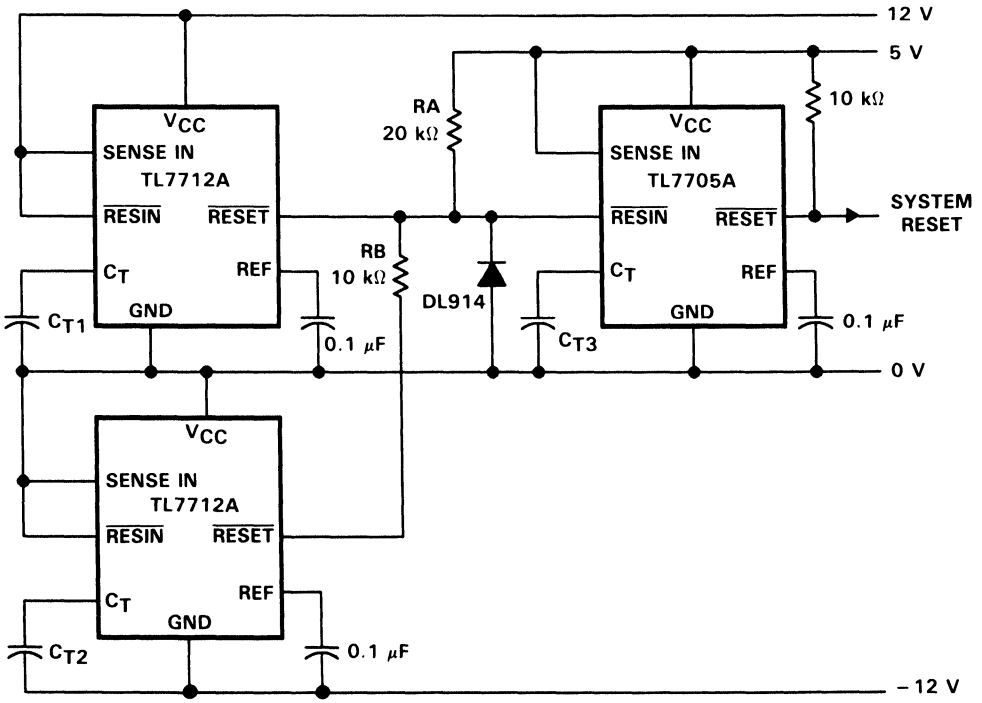

Figure 10. TL7705A Supply Voltage Monitor Circuit

Speeding Up the TL77XXA Output

The rise and fall time of the TL77XXA output can be shortened with only a minor modification to the circuit.

The circuit shown in Figure 11 can be used in applications where the normal $\overline{\text{RESET}}$ output pulse transition time is too slow. Connecting a transistor-inverter circuit to the RESET output provides a $\overline{\text{RESET}}$ at its collector. This circuit results in a faster response because the saturation region of Q1 is avoided by clamping its base-collector junction. Under normal operating voltage levels RESET is inactive, Q1 is ensured to be off by RB, and $\overline{\text{RESET}}$ is high. When a voltage drop occurs at SENSE IN, RESET goes high. This turns on Q1 which pulls $\overline{\text{RESET}}$ low.

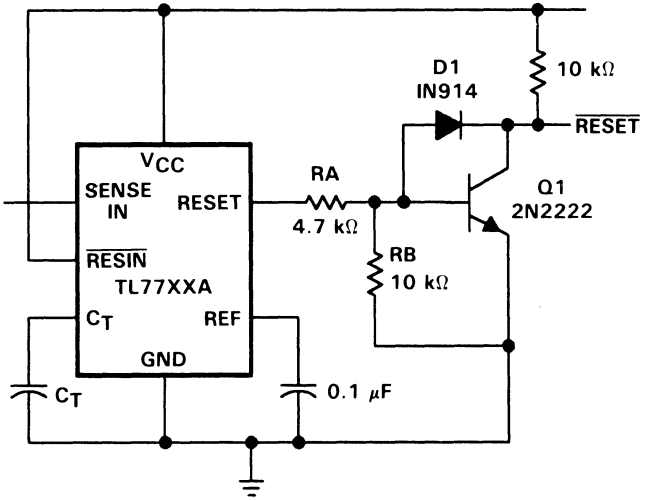

Figure 11. Circuit Modification to Shorten Transition Times

Slowing the SENSE IN Glitch Response

An RC reset network can be connected to the TL77XXA supply voltage supervisor to slow the supervisor response to voltage drops. The TL77XXA supply voltage supervisors are designed to detect voltage drops of less than 1 μs in duration. The circuit shown in Figure 12 can be used in applications where this fast response is not desired, such as very noisy environments.

With an external RC reset network connected to the SENSE IN pin, the device normal response is delayed by an amount t_A, such that

$$t_A = C_A \times RA$$

where: t_A is in seconds
C_A is in farads
RA is in ohms

The value of RA should be small (less than 22 Ω) so that RA will not affect the SENSE IN threshold voltage.

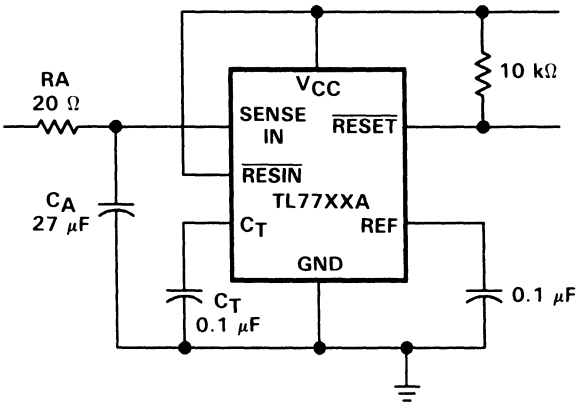

Figure 12. Circuit to Slow SENSE IN Glitch Response

Connecting a TL77XXA as an Oscillator

The TL77XXA can be connected so that it will perform as an oscillator. Figure 13 shows a TL77XXA performing an oscillator function. When power is turned on, both outputs are active ($\overline{\text{RESET}}$ low, RESET high) and capacitor C is charging. When the voltage on C reaches the SENSE IN threshold, RESET and $\overline{\text{RESET}}$ change states. At this time, the capacitor begins to discharge until SENSE IN voltage falls below the threshold and the outputs become active again. The cycle is then repeated.

A sawtooth waveform is generated at the junction of RA and RB. Because the SENSE IN voltage crosses the threshold regularly, RESET alternates between high and low. In this configuration, $\overline{\text{RESET}}$ provides a square wave suitable for main clock output. The duty cycle of the square wave depends upon the time that the sawtooth wave is above and below the threshold.

The rise and fall time of the sawtooth output, as well as its general shape, is determined by the values of capacitor C, the two resistors RA and RB, and the timing capacitor C_T.

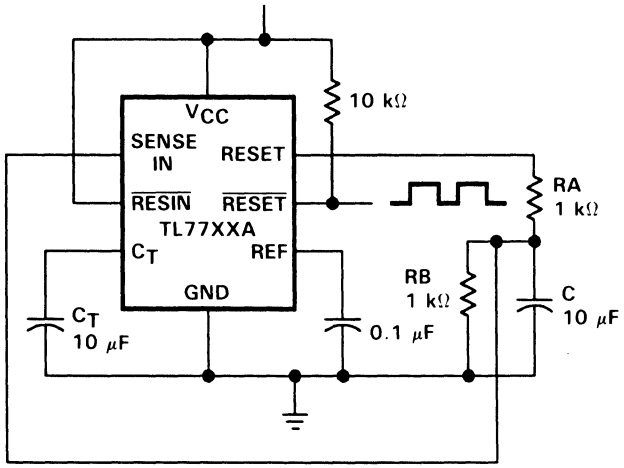

Figure 13. TL77XXA Oscillator Circuit

Building a Watchdog Circuit

A TL7702A and a TL7705A can be used in building a watchdog circuit that monitors incoming pulses and generates a reset whenever an input pulse is absent. Figure 14 shows a TL7702A and a TL7705A in a watchdog circuit. If the microcomputer is operating, the watchdog input is continuously strobed by input pulses that, through C1 and D1, charge C2. To allow C2 to receive an equal charge from each input pulse, C1 is discharged through RA between pulses.

In the absence of input pulses, C2 discharges through RB; when this occurs, the voltage at the TL7702A SENSE IN drops below its threshold and a reset signal is generated. This reset signal causes $\overline{\text{RESIN}}$ of the TL7705A to go low, in turn causing its $\overline{\text{RESET}}$ to go low, which provides a reset signal to the microprocessor or computer.

When the supply voltage (V_{CC}) drops below its operational range, the TL7705A also generates a $\overline{\text{RESET}}$ to the microcomputer.

When the string of input pulses is resumed, C2 again charges to a value above the TL7702A threshold and $\overline{\text{RESET}}$ of the TL7705A becomes inactive.

Diode D2 is connected from the TL7702A RESET output to SENSE IN to allow C2 to be charged during power-up. For proper operation, the value for C_{T1} must be less than that of C_{T2}.

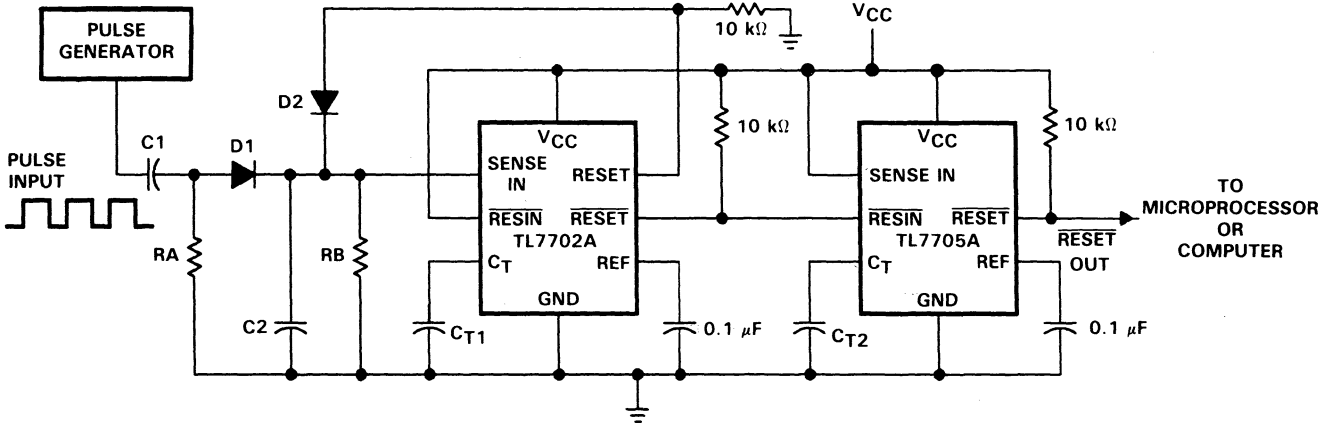

Figure 14. TL7705A Watchdog Circuit

The TL77XXA as a Retriggerable One-Shot Circuit

Figure 15 shows the TL77XXA used as a retriggerable one-shot circuit. In this application, complementary active outputs (from RESET and $\overline{\text{RESET}}$) are obtained every time the $\overline{\text{RESIN}}$ input is triggered, the trigger pulse duration plus t_d equals the one shot pulse duration, and SENSE IN is tied to V_{CC}.

The outputs become active when $\overline{\text{RESIN}}$ passes from a high to a low state. Outputs remain active if the input has a period less than the delay time, t_d.

In this configuration, the $\overline{\text{RESIN}}$ input can be used as a panic button to provide an interrupt signal regardless of system condition.

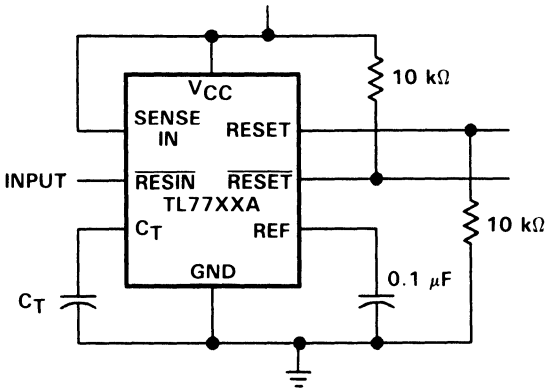

Figure 15. TL77XXA Retriggerable One-Shot Circuit

Connecting V_{CC} of the TL77XXA to a High-Voltage Line

The TL77XXA supply voltage supervisors can be used to monitor the output of a regulator and to generate a reset even if the sensed voltage line drops to zero. Figure 16 shows such a circuit.

The V_{CC} input is fed from the input side of the regulator so that it is not affected by failures in the regulator. Because the regulator input voltage cannot be 35 V, a TL431 programmable reference is used to drop the voltage to a level that is compatible with the TL77XXA. Therefore, the $\overline{\text{RESET}}$ output remains active with 0 V at SENSE IN, provided that there is enough voltage at the regulator input.

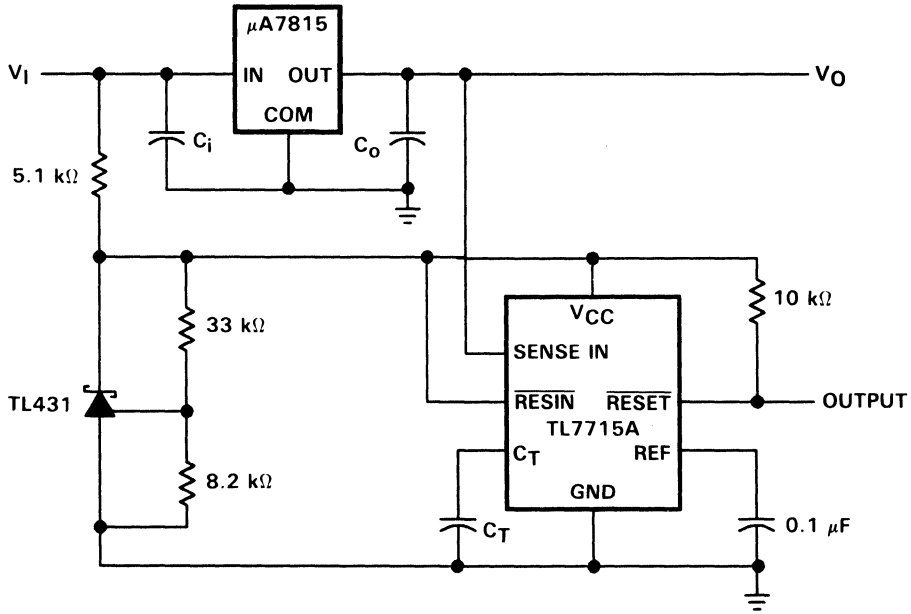

Figure 16. V_{CC} of the TL7715A Connected to a High-Voltage Line

Monitoring AC and Unregulated DC Voltages

The TL77XXA can be used in a voltage regulator system to monitor either the ac input line to the power supply or the unregulated dc input. To avoid undefined operations, the point monitored must be one at which a power loss can be detected as quickly as possible.

When a TL77XXA supply voltage supervisor is used to supervise a voltage regulator system, the regulator output should not be used as a sensing point. The preferred points in a regulator system, because they respond more quickly to a system power loss, are the ac input line to the power supply and the unregulated dc input to the regulator.

When the ac voltage is being monitored, the output of the input transformer can be monitored by a TL7702A, see Figure 17. Resistors RA and RB are selected for the desired trip point above the regulator required minimum input voltage. Diode D1 acts as a half-wave rectifier. Capacitor C1 filters this half-wave signal so that a reset does not occur at every half cycle. Capacitor C1 also introduces a delay between the ac power loss and the reset signal.

When a drop in the ac line voltage is detected, the dc value of the rectified signal drops. The values of RA and RB should be such that any change greater than the maximum allowable drop will be detected.

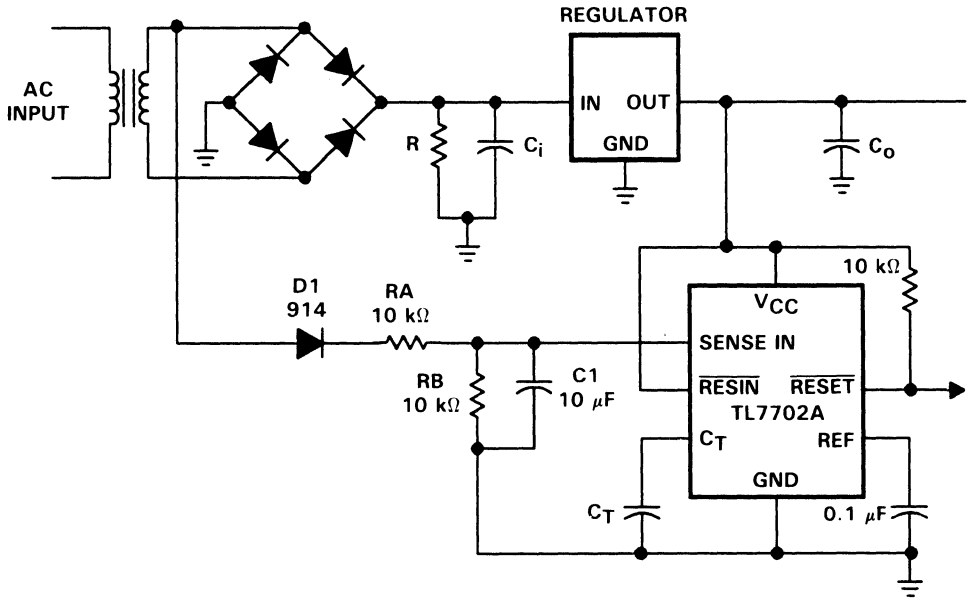

Figure 17. TL7702A Circuit for Monitoring Input-Transformer Output

Figure 18 shows a TL7702A used to monitor the unregulated dc voltage. The regulator remains within its specified output voltage rating as long as the input voltage remains within its minimum and maximum limits. During a power drop, the regulator input starts to drop before the output experiences any voltage change.

When the input voltage begins to drop, the ripple voltage also starts to drop. Resistors RA and RB should be selected so that the threshold of the TL7702A SENSE IN voltage is below the ripple voltage at the desired detection level (which should be above the regulator minimum input voltage). The TL7702A therefore warns of a power failure at the regulator input before the regulator output is significantly affected.

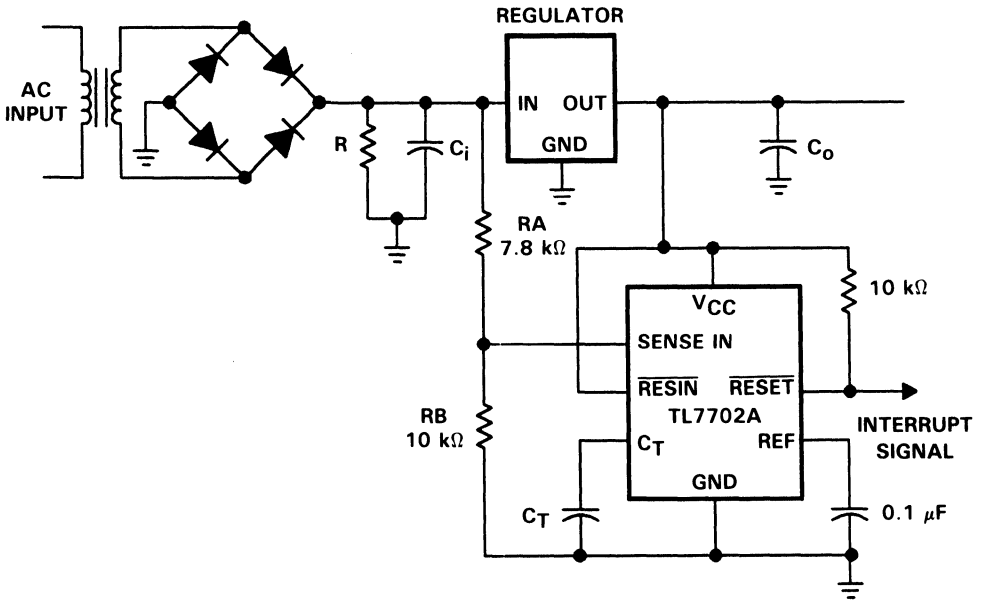

Figure 18. TL7702A Circuit for Monitoring Unregulated DC Voltage

The TL7705A in a Battery-Buffered Memory System

The TL7705A can be used in a circuit that protects the memory contents of a microprocessor against spikes on the "write" line after failure of the line voltage. Figure 19 shows the TL7705A in a battery-buffered memory system. A switch consisting of transistor Q1 and diode D1 is inserted on the memory chip select line. If SYSTEM RESET (tied to $\overline{\text{RESIN}}$) is high, the $\overline{\text{RESET}}$ output of the TL7705A is high, which turns on transistor Q1.

When a power failure occurs, SYSTEM RESET goes low (triggering the TL7705A) and $\overline{\text{RESET}}$ goes low (turning off Q1 and reverse-biasing diode D1). Therefore, the chip select input of the memory (CS) is isolated from the chip-select line.

Eliminating Undefined States of TL77XXA Outputs

An external circuit can be connected to the TL77XXA supply voltage supervisor in applications where the state of the TL77XXA outputs is to remain defined down to the point at which V_{CC} is 0 V. Figure 20 shows an external circuit that, when connected to the TL77XXA, eliminates undefined states of the TL77XXA outputs during power-up and power-down.

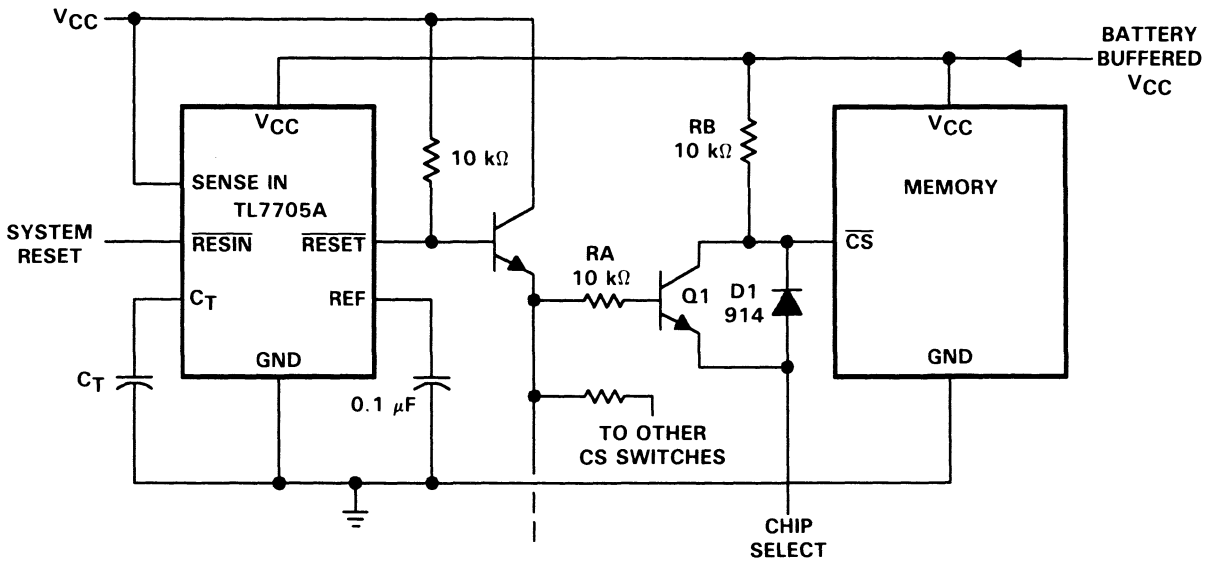

Figure 19. TL7705A in a Battery-Buffered Memory System

The RESET output is used to switch transistor Q1 on or off. Switching Q1 on causes the collector (the $\overline{RES}$ output) to go high. Switching Q1 off causes the collector to go low. When V_{CC} is above minimum operational value, RESET is at a low voltage. This condition turns on Q1 and causes $\overline{RES}$ to go high. As V_{CC} drops, the RESET output keeps Q1 turned off. This causes the $\overline{RES}$ output to remain active down to the point at which V_{CC} is 0 V.

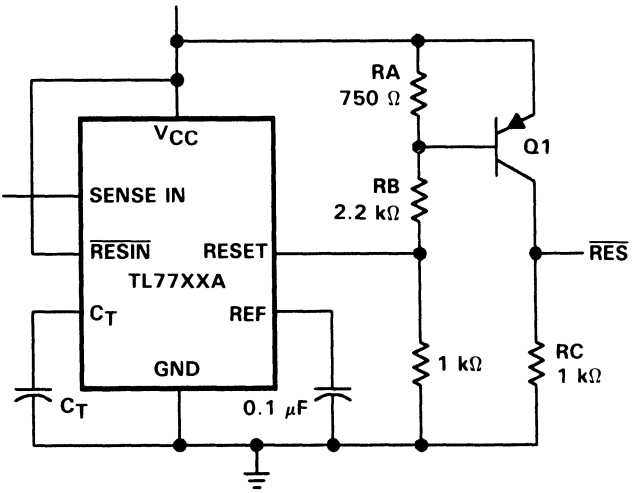

Figure 20. Elimination of Undefined States

Figure 21 shows a circuit application that eliminates the undefined state of the TL77XXA outputs by using a p-channel depletion JFET.

To ensure that the transistor is switched off when the supply voltage reaches a nominal value, the gate must be more positive than the source. The circuit in Figure 21 provides the advantage of less power dissipation than the circuit in Figure 20.

Sensing Different Voltage Thresholds

The TL77XXA supply voltage supervisors are capable of detecting voltage drops of 10%. The TL7702A can be used in a modified circuit to detect even smaller voltage drops.

The threshold voltage at SENSE IN of the TL77XXA is designed to detect a voltage drop of approximately 10% below the rated voltage. The TL7705A, for example, is for use in 5 V systems and the threshold voltage at its SENSE IN is typically 4.55 V. The TL7709A, the TL7712A, and the TL7715A have typical threshold voltages at SENSE IN of 7.6 V, 10.8 V, and 13.5 V, respectively.

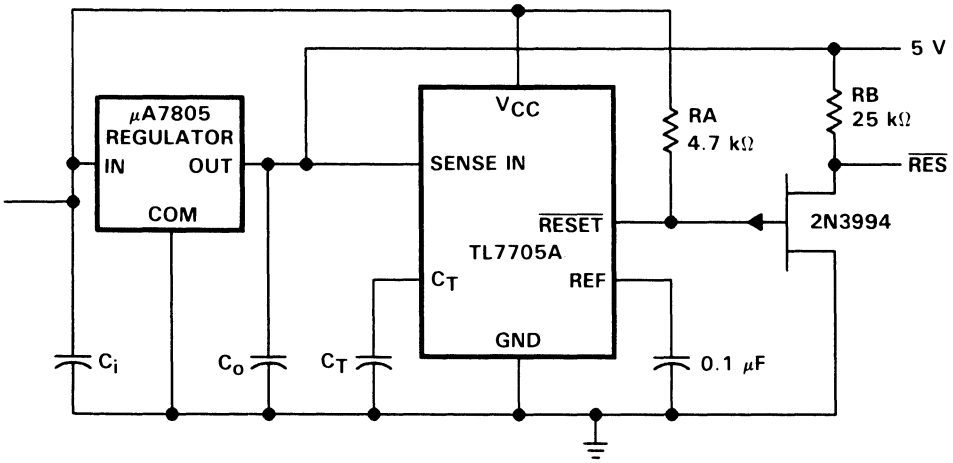

Figure 21. Elimination of Undefined State Using P-Channel Depletion JFET

In applications where a 10% drop in voltage is harmful and therefore a drop of 5% must be detected, the programmable TL7702A with a precision voltage divider at SENSE IN can be used as shown in Figure 22. To calculate the exact threshold voltage for the TL7702A, the following equation is used:

$$V_S = \frac{R1 + R2}{R2} (V_{T-})$$

where:

$V_T = 2.53$ V

For a 5-V system with a −5% detection level: $V_S = 4.75$ V, $V_T = 2.53$ V and R2 is selected as 10 kΩ. R1, therefore, is 8.775 kΩ.

Preventing Voltage Above V_{CC} − 1 at SENSE IN of the TL7702A

The TL7702 must be used in a circuit that ensures that the voltage at SENSE IN never exceeds the recommended voltage. Figure 23 shows a circuit that clamps the voltage at SENSE IN to a value below V_{CC}.

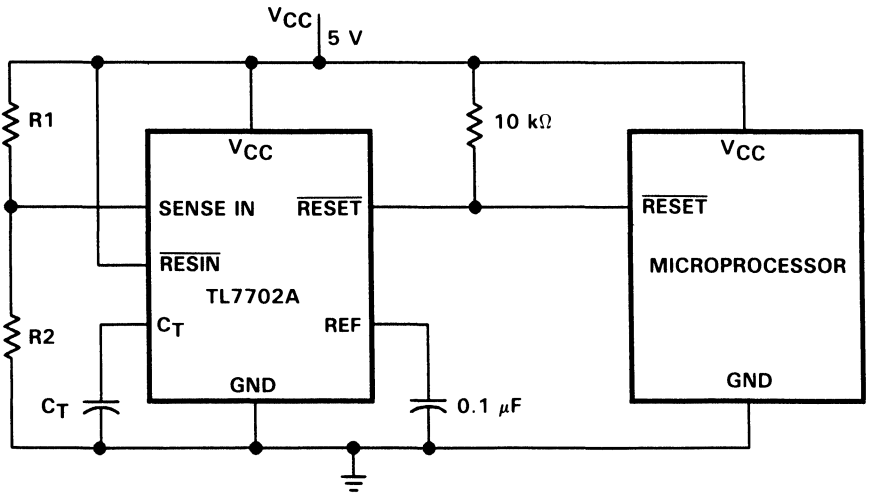

Figure 22. TL7702A 5% Detection Circuit

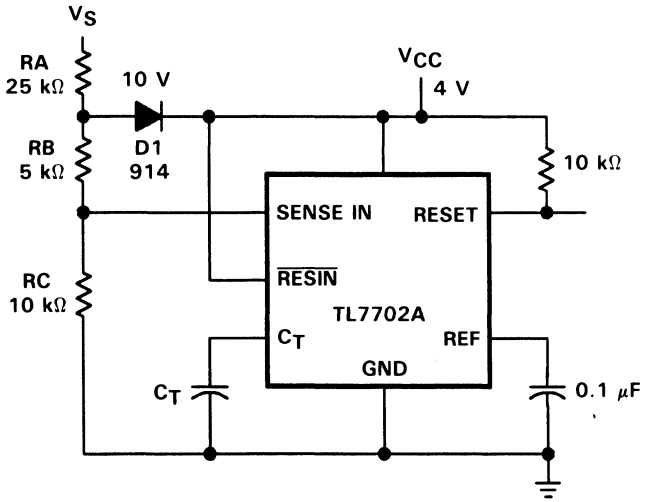

Figure 23. Clamp Circuit for TL7702A SENSE IN

To select the resistor values, a minimum V_{CC} (V_{CCmin}) and a maximum SENSE IN voltage (V_{Tmax}) must be selected. Resistors RB and RC are chosen such that:

$$V_{Tmax} = \frac{RC}{RB + RC} V_{CCmin} + V_{diode}$$

With this accomplished, the value for RA is calculated for the desired trip point (V_S) such that:

$$V_{Tnom} = \frac{RC}{RA + RB + RC} (V_S)$$

where:

$V_{Tnom} = 2.53$ V

500-W, 80-A, Off-the-Line, Half-Bridge Converter, Switching Power Supply

TEXAS INSTRUMENTS

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Introduction

The power supply was designed and built for the purposes of demonstrating and evaluating switching power supply components under operating conditions. The primary consideration of the mechanical design was to facilitate instrumentation, not particularly to achieve a compact modular design.

The half-bridge circuit configuration was selected because it is one of the more common types of converter circuits in use today. The half-bridge power converter is very popular because of its many advantages which include: (1) voltage stress on the power switches is no greater than the rectified power mains voltage; (2) power transformer dc core flux can be eliminated by the use of a capacitor in series with the primary of the power transformer; (3) reverse energy created by the transformer leakage inductance can be commutated back to the dc bus and therefore need not be absorbed by the power switches; and (4) a simple power transformer primary is required.

Although the half-power bridge converter is very popular, it does require additional consideration for the base drive of the power switches. These considerations include switching speed and isolation requirements. This work details the construction of such a base driver section that very successfully interfaces between a TL494 control circuit and the bases of the TIPL755 power inverter transistors.

The discussion will begin with a power supply specification and then proceed with the detailed design considerations.

The selection of the operating frequency is a compromise between physical size of the magnetics and filters and loss of efficiency due to increased switching losses. The frequency of this design was set at 20 kHz.

Power Supply Definitions

Specifications

Regulated Output Power:

1) +5 volts ± 0.5% at 80 A
2) +10 volts ±2% at 2.5 A
3) +26 volts ±2% at 2 A.

Ripple: Shall be ≤125 mV peak-to-peak on all outputs

Input Power: 120 V or 240 V, 1ϕ, 60 Hz

Efficiency: 65% minimum at full load

Protection Circuits:

1) All regulated outputs shall be current limited.
2) The 5 V/80 A output shall have overvoltage protection.

Input Voltage Range:

	120-V ac Input	240-V ac Input
Minimum	96	192
Nominal	120	240
Maximum	132	264

Holdup Time, t_h: 10 ms (time outputs remain in regulation following loss of input power)

Block Diagram

A block diagram of the half-bridge converter switching power supply is shown as Figure 1.

Half-Bridge Converter Description

The idealized waveforms of Figure 2 define the voltage and current characteristics of the Power Converter Section.

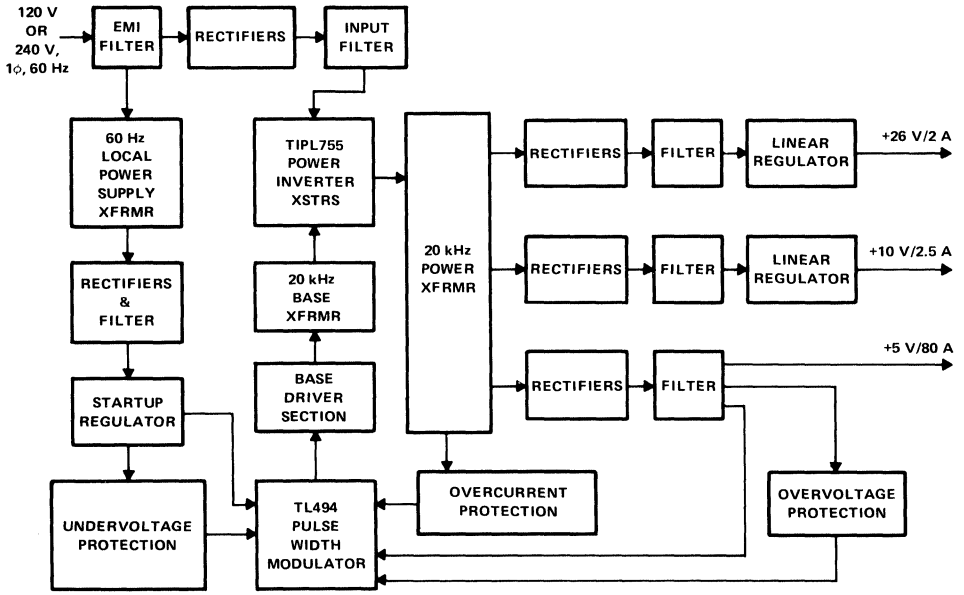
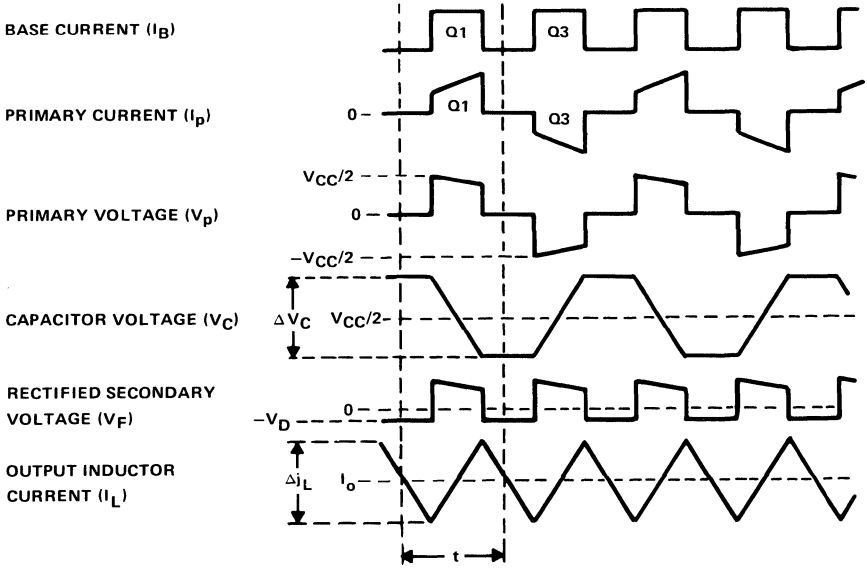
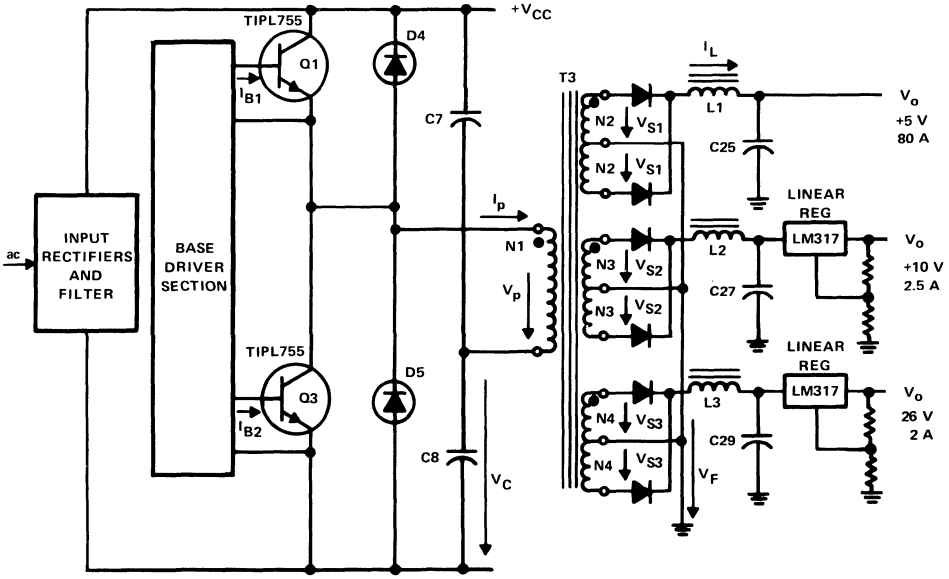


Figure 1. 500-W, 80-A Half-Bridge Converter Switching Power Supply



HALF-BRIDGE INVERTER IDEALIZED WAVEFORMS



HALF-BRIDGE POWER CONVERTER SECTION

Figure 2. Half-Bridge Inverter Waveforms and Power Converter Section

Preliminary Calculations

Input Voltage Range

The input rectifiers and filter capacitors are designed to operate as a standard full-wave rectifier with 240-V ac input and as a doubler with 120-V ac input (Figure 3). Switch S2A is closed for the 120-V ac operation.

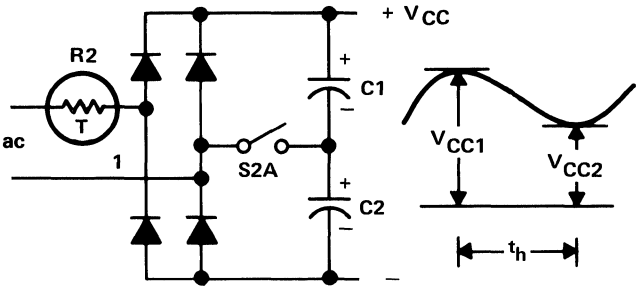


Figure 3. Input Filter Circuit

Based on the specification, the theoretical minimum converter voltage, V_{CC}, with 120-V ac input and switch S2A closed is:

$$V_{CC} = \sqrt{2} \times 96\ V_{rms} \times 2 = 271\ V \qquad \text{(Eq.1)}$$

By allowing 10 V for EMI filter, surge limiting, thermistor, rectifier, and wiring losses, the value of V_{CC} is reduced to 261 V. This value represents V_{CC1} in Figure 3 and Equation 2. From the specification, the holdup time, t_h, is 10 ms. The value of minimum filter capacitance is calculated by allowing V_{CC2} to be 220 V.

$$C = \frac{2\ P_{IN}\ t_h}{\left[(V_{CC1})^2 - (V_{CC2})^2\right]} \qquad \text{(Eq.2)}$$

The term P_{IN} is the input power supplied to the converter and based on a 65% efficiency, it is estimated to be:

$$P_{IN} = \frac{5\ V \times 80\ A + 10\ V \times 2.5\ A + 26\ V \times 2\ A}{0.65}$$

$$P_{IN} = 734\ W$$

Therefore:

$$C = \frac{2 \times 734\ W \times 10 \times 10^{-3} s}{\left[(261\ V)^2 - (220\ V)^2\right]} = 744\ \mu F \qquad \text{(Eq.3)}$$

The capacitors C1 and C2 are connected in series for 240 V_{rms} operation, so the minimum value required of each is $2 \times C$ or $\approx$ 1488 μF.

Power Transformer Turns Ratio Estimate

Equation (4) is used to estimate the transformer turns ratio.

$$N = \frac{N_P}{N_S} = \frac{V_P}{V_S} = \frac{\delta\left[\frac{V_{CC}}{2}\right]}{V_O + V_D + V_W + V_{REG}} \qquad \text{(Eq.4)}$$

where

N_P = number of turns on primary
N_S = number of turns on secondary
V_P = transformer primary voltage [or $(V_{CC})/(2)$]
δ = duty cycle (80% assumed)
V_O = regulated output voltage
V_S = transformer secondary voltage
V_D = rectifier conduction voltage
V_W = power supply wiring voltage
V_{REG} = linear regulator voltage

Turns Ratio Calculation for +5 V Output

Assume:
V_O = 5 V
V_D = 0.6 V
V_W = 0.1 V
V_{CC} = 220 V
δ = 0.8

$$N = \frac{N1}{N2} = \frac{0.8\left[\frac{220\ V}{2}\right]}{5\ V + 0.6 + 0.1\ V} = 15.43 \text{ max}$$

Turns Ratio Calculation for +10 V Output

Assume:
V_O = 10 V
V_D = 0.7 V
V_W = 0.1 V
V_{REG} = 5 V
V_{CC} = 220 V
δ = 0.8

$$N = \frac{N1}{N3} = \frac{0.8\left[\frac{220\ V}{2}\right]}{10\ V + 0.7\ V + 0.1\ V + 5\ V} = 5.56 \text{ max}$$

Turns Ratio Calculation for +26 V Output

Assume:

$V_O = 26$ V
$V_D = 0.7$ V
$V_W = 0.1$ V
$V_{REG} = 5$ V
$V_{CC} = 220$ V
$\delta = 0.8$

$$N = \frac{N1}{N4} = \frac{0.8\left[\frac{220\text{ V}}{2}\right]}{26\text{ V} + 0.7\text{ V} + 0.1\text{ V} + 5\text{ V}} = 2.76 \text{ max}$$

Pulse Engineering Transformer PE63203 has turns ratio N1: N2: N3: N4 of 14: 1: 3: 6 and was selected for the application (see Figure 2).

Based on the PE63203 transformer turns ratio of (N1)/(N2) = (14)/(1) = 14, the converter duty cycle, δ, is calculated for various 120-V ac input voltages (assume 35-V filter loss):

Input (V)	δ
96	0.68
120	0.52
132	0.42

Power Transformer Current Calculations

The total power provided to the transformer secondaries is

$$P_{(sec)} \approx 80\text{ A}\ (5\text{ V} + 0.6\text{ V} + 0.1\text{ V}) + 2\text{ A}\ (26\text{ V} + 0.7\text{ V} + 0.1\text{ V} + 5\text{ V}) + 2.5\text{ A}\ (10\text{ V} + 0.7\text{ V} + 0.1\text{ V} + 5\text{ V})$$

$$P_{(sec)} \approx 559.1 \text{ W}.$$

Assuming the inverter transformer efficiency is 95%, the inverter input power is

$$P_{(INV)} \approx \frac{P_{(sec)}}{0.95} \approx \frac{559\text{ W}}{0.95} \approx 588 \text{ W}.$$

Under low line conditions, the maximum duty cycle is 0.68 and the voltage applied to the transformer primary V_P is

$$\frac{V_{CC}}{2} = \frac{236\ V}{2} = 118\ V$$

The peak primary current is

$$I_P \approx \frac{P_{(INV)}}{V_P} \approx \frac{588\ W}{0.68 \times 118\ V} \approx 7.3\ A.$$

The actual peak current is estimated to be about 10% higher or ≈8 A due to magnetizing current in the inverter transformer and current variations in the output filter choke.

Efficiency Estimate

Regulated Output Power = P_O

$$P_O = 5\ V \times 80\ A + 10\ V \times 2.5\ A + 26\ V \times 2\ A$$

$$P_O = 488\ W$$

Input Power for 65% efficiency = P_{IN}.

$$P_{IN} = \frac{P_O}{0.65} \quad \frac{477\ W}{0.65} = 734\ W.$$

A power of 588 W has already been accounted for, so 146 W remains for power transistors, input rectifiers and wiring losses.

Output Filter Design

Choke Inductance Calculations

The output inductor is selected to limit the ripple current the output capacitors must filter. Equation (5) is used to calculate the required inductance, L, once the Δi_L is defined. A Δi_L is equal to 15% of the maximum output current, I_O, is used in this design.

$$L = \frac{(V_O + V_D + V_W + V_{REG})\ (1 - \delta)t}{\Delta i_L} \qquad \text{(Eq.5)}$$

All Equation (5) symbols have been previously defined in Preliminary Calculations except t, which is the clock period of 25 μs. δ is the converter duty cycle of 0.42, previously calculated, for 132-V ac input voltage.

Filter Inductance Calculations for +5 V Output

$$\Delta i_L = 0.15 \times 80 \text{ A} = 12 \text{ A}$$

$$L1 \geq \frac{(5 \text{ V} + 0.6 \text{ V} + 0.1 \text{ V})(1 - 0.42)25 \times 10^{-6}\text{s}}{12 \text{ A}}$$

$$L1 \geq 6.9 \ \mu\text{H}$$

Filter Inductance Calculations for +10 V Output

$$\Delta i_L = 0.15 \times 2.5 \text{ A} = 0.37 \text{ A}$$

$$L2 \geq \frac{(10 \text{ V} + 0.7 \text{ V} + 0.1 \text{ V} + 5 \text{ V})(1 - 0.42)25 \times 10^{-6}\text{s}}{0.37 \text{ A}}$$

$$L2 \geq 619 \ \mu\text{H}$$

Filter Inductance Calculations for +26 V Output

$$\Delta i_L = 0.15 \times 2 \text{ A} = 0.3 \text{ A}$$

$$L3 \geq \frac{(26 \text{ V} + 0.7 \text{ V} + 0.1 \text{ V} + 5 \text{ V})(1 - 0.42)25 \times 10^{-6}\text{s}}{0.3 \text{ A}}$$

$$L3 \geq 1537 \ \mu\text{H}$$

Pulse Engineering laminated output inductors PE50742 (8 μH), PE50731 (590 μH) and PE50732 (2350 μH) were selected for L1, L2, and L3 respectively.

Output Capacitance Calculations

Since the filter inductances have been chosen, the output capacitors can be selected to meet the ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. If good filtering is to be provided, the ripple frequency must be far below those at which the series inductance becomes important, so the two components of interest are the capacitance and the series resistance, R_C. To estimate the ESR ripple voltage, $\Delta V_{O(ESR)}$, it is assumed that all the ripple current in the inductor, Δi_L, flows through the output capacitance.

$$\Delta V_{O(ESR)} = \Delta i_L \, R_S \qquad \text{(Eq.6)}$$

where

ΔV_O = peak-to-peak ripple voltage due to ESR
Δi_L = peak-to-peak ripple current
R_S = capacitor ESR.

The peak-to-peak ripple voltage due to the capacitance is

$$\Delta V_{O(C)} = \frac{\Delta i_L t}{8C} \qquad \text{(Eq.7)}$$

where

t = clock period = 25×10^{-6}s.

Capacitance Calculation for +5 V Output

The peak-to-peak output ripple must, by specification, be less than 125 mV.

The Δi_L will be limited by the 8 μH filter inductor to $\leq$10.3 A.

The maximum capacitor ESR is then

$$R_S \leq \frac{0.125\ V}{10.3\ A} \leq 0.012\ \Omega$$

The Sprague 674D159H7R5JT5A, 15,000-μF/7.5-V capacitor was selected because it has a maximum ESR 0.01 Ω and a maximum ripple current 12.3 A. The ripple due to capacitance is

$$\Delta V_{O(C)} = \frac{10.3\ A \times 25 \times 10^{-6}s}{8 \times 15 \times 10^{-3}F} \approx 2\ mV$$

which is negligible.

Capacitance Calculation for +10 V Output

$$R_S \leq \frac{0.125\ V}{0.37\ A} \leq 0.337\ \Omega$$

$$C \leq \frac{0.37\ A \times 25 \times 10^{-6}}{0.125\ V} \leq 74\ \mu F.$$

The Sprague 672D687H020ET5C, 680-μF/20-V capacitor was selected because it has a maximum ESR 0.08 Ω and a maximum ripple current 2.5 A.

Capacitance Calculation for +26 V Output

$$R_S \leq \frac{0.125\ V}{0.3\ A} \leq 0.416\ \Omega$$

$$C \leq \frac{0.3\ A \times 25 \times 10^{-6}}{0.125\ V} \leq 60\ \mu F$$

The Sprague 672D337H040ET5C, 330-μF/40-V capacitor was selected because it has a maximum ESR 0.2 Ω and a maximum ripple current 2 A.

Magnetic Design

20-kHz Power Transformer

A ferrite "E" core with a rectangular center leg is used for the power transformer. Dimensions are shown in Figure 4. This is generally the most economical shape and is easy to wind and insulate. The core has a throughput power rating of 620 W for a 40 °C temperature rise.

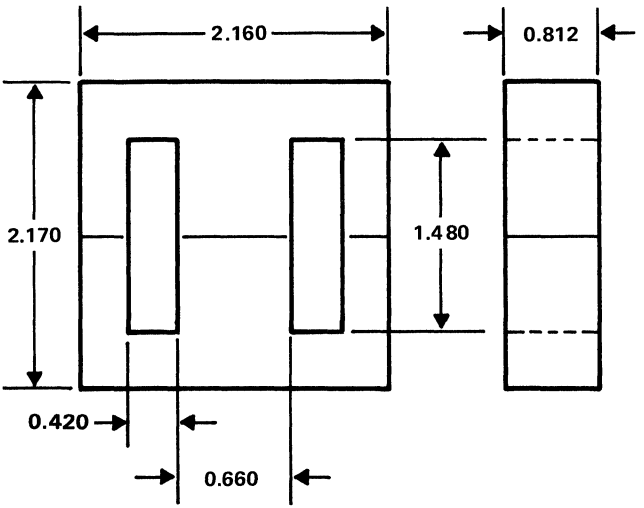


Figure 4. Core Dimensions

The coil is designed with 8-mm creepage/clearance and three layers of 0.1-mm thick insulation between the primary and secondaries to comply with the most common international safety requirements for construction. The 5-V winding is wound with copper foil for low ac winding resistance at 20 kHz. To further reduce ac resistance and to minimize leakage inductance of the 5-V output, windings are arranged as shown in Figure 5. Low leakage inductance is illustrated by the low voltage overshoot at the start of "dead-time" in Figure 26. Data for this application are tabulated in Table 1.

Table 1. Power Transformer Data

	1/2 Primary	5 V Secondary	10 V Secondary	26 V Secondary
Turns	28	2–0–2	6–0–6	12–0–12
Conductor Size	19 AWG	2X.01 Cu	22 AWG	22 AWG
Pk Term, Voltage	100	7.96	23.57	47.1
DC Term, Voltage ⑤	—	5.66	16.97	33.9
DC Current, A	—	80	2.5	2.0
RMS Wdg Current ⑤	5.72	52.5	1.64	1.31
Throughput Power, W	562.2	452	42.4	67.8
DC Resistance,	0.079	0.0007	0.095	0.185
AC Resistance,	0.130	0.0007	0.100	0.194
Copper Loss, W ⑤	2.13 ①	1.93	0.27	0.33

Total Cu Loss: 4.66 Core Loss: 1.04 Total Loss: 5.7 W ④

① Primary halves parallel connected.
② Nominal primary leakage inductance: 3 μH (5-V Secondary shorted)
③ Primary throughput power = Σ (dc Term Voltage) × (dc Current)
④ Transformer efficiency = 99% at 562 W throughput power.
⑤ At 72% duty cycle.

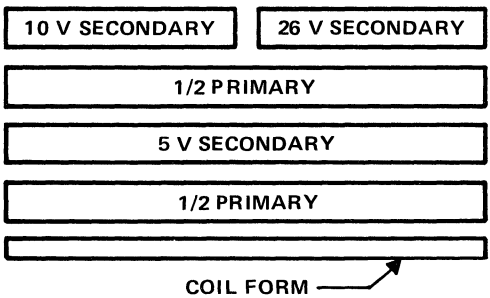


Figure 5. Coil Construction

20-kHz Base-Drive Transformer

The design objectives for the base-drive transformers were to provide:

1) Base current of 1.0 A minimum
2) Fast base-current rise time
3) Simple means to clamp dead-time voltage
4) Balanced secondary waveforms
5) Insulation for off-line operation.

To meet the first objective, ferrite E cores sized to limit temperature rise to 40 °C were selected. E cores are easier to insulate reliably for off-line operation than toroids or more complex shapes. Units are fully encapsulated for improved insulation and thermal characteristics. The transformers will withstand 1500 Vrms dielectric strength test between base windings. Temperature rise is under 40 °C at 1.5 A base current.

To obtain fast base-current rise time, minimum turns limited by core saturation are used and the base windings are tightly coupled to the primary. The clamp winding is also tightly coupled to the primary to assure effective core shorting during the dead time using the circuitry described in the Preliminary Calculations Section.

The winding sequence of Figure 6 is used to obtain coupling requirements. Base windings are multifilar wound for balanced drive.

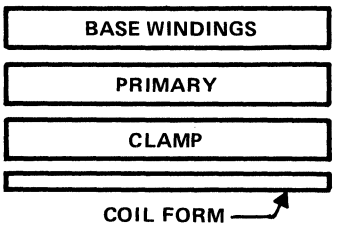


Figure 6. Winding Sequence

A simplified equivalent is shown in circuit Figure 7 and calculations are discussed.

From catalog data for Pulse Engineering PE62129, the internal secondary resistance (R_{Si}) is 0.14 Ω, yielding a typical internal voltage drop of 0.14 V/A amp of load current. Since this is usually negligible, the following are reasonable approximations:

Secondary terminal voltage (V_S):

$$V_S \cong V_{in}/n \qquad \text{(Eq.8)}$$

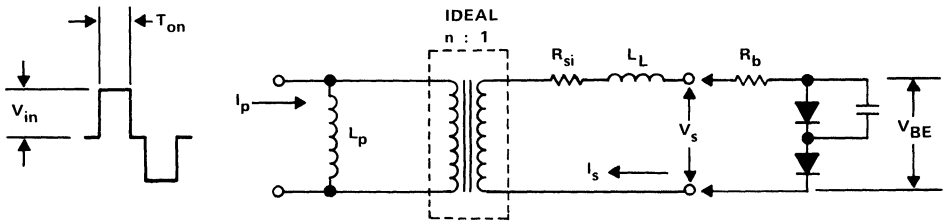
Peak secondary current (I_S):

$$I_S \simeq \frac{V_S - V_{BE}}{R_b} \qquad \text{(Eq.9)}$$

Note: $I_S = I_{B1}$

Solving Eq. 9 for R_b:

$$R_b = \frac{V_S - V_{BE}}{I_S} \qquad \text{(Eq.10)}$$



NOTE: R_{si} = SECONDARY INTERNAL RESISTANCE = $R_p/n^2 + R_s$
R_b = BASE CURRENT LIMITING RESISTOR
R_p = PRIMARY WINDING RESISTANCE
R_s = SECONDARY WINDING RESISTANCE
n = PRIMARY TO SECONDARY TURNS RATIO

Figure 7. Simplified Transformer Equivalent Circuit and Calculations

Peak primary current (I_p):

$$I_p = \frac{K}{n} I_s + \frac{V_{in}\, t_{on}}{L_p} \qquad \text{(Eq.11)}$$

Note: K is the number of secondaries conducting at any time (secondaries assumed identical). The second term is the peak value of the current ramp due to primary inductance.

Leakage inductance impacts the rate of current rise after the load semiconductor starts conducting. Rise time (t_r) is approximately:

$$t_r = \frac{2.2\, L_L}{R_e} \qquad \text{(Eq.12)}$$

Note: R_e is the effective secondary load resistance and is nonlinear. To estimate rise time, take $R_e = V_S/I_S$

Calculations for this application (Figure 7):
Conditions:

Circuit	: Half-bridge (K = 1)
Input voltage	: 14 V
Turns ratio	: n = 3
Power-on time	: t_{on} = 18 μs maximum
Primary inductance	: L_p = 1.25 mH
Leakage inductance	: L_L = 0.85 μH
Base-emitter voltage	: V_{BE} = 1 V

Determine I_{B1} to obtain $R_b = 5\ \Omega$

$$V_S = 14/3 = 4.67\ V \qquad \text{from Eq.8}$$

$$I_{B1} = \frac{4.67 - 1.0}{5} = 0.73\ A \qquad \text{from Eq.9}$$

since $I_{B1} = I_S$

Determine peak primary current:

$$I_p = \frac{1}{3} \times 0.73 + \frac{14 \times 18 \times 10^{-6}}{1.25 \times 10^{-3}} = 0.24 + 0.20$$

$$= 0.44\ A \qquad \text{from Eq.11}$$

Estimate base current rise time:

$$t_r = \frac{2.2 \times 0.85 \times 10^{-6}}{4.67} = 0.4\ \mu s \qquad \text{from Eq.12}$$

Note: This yields $\beta \cong 10$ which is satisfactory. I_{B1} could be increased to 1 A at the expense of increased losses by reducing R_b to 3.5 Ω.

Waveforms for a load as shown in the equivalent circuit with $R_b = 2.5\ \Omega$ and $V_{BE} = 2$ V are shown in Figure 8.

Current Sense Inductor

From Figure 9, it can be seen that magnetizing current is "robbed" from the input current. This results in a droop of the voltage waveforms with rectangular current pulses.

Primary voltage is:

$$V_p = \frac{(I_{in} - I_m)\ (R_s + R_{ser} + R_t)}{n^2}$$

If $I_m << I_{in}$:

$$V_p = \frac{I_{in}(R_s + R_{ser} + R_t)}{n^2}$$

And the output voltage is:

$$V_o = \frac{I_{in}\ R_t}{n}$$

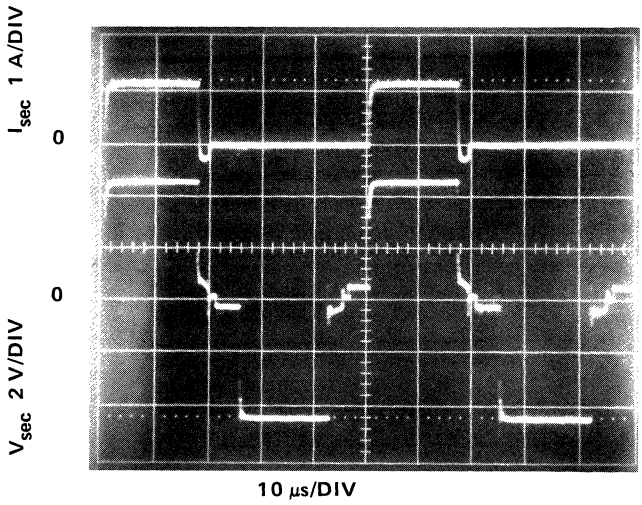
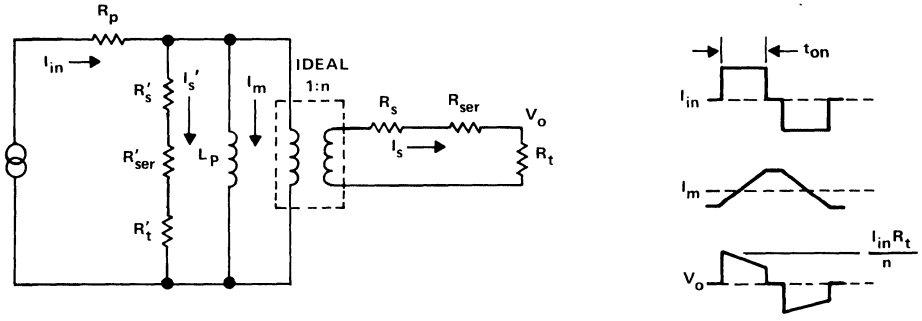


Figure 8. 20-kHz Base-Drive Transformer Waveform



R_p = PRIMARY WINDING RESISTANCE
R_s = SECONDARY WINDING RESISTANCE
R_{ser} = EXTERNAL RESISTANCE IN SERIES WITH TERMINATING RESISTOR
R_t = TERMINATING RESISTOR
L_p = PRIMARY INDUCTANCE
n = PRIMARY-TO-SECONDARY TURNS RATIO OR SECONDARY TURNS FOR ONE TURN PRIMARY
I_{in} = INPUT CURRENT
I_m = MAGNETIZING CURRENT
I_s = SECONDARY CURRENT

NOTE: PRIMES FOR SECONDARY VALUES REFERRED TO PRIMARY.

Figure 9. Simplified Equivalent Circuit

If the primary is one turn and the terminating resistor ohmic value equals turns, output voltage is 1 V/A of output current (scale factor). The scale factor is proportional to the terminating resistor and independent of winding and other series resistances.

For minimum output voltage droop, magnetizing current must be low. For rectangular pulses, magnetizing current is approximately:

$$I_m \cong \frac{V_p\ t_{on}}{L_p} \cong \frac{I_{in}\ (R_s + R_{ser} + R_t)\ t_{on}}{n^2 L_p}$$

This neglects voltage droop.

The PE51719 has 100 turns on each side of the center tap. Resistance of each side is 2 Ω. A one-turn primary has 2-μH inductance and will support a 4 V-μs unipolar, or an 8 V-μs bipolar waveform.

For this application, peak input current is 8 A and maximum t_{on} is 18 μs. A diode is in series with the 100-Ω terminating resistor R32. Assuming 0.6-V drop, effective diode resistance is approximately $0.6\ n/I_{in} = 0.6(100)8 = 7.5\ \Omega$. Shunting of R31, R30, and Q6 is negligible. Magnetizing current is approximately:

$$I_m \cong \frac{8(2 + 7.5 + 100)(18 \times 10^{-6})}{100^2\ (2 \times 10^{-6})} \cong 0.79\ A$$

This results in output voltage droop of about 10%. $V_p t_{on}$ is 1.75 V-μs which is well within the 8 V-μs rating. Droop and scale factor could be reduced by using a smaller terminating resistor.

Local Power Supply

The function of the local (auxilliary) power supply is to provide the TL494 control circuit and the base drive section with a source of regulated power. The anticipated power requirement for the TL494 is 100 mA at 15 V and the anticipated base drive section power requirement is 500 mA at 15 V. The estimated total regulated power is therefore 600 mA at 15 V. A 60-Hz transformer, rectifier, linear regulator system was selected.

The secondary voltage rating, V_S, of the transformer was then calculated based on (Eq.13).

$$V_S = \frac{V_D + \Delta V_C + V_{REG} + V_O}{\sqrt{2}} \qquad \text{(Eq.13)}$$

where

V_{REG} = linear regulator Δ Voltage = 3 V
V_D = rectifier voltage = 1 V
ΔV_C = filter capacitor voltage swing = 4 V
V_O = regulated output voltage = 15 V

$$V_S = \frac{1\ V + 4\ V + 3\ V + 15\ V}{\sqrt{2}} = 16.3\ Vrms$$

The nearest commercial transformer secondary voltage value to 16.3 V is probably 24 V, therefore the wattage rating of the 60-Hz transformer should be 14.4 W, i.e.,

$$VA = (24\ V)\ (0.6\ A) = 14.4\ W.$$

The input filter capacitor, C10, minimum value was determined to be 846 μF based on (Eq.14). A 1000-μF/50-V capacitor was selected.

$$C10 = \frac{2 \times P_{IN} \times t_h}{[(V_{CC1})^2 - (V_{CC2})^2]} \qquad \text{(Eq.14)}$$

where

$P_{IN} = 0.6\ A \times 18\ V = 10.8\ W$

t_h = hold-up time = $10 \times 10^{-3} s$

$V_{CC1} = \sqrt{2} \times 24\ V = 33.9\ V$

$V_{CC2} = \sqrt{2} \times 24\ V - 4\ V = 29.9\ V$

Control Circuit

Description

The TL494 integrated circuit (Figure 10) was selected for the control of the power supply over a discrete design to take advantage of the lower component count with the TL494.

In addition to the basic functions of oscillator, pulse-width modulator, and error amplifier, the circuit also provides independent dead-time control and overcurrent detection.

The TL494 supply voltage can be varied in the range 7 V – 40 V. The reference voltage developed on the integrated circuit is 5 V ±5% and is set by a bandgap reference giving excellent immunity to supply and temperature variation.

The TL494 also has an output control logic feature which allows single-ended (90% max duty cycle) or push-pull operation (45% max duty cycle at each output).

Oscillator

The TL494's oscillator frequency is programmed with an external capacitor and an external resistor, pins 5 and 6. The oscillator clock frequency, f_{op}, must be set at 40 kHz for the converter to operate at the specified 20 kHz.

$$f_{op} = \frac{1}{2\ R_T\ C_T} \qquad \text{(Eq.15)}$$

Choose $C_T = 0.001\ \mu F$ and calculate R_T.

$$R_T = \frac{1}{2 \times 20 \times 10^3 \times 0.001 \times 10^{-6}}$$

$$= 25\ k\Omega$$

Dead-Time Generator

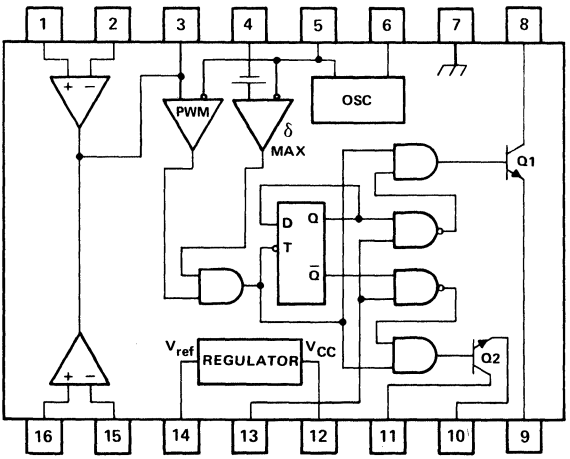
The duty cycle must not be limited to less than 68% or the supply may not be able to output rated voltage at low input line voltage. It is also important to limit the maximum duty cycle to 86% or less to allow the TIPL755 power switches 3.5 μs of storage time. An 80% duty cycle design was selected. By choosing R23 = 1 kΩ, R22 was calculated to be 9 kΩ.

$$\frac{t}{t_d} = \frac{3\ V}{0.1\ V + 5\ V\left[\frac{R23}{R23 + R22}\right]} \qquad \text{(Eq.16)}$$

where

$t = 25\ \mu s$ = clock period
$t_d = 5\ \mu s$ = dead time
$R_{23} = 1\ k\Omega$

The dead-time generator circuit is shown in Figure 11.



PIN NO.	FUNCTION
1.	ERROR AMP. 1, NONINVERTING INPUT
2.	ERROR AMP. 1, INVERTING INPUT
3.	COMPENSATION INPUT
4.	DEAD TIME CONTROL INPUT
5.	OSCILLATOR TIMING CAPACITOR
6.	OSCILLATOR TIMING RESISTOR
7.	GROUND
8.	DRIVE TRANSISTOR 1, COLLECTOR
9.	DRIVE TRANSISTOR 1, EMITTER
10.	DRIVE TRANSISTOR 2, EMITTER
11.	DRIVE TRANSISTOR 2, COLLECTOR
12.	INPUT SUPPLY
13.	OUTPUT MODE CONTROL
14.	STABILIZED REFERENCE VOLTAGE
15.	ERROR AMP 2, INVERTING INPUT
16.	ERROR AMP 2, NONINVERTING INPUT

Figure 10. TL494 Block Diagram and Pin Assignments

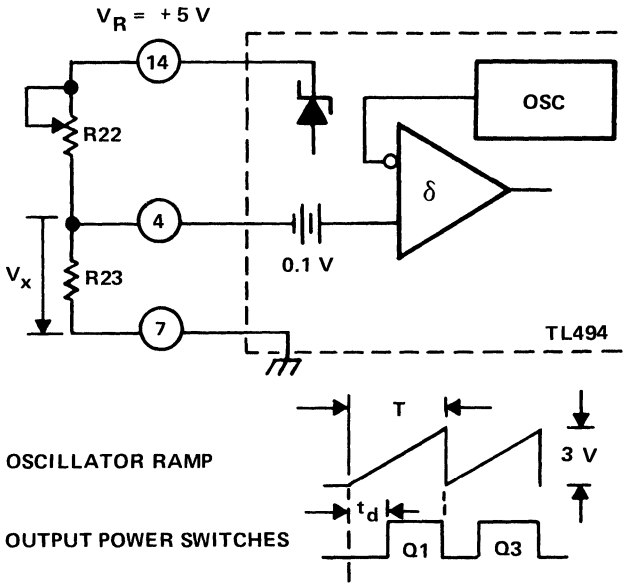


Figure 11. Dead-Time Generator

Error Amplifier

The error amplifier (Figure 12) compares a sample of +5-V output to a voltage reference and adjusts the pulse-width modulator to maintain the proper output. It also contains the compensation input for the network which shapes the frequency response of the regulator so that it is stable over the range of the line and load variations.

Protection Networks

Soft-Start Circuitry

In order to reduce the stress on the TIPL755 power switches at power supply startup, it is necessary to reduce the startup surge which is otherwise seen as the output filter capacitors charge.

By applying a negative slope waveform to pin 4 of the TL494's dead-time comparator, this "soft-start" characteristic is achieved, allowing the pulse width at the output stage to increase slowly (Figure 13).

The soft-start timing capacitor is selected to provide a time constant, t_{const}, which is approximately one-third the desired output rise time, t_r, of 50 ms.

$$t_{const} = 1/3\ t_r = \frac{(C15)\ (R22 \times R23)}{[R22 + R23]}$$

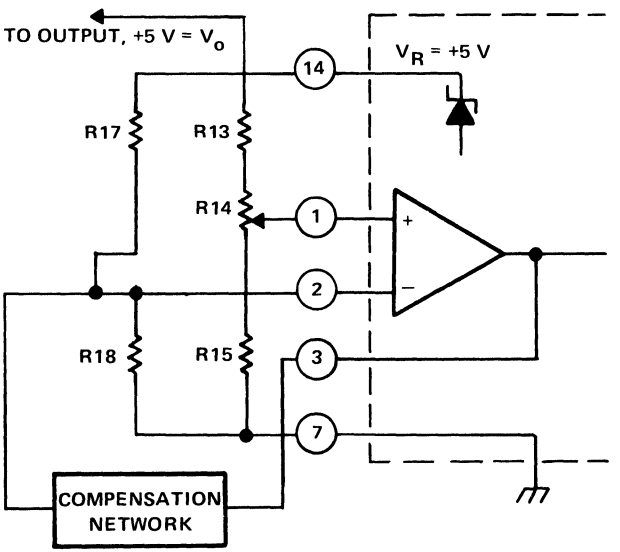
or

$$C15 = \left[1/3\ t_r\right]\left[\frac{R22 + R23}{R22 \times R23}\right] \qquad \text{(Eq.17)}$$

C15 is calculated to be 18 μF

where

t_r = 50 ms
R22 = 9 kΩ
R23 = 1 kΩ



$$V_o = \left(V_R\right)\left(\frac{R18}{R17 + R18}\right)\left(1 + \frac{R13 + \frac{R14}{2}}{R15 + \frac{R14}{2}}\right)$$

WHERE V_R = 5 V

R14 POTENTIOMETER SET MID VALUE

Figure 12. Error Amplifier

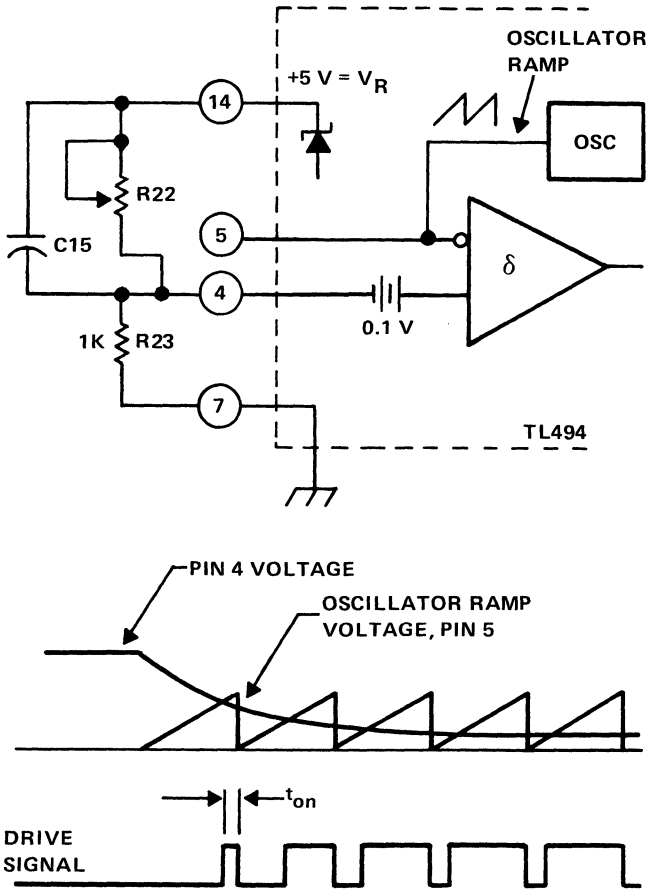


Figure 13. Soft-Start Circuit

Undervoltage Protection

In the low supply condition, ($V_{CC} \leq 7$ V), correct operation of the control logic cannot be guaranteed even when pin 13 is correctly wired to the regulated voltage source and the pulse-steering flip-flop is enabled. Under this low voltage condition, simultaneous conduction of both outputs may occur and, of course, TIPL755 immediate destruction is certain to follow.

The circuit shown in Figure 14 is designed to cause Q5 to be turned on when $V_{CC} \leq 9.4$ V. This Q5 on condition causes the reference voltage to be applied to pin 4 of dead-time comparator which causes both outputs to be disabled. (The TL494A has a monolithic undervoltage protection network and its use eliminates the Figure 14 circuit.)

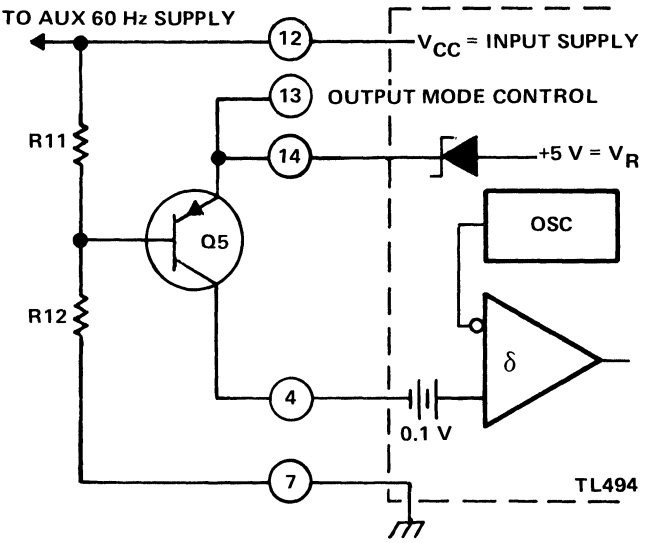


Figure 14. Undervoltage Protection Circuit

The R11, R12 voltage divider was designed according to Equation 18.

$$\left[V_{CC(min)}\right]\left[\frac{R12}{R11+R12}\right] = V_R - V_{BE(Q5)} \qquad \text{(Eq.18)}$$

where

$V_{CC(min)}$ = 9.4 V
V_R = 5 V = reference voltage
$V_{BE(Q5)}$ = 0.7 V (assumed)
R12 = 4.7 kΩ

Overcurrent Protection

A current sense inductor, T4, is placed in the primary side of the power transformer, T3, so that it will be responsive to core saturation as well as provide overcurrent limiting by use of the TL494 dead-time control input (Figure 15).

The load fault primary current, I_p, chosen for the design is 8 A based on the peak primary current calculation of the Preliminary Calculations Section.

Pulse Engineering current sense inductor PE51719, when connected to a 100-Ω terminating resistance, is designed to generate an output voltage, V_O, of 1 V/A. Therefore, at the 8-A fault condition, an output voltage, V_O, of approximately 8 V will be produced. At V_O = 8 V, the voltage divider network consisting of R30 and R31 is designed to turn

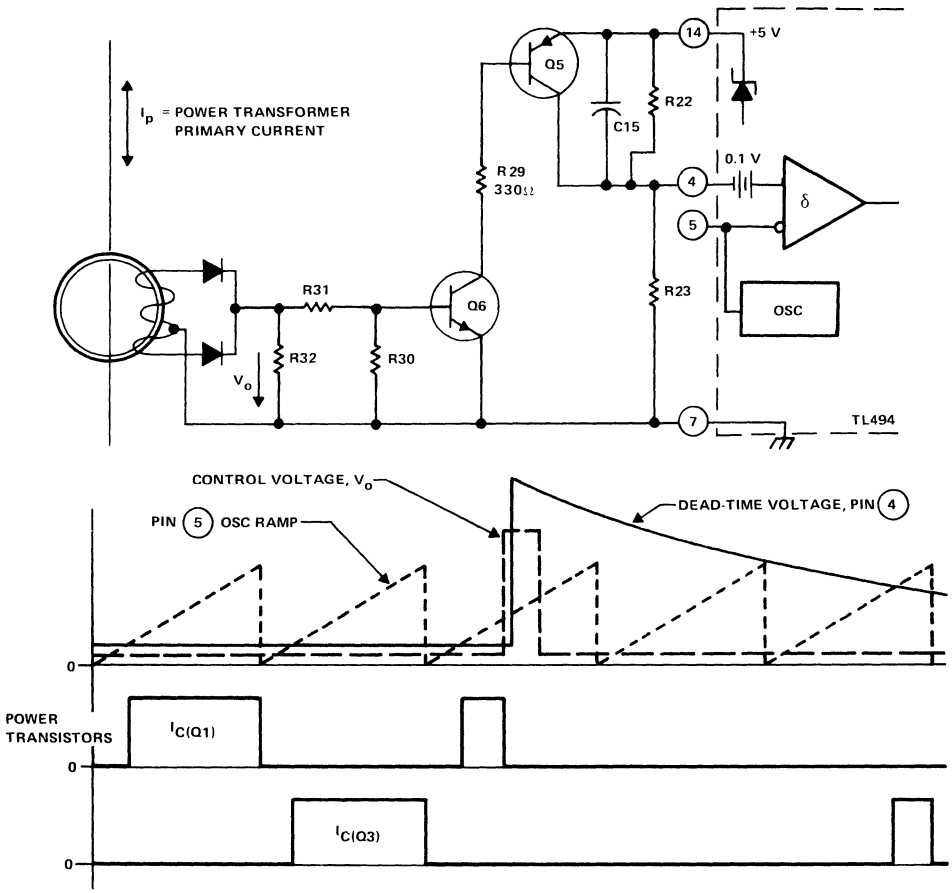


Figure 15. Overcurrent Protection Circuit

on Q6 which turns on Q5. The turned-on Q5 applies the +5 V reference voltage to pin 4 of the dead-time comparator. The reference voltage on pin 4 causes the output drive to be terminated and also toggles the pulse-steering flip-flop to the other output drive prior to the completion of the oscillator period. However, both output drives are inhibited because C15 is discharged through the turned-on Q5 and this action causes a voltage to remain on pin 4 until C15 can charge through R23 according to the normal "soft-start" mode described in this section.

Overvoltage Protection Circuit

The MC3423 is used to sense an overvoltage condition at the 5-V/80-A output and will trigger the crowbar SCR2. The trip voltage is programmed at 5.3 V, reference Equation 15. See Figure 16.

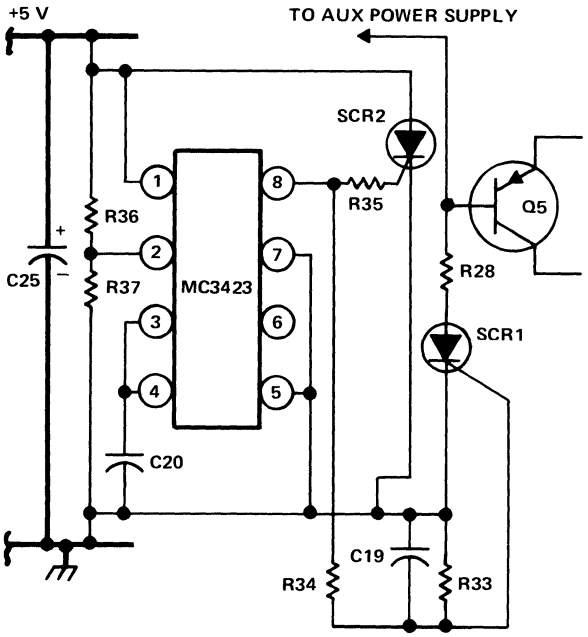


Figure 16. Overvoltage Protection Circuit

$$V_{trip} \approx V_{REF}\left[1 + \frac{R36}{R37}\right] \qquad \text{(Eq.19)}$$

where

$R36 = 4.7\ k\Omega$
$R37 = 5.1\ k\Omega$
$V_{REF} = 2.75\ V$ max

The MC3423 is also programmed for a 40-μs minimum duration of overvoltage condition, t_d, before triggering, thus supplying noise immunity, reference Equation 20.

$$t_d \approx \left[1.2 \times 10^4\right] C20 \qquad \text{(Eq.20)}$$

where

$C20 = 0.0033\ \mu F$
$t_d = \mu s$ duration overvoltage

Any overvoltage condition that causes crowbar SCR2 to fire also causes a signal to be concurrently sent to SCR1 and it is also caused to fire. The turned-on SCR1 provides base current to Q5. Q5 turns on and provides $\approx$ 4 V to the TL494 dead-time control, which shuts down the converter and thereby prevents the crowbar SCR from destruction. To reset, the power supply must be turned off for at least 15 seconds.

Base Driver Section

The base driver section is designed to provide an electrical isolation interface between the TL494 control circuit and the TIPL755 power transistor switches. This driver section also provides current outputs of approximately 1 A to the bases of the power switches. It is necessary to provide about 1-A base drive in order for the TIPL755s to switch as much as an 8-A transformer primary current.

To provide the required isolation, Pulse Engineering's 20-kHz Base-Drive Transformer PE62129, with two secondaries, was selected. This transformer is designed with a 15:15:5 turns ratio and 15-V input, 5-V/1.5-A output. An important feature of this base drive transformer is that a clamp winding is provided to eliminate switching transients during the turnoff or converter "dead-time" interval. The clamp winding is shorted to ground during the converter "dead-time" by means of a 1/2 SN75413 OR driver that has its two inputs connected to the respective TL494 outputs. The TL494 is operating in a push-pull mode so that one output is high while the other is low, except during the "dead-time" interval when both emitter follower outputs are low, e.g.:

	TL494 Outputs (SN75413 Inputs)		SN75413
	Output A	Output B	Output
	H	L	H
("Dead-Time")	L	L	L
	L	H	H
("Dead-Time")	L	L	L

When driving a 1-A load, the PE62129 primary current is estimated to be = 0.44 A (see the Magnetic Design Section). The maximum current of the TL494 output transistors is only 250 mA, therefore a predriver stage was needed. To meet this requirement, the ULN2066, which has a 1.5-A current rating, was selected to drive the transformer primary. Because the transformer primary is connected in a push-pull configuration operating from +15 V, the ULN2066 must switch 30 V or double the +15-V supply. The ULN2066 has a 50-V rating; therefore, an approximate 20-V safety margin exists. To provide a low impedance off-drive for a reduction of storage time and fall time of the power switches, the circuit shown in Figure 17 was incorporated into the design to provide approximately 1.5-A I_{B2} reverse-bias current.

Feedback Loop Stabilization

Many papers have been written concerning the mathematical analysis of feedback loop phase-gain calculations and equipment measurement techniques. Some of these papers are listed in the references. The error amplifier and loop compensation network design methods used in this report are based on techniques presented in the Texas Instruments Incorporated, *Switching Power Supply Design Student Guide*, Chicago Regional Technology Center.

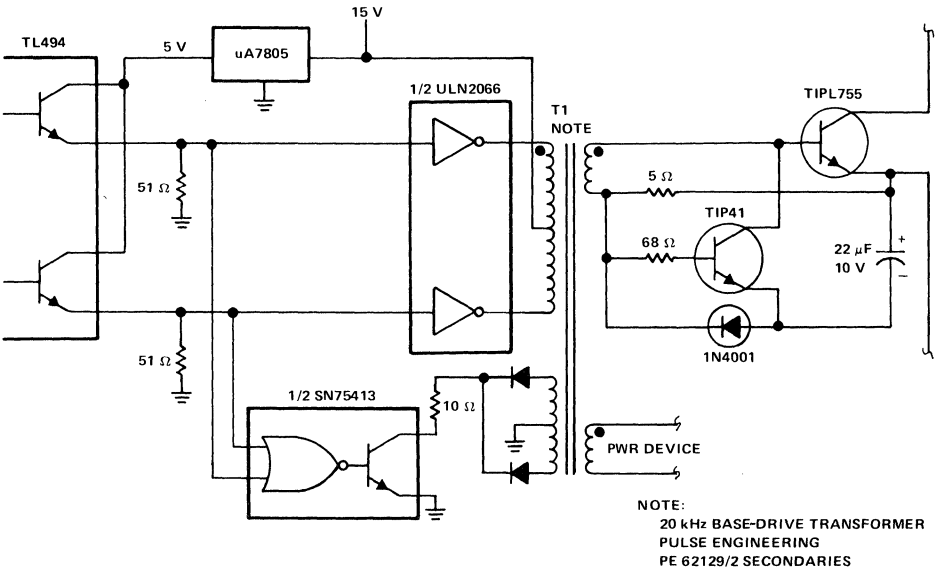


Figure 17. Base Driver Section for Power Converter

This power supply system is described by a total linearized single-loop model made up of five stages, as shown in Figure 18.

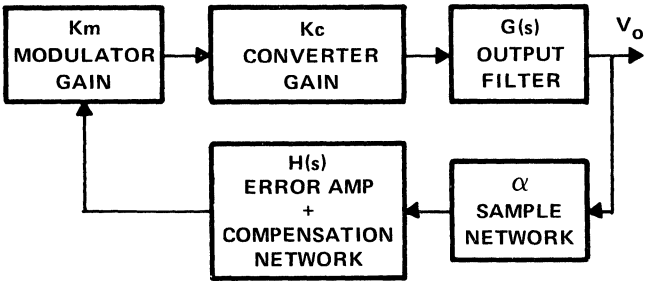


Figure 18. Linearized Loop Model

Km: Pulse-Width Modulator Gain

The pulse-width modulator converts an error voltage into a drive pulse width. Its gain is the change in pulse width resulting from a change in error voltage. The modulator used in the TL494 is a comparator with a triangular wave applied to one input and the error signal applied to the other; drive command duration is equal to the time the sawtooth exceeds the error voltage. The drive pulse width changes from maximum to minimum as the error signal changes from the minimum ramp value to its maximum.

Therefore

$$Km = \frac{t_{on(max)} - t_{on(min)}}{V_{ramp(min)} - V_{ramp(max)}}$$

where

$t_{on(max)}$ = maximum drive period = t = 25 μs
$t_{on(min)}$ = minimum period = 0
$V_{ramp(min)} \approx 0$ V
$V_{ramp(max)} \approx 3$ V

$$Km = \frac{25\ \mu s}{-3\ V} = -8.34\ \mu s/V$$

Kc: Converter Gain

The gain of the converter is the change in output voltage relative to a change in drive pulsewidth.

$$Kc = \frac{\Delta V_o}{\Delta t_{on}} = \frac{\frac{V_{CC}}{2\ n} - V_D}{t}$$

where

V_{CC} = converter input voltage = 290 V
n = turns ratio = 14
V_D = rectifier drop $\approx$ 1 V
t = clock period = 25 μs

$$Kc = \frac{\frac{290\ V}{2 \times 14} - 1\ V}{25\ \mu s} = 0.37\ V/\mu s.$$

G(s): Output Filter Response

The model shown in Figure 19 is used to predict the low-pass filter response and filter break frequency, f_f.

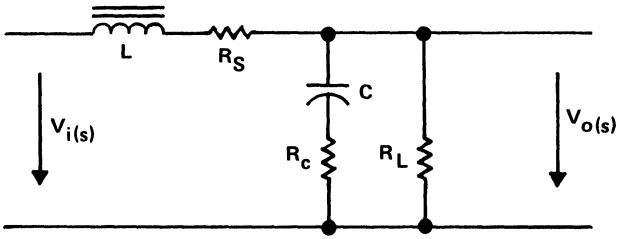


Figure 19. Output Filter Model

where

L = output choke inductance $\approx$ 8 μH
C = output capacitance $\approx$ 15,000 μF
R_S = wiring and choke resistance $\approx$ 0.01 Ω
R_C = output capacitor ESR $\approx$ 0.006 Ω
R_L = load resistance $\approx$ 0.0625 Ω minimum

without going through the mathematics,

$$G(s) = \frac{V_o(s)}{V_i(s)}$$

$$= \frac{R_C R_L (s + 1/R_C C)/L (R_L + R_C)}{s^2 + s\left[\frac{1}{(R_L + R_C)C} + \frac{R_S}{L} + \frac{R_L R_C}{L(R_L + R_C)}\right] + \frac{R_S + R_L}{L(R_L + R_C)C}}$$

The open-loop response of the regulator is

$$\frac{V_{o(s)}}{V_{in}} = Km \times Kc \times G(s)$$

The filter break frequency is

$$f_f = \frac{1}{2\,\pi\,\sqrt{LC}}$$

$$f_f = \frac{1}{2\,\pi\sqrt{8 \times 10^{-6}H \times 15{,}000 \times 10^{-6}F}}$$

A compensation network was designed to provide a zero, f_{z1} near the filter break frequency, f_f, and a pole at a much higher frequency, f_{p2}, where the response has already gone through unity. Since very high gains at low frequencies are required for dc accuracy,

an additional pole, f_{p1}, and a zero, f_{z2}, are required. The pole, f_{p1}, is positioned at 50 Hz to reduce the gain sufficiently for the regulator response to go through unity gain, f_T, beyond the filter breakpoint but well below the regulator operating frequency, f_O = 20 kHz. The zero, f_{z2}, is positioned at the filter break frequency to cancel the slope of the response due to the filter low frequency pole. The net effect is an open-loop response with a slope of approximately −20 dB/decade through unity gain, see Figure 20.

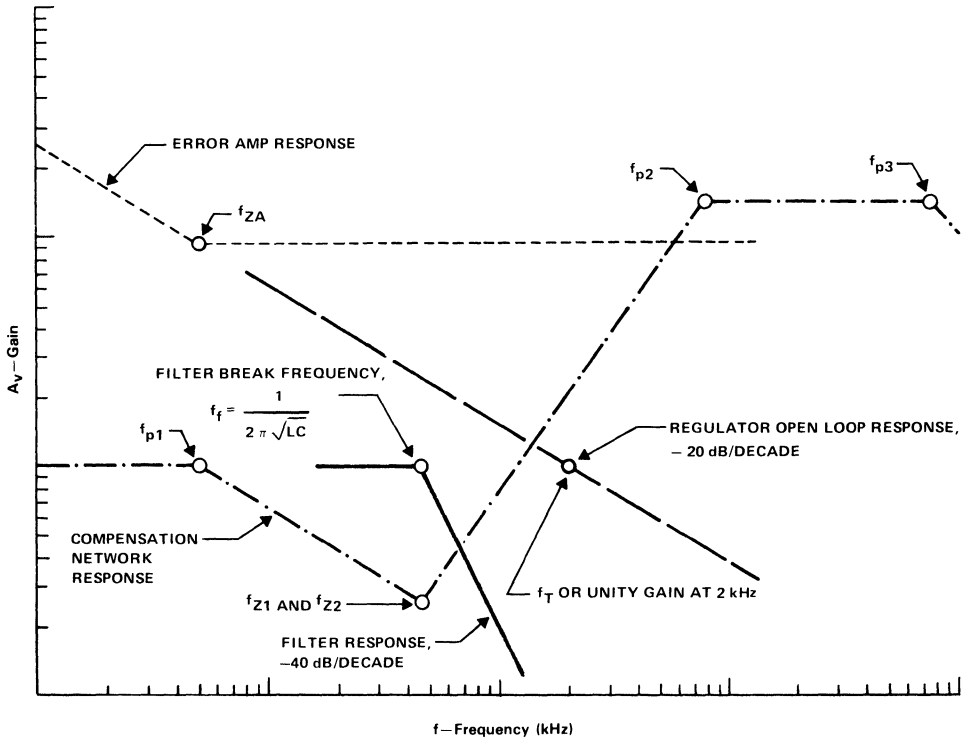


Figure 20. Frequency Response Curves

The following equations and chosen values were used to calculate the component values for the compensation network, see Figure 21.

$$f_f = f_{z1} = \frac{1}{2\pi\sqrt{LC}}$$

$$f_T = 2000\ \text{Hz} = \frac{\frac{R13}{(R13+R15)}\,Km \times Kc}{2\pi\ R19\ C17}$$

$$f_{za} = 50\ \text{Hz} = \frac{1}{2\pi(R20+R19)\ C17}$$

$$f_{p1} = 50\ \text{Hz} = \frac{1}{2\pi[(R13 \| R15)+R16]\ C13}$$

$$f_{z1} = 460\ \text{Hz} = \frac{1}{2\pi\ R16\ C13}$$

$$f_{z2} = 460\ \text{Hz} = \frac{1}{2\pi\ (R13+R21)\ C16}$$

$$f_{p2} = 8{,}000\ \text{Hz} = \frac{1}{2\pi\ [(R13 \| R15 \| R16)+R21]\ C16}$$

$$f_{p3} = 40{,}000\ \text{Hz} = \frac{1}{2\pi\ (R13 \| R15 \| R21 \| R16)\ C14}$$

where

$L = 8\ \mu H$
$C = 15{,}000\ \mu F$
$Km = 8.34\ \mu s/V$
$Kc = 0.37\ V/\mu s$
$C17 = 0.02\ \mu F$
$C13 = 0.47\ \mu F$

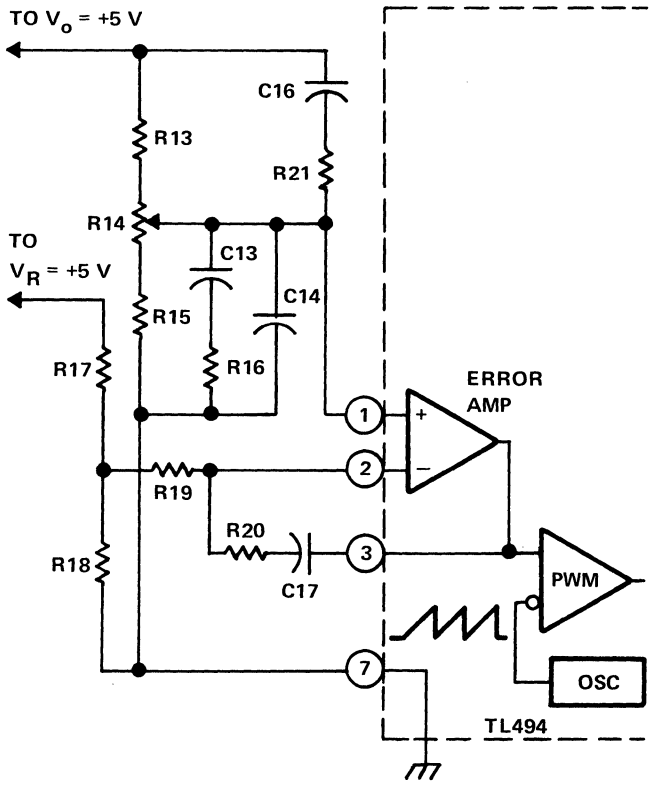
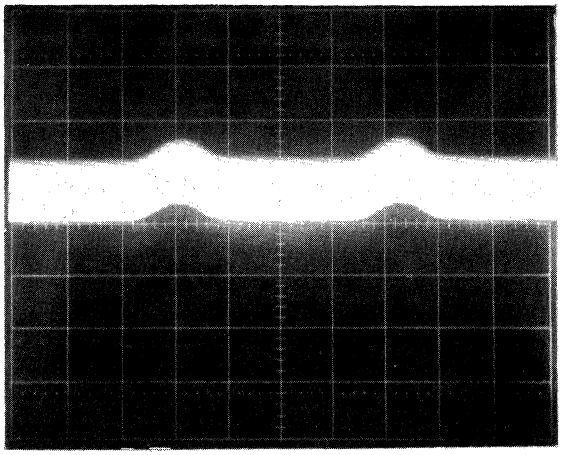


Figure 21. Error Amplifier and Loop Compensation Network

Measurement Results and Conclusions

Measurements of load and line regulation were made at various input voltages while load conditions were changed from 5 A to 80 A at each input voltage. The overall regulation of each of the 10-V and 26-V outputs, which are regulated by linear regulators, was measured as better than 1%. The overall regulation of the 5-V, 80-A output, which is regulated by the TL494 master control, was measured as 0%. The test results are shown in Table 2.

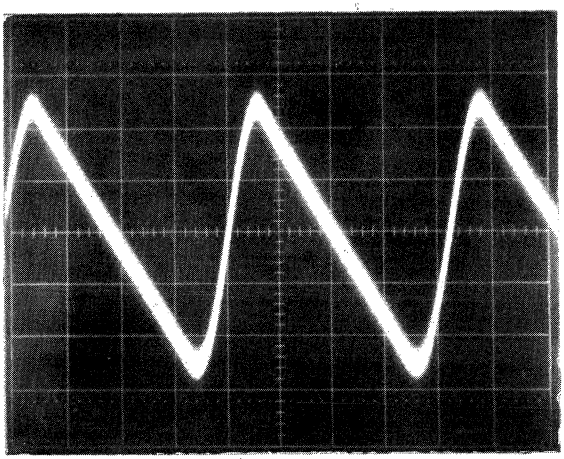
The 40-kHz ripple of the 5-V output was measured as approximately 60 mV peak-to-peak (Figure 22). The ripple across the 60-Hz input line voltage capacitors under 80-A full-load conditions was measured as approximately 11-V peak-to-peak (Figure 23).



VERTICAL: 50 mV/cm HORIZONTAL: 2 ms/cm

V_{IN} = 120 V_{rms}
V_{CC} = 304 V dc
LOAD = 80 A/5 V

Figure 22. The 40-kHz 5-V Output Filter Ripple



VERTICAL: 2 V/cm HORIZONTAL: 2 ms/cm

V_{IN} = 120 V_{rms}
V_{CC} = 304 V dc
LOAD = 80 A/5 V

Figure 23. The 60-Hz Input Line Filter Ripple

One of the more important accomplishments of this work was the design and a subsequent successful evaluation of the overcurrent network described in the Protection Network Section. This network, consisting in part of current sense inductor T4 that is placed in the primary side of the power transformer T3, not only proved its capability to provide short circuit protection for the 80-A output but it also eliminated the need for a capacitor to be connected in series with the primary of the power transformer T3. Usually in bridge-type converter circuits, a low ESR, high-voltage capacitor is required to be connected in series with the primary of the power transformer to provide protection against transformer core saturation due to the switching time differences of the power transistors.

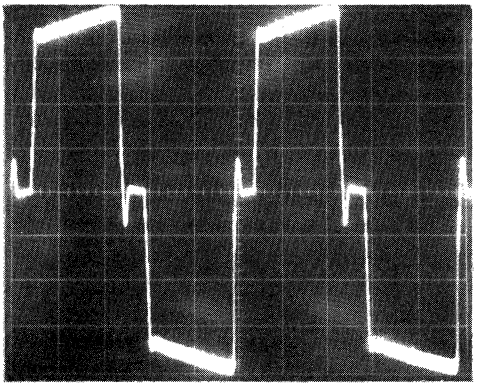
Table 2. Measured Regulation Characteristics

V_{IN} INPUT LINE VOLTAGE (V_{rms})	V_{CC} LINE FILTER VOLTAGE (V_{dc})	V_o = 5 V			V_o = 26 V			V_o = 10 V		
		V_{om} (V)	I_o (A)	% REG*	V_{om} (V)	I_o (A)	% REG*	V_{om} (V)	I_o (A)	% REG*
96	237	5.00	80	0	26.03	2	0.115	10.09	2.5	0.9
		5.00	5	0	25.99	2	−0.384	10.08	2.5	0.8
120	304	5.00	80	0	26.03	2	0.115	10.08	2.5	0.8
		5.00	5	0	26.00	2	0	10.08	2.5	0.8
132	335	5.00	80	0	26.03	2	0.11	10.08	2.5	0.8
		5.00	5	0	25.99	2	−0.038	10.08	2.5	0.8

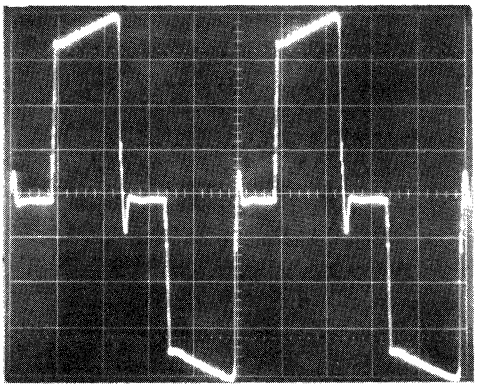
*% Regulation $= \frac{V_{om} - V_o}{V_o} \times 100\%$

Figure 24 shows the T3 power transformer primary current, thereby illustrating the excellent current symmetry characteristic obtained under various input voltage conditions of 96 V_{rms}, 120 V_{rms}, and 132 V_{rms} during constant 100% load.

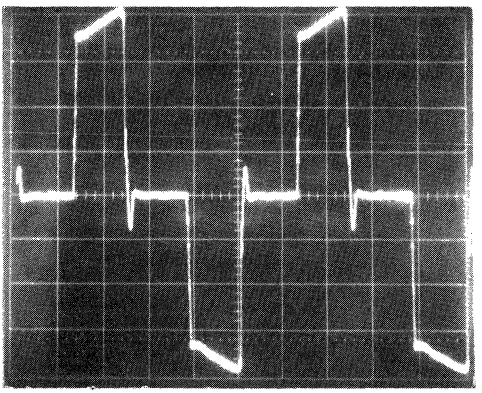
Figures 25 and 26 of the TIPL755 power transistor's collector voltage and current characteristics illustrate the TIPL755 very fast switching speed that was obtained by use of the Base Driver Section.



VERTICAL: 2 A/cm
HORIZONTAL: 10 μs/cm
V_{IN} = 96 V_{rms}
V_{CC} = 237 V dc
LOAD = 100% ALL OUTPUTS

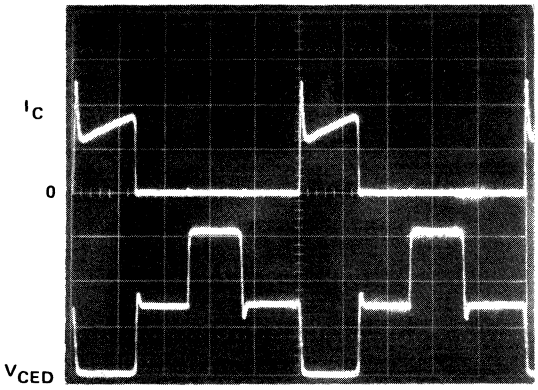


VERTICAL: 2 A/cm
HORIZONTAL: 10 μs/cm
V_{IN} = 120 V_{rms}
V_{CC} = 304 V dc
LOAD = 100% ALL OUTPUTS



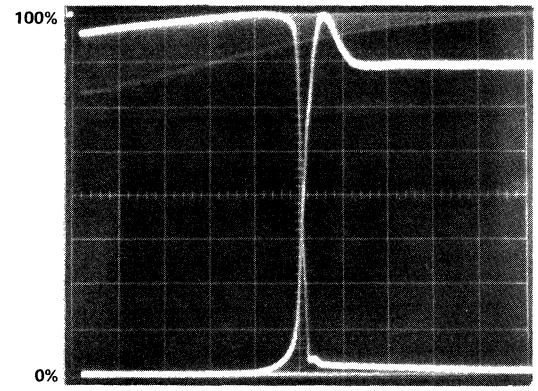
VERTICAL: 2 A/cm
HORIZONTAL: 10 μs/cm
V_{IN} = 132 V_{rms}
V_{CC} = 335 V dc
LOAD = 100% ALL OUTPUTS

Figure 24. Power Transformer Primary Current



VERTICAL: I_C = 2 A/cm
V_{CE} = 100 V/cm
HORIZONTAL: 10 μs/cm
V_{IN} = 132 V_{rms}
V_{CC} = 335 V dc
LOAD = 20 A/5 V

Figure 25. TIPL755 Power Transistor Switching Characteristics



VERTICAL: I_C = 100%
V_{CE} = 100%
HORIZONTAL: 1 μs/cm
V_{IN} = 132 V_{rms}
V_{CC} = 335 V dc
LOAD= 20 A/5 V

Figure 26. TIPL755 Power Transistor t_{xo} Switching Characteristics

Measurements of the overall power supply efficiency were made at various input voltages, while load conditions were changed from 50% to 100% full load, at each input voltage. An efficiency of 65 to 67% was measured, see Table 3.

In conclusion, the measurement results that were obtained proved the power supply described in this report did meet or exceed all of the requirements of the Power Supply Specification.

Figure 27 shows the power supply as constructed for this report.

Table 3. Power Supply Efficiency and Power Factor

V_{IN} (V_{rms})	I_{IN} (A_{rms})	P_{IN} (W)	POWER FACTOR $\frac{P_{IN}}{V_{IN} \times I_{IN}}$	POWER OUTPUTS						% EFFICIENCY $\eta = \frac{P_1 + P_2 + P_3}{P_{IN}}$
				$V_o = 5$ V		$V_o = 10$ V		$V_o = 26$ V		
				I_o (A)	P_1 (W)	I_o (A)	P_2 (W)	I_o (A)	P_3 (W)	
100	9.49	721	0.759	80	400	3	30	2	52	67
99.2	5.78	419	0.731	40	200	3	30	2	52	67
112.8	8.9	738	0.735	80	400	3	30	2	52	65
113.9	5.3	426	0.704	40	200	3	30	2	52	66
132	7.46	733	0.744	80	400	3	30	2	52	66
132	4.67	435	0.705	40	200	3	30	2	52	65

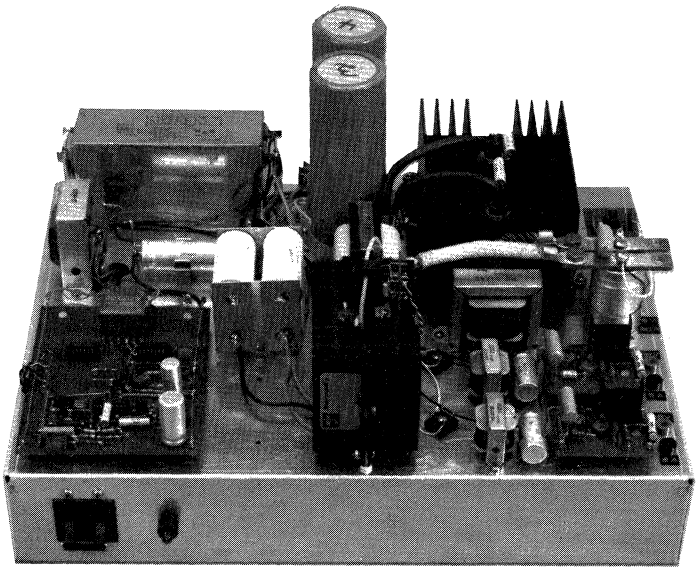


Figure 27. The 500-W, 80-A, Off-the-Line, Half-Bridge Converter Switching Power Supply

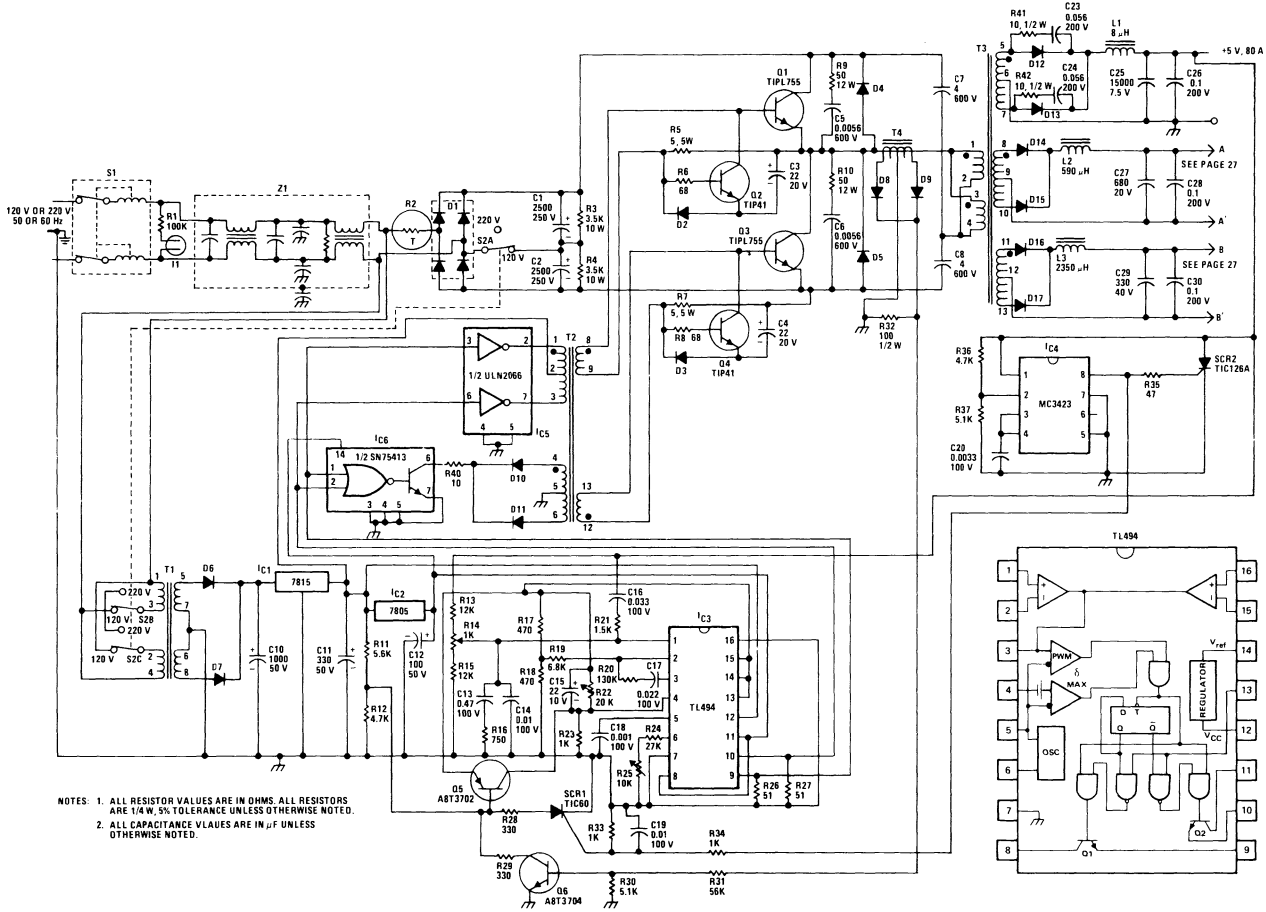


Figure 28. 500-W, 80-A Switching Power Supply

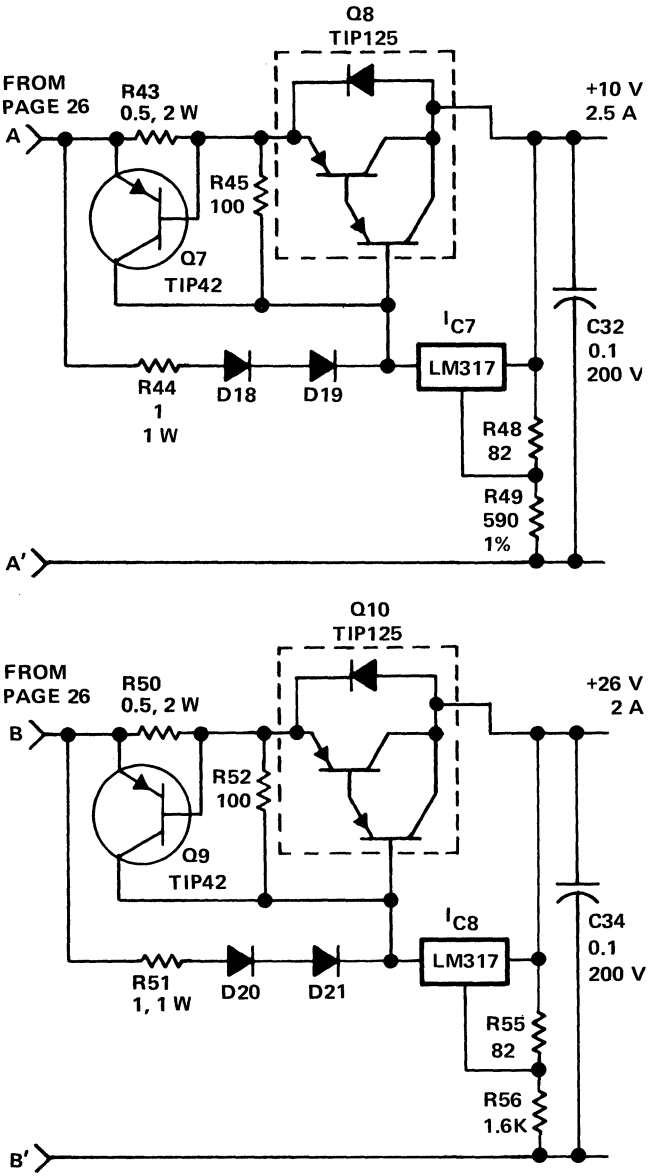


Figure 29. Linear Post Regulators

Acknowledgment

The authors wish to thank Ira N. Frost of the Texas Instruments Linear Applications Lab for his most valuable assistance in this project.

Acknowledgement of important technical information received from Texas Instruments DRC engineers, Carl B. Jones and John H. Vincent, is also given with our appreciation.

References

1. John Spencer, *Designing Switching Voltage Regulators with TL494*, A Texas Instruments Application Report, Bulletin CA-198.

2. Peter Wilson, *The TL494/5 Switching Regulator*, A Texas Instruments Application Report, Bulletin B209.

3. *Switching Power Supply Design Student Guide*, Texas Instruments Incorporated, Semiconductor Group Regional Technology Center.

Parts List

QTY.	CIRCUIT DESIGNATOR	DESCRIPTION
2	C1, C2	2500-μF, 250-V Electrolytic Capacitor, Sprague 36DX252F250BF2A
2	C3, C4	25-μF, 25-V Electrolytic Capacitor, Sprague 500D
2	C5,C6	0.0056-μF, 600-V Polypropylene Capacitor, Sprague 715P56296JA3
2	C7, C8	4-μF, 400-V Polypropylene Capacitor (made up of 2 each 2-μF Sprague 735P205X9400UTL in parallel)
1	C10	1000-μF, 50-V Electrolytic Capacitor, Sprague 674D108H050HL5A
1	C11	270-μF, 50-V Electrolytic Capacitor, Sprague 674D277H050HE5A
1	C12	100-μF, 50-V Electrolytic Capacitor, Sprague 672D107H050DT5C
1	C13	0.47-μF, 100-V Mylar Capacitor, Sprague 225P
2	C14, C19	0.01-μF, 200-V Mylar Capacitor, Sprague
1	C15	25-μF, 12-V Electrolytic Capacitor, Sprague 500D
1	C16	0.033-μF, 100-V Mylar Capacitor, Sprague 225P
1	C17	0.022-μF, 100-V Mylar Capacitor, Sprague 225P
1	C18	0.001-μF, 200-V Mylar Capacitor, Sprague 192P
1	C20	0.0033-μF, 100-V Mylar Capacitor, Sprague 225P
2	C23, C24	0.056-μF, 200-V Polypropylene Capacitor, Sprague 715P56392K
1	C25	15,000-μF, 715-V Electrolytic Capacitor, Sprague 674D159H7R5JT5A
5	C26, C28, C30, C32, C34	0.1-μF, 200-V Polypropylene Capacitor, Sprague 715P10402L
1	C27	680-μF, 20-V Electrolytic Capacitor, Sprague 672D687H020ET5C
1	C29	330-μF, 40-V Electrolytic Capacitor, Sprague 672D337H040ET5C
1	D1	25-A, 600-V Bridge Rectifier, Varo VT600S
12	D2, D3, D6, D7, D8, D9, D10, D11, D18, D19, D20, D21	1N4001 Diode
2	D4, D5	4-A, 600-V Fast-Recovery Diode, TRW DSR5600X
2	D12, D13	75-A, 45-V Power Schottky Diode, TRW SD75
2	D14, D15	10-A, 200-V Fast-Recovery Diode, Varo VH248X
1	IC1	15-V, 1.5-A Positive Voltage Regulator, TI uA7815C

PARTS LIST (continued)

QTY.	CIRCUIT DESIGNATOR	DESCRIPTION
1	IC2	5-V, 1.5-A Positive Voltage Regulator, TI uA7805C
1	IC3	Pulsewidth Modulator Control Circuit, TI TL494CN
1	IC4	Overvoltage-Sensing Circuit, TI MC3423CP
1	IC5	High-Current Darlington Switch, TI ULN2066B
1	IC6	Peripheral OR Driver, TI SN75413
2	IC7, IC8	1.5-A, 3-Terminal Adjustable Regulator, TI LM317
1	L1	Output Inductor, 8-μH, 100-A, Pulse Engineering PE50742
1	L2	Output Inductor, 590-μH, 4-A, Pulse Engineering PE50731
1	L3	Output Inductor, 2350-μH, 2-A, Pulse Engineering PE50732
1	T1	60-Hz Auxiliary Transformer, Triad-Utrad F-211Z
1	T2	20-kHz Base Drive Transformer, Pulse Engineering PE62129
1	T3	20-kHz Switching Transformer, Pulse Engineering PE63202
1	T4	Current Sense Inductor, Pulse Engineering PE51719
1	Z1	Line Filter, 220-V, 10-A, Pulse Engineering PE622A10
1	R1	100-kΩ Resistor, 1/4 W, 5%
1	R2	Thermistor, 2.5 Ω (cold), 0.045 Ω (hot), 10-A, 5%, Rodan-Surge-Guard SG-7
2	R3, R4	3.5 kΩ Resistor, 10 W, 5%
2	R5, R7	5-Ω Resistor, 5 W, 5%
2	R6, R8	68-Ω Resistor, 1/4 W, 5%
2	R9, R10	50-Ω, Resistor, 12 W, 5%
1	R11	5.6-kΩ Resistor, 1/4 W, 5%
2	R12, R36	4.7-kΩ Resistor, 1/4 W, 5%
2	R13, R15	12-kΩ Resistor, 1/4 W, 5%
1	R14	Potentiometer, 1 kΩ
1	R16	750-Ω Resistor, 1/4 W, 5%
2	R17, R18	470-Ω Resistor, 1/4 W, 5%
1	R19	6.8-kΩ Resistor, 1/4 W, 5%
1	R20	130-kΩ Resistor, 1/4 W, 5%
1	R21	1.5-kΩ Resistor, 1/4 W, 5%
1	R22	Potentiometer, 20 kΩ
5	R23, R33, R34, R47, R54	1-kΩ Resistor, 1/4, 5%
1	R24	27-kΩ Resistor, 1/4 W, 5%

PARTS LIST (continued)

QTY.	CIRCUIT DESIGNATOR	DESCRIPTION
1	R25	Potentiometer, 10 kΩ
2	R26, R27	51-Ω Resistor, 1/4 W, 5%
2	R28, R29	330-Ω Resistor, 1/4 W, 5%
2	R30, R37	6.1-kΩ Resistor, 1/4 W, 5%
1	R31	56-kΩ Resistor, 1/2 W, 5%
1	R32	100-Ω Resistor, 1/4 W, 5%
1	R35	47-Ω Resistor, 1/4 W, 5%
1	R40	10-Ω Resistor, 1/4 W, 5%
2	R41, R42	10-Ω Resistor, 1/2 W, 5%
1	R43, R50	0.5-Ω Resistor, 2 W, 5%
2	R44, R51	1-Ω Resistor, 1 W, 5%
2	R45, R52	100-Ω Resistor, 1/4 W, 5%
2	R48, R55	82-Ω Resistor, 1/4 W, 5%
1	R49	590-Ω Resistor, 1/4 W, 1%
1	R56	1.6-kΩ Resistor, 1/4 W, 5%
2	Q1, Q3	10-A, 800-V, NPN Fast-Switching Transistor, TIPL755
2	Q2, Q4	6-A, 40-V, NPN Transistor, TIP41
1	Q5	0.2-A, 40-V, PNP Transistor, A8T3702 or MPS3702
1	Q6	0.8-A, 50-V, NPN Transistor, A8T3704 or MPS3704
2	Q7, Q9	6-A, 40-V, PNP Transistor, TIP42
2	Q8, Q10	5-A, 60-V, PNP Darlington Transistor, TIP125
1	SCR1	Sensitive-Gate Thyristor, 2N5060
1	SCR2	12-A, 100-V Thyristor, TIC126A
1	HS1	Schottky Rectifier Heat Sink, Thermalloy 6423B
1	HS2	Power Transistor Heat Sink, Thermalloy 6123B
1	HS3	Clip-On Heat Sink, Linear Regulators, Thermalloy THM 6038B
1	HS4	Power Transistor Heat Sink, Thermalloy THM 6025
1	I1	Indicator Light
1	S1	Klixon 15-A Circuit Breaker, TI MC8-122-15
1	S2	Triple-Pole, Double-Throw Switch

General Information 1

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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: TL 317M JG /883B

Prefix

MUST CONTAIN TWO OR THREE LETTERS

TL . . . . . TI Linear Products

STANDARD SECOND-SOURCE PREFIXES

LT . . . . . Linear Technology
LTC . . . . Linear Technology
LM . . . . . National
MC . . . . . Motorola
SG . . . . . Silicon General
uA . . . . . Fairchild/National
UC . . . . . Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN THREE OR MORE CHARACTERS
(From Individual Data Sheets)

Examples: 317M 79L15A
497A 79L12AC
79M24

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DW, FN, J, JG, KA, KC, KJ, KK, KV, L, LD, LP, N, P, U
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

OMIT/883B WHEN NOT APPLICABLE

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

Small Outline (D, DW)
Dual-In-Line (J, JG, N, P)
—Slide Magazines
—A-Channel Plastic Tubing
—Sectioned Cardboard Box
—Individual Cardboard Box

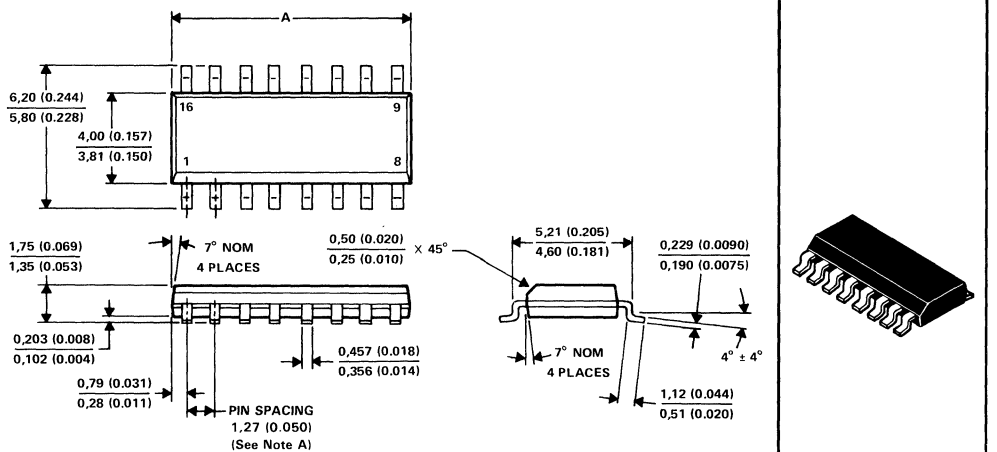
Power Tab (KA, KC, KJ, KK, KV)
—Sleeves
Chip Carriers (FN)
—Anti-Static Plastic Tubing
Flat (U)
—Milton Ross Carrier

Plug-In (L, LD, LP)
—Sectional Cardboard Box
—Individual Cardboard Box

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)



DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

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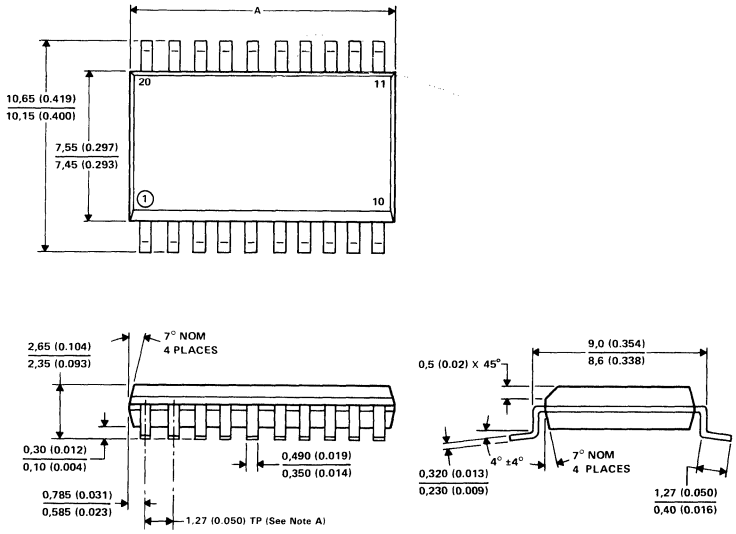
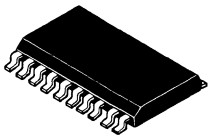
DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

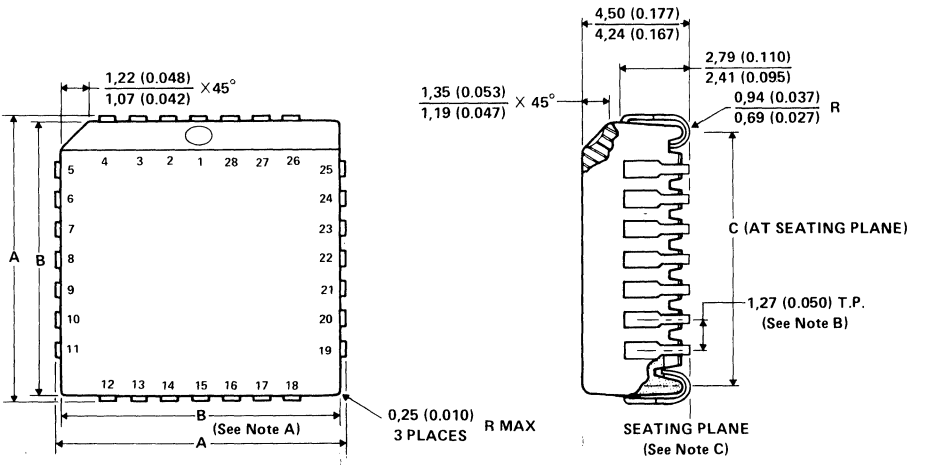
†The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

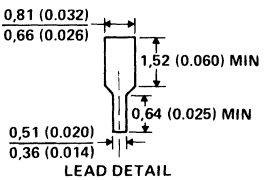
FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN068, and FN084
(28-terminal package used for illustration)



NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

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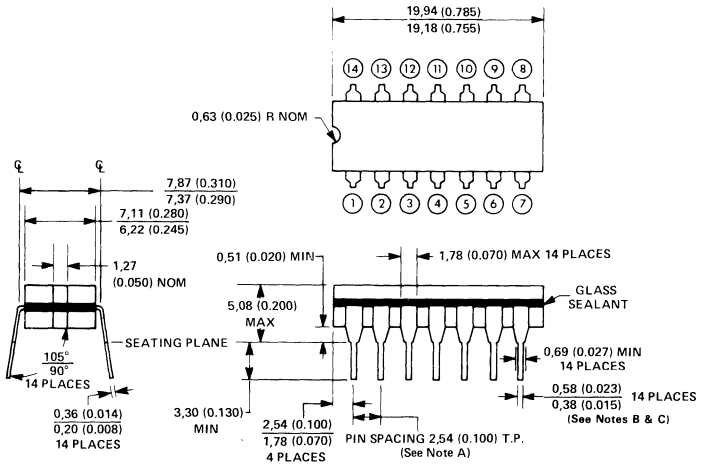
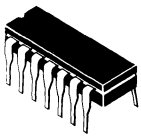
J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

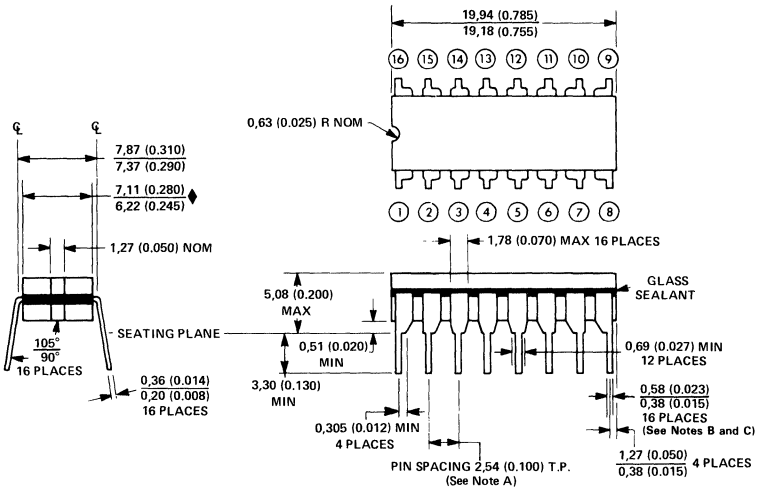
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

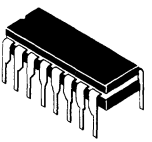
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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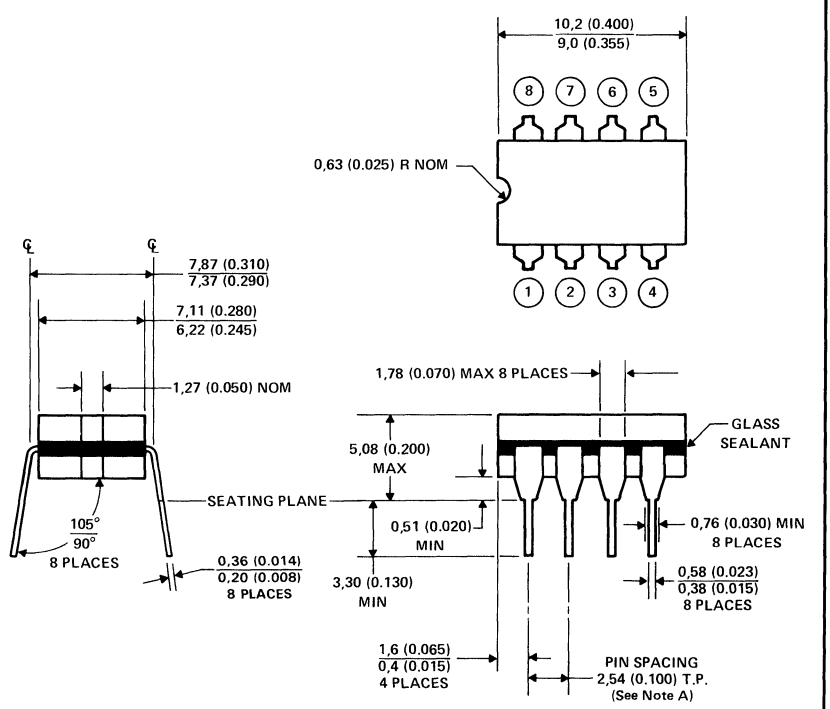
JG008 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-pin lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

JG008



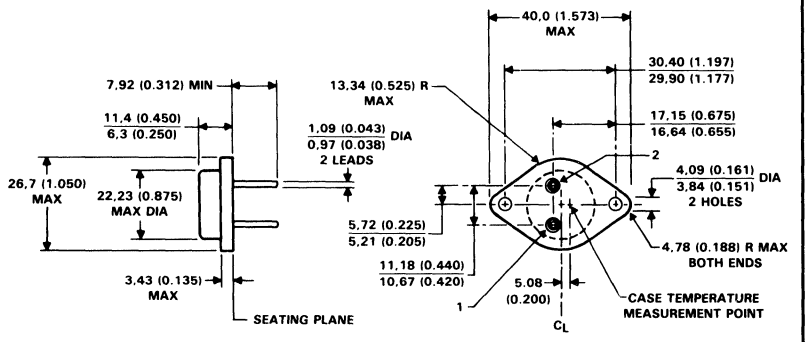
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

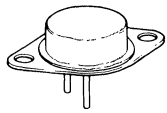
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

KA003 metal flange-mount package

This hermetically sealed package comprises a base of steel and a can of nickel material. The leads are tin-plated Alloy 52 with solder-dip finish. Leads require no additional cleaning or processing when used in soldered assembly.

KA003





ALL JEDEC TO-3 DIMENSIONS AND NOTES ARE APPLICABLE

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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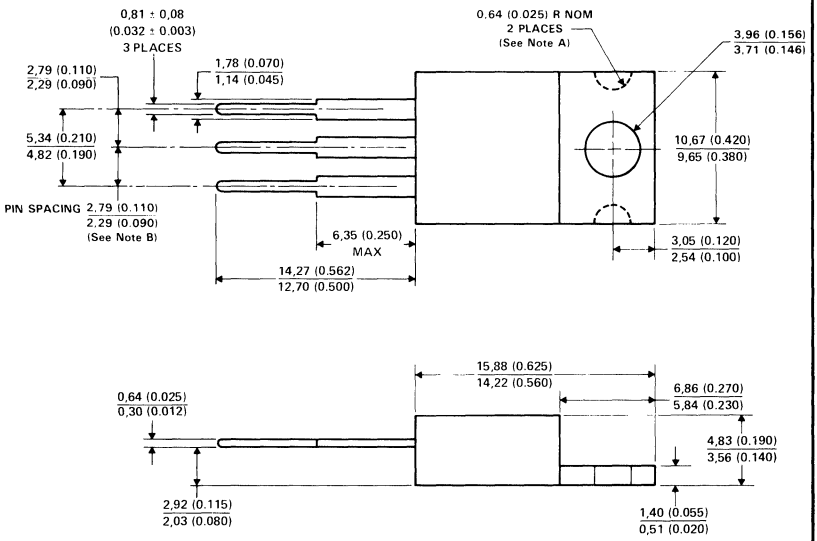
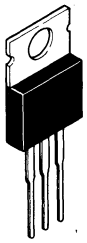
KC003 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC003





THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-220AB DIMENSIONS

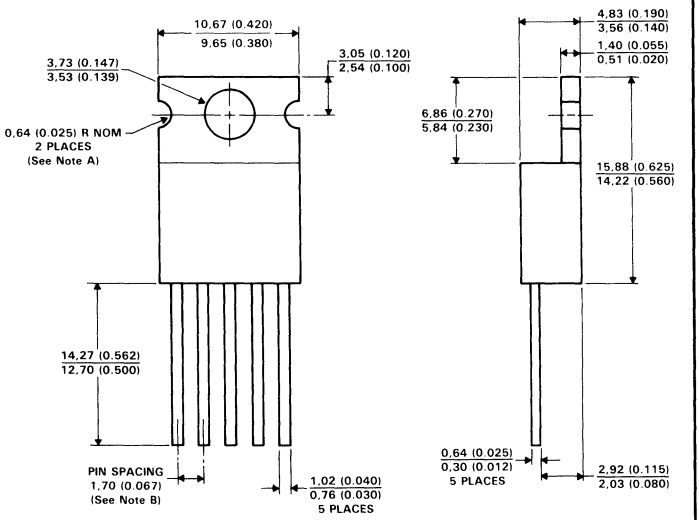
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

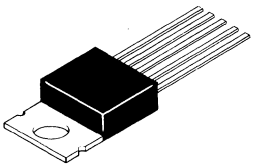
NOTES: A. Notches may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condtions.

KC005 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC005





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Notches may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

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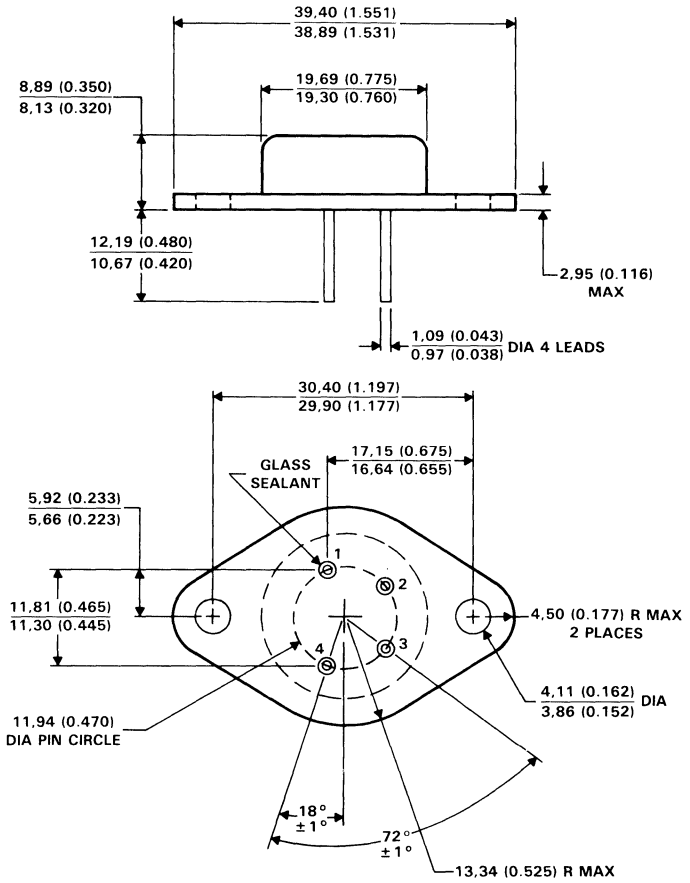
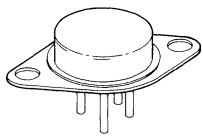
KJ004 metal flange-mount package

This hermetically sealed package consists of a base and can of nickel-plated steel. The leads are nickel-plated Alloy 52 with solder-dip finish.

KJ004



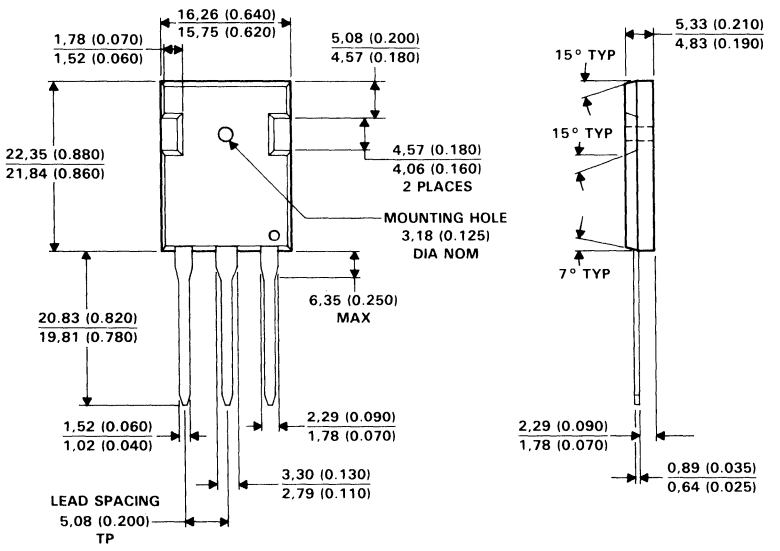


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

KK003 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions:

KK003



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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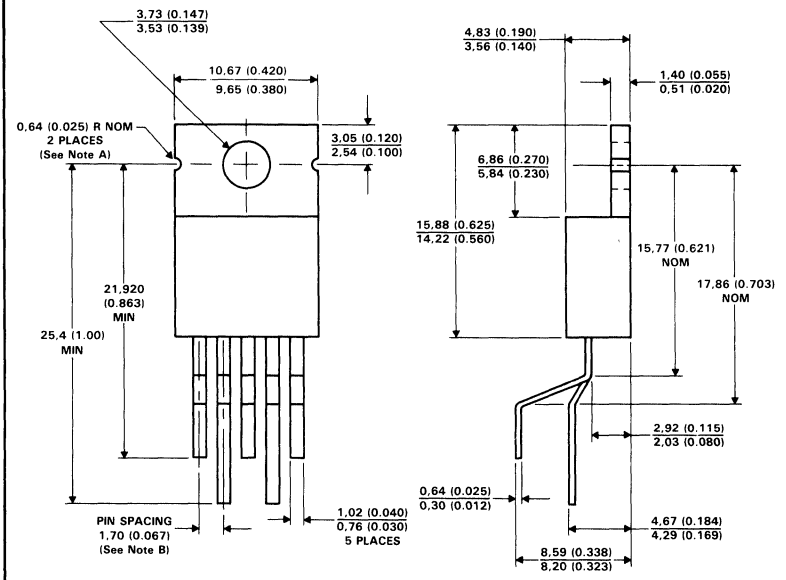
KV005 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KV005



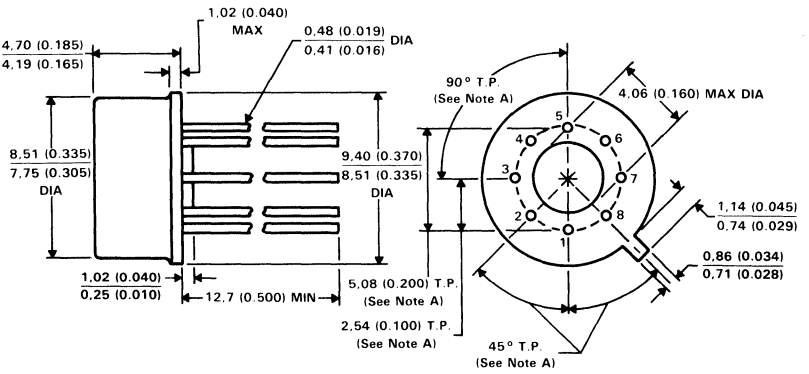
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Notches may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

L008 metal cylindrical package

This hermetically sealed cylindrical package consists of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (—00) require no additional cleaning or processing when used in soldered assembly.

L008



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

NOTE A: Each lead is located within 0,18 (0.007) of its true position at maximum material condition.

TEXAS INSTRUMENTS
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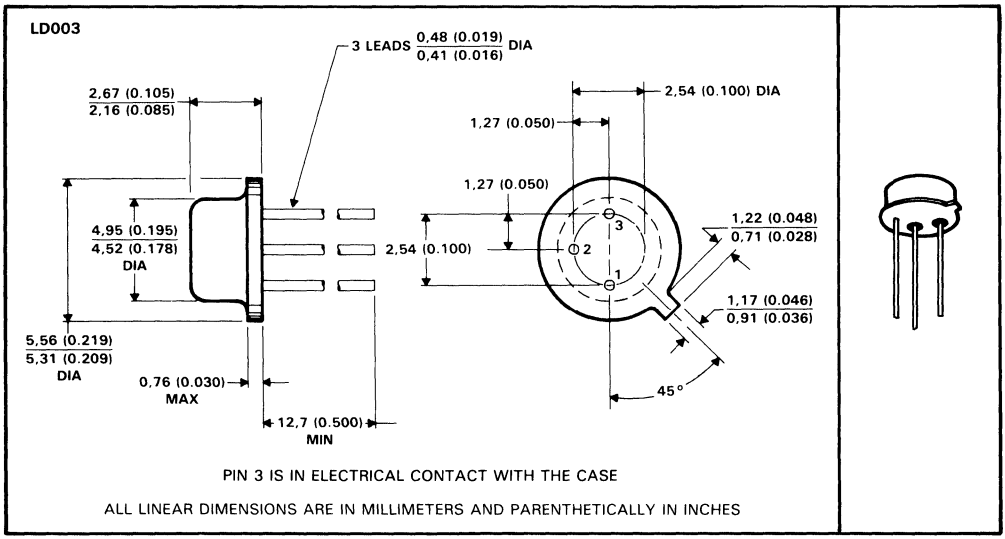
LD003 metal cylindrical package

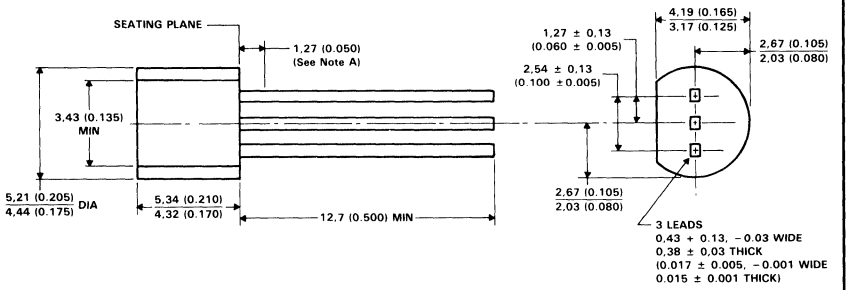
This hermetically sealed cylindrical package consists of a welded metal base and can with individual leads secured by an insulating glass sealant. The gold-plated leads (−00) require no additional cleaning or processing when used in soldered assembly.



LP003 cylindrical plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LP003



Falls Within JEDEC TO-226AA Dimensions
(TO-226AA Replaces TO-92)
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

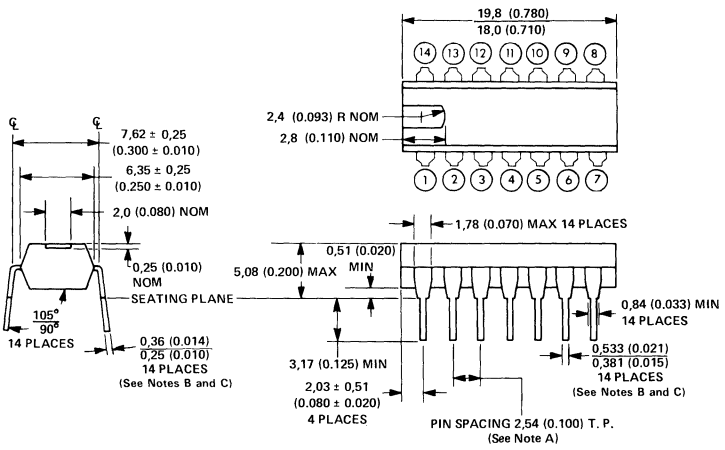
NOTE A: Lead dimensions are not controlled within this area.

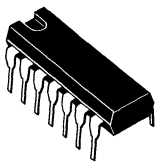
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

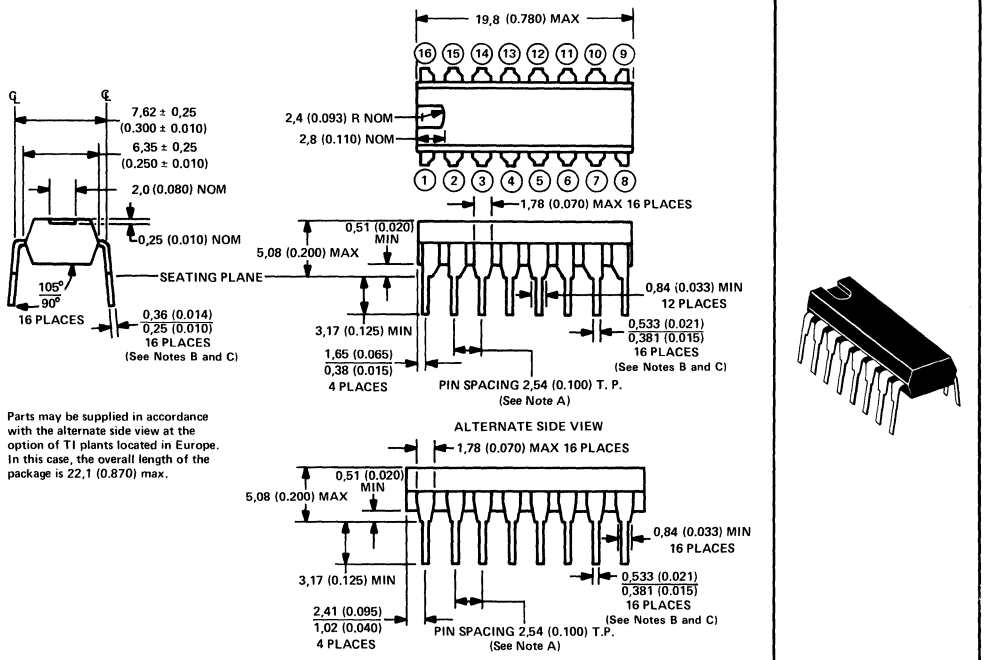
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

TEXAS INSTRUMENTS
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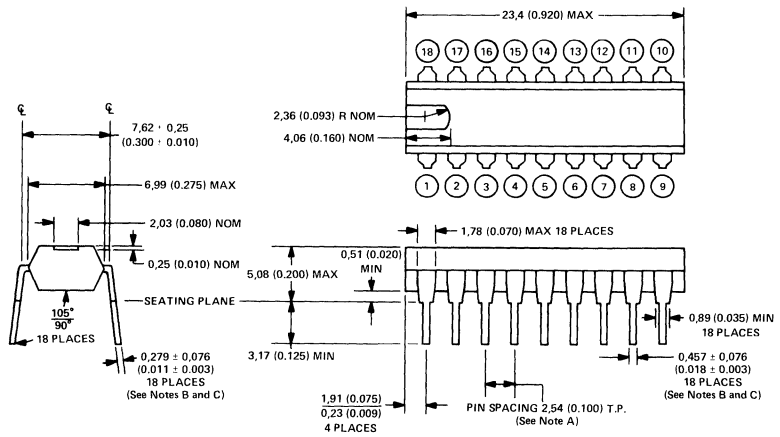
N018 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N018



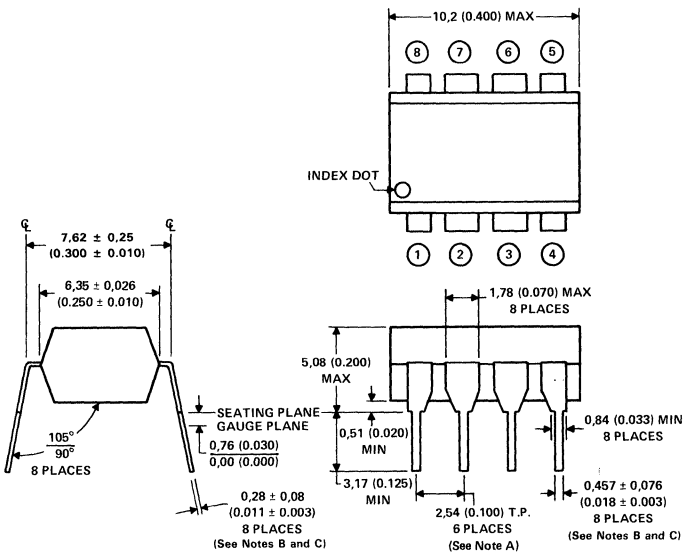
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008 dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

P008

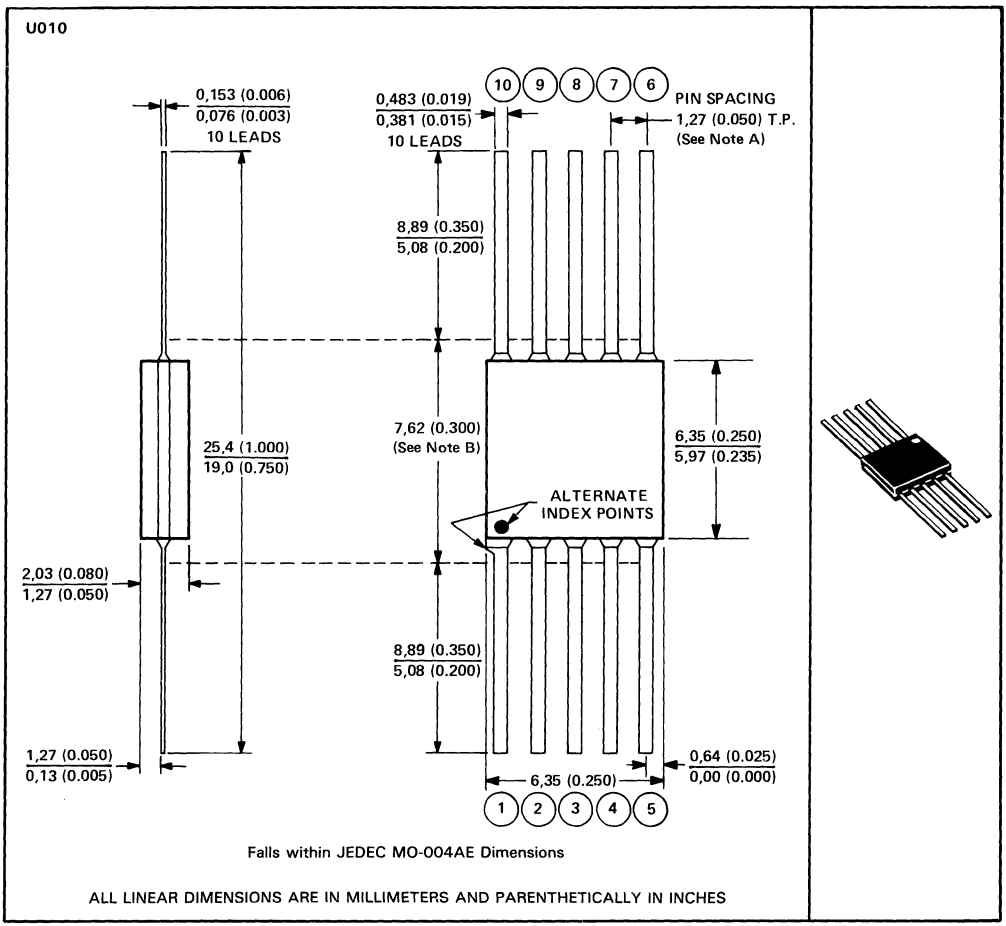


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

U010 ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

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JAPAN: Tokyo Marketing/Sales (Headquarters): Texas Instruments Japan Ltd., MS Shibaura Bldg., 9F, 4-13-23 Shibaura, Minato-ku, Tokyo 108, Japan, 03-769-8700. Texas Instruments Japan Ltd.: Nissho-Iwai Bldg. 5F, 30 Imabashi 3-chome, Higashi-ku, Osaka 541, Japan, 06-294-1881; Daini Toyota West Bldg. 7F, 10-27 Meieki 4-chome, Nakamura-ku, Nagoya 450, 052-583-8691; Daiichi Seimei Bldg. 6F, 3-10 Oyama-cho, Kanazawa 920, Ishikawa-ken, 0762-23-5471; Daiichi Olympic Tachikawa Bldg. 6F, 1-25-12 Akebono-cho, Tachikawa 190, Tokyo, 0425-27-6426; Matsumoto Showa Bldg. 6F, 2-11 Fukashi 1-chome, Matsumoto 390, Nagano-ken, 0263-33-1060; Yokohama Nishiguchi KN Bldg. 6F, 2-8-4 Kita-Saiwai-cho, Nishi-ku, Yokohama 220, 045-322-6741; Nihon Seimei Kyoto Yasaka Bldg. 5F, 843-2 Higashi Shiokohjidori, Nishinotoh-in Higashi-iru, Shiokouji, Shimogyo-ku, Kyoto 600, 075-341-7713; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki 873, Oita-ken, 09786-3-3211; Miho Plant, 2350 Kihara Miho-mura, Inashiki-gun 300-04, Ibaragi-ken, 0298-85-2541.

KOREA: Texas Instruments Korea Ltd., 28th Fl., Trade Tower, #159, Samsung-Dong, Kangnam-ku, Seoul, Korea 2 + 551-2810.

MEXICO: Texas Instruments de Mexico S.A.: Alfonso Reyes—115, Col. Hipodromo Condesa, Mexico, D.F., Mexico 06120, 525/525-3860.

MIDDLE EAST: Texas Instruments: No. 13, 1st Floor Mannai Bldg., Diplomatic Area, P.O. Box 26335, Manama Bahrain, Arabian Gulf, 973 + 274681.

NETHERLANDS: Texas Instruments Holland B.V., 19 Hogehilweg, 1100 AZ Amsterdam—Zuidoost, Holland 20 + 5602911.

NORWAY: Texas Instruments Norway A/S: PB106, Refstad 0585, Oslo 5, Norway, (2) 155090.

PEOPLES REPUBLIC OF CHINA: Texas Instruments China Inc., Beijing Representative Office, 7-05 Citic Bldg., 19 Jianguomenwai Dajie, Beijing, China, (861) 5002255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd.: 14th Floor, Ba- Lepanto Bldg., Paseo de Roxas, Makati, Metro Manila, Philippines, 817-60-31.

PORTUGAL: Texas Instruments Equipamento Electronico (Portugal), Lda.: Rua Eng. Frederico Ulrich, 2650 Moreira Da Maia, 4470 Maia, Portugal, 2-948-1003.

SINGAPORE (+ INDIA, INDONESIA, MALAYSIA, THAILAND): Texas Instruments Singapore (PTE) Ltd., Asia Pacific Division, 101 Thompson Rd. #23-01, United Square, Singapore 1130, 350-8100.

SPAIN: Texas Instruments Espana, S.A.: C/Jose Lazaro Galdiano No. 6, Madrid 28036, 1/458.14.58.

SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen): S-164-93, Stockholm, Sweden, 8 - 752-5800.

SWITZERLAND: Texas Instruments, Inc., Reidstrasse 6, CH-8953 Dietikon (Zuerich) Switzerland, 1-740 2220.

TAIWAN: Texas Instruments Supply Co., 9th Floor Bank Tower, 205 Tun Hwa N. Rd., Taipei, Taiwan, Republic of China, 2 + 713-9311.

UNITED KINGDOM: Texas Instruments Limited: Manton Lane, Bedford, MK41 7PA, England, 0234 270111.

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