Data Book

Optoelectronics and Image Sensors

1990

TEXAS INSTRUMENTS

Optoelectronics and Image Sensors

CCD Sensors, Optocouplers, IR Emitters, Intelligent Displays, and Phototransistors

Data Book

1990

Linear Products

Linear Products Data Book Guide

Data Book	Contents	Document No.
● Linear Circuits Vol 1 Amplifiers, Comparators, and Special Functions	Operational Amplifiers Voltage Comparators Video Amplifiers Hall-Effect Devices Timers and Current Mirrors Magnetic-Memory Interface Frequency-to-Voltage Converters Sonar Ranging Circuits/Modules Sound Generators	SLYD003 1989
● Linear Circuits Vol 2 Data Acquisition and Conversion	A/D and D/A Converters DSP Analog Interface Analog Switches and Multiplexers Switched-Capacitor Filters	SLYD004 1989
● Linear Circuits Vol 3 Voltage Regulators and Supervisors	Supervisor Functions Series-Pass Voltage Regulators Shunt Regulators Voltage References DC-to-DC Converters PWM Controllers	SLYD005 1989
● Telecommunications Circuits	Equipment Line Interfaces Subscriber Line Interfaces Modems and Receivers/Transmitters Ringers, Detectors, Tone Encoders PCM Interface Transient Suppressors	SCTD001A 1988/89
● Optoelectronics and Image Sensors	Optocouplers CCD Image Sensors and Support Phototransistors IR-Emitting Diodes Hybrid Displays	SOYD002A 1990
● Interface Circuits	High-Voltage (Display) Drivers High-Power (Peripheral/Motor) Drivers Line Drivers, Receivers, Transceivers EIA RS-232, RS-422, RS-423, RS-485 IBM 360/370, IEEE 802.3, CCITT Military Memory Interface	SLYD002 1987
● Speech System Manuals	TSP50C4X Family	SPSS010 1990

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Information contained in this data book supersede all data for this technology published by TI in the United States before January 1990.

INTRODUCTION

This data book presents the three major categories of Optoelectronic and Image Sensing devices that Texas Instruments now offers to the Military, Computer, Industrial, and Consumer electronics markets. These categories are:

- CCD Linear Image Sensors
- Optocouplers/Optoisolators
- Intelligent LED Displays

The CCD Image Sensor product line offers a range of linear sensors from an organization of 128 × 1 to 3456 × 1. The product family utilizes TI's patented Virtual Phase technology to minimize the number of clock electrodes required by the imager, resulting in simpler external circuitry requirements and improved performance.

The Optocoupler/Optoisolator devices are offered in metal-can and plastic dual-in-line (P-DIP) packages, JEDEC-registered metal cans provide transistor output functions. All of TI's Optocoupler/Optoisolator P-DIPs are UL recognized and provide functions such as logic gates, triac, and transistor/Darlington outputs.

The Intelligent red LED Displays are plastic-encapsulated dual-in-line packages that contain TTL-compatible on-board electronics to decode input signals and provide constant current to each LED.

This data book also contains information on hermetically sealed standard Pill package Infrared Emitters and Phototransistors.

A selection guide, located in Section 1, lists the important electrical parameters and features. The glossary describes the symbols, abbreviations, terms, and definitions. Included is a cross-reference table listing other manufacturers with the direct or nearest replacement devices. The contents provides easy location of major information in the general information, quality and reliability, and applications sections. The alphanumeric index lists page numbers for all the device types. The detailed data sheets complete the salient features of the data book.

While this volume offers design and specification data only for Optoelectronic and Image Sensing components, complete technical information for all TI semiconductor products are available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that you will discover this new *1990 Optoelectronics and Image Sensor Data Book* to be a significant addition to your collection of technical literature.

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linear arrays

TYPE	PIXELS	PIXEL SIZE	SENSITIVITY	PACKAGE	PAGE NO.
TC102†	128 × 1	12.7 μm × 12.7 μm	3.5 V/μJ/cm^2	10-pin CDIP (0.300 in)	2-5
TC102-1‡	128 × 1	12.7 μm × 12.7 μm	3.5 V/μJ/cm^2	10-pin CDIP (0.300 in)	2-17
TC103†	2048 × 1	12.7 μm × 12.7 μm	3.5 V/μJ/cm^2	24-pin CDIP (0.600 in)	2-29
TC103-1‡	2048 × 1	12.7 μm × 12.7 μm	3.5 V/μJ/cm^2	24-pin CDIP (0.600 in)	2-41
TC104†	3456 × 1	10.7 μm × 10.7 μm	2.0 V/μJ/cm^2	24-pin CDIP (0.600 in)	2-53
TC104-1‡	3456 × 1	10.7 μm × 10.7 μm	2.0 V/μJ/cm^2	24-pin CDIP (0.600 in)	2-65
TC106-1‡	2592 × 1	10.7 μm × 10.7 μm	2.0 V/μJ/cm^2	24-pin CDIP (0.600 in)	2-77

† Minimum and typical values of Write Reference (WR) and End of Scan (EOS) are specified.
‡ Typical values of WR and EOS are specified.

evaluation boards

PART NO.	DEVICE EVALUATED	REMARKS	PAGE NO.
PC401	TC103, TC103-1, TC104, TC104-1 and TC106-1	Device socket fits TC103, TC103-1, TC104, TC104-1, and TC106-1 (See TCK Evaluation Kits below)	7-59
PC402	TC102 and TC102-1	Device socket fits TC102 and TC102-1 (See TCK102 below)	

evaluation kits

PART NO.	CONTENTS	REMARKS	PAGE NO.
TCK102	TC102 plus PC402	See Application section "Operating Instructions for Linear CCD Image Sensors"	7-59
TCK103	TC103 plus PC401	See Application section "Operating Instructions for Linear CCD Image Sensors"	
TCK104	TC104 plus PC401	See Application section "Operating Instructions for Linear CCD Image Sensors"	
TCK106-1	TC106-1 plus PC401	See Application section "Operating Instructions for Linear CCD Image Sensors"	

recommended support functions for linear image sensors

TYPE	DESCRIPTION	SUPPLY VOLTAGE, V_{CC}		ANALOG INPUT VOLTAGE, ANLG IN		FEATURES	PAGE NO.
		MIN(V)	MAX(V)	MIN(V)	MAX(V)		
TL1591	Sample and hold	4.75	5.5		0.8	Bandwidth 25 MHz Typ — Sample Rate 15 MHz Max	2-89
TLD369	Dual clock driver	4.75	22	—	—	Can switch negative voltage with respect to V_{DD}	2-93

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

optocouplers, 6-pin plastic DIP and metal can

TYPE	ISOLATION VOLTAGE (kV) f = 60 Hz		MINIMUM CTR (%)	FEATURES	PAGE NO.
	PEAK	RMS			
3N261	1.0	–	50		
3N262	1.0	–	100 (500 max)	JEDEC, Metal Can	3-3
3N263	1.0	–	200 (1000 max)		
4N22†	1.0	–	25		
4N23†	1.0	–	60	JEDEC, Metal Can	3-9
4N24†	1.0	–	100		
4N22A†	1.0	–	25		
4N23A†	1.0	–	60	JEDEC, Isolated Metal Can	3-13
4N24A†	1.0	–	100		
4N25‡	2.5	–	20		
4N26	1.5	–	20	JEDEC, Plastic DIP, UL File E-65085	3-19
4N27	1.5	–	10		
4N28	0.5	–	10		
4N35‡	3.54	2.5	100		
4N36	2.5	1.75	100	JEDEC, Plastic DIP, UL File E-65085	3-21
4N37	1.5	1.05	100		
4N47§	1.0	–	50		
4N48§	1.0	–	100 (500 max)	JEDEC, Metal Can	3-25
4N49§	1.0	–	200 (1000 max)		
MCT2	1.5	–	20	Plastic DIP, UL File E-65085	3-109
MCT2E	3.54	2.5	20		
TIL102	1.0	–	25	Metal Can	3-133
TIL103	1.0	–	100		
TIL111	1.5	–	13		3-137
TIL113	1.5	–	300		3-143
TIL114	2.5	–	13		3-137
TIL116	2.5	–	20	Plastic DIP, UL File E-65085	3-137
TIL117	2.5	–	50		3-137
TIL118	1.5	–	10		3-147
TIL119A	1.5	–	300	TIL119A has no base connection.	3-143
TIL120	1.0	–	25	Metal Can	3-151
TIL121	1.0	–	50		
TIL124	5.0	–	10	High Voltage, Plastic DIP, UL File E-65085	3-155
TIL125	5.0	–	20		
TIL126	5.0	–	50		
TIL127	5.0	–	300	High-Voltage Darlington, Plastic DIP UL File E-65085 TIL128A has no base connection.	3-161
TIL128A	5.0	–	300		

†JAN, JANTX, JANTXV levels to MIL-S-19500/486A USAF are also available.
‡Available in PEP3 processing also.
§JAN, JANTX, JANTXV levels to MIL-S-19500/548 are also available.

optocouplers, 6-pin plastic DIP and metal can (continued)

TYPE	ISOLATION VOLTAGE (kV) f = 60 Hz		MINIMUM CTR (%)	FEATURES	PAGE NO.
	PEAK	RMS			
TIL153 TIL154 TIL155	3.54	2.5	10 20 50	High Voltage, Plastic DIP, UL File E-65085	3-165
TIL156 TIL157A	3.54	2.5	300 300	High-voltage, Darlington, Plastic DIP, UL File E-65085 TIL157A has no base connection.	3-171
TIL181	3.54	2.5	50	Plastic DIP, UL File E-65085	3-175
TIL186-1 TIL186-2 TIL186-3 TIL186-4	3.54	2.5	10 20 50 (I_F = 10 mA) 300	AC Input Darlington, Plastic DIP, UL File E-65085	3-179
TIL187-1 TIL187-2 TIL187-3 TIL187-4	3.54	2.5	250 500 1000 (I_F = 2 mA) 1500	AC Input Darlington, Plastic DIP, UL File E-65085	3-185
TIL188-1 TIL188-2 TIL188-3 TIL188-4	3.54	2.5	250 500 1000 (I_F = 2 mA) 1500	Same as TIL189 except TIL190 has no base lead connection for high-EMI environment. UL File E-65085.	3-185
TIL189-1 TIL189-2 TIL189-3 TIL189-4	3.54	2.5	250 500 1000 (I_F = 2 mA) 1500	High-Voltage, Plastic DIP, UL File E-65085	3-191
TIL190-1 TIL190-2 TIL190-3 TIL190-4	3.54	2.5	250 500 1000 (I_F = 2 mA) 1500	Same as TIL189 except TIL190 has no base lead connection for high-EMI environment. UL File E-65085.	3-191
TIL191 TIL191A TIL191B	3.54	2.5	20 50 (I_F = 5 mA) 100	Single Channel 4-pin DIP UL File 65085	3-197
TIL192 TIL192A TIL192B	3.54	2.5	20 50 (I_F = 5 mA) 100	Dual Channel 8-pin DIP UL File 65085	3-197
TIL193 TIL193A TIL193B	3.54	2.5	20 50 (I_F = 5 mA) 100	Quad Channel 16-pin DIP UL File 65085	3-197
TIL194 TIL194A TIL194B	3.54	2.5	20 50 (I_F = 5 mA) 100	AC Input, Single Channel 4-pin DIP UL File E-65085	3-203
TIL195 TIL195A TIL195B	3.54	2.5	20 50 (I_F = 5 mA) 100	AC Input, Single Channel 8-pin DIP UL File E-65085	3-203
TIL196 TIL196A TIL196B	3.54	2.5	20 50 (I_F = 5 mA) 100	AC Input, Single Channel 16-pin DIP UL File E-65085	3-203

optocouplers, 8-pin plastic DIP, high-speed (T_A = 25°C unless otherwise noted)

TYPE	CTR (MIN) V_O = 0.4 V, I_F = 16 mA	V_{OL} (MAX) I_F = 16 mA T_A = 0°C to 70°C	V_F (MAX) I_F = 16 mA	SWITCHING TIMES (MAX) I_F = 16 mA t_{PLH} OR t_{PHL}	ISOLATION VOLTAGE (MIN)	PAGE NO.
6N135†	7%	0.4 V (I_O = 1.1 mA)	1.7 V	1.5 μs (R_L = 4.1 kΩ)	3 kV dc	3-33
6N136†	19%	0.4 V (I_O = 2.4 mA)	1.7 V	0.8 μs (R_L = 1.9 kΩ)	3 kV dc	3-33
HCPL2502	15%	0.4 V (I_O = 2.4 mA)	1.7 V	0.8 μs (R_L = 1.9 kΩ)	3 kV dc	3-59
HCPL2530	7%	0.4 V (I_O = 2.4 mA)	1.7 V	1.5 μs (R_L = 4.1 kΩ)	3 kV dc	3-67
HCPL2531	19%	0.4 V (I_O = 2.4 mA)	1.7 V	0.8 μs (R_L = 1.9 kΩ)	3 kV dc	3-67
HCPL4502	19%	0.4 V (I_O = 2.4 mA)	1.7 V	0.8 μs (R_L = 1.9 kΩ)	3 kV dc	3-33

optocouplers, 8-pin plastic DIP, high-speed logic gate (T_A = 25°C unless otherwise noted)

TYPE	V_{OL} (MAX) I_F = 5 mA, I_{OL} = 13 mA T_A = 0°C to 70°C	V_F (MAX) I_F = 10 mA	SWITCHING TIMES (MAX) I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF		ISOLATION VOLTAGE (MIN)	PAGE NO.
			t_{PLH}	t_{PHL}		
6N137†	0.6 V	1.75 V	75 ns	75 ns	3 kV dc	3-41
HCPL2601	0.6 V	1.75 V	75 ns	75 ns	3 kV dc	3-75
HCPL2630‡	0.6 V	1.75 V	75 ns	75 ns	3 kV dc	3-83
HCPL2631‡	0.6 V	1.75 V	75 ns	75 ns	3 kV dc	3-91

optocouplers, 8-pin plastic DIP, high-speed, high-gain (T_A = 25°C unless otherwise noted)

TYPE	CTR (MIN) V_O = 0.4 V I_F = 1.6 mA, T_A = 0°C to 70°C	V_{OL} (MAX) I_F = 1.6 mA T_A = 0°C to 70°C	V_F (MAX) I_F = 1.6 mA	SWITCHING TIMES (MAX) I_F = 1.6 mA		ISOLATION VOLTAGE (MIN)	PAGE NO.
				t_{PLH}	t_{PHL}		
6N138†	300%	0.4 V (I_O = 4.8 mA)	1.7 V	35 μs, R_L = 2.2 kΩ	10 μs, R_L = 2.2 kΩ	3 kV dc	3-49
6N139†	500%	0.4 V (I_O = 6.4 mA)	1.7 V	60 μs, R_L = 4.7 kΩ	25 μs, R_L = 4.7 kΩ	3 kV dc	3-49
HCPL2730	300%	0.4 V (I_O = 4.8 mA)	1.7 V	35 μs, R_L = 2.2 kΩ	20 μs, R_L = 2.2 kΩ	3 kV dc	3-99
HCPL2731	500%	0.4 V (I_O = 6.4 mA)	1.7 V	35 μs, R_L = 2.2 kΩ	20 μs, R_L = 2.2 kΩ	3 kV dc	3-99

optocouplers, 6-pin plastic DIP TRIAC driver (T_A = 25°C unless otherwise noted)

TYPE	I_{FT} (MAX) V_{TM} = 3 V	V_F (MAX) I_F = 10 mA	V_{TM} (MAX) I_{TM} = 100 mA	I_{DRM} (MAX) RATED V_{DRM}	dv/dt (TYP)	ISOLATION VOLTAGE (MIN)	PAGE NO.
MOC3009	30 mA	1.5 V	3 V	100 nA	12 V/μs	7.5 kV dc	3-113
MOC3010	15 mA	1.5 V	3 V	100 nA	12 V/μs	7.5 kV dc	
MOC3011	10 mA	1.5 V	3 V	100 nA	12 V/μs	7.5 kV dc	
MOC3012	5 mA	1.5 V	3 V	100 nA	12 V/μs	7.5 kV dc	
MOC3020	30 mA	1.5 V	3 V	100 nA	100 V/μs	7.5 kV dc	3-119
MOC3021	15 mA	1.5 V	3 V	100 nA	100 V/μs	7.5 kV dc	
MOC3022	10 mA	1.5 V	3 V	100 nA	100 V/μs	7.5 kV dc	
MOC3023	5 mA	1.5 V	3 V	100 nA	100 V/μs	7.5 kV dc	

†JEDEC registered
‡Dual channel

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optocouplers, 6-pin plastic DIP TRIAC driver (T_A = 25°C unless otherwise noted)

TYPE	I_{FT} (MAX) V_{TM} = 3 V	V_F (MAX) I_F = 10 mA	V_{TM} (MAX) I_{TM} = 100 mA	I_{DRM} (MAX) RATED V_{DRM}	dv/dt (TYP)	ISOLATION VOLTAGE (MIN)	PAGE NO.
TIL3009	30 mA	1.5 V	3 V	100 nA	12 V/μs	3.5 kV dc	3-207
TIL3010	15 mA	1.5 V	3 V	100 nA	12 V/μs	3.5 kV dc	
TIL3011	10 mA	1.5 V	3 V	100 nA	12 V/μs	3.5 kV dc	
TIL3012	5 mA	1.5 V	3 V	100 nA	12 V/μs	3.5 kV dc	
TIL3020	30 mA	1.5 V	3 V	100 nA	100 V/μs	3.5 kV dc	3-213
TIL3021	15 mA	1.5 V	3 V	100 nA	100 V/μs	3.5 kV dc	
TIL3022	10 mA	1.5 V	3 V	100 nA	100 V/μs	3.5 kV dc	
TIL3023	5 mA	1.5 V	3 V	100 nA	100 V/μs	3.5 kV dc	

optocouplers, 6-pin plastic DIP, Schmitt trigger (T_A = 25°C unless otherwise noted)

TYPE	LOGIC FUNCTION	OUTPUT CONFIGURATION	I_{FT+} (MAX)	HYSTERESIS RATIO (TYP)	SWITCHING TIMES (MAX)		ISOLATION VOLTAGE (MIN)	PAGE NO.
					t_r OR t_f	t_{PLH} OR t_{PHL}		
OPI8012	Buffer	Totem pole	10 mA	1.4	70 ns	5 μs	3.54 kV dc	3-125
OPI8013	Buffer	Open collector	10 mA	1.4	70 ns	5 μs	3.54 kV dc	
OPI8014	Inverter	Totem pole	10 mA	1.4	70 ns	5 μs	3.54 kV dc	
OPI8015	Inverter	Open collector	10 mA	1.4	70 ns	5 μs	3.54 kV dc	

hybrid displays

TYPE	TYPE OF CHARACTER(S)	CHARACTER HEIGHT mm (inches)	COLOR OF DISPLAY	PACKAGE	REMARKS	PAGE NO.
TIL302	7-segment	6,9 (0.270)	Red	14-lead dual-in-line plastic	Left decimal	4-3
TIL302A					Left decimal	
TIL303					Right decimal	
TIL303A					Right decimal	
TIL304	Polarity and overflow unit	6,9 (0.270)	Red	14-lead dual-in-line plastic	Right decimal	4-3
TIL304A					Right decimal	
TIL305	5 × 7 alphanumeric	7,6 (0.300)	Red	14-lead dual-in-line plastic	Left decimal	4-9
TIL306	7-segment	6,9 (0.270)	Red	16-lead dual-in-line plastic	Left decimal	4-11
TIL306A					Left decimal	
TIL307					Right decimal	
TIL307A					Right decimal	
TIL308					Left decimal	4-17
TIL308A					Left decimal	
TIL309					Right decimal	
TIL309A					Right decimal	
TIL311	Hexadecimal	7,6 (0.300)	Red	14-lead dual-in-line plastic	Logic includes latch, decoder, and driver.	4-23
TIL311A					TL311 and TL311A — left and right decimals	

infrared-emitting diodes

TYPE	POWER OUTPUT		Φ_{HI}	V_F (MAX) I_F = 50 mA	λ_P (TYP) (nm)	FEATURES	PAGE NO.
	P_O (MIN) (mW)	I_F (mA)					
TIL23	0.4	50	35°	1.5 V	940	Pill package for mounting on double-sided printed circuit boards. Compatible with TIL601 Series.	5-7
TIL24	1.0	50	35°	1.5 V	940		
TIL25	0.75	50	35°	1.5 V	940		
TIL24HR2	1.0	50	35°	1.5 V	940		5-11

phototransistors

TYPE	LIGHT CURRENT V_{CE} = 5 V		DARK CURRENT (MAX) V_{CE} = 30 V	POWER DISSIPATION	FEATURES	PAGE NO.
	MIN	MAX				
IN5722	0.5 mA	3 mA	25 nA	50 mW	EIA-registered versions of TIL601 thru TIL604	5-3
IN5723	2 mA	5 mA	25 nA	50 mW		
IN5724	4 mA	8 mA	25 nA	50 mW		
IN5725	7 mA		25 nA	50 mW		
LS600	0.8 mA	—	25 nA	50 mW	Pill package designed for mounting on double-sided printed board. Compatible with TIL23 series.	5-25
LS602	0.5 mA	—	25 nA	50 mW		
LS611	0.5 mA	2 mA	25 nA	50 mW		
LS612	1 mA	3 mA	25 nA	50 mW		
LS613	2 mA	4 mA	25 nA	50 mW		
LS614	3 mA	5 mA	25 nA	50 mW		
LS615	4 mA	6 mA	25 nA	50 mW		
LS616	5 mA	7 mA	25 nA	50 mW		
LS617	6 mA	8 mA	25 nA	50 mW		
LS618	7 mA	9 mA	25 nA	50 mW		
LS619	8 mA	—	25 nA	50 mW		
TIL601	0.5 mA	3 mA	25 nA	50 mW		5-25
TIL602	2 mA	5 mA	25 nA	50 mW		
TIL603	4 mA	8 mA	25 nA	50 mW		
TIL604	7 mA		25 nA	50 mW		
TIL604HR2	7 mA		25 nA	50 mW		5-33

sensor-emitter arrays

TYPE	FUNCTION	POWER OUTPUT MIN I_F = 50 mA	V_F MAX I_F = 50 mA	I_L MIN V_{CE} = 5 V	I_C I_F = 50 mA V_{CE} = 5 V	$V_{CE(sat)}$ TYP I_C = 2 mA I_F = 50 mA	FEATURES	PAGE NO.
TIL131	Nine-element gallium arsenide IRED array	0.4 mW	1.5 V				Nine TIL23s mounted on pc board for paper tape readers	5-13
TIL132	Nine-element phototransistor array			2 mA			Nine LS600s mounted on pc board for paper tape readers	5-13
TIL133	Nine-channel IRED-photo-transistor pair				2.5 mA to 10 mA	0.4 V	Consists of a TIL131 and TIL132 with specified channel performance	5-13
TIL134	Twelve-element gallium arsenide IRED array	0.4 mW	1.5 V				Twelve TIL23s mounted on 6,4-mm (0.250-in) centers. For reading punched cards	5-19
TIL135	Twelve-element phototransistor array			2 mA			Twelve L600s mounted on 6,4-mm (0.250-in) centers in double-sided pc board	5-19
TIL136	Twelve-channel IRED-photo-transistor pair				2.5 mA to 10 mA	0.4 V	Consists of a TIL134 and TIL135 with specified channel performance	5-19

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages from the use of the information contained herein.

DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
3N243	JEDEC Registered (Industry common)	TIL120	B
3N244	JEDEC Registered (Industry common)	TIL120	B
3N245	JEDEC Registered (Industry common)	TIL120	B
4N22	JEDEC Registered (Industry common)	4N22	A
4N22A	JEDEC Registered (Industry common)	4N22	A
4N23	JEDEC Registered (Industry common)	4N23	A
4N23A	JEDEC Registered (Industry common)	4N23	A
4N24	JEDEC Registered (Industry common)	4N24	A
4N24A	JEDEC Registered (Industry common)	4N24	A
4N25	JEDEC Registered (Industry common)	4N25	A
4N25A	JEDEC Registered (Industry common)	TIL154	A
4N26	JEDEC Registered (Industry common)	4N26	A
4N27	JEDEC Registered (Industry common)	4N27	A
4N28	JEDEC Registered (Industry common)	4N28	A
4N29A	JEDEC Registered (Industry common)	TIL156	A
4N30	JEDEC Registered (Industry common)	TIL113	A
4N31	JEDEC Registered (Industry common)	TIL119	A
4N33	JEDEC Registered (Industry common)	TIL113	A
4N34	JEDEC Registered (Industry common)	TIL113	A
4N35	JEDEC Registered (Industry common)	4N35	A
4N36	JEDEC Registered (Industry common)	4N36	A
4N37	JEDEC Registered (Industry common)	4N37	A
4N47	JEDEC Registered (Industry common)	4N47	A
4N48	JEDEC Registered (Industry common)	4N48	A
4N49	JEDEC Registered (Industry common)	4N49	A
6N135	Hewlett Packard	6N135	A
6N136	Hewlett Packard	6N136	A
6N137	Hewlett Packard	6N137	A
6N138	Hewlett Packard	6N138	A
6N139	Hewlett Packard	6N139	A
6N140A	Hewlett Packard	6N140A	A
5082-7100	Hewlett Packard	TIL305	B
5082-7101	Hewlett Packard	TIL305	B
5082-7300	Hewlett Packard	TIL309	B
5082-7300	Hewlett Packard	TIL307	B
5082-7302	Hewlett Packard	TIL308	B
5082-7302	Hewlett Packard	TIL306	B
5082-7340	Hewlett Packard	TIL311	B
BPX621	Siemens	TIL602	B
BPX6211	Siemens	TIL602	B
BPX62111	Siemens	TIL603	B
CL12	Clairex	TIL118	B

A = TI Direct Replacement
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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
CL13	Clairex	4N37	B
CL15	Clairex	TIL116	B
CL16	Clairex	TIL117	B
CL17	Clairex	TIL118	B
CL18	Clairex	TIL116	B
CL19	Clairex	TIL116	B
CL112	Clairex	TIL157	B
CL1506	Clairex	TIL118	B
CL1510	Clairex	4N37	B
CL1511	Clairex	4N37	B
CL10506A	Clairex	TIL116	B
CLT3160	Clairex	TIL602	B
CLT3170	Clairex	TIL604	B
CNX35	Quality Technologies Corp.	TIL126	A
CNX36	Quality Technologies Corp.	4N35	A
CNY17-1	General Electric	TIL126	B
CNY17-2	General Electric	TIL126	B
CNY17-3	General Electric	TIL127	B
CNY17-4	General Electric	TIL128	B
CNY18-2	Siemens	TIL120	B
CNY18-3	Siemens	TIL121	B
CNY35	General Electric	TIL186-1	A
CNY47	General Electric	TIL116	A
CNY47A	General Electric	TIL117	A
CQY80	General Electric	4N35	A
DL1A	Siemens	TIL302	B
DL10	Siemens	TIL302	B
DL10A	Siemens	TIL302	B
DL57	Siemens	TIL305	B
DL101	Siemens	TIL304	B
DL101A	Siemens	TIL304	B
GE3009	General Electric	TIL3009	A
GE3010	General Electric	TIL3010	A
GE3011	General Electric	TIL3011	A
GE3012	General Electric	TIL3012	A
GE3020	General Electric	TIL3020	A
GE3021	General Electric	TIL3021	A
GE3022	General Electric	TIL3022	A
GE3023	General Electric	TIL3023	A
GEPS2001	General Electric	TIL117	A
H11A1	General Electric	TIL117	A
H11A1	Motorola	TIL117	A
H11A2	General Electric	TIL112	A
H11A2	Motorola	4N26	A
H11A3	General Electric	TIL114	B
H11A3	General Electric	TIL114	A
H11A3	General Electric	TIL115	B
H11A3	General Electric	TIL116	A
H11A3	General Electric	TIL116	A

A = TI Direct Replacement
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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
H11A3	Motorola	4N25	A
H11A4	General Electric	TIL111	A
H11A4	Motorola	4N27	A
H11A5	General Electric	TIL118	B
H11A5	General Electric	TIL116	A
H11A5	Motorola	TIL117	A
H11A10	General Electric	4N27	A
H11A520	General Electric	TIL125	A
H11A520	General Electric	TIL124/TIL154	B
H11A550	General Electric	TIL126	A
H11A590	General Electric	TIL126	A
H11A590	General Electric	TIL126/TIL155	B
H11A5100	General Electric	4N35	A
H11AA1	General Electric	TIL186-2	A
H11AA1	Motorola	TIL186-1	A
H11AA2	General Electric	TIL186-1	A
H11AA2	Motorola	TIL186-2	A
H11AA3	General Electric	TIL186-3	A
H11AA3	Motorola	TIL186-3	A
H11AA4	General Electric	TIL186-4	A
H11AA4	Motorola	TIL186-4	A
H11B1	General Electric	TIL189-2	A
H11B1	General Electric	TIL113	B
H11B1	General Electric	TIL187	B
H11B1	General Electric	TIL188	B
H11B2	General Electric	TIL119	B
H11B2	General Electric	TIL113	A
H11B3	General Electric	TIL119	A
H11B255	General Electric	TIL189-1	A
H11BX522	General Electric	TIL189-3	A
H11G2	General Electric	TIL156	B
H11J1	General Electric	TIL3011	A
H11J2	General Electric	TIL3010	A
H11J3	General Electric	TIL3011	A
H11J4	General Electric	TIL3010	A
H11J5	General Electric	TIL3010	A
H11L1	General Electric	OPI8015	A
H11L2	General Electric	OPI8015	A
HCPL2502	Hewlett Packard	HCPL2502	A
HCPL2530	Hewlett Packard	HCPL2530	A
HCPL2531	Hewlett Packard	HCPL2531	A
HCPL2601	Hewlett Packard	HCPL2601	A
HCPL2630	Hewlett Packard	HCPL2630	A
HCPL2631	Hewlett Packard	HCPL2631	A
HCPL2730	Hewlett Packard	HCPL2730	A
HCPL2731	Hewlett Packard	HCPL2731	A
HCPL4502	Hewlett Packard	HCPL4502	A
IL-1	Siemens	TIL125	A
IL-5	Siemens	TIL117	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
IL-12	Siemens	TIL111	B
IL-15	Siemens	TIL112	A
IL-16	Siemens	TIL118	B
IL-30	Siemens	TIL113	B
IL-74	Siemens	TIL111	A
IL-94	Siemens	TIL153	B
IL-101	Siemens	HCPL2601	A
IL-203	Siemens	TIL127	B
IL-250	Siemens	TIL186-3	A
IL-251	Siemens	TIL186-2	A
IL-252	Siemens	TIL186-4	A
IL-501	Siemens	TIL126	A
IL-505	Siemens	4N35	A
IL-512	Siemens	TIL125	A
ILA-30	Siemens	TIL113	A
ILA-55	Siemens	TIL189-1	A
ILCA2-30	Siemens	TIL113	A
ILCA2-55	Siemens	TIL189-1	A
JAN4N22	Micropac	JAN4N22	A
JAN4N22A	Micropac	JAN4N22A	A
JAN4N22A	Optek/Optron	JAN4N22A	A
JAN4N23	Micropac	JAN4N23	A
JAN4N23A	Micropac	JAN4N23A	A
JAN4N23A	Optek/Optron	JAN4N23A	A
JAN4N24	Micropac	JAN4N24	A
JAN4N24A	Micropac	JAN4N24A	A
JAN4N24A	Optek/Optron	JAN4N24A	A
JAN4N47	Micropac	JAN4N47	A
JAN4N48	Micropac	JAN4N48	A
JAN4N49	Micropac	JAN4N49	A
JANTX4N22	Micropac	JANTX4N22	A
JANTX4N22A	Micropac	JANTX4N22A	A
JANTX4N22A	Optek/Optron	JANTX4N22A	A
JANTX4N23	Micropac	JANTX4N23	A
JANTX4N23A	Micropac	JANTX4N23A	A
JANTX4N23A	Optek/Optron	JANTX4N23A	A
JANTX4N24	Micropac	JANTX4N24	A
JANTX4N24A	Micropac	JANTX4N24A	A
JANTX4N24A	Optek/Optron	JANTX4N24A	A
JANTX4N47	Micropac	JANTX4N47	A
JANTX4N48	Micropac	JANTX4N48	A
JANTX4N49	Micropac	JANTX4N49	A
JANTXV4N22	Micropac	JANTXV4N22	A
JANTXV4N22A	Micropac	JANTXV4N22A	A
JANTXV4N22A	Optek/Optron	JANTXV4N22A	A
JANTXV4N23	Micropac	JANTXV4N23	A
JANTXV4N23A	Micropac	JANTXV4N23A	A
JANTXV4N23A	Optek/Optron	JANTXV4N23A	A
JANTXV4N24	Micropac	JANTXV4N24	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
JANTXV4N24A	Micropac	JANTXV4N24A	A
JANTXV4N24A	Optek/Optron	JANTXV4N24A	A
JANTXV4N47	Micropac	JANTXV4N47	A
JANTXV4N48	Micropac	JANTXV4N48	A
JANTXV4N49	Micropac	JANTXV4N49	A
L15AX601	General Electric	TIL601	A
L15AX604	General Electric	TIL604	A
MAN1A	Quality Technologies Corp.	TIL302	A
MAN2A	Quality Technologies Corp.	TIL305	A
MAN10A	Quality Technologies Corp.	TIL302	A
MAN101A	Quality Technologies Corp.	TIL304	A
MAN1001A	Quality Technologies Corp.	TIL304	A
MCA230	Quality Technologies Corp.	TIL156	A
MCA231	Quality Technologies Corp.	TIL156	A
MCA255	Quality Technologies Corp.	TIL189-1	A
MCA2230	Quality Technologies Corp.	TIL127	A
MCA2231	Quality Technologies Corp.	TIL189-2	A
MCA2255	Quality Technologies Corp.	TIL189-2	A
MCC670	Quality Technologies Corp.	6N138	A
MCC671	Quality Technologies Corp.	6N139	A
MCL2502	Quality Technologies Corp.	HCPL2502	A
MCL2530	Quality Technologies Corp.	HCPL2530	A
MCL2531	Quality Technologies Corp.	HCPL2531	A
MCL2601	Quality Technologies Corp.	HCPL2601	A
MCL2630	Quality Technologies Corp.	HCPL2630	A
MCL2631	Quality Technologies Corp.	HCPL2631	A
MCP3009	Quality Technologies Corp.	MOC3009	A
MCP3010	Quality Technologies Corp.	MOC3010	A
MCP3011	Quality Technologies Corp.	MOC3011	A
MCP3012	Quality Technologies Corp.	MOC3012	A
MCP3020	Quality Technologies Corp.	MOC3020	A
MCP3021	Quality Technologies Corp.	MOC3021	A
MCP3022	Quality Technologies Corp.	MOC3022	A
MCP3023	Quality Technologies Corp.	MOC3023	A
MCT2	Quality Technologies Corp.	MCT2	A
MCT2E	Quality Technologies Corp.	MCT2E	A
MCT4	Quality Technologies Corp.	TIL120	A
MCT26	Quality Technologies Corp.	TIL111	A
MCT210	Quality Technologies Corp.	TIL126	A
MCT270	Quality Technologies Corp.	TIL125	A
MCT271	Quality Technologies Corp.	TIL117	A
MCT272	Quality Technologies Corp.	4N36	A
MCT273	Quality Technologies Corp.	TIL127	B
MCT274	Quality Technologies Corp.	TIL128	B
MCT275	Quality Technologies Corp.	TIL127	B
MCT276	Quality Technologies Corp.	TIL116	A
MCT277	Quality Technologies Corp.	4N35	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
MCT2201	Quality Technologies Corp.	4N35	A
MCT2202	Quality Technologies Corp.	TIL126	A
MCT5200	Quality Technologies Corp.	4N35	A
MCT5201	Quality Technologies Corp.	4N35	A
MCT5210	Quality Technologies Corp.	4N35	A
MCT5211	Quality Technologies Corp.	4N35	A
MLED910	Motorola	TIL23	A
MOC119	Motorola	TIL128A	A
MOC1000	Motorola	TIL116	A
MOC1000	Motorola	4N26	B
MOC1001	Motorola	4N25	B
MOC1001	Motorola	TIL116	A
MOC1002	Motorola	4N27	B
MOC1002	Motorola	TIL116	A
MOC1003	Motorola	4N28	B
MOC1005	Motorola	TIL125	A
MOC1006	Motorola	TIL124	A
MOC1100	Motorola	TIL113	A
MOC1200	Motorola	TIL113	A
MOC3009	Motorola	MOC3009	A
MOC3010	Motorola	MOC3010	A
MOC3011	Motorola	MOC3011	A
MOC3012	Motorola	MOC3012	A
MOC3020	Motorola	MOC3020	A
MOC3021	Motorola	MOC3021	A
MOC3022	Motorola	MOC3022	A
MOC3023	Motorola	MOC3023	A
MOC5007	Motorola	OPI8015	A
MOC5008	Motorola	OPI8015	A
MOC5009	Motorola	OPI8015	A
MOC8020	Motorola	TIL190-2	A
MOC8021	Motorola	TIL190-3	A
MOC8030	Motorola	TIL190-1	A
MOC8050	Motorola	TIL190-2	A
MOC8080	Motorola	TIL189-2	A
MOC8100	Motorola	TIL126	A
MRD601	Motorola	TIL601	A
MRD602	Motorola	TIL602	A
MRD603	Motorola	TIL603	A
MRD603	Motorola	TIL604	B
MRD604	Motorola	TIL604	A
OP123	Optek/Optron	TIL23	A
OP124	Optek/Optron	TIL24	A
OP600	Optek/Optron	LS600	A
OP601	Optek/Optron	TIL601	A
OP602	Optek/Optron	TIL602	A
OP603	Optek/Optron	TIL603	A
OP604	Optek/Optron	TIL604	A
OP640	Optek/Optron	LS600	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
OP641	Optek/Optron	TIL601	A
OP642	Optek/Optron	TIL602	A
OP643	Optek/Optron	TIL603	A
OPI102	Optek/Optron	TIL102/4N22	A
OPI103	Optek/Optron	TIL103/4N24	A
OPI130	Optek/Optron	4N48	A
OPI140	Optek/Optron	TIL120	B
OPI2100	Optek/Optron	4N35	A
OPI2150	Optek/Optron	TIL112	A
OPI2151	Optek/Optron	4N27	A
OPI2152	Optek/Optron	4N26	A
OPI2153	Optek/Optron	TIL117	A
OPI2154	Optek/Optron	4N37	A
OPI2155	Optek/Optron	4N37	A
OPI2250	Optek/Optron	TIL115	A
OPI2251	Optek/Optron	TIL153	A
OPI2252	Optek/Optron	TIL116	A
OPI2253	Optek/Optron	TIL117	A
OPI2254	Optek/Optron	4N36	A
OPI2255	Optek/Optron	4N36	A
OPI2500	Optek/Optron	TIL186-1	A
OPI2501	Optek/Optron	TIL186-2	A
OPI2502	Optek/Optron	HCPL2502	A
OPI2630	Optek/Optron	HCPL2630	A
OPI3009	Optek/Optron	TIL3009	A
OPI3010	Optek/Optron	TIL3010	A
OPI3011	Optek/Optron	TIL3011	A
OPI3012	Optek/Optron	TIL3012	A
OPI3020	Optek/Optron	TIL3020	A
OPI3021	Optek/Optron	TIL3021	A
OPI3022	Optek/Optron	TIL3022	A
OPI3023	Optek/Optron	TIL3023	A
OPI3150	Optek/Optron	TIL119A	A
OPI3151	Optek/Optron	TIL119A	A
OPI3152	Optek/Optron	TIL189-1	A
OPI3250	Optek/Optron	TIL157A	A
OPI3251	Optek/Optron	TIL157A	A
OPI3252	Optek/Optron	TIL189-1	A
OPI8012	Optek/Optron	OPI8012	A
OPI8013	Optek/Optron	OPI8013	A
OPI8014	Optek/Optron	OPI8014	A
OPI8015	Optek/Optron	OPI8015	A
OPI8137	Optek/Optron	6N137	A
PC110	Sharp	TIL126	A
PC4N25	Sharp	4N25	A
PC4N26	Sharp	4N26	A
PC4N27	Sharp	4N27	A
PC4N28	Sharp	4N28	A
PC4N35	Sharp	4N35	A

A = TI Direct Replacement
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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
PC4N36	Sharp	4N36	A
PC4N37	Sharp	4N37	A
PC613	Sharp	TIL117	A
PC618	Sharp	6N136	A
PC713	Sharp	TIL126	A
PC733	Sharp	TIL186-2	A
PC733H	Sharp	TIL186-2	A
PC810	Sharp	TIL191A	A
PC810A	Sharp	TIL191A	A
PC810B	Sharp	TIL191B	A
PC812	Sharp	TIL191B	A
PC812A	Sharp	TIL191B	A
PC813	Sharp	TIL194	A
PC813A	Sharp	TIL194A	A
PC814	Sharp	TIL194	A
PC814A	Sharp	TIL194A	A
PC815	Sharp	TIL197	A
PC816	Sharp	TIL191A	A
PC816A	Sharp	TIL191B	A
PC816AB	Sharp	TIL191B	A
PC816AC	Sharp	TIL191B	A
PC816AD	Sharp	TIL191B	A
PC817	Sharp	TIL191A	A
PC817T1	Sharp	TIL191B	A
PC818	Sharp	TIL191	A
PC823	Sharp	TIL195	A
PC823A	Sharp	TIL195A	A
PC825	Sharp	TIL198	A
PC826	Sharp	TIL192A	A
PC826A	Sharp	TIL192B	A
PC826AB	Sharp	TIL192B	A
PC826AC	Sharp	TIL192B	A
PC826AD	Sharp	TIL192B	A
PC827	Sharp	TIL192A	A
PC827T1	Sharp	TIL192B	A
PC829	Sharp	TIL913A	A
PC843	Sharp	TIL196	A
PC843A	Sharp	TIL196A	A
PC845	Sharp	TIL199	A
PC846	Sharp	TIL193A	A
PC846A	Sharp	TIL193B	A
PC846AB	Sharp	TIL193B	A
PC846AC	Sharp	TIL193B	A
PC846AD	Sharp	TIL193B	A
PC847	Sharp	TIL193A	A
PC847T1	Sharp	TIL193B	A
PC849	Sharp	TIL914A	A
PC900	Sharp	OPI8015	A
PC901	Sharp	OPI8015	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
PS2001B	NEC	TIL117	A
PS2002B	NEC	TIL157A	A
PS2003B	NEC	TIL117	A
PS2004B	NEC	TIL189-4	A
PS2006B	NEC	6N136	A
PS2006B(1)	NEC	6N135	A
PS2007B	NEC	6N137	A
PS2010-K	NEC	4N36	A
PS2010-L	NEC	TIL117	A
PS2010-M	NEC	TIL116	A
PS2011-L	NEC	4N35	A
PS2011-M	NEC	TIL126	A
PS2012(1)-M	NEC	TIL128	A
PS2012-M	NEC	TIL128A	A
PS2015-N	NEC	TIL125	A
PS2016B	NEC	6N136	A
PS2018-L	NEC	4N35	A
PS2018-M	NEC	TIL126	A
PS2021-L	NEC	4N35	A
PS2021-M	NEC	TIL126	A
PS2031-L	NEC	4N35	A
PS2031-M	NEC	TIL126	A
PS2044	NEC	6N136	A
PS2401A-1R	NEC	TIL191B	A
PS2401A-2R	NEC	TIL192B	A
PS2401A-4R	NEC	TIL193B	A
PS2403-1M	NEC	TIL191B	A
PS2403-2M	NEC	TIL192B	A
PS2403-4M	NEC	TIL193B	A
PS2501-1D	NEC	TIL191B	A
PS2501-2D	NEC	TIL192B	A
PS2501-4D	NEC	TIL193B	A
PS2505-1	NEC	TIL194B	A
PS2505-2	NEC	TIL195B	A
PS2505-4	NEC	TIL196B	A
S11MD5V	Sharp	MOC3022	A
SCD11B2	Honeywell	TIL127	B
SCD11B2	Honeywell	TIL113	B
SCD11B2	Honeywell	TIL157	B
SCD11B2	Honeywell	TIL119	B
SCD11B2	Honeywell	TIL156	B
SCD11B2	Honeywell	TIL128	B
SD2440-1	Honeywell	TIL601	A
SD2440-2	Honeywell	TIL602	A
SD2440-3	Honeywell	TIL603	A
SD2440-4	Honeywell	TIL604	A
SE2450-1	Honeywell	TIL23	A
SE2450-2	Honeywell	TIL23	A
SE2450-3	Honeywell	TIL25	A

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DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
SE2460-1	Honeywell	TIL23	B
SE2460-2	Honeywell	TIL23	B
SE2460-3	Honeywell	TIL24	A
SFH600	Honeywell	TIL117	B
SFH600-0	Honeywell	TIL117	B
SFH601-1	Honeywell	TIL155	B
SPX2E	Honeywell	TIL125	B
SPX2E	Honeywell	TIL124	B
SPX6	Honeywell	TIL126	A
SPX26	Honeywell	TIL153	A
SPX26	Honeywell	TIL118	B
SPX26	Honeywell	TIL115	B
SPX33	Honeywell	TIL154	B
SPX33	Honeywell	TIL153	B
SPX33B2	Honeywell	TIL116	B
SPX33B2	Honeywell	TIL114	B
SPX53	Honeywell	TIL117	B
SPX53	Honeywell	TIL155	A
TLP2530	Toshiba	HCPL2530	A
TLP2531	Toshiba	HCPL2531	A
TLP2601	Toshiba	HCPL2601	A
TLP2630	Toshiba	HCPL2630	A
TLP2631	Toshiba	HCPL2631	A
TLP3009	Toshiba	MOC3009	A
TLP3010	Toshiba	MOC3010	A
TLP3011	Toshiba	MOC3011	A
TLP3012	Toshiba	MOC3012	A
TLP3020	Toshiba	MOC3020	A
TLP3021	Toshiba	MOC3021	A
TLP3022	Toshiba	MOC3022	A
TLP3023	Toshiba	MOC3023	A
TLP504A	Toshiba	TIL192A	A
TLP504A-2	Toshiba	TIL193A	A
TLP504A-2GB	Toshiba	TIL193B	A
TLP504AGB	Toshiba	TIL192B	A
TLP521-1A	Toshiba	TIL191A	A
TLP521-1GB	Toshiba	TIL191B	A
TLP521-2A	Toshiba	TIL192A	A
TLP521-2GB	Toshiba	TIL192B	A
TLP521-4A	Toshiba	TIL193A	A
TLP521-4GB	Toshiba	TIL193B	A
TLP575	Toshiba	TIL157A	A
TLP620	Toshiba	TIL194A	A
TLP620-2	Toshiba	TIL195A	A
TLP620-2GB	Toshiba	TIL195B	A
TLP620-4	Toshiba	TIL196A	A
TLP620-4GB	Toshiba	TIL196B	A
TLP620GB	Toshiba	TIL194B	A
TLP621	Toshiba	TIL191A	A

A = TI Direct Replacement
B = Nearest Replacement

DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
TLP621-2	Toshiba	TIL192A	A
TLP621-2GB	Toshiba	TIL192B	A
TLP621-4	Toshiba	TIL193A	A
TLP621-4GB	Toshiba	TIL193B	A
TLP621GB	Toshiba	TIL191B	A
TLP624	Toshiba	TIL191B	A
TLP624-2	Toshiba	TIL192B	A
TLP624-4	Toshiba	TIL193B	A
TLP626	Toshiba	TIL194B	A
TLP626-2	Toshiba	TIL195B	A
TLP626-4	Toshiba	TIL196B	A
TLP630	Toshiba	TIL186-3	A
TLP630GB	Toshiba	TIL186-4	A
TLP651	Toshiba	6N136	A

A = TI Direct Replacement

DEVICE	MANUFACTURER/SOURCE	TI DEVICE	CODE
RL128G	EG&G Reticon	TC102	B
RL2048	EG&G Reticon	TC103	B
CCD111	Fairchild	TC102	B
CCD142	Fairchild	TC103	B
CCD143	Fairchild	TC103	B

B = Nearest Replacement

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Introduction

This glossary contains letter symbols, abbreviations, terms, and definitions commonly used with optoelectronic devices. Most of the information, excluding the image-sensing concepts, was obtained from JEDEC Standard No. 77.

Index to Glossary by Symbols and Abbreviations

B	Demodulation bandwidth
CCD	Charge-coupled device
CTD	Charge-transfer device
CRT	Cathode-ray tube
CTR	Current transfer ratio
E_e	Irradiance
E_v	Illuminance
f_{mod}	Modulation frequency
H	Irradiance
h_F	Current transfer ratio
$I_{C(off)}$	Off-state collector current
$I_{C(on)}$	On-state collector current
I_D	Dark current
I_e	Radiant intensity
I_F	Forward current
I_L	Light current
I_R	Reverse current
IRED	Infrared-emitting diode
I_v	Luminous intensity
L_e	Radiance
L_v	Luminance
LED	Light-emitting diode
NEP	Noise equivalent power (spectral density)
NTSC	National Television System Committee
P_n	Noise equivalent power (spectral density)
P_O	Radiant flux or power output
Q_e	Radiant energy
Q_v	Luminous energy
R_e	Radiant responsivity
RGB	Red-green-blue (monitor)
R_v	Luminous responsivity
sr	Steradian
t_d	Delay time
t_f	Fall time
t_f	Radiant pulse fall time
t_r	Radiant pulse rise time
t_r	Rise time
t_s	Storage time
V_F	Forward voltage
Δf	Noise equivalent bandwidth
$\Delta\lambda$	Spectral bandwidth
θ_{HI}	Half-intensity beam angle
λp	Wavelength at peak emission
Φe	Radiant flux
Φv	Luminous flux

Units of Measurement

Unit	Symbol	Note
ampere†	A	
angstrom	Å	1 Å = 10^{-10} m = 10^{-4} μm = 0.1 nm
candela†	cd	1 cd = 1 lm/sr
candela/foot^2	cd/ft^2	1 cd/ft^2 = 10.76391 cd/m^2
candela/meter^2†	cd/m^2	
degree Celsius†	°C	
	°K	See K
farad†	F	
foot	ft	1 ft = 0.3048 m (exactly)
footcandle	fc	1 fc = 1 lm/ft^2 = 10.76391 lx
footlambert	fL	1 fL = (1/π) cd/ft^2 = 3.426259 cd/m^2
hertz†	Hz	
inch	in	1 in = 2.54 cm (exactly)
kelvin†	K	Formerly °K, degree Kelvin
lambert	L	1 L = 3183.099 cd/m^2
lumen†	lm	
lux†	lx	1 lx = 1 lm/m^2
meter†	m	
mho	mho	1 mho = 1 S
micron	μ	The equivalent unit μm is preferred
mil	mil	1 mil = 10^{-3} in = 0.0254 mm (exactly)
nit	nt	1 nt = 1 cd/m^2
ohm†	Ω	
phot	ph	1 ph = 1 lm/cm^2
second†	s	
siemens†	S	
steradian†	sr	
stilb	sb	1 sb = 1 cd/cm^2
volt†	V	
watt†	W	

† International System (SI) units.

Metric Multipliers

Most of the preceding SI unit symbols can be combined with the metric multipliers that follow.

Symbol	Prefix	Multiple
G	giga	10^9
M	mega	10^6
k	kilo	10^3
h	hecto	10^2
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}

Analog Output

An output whose amplitude is continuously proportionate to the input.

Axis of Measurement

The direction from the source of radiant energy, relative to the mechanical axis, in which the measurement of radiometric and/or spectroradiometric characteristics is performed.

Black Level

The display signal level corresponding to the maximum limit for black peaks.

Brightness

See Luminance.

Charge-Coupled Device (CCD)

A charge-transfer device that stores charge in potential wells and transfers this charge almost completely as a packet by translating the position of the potential wells.

Charge-Coupled Image Sensor

A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

Charge-Transfer Device (CTD)

A device in which the operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface, or through the interconnections on the semiconductor surface.

Color Contrast

The ratio of the luminance values of two colors.

Color Encoder

A device that produces an encoded color signal from separate red, green, and blue color inputs.

Color Edging

Undesired colors appearing at the edges of colored images.

Color Temperature (of a light source)

The absolute temperature of a blackbody radiator having a chromaticity equal to that of the light source.

TYPICAL UNIT: K (formerly °K).

Coordinates

A method of locating a pixel in space, typically using an x, y, and z axis. (Cartesian Coordinates System).

Current Transfer Ratio, DC (of an Optocoupler) (h_F or CRT)

The ratio of the dc output current to the dc input current.

Dark Current (I_D)

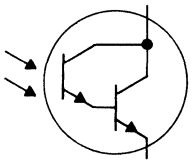
The current that flows through a photosensitive device in the dark condition.

NOTE: The dark condition is attained when the electrical parameter under consideration approaches a value that cannot be altered by further irradiation shielding.

Darlington Phototransistor

A phototransistor whose collector and emitter are connected to the collector and base, respectively, of a second transistor. The emitter current of the input transistor is amplified by the second transistor and the device has very high sensitivity to illumination or irradiation.

GRAPHIC SYMBOL:



NOTE: The base region(s) may or may not be brought out as (an) electrical terminal(s).

Delay Time (t_d)

The time interval from the point at which the leading edge of the input pulse has reached 10% of its maximum amplitude to point at which the leading edge of the output pulse has reached 10% of its maximum amplitude.

Demodulation Bandwidth (B)

The frequency interval in which the demodulated output of a photodetector, or a system including a photodetector, is not more than 3 dB below the midband output. Midband output is the output in the region of flat response or the average output over a specific frequency range.

Fall Time (t_f)

The time duration during which the trailing edge of a pulse is decreasing from 90% to 10% of its maximum amplitude.

Forward Current (I_F)

The current through a semiconductor diode when the p-region (anode) is a positive potential with respect to the n-region (cathode).

Forward Voltage (V_F)

The voltage across a semiconductor diode associated with the flow of forward current. The p-region is a positive potential width respect to the n-region.

Gray Scale

An optical pattern in discrete steps between light and dark.

Note: A gray scale with ten steps that differ by the square root of two is usually in resolution test charts.

Half-Intensity Beam Angle (θ_{HI})

The angle within which the radiant intensity is not less than half of the maximum intensity.

Hexadecimal Display

A solid-state display capable of exhibiting numbers 0 through 9 and alpha characters A through F.

NOTE: The TIL311 is a hexadecimal display with an integral TTL circuit that will accept, store, and display 4-bit binary data.

Illuminance (Illumination) (E_V)

The luminous flux density incident on a surface; the quotient of the flux divided by the area of illuminated surface.

TYPICAL UNITS: lm/ft^2, lx = lm/m^2; 1 lm/ft^2 = 10.76391 lx.

Image

A displayed view of one or more objects or parts of objects.

Infrared Emission

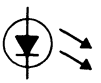
Radiant energy that is characterized by wavelengths longer than visible red, i.e., about 0.78 μm to 100 μm.

Infrared-Emitting Diode (IRED)

A diode capable of emitting radiant energy in the infrared region of the spectrum resulting from the recombination of electrons and holes.

NOTE: TI manufactures GaAs and GaAlAs radiant-energy sources that emit in the 0.82-um to 0.94-um portion of the near-infrared region. These emitters are spectrally matched with TI silicon photodetectors.

GRAPHIC SYMBOL:



Irradiance (E_e, formerly H)

The radiant flux density incident on a surface; the quotient of the flux divided by the area of irradiated surface.

TYPICAL UNITS: W/ft^2, W/m^2; 1 W/ft^2 = 10.76391 W/m^2.

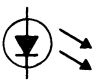
Light Current (I_L)

The current that flows through a photosensitive device, such as a phototransistor or a photodiode, when it is exposed to radiant energy.

Light-Emitting Diode (LED)

A diode capable of emitting luminous energy resulting from the recombination of electrons and holes.

GRAPHIC SYMBOL:



Linearity

The property of being linear. A linear relationship exists between two quantities when a change in a second quantity is directly proportional to change in the first quantity.

Luminance (L_V) (Photometric Brightness)

The luminous intensity of a surface in a given direction per unit of projected area of the surface as viewed from that direction.

TYPICAL UNITS: fL, cd/ft^2, cd/m^2; 1 fL = $(1/\pi)$ cd/ft^2 = 3.426259 cd/m^2.

Luminous Energy (Q_V)

The time rate of flow of luminous energy.

TYPICAL UNITS: lm∗s.

Luminous Flux (Φ_V)

Energy traveling in the form of visible radiation.

TYPICAL UNIT: lm

NOTE: Luminous flux is related to radiant flux by the eye-response curve of the International Commission of Illumination (CIE). At the peak response (λ = 555 nm), 1 W = 680 lm.

Luminous Intensity (I_V)

Luminous flux per unit solid angle in a given direction.

TYPICAL UNIT: cd. 1 cd = 1 lm/sr.

Luminous Responsivity (R_V)

The quotient of the rms value of the fundamental component of the electrical output divided by the rms value of the fundamental component of the luminous flux of a specified distribution.

TYPICAL UNITS: V/lm, A/lm.

Modulation Frequency (f_{mod})

The frequency of modulation of the luminous or radiant flux.

Monochrome

Any combination of colors of the same hue, but of different saturations and luminances.

Noise Equivalent Bandwidth (Δf)

The equivalent bandwith of a flat (or white) sharp-cutoff noise spectrum, having the same maximum value and containing the same noise power as the actual broadband output noise power of the device or circuit.

TYPICAL UNIT: Hz.

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Noise Equivalent Power (P_n or NEP)

The rms value of the fundamental component of a modulated radiant flux incident on the detector area that will produce a signal (voltage or current) at the detector output that is equal to the broadband rms noise (voltage or current).

TYPICAL UNIT: W.

NOTE: The noise equivalent power equals the broadband output noise (voltage or current) divided by the responsivity (in volts/watt or amperes/watt).

Noise Equivalent Power (Spectral Density) (P_n or NEP)

The noise equivalent power in a one-hertz bandwidth at the detector output.

TYPICAL UNITS: $W/Hz^{1/2}$.

NOTE: The noise equivalent power spectral density equals the noise equivalent power divided by the square root of the noise bandwidth.

Off-State Collector Current ($IC(_{off})$) (of an Optocoupler)

The output current when the input current is zero.

On-State Collector Current ($IC(_{on})$) (of an Optocoupler)

The output current when the input current is above the threshold level.

NOTE: An increase in the input current will usually result in a corresponding increase in the on-state collector current.

Optical Axis

A line about which the radiant-energy pattern is centered.

NOTES: 1. The radiant-energy pattern may be nonsymmetrical.
2. The optical axis may deviate from the mechanical axis.

Optocoupler (Optically Coupled Isolator, Photocoupler)

A device designed for the transformation of electrical signals by utilizing optical radiant energy so as to provide coupling with electrical isolation between the input and the output.

NOTE: As manufactured by Texas Instruments, these devices consist of a gallium arsenide infrared-emitting diode and a silicon phototransistor and provide high-voltage isolation between separate pairs of input and output terminals.

Optoelectronic Device

A device that is responsive to or that emits or modifies coherent or noncoherent electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions; or a device that utilizes such electromagnetic radiation for its internal operation.

Photocurrent

The difference between light current (I_L) and dark current (I_D) in a photodetector.

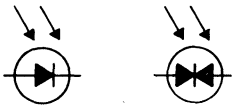
Photodetector, Photosensitive Device

A device that is responsive to electromagnetic radiation in the visible, infrared, and/or ultraviolet spectral regions.

Photodiode

A diode that is intended to be responsive to radiant energy.

GRAPHIC SYMBOLS:



NOTE: The photodiode is characterized by linearity between the input radiation and the output current. It has faster switching speeds than a phototransistor.

Photometric Axis

See Axis of Measurement.

Photometric Brightness

See Luminance.

Photon

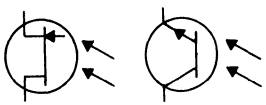
A quantum (the smallest possible unit) of radiant energy; a photon carries a quantity of energy equal to Planck's constant (6.6262×10^{-34} joule/hertz) times the frequency.

Phototransistor

A transistor (bipolar or field-effect) that is intended to be responsive to radiant energy.

NOTE: The base region or gate may or may not be brought out as an external terminal.

GRAPHIC SYMBOLS:



Picture Element

The smallest segment of a raster line which can be discretely controlled by the display system. Also called a pixel, pel, or pixcell.

Quantum Efficiency (of a Photosensitive Device)

The fractional number of effective electron-hole pairs produced within the device for each incident photon. For devices that internally amplify or multiply the electron-hole pairs, such as phototransistors or avalanche photodiodes, the effect of the gain is to be excluded from quantum efficiency.

Quantum Efficiency, External (of a Photoemitter)

The number of photons radiated for each electron flowing into the radiant source.

Radiance (L_e)

The radiant intensity of a surface in a given direction per unit of projected area of the surface as viewed from that direction.

TYPICAL UNIT: $W*sr^{-1}m^{-2}$.

Radiant Energy (Q_e)

Energy traveling in the form of electromagnetic waves.

TYPICAL UNITS: W*s, J.

Radiant Flux or Power Output (Φe or P_O)

The time rate of flow of radiant energy.

TYPICAL UNITS: W.

Radiant Intensity (I_e)

Radiant flux per unit solid angle in a given direction.

TYPICAL UNIT: W/sr.

Radiant Pulse Fall Time (t_f)

The time required for a radiometric quantity to change from 90% to 10% of its peak value for a step change in electrical input.

Radiant Pulse Rise Time (t_r)

The time required for a radiometric quantity to change from 10% to 90% of its peak value for a step change in electrical input.

Radiant Responsivity (Re)

The quotient of the rms value of the fundamental component of the electrical output divided by the rms value of the fundamental component of the radiant flux of a specified distribution.

TYPICAL UNITS: V/W, A/W.

Resolution

The number of visible distinguishable units in the device coordinate space.

Reverse Current (I_R)

The current through a semiconductor diode when the n region (cathode) is at a positive potential with respect to the p region (anode).

Reverse Voltage (V_R)

The voltage across a semiconductor diode associated with the flow of reverse current. The n region is at a positive potential with respect to the p region.

Rise Time (t_r)

The time duration during which the leading edge of a pulse is increasing from 10% to 90% of its maximum amplitude.

Series Resistance

The undepleted bulk resistance of the photodiode substrate.

NOTE: This characteristic becomes significant at higher frequencies where the capacitive reactance of the junction is of the same or lower magnitude compared to the series resistance.

Shift Register

A register in which the stored data can be moved from left to right, or vice versa.

Spectral Bandwidth ($\Delta\lambda$)

The wavelength interval in which the spectral concentration of a photometric or radiometric quantity is not less than half of its maximum value.

TYPICAL UNITS: Å, μm, nm.

Steradian (sr)

A unit of solid angular measurement equal to the solid angle at the center of a sphere subtended by a portion of the surface area equal to the square of the radius; there are 4 π steradians in a complete sphere. The number of steradians in a cone of full angle θ is 2 π (1 $-$ cos 0.5).

Storage Time (t_s)

The time interval from a point at which the trailing edge of the input pulse has dropped to 90% of its maximum amplitude to a point at which the trailing edge of the output pulse has dropped to 90% of its maximum amplitude.

Visible Emission

Radiant energy that is characterized by wavelengths of about 0.38 μm to 0.78 μm.

Wavelength at Peak Emission (λp)

The wavelength at which the spectral radiant intensity is maximum.

TYPICAL UNITS: Å, μm, nm. 1 Å $= 10^{-4}$ μm $= 0.1$ nm.

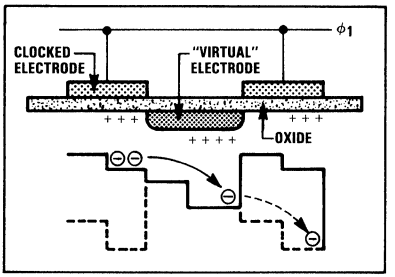


Fig. 1 TI's Patented Virtual Phase Design

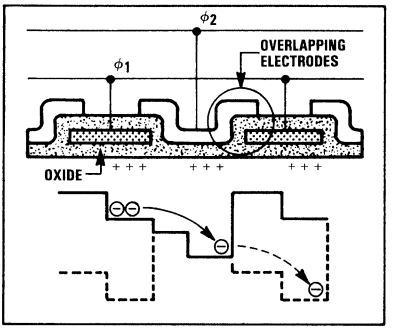


Fig. 2 Standard 2 Phase Design

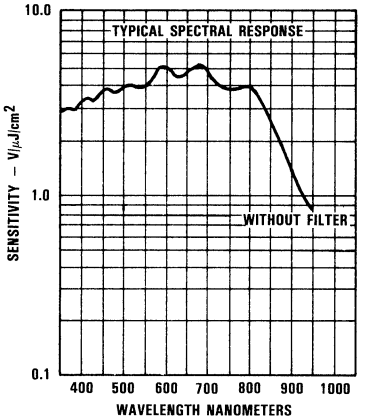


Fig. 3. Typical Sensitivity vs Wavelength

The CCD (Charge Coupled Device) approach to linear image sensing will become the leading edge among industry methods because of process and performance advantages.

Multiple-clock-electrode CCD processing methods have remained complex and difficult to implement in the manufacturing environment with any measure of cost/performance effectiveness ... until now.

The breakthrough: Now, Texas Instruments announces a breakthrough in CCD image sensor processing technology ... Virtual Phase (VP).

This giant technological stride greatly simplifies the processing techniques by **reducing the number of clock electrodes on the device surface to one** (Fig. 1). Other techniques require anywhere from two to three levels (Fig. 2). Additional benefits of this milestone process include simplified device operation and enhanced device quality.

Now, with just one level, the possibility of surface damage and shorts, common to the multilevel approach, is inherently reduced. So, the new Virtual Phase technology can boast the same degree of reliability as standard MOS technology.

The benefits of this TI-patented Virtual Phase technology are:

- Simplified clocking
- Lower noise/Higher dynamic range
- Greater sensitivity to light
- Ease of processing and use
- Greater stability
- Lower dark current
- Improved spectral response in the lower wave length (blue) regions (Fig. 3).

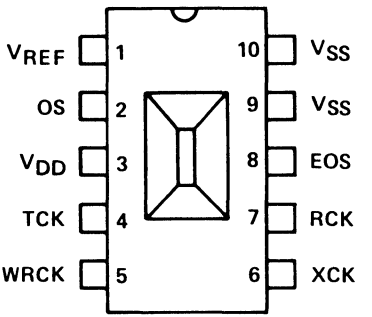
Features:

- Virtual Phase N-Channel silicon MOS technology
- High spectral responsivity ... particularly in the blue region
- Approximately 1-V peak-to-peak output signal
- Dynamic range typically 1000:1
- End-of-scan signal
- Internal dark and white references
- Blemish-free uniformity of image
- Simple, stable operation

D2664, APRIL 1982–REVISED JULY 1989

- 128 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 1 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation

CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the output amplifiers.

description

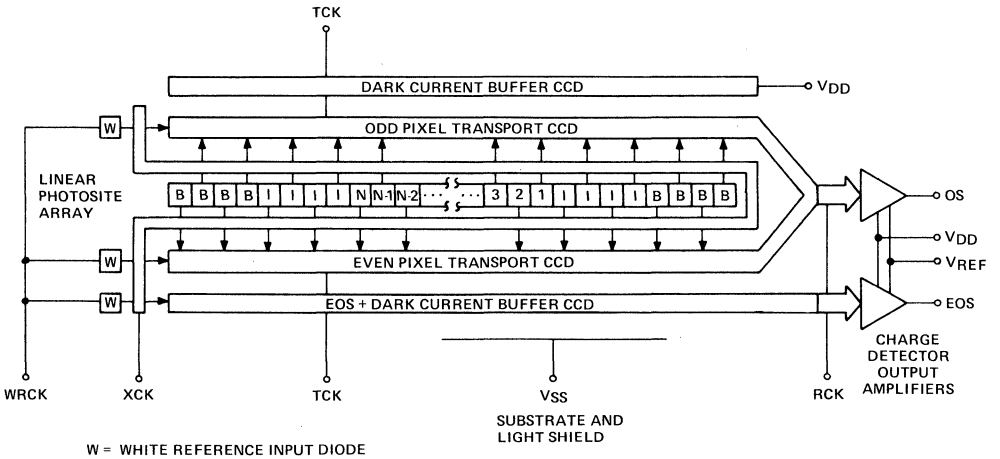
The TC102, a 128-element CCD line image sensor, functions in high-resolution image scanning applications such as document reading and optical character recognition. The TC102 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability.

This device is supplied in a 10-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 7.6-mm (0.300-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

virtual-phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. Virtual-phase technology utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 128 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers.
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier.
3	V_{DD}	Supply Voltage	Output amplifier supply voltage.
4	TCK	Transport Clock	Drives the CCD transport registers.
5	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
6	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
7	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
8	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.
9, 10	V_{SS}	Substrate	All voltages are referenced to the substrate.

functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 128 photo-sensitive areas, 12.7 micrometers (0.5 milliinches) square and approximately 12.7 micrometers from center to center. Image photons create electron-hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry. The white reference pulse amplitude is approximately 70% of the maximum output signal amplitude.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. A reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output. No external current sink is needed. The output signal is a series of negative-going pulses on a dc level.

resolution

The modulation transfer function decreases at longer wavelengths (see Figures 7 and 8). If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 161 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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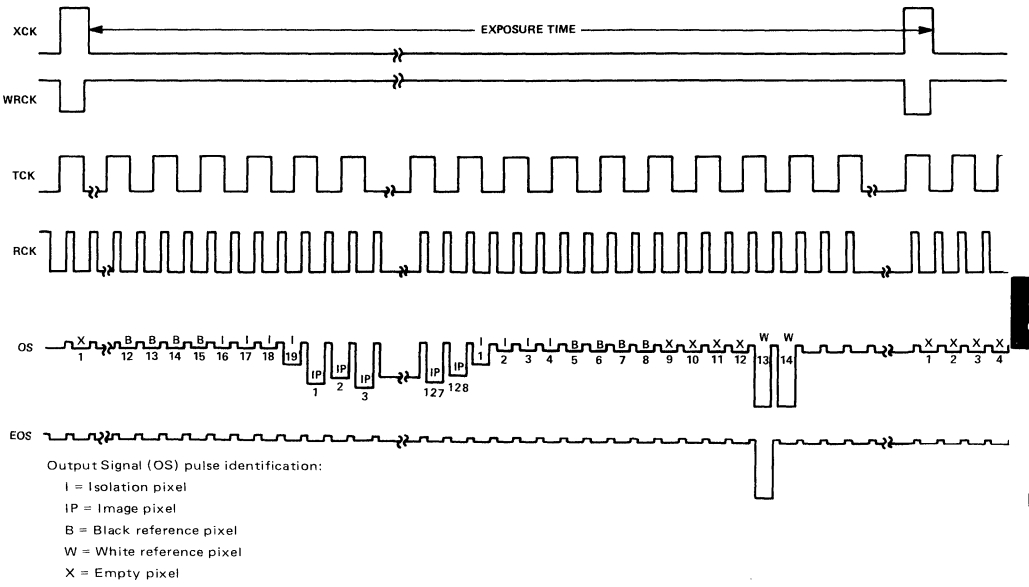

FIGURE 1 – OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage (V_{DD})	−0.3 V to 30 V
Amplifier reference voltage (V_{REF})	−0.3 V to 30 V
Transfer clock (XCK) voltage	−25 V to 5 V
Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25 °C to 125 °C
Operating free-air temperature	−25 °C to 70 °C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions at T_A = 25°C

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	15	16	20	V
V_{REF}	Amplifier reference voltage	6	7	8	V
$V_{IH(X)}$	Transfer clock high-level input voltage	1	2	3	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(T)}$	Transport clock high-level input voltage	1	2	3	V
$V_{IL(T)}$	Transport clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(R)}$	Reset clock high-level input voltage	1	2	3	V
$V_{IL(R)}$	Reset clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(WR)}$	White reference clock high-level input voltage	15	16	20	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)		2	10	MHz

¶The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.

electrical characteristics at 25°C free-air temperature, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values.

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low frequency component		0.5	5	
	Nonuniformity relative to average of adjacent pixels		1	20	
Sensitivity		2	3.5	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		50	100	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			1		mV
Equivalent exposure§ of peak-to-peak noise			0.35		nJ/cm²
Saturation exposure§			350		nJ/cm²
Saturation output amplitude		700	1000	1400	mV
Dynamic range relative to peak-to-peak noise†		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude		500	700		mV
End-of-scan amplitude		300	500		mV
Output offset (dc) voltage			10		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		45		kΩ
	Transport gate		45		
	Reset gate		45		
Capacitance to V_{SS}	Transfer gate		26		pF
	Transport gate		57		
	Reset gate		7		
I_{REF}	Amplifier reference current		3		nA
I_{DD}	Supply current		6.3	9.4	mA
Power dissipation			100		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 700 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time

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timing requirements

		MIN	NOM	MAX	UNIT
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge	0		100	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge	0		100	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge	0		100	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse	50			ns
t_r	rise time (all clocks)	15			ns
t_f	fall time (all clocks)	5			ns

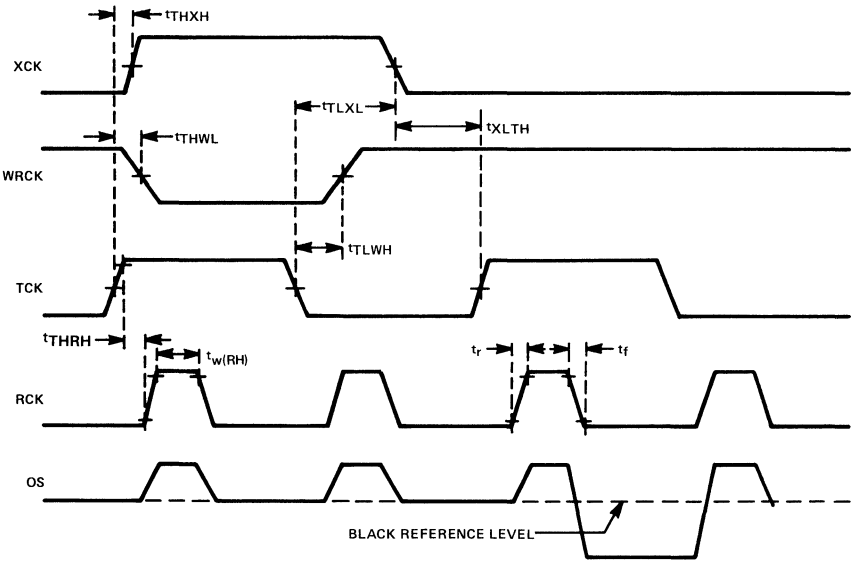
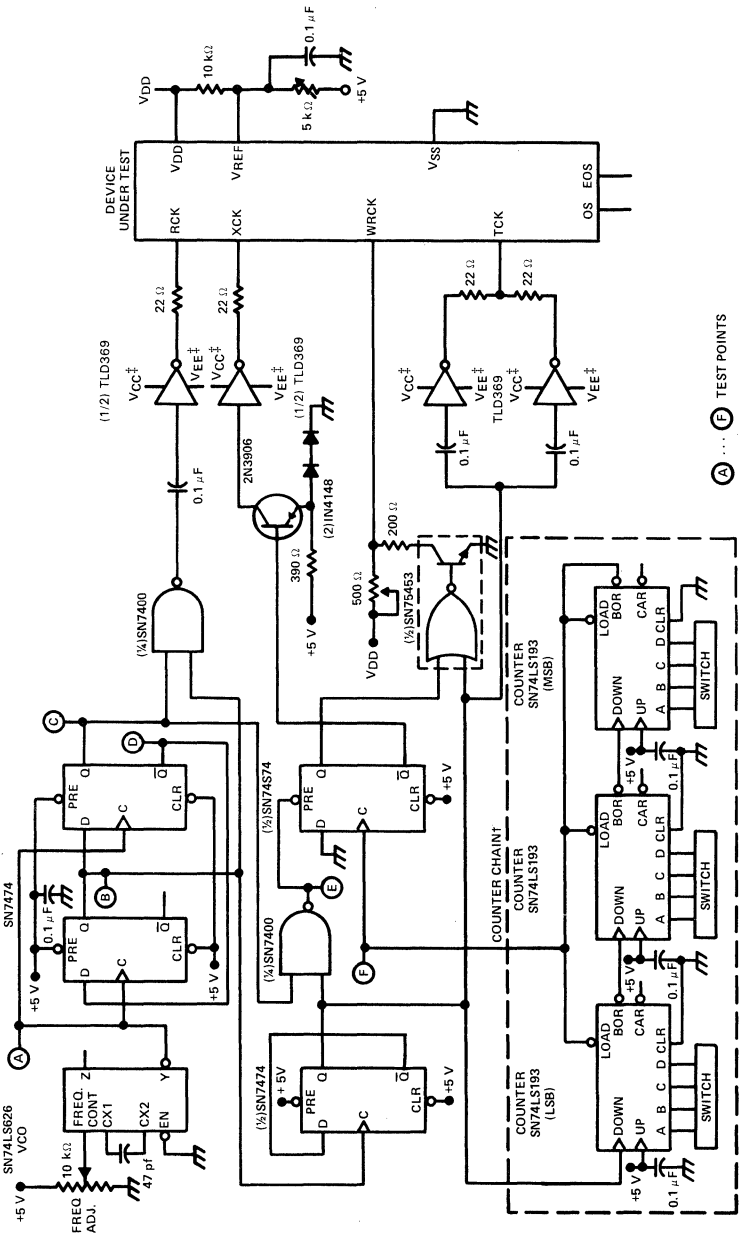


FIGURE 2 – DEVICE TIMING REQUIREMENTS

PARAMETER MEASUREMENT INFORMATION



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3 – DRIVER CIRCUIT FOR TESTING LINE IMAGE SENSOR

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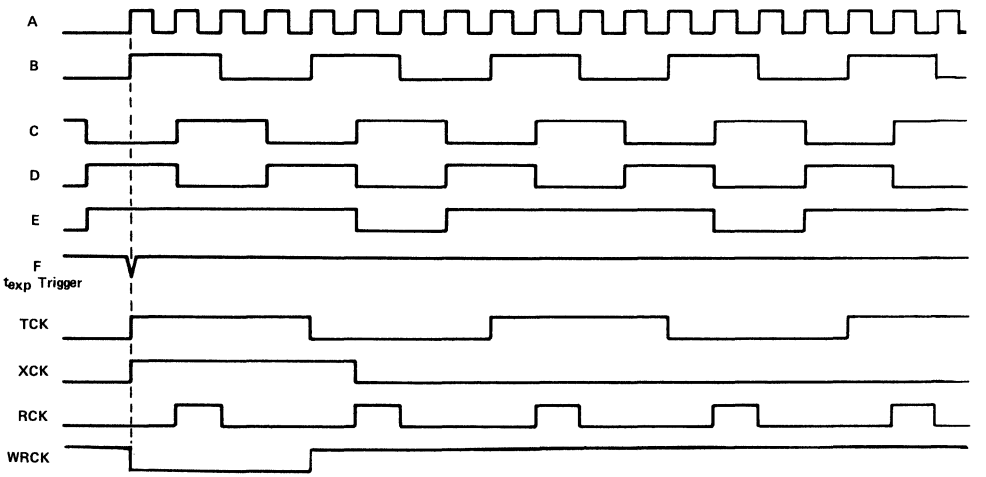

FIGURE 4 – WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

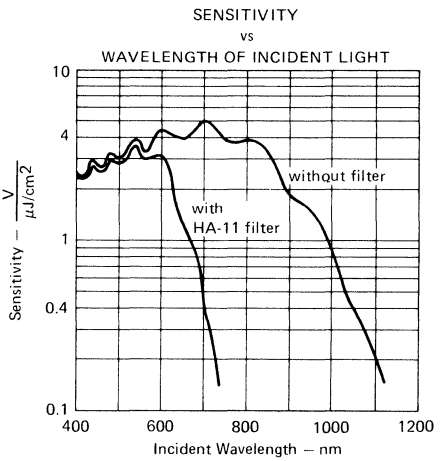

FIGURE 5

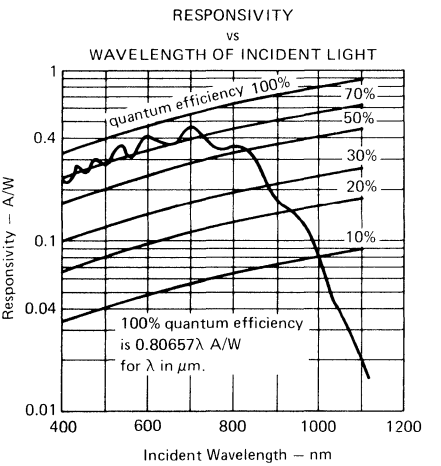

FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

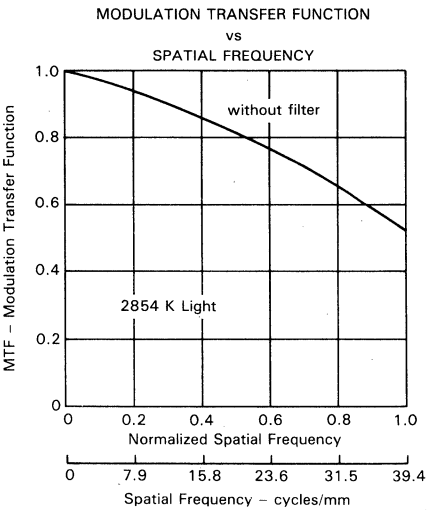

FIGURE 7

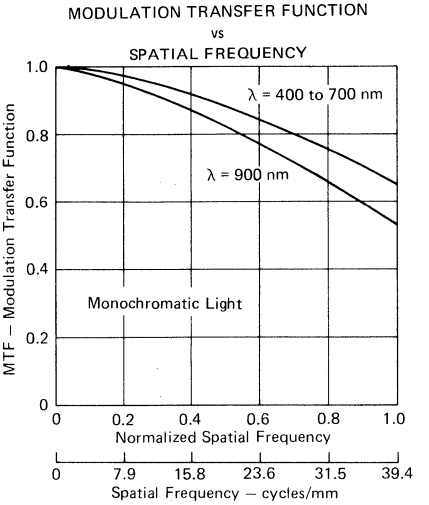

FIGURE 8

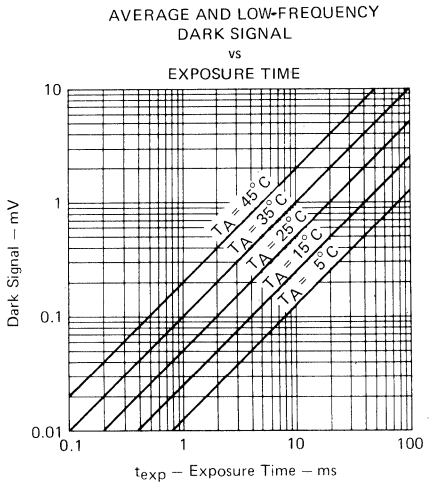

FIGURE 9

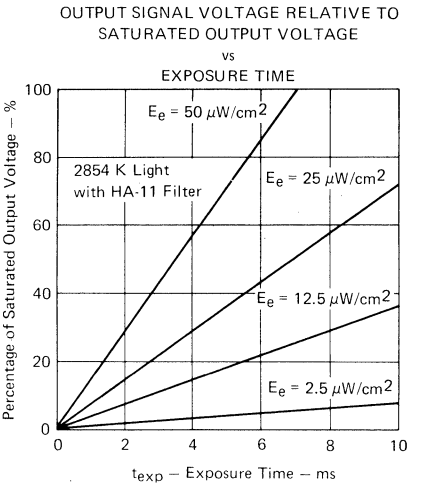

FIGURE 10

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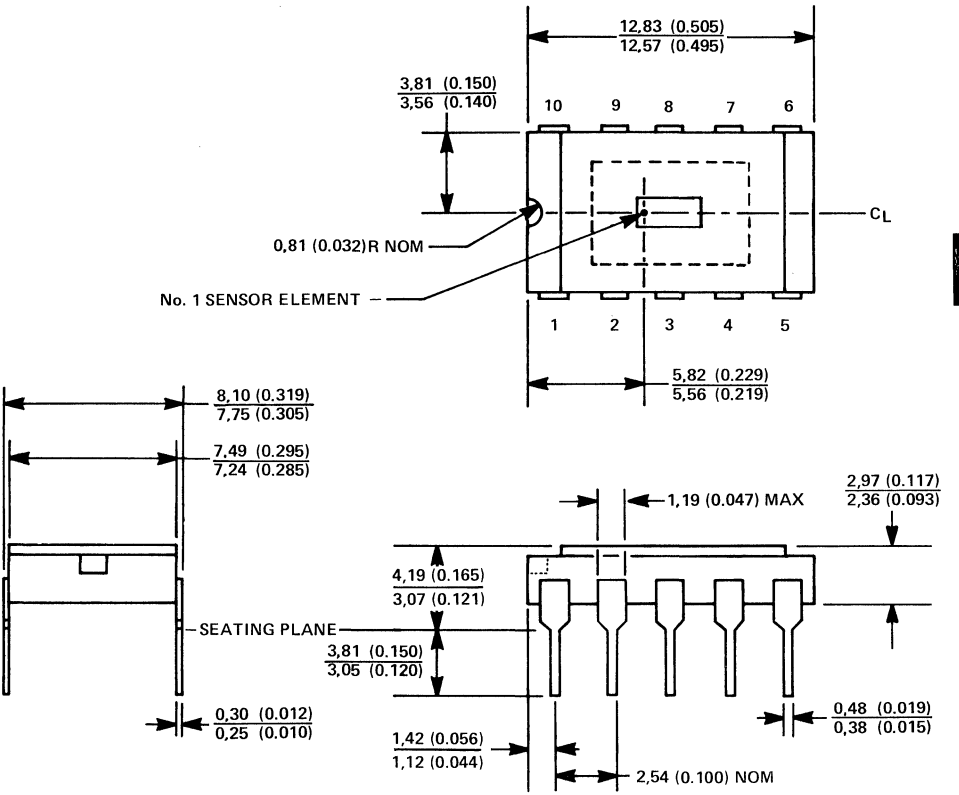
MECHANICAL DATA

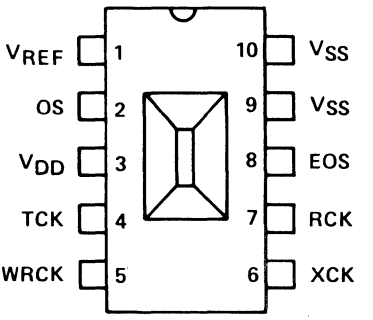


NOTES: 1. All dimensions are in millimeters and parenthetically in inches.
2. The distance between the top surface of the window and the surface of the sensor is nominally 0,89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

D2664, DECEMBER 1983—REVISED JULY 1989

- 128 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 1 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- Same as TC102 Except for "White Reference Amplitude" and "End-of-Scan Amplitude" Specifications

CERAMIC DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

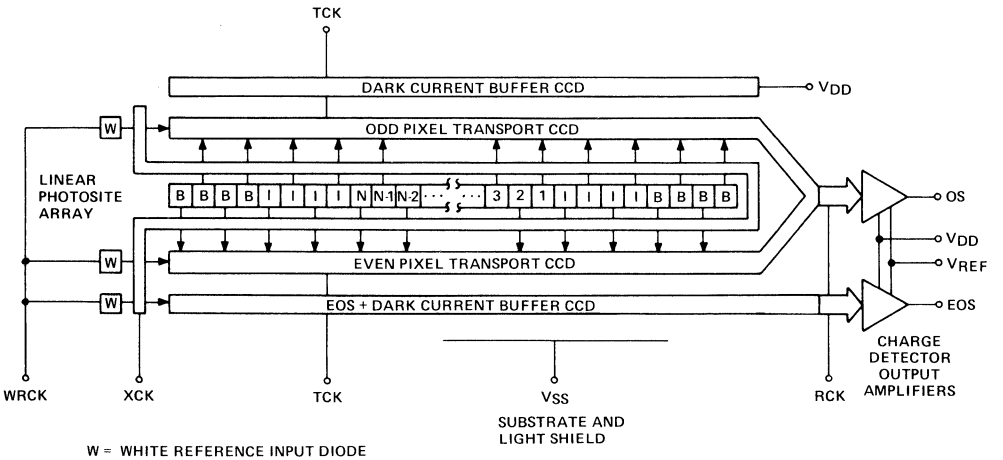
The TC102-1, a 128-element CCD line image sensor, functions in high-resolution image scanning applications such as document reading and optical character recognition. The TC102-1 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the output amplifiers.

virtual phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. Virtual-phase technology utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 128 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers.
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier.
3	V_{DD}	Supply Voltage	Output amplifier supply voltage.
4	TCK	Transport Clock	Drives the CCD transport registers.
5	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
6	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
7	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
8	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.
9, 10	V_{SS}	Substrate	All voltages are referenced to the substrate.

functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 128 photo-sensitive areas, 12.7 micrometers (0.5 milliinches) square and approximately 12.7 micrometers from center to center. Image photons create electron-hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. A reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output. No external current sink is needed. The output signal is a series of negative-going pulses on a dc level.

resolution

The modulation transfer function decreases at longer wavelengths (see Figures 7 and 8). If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 161 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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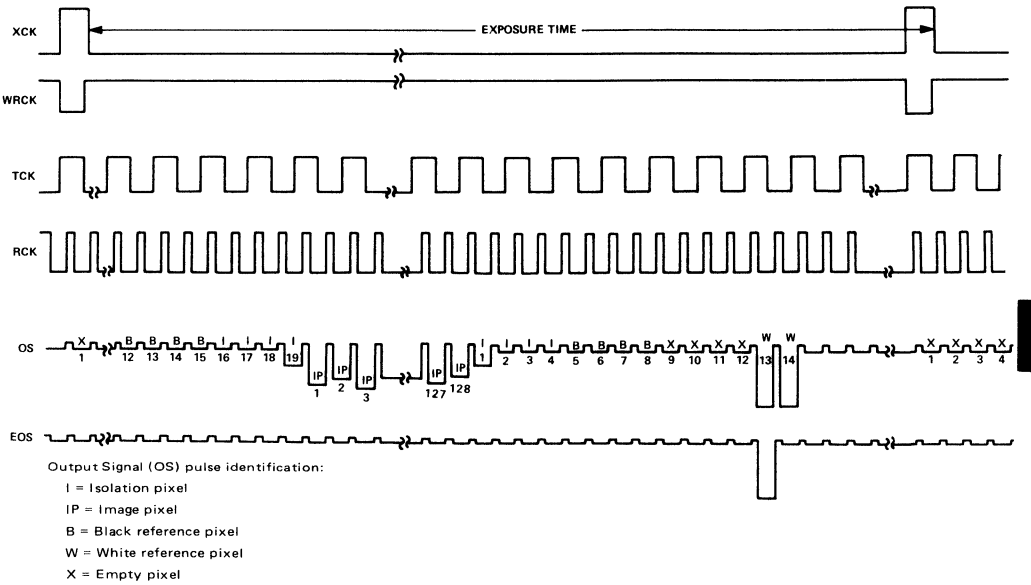


FIGURE 1 – OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage (V_{DD})	−0.3 V to 30 V
Amplifier reference voltage (V_{REF})	−0.3 V to 30 V
Transfer clock (XCK) voltage	−25 V to 5 V
Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25 °C to 125 °C
Operating free-air temperature	−25 °C to 70 °C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions at T_A = 25°C

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	15	16	20	V
V_{REF}	Amplifier reference voltage	6	7	8	V
$V_{IH(X)}$	Transfer clock high-level input voltage	1	2	3	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(T)}$	Transport clock high-level input voltage	1	2	3	V
$V_{IL(T)}$	Transport clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(R)}$	Reset clock high-level input voltage	1	2	3	V
$V_{IL(R)}$	Reset clock low-level input voltage	−17¶	−16	−15	V
$V_{IH(WR)}$	White reference clock high-level input voltage	15	16	20	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)		2	10	MHz

¶The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.

electrical characteristics at 25°C free-air temperature, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values.

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low frequency component		0.5	5	
	Nonuniformity relative to average of adjacent pixels		1	20	
Sensitivity		2	3.5	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		50	100	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			1		mV
Equivalent exposure§ of peak-to-peak noise			0.35		nJ/cm²
Saturation exposure§			350		nJ/cm²
Saturation output amplitude		700	1000	1400	mV
Dynamic range relative to peak-to-peak noise†		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude			500		mV
End-of-scan amplitude			300		mV
Output offset (dc) voltage			10		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		45		kΩ
	Transport gate		45		
	Reset gate		45		
Capacitance to V_{SS}	Transfer gate		26		pF
	Transport gate		57		
	Reset gate		7		
I_{REF}	Amplifier reference current		3		nA
I_{DD}	Supply current		6.3	9.4	mA
Power dissipation			100		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 700 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time

timing requirements

		MIN	NOM	MAX	UNIT
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge	0		100	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge	0		100	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge	0		100	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse	50			ns
t_r	rise time (all clocks)	15			ns
t_f	fall time (all clocks)	5			ns

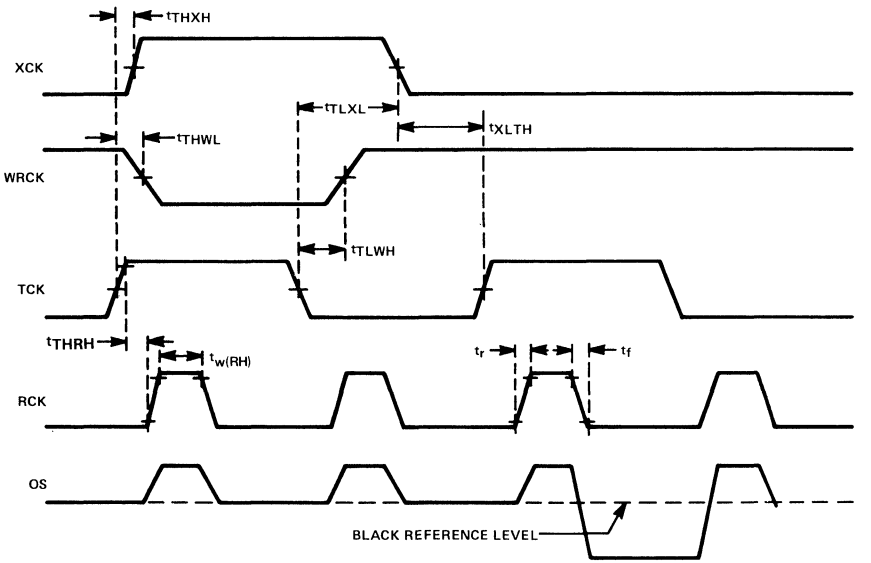
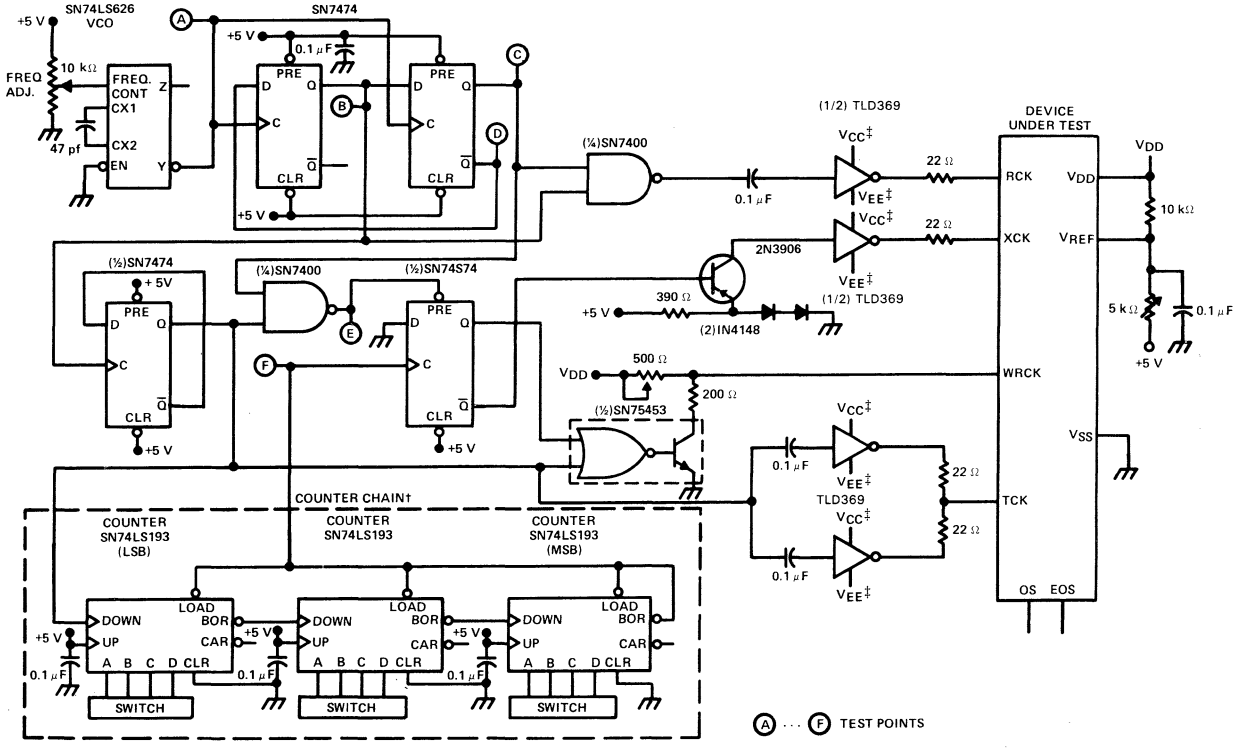


FIGURE 2 – DEVICE TIMING REQUIREMENTS



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.

‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3 – DRIVER CIRCUIT FOR TESTING LINE IMAGE SENSOR

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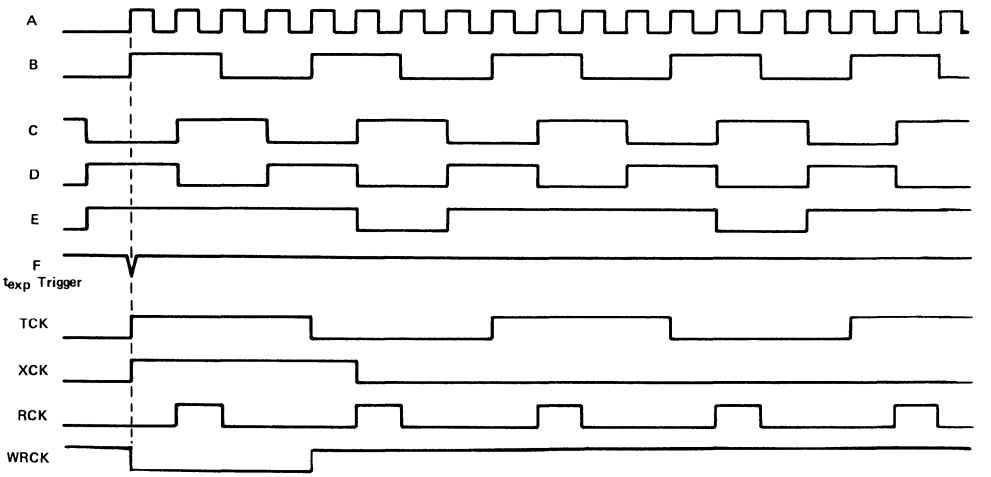

FIGURE 4 – WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

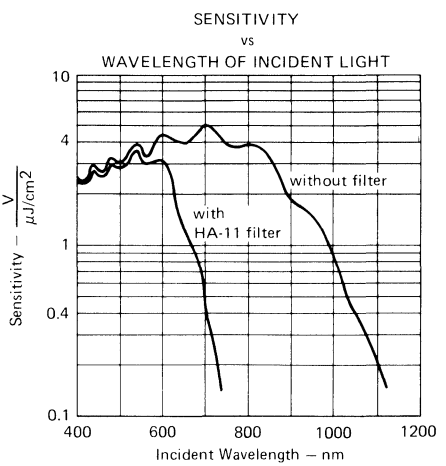

FIGURE 5

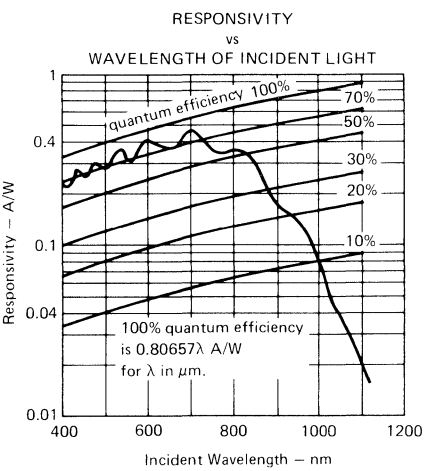

FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

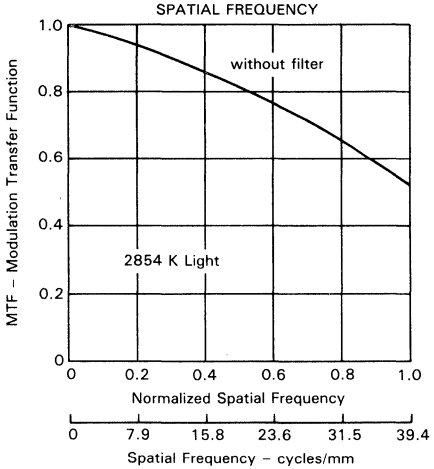

FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

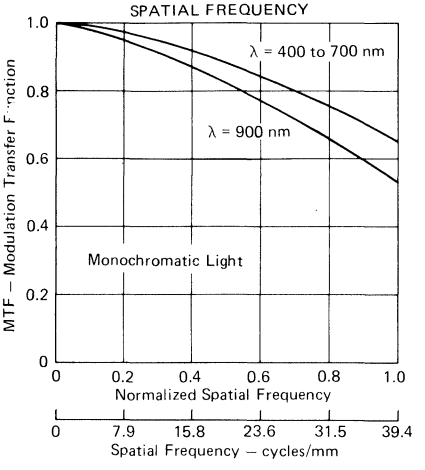

FIGURE 8

AVERAGE AND LOW-FREQUENCY
DARK SIGNAL
vs
EXPOSURE TIME

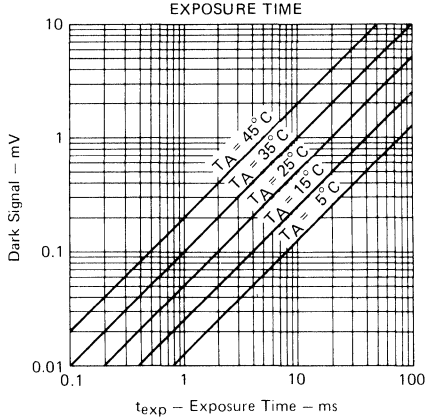

FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO
SATURATED OUTPUT VOLTAGE
vs
EXPOSURE TIME

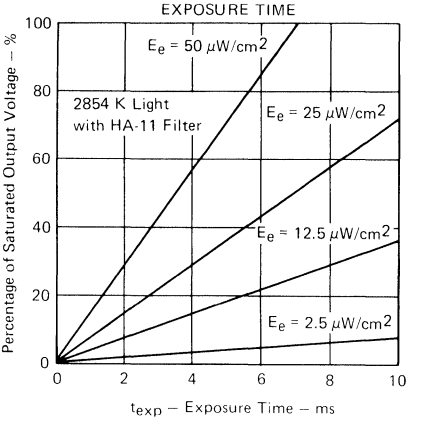

FIGURE 10

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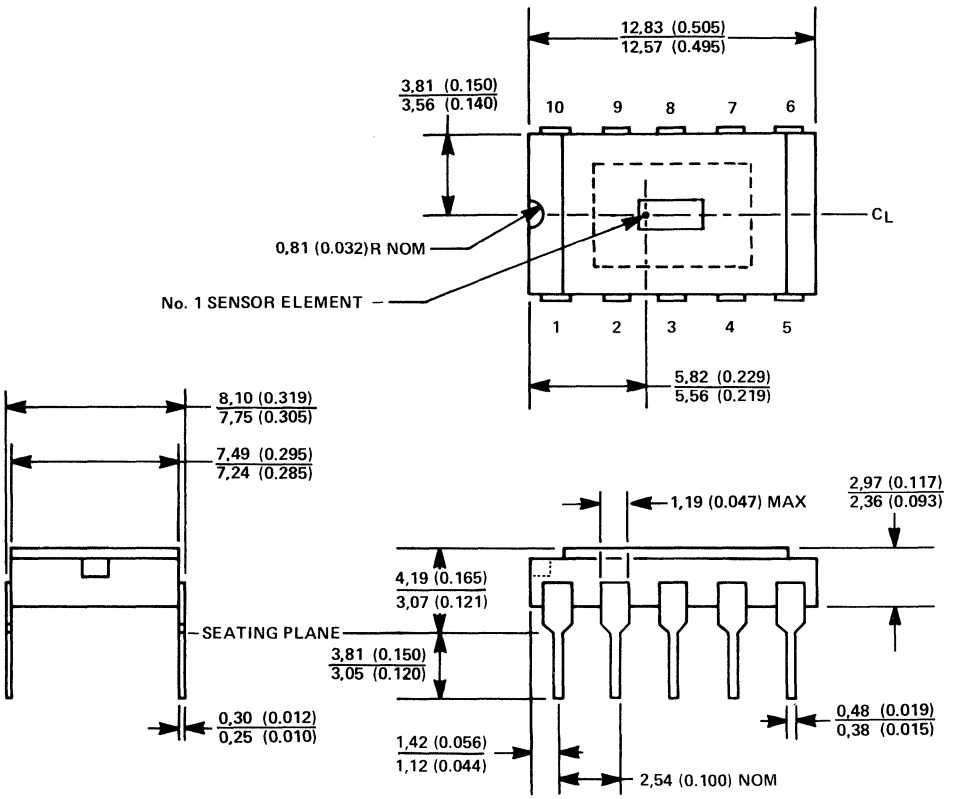
MECHANICAL DATA

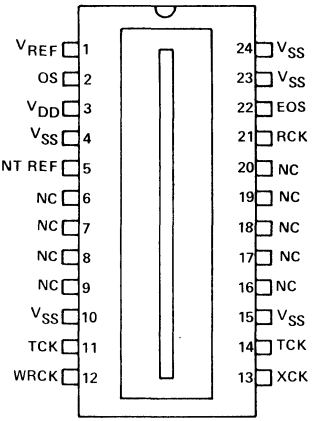


NOTE: The distance between the top surface of the window and the surface of the sensor is nominally 0,89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICLALY IN INCHES

- 2048 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 1.0 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- OPTIONAL FEATURE: Internal Reference Voltage

TC103 . . . DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC — No internal connection

description

The TC103, a 2048-element CCD line image sensor, functions in high-resolution image scanning applications such as facsimile and optical character recognition. The TC103 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability. The 2048 sensor elements provide 8 points-per-millimeter resolution across 256 millimeters.

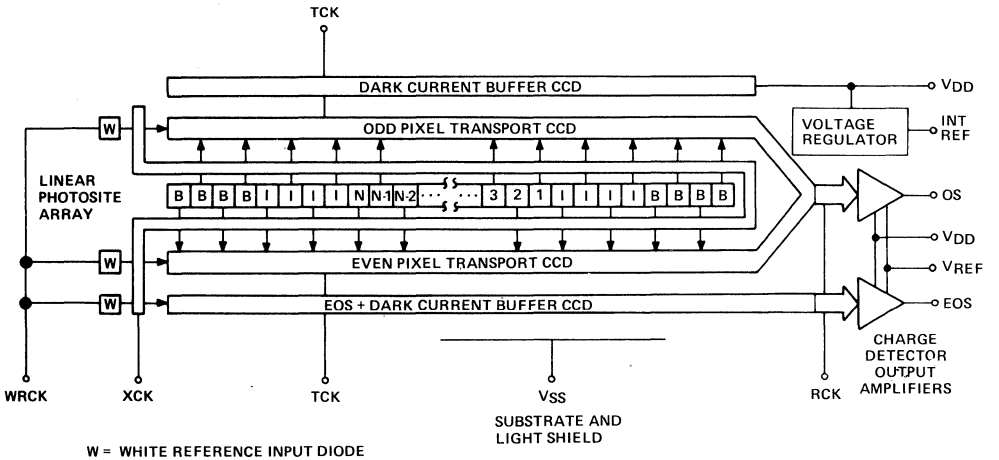
This device is supplied in a 24-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 15,2-mm (0,600-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

virtual phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. The virtual phase utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 2048 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers and internal reference.
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier.
3	V_{DD}	Supply Voltage	Output amplifier supply voltage.
4, 10, 15, 23, 24	V_{SS}	Substrate	All voltages are referenced to the substrate.
5	INT REF	Internal Reference	Potential derived internally for operational reference voltage.
6, 7, 8, 9, 16 17, 18, 19, 20	NC		No internal connection.
11, 14	TCK	Transport Clock	Drives the CCD transport registers.
12	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
13	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
21	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
22	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.

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functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 2048 photo-sensitive areas, 12,7 micrometers (0.5 milliinches) square and approximately 12,7 micrometers from center to center. Image photons create electron/hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements, and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry. The white reference pulse amplitude is approximately 70% of the maximum output signal amplitude.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. Reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output, so no external current sink is needed. The output signal on pin 2 is a series of negative-going pulses on a dc level.

internal reference voltage

An internal reference voltage (INT REF) is available on the chip to provide the V_{REF} voltage. The required connections appear in Figure 3. If the internal reference voltage is not used, an external voltage is connected directly to pin 1. Pin 5 is then left unconnected.

resolution

The modulation transfer function decreases at longer wavelengths. (See Figures 7 and 8.) If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 2081 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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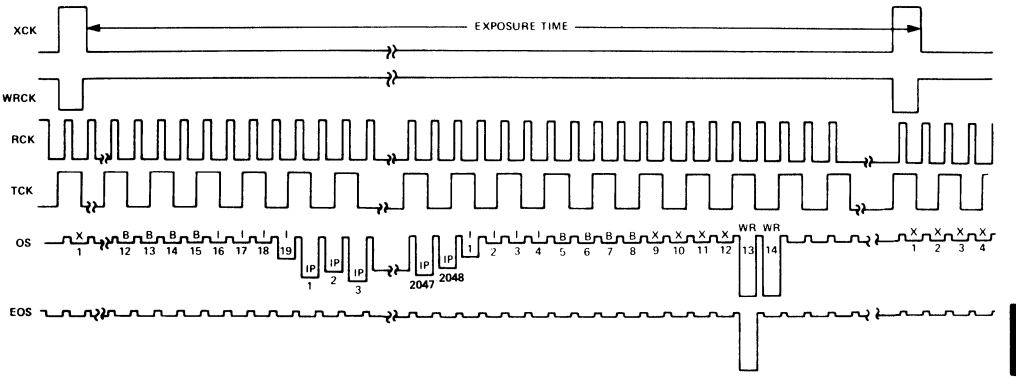


Output Signal (OS) pulse identification: I = isolation pixel, IP = Image pixel, B = Black reference pixel, WR = White reference pixel, X = empty pixel.

FIGURE 1—OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage (V_{DD1})	−0.3 V to 30 V
Transfer clock (XCK) voltage	−25 V to 5 V
Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25°C to 125°C
Operating free-air temperature	−25°C to 70°C

recommended operating conditions at T_A = 25°C (see Note 1)

		MIN	NOM	MAX	UNIT
V_{DD}	Amplifier supply voltage	13	14	15	V
$V_{IH(X)}$	Transfer clock high-level input voltage	3	4	5	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−15†	−14	−13	V
$V_{IH(T)}$	Transport clock high-level input voltage	3	4	5	V
$V_{IL(T)}$	Transport clock low-level input voltage	−15†	−14	−13	V
$V_{IH(R)}$	Reset clock high-level input voltage	3	4	5	V
$V_{IL(R)}$	Reset clock low-level input voltage	−15†	−14	−13	V
$V_{IH(WR)}$	White reference clock high-level input voltage	13	14	15	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)			10	MHz

†The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.

NOTE 1: Voltage values are with respect to V_{SS}.

electrical characteristics at 25°C free-air temperature¶

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low frequency component		0.5	5	mV
	Nonuniformity relative to average of adjacent pixels		1.0	20	
Sensitivity		2	3.5	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		50	100	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			1		mV
Equivalent exposure§ of peak-to-peak noise			0.35		nJ/cm²
Saturation exposure§			350		nJ/cm²
Saturation output amplitude		700	1000	1400	mV
Dynamic range relative to peak-to-peak noise†		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude		500	700		mV
End-of-scan amplitude		300	500		mV
Output offset (dc) voltage			7		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		150		kΩ
	Transport gate		500		
	Reset gate		500		
Amplifier reference voltage, V_{REF}			7		V
Capacitance to V_{SS}	Transfer gate		250		pF
	Transport gate		600		
	Reset gate		16		
Amplifier supply current			8	12	mA
Total power dissipation			110		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 700 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time
¶Test conditions are f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values using the internal reference voltage.

timing requirements

		MIN	NOM	MAX	UNITS
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge.	0		50	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge.	0		50	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge.	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock.	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge.	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge.	0		50	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse.	50			ns
t_r	rise time (all clocks)		15		ns
t_f	fall time (all clocks)		5		ns

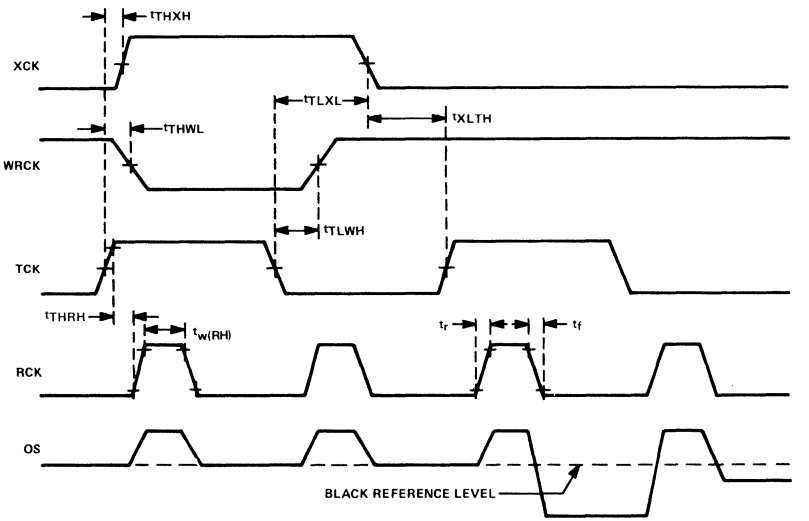
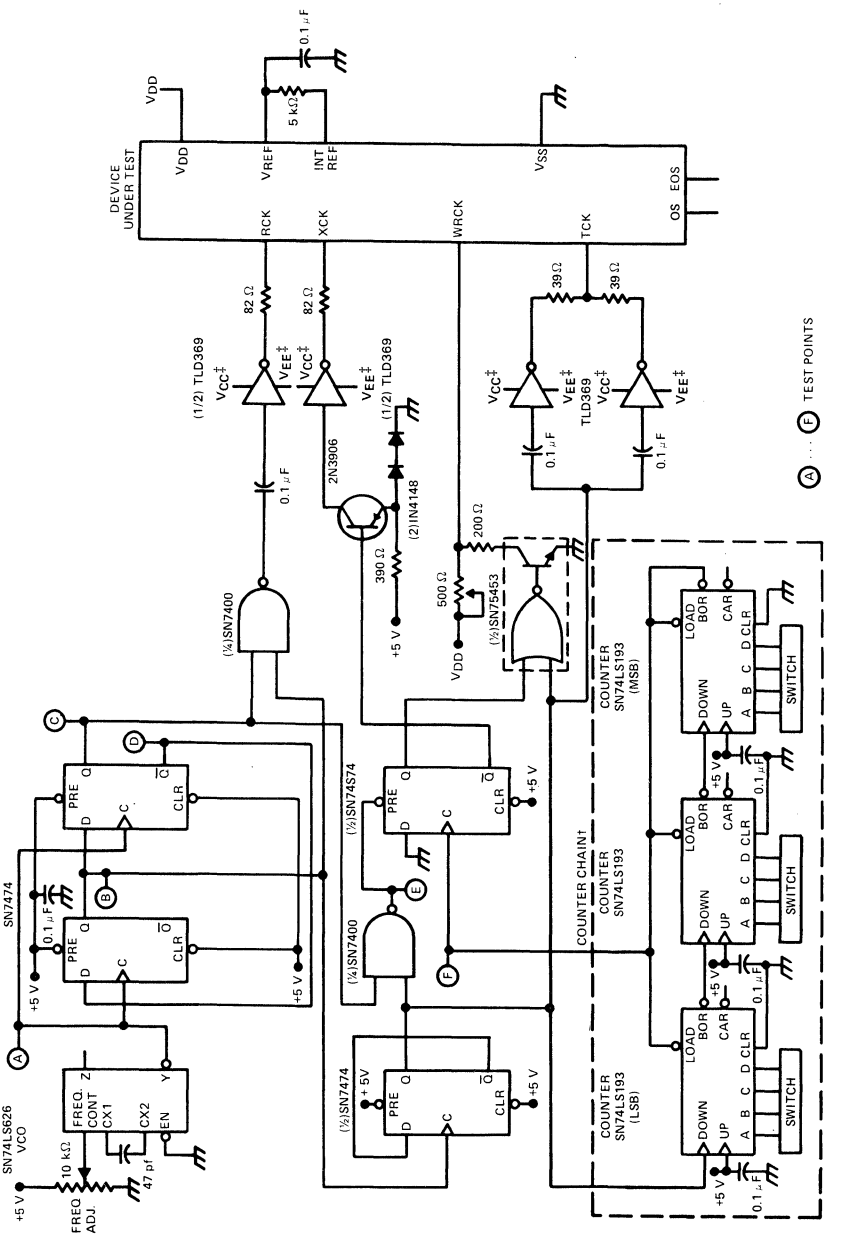


FIGURE 2—DEVICE TIMING REQUIREMENTS

PARAMETER MEASUREMENT INFORMATION



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3—DRIVER CIRCUIT FOR TESTING IMAGE SENSOR

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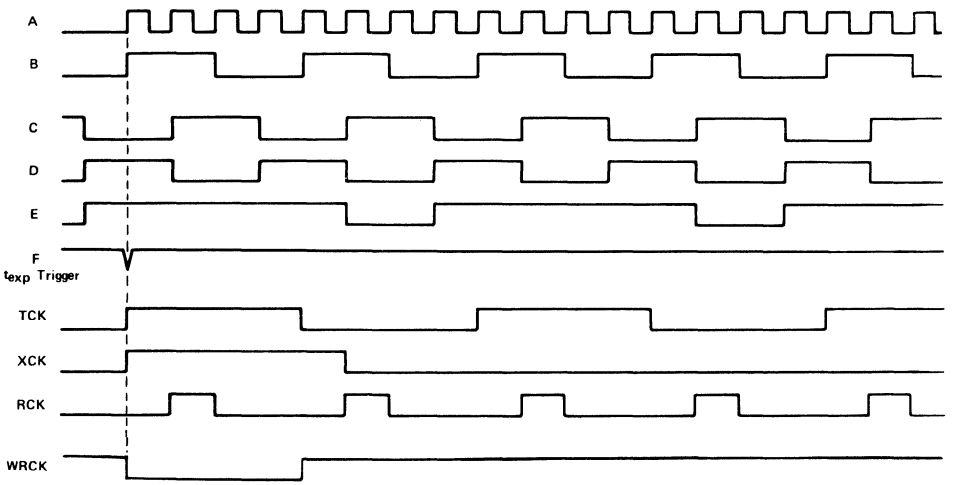

FIGURE 4 – WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

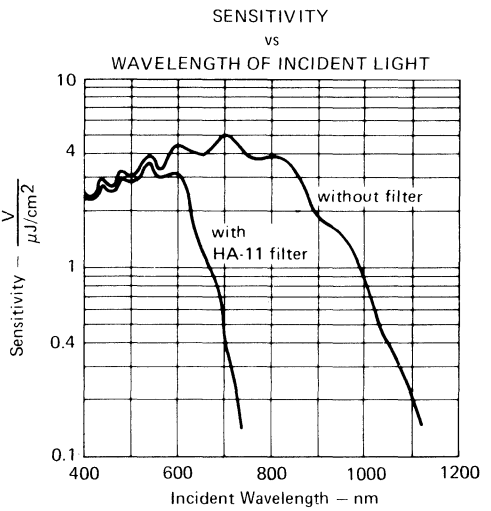

FIGURE 5

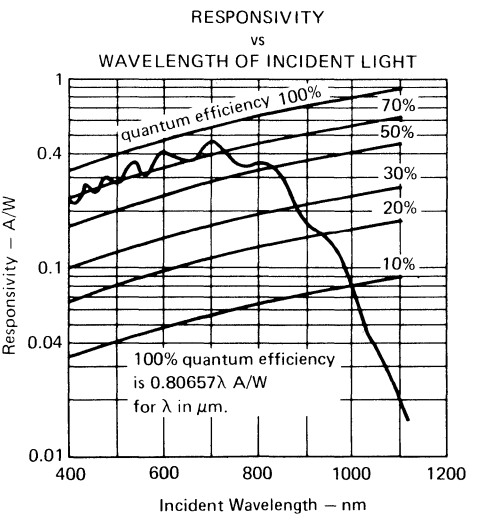

FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25 °C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

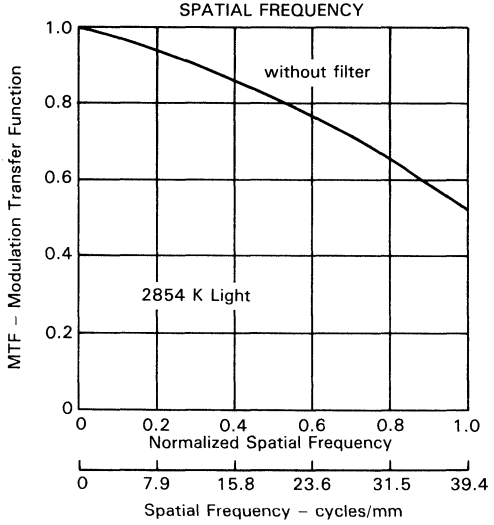

FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

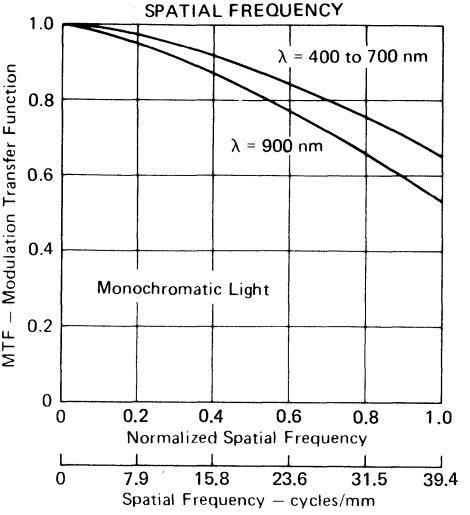

FIGURE 8

AVERAGE AND LOW FREQUENCY
DARK SIGNAL
vs
EXPOSURE TIME

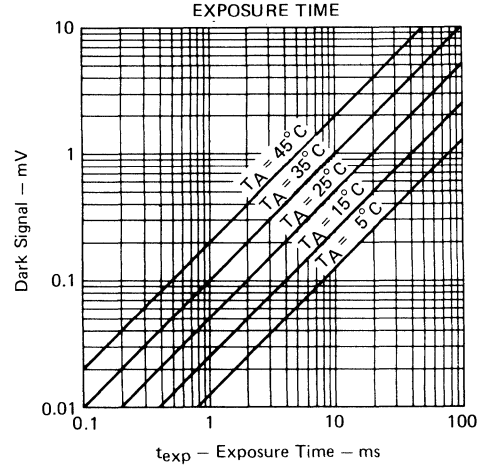

FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO
SATURATED OUTPUT VOLTAGE
vs
EXPOSURE TIME

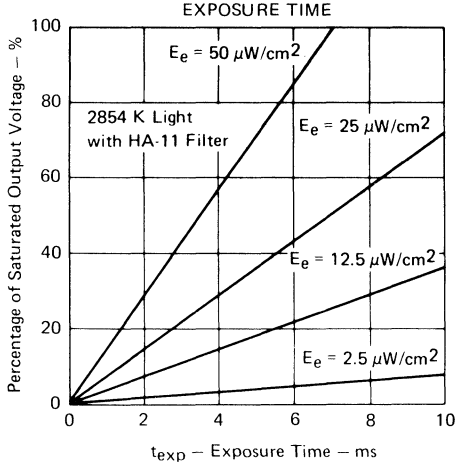

FIGURE 10

TEXAS INSTRUMENTS
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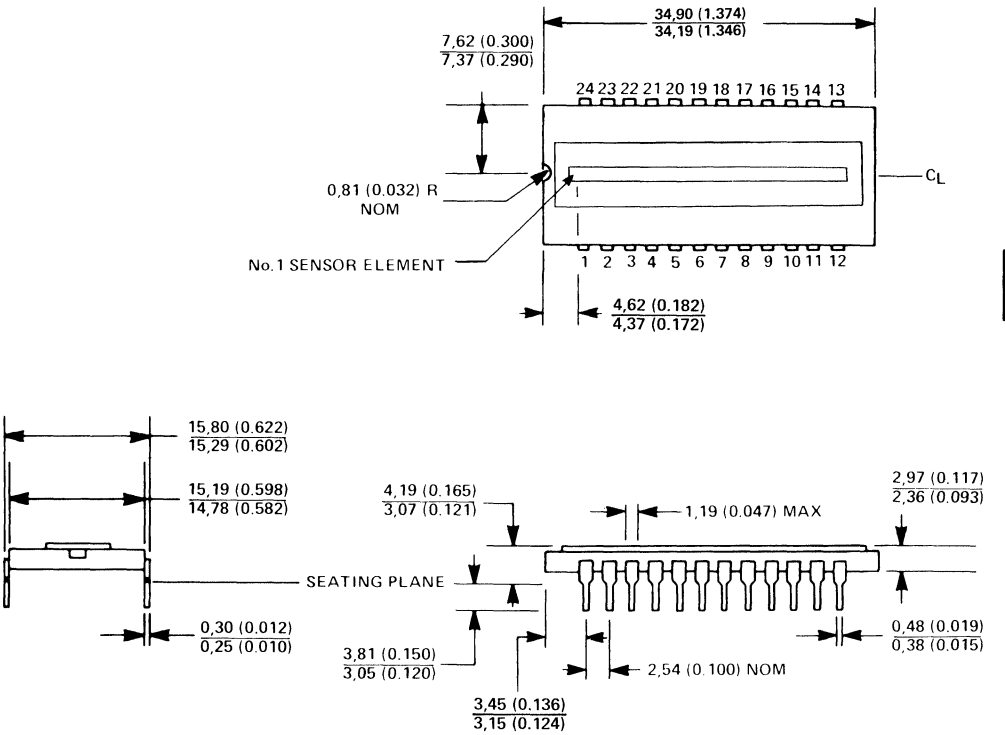
MECHANICAL DATA



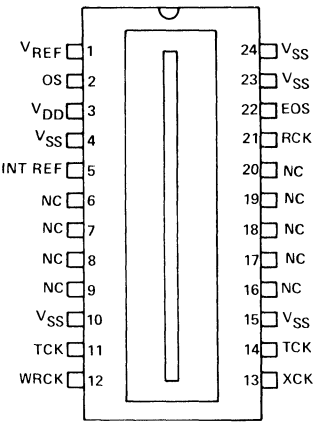
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE 1: The distance between the top surface of the window and the surface of the sensor is nominally 0,89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

D2686, DECEMBER 1983—REVISED JULY 1989

- 2048 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 1.0 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- OPTIONAL FEATURE: Internal Reference Voltage
- Same as TC103 Except for "White Reference Amplitude" and "End-of-Scan Amplitude" Specifications

TC103 . . . DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TC103-1, a 2048-element CCD line image sensor, functions in high-resolution image scanning applications such as facsimile and optical character recognition. The TC103-1 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability. The 2048 sensor elements provide a 8-points-per-inch resolution across 256 millimeters.

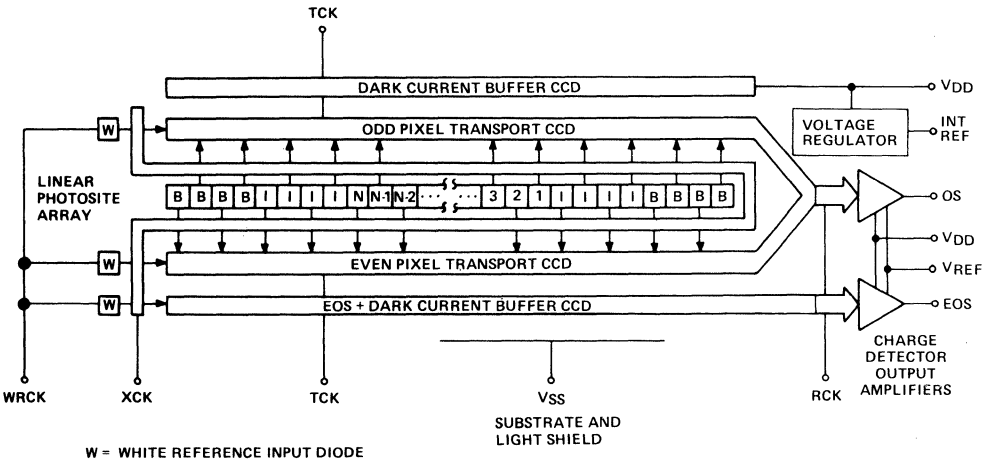
This device is supplied in a 24-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 15,2-mm (0,600-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

virtual phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. The virtual phase utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 2048 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers and internal reference.
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier.
3	V_{DD}	Supply Voltage	Output amplifier supply voltage.
4, 10, 15, 23, 24	V_{SS}	Substrate	All voltages are referenced to the substrate.
5	INT REF	Internal Reference	Potential derived internally for operational reference voltage.
6, 7, 8, 9, 16 17, 18, 19, 20	NC		No internal connection.
11, 14	TCK	Transport Clock	Drives the CCD transport registers.
12	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
13	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
21	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
22	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.

functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 2048 photo-sensitive areas, 12,7 micrometers (0.5 milliinches) square and approximately 12,7 micrometers from center to center. Image photons create electron/hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements, and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. Reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output, so no external current sink is needed. The output signal on pin 2 is a series of negative-going pulses on a dc level.

internal reference voltage

An internal reference voltage (INT REF) is available on the chip to provide the V_{REF} voltage. The required connections appear in Figure 3. If the internal reference voltage is not used, an external voltage is connected directly to pin 1. Pin 5 is then left unconnected.

resolution

The modulation transfer function decreases at longer wavelengths. (See Figures 7 and 8.) If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 2081 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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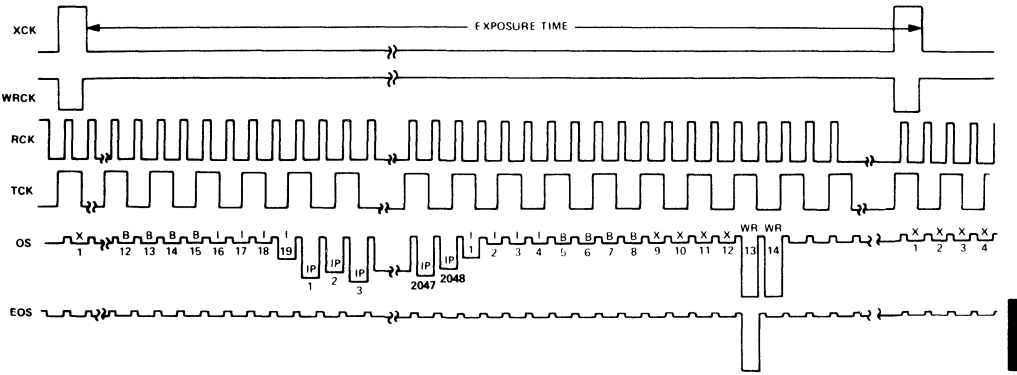


Output Signal (OS) pulse identification: I = isolation pixel, IP = Image pixel, B = Black reference pixel, WR = White reference pixel, X = empty pixel.

FIGURE 1—OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage (V_{DD1})	−0.3 V to 30 V
Transfer clock (XCK) voltage	−25 V to 5 V
Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25°C to 125°C
Operating free-air temperature	−25°C to 70°C

recommended operating conditions at T_A = 25°C (see Note 1)

		MIN	NOM	MAX	UNIT
V_{DD}	Amplifier supply voltage	13	14	15	V
$V_{IH(X)}$	Transfer clock high-level input voltage	3	4	5	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−15†	−14	−13	V
$V_{IH(T)}$	Transport clock high-level input voltage	3	4	5	V
$V_{IL(T)}$	Transport clock low-level input voltage	−15†	−14	−13	V
$V_{IH(R)}$	Reset clock high-level input voltage	3	4	5	V
$V_{IL(R)}$	Reset clock low-level input voltage	−15†	−14	−13	V
$V_{IH(WR)}$	White reference clock high-level input voltage	13	14	15	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)			10	MHz

†The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.
NOTE 1: Voltage values are with respect to V_{SS}.

electrical characteristics at 25°C free-air temperature¶

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low frequency component		0.5	5	mV
	Nonuniformity relative to average of adjacent pixels		1.0	20	
Sensitivity		2	3.5	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		50	100	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			1		mV
Equivalent exposure§ of peak-to-peak noise			0.35		nJ/cm²
Saturation exposure§			350		nJ/cm²
Saturation output amplitude		700	1000	1400	mV
Dynamic range relative to peak-to-peak noise†		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude			500		mV
End-of-scan amplitude			300		mV
Output offset (dc) voltage			7		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		150		kΩ
	Transport gate		500		
	Reset gate		500		
Amplifier reference voltage, V_{REF}			7		V
Capacitance to V_{SS}	Transfer gate		250		pF
	Transport gate		600		
	Reset gate		16		
Amplifier supply current			8	12	mA
Total power dissipation			110		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 700 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time
¶Test conditions are f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values using the internal reference voltage.

timing requirements

		MIN	NOM	MAX	UNITS
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge.	0		50	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge.	0		50	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge.	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock.	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge.	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge.	0		50	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse.	50			ns
t_r	rise time (all clocks)		15		ns
t_f	fall time (all clocks)		5		ns

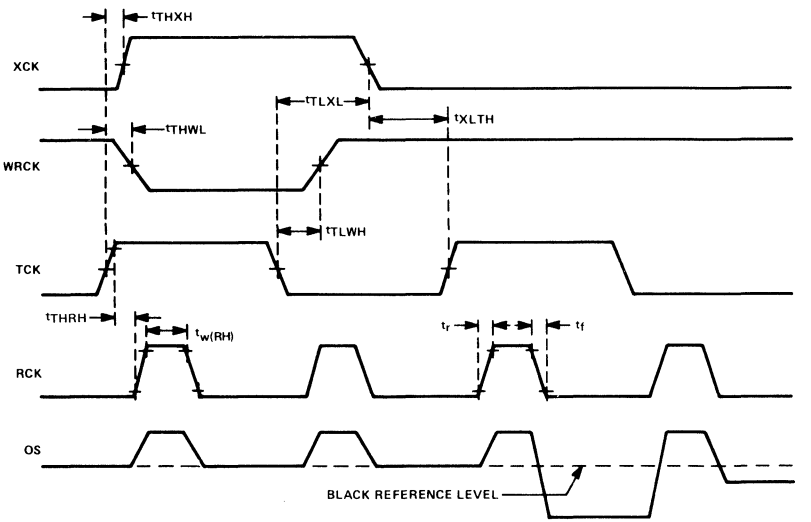
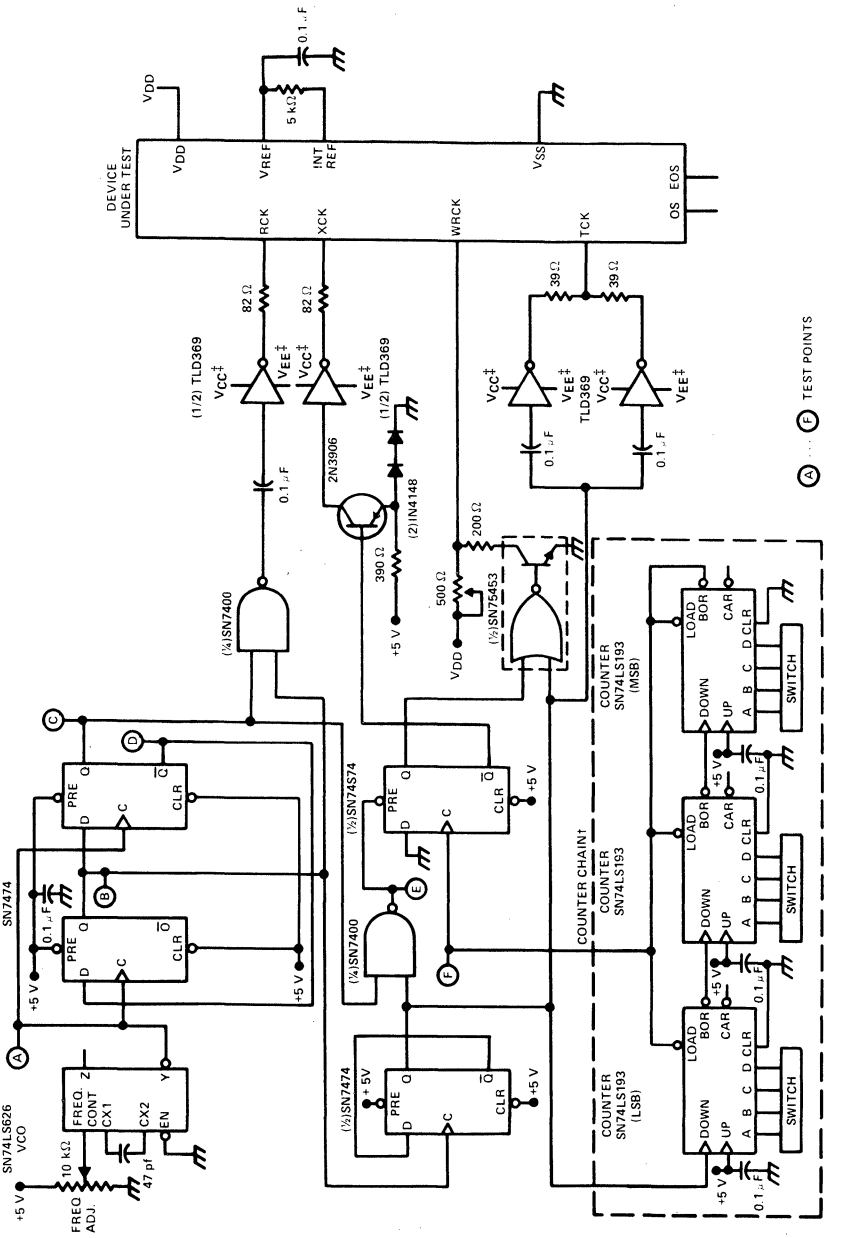


FIGURE 2—DEVICE TIMING REQUIREMENTS

PARAMETER MEASUREMENT INFORMATION



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3—DRIVER CIRCUIT FOR TESTING IMAGE SENSOR

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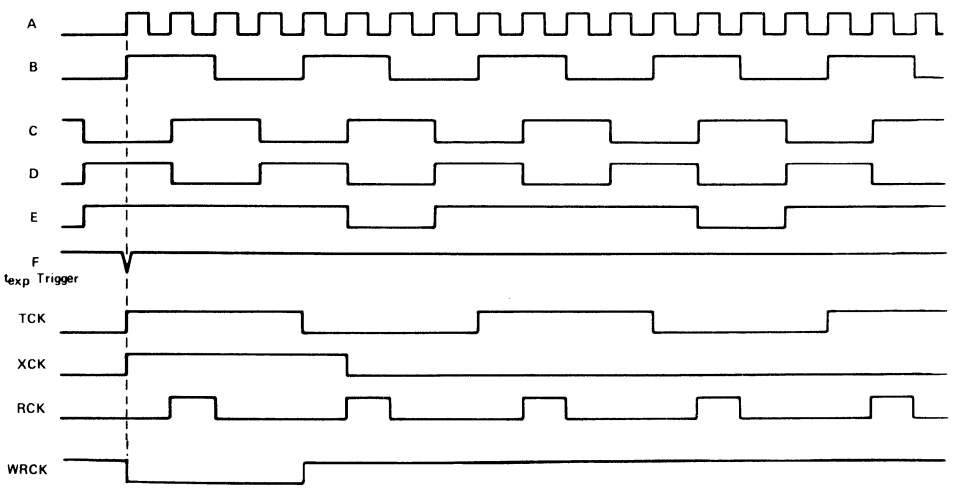

FIGURE 4 – WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25 °C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

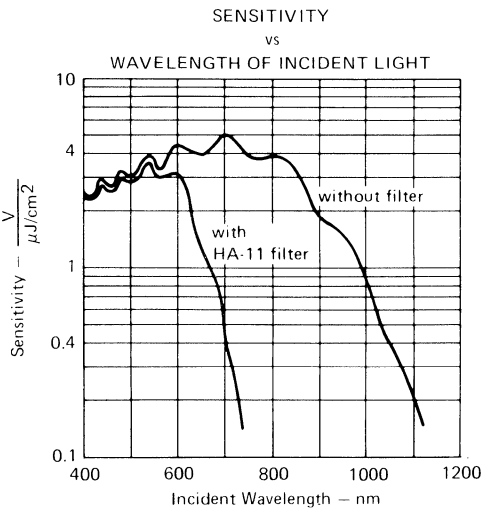

FIGURE 5

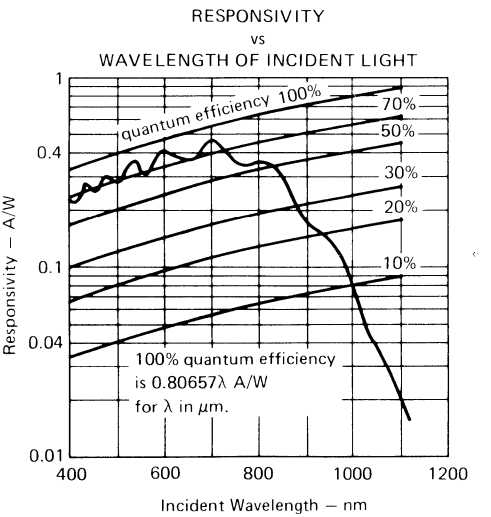

FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25 °C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

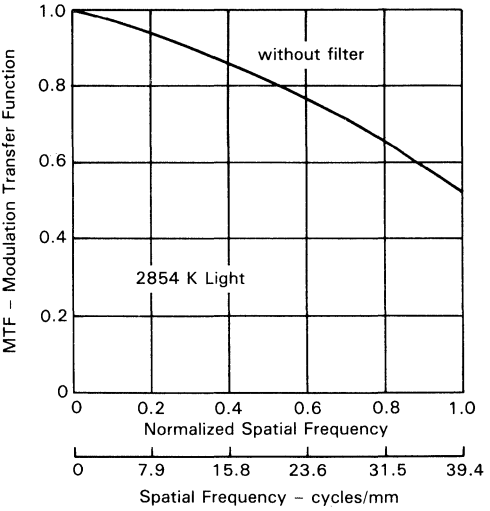

FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

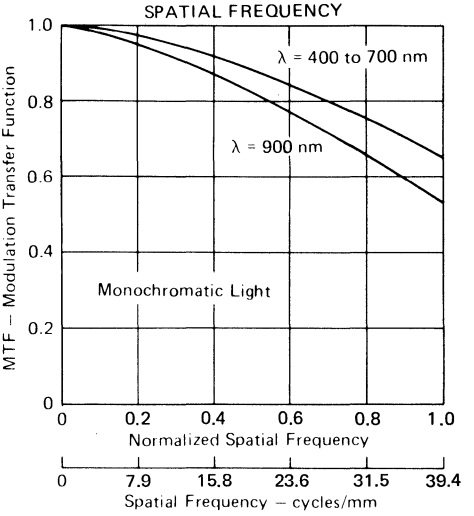

FIGURE 8

AVERAGE AND LOW FREQUENCY
DARK SIGNAL
vs
EXPOSURE TIME

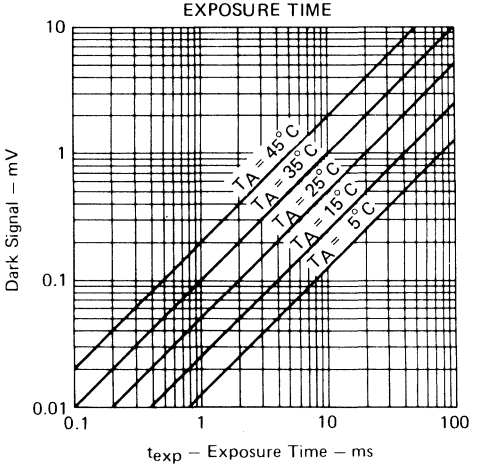

FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO
SATURATED OUTPUT VOLTAGE
vs
EXPOSURE TIME

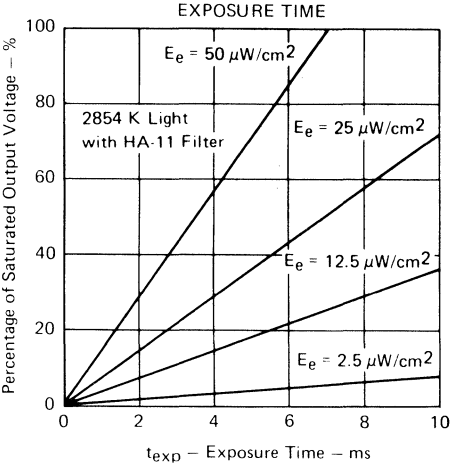

FIGURE 10

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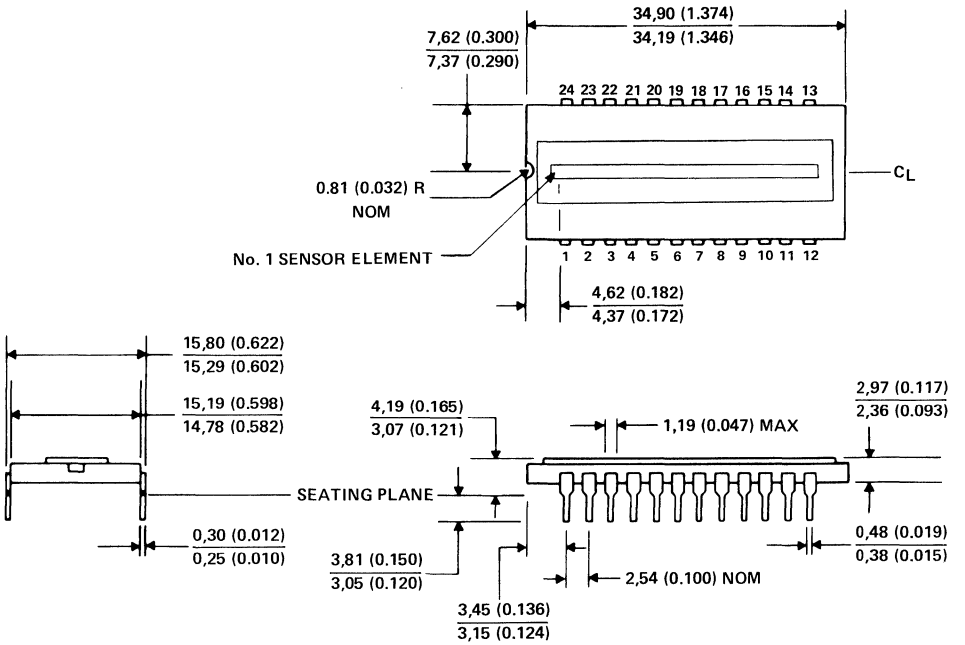
MECHANICAL DATA



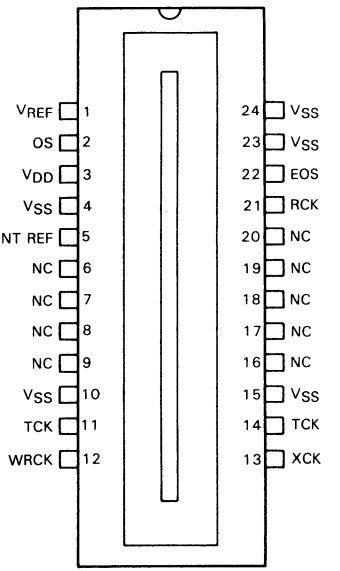
NOTE: The distance between the top surface of the window and the surface of the sensor is nominally 0.89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

D2687, FEBRUARY 1983—REVISED JULY 1989

- 3456 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 0.6 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- OPTIONAL FEATURE: Internal Reference Voltage

TC104 . . . DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC — No internal connection.

description

The TC104, a 3456-element CCD line image sensor, functions in high-resolution image scanning applications such as document reading and optical character recognition. The TC104 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability. The 3456 sensor elements provide 400 points-per-inch resolution across 8.5 inches.

This device is supplied in a 24-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 15.2-mm (0,600-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

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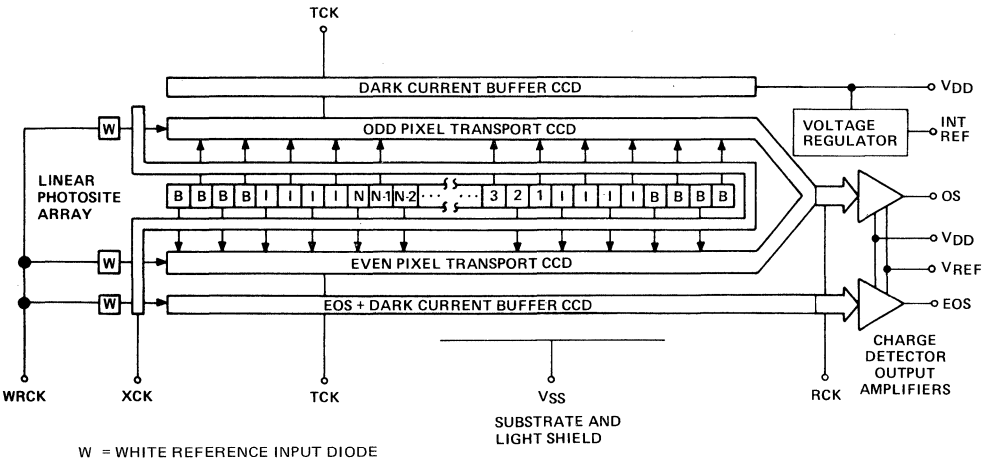
This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. The virtual phase utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



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6, 7, 8, 9, 16 17, 18, 19, 20	NC		No internal connection.
11, 14	TCK	Transport Clock	Drives the CCD transport registers.
12	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
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21	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
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functional description

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transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry. The white reference pulse amplitude is approximately 100% of the maximum output signal amplitude.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. Reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output, so no external current sink is needed. The output signal on pin 2 is a series of negative-going pulses on a dc level.

internal reference voltage

An internal reference voltage (INT REF) is available on the chip to provide the V_{REF} voltage. The required connections appear in Figure 3. If the internal reference voltage is not used, an external voltage is connected directly to pin 1. Pin 5 is then left unconnected.

resolution

The modulation transfer function decreases at longer wavelengths. (See Figures 7 and 8.) If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 3489 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

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The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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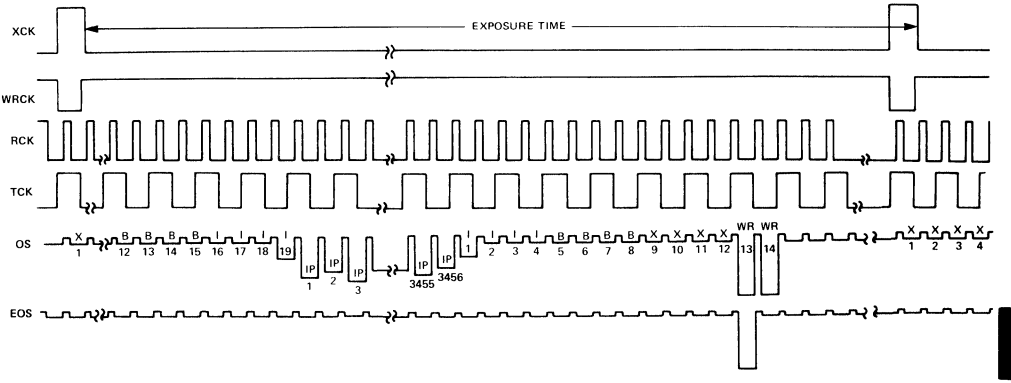


Output Signal (OS) pulse identification: I = Isolation pixel, IP = Image pixel, B = Black reference pixel, WR = White reference pixel, X = empty pixel.

FIGURE 1—OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage (V_{DD})	−0.3 V to 30 V
Transfer clock (XCK) voltage	−25 V to 5 V
Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25°C to 125°C
Operating free-air temperature	−25°C to 70°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions at T_A = 25°C (see Note 1)

		MIN	NOM	MAX	UNIT
V_{DD}	Amplifier supply voltage	13	14	15	V
$V_{IH(X)}$	Transfer clock high-level input voltage	3	4	5	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−15†	−14	−13	V
$V_{IH(T)}$	Transport clock high-level input voltage	3	4	5	V
$V_{IL(T)}$	Transport clock low-level input voltage	−15†	−14	−13	V
$V_{IH(R)}$	Reset clock high-level input voltage	3	4	5	V
$V_{IL(R)}$	Reset clock low-level input voltage	−15†	−14	−13	V
$V_{IH(WR)}$	White reference clock high-level input voltage	13	14	15	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)			8	MHz

†The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.
NOTE 1: Voltage values are with respect to V_{SS}.

electrical characteristics at 25 °C free-air temperature ¶

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low frequency component		0.5	5	mV
	Nonuniformity relative to average of adjacent pixels		4	20	
Sensitivity		1.4	2	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		30	60	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			0.6		mV
Equivalent exposure§ of peak-to-peak noise			0.3		nJ/cm²
Saturation exposure§			300		nJ/cm²
Saturation output amplitude		400	600	1200	mV
Dynamic range relative to peak-to-peak noise †		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude		400	600		mV
End-of-scan amplitude		200	350		mV
Output offset (dc) voltage			6		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		150		kΩ
	Transport gate		700		
	Reset gate		700		
Amplifier reference voltage, V_{REF}			7		V
Capacitance to V_{SS}	Transfer gate		400		pF
	Transport gate		900		
	Reset gate		16		
Amplifier supply current			8	12	mA
Total power dissipation			112		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 400 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time
¶Test conditions are f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values using the internal reference voltage.

timing requirements

		MIN	NOM	MAX	UNITS
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge.	0		50	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge.	0		50	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge.	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock.	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge.	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge.	0		50	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse.	50			ns
t_r	Rise time (all clocks)	15			ns
t_f	Fall time (all clocks)	5			ns

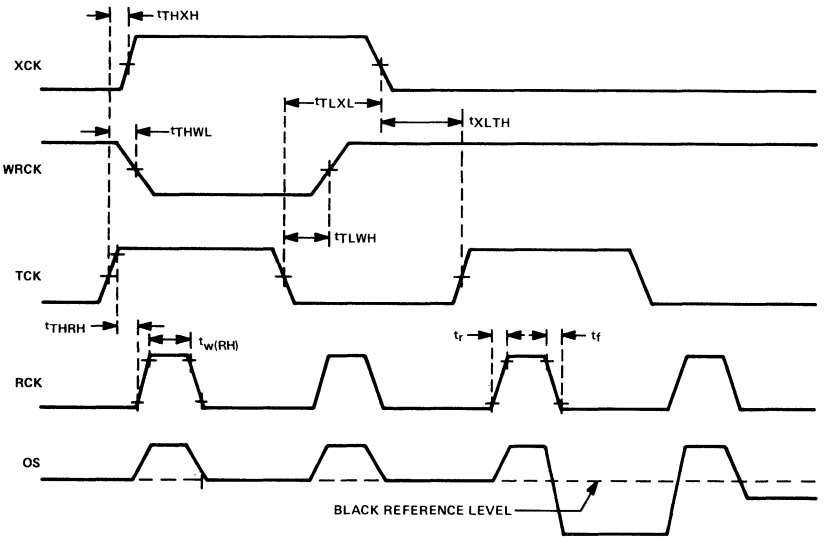
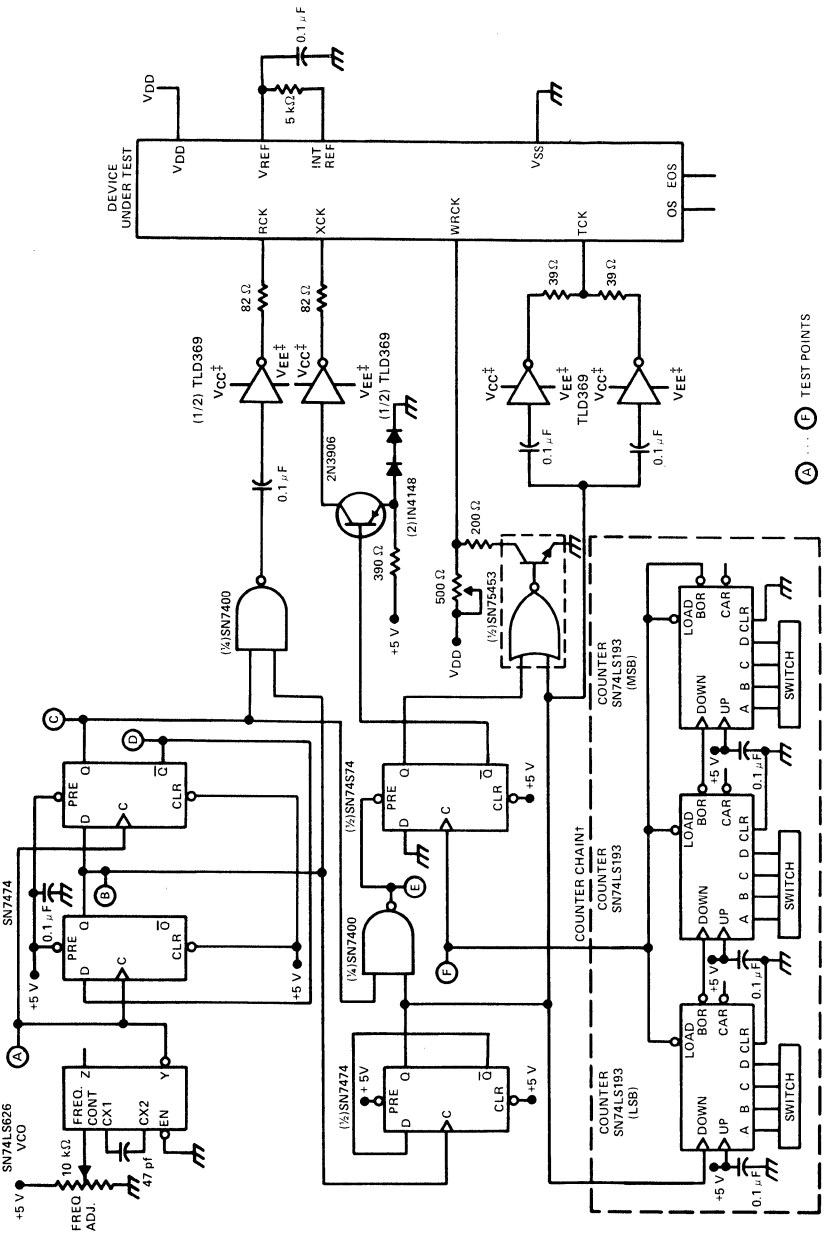


FIGURE 2—DEVICE TIMING REQUIREMENTS

PARAMETER MEASUREMENT INFORMATION



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3—DRIVER CIRCUIT FOR TESTING IMAGE SENSOR

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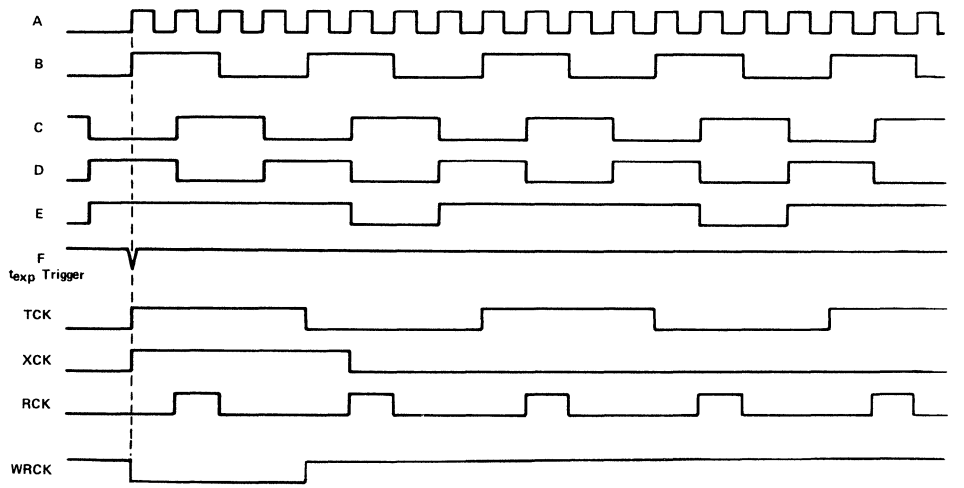

FIGURE 4 – WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25 °C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

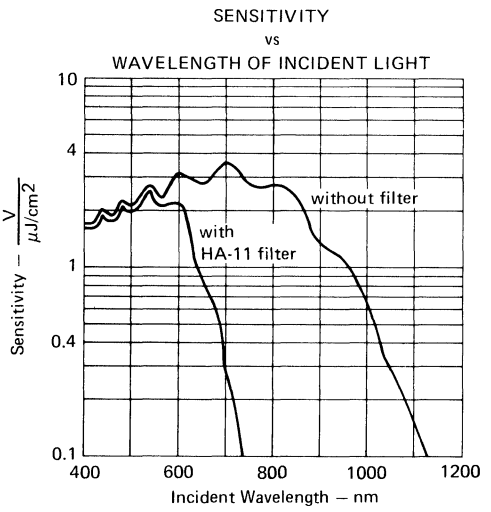

FIGURE 5

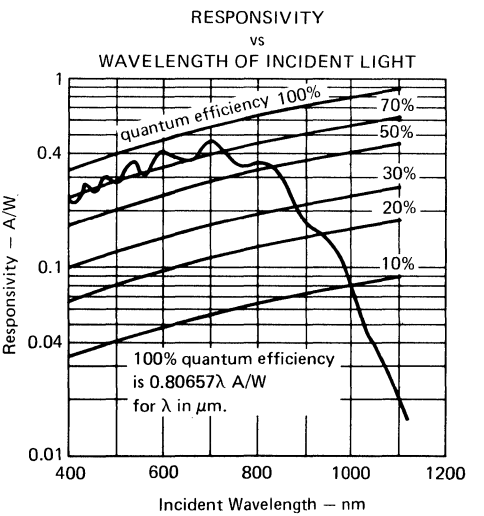

FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

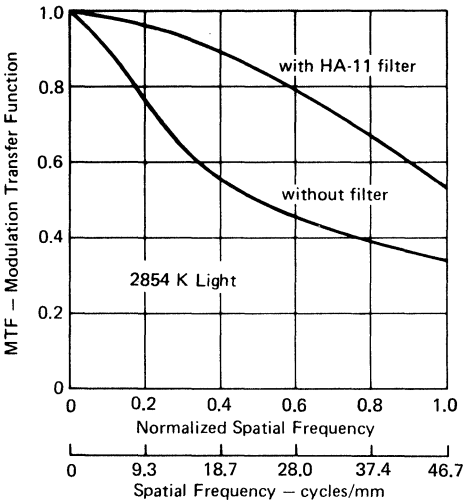

FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

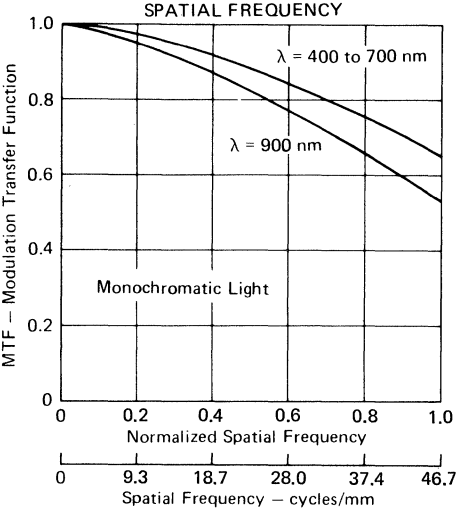

FIGURE 8

AVERAGE AND LOW FREQUENCY
DARK SIGNAL
vs
EXPOSURE TIME

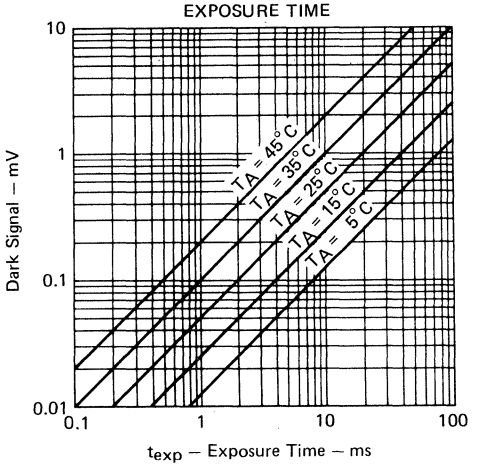

FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO
SATURATED OUTPUT VOLTAGE
vs
EXPOSURE TIME

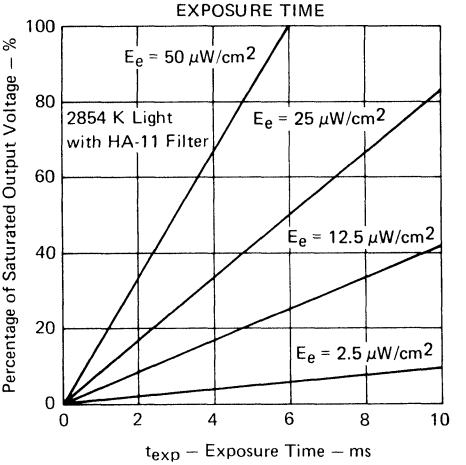

FIGURE 10

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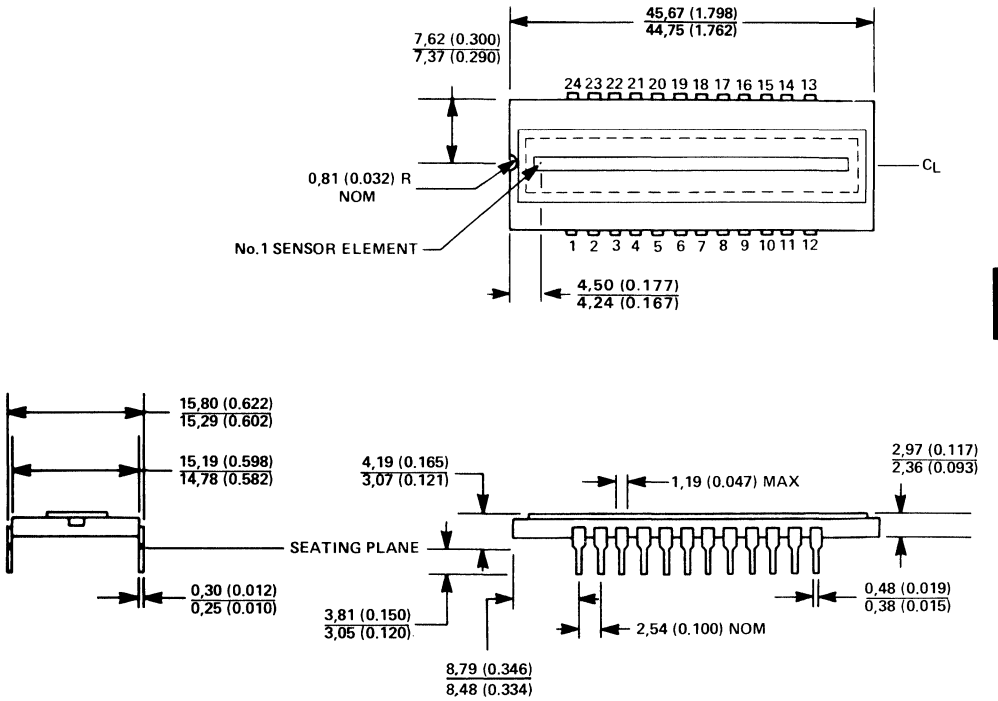
MECHANICAL DATA



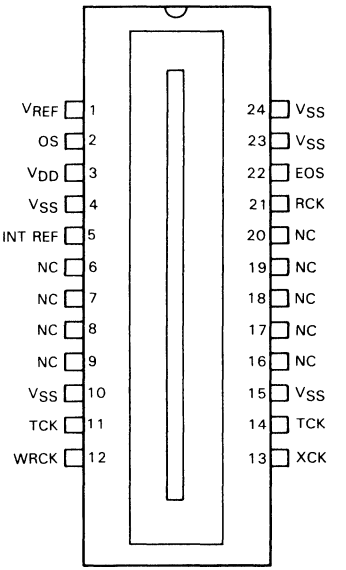
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE 1: The distance between the top surface of the window and the surface of the sensor is nominally 0,89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

D2687, DECEMBER 1983—REVISED JULY 1989

- 3465 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 0.6 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- OPTIONAL FEATURE: Internal Reference Voltage
- Same as TC104 Except for "White Reference Amplitude" and "End-of-Scan Amplitude" Specifications

TC104 . . . DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC — No internal connection.

description

The TC104-1, a 3456-element CCD line image sensor, functions in high-resolution image scanning applications such as document reading and optical character recognition. The TC104-1 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability. The 3456 sensor elements provide 400 points-per-inch resolution across 8.5 inches.

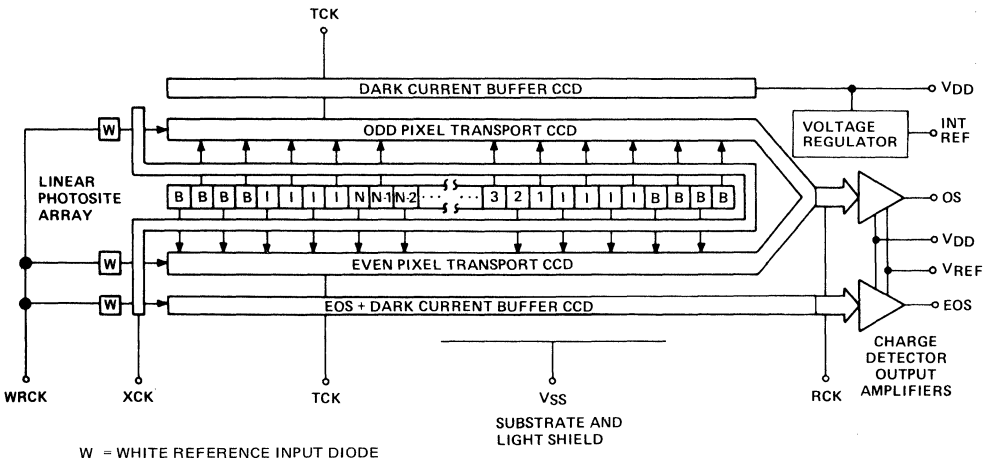
This device is supplied in a 24-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 15.2-mm (o,600-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive form during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

virtual phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. The virtual phase utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 3456 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers and internal reference.
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier.
3	V_{DD}	Supply Voltage	Output amplifier supply voltage.
4, 10, 15, 23, 24	V_{SS}	Substrate	All voltages are referenced to the substrate.
5	INT REF	Internal Reference	Potential derived internally for operational reference voltage.
6, 7, 8, 9, 16 17, 18, 19, 20	NC		No internal connection.
11, 14	TCK	Transport Clock	Drives the CCD transport registers.
12	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
13	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
21	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
22	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.

functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 3456 photo-sensitive areas, 10,7 micrometers (0.42 milliinches) square and approximately 10,7 micrometers from center to center. Image photons create electron/hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements, and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift registers. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan waveform. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. Reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output, so no external current sink is needed. The output signal on pin 2 is a series of negative-going pulses on a dc level.

internal reference voltage

An internal reference voltage (INT REF) is available on the chip to provide the V_{REF} voltage. The required connections appear in Figure 3. If the internal reference voltage is not used, an external voltage is connected directly to pin 1. Pin 5 is then left unconnected.

resolution

The modulation transfer function decreases at longer wavelengths. (See Figures 7 and 8.) If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 3489 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

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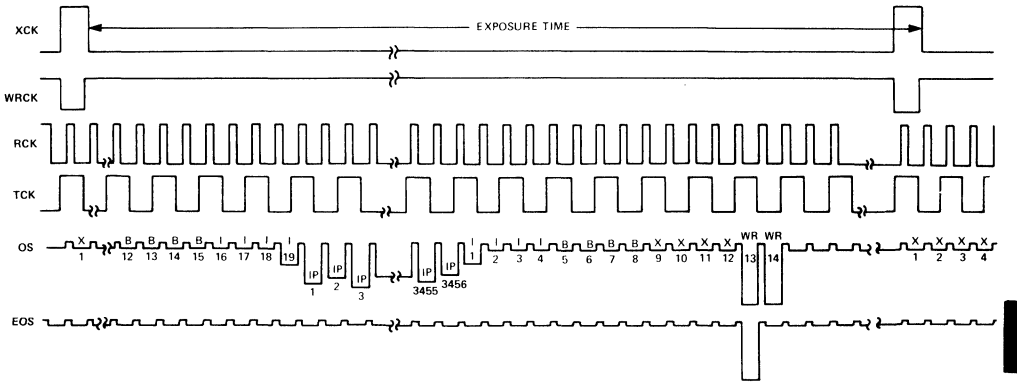

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Transport clock (TCK) voltage	−25 V to 5 V
Reset clock (RCK) voltage	−25 V to 5 V
White reference clock (WRCK) voltage	−0.3 V to 30 V
Storage temperature	−25°C to 125°C
Operating free-air temperature	−25°C to 70°C

NOTE 1: Voltage values are with respect to V_{SS}.

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$V_{IL(T)}$	Transport clock low-level input voltage	−15†	−14	−13	V
$V_{IH(R)}$	Reset clock high-level input voltage	3	4	5	V
$V_{IL(R)}$	Reset clock low-level input voltage	−15†	−14	−13	V
$V_{IH(WR)}$	White reference clock high-level input voltage	13	14	15	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)			8	MHz

†The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.
NOTE 1: Voltage values are with respect to V_{SS}.

electrical characteristics at 25 °C free-air temperature ¶

PARAMETER		MIN	TYP	MAX	UNIT
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Output amplitude variation (PRNU)‡	Peak-to-peak		30	60	mV
	Adjacent pixels from alternate registers (imbalance)		10		
Peak-to-peak noise			0.6		mV
Equivalent exposure§ of peak-to-peak noise			0.3		nJ/cm²
Saturation exposure§			300		nJ/cm²
Saturation output amplitude		400	600	1200	mV
Dynamic range relative to peak-to-peak noise †		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude			400		mV
End-of-scan amplitude			200		mV
Output offset (dc) voltage			6		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		150		kΩ
	Transport gate		700		
	Reset gate		700		
Amplifier reference voltage, V_{REF}			7		V
Capacitance to V_{SS}	Transfer gate		400		pF
	Transport gate		900		
	Reset gate		16		
Amplifier supply current			8	12	mA
Total power dissipation			112		mW

†Dynamic range = saturation output amplitude/standard deviation peak-to-peak noise.
‡Measured at 400 mV output amplitude with an f/2.8 lens.
§Exposure = intensity x time
¶Test conditions are f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values using the internal reference voltage.

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timing requirements

		MIN	NOM	MAX	UNITS
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge.	0		50	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge.	0		50	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge.	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock.	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge.	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge.	0		50	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse.	50			ns
t_r	Rise time (all clocks)	15			ns
t_f	Fall time (all clocks)	5			ns

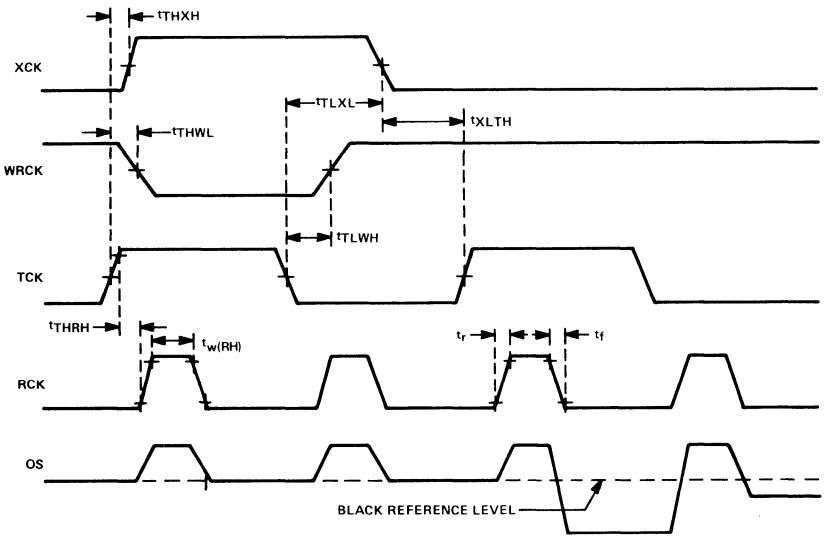
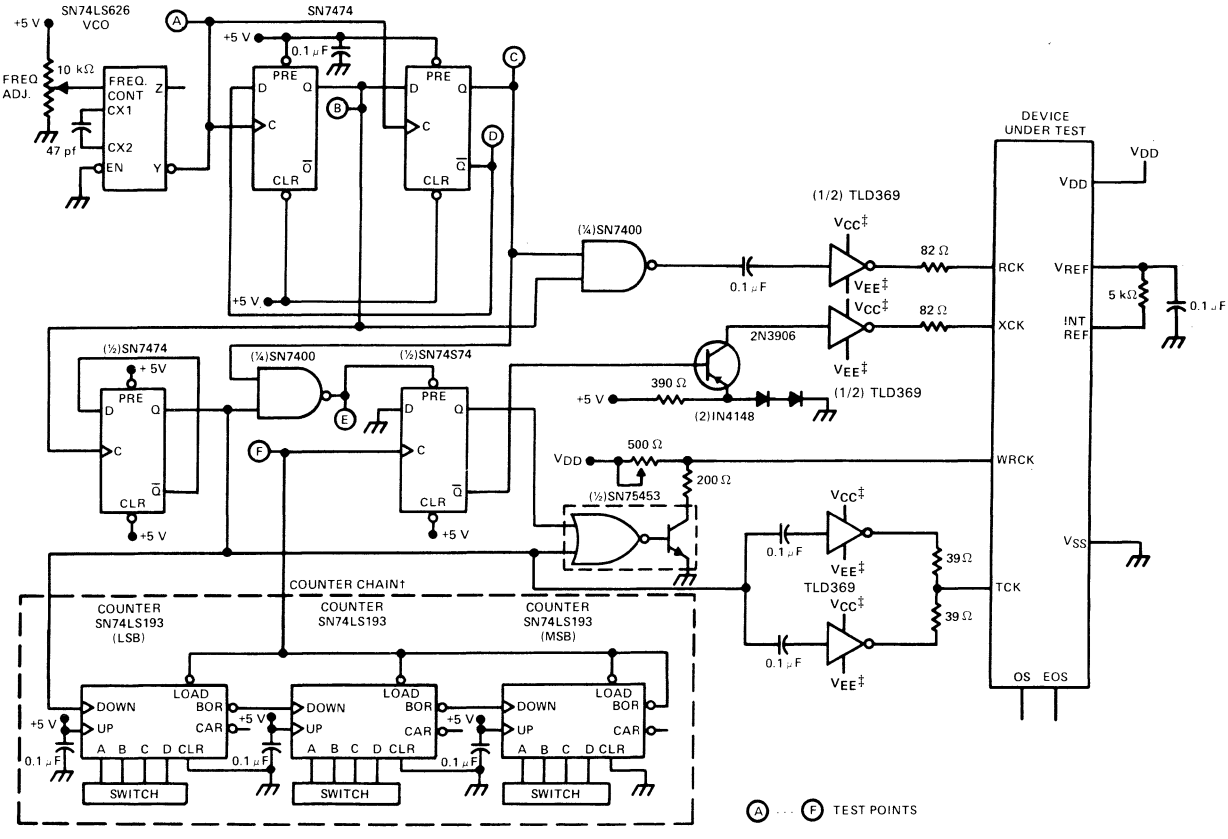


FIGURE 2—DEVICE TIMING REQUIREMENTS



†This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3—DRIVER CIRCUIT FOR TESTING IMAGE SENSOR

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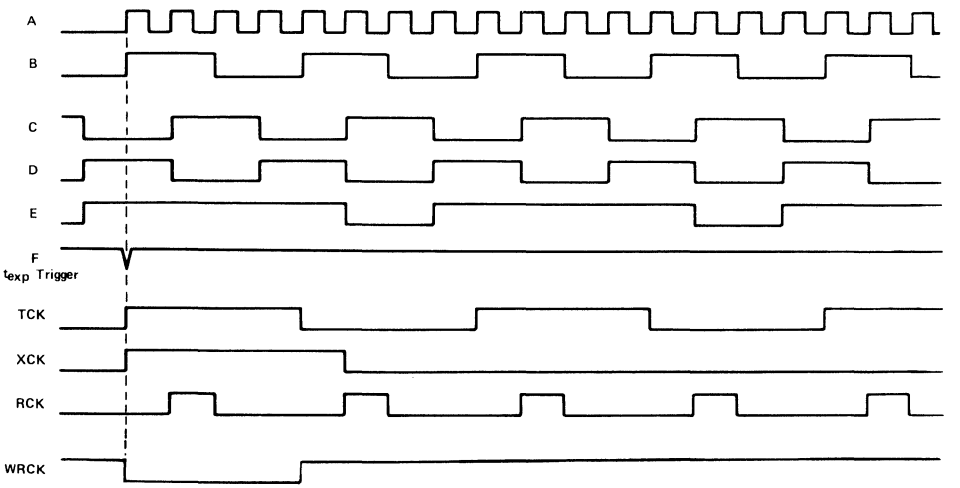


FIGURE 4 — WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25 °C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

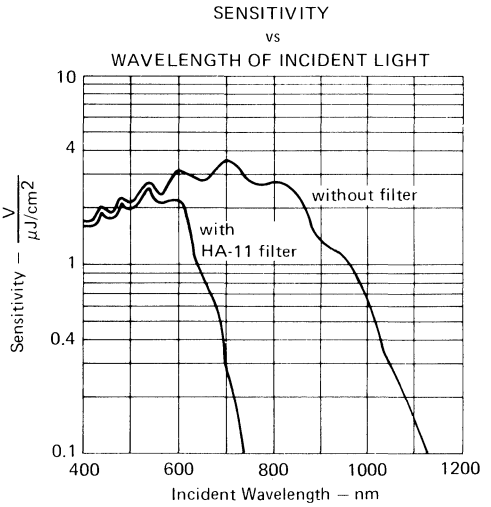


FIGURE 5

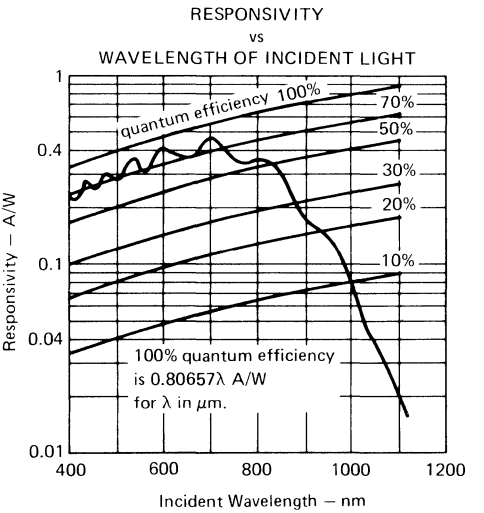


FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

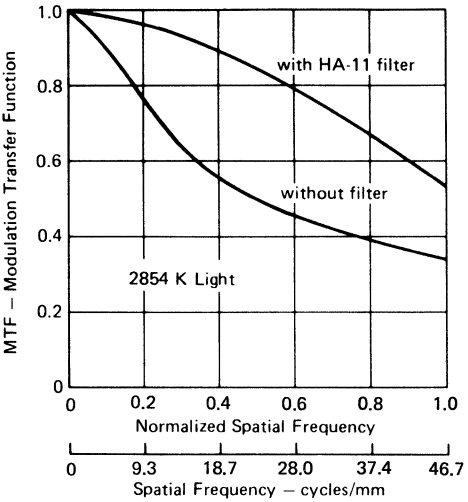


FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

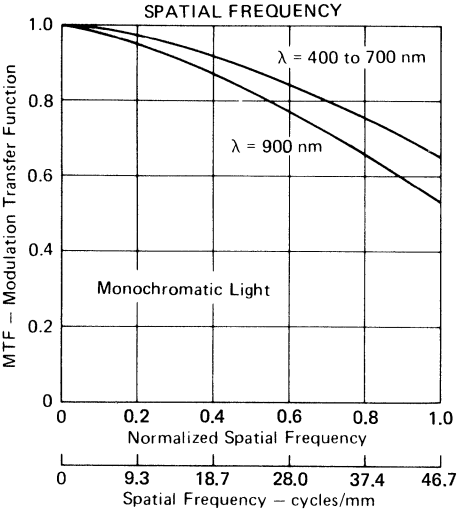


FIGURE 8

AVERAGE AND LOW FREQUENCY
DARK SIGNAL
vs
EXPOSURE TIME

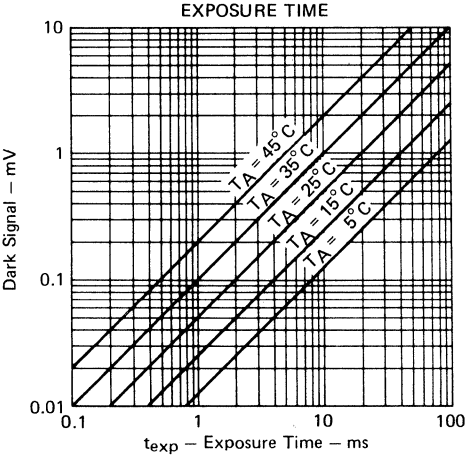


FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO
SATURATED OUTPUT VOLTAGE
vs
EXPOSURE TIME

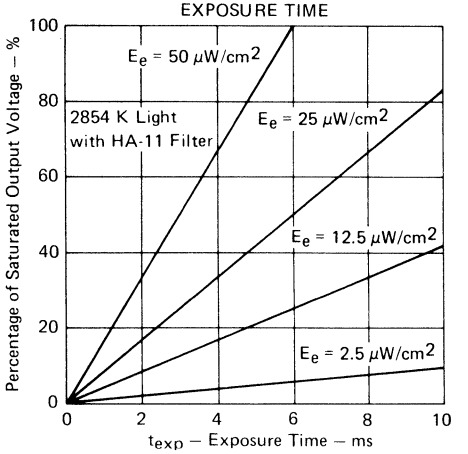
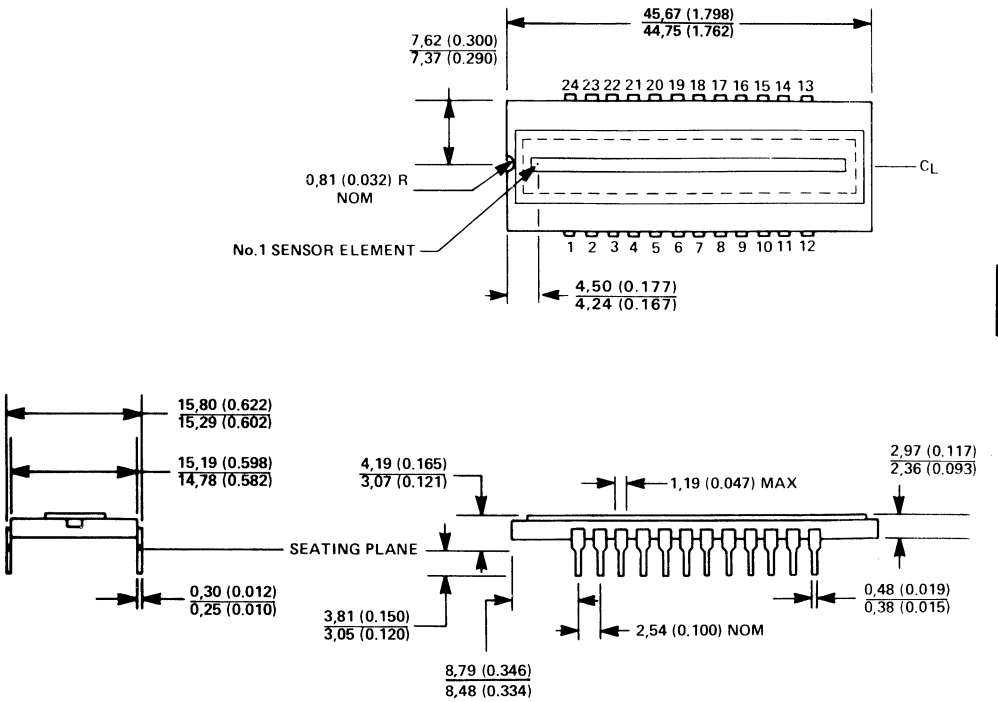


FIGURE 10

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

MECHANICAL DATA



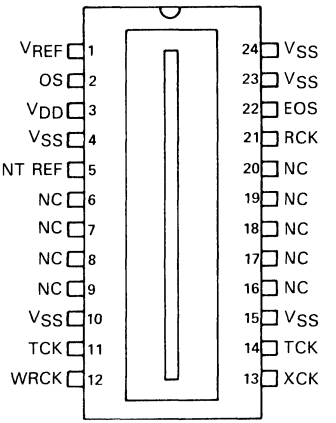
NOTE: The distance between the top surface of the window and the surface of the sensor is nominally 0,89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

D2992, SEPTEMBER 1986—REVISED JULY 1989

- 2592 x 1 Sensor Element Organization
- Virtual-Phase N-Channel Silicon MOS Technology
- High Quantum Efficiency
- Enhanced Blue Response
- Output Signal Approximately 0.6 Volt Peak-to-Peak
- Dynamic Range Relative to Peak-to-Peak Noise Typically 1000:1
- End-of-Scan Signal
- Internal Black and White References
- Simple and Stable Operation
- Optional Feature:
  Internal Reference Voltage

TC106-1 . . . DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TC106-1, a 2592-element CCD line image sensor, functions in high-resolution image scanning applications such as document reading and optical character recognition. The TC106-1 incorporates virtual-phase MOS technology, which provides simplified operation and high reliability. The 2592 sensor elements provide 300 points-per-inch resolution across 8.5 inches.

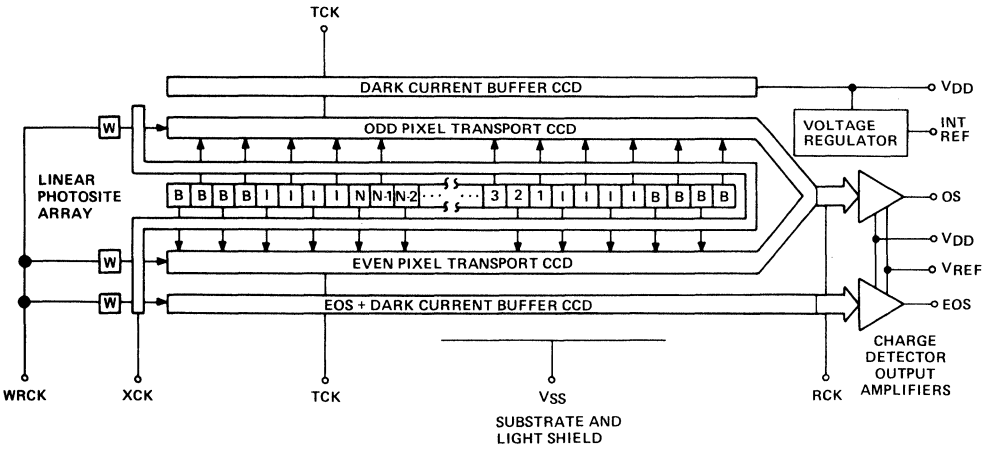
This device is supplied in a 24-pin dual-in-line ceramic side-braze package designed for insertion in mounting-hole rows on 15.2-mm (0,600-inch) centers. The glass window may be cleaned by wiping with a cotton swab soaked in alcohol.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive form during storage or handling to prevent electrostatic damage to the MOS gates. Avoid shorting either OS or EOS to V_{SS} during operation to prevent damage to the amplifiers.

virtual phase technology

This patented design results in simplified clocking circuits, reduced noise, and greater light sensitivity. The virtual phase utilizes a junction-gate region at the substrate dc potential. This accomplishes the same gating and transport function as a separate gate electrode requiring multiple layers and multiple process steps common in other device designs. The resulting simplicity of process and ease of operation will increase performance and reliability for the user.

functional block diagram



W = WHITE REFERENCE INPUT DIODE
B = BLACK REFERENCE ELEMENT
I = ISOLATION ELEMENT
N = 2592 SENSOR ELEMENTS

PIN FUNCTIONAL DESCRIPTION

PIN NUMBER	SIGNATURE	NAME	DESCRIPTION
1	V_{REF}	Reference Voltage	Bias input for the output amplifiers and internal reference
2	OS	Output Signal	Video output from a cascaded source-follower MOS amplifier
3	V_{DD}	Supply Voltage	Output amplifier supply voltage
4, 10, 15, 23, 24	V_{SS}	Substrate	All voltages are referenced to the substrate
5	INT REF	Internal Reference	Potential derived internally for operational reference voltage
6, 7, 8, 9, 16 17, 18, 19, 20	NC		No internal connection
11, 14	TCK	Transport Clock	Drives the CCD transport registers
12	WRCK	White Reference Clock	Injects a controlled charge into the white reference CCD shift register elements to become white-reference and end-of-scan pulses.
13	XCK	Transfer Clock	Controls the transfer of charge packets from sensor elements to shift registers. The interval between pulses of the transfer clock determines the exposure time.
21	RCK	Reset Clock	Controls recharging of the charge-detection diodes in the output amplifiers, and clocks the output shift registers where the odd and even signals have been merged.
22	EOS	End-of-Scan Pulse	Indicates that all charge packets have been shifted out of the transport registers.

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functional description

image sensor elements

The line of sensor elements (also called photosites or pixels) consists of 2592 photo-sensitive areas, 10.7 micrometers (0.42 milliinches) square and 10.7 micrometers from center to center. Image photons create electron/hole pairs in the single-crystal silicon. The electrons are collected in the sensor elements, and the holes are swept into the substrate. The amount of charge accumulated in each element is a linear function of the incident light and the exposure time. The output signal charge will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

transfer gate

This structure is adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred into the transfer gate storage well when the transfer gate voltage goes high. When the transfer gate voltage goes low, the charge is transferred into the CCD transport shift register. The transfer gate also controls the exposure time for the sensor elements and permits charges to enter the end-of-scan (EOS) shift registers to create the end-of-scan signal. In addition, the transfer gate permits entry of charge packets to the transport CCD shift register to create the white reference signals.

shift registers

There are two CCD transport registers, one on each side of the line of image sensor elements and outside of the transfer gate. Alternate charge packets are transferred to the CCD transport shift registers and moved serially to the output amplifier. The phase relationship of the reset clock and the transport clock and the geometric layout of the paths provide for alternate delivery of charge packets to re-establish the original sequence of the linear image data. The two outer buffer CCD shift registers protect the signal charges in the inner transport CCD shift registers from peripherally generated dark current noise.

black and white reference elements

Four additional sensor elements at each end of the sensor element array (labelled "B" in the block diagram) are covered by opaque metallization. They provide a black (no illumination) signal reference that is delivered at each end of the linear image output signal. Also included on the transport CCD shift register, at the opposite end from the amplifier, is an input diode that provides two white reference pulses in the output signal. The reference pulses are useful as inputs to external dc restoration and/or automatic exposure control circuitry.

output signal amplifier

The charge packets are transported to a precharge diode whose potential changes linearly in response to the amount of the signal charge delivered. This potential is applied to the input gate of an N-channel MOS double-source-follower amplifier to produce an output signal (OS). A reset transistor, driven by the reset clock (RCK), recharges the charge-detector-diode capacitance before the arrival of each new signal charge packet from the CCD shift registers. Reference voltage (V_{REF}) is applied to the drain of the reset transistor and acts to bias the OS and EOS amplifiers. A current sink is used as an on-chip load for the amplifier output, so no external current sink is needed. The output signal on pin 2 is a series of negative-going pulses on a dc level.

internal reference voltage

An internal reference voltage (INT REF) is available on the chip to provide the V_{REF} voltage. The required connections appear in Figure 3. If the internal reference voltage is not used, an external voltage is connected directly to pin 1. Pin 5 is then left unconnected.

resolution

The modulation transfer function decreases at longer wavelengths. (See Figures 7 and 8.) If optimum resolution is required with a light source that has a significant infrared component, then the designer must use appropriate filters to restrict the optical pass band to shorter wavelengths.

end-of-scan amplifier

The EOS amplifier is similar to the OS amplifier. XCK transfers charge from the input diode into the EOS register where it is transported at the TCK clock frequency to the EOS amplifier. This EOS pulse is coincident with the first of the two white reference pulses that pass through the odd and even transport CCDs, respectively. The EOS output can be used to alert the external circuitry that the linear image data readout has been completed.

clocks

The transfer clock (XCK) pulse controls the exposure time of the sensor elements. The minimum exposure time is the time required to shift the entire contents of the transport registers to the output signal amplifier and equals 2625 multiplied by the RCK period. The maximum exposure time is determined by the tolerable level of dark signal.

The transport clock (TCK) transports the linear image signal charge from the sensor element region to the output amplifier.

The reset clock (RCK) operates at twice the transport clock frequency so as to recombine the signal charge in the original sequence and present the charge to the output amplifier. The data rate is equal to the reset clock frequency.

The white reference clock (WRCK) runs at the transfer clock frequency and generates the white reference and the end-of-scan pulses. These pulses can be eliminated by connecting WRCK to V_{DD}. Transients on WRCK going below zero volts will cause charge injection resulting in an increase in apparent dark signal.

Figure 3 presents a suggested circuit for generating the clock waveforms. The RCK clock generator runs continuously. A binary divider halves the frequency to create TCK. After all signal charges have been transported to the output amplifier, TCK continues to run to keep thermally generated charges from accumulating in the transport registers.

The XCK and WRCK clock frequencies are submultiples of the TCK frequency. Figure 2 details the timing relationships among the different clock pulses.

TEXAS INSTRUMENTS
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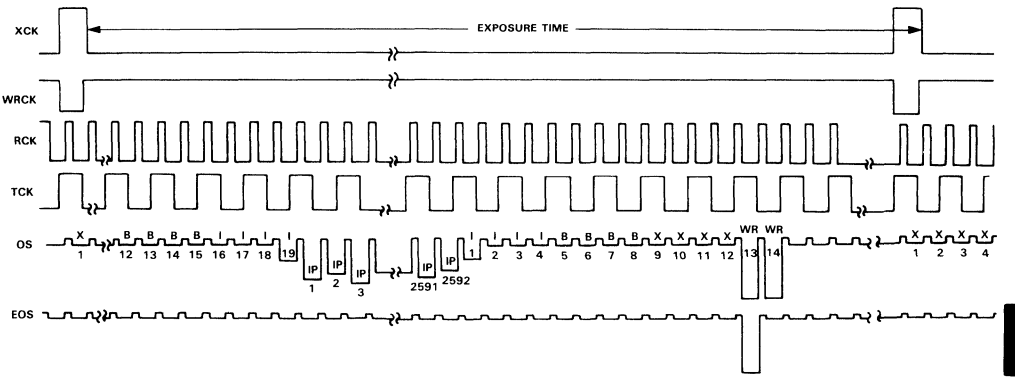


Output Signal (OS) pulse identification: I = Isolation pixel, IP = Image pixel, B = Black reference pixel, WR = White reference pixel, X = Empty pixel.

FIGURE 1. OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)

Amplifier drain voltage range (V_{DD})	−0.3 V to 30 V
Transfer clock (XCK) voltage range	−25 V to 5 V
Transport clock (TCK) voltage range	−25 V to 5 V
Reset clock (RCK) voltage range	−25 V to 5 V
White reference clock (WRCK) voltage range	−0.3 to 30 V
Storage temperature range	−25°C to 125°C
Operating free-air temperature range	−25°C to 70°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions at T_A = 25°C (see Note 2)

		MIN	NOM	MAX	UNIT
V_{DD}	Amplifier supply voltage	13	14	15	V
$V_{IH(X)}$	Transfer clock high-level input voltage	3	4	5	V
$V_{IL(X)}$	Transfer clock low-level input voltage	−15†	−14	−13	V
$V_{IH(T)}$	Transport clock high-level input voltage	3	4	5	V
$V_{IL(T)}$	Transport clock low-level input voltage	−15†	−14	−13	V
$V_{IH(R)}$	Reset clock high-level input voltage	3	4	5	V
$V_{IL(R)}$	Reset clock low-level input voltage	−15†	−14	−13	V
$V_{IH(WR)}$	White reference clock high-level input voltage	13	14	15	V
$V_{IL(WR)}$	White reference clock low-level input voltage	6	7	8	V
f_{RCK}	Reset clock frequency (output data rate)			8	MHz

NOTE 2: The algebraic convention, in which the more negative limit is designated as minimum, is used in this data sheet for clock voltage levels only.

electrical characteristics at 25°C free-air temperature†

PARAMETER		MIN	TYP	MAX	UNIT
Dark-signal amplitude	Average		0.5	10	mV
	Low-frequency component		0.5	5	mV
	Nonuniformity relative to average of adjacent pixels		4	20	mV
Sensitivity		1.4	2	5	V/(μJ/cm²)
Output amplitude variation (PRNU)‡	Peak-to-peak		30	60	mV
	Adjacent pixels from alternate registers (imbalance)		10		mV
Peak-to-peak noise			0.6		mV
Equivalent exposure§ of peak-to-peak noise			0.3		nJ/cm²
Saturation exposure§			300		nJ/cm²
Saturation output amplitude		400	600	**1200**	mV
Dynamic range relative to peak-to-peak noise¶		500:1	1000:1		
Charge transfer efficiency			0.99999		
White reference amplitude			400		mV
End-of-scan amplitude			200		mV
Output offset (dc) voltage			6		V
Output impedance			1		kΩ
Resistance to V_{SS}	Transfer gate		50		kΩ
	Transport gate		250		kΩ
	Reset gate		250		kΩ
Amplifier reference voltage, V_{REF}			7		V
Capacitance to V_{SS}	Transfer gate		400		pF
	Transport gate		900		pF
	Reset gate		16		pF
Amplifier supply current			8	12	mA
Total power dissipation			112		mW

† Test conditions are f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, tungsten light source operating at color temperature of 2854 K with 2.0-mm-thick Fish-Schurman HA-11 IR-absorbing filter, and all operating voltages at nominal recommended values using the internal reference voltage.
‡ Measured at 400 mV output amplitude with an f/2.8 lens.
§ Exposure = intensity x time
¶ Dynamic Range = saturation output amplitude/standard deviation peak-to-peak noise.

timing requirements

		MIN	NOM	MAX	UNIT
t_{THXH}	Time delay from the transport clock rising edge to the transfer clock rising edge	0		50	ns
t_{THWL}	Time delay from the transport clock rising edge to the white reference clock falling edge	0		50	ns
t_{THRH}	Time delay from the transport clock rising edge to the reset clock rising edge	0			ns
$t_{w(RH)}$	Pulse duration of the high state for the reset clock	40			ns
t_{TLXL}	Time delay from the transport clock falling edge to the transfer clock falling edge	50			ns
t_{TLWH}	Time delay from the transport clock falling edge to the white reference clock rising edge	0		50	ns
t_{XLTH}	Time delay from the transfer clock falling edge to the rising edge of the next transport clock pulse	50			ns
t_r	Rise time (all clocks)	15			ns
t_f	Fall time (all clocks)	5			ns

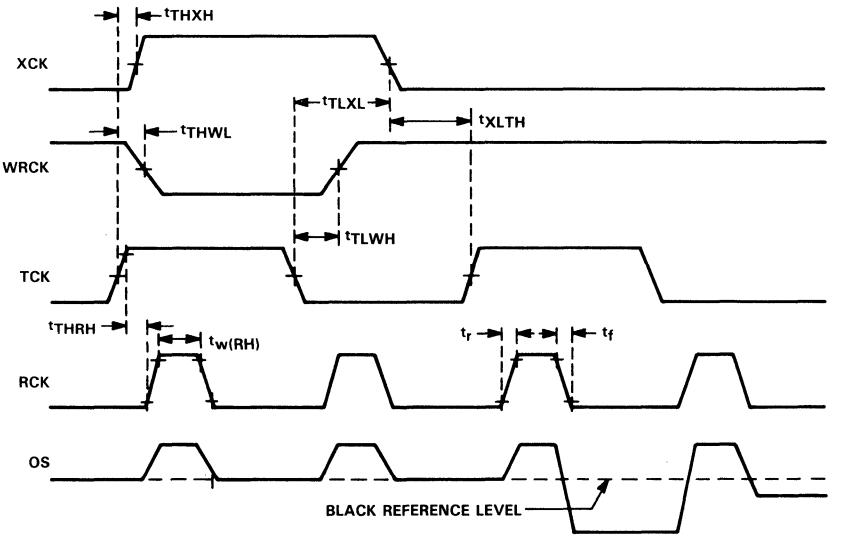
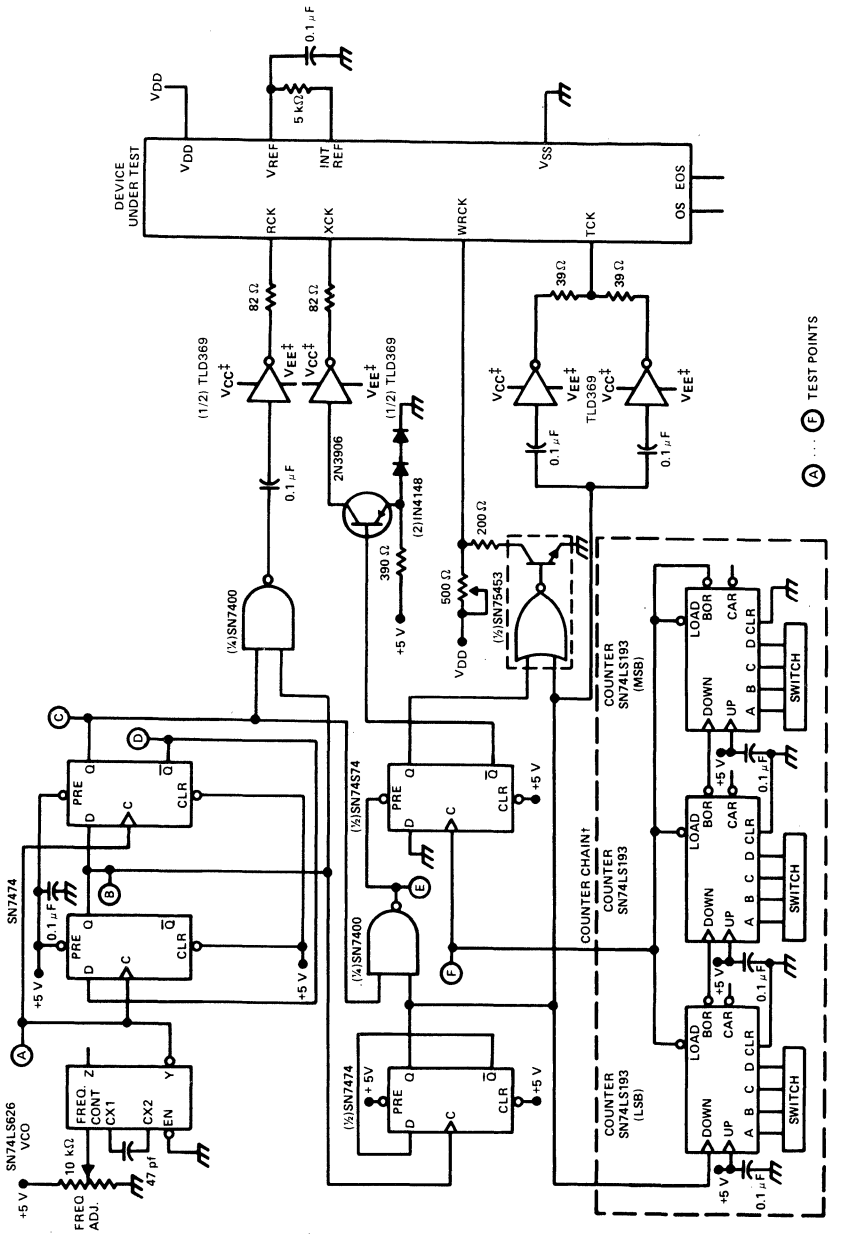


FIGURE 2. DEVICE TIMING REQUIREMENTS

PARAMETER MEASUREMENT INFORMATION



† This counter chain counts transport clock periods to generate the exposure time interval. The data rate is twice the count rate.
‡ V_{CC} and V_{EE} are the voltages that will produce the desired values of V_{IH} and V_{IL}, respectively, at the RCK, XCK, and TCK inputs.

FIGURE 3. DRIVER CIRCUIT FOR TESTING IMAGE SENSOR

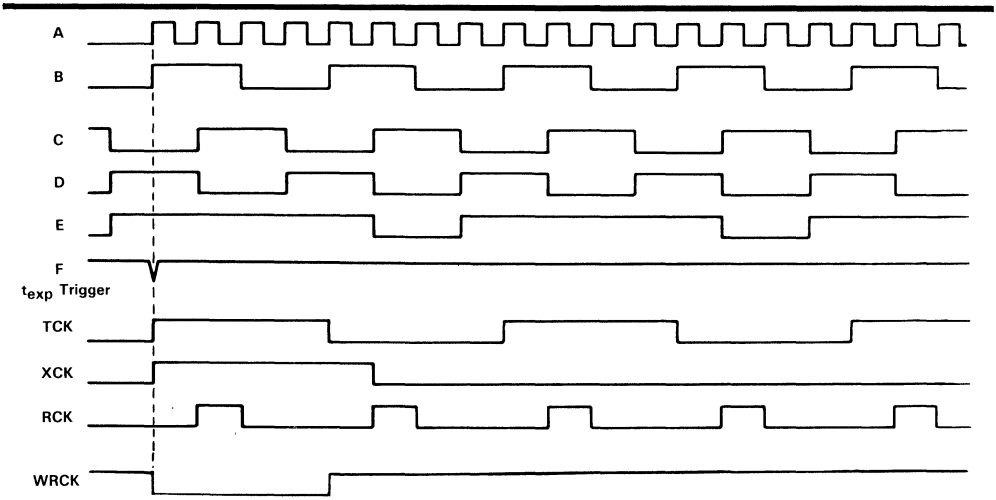


FIGURE 4. WAVEFORMS IN DRIVER CIRCUIT

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

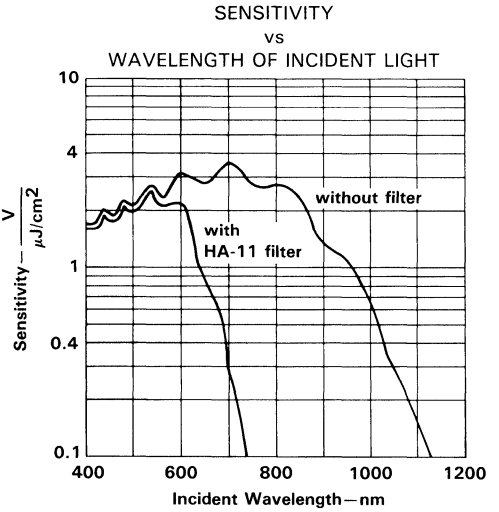


FIGURE 5

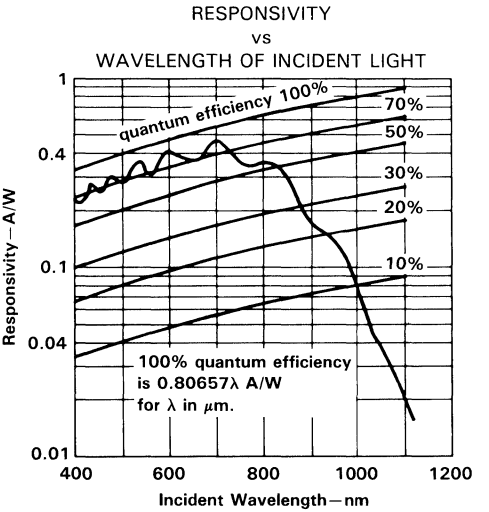


FIGURE 6

TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

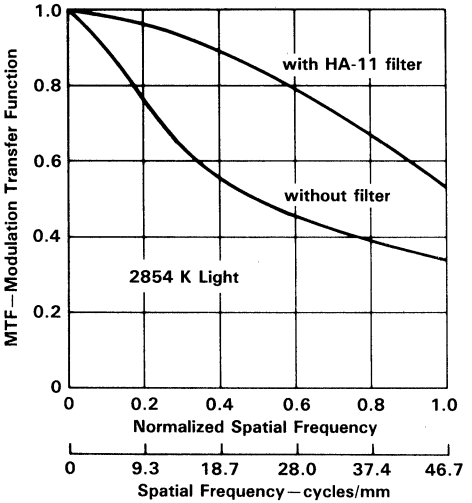


FIGURE 7

MODULATION TRANSFER FUNCTION
vs
SPATIAL FREQUENCY

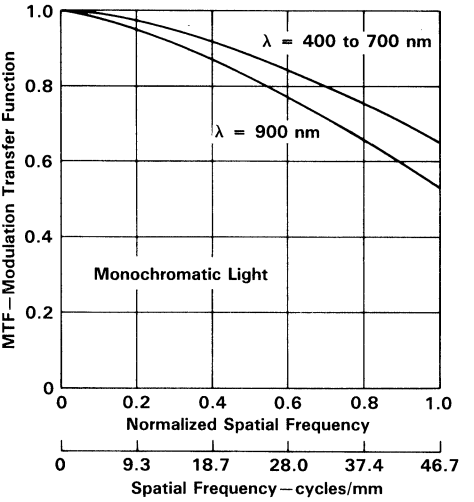


FIGURE 8

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

(In the circuit of Figure 3 with T_A = 25°C, f_{RCK} = 0.5 MHz, t_{exp} = 10 ms, and all operating voltages at nominal recommended values, unless otherwise noted)

AVERAGE AND LOW FREQUENCY DARK SIGNAL vs EXPOSURE TIME

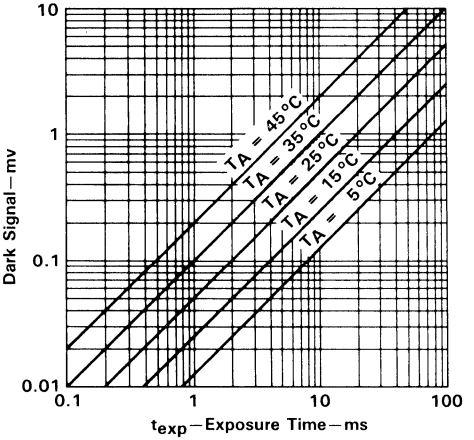


FIGURE 9

OUTPUT SIGNAL VOLTAGE RELATIVE TO SATURATED OUTPUT VOLTAGE vs EXPOSURE TIME

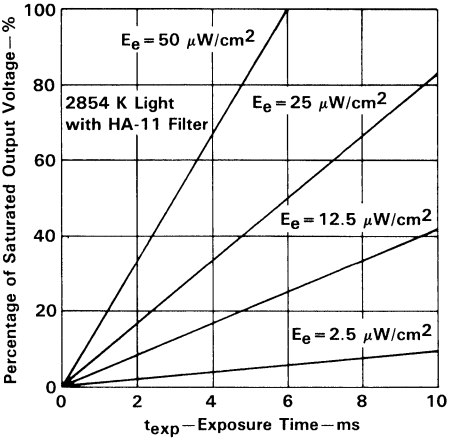
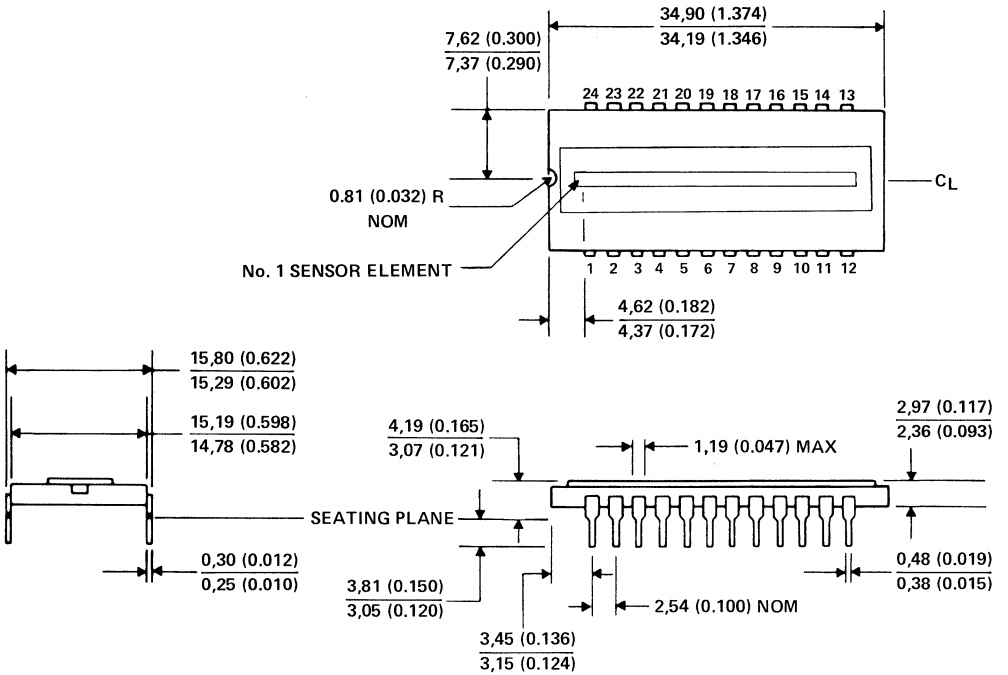


FIGURE 10

MECHANICAL DATA



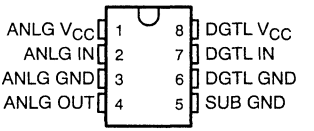
NOTE: The distance between the top surface of the window and the surface of the sensor is nominally 0.89 (0.035). This is determined by observing the vertical motion of a microscope focused first at one plane, then at the other.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

D3327, SEPTEMBER 1989

- 15-MHz Sampling Rate
- 30-ns Acquisition Time
- Diode-Bridge Switch
- 25-MHz Bandwidth
- Low-Voltage Supply

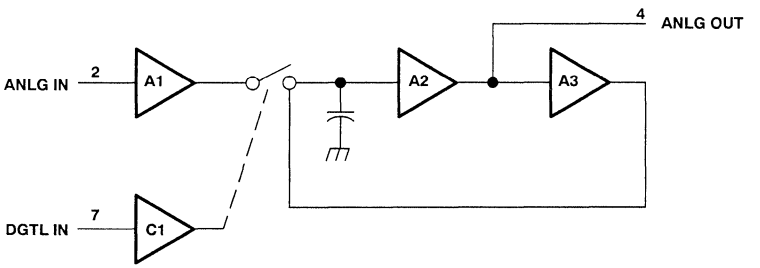
D OR P PACKAGE
(TOP VIEW)



description

The TL1591 is a monolithic integrated sample-and-hold circuit with excellent performance features using the BiFET process with Schottky-barrier diodes and designed for use with CCD area imagers. This device consists of an ultra-fast input buffer amplifier, a digital-controlled diode-bridge switch, and a high-impedance output buffer amplifier. The electronic switch is controlled by an LS-TTL-compatible logic input.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Digital input voltage ..... 0 to V_{CC}
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −25°C to 80°C
Storage temperature range ..... −55°C to 150°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 80°C$ POWER RATING
D	725 mW	5.8 mW/°C	406 mW
P	1000 mW	8.0 mW/°C	560 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.5	V
V_{IH}	High-level digital input voltage	2			V
V_{IL}	Low-level digital input voltage			0.8	V
$V_{I(PP)}$	Peak-to-peak analog input voltage			0.8	V

electrical characteristics over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage					−1.5	V
$V_{O(PP)}$	Analog peak-to-peak output voltage				1.1		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_{IL} = 0.4 V		−0.28	−0.4	mA
I_O	Analog output current				0.6		mA
I_{CC}	Supply current	V_{CC} = 5.5 V			15	20	mA
r_i	Input resistance				10		kΩ
r_o	Analog output resistance				50		Ω

operating characteristics

	PARAMETER	MIN	TYP†	MAX	UNIT
	Linearity		0.7%	2%	
A_v	Voltage amplification		0.8	0.9	V/V
	Sample-to-hold offset error		15		mV
	Sample-mode offset error		−50	50 −150	mV
	Hold-mode feedthrough			−50	dB
	Hold-mode droop			100	μV/μs

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

dynamic characteristics (see Figure 1)

PARAMETER	MIN	TYP†	MAX	UNIT
Acquisition time 0.6 V to 2% (see Note 1)		18		ns
Acquisition time 0.6 V to 1% (see Note 1)		31		ns
Hold-mode settling time (see Note 2)		35		ns
Sampling-mode bandwidth		25		MHz
Sampling rate			15	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

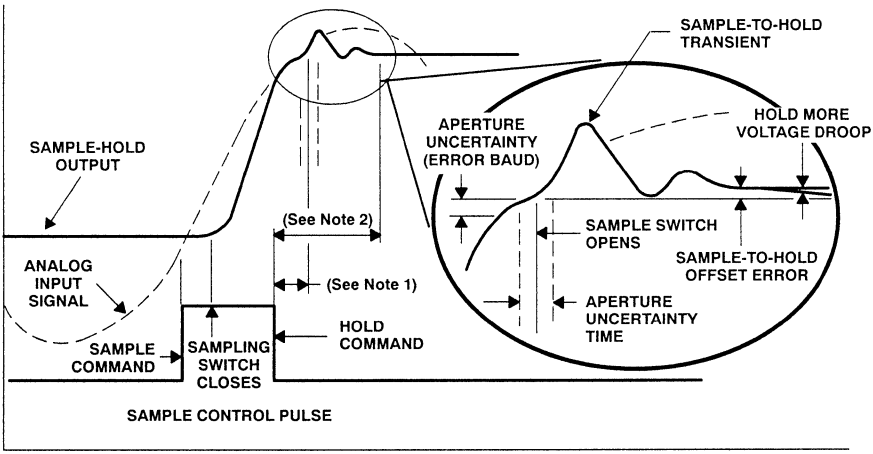


FIGURE 1. SAMPLE-HOLD DEFINITIONS

NOTES: 1. Acquisition time is the time required, after the closing of the sampling switch, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.
2. Hold-mode settling time is the time from the hold command transistion until the output has settled within a specified error band around the final value.

PARAMETER MEASUREMENT INFORMATION

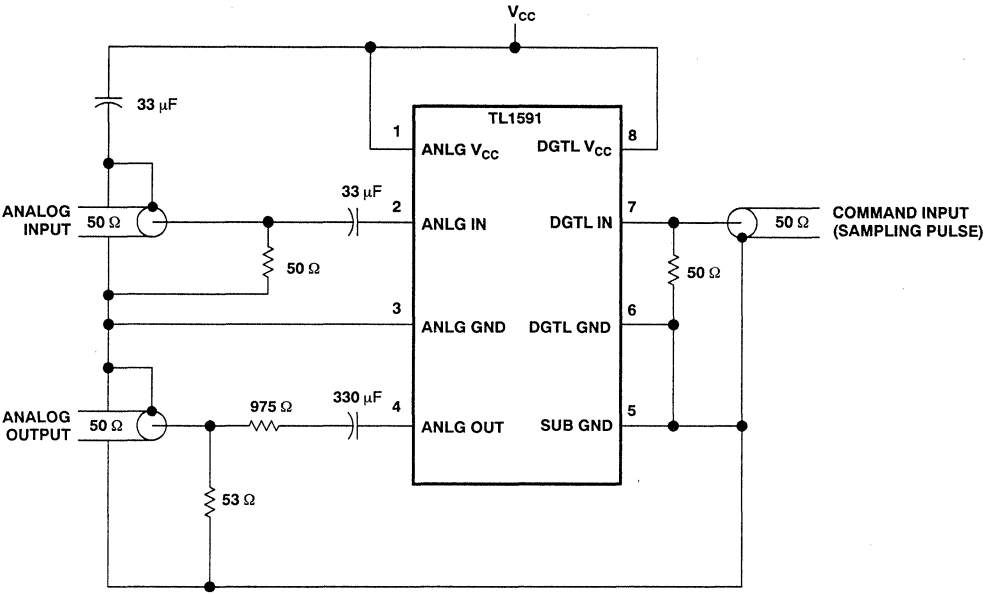


FIGURE 2. TEST CIRCUIT

TYPICAL CHARACTERISTICS

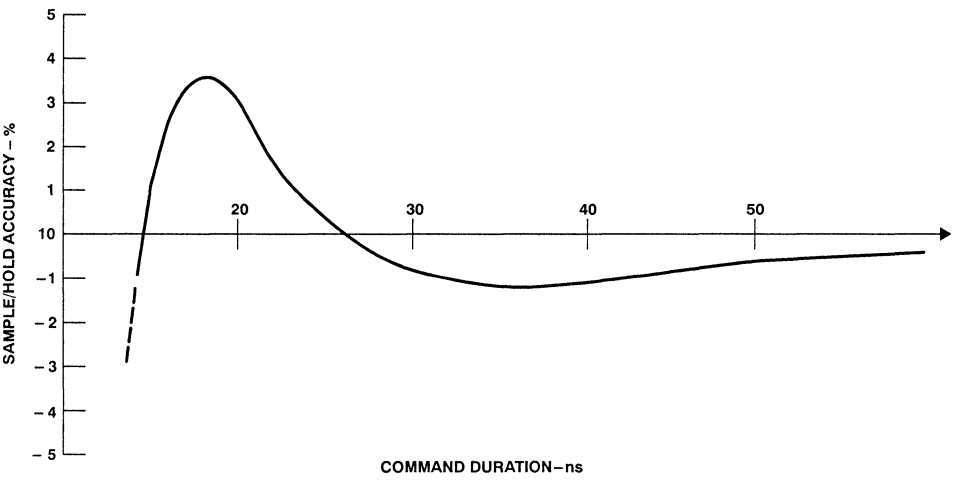


FIGURE 3. SAMPLE/HOLD ACCURACY VS COMMAND DURATION

TEXAS INSTRUMENTS
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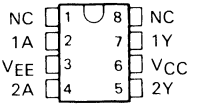
D3296, JUNE 1989

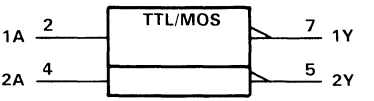
- **Dual Inverting MOS Driver**
- **Low Standby Power Dissipation**
- **Versatile Interface Circuit for Use between TTL Levels and Level-Shifted High-Current, High-Voltage Systems**
- **Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source**
- **Designed to Be Functionally Interchangeable with National DS0026**
- **Capable of Driving High-Capacitance Loads**
- **V_{CC} Supply Voltage Variable over Wide Range to 22 V Maximum with Respect to V_{EE}**
- **Operates from Standard Bipolar and/or MOS Supply Voltage**
- **High-Speed Switching**
- **Transient Overdrive Minimizes Power Dissipation**

P PACKAGE
(TOP VIEW)



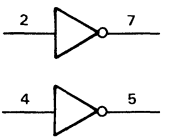
NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



description

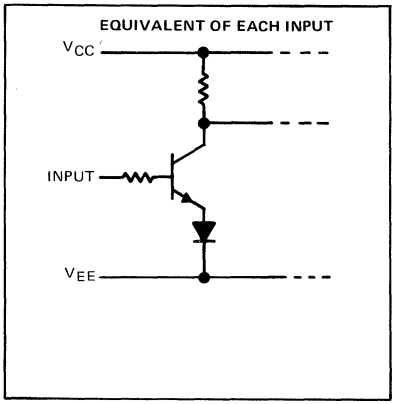
The TLD369 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

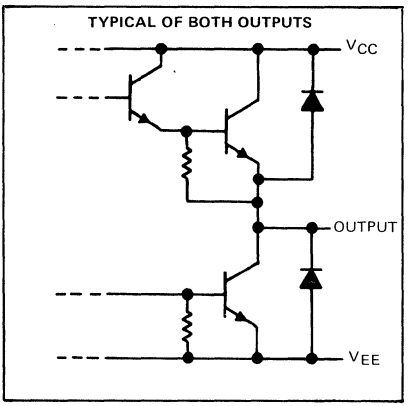
The TLD369 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC} supply voltage from 12 V to 20 V positive with respect to V_{EE}. However, it is designed so as to be usable over a wide range of V_{CC}.

Inputs of the TLD369 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications, the V_{EE} terminal is connected to the MOS V_{DD} supply of -12 V to -15 V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

The TLD369 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . −0.5 V to 22 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, derate linearly to 640 mW at 70°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	20	22	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.5		4.5	V
V_{IL}	Low-level input voltage			0.5	V
I_{IH}	High-level input current	8		20	mA
I_{IL}	Low-level input current			1.5	mA

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA					−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.5 V,	I_{OH} = −50 μA		V_{CC}−1	V_{CC}−0.7		V
		I_{IL} = 0.7 mA,	I_{OH} = −50 μA					
		V_{IL} = 0.5 V,	I_{OH} = −10 mA		V_{CC}−2.3	V_{CC}−1.8		
		I_{IL} = 0.7 mA,	I_{OH} = −10 mA					
V_{OL}	Low-level output voltage	V_{IH} = 2.5 V,	I_{OL} = 10 mA			0.15	0.3	V
		I_{IH} = 8 mA,	I_{OL} = 10 mA					
		V_{CC} = 10 V to 22 V,	V_{IH} = 2.5 V,	I_{OL} = 30 mA		0.2	0.4	
		V_{CC} = 10 V to 22 V,	I_{IH} = 8 mA,	I_{OL} = 30 mA				
V_{OK}	Output clamp voltage	V_I = 0,	I_{OH} = 20 mA				V_{CC}+1.5	V
V_I	Input voltage	I_I = 20 mA				3.7	5	V
		I_I = 8 mA				2.4	3	
		I_I = 1.5 mA				0.4	0.6	
I_I	Input current	V_I = 4.5 V				27	45	mA
		V_I = 2.5 V				9	15	
		V_I = 0.5 V					1.5	
$I_{CC(H)}$	Supply current from V_{CC}, both outputs high	V_{CC} = 22 V, No load	Both inputs at 0 V,				0.5	mA
$I_{CC(L)}$	Supply current from V_{CC}, both outputs low	V_{CC} = 22 V, No load	Both inputs at 3 V,			7	12	mA

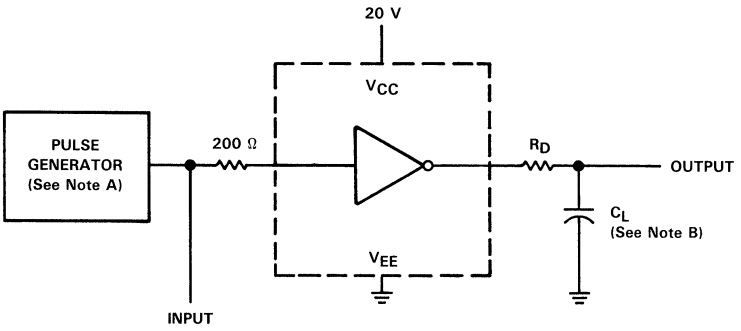
†All typical values are at V_{CC} = 20 V and T_A = 25°C.

NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

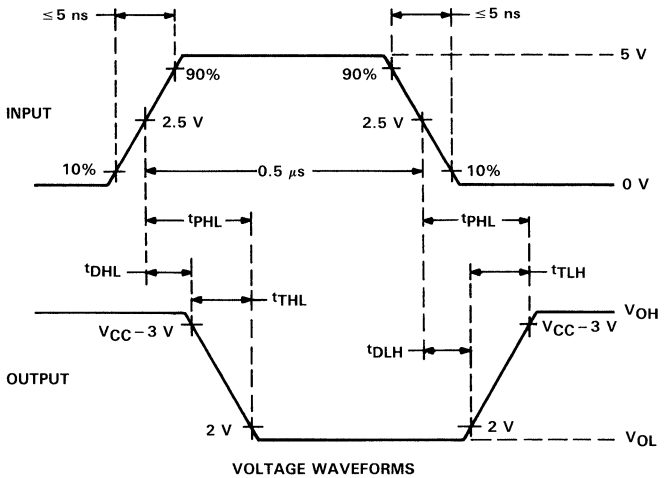
switching characteristics, V_{CC} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1	8	16	24	ns
t_{DHL}	Delay time, high-to-low-level output		4	11	20	ns
t_{TLH}	Transition time, low-to-high-level output		8	18	30	ns
t_{THL}	Transition time, high-to-low-level output		6	16	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		16	35	54	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	28	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

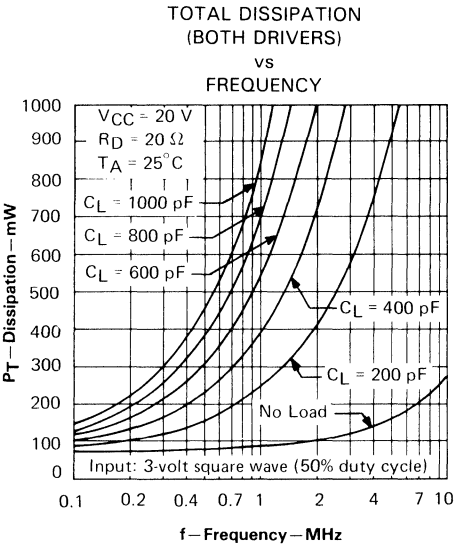


FIGURE 2

CCD Image Sensors/Support Functions

D2655, OCTOBER 1981

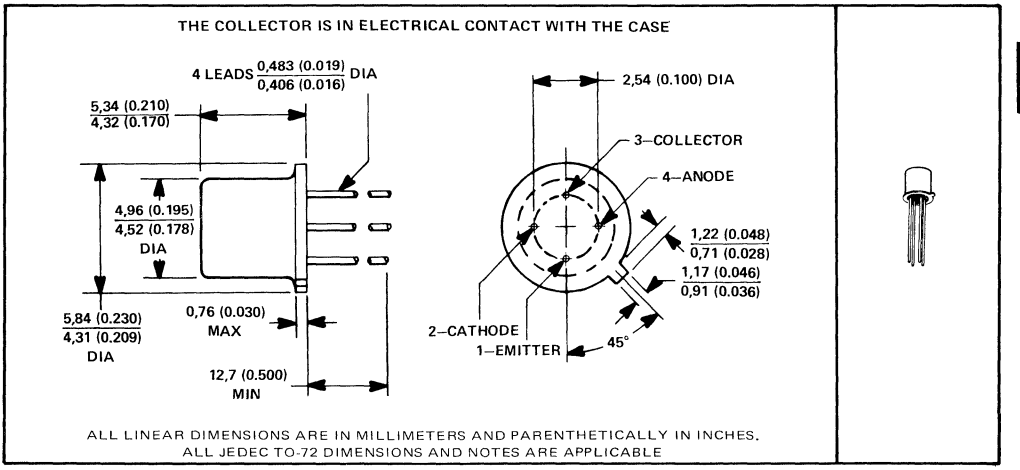
GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

- Photon Coupling for Isolator Applications
- Very High Current Transfer Ratio . . . 500%
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable Over Wide Temperature Range
- Hermetically Sealed TO-72 Package

description

This optocoupler features an improved current transfer ratio (CTR) at an input of one milliampere making it ideal for coupling with isolation from low-output MOS and CMOS devices to power devices or other systems. Typical applications include motor-speed controls, numeric control systems, meters, and instrumentation.

mechanical data



*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input to-Output Voltage	±1 kV
Collector-Emitter Voltage	40 V
Emitter-Collector Voltage	7 V
Input Diode Reverse Voltage	2 V
Input Diode Continuous Forward Current at (or below) 65°C Free-Air Temperature (See Note 1)	40 mA
Continuous Collector Current	50 mA
Peak Diode Current ($t_W < 1\ \mu s$, PRR < 300 pps)	1A
Continuous Transistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	190 mW
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−55°C to 125°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	240°C

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. Derate linearly to 125°C free-air temperature at the rate of 1.9 mW/°C.

*JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	3N261			3N262			3N263			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_E = 0, I_F = 0	40			40			40			V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 100 μA, I_C = 0 I_F = 0	7			7			7			V
I_R	Input Diode Static Reverse Current	V_R = 2 V			100			100			100	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 5 V, I_F = 1 mA	0.5			1		5	2		10	mA
		V_{CE} = 5 V, I_F = 2 mA, T_A = −55°C	0.7			1.4			2.8			
		V_{CE} = 5 V, I_F = 2 mA, T_A = 100°C	0.5			1			2			
		V_{CE} = 5 V, I_F = 10 mA, See Note 3		50			80			90		
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 20 V, I_F = 0		6	100		6	100		6	100	nA
		V_{CE} = 20 V, I_F = 0, T_A = 100°C		4	100		4	100		4	100	μA
V_F	Input Diode Static Forward Voltage	I_F = 10 mA, T_A = −55°C	1		1.7	1		1.7	1		1.7	V
		I_F = 10 mA	0.8	1.4	1.5	0.8	1.4	1.5	0.8	1.4	1.5	
		I_F = 10 mA, T_A = 100°C	0.7		1.3	0.7		1.3	0.7		1.3	
$V_{CE(sat)}$	Collector Emitter Saturation Voltage	I_C = 0.5 mA, I_F = 2 mA			0.3							V
		I_C = 1 mA, I_F = 2 mA						0.3				
		I_C = 2 mA, I_F = 2 mA									0.3	
r_{IO}	Input-to-Output Internal Resistance	V_{in-out} = ±1 kV, See Note 4	10^{11}	10^{12}		10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, f = 1 MHz, See Note 4		2.5	5		2.5	5		2.5	5	pF

*switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	3N261			3N262			3N263			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 10 V, $I_{F(on)}$ = 5 mA, R_L = 100 Ω, See Figure 1		10	20		10	20		15	25	μs
t_f	Fall Time			10	20		10	20		15	25	μs

NOTES: 3. This parameter must be measured using pulse techniques, t_w = 100 μs, duty cycle ≤ 1%.

4. These parameters are measured between all the input diode leads shorted together and all the phototransistor leads shorted together.

*JEDEC registered data.

TEXAS INSTRUMENTS
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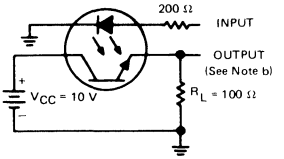
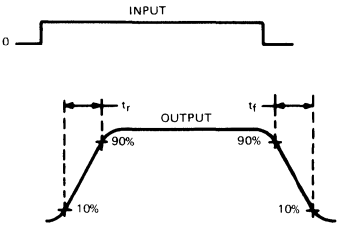
PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for
$I_{F(on)}$ = 5 mA



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

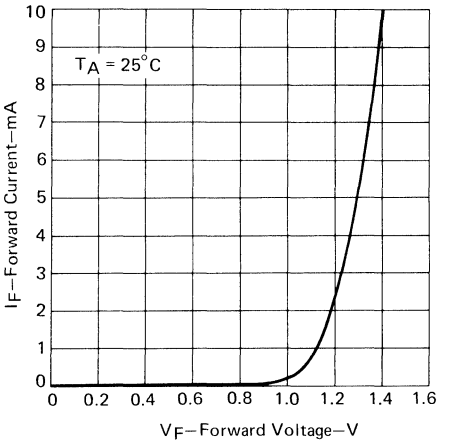


FIGURE 2

TYPICAL CHARACTERISTICS

3N262
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

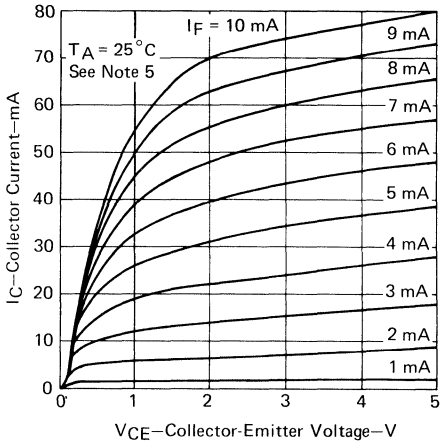


FIGURE 3

3N262
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

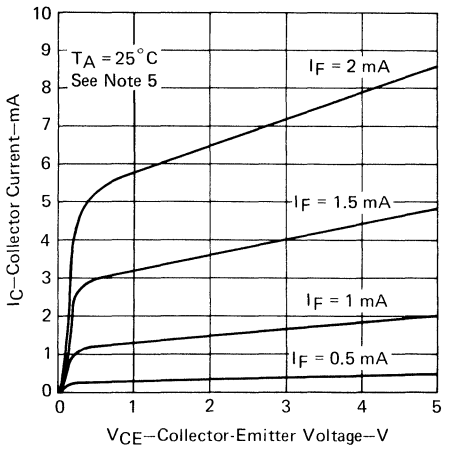


FIGURE 4

3N262
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

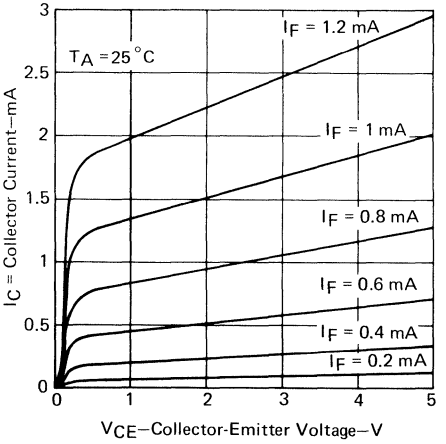


FIGURE 5

3N262
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

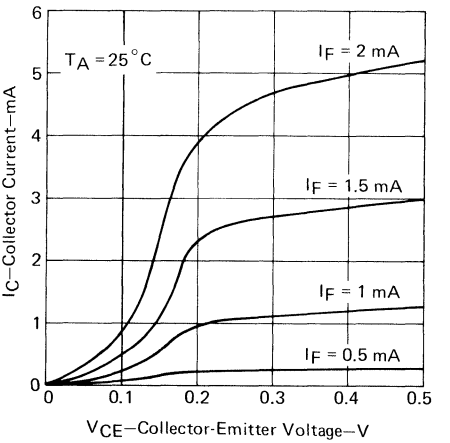


FIGURE 6

NOTE 5: This parameter was measured using pulse techniques, t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

3N262
COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

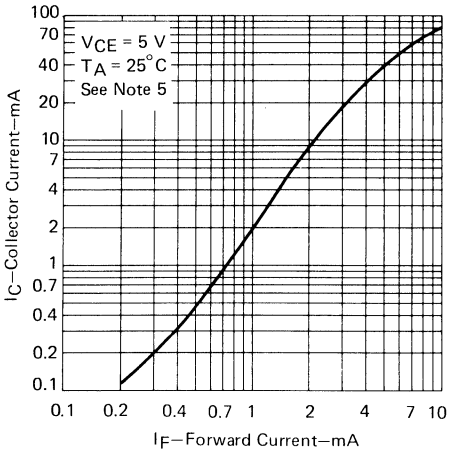


FIGURE 7

3N262
RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

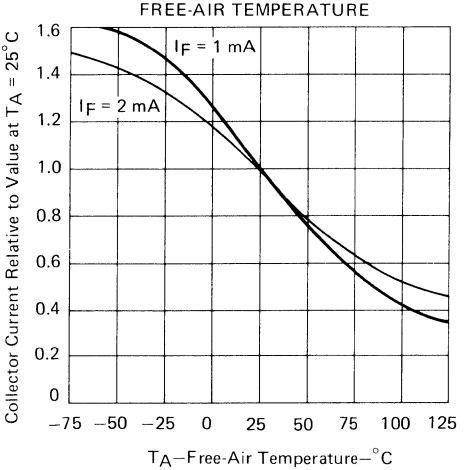


FIGURE 8

NOTE 5: This parameter was measured using pulse techniques. t_w = 100 μs, duty cycle = 1%.

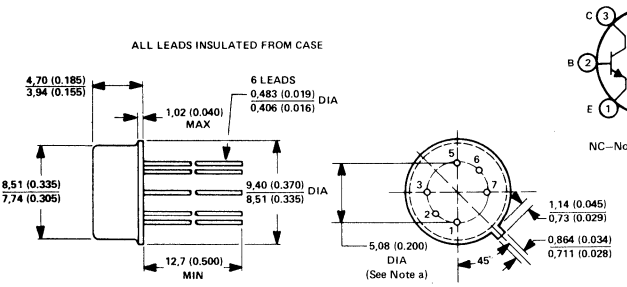
D1424, AUGUST 1973–REVISED APRIL 1987

JEDEC REGISTERED DEVICES
GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

- JAN, JAN TX, JAN TXV Versions Available
- Base Lead Provided for Conventional Transistor Biasing
- High Overall Current Gain . . . 1.5 Typ (4N24)
- High-Gain, High-Voltage Transistor. . . h_{FE} = 700 Typ (4N24), $V_{(BR)CEO}$ = 35 V MIN
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable over Wide Temperature Range

***mechanical data**

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



NOTE: a. Leads having maximum diameter shall be within 0,18 mm (0.007 inch) of true position relative to a maximum-width tab when measured in the gaging plane between 1,371 mm (0.054 inch) and 1,397 mm (0.055 inch) below the seating plane.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

***absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Input-to-Output Voltage	±1 kV
Collector-Base Voltage	35 V
Collector-Emitter Voltage	35 V
Emitter-Base Voltage	4 V
Input Diode Reverse Voltage	2 V
Input Diode Continuous Forward Current at (or below) 65°C Free-Air Temperature (See Note 1)	40 mA
Continuous Collector Current	50 mA
Peak Diode Current (See Note 2)	1A
Continuous Transistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	300 mW
Storage Temperature Range	−55°C to 125°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	240°C

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. This value applies for $t_w \leq 1\ \mu s$, PRR ≤ 300 pps.
3. Derate linearly to 125°C free-air temperature at the rate of 3 mW/°C.

*JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	4N22			4N23			4N24			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0, I_F = 0	35			35			35			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0, I_F = 0	35			35			35			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0, I_F = 0	4			4			4			V
I_R	Input Diode Static Reverse Current	V_R = 2 V			100			100			100	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 5 V, I_B = 0, I_F = 2 mA	0.15			0.2			0.4			mA
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA, T_A = −55°C	1			2.5			4			
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA	2.5	4		6	8		10	15		
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA, T_A = 100°C	1			2.5			4			
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 20 V, I_B = 0, I_F = 0			100			100			100	nA
		V_{CE} = 20 V, I_B = 0, I_F = 0, T_A = 100°C			100			100			100	μA
V_F	Input Diode Static Forward Voltage	I_F = 10 mA, T_A = −55°C	1		1.5	1		1.5	1		1.5	V
		I_F = 10 mA	0.8		1.3	0.8		1.3	0.8		1.3	
		I_F = 10 mA, T_A = 100°C	0.7		1.2	0.7		1.2	0.7		1.2	
$V_{CE(sat)}$	Collector-Emitter Stauration Voltage	I_C = 2.5 mA, I_B = 0, I_F = 20 mA			0.3							V
		I_C = 5 mA, I_B = 0, I_F = 20 mA						0.3				
		I_C = 10 mA, I_B = 0, I_F = 20 mA									0.3	
r_{IO}	Input-to-Output Internal Resistance	V_{in-out} = ±1 kV, See Note 5	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, f = 1 MHz, See Note 4			5			5			5	pF

*switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	4N22			4N23			4N24			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 10 V, $I_{F(on)}$ = 10 mA, R_L = 100 Ω, See Figure 1			15			15			20	μs
t_f	Fall Time				15			15			20	μs

NOTE 4: These parameters are measured between all the input diode leads shorted together and all the phototransistor leads shorted together.

*JEDEC registered data

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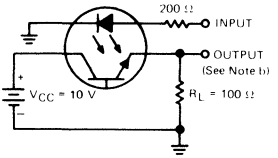
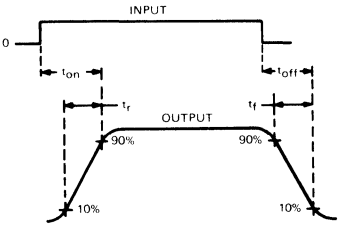
*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

Adjust amplitude of input pulse for $I_{F(on)}$ = 10 mA



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, t_w = 100 μs, duty cycle ≈ 1%.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ MΩ, $C_{in} \leq$ 20 pF.

*JEDEC registered data

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

4N22
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

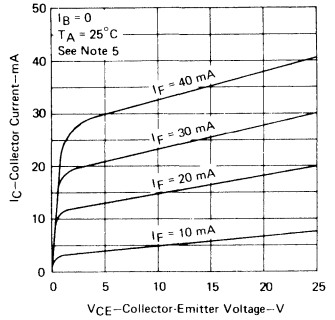


FIGURE 2

4N23
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

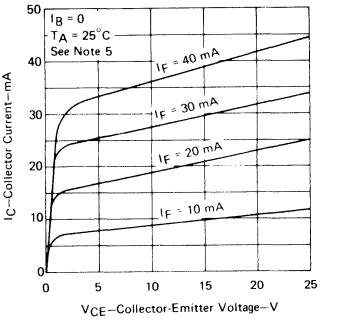


FIGURE 3

4N24
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

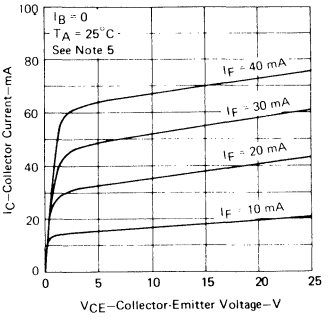


FIGURE 4

NOTE 5: This parameter was measured using pulse techniques. t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

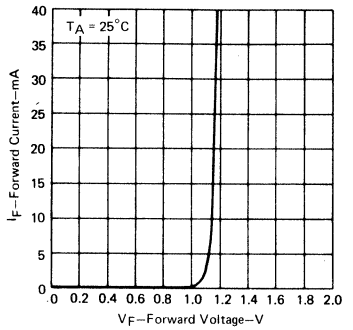
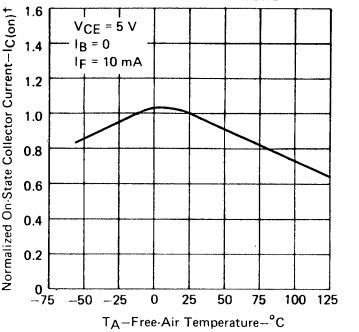


FIGURE 5

NORMALIZED ON-STATE COLLECTOR CURRENT†
vs
FREE-AIR TEMPERATURE



†Normalized to value at T_A = 25° C

FIGURE 6

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

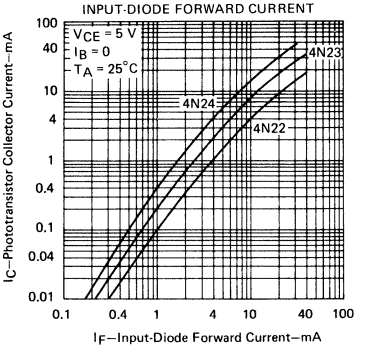


FIGURE 7

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

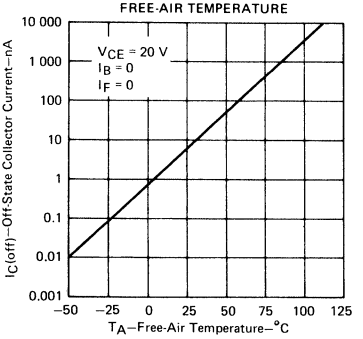


FIGURE 8

AVERAGE SWITCHING TIME
vs
LOAD RESISTANCE

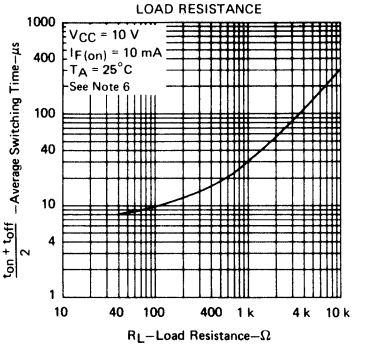


FIGURE 9

NOTE 6: This parameter was measured in the test circuit of Figure 1 with R_L varied between 40 Ω and 10 kΩ.

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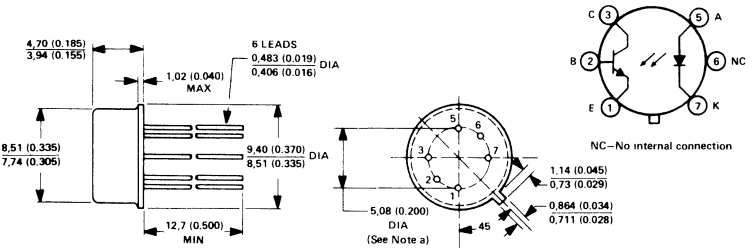
D3055, AUGUST 1987

JEDEC REGISTERED DEVICES
GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

- Both Input and Output Circuits Are Isolated from the Can
- JAN, JAN TX, JAN TXV Versions Available
- High Overall Current Gain . . . 1.5 Typ (4N24A)
- High-Gain, High-Voltage Transistor . . . h_{FE} = 700 Typ (4N24A), $V_{(BR)CEO}$ = 35 V Min
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable over Wide Temperature Range

***mechanical data**

ALL LEADS ARE ELECTRICALLY INSULATED FROM THE CASE



NOTE: a. Leads having maximum diameter shall be within 0,18 mm (0.007 inch) of true position relative to a maximum-width tab when measured in the gaging plane between 1,371 mm (0.054 inch) and 1,397 mm (0.055 inch) below the seating plane.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

***absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Input-to-output voltage	±1 kV
Collector-base voltage	35 V
Collector-emitter voltage	35 V
Emitter-base voltage	4 V
Input diode reverse voltage	2 V
Input diode continuous forward current at (or below) 65°C free-air temperature (see Note 1)	40 mA
Continuous collector current	50 mA
Peak diode current (see Note 2)	1 A
Continuous transistor power dissipation at (or below) 25°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	240°C

* JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. This value applies for $t_w \leq 1\ \mu s$, PRR ≤ 300 pps.
3. Derate linearly to 125°C free-air temperature at the rate of 3 mW/°C.

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	4N22A			4N23A			4N24A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100 μA, I_E = 0, I_F = 0	35			35			35			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 1 mA, I_B = 0, I_F = 0	35			35			35			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100 μA, I_C = 0, I_F = 0	4			4			4			V
I_R	Input diode static reverse current	V_R = 2 V			100			100			100	μA
$I_{C(on)}$	On-state collector current	V_{CE} = 5 V, I_B = 0, I_F = 2 mA	0.15			0.2			0.4			mA
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA, T_A = −55°C	1			2.5			4			
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA	2.5	4		6	8		10	15		
		V_{CE} = 5 V, I_B = 0, I_F = 10 mA, T_A = 100°C	1			2.5			4			
$I_{C(off)}$	Off-state collector current	V_{CE} = 20 V, I_B = 0, I_F = 0			100			100			100	nA
		V_{CE} = 20 V, I_B = 0, I_F = 0, T_A = 100°C			100			100			100	μA
V_F	Input diode static forward voltage	I_F = 10 mA, T_A = −55°C	1		1.5	1		1.5	1		1.5	V
		I_F = 10 mA	0.8		1.3	0.8		1.3	0.8		1.3	
		I_F = 10 mA, T_A = 100°C	0.7		1.2	0.7		1.2	0.7		1.2	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 2.5 mA, I_B = 0, I_F = 20 mA			0.3							V
		I_C = 5 mA, I_B = 0, I_F = 20 mA						0.3				
		I_C = 10 mA, I_B = 0, I_F = 20 mA									0.3	
r_{IO}	Input-to-output internal resistance	V_{in-out} = ±1 kV, See Note 4	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-output capacitance	V_{in-out} = 0, f = 1 MHz, See Note 4			5			5			5	pF

*switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	4N22A			4N23A			4N24A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_{CC} = 10 V, $I_{F(on)}$ = 10 mA, R_L = 100 Ω, See Figure 1			15			15			20	μs
t_f	Fall time				15			15			20	μs

NOTE 4: These parameters are measured between all the input diode leads shorted together and all the phototransistor leads shorted together.
*JEDEC registered data

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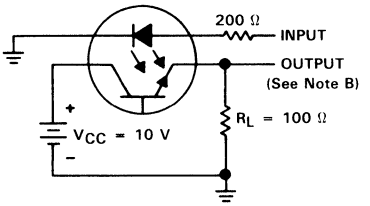
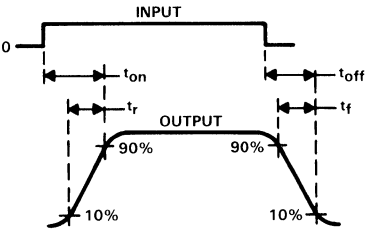
*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

Adjust amplitude of input pulse for $I_{F(on)}$ = 10 mA



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq 15$ ns, t_w = 100 μs, duty cycle = 1%.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 12$ ns, $R_{in} \geq 1$ MΩ, $C_{in} \leq 20$ pF.
* JEDEC registered data

TYPICAL CHARACTERISTICS

4N22A
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

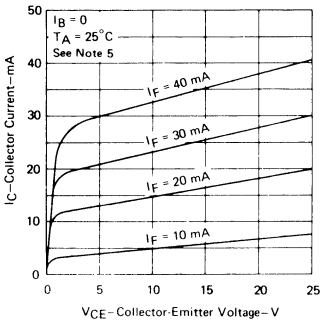


FIGURE 2

4N23A
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

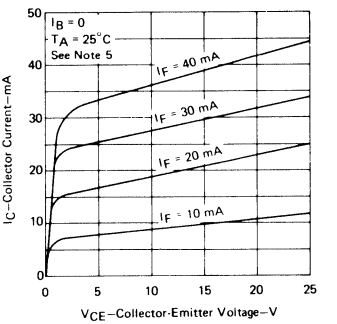


FIGURE 3

4N24A
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

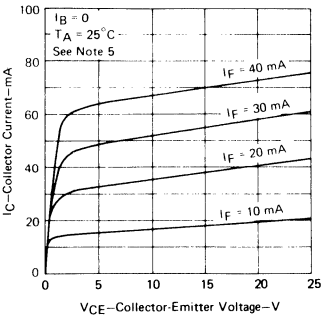


FIGURE 4

NOTE 5: This parameter was measured using pulse techniques, t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

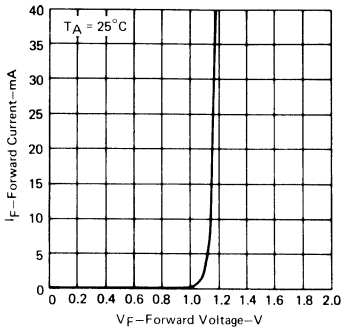
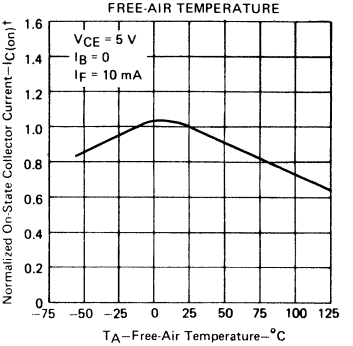


FIGURE 5

NORMALIZED ON-STATE COLLECTOR CURRENT†
vs
FREE-AIR TEMPERATURE



†Normalized to value at T_A = 25° C

FIGURE 6

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

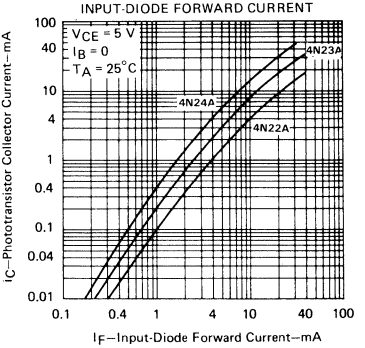


FIGURE 7

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

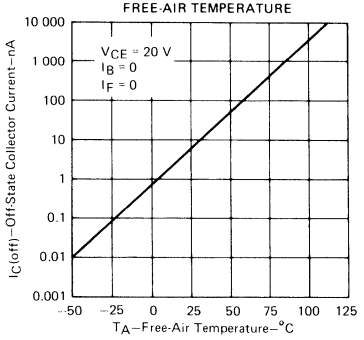


FIGURE 8

AVERAGE SWITCHING TIME
vs
LOAD RESISTANCE

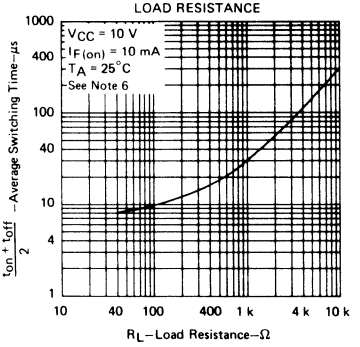


FIGURE 9

NOTE 6: This parameter was measured in the test circuit of Figure 1 with R_L varied between 40 Ω and 10 kΩ.

TEXAS INSTRUMENTS
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This processing applies only to optocouplers ordered under part numbers shown below:

JAN4N22, JAN4N22A, JANTX4N22, JANTX4N22A, JANTXV4N22, JANTXV4N22A
JAN4N23, JAN4N23A, JANTX4N23, JANTX4N23A, JANTXV4N23, JANTXV4N23A
JAN4N24, JAN4N24A, JANTX4N24, JANTX4N24A, JANTXV4N24, JANTXV4N24A

TEST (PER MIL-S-19500/486A)	MIL-STD-750 TEST METHOD	JAN	JANTX	JANTXV
100% Processing				
Internal visual	2072			X
Storage: T_A = 125°C, t = 72 h	—		X	X
Temperature cycle: −55°C to 125°C, 10 cycles	1051		X	X
Constant acceleration: 20,000 G, Y_1 axis	2006		X	X
High-temperature reverse bias: I_F = 0, T_A = 125°C, V_{CB} = 20 V, t = 96 h	1039		X	X
Power burn-in: I_F = 40 mA, P_D = 275 ± 25 mW, t = 168 h	1039		X	X
Hermetic seal, fine	1071 Cond. G or H		X	X
Hermetic seal, gross	1071 Cond. C or D		X	X
External visual	2071		X	X
Product Acceptance				
Group A				
External visual: LTPD is 10 for JAN, 7 for JANTX and JANTXV	2071	X	X	X
Electrical: T_A = 25°C, LTPD is 7 for JAN, 5 for JANTX and JANTXV	as needed	X	X	X
Electrical: T_A = 100°C, LTPD is 10 for JAN, 7 for JANTX and JANTXV	as needed	X	X	X
Electrical: T_A = −55°C, LTPD is 10 for JAN, 7 for JANTX and JANTXV	as needed	X	X	X
Group B-1: LTPD = 15				
Solderability	2026	X	X	X
Thermal shock	1051 Cond. B	X	X	X
Thermal shock	1056 Cond. A	X	X	X
Hermetic seal, fine	1071 Cond. G or H	X	X	X
Hermetic seal, gross	1071 Cond. C or D	X	X	X
Moisture resistance	1021	X	X	X
Group B-2: LTPD = 10				
Shock: 1500 G	2016	X	X	X
Vibration: 50 G	2056	X	X	X
Acceleration: 30,000 G	2006	X	X	X
Group B-3: LTPD = 20				
Isolation voltage: V_{IO} = 150 V, T_A = 125°C, t = 24 h	1016	X	X	X
Group B-4: LTPD is 7 for JAN, 5 for JANTX and JANTXV				
High temperature life (nonoperating): T_A = 125°C, t = 340 h	1032	X	X	X
Group B-5: LTPD is 7 for JAN, 5 for JANTX and JANTXV				
Steady-state operating life: t = 340 h	1027	X	X	X

TEST (PER MIL-S-19500/486A)	MIL-STD-750 TEST METHOD	JAN	JANTX	JANTXV
(Group C tests are run on one lot every six months)				
Group C-1				
Barometric pressure: LTPD = 10	1001	X	X	X
Group C-2				
Physical dimensions: LTPD = 20	2066	X	X	X
Group C-3 (MIL-STD 202, Method 215)				
Resistance to solvents: LTPD = 10	—	X	X	X
Group C-4				
Terminal strength: LTPD = 10	2036 Cond. E	X	X	X
Group C-5				
Salt atmosphere: LTPD = 10	1041	X	X	X
Group C-6				
High-temperature life (nonoperating): T_A = 125°C, t = 1000 h, LTPD is 7 for JAN, 5 for JANTX and JANTXV	1032	X	X	X
Group C-7				
Steady-state operating life: t = 1000 h, LTPD is 7 for JAN, 5 for JANTX and JANTXV	1027	X	X	X

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

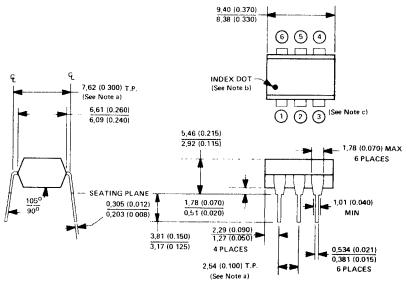
D2493, SEPTEMBER 1978--REVISED MARCH 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 2.5-kV, 1.5-kV, or 0.5-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching . . . t_r = 2 μs, t_f = 2 μs Typical**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,127 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.
c. Terminal connections:
1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

*Peak Input-to-Output Voltage: 4N25	±2.5 kV
4N26, 4N27	±1.5 kV
4N28	±0.5 kV
*Collector-Base Voltage	70 V
*Collector-Emitter Voltage (See Note 1)	30 V
*Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
*Input-Diode Reverse Voltage	3 V
*Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	80 mA
*Input-Diode Peak Forward Current (t_W = 300 μs, duty cycle = 2%)	3 A
*Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 3)	150 mW
Phototransistor (See Note 3)	150 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 4)	250 mW
*Storage Temperature Range	−55°C to 150°C
*Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

*JEDEC registered data. This data sheet contains all applicable JEDEC-registered data in effect at the time of publication.

NOTES: 1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	4N25, 4N26			4N27,4N28			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
*$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0, I_F = 0	70			70			V
*$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0, I_F = 0	30			30			V
*$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 100 μA, I_B = 0, I_F = 0	7			7			V
*I_R	Input Diode Static Reverse Current	V_R = 3 V			100			100	μA
*$I_{C(on}$	On-State Collector Current (Phototransistor Operation)	V_{CE} = 10 V, I_B = 0, I_F = 10 mA	2	5		1	3		mA
$I_{C(on)}$	On-State Collector Current (Photodiode Operation)	V_{CB} = 10 V, I_E = 0, I_F = 10 mA		20			20		μA
*$I_{C(off)}$	Off-State Collector Current (Phototransistor Operation)	V_{CE} = 10 V, I_B = 0, I_F = 0		1	50		1	50	nA
*$I_{C(off)}$	Off-State Collector current (Photodiode Operation)	V_{CB} = 10 V, I_E = 0, I_F = 0		0.1	20		0.1	20	nA
*V_F	Input Diode Static Forward Voltage	I_F = 10 mA		1.25	1.5		1.25	1.5	V
*$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 2 mA, I_B = 0, I_F = 50 mA		0.25	0.5		0.25	0.5	V
r_{IO}	Input-to-Output Internal resistance	V_{in-out} = ±2.5 kV for 4N25, ±1.5 kV for 4N26, 4N27, ±0.5 kV for 4N28, See Note 5	10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, f = 1 MHz, See Note 5		1			1		pF

*JEDEC registered data

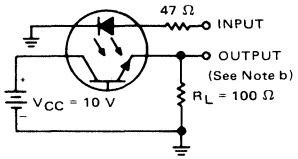
NOTE 5: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

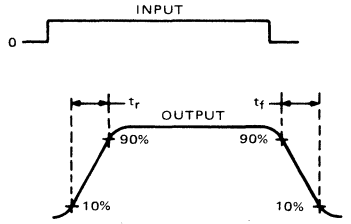
PARAMETER			TEST CONDITIONS	TYP	UNIT
t_r	Rise Time	Phototransistor	V_{CC} = 10 V, I_B = 0, $I_{C(on)}$ = 2 mA,	2	μs
t_f	Fall Time	Operation	R_L = 100 Ω, See Test Circuit A of Figure 1	2	
t_r	Rise Time	Photodiode	V_{CC} = 10 V, I_E = 0, $I_{C(on)}$ = 20 μA,	1	μs
t_f	Fall Time	Operation	R_L = 1 kΩ, See Test Circuit B of Figure 1	1	

PARAMETER MEASUREMENT INFORMATION

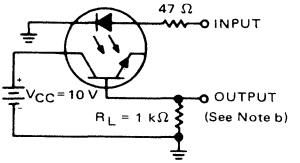
Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS



TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1 – SWITCHING TIMES

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

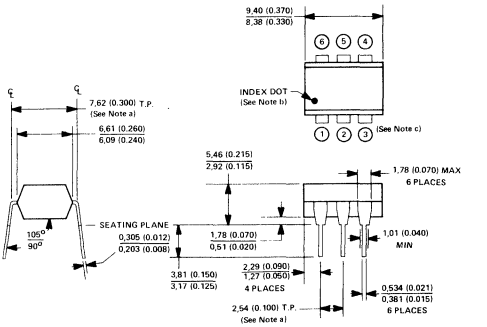
D2657, NOVEMBER 1981 – REVISED APRIL 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor
- High Direct-Current Transfer Ratio
- High-Voltage Electrical Isolation . . . 1.5 kV, 2.5 kV, or 3.55 kV Rating
- Plastic Dual-In-Line Package
- High-Speed Switching: t_r = 7 μs, t_f = 7 μs Typical
- Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays, and Pulse Transformers

mechanical

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.
c. Terminal connections:
1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	4N35	4N36	4N37
Input-to-Output Peak Voltage (8-ms half sine wave)	3.55 kV	2.5 kV	1.5 kV
Input-to-Output Root-Mean-Square Voltage (8-ms half sine wave)	2.5 kV	1.75 kV	1.05 kV
Collector-Base Voltage	70 V		
Collector-Emitter Voltage (See Note 1)	30 V		
Emitter-Base Voltage	7 V		
Input-Diode Reverse Voltage	6 V		
Input-Diode Forward Current: Continuous	60 mA		
Peak (1 μs, 300 pps)	3 A		
Phototransistor Continuous Collector Current	100 mA		
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:			
Infrared-Emitting Diode (See Note 2)	100 mW		
Phototransistor (See Note 3)	300 mW		
Continuous Power Dissipation at (or below) 25°C Lead Temperature:			
Infrared-Emitting Diode (See Note 4)	100 mW		
Phototransistor (See Note 5)	500 mW		
Storage Temperature Range	−55°C to 150°C		
Operating Temperature Range	−55°C to 100°C		
Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C		

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C lead temperature at the rate of 1.33 mW/°C. Lead temperature is measured on the collector lead 0.8 mm (1/32 inch) from the case.
5. Derate linearly to 100°C lead temperature at the rate of 6.7 mW/°C.

*JEDEC registered data. This sheet contains all applicable registered data in effect at the time of publication.

electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_F = 0	I_E = 0,	70*			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_F = 0	I_B = 0,	30*			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_F = 0	I_C = 0,	7*			V
I_R	Input Diode Static Reverse Current	V_R = 6 V				10*	μA
I_{IO}	Input-to-Output Current	V_{IO} = rated peak value,	t = 8 ms			100	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 10 V, I_B = 0	I_F = 10 mA,	10*			mA
		V_{CE} = 10 V, I_B = 0,	I_F = 10 mA, T_A = −55°C	4*			
		V_{CE} = 10 V, I_B = 0,	I_F = 10 mA T_A = 100°C	4*			
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 10 V, I_B = 0	I_F = 0,		1	50	nA
		V_{CE} = 30 V, I_B = 0,	I_F = 0, T_A = 100°C			500*	μA
h_{FE}	Transistor Static Forward Current Transfer Ratio	V_{CE} = 5 V, I_F = 0	I_C = 10 mA,		500		
V_F	Input Diode Static Forward Voltage	I_F = 10 mA		0.8*		1.5*	V
		I_F = 10 mA,	T_A = −55°C	0.9*		1.7*	
		I_F = 10 mA, T_A = 100°C		0.7*		1.4*	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 0.5 mA, I_B = 0	I_F = 10 mA,			0.3*	V
r_{IO}	Input-to-Output Internal Resistance	V_{IO} = 500 V,	See Note 6	10^{11}*			Ω
C_{io}	Input-to-Output Capacitance	V_{IO} = 0, See Note 6	f = 1 MHz,		1	2.5*	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

*switching characteristics at 25°C free-air temperature

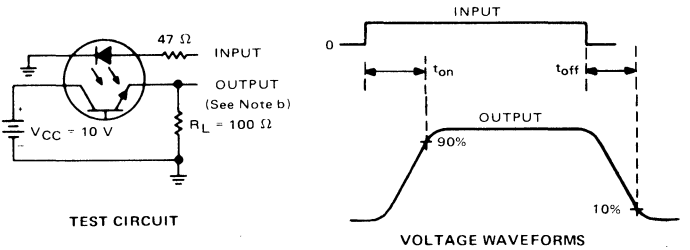
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{CC} = 10 V, R_L = 100 Ω,	$I_{C(on)}$ = 2 mA, See Figure 1			10	μs
t_{off}	Turn-off time					10	μs

*JEDEC registered data.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for
$I_{C(on)}$ = 2 mA



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF

FIGURE 1—SWITCHING TIMES

TYPICAL CHARACTERISTICS

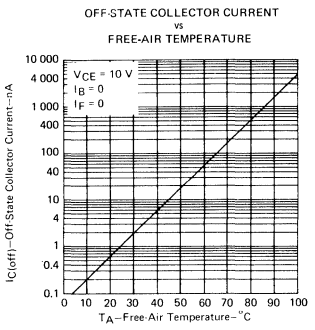


FIGURE 2

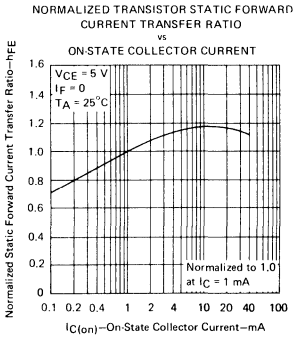


FIGURE 3

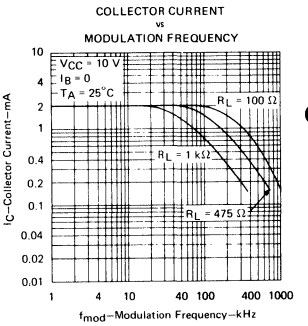


FIGURE 4

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

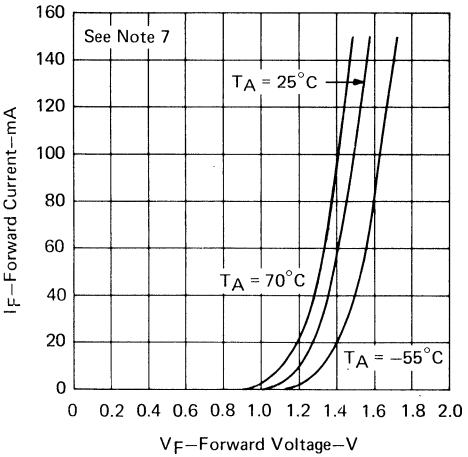


FIGURE 5

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

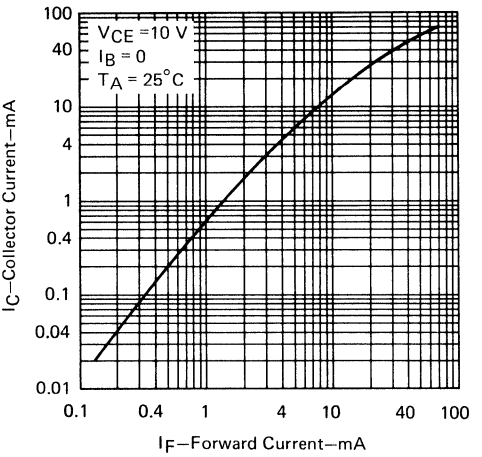


FIGURE 6

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

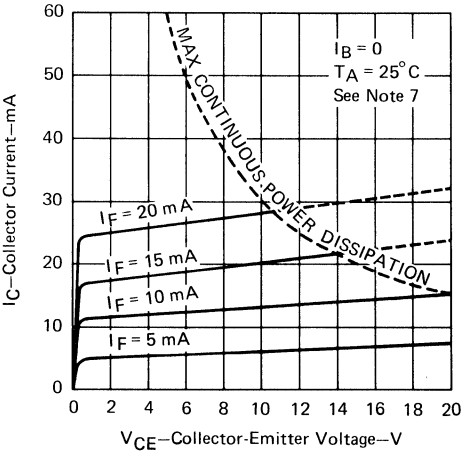


FIGURE 7

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

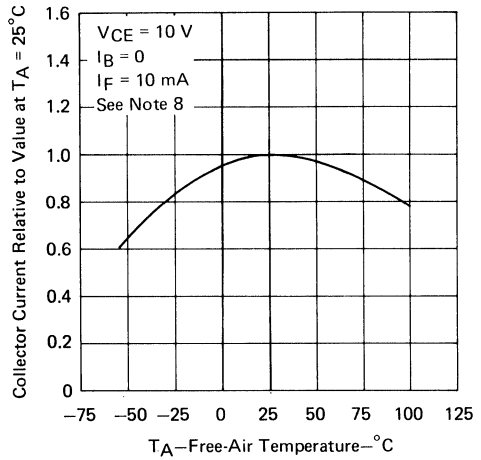


FIGURE 8

NOTES: 7. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
8. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2413, FEBRUARY 1978 – REVISED SEPTEMBER 1981

GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

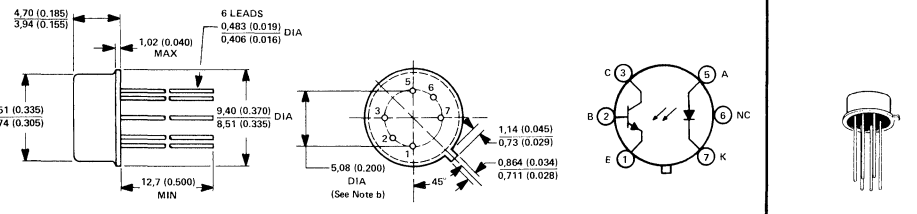
- JAN, JANTX, JANTXV Versions Available
- Very High Current Transfer Ratio . . . 500% Typical (4N49)
- Photon Coupling for Isolator Applications
- Base Lead Provided for Conventional Transistor Biasing
- High-Speed Photodiode-Mode Operation
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable over Wide Temperature Range
- Hermetically Sealed Package

description

This optocoupler features an improved current transfer ratio (CTR) at an input of one milliampere making it ideal for coupling with isolation from low-output MOS and CMOS devices to power devices or other systems. Typical applications include motor-speed controls, numeric systems, meters, and instrumentation.

*mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



NOTES: a. All linear dimensions are in millimeters and parenthetically in inches.
b. Leads having maximum diameter shall be within 0,18 mm (0.007 inches) of true position relative to a maximum-width tab when measured in the gaging plane between 1,371 mm (0.054 inches) and 1,397 mm (0.055 inches) below the seating plane.

*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±1 kV
Collector-Emitter Voltage	40 V
Collector-Base Voltage	45 V
Emitter-Base Voltage	7 V
Input Diode Reverse Voltage	2 V
Input Diode Continuous Forward Current at (or below) 65°C Free-Air Temperature (See Note 1)	40 mA
Continuous Collector Current	50 mA
Peak Diode Current (See Note 2)	1 A
Continuous Transistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	300 mW
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−55°C to 125°C
Lead Temperature 1/16 Inch (1.6 mm) from Case for 10 Seconds	240°C

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. This values applies for $t_w \leq 1\ \mu s$, PRR ≤ 300 pps.
3. Derate linearly to 125°C free-air temperature at the rate of 3 mW/°C.

*JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		4N47			4N48			4N49			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_F = 0	I_E = 0,	45			45			45			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_F = 0	I_B = 0,	40			40			40			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_F = 0	I_C = 0,	7			7			7			V
I_R	Input Diode Static Reverse Current	V_R = 2 V				100			100			100	μA
$I_{C(on)}$	On-State Collector Current (Phototransistor Mode)	V_{CE} = 5 V, I_F = 1 mA	I_B = 0,	0.5			1		5	2		10	mA
		V_{CE} = 5 V, I_F = 2 mA,	I_B = 0, T_A = −55°C	0.7			1.4			2.8			
		V_{CE} = 5 V, I_F = 2 mA,	I_B = 0, T_A = 100°C	0.5			1			2			
		V_{CE} = 5 V, I_F = 10 mA,	I_B = 0, See Note 4		50			80			90		
$I_{C(on)}$	On-State Collector Current (Photodiode Mode)	V_{CB} = 5 V, I_E = 0	I_F = 10 mA,	30	80		30	80		30	80		μA
$I_{C(off)}$	Off-State Collector Current (Phototransistor Mode)	V_{CE} = 20 V, I_F = 0	I_B = 0,		6	100		6	100		6	100	nA
		V_{CE} = 20 V, I_F = 0,	I_B = 0, T_A = 100°C		4	100		4	100		4	100	μA
$I_{C(off)}$	Off-State Collector Current (Photodiode Mode)	V_{CB} = 20 V, I_F = 0	I_E = 0,		1	10		1	10		1	10	nA
V_F	Input Diode Static Forward Voltage	I_F = 10 mA,	T_A = −55°C	1		1.7	1		1.7	1		1.7	V
		I_F = 10 mA		0.8	1.4	1.5	0.8	1.4	1.5	0.8	1.4	1.5	
		I_F = 10 mA,	T_A = 100°C	0.7		1.3	0.7		1.3	0.7		1.3	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 0.5 mA, I_F = 2 mA	I_B = 0,			0.3							V
		I_C = 1 mA, I_F = 2 mA	I_B = 0,						0.3				
		I_C = 2 mA, I_F = 2 mA	I_B = 0,									0.3	
r_{io}	Input-to-Output Internal Resistance	V_{in-out} = ±1 kV, See Note 5		10^{11}	10^{12}		10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, See Note 5	f = 1 MHz,		2.5	5		2.5	5		2.5	5	pF

switching characteristics at 25°C free-air temperature (See Figure 1)

PARAMETER		TEST CONDITIONS		4N47			4N48			4N49			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
*t_r	Rise Time	V_{CC} = 10 V, R_L = 100 Ω,	$I_{F(on)}$ = 5 mA, Test Circuit A		10	20		10	20		15	25	μs
*t_f	Fall Time				10	20		10	20		15	25	μs
t_r	Rise Time	V_{CC} = 10 V, R_L = 100 Ω,	$I_{F(on)}$ = 5 mA, Test Circuit B		1	3		1	3		1	3	μs
t_f	Fall Time				1	3		1	3		1	3	μs

NOTES: 4. This parameter must be measured using pulse techniques, t_w = 100 μs, duty cycle ≤ 1%.

5. These parameters are measured between all the input diode leads shorted together and all the phototransistor leads shorted together.

*JEDEC registered data

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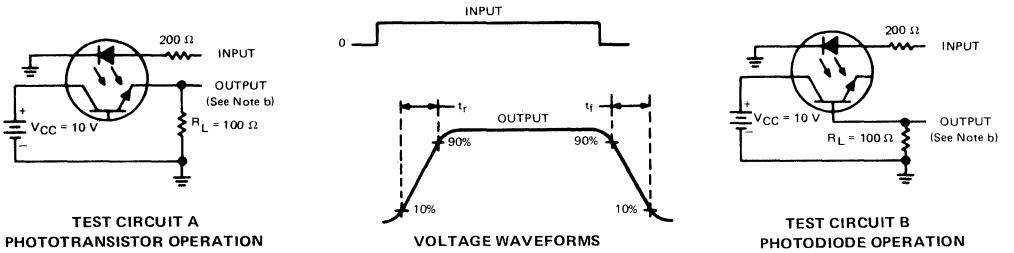
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%. For Test Circuit A, t_w = 100 μs. For Test Circuit B, t_w = 1 μs.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

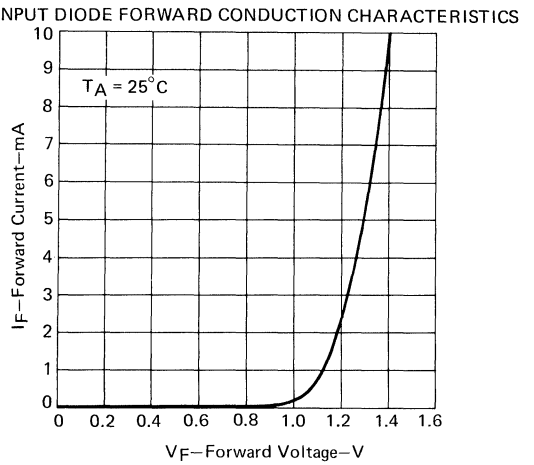


FIGURE 2

TYPICAL CHARACTERISTICS

4N48
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

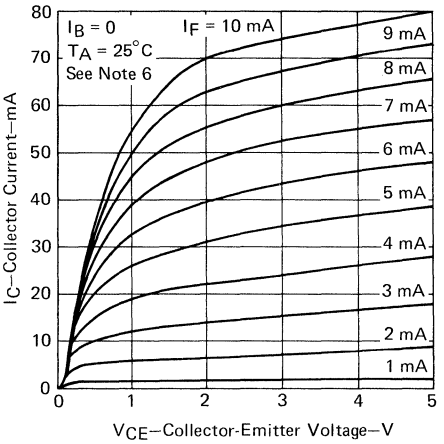


FIGURE 3

4N48
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

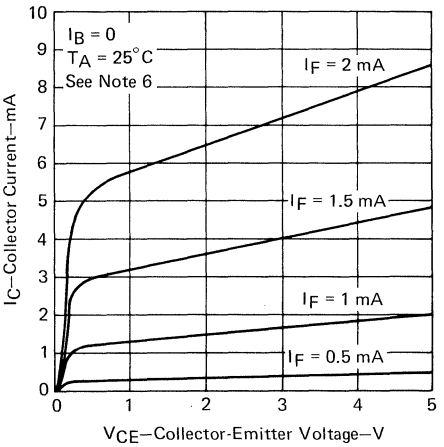


FIGURE 4

4N48
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

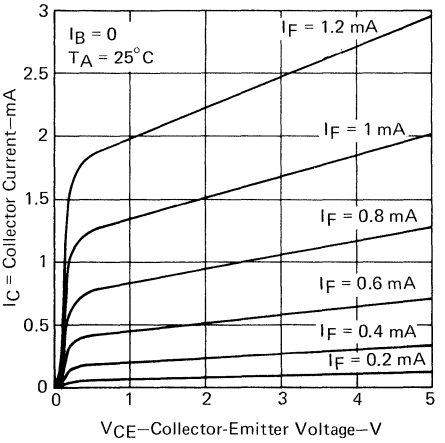


FIGURE 5

4N48
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

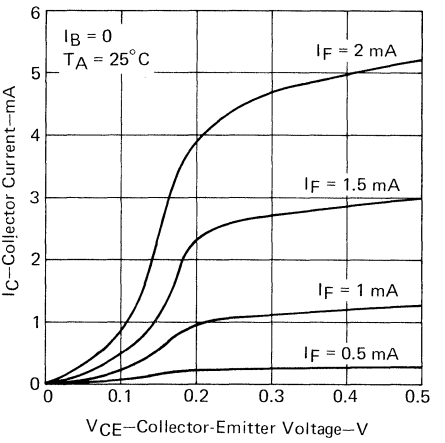


FIGURE 6

NOTE 6: This parameter was measured using pulse techniques, t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

4N48

COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

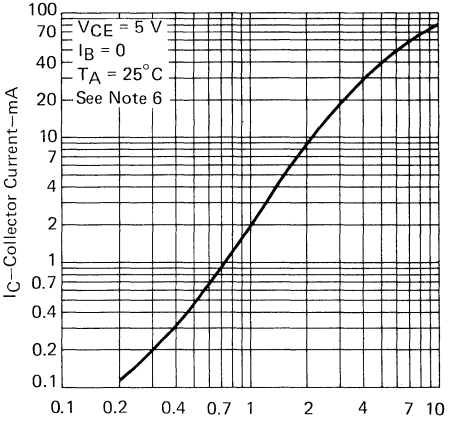


FIGURE 7

4N48

TRANSISTOR COLLECTOR CHARACTERISTICS

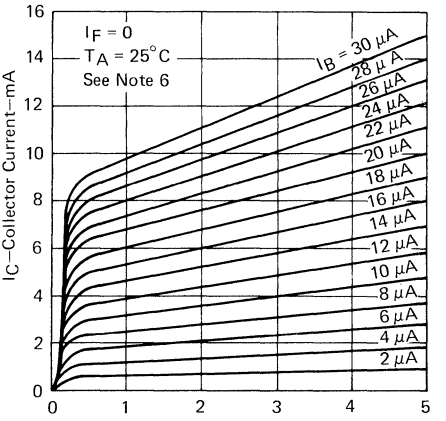


FIGURE 8

COLLECTOR CURRENT
vs
COLLECTOR-BASE VOLTAGE
(PHOTODIODE OPERATION)

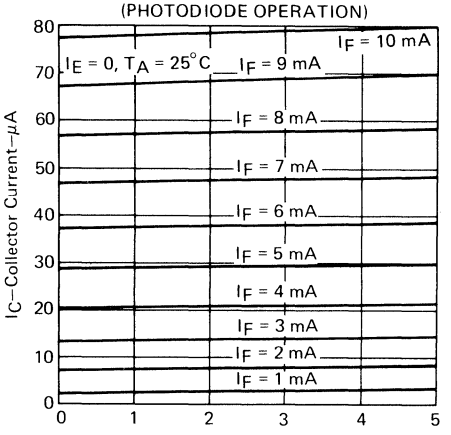


FIGURE 9

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

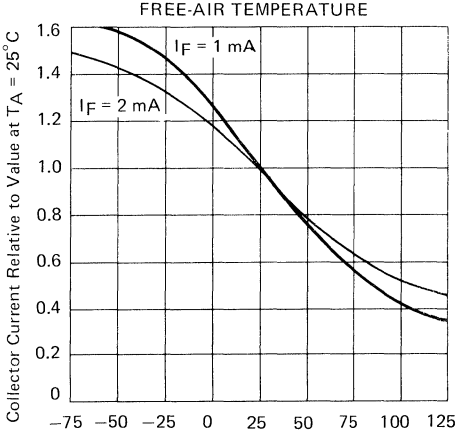


FIGURE 10

NOTE 6: This parameter was measured using pulse techniques. t_w = 100 μs, duty cycle = 1%.

This processing applies only to optocouplers ordered under part numbers shown below:

JAN4N47, JANTX4N47, JANTXV4N47
JAN4N48, JANTX4N48, JANTXV4N48
JAN4N49, JANTX4N49, JANTXV4N49

TEST (PER MIL-S-19500/548)	MIL-STD-750 TEST METHOD	JAN	JANTX	JANTXV
100% Processing				
Internal Visual	2072			X
Storage: T_A = 125°C, t = 24 hr	1032		X	X
Temperature Cycle: −55°C to 125°C, 10 cycles	1051		X	X
Constant Acceleration: 20,000 G, Y_1 axis	2006		X	X
High-Temperature Reverse Bias: I_F = 0, T_A = 125°C, V_{CB} = 36 V, t=48 hr	1039		X	X
Power Burn-in: I_F = 40 mA, P_D = 275 ±25 mW, t = 168 hr	1039		X	X
Hermetic Seal, Fine	1071 Cond. G or H		X	X
Hermetic Seal, Gross	1071 Cond. C or D		X	X
Monitored Thermal Shock	Para. 4.2.1.1.*	X	X	X
External Visual	2071		X	X
Product Acceptance				
Group A: LTPD = 5				
External Visual	2071	X	X	X
Electrical: T_A = 25°C	as needed	X	X	X
Electrical: T_A = 100°C	as needed	X	X	X
Electrical: T_A = −55°C	as needed	X	X	X
Group B-1: LTPD = 15				
Solderability	2026	X	X	X
Resistance to Solvents	1022	X	X	X
Group B-2: LTPD = 10				
Thermal Shock	1051 Cond. B-1	X	X	X
Hermetic Seal, Fine	1071 Cond. G or H	X	X	X
Hermetic Seal, Gross	1071 Cond. C or D	X	X	X
Group B-3:				
Isolation Voltage: V_{IO} = 150 V, T_A = 125°C, t = 24, LTPD = 20	1016	X	X	X
Steady State Operating Life: t = 340 hr, LTPD = 5	1027	X	X	X
Group B-4:				
Decap, Internal Visual; Design Verification		X	X	X
1 Device/0 Failure	2075	X	X	X
Bond Strength LTPD = 20 (C = 0)	2037 Cond. A	X	X	X
Group B-5: Not Applicable				
Group B-6: LTPD = 7				
High-Temperature Life (Nonoperating) t = 340 hr	1032	X	X	X

*MIL-S-19500/548

TEST (PER MIL-S-19500/548)	MIL-STD-750 TEST METHOD	JAN	JANTX	JANTXV
(Group C Tests are run on one lot every six months)				
Group C-1: LTPD = 15				
Physical Dimensions	2066	X	X	X
Group C-2: LTPD = 10				
Thermal Shock (Glass Strain)	1056 Cond. A	X	X	X
Terminal Strength	2036 Cond. E	X	X	X
Hermetic Seal, Fine	1071 Cond. G or H	X	X	X
Hermetic Seal, Gross	1071 Cond. C or D	X	X	X
Moisture Resistance	1021	X	X	X
External Visual	2071	X	X	X
Group C-3: LTPD = 10				
Shock: 1500 G	2016	X	X	X
Vibration: 50 G	2056	X	X	X
Acceleration: 30000 G	2006	X	X	X
Group C-4: LTPD = 15				
Salt Atmosphere	1041	X	X	X
Group C-5: Not Applicable				
Group C-6: λ = 10				
Steady State Operating Life	1026	X	X	X

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D2918, JULY 1986—REVISED JULY 1989

- **Compatible with TTL Inputs**
- **High-Speed Switching . . . 1 Mbit/s Typ**
- **Bandwidth . . . 2 MHz Typ**
- **High Common-Mode Transient Immunity . . . 1000 V/μs Typ**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **Open-Collector Output**
- **UL Recognized . . . File Number 65085**

description

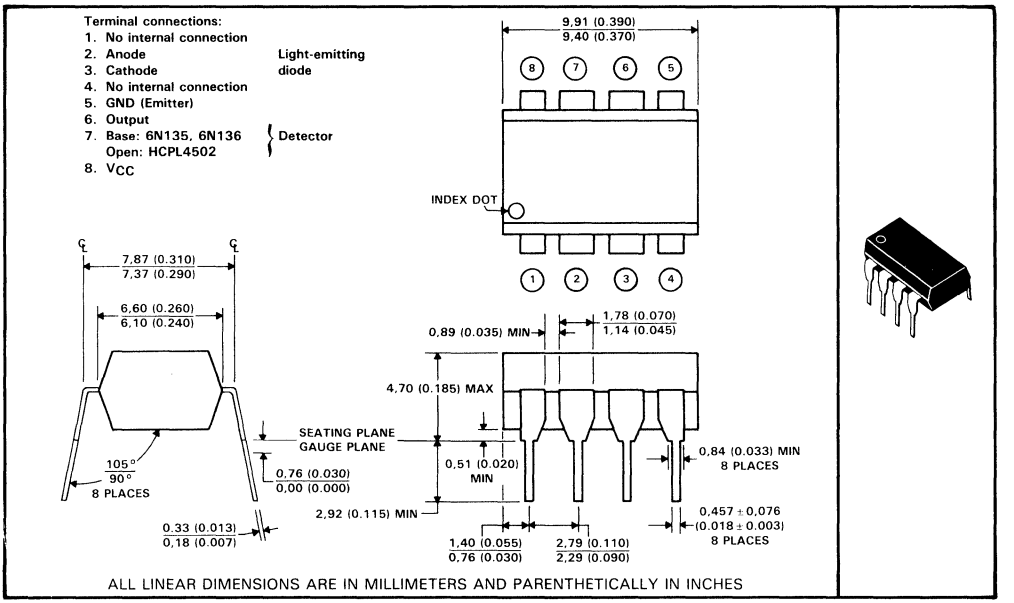
These high-speed optocouplers are designed for use in analog or digital interface applications that require high-voltage isolation between the input and output. Applications include line receivers that require high common-mode transient immunity, and analog or logic circuits that require input-to-output electrical isolation.

The 6N135, 6N136, and HCPL4502 optocouplers each consists of a light-emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor collector output. This feature, which reduces the transistor base-to-collector capacitance, results in speeds up to one hundred times that of a conventional phototransistor optocoupler.

The 6N135 is designed for TTL/CMOS, TTL/LSTTL, and wide-band analog applications.

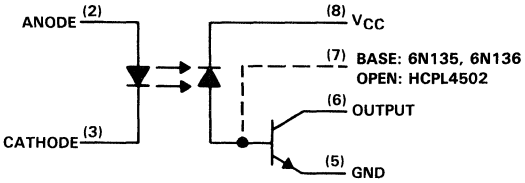
The 6N136 and HCPL4502 are designed for high-speed TTL/TTL applications. The HCPL4502 has no base connection.

*mechanical data



*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

schematic



***absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Supply and output voltage range, V_{CC} and V_O	−0.5 V to 15 V
Reverse input voltage	5 V
Emitter-base reverse voltage	5 V
Peak input forward current (pulse duration = 1 ms, 50% duty cycle, see Note 1)	50 mA
Peak transient input forward current (pulse duration 1 μs, 300 Hz)	1 A
Average forward input current (see Note 2)	25 mA
Peak output current	16 mA
Average output current	8 mA
Base current	5 mA
Input power dissipation at (or below) 70°C free-air temperature (see Note 3)	45 mW
Output power dissipation at (or below) 70°C free-air temperature (see Note 4)	100 mW
Storage temperature range	−55°C to 125°C
Operating free-air temperature range	−55°C to 100°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

*JEDEC registered data for 6N135 and 6N136

NOTES: 1. Derate linearly above 70°C free-air temperature at the rate of 1.67 mA/°C.
2. Derate linearly above 70°C free-air temperature at the rate of 0.83 mA/°C.
3. Derate linearly above 70°C free-air temperature at the rate of 1.50 mW/°C.
4. Derate linearly above 70°C free-air temperature at the rate of 3.33 mW/°C.

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electrical characteristics over operating free-air temperature range of 0 °C to 70 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		6N135			6N136, HCPL4502			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
*V_F	Input forward voltage	I_F = 16 mA,	T_A = 25°C		1.6	1.7		1.6	1.7	V
α_{VF}	Temperature coefficient of forward voltage	I_F = 16 mA			−1.8			−1.8		mV/°C
*V_{BR}	Input breakdown voltage	I_R = 10 μA,	T_A = 25°C	5			5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_F = 16 mA, I_B = 0	I_{OL} = 1.1 mA		0.1	0.4				V
			I_{OL} = 2.4 mA					0.1	0.4	
*I_{OH}	High-level output current	I_F = 0, I_B = 0, T_A = 25°C	V_{CC} = VO = 5.5 V		3	500		3	500	nA
			V_{CC} = V_O = 15 V		0.01	1		0.01	1	μA
I_{OH}	High-level output current	V_{CC} = 15 V, I_F = 0,	V_O = 15 V, I_B = 0			50			50	μA
*I_{CCH}	Supply current, high-level output	V_{CC} = 15 V, I_F = 0, T_A = 25°C	I_O = 0, I_B = 0,		0.02	1		0.02	1	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 15 V, I_F = 0,	I_O = 0, I_B = 0			2			2	μA
I_{CCL}	Supply current, low-level output	V_{CC} = 15 V, I_F = 16 mA,	I_O = 0, I_B = 0		40			40		μA
h_{FE}	Transistor forward current transfer ratio	V_O = 5 V,	I_O = 3 mA		100			100 (6N136 only)		
*CTR	Current transfer ratio	V_{CC} = 4.5 V, I_F = 16 mA, T_A = 25°C,	V_O = 0.4 V, I_B = 0, See Note 5	7%	18%		19%	24%		%
CTR	Current transfer ratio	V_{CC} = 4.5 V, I_F = 16 mA, See Note 5	V_O = 0.5 V, I_B = 0,	5%			15%			%
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 6	T_A = 25°C,		10^{12}			10^{12}		Ω
*I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, See Note 6	t = 5 s, RH = 45%,			1			1	μA
C_i	Input capacitance	V_F = 0,	f = 1 MHz		60			60		pF
C_{io}	Input-output capacitance	f = 1 MHz,	See Note 6		0.6			0.6		pF

† All typical values are at T_A = 25°C.
*JEDEC registered data for 6N135 and 6N136
NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.

operating characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C

PARAMETER		TEST CONDITIONS	6N135			6N136, HCPL4502			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Bandwidth (−3 dB)	R_L = 100 Ω, See Note 7		2			2		MHz

NOTE 7: Bandwidth is the range of frequencies within which the ac output voltage is not more than 3 dB below the low-frequency value.

switching characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	6N135			6N136, HCPL4502			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
*t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 4.1 kΩ, See Figure 1 See Note 8,		1.0	1.5				μs
		R_L = 1.9 kΩ, See Figure 1 See Note 9,					0.6	0.8	
*t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 4.1 kΩ, See Figure 1 See Note 8,		0.7	1.5				μs
		R_L = 1.9 kΩ, See Figure 1 See Note 9,					0.6	0.8	
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, R_L = 4.1 kΩ, See Figure 2 I_F = 0, See Notes 8 and 10,	1000						V/μs
		ΔV_{CM} = 10 V, R_L = 1.9 kΩ, See Figure 2 I_F = 0, See Notes 9 and 10,					−1000		
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = 10 V, R_L = 4.1 kΩ, See Figure 2, See Notes 8 and 10,	−1000						V/μs
		ΔV_{CM} = 10 V, R_L = 1.9 kΩ, See Figure 2, See Notes 9 and 10					−1000		

*JEDEC registered data for 6N135 and 6N136

NOTES: 8. The 4.1-kΩ load represents one LSTTL unit load of 0.36 mA and a 6.1-kΩ pullup resistor.
9. The 1.9-kΩ load represents one TTL unit load of 1.6 mA and a 5.6-kΩ pullup resistor.
10. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

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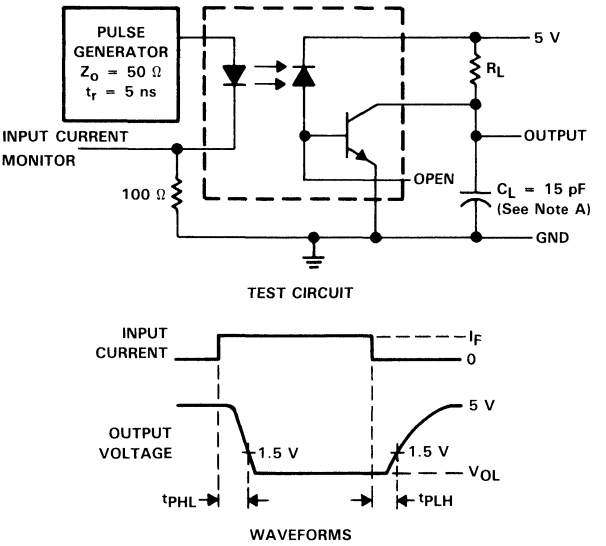
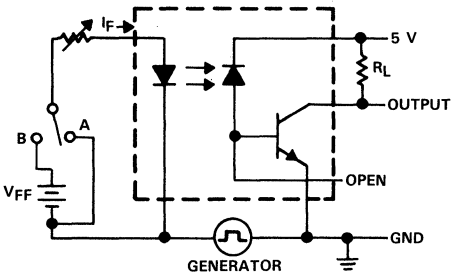
PARAMETER MEASUREMENT INFORMATION



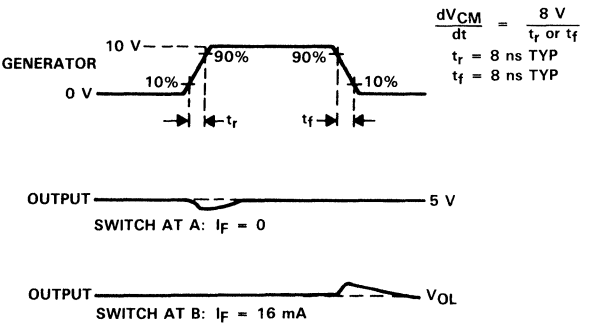
NOTE A: C_L includes probe and stray capacitance.

FIGURE 1. SWITCHING TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

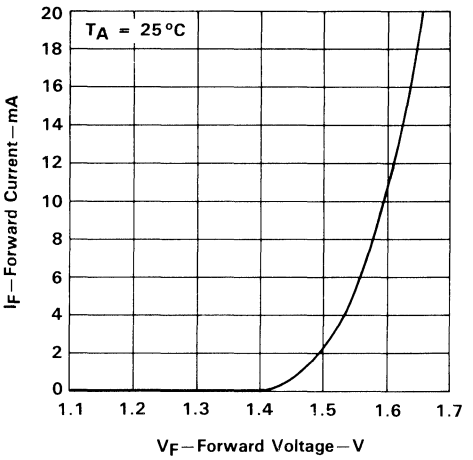


FIGURE 3

6N135
CURRENT TRANSFER CHARACTERISTICS

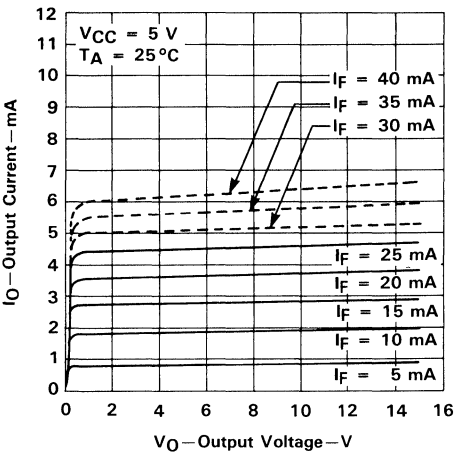


FIGURE 4

NORMALIZED CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

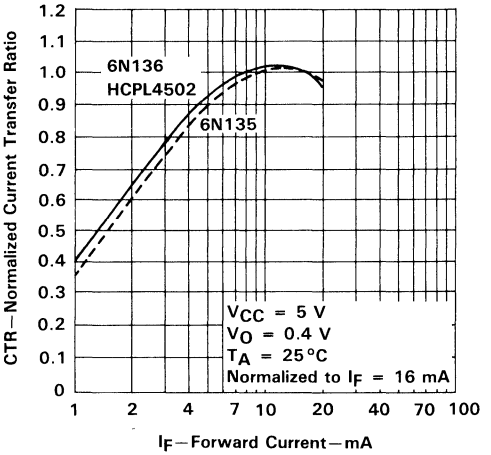


FIGURE 5

NORMALIZED CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

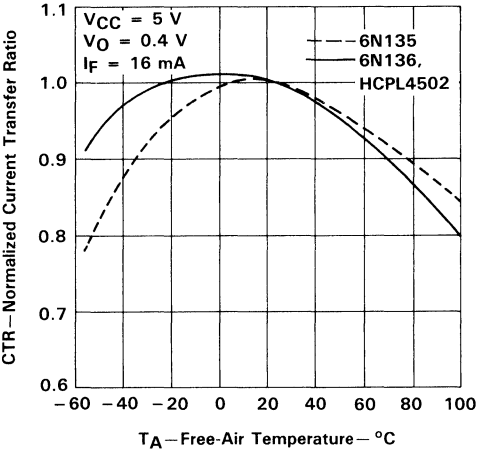


FIGURE 6

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

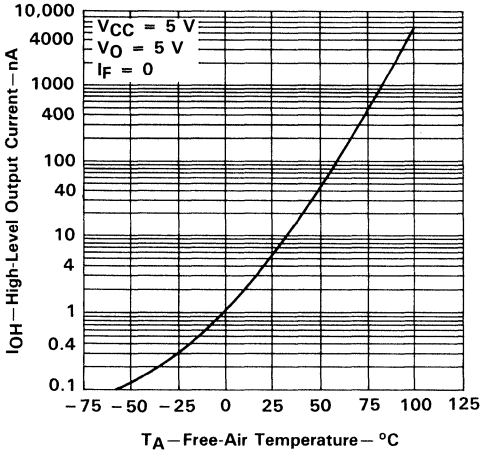


FIGURE 7

DIFFERENTIAL CURRENT TRANSFER RATIO
vs
INPUT DIODE QUIESCENT FORWARD CURRENT

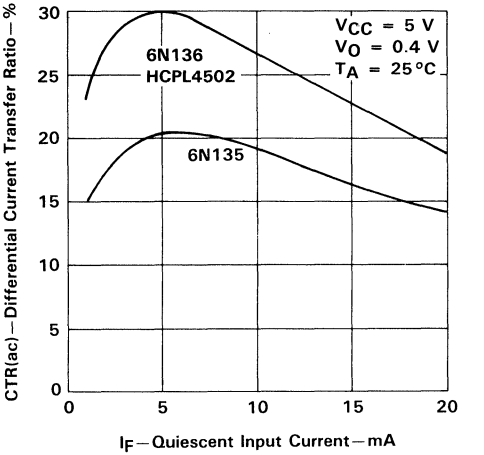


FIGURE 8

NORMALIZED FREQUENCY RESPONSE
vs
LOAD RESISTANCE

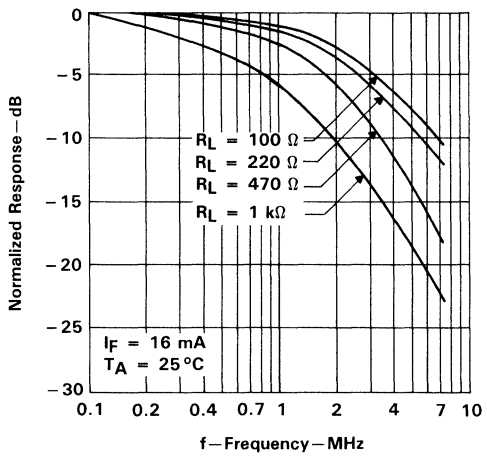


FIGURE 9

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

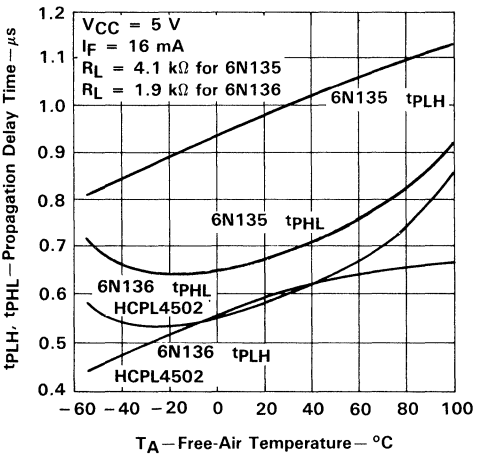


FIGURE 10

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2919, JULY 1986

- **Gallium Arsenide Phosphide LED Optically Coupled to Integrated Circuit Detector**
- **Compatible with TTL and LSTTL Inputs**
- **Low Input Current Required to Turn Output On . . . 5 mA Max**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High-Speed Switching . . . 75 ns Max**
- **Plastic Dual-In-Line Package**
- **UL Recognized . . . File Number 65085**

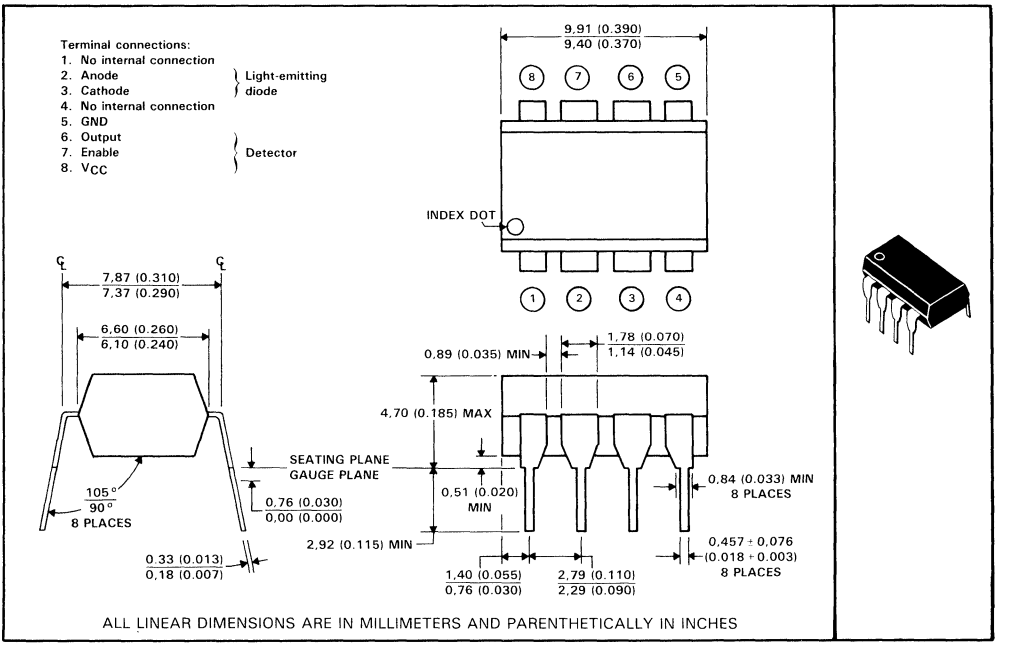
description

The 6N137 optocoupler is designed for use in high-speed digital interfacing applications that require high-voltage isolation between the input and output. Applications include line receivers, microprocessors or computer interface, digital programming of floating power supplies, motors, and other control systems.

The 6N137 high-speed optocoupler consists of a GaAsP light-emitting diode and an integrated light detector composed of a photodiode, a high-gain amplifier, and a Schottky-clamped open-collector output transistor. An input diode forward current of 5 milliamperes will switch the output transistor low, providing an on-state drive current of 13 milliamperes (eight 1.6-milliampere TTL loads). A TTL-compatible enable input is provided for applications that require output-transistor gating.

The 6N137 is characterized for operation over the temperature range of 0°C to 70°C.

*mechanical data



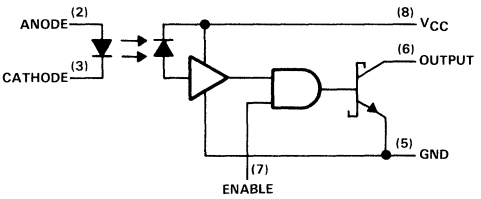
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

FUNCTION TABLE

INPUT	ENABLE	OUTPUT
$I_{F(on)}$	H	L
$I_{F(off)}$	X	H
X	L	H

logic diagram (positive logic)



***absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V_{CC} . . . . . 7 V
Reverse input voltage . . . . . 5 V
Enable input voltage (not to exceed V_{CC} by more than 500 mV) . . . . . 5.5 V
Output voltage . . . . . 7 V
Peak forward input current (≤ 1 ms duration) (TI-guaranteed value) . . . . . 40 mA
(JEDEC-registered value) . . . . . 20 mA
Average forward input current (TI-guaranteed value) . . . . . 20 mA
(JEDEC-registered value) . . . . . 10 mA
Output current . . . . . 50 mA
Output power dissipation . . . . . 85 mW
Storage temperature range . . . . . −55°C to 125°C
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

*JEDEC registered data

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Output supply voltage (see Note 1)	4.5	5	5.5	V
$V_{IH(EN)}$	High-level enable input voltage (see Note 2)	2		V_{CC}	V
$V_{IL(EN)}$	Low-level enable input voltage	0		0.8	V
$I_{F(on)}$	Input forward current to turn output on	6.3		15	mA
$I_{F(off)}$	Input forward current to turn output off	0		250	μA
I_{OL}	Low-level (on-state) output current			13	mA
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. All voltage values are with respect to GND (pin 5).
2. No external pullup is required at the enable input; an open circuit will establish the high level.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
*V_F	Input forward voltage	I_F = 10 mA, T_A = 25°C		1.6	1.75	V
αV_F	Temperature coefficient of forward voltage	I_F = 10 mA		−1.8		mV/°C
*V_{BR}	Input reverse breakdown voltage	I_R = 10 μA, T_A = 25°C	5			V
*V_{OL}	Low-level output voltage	V_{CC} = 5.5 V, $V_{(EN)}$ = 2 V, I_F = 5 mA, I_{OL} = 13 mA		0.23	0.6	V
*I_{OH}	High-level output current	V_{CC} = 5.5 V, V_O = 5.5 V, $V_{(EN)}$ = 2 V, I_F = 250 μA			250	μA
$I_{IH(EN)}$	High-level enable input current	V_{CC} = 5.5 V, $V_{(EN)}$ = 2 V		−0.2		mA
*$I_{IL(EN)}$	Low-level enable input current	V_{CC} = 5.5 V, $V_{(EN)}$ = 0.5 V		−0.5	−2	mA
*I_{CCH}	Supply current, high-level output	V_{CC} = 5.5 V, $V_{(EN)}$ = 0.5 V, I_F = 0		10	15	mA
*I_{CCL}	Supply current, low-level output	V_{CC} = 5.5 V, $V_{(EN)}$ = 0.5 V, I_F = 10 mA		13	18	mA
*I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, t = 5 s, T_A = 25°C, RH = 45%, See Note 1			1	μA
r_{IO}	Input-output resistance	V_{IO} = 500 V, T_A = 25°C, See Note 1		10^{12}		Ω
C_i	Input capacitance	V_F = 0, f = 1 MHz		60		pF
C_{io}	Input-output capacitance	f = 1 MHz, T_A = 25°C, See Note 1		0.6		pF

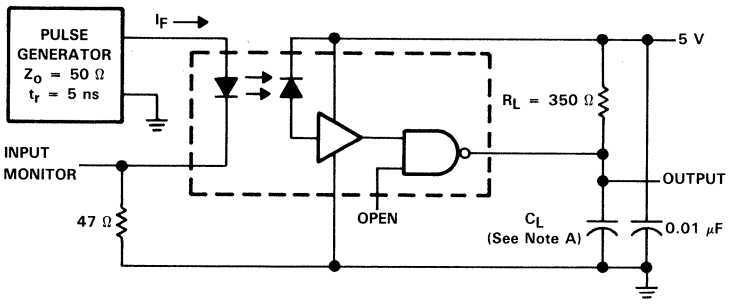
*JEDEC registered data
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

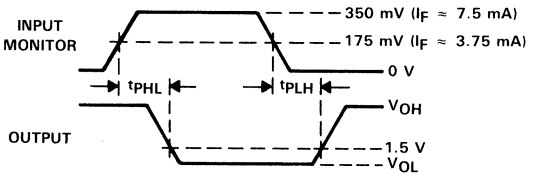
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
*t_{PLH}	Propagation delay time, low-to-high-level output, from LED input	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 1		42	75	ns
*t_{PHL}	Propagation delay time, high-to-low level output, from LED input	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 1		42	75	ns
$t_{PLH(EN)}$	Propagation delay time, low-to-high level output, from enable	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 2		40		ns
$t_{PHL(EN)}$	Propagation delay time, high-to-low-level output, from enable	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 2		25		ns
t_r	Rise time	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF		20		ns
t_f	Fall time	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF		30		ns
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, I_F = 0, R_L = 350 Ω, See Note 2 and Figure 3		50		V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = −10 V, I_F = 5 mA, R_L = 350 Ω, See Note 2 and Figure 3		−150		V/μs

*JEDEC registered data
NOTE 2: Common-mode input transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

PARAMETER MEASUREMENT INFORMATION

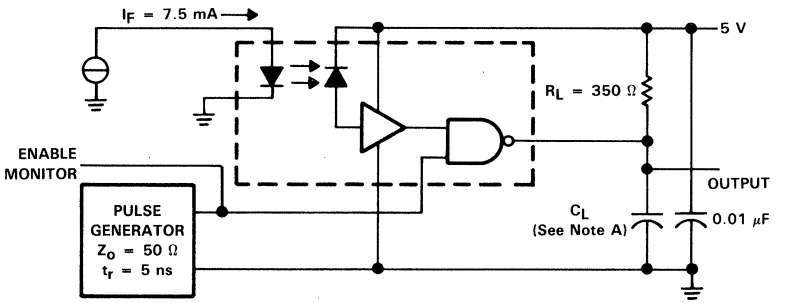


TEST CIRCUIT

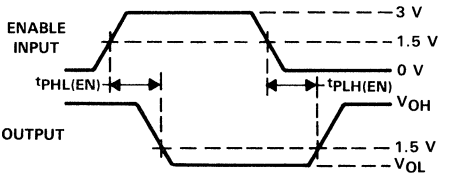


VOLTAGE WAVEFORMS

FIGURE 1. t_{PLH} AND t_{PHL} FROM LED INPUT TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. $t_{PLH(EN)}$ AND $t_{PHL(EN)}$ FROM ENABLE TEST CIRCUIT AND WAVEFORMS

NOTE A: C_L is approximately 15 pF, which includes probe and stray wiring capacitances.

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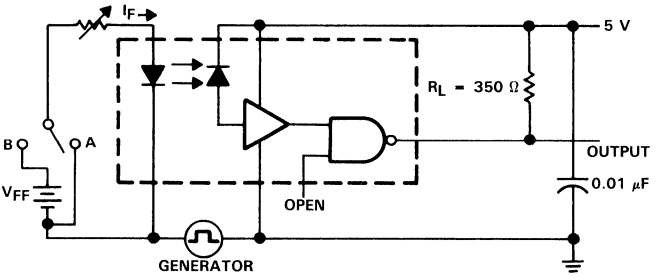
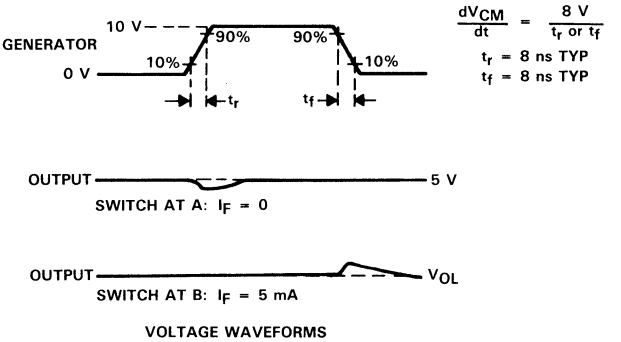
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION INFORMATION

A ceramic capacitor (0.01 μF to 0.1 μF) should be connected between pins 8 and 5 to stabilize the high-gain amplifier. The total lead length between the capacitor and the optocoupler should not exceed 20 mm (0.8 inches). Failure to provide a bypass capacitor may result in impaired switching characteristics.

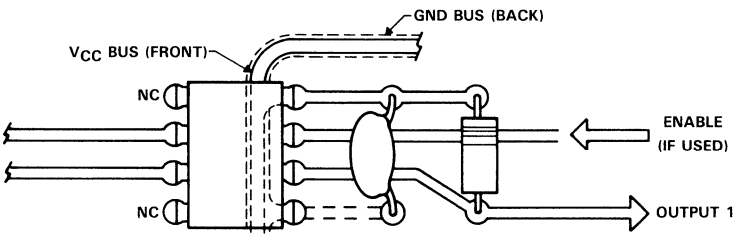


FIGURE 4. RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

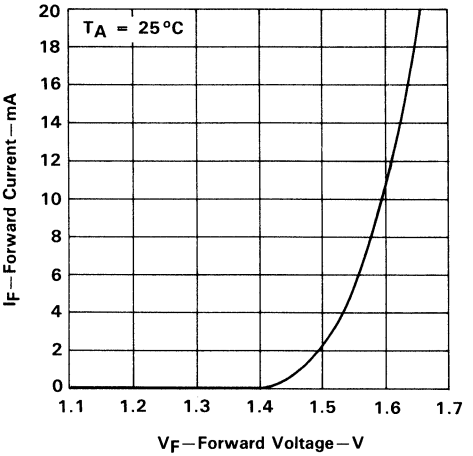


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

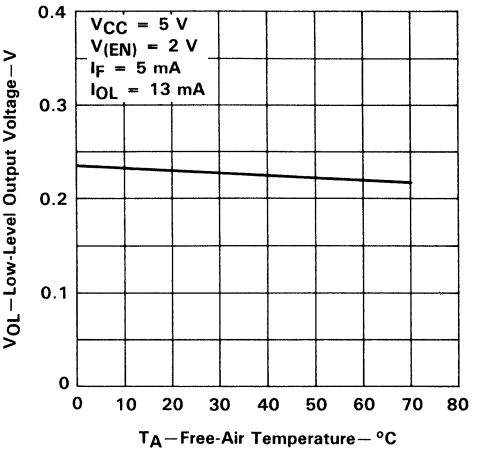


FIGURE 6

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

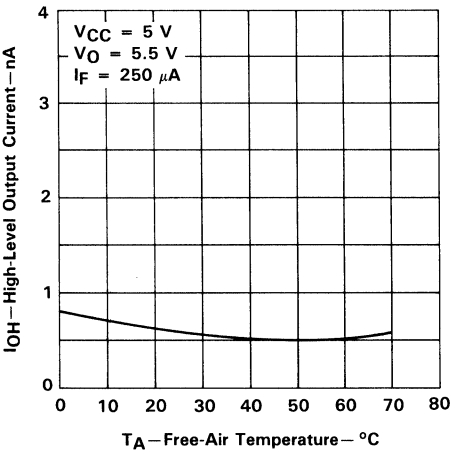


FIGURE 7

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME FROM LED INPUT
vs
PULSE FORWARD CURRENT

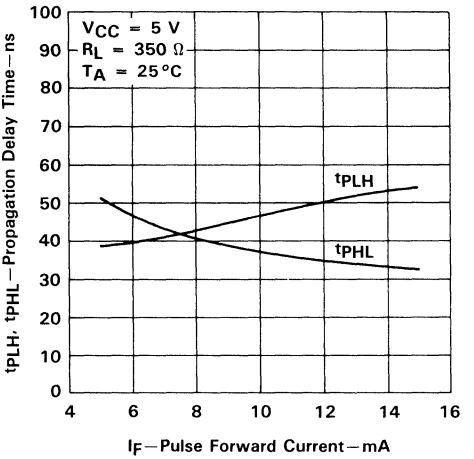


FIGURE 8

PROPAGATION DELAY TIME FROM LED INPUT
vs
LOAD RESISTANCE

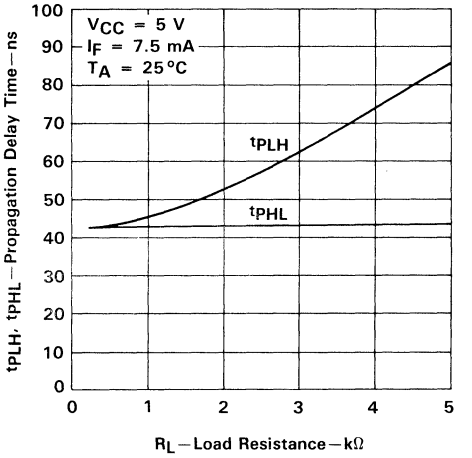


FIGURE 9

D3012, JULY 1986

- **Compatible with TTL Inputs**
- **High Current Transfer Ratio . . . 800% Typ at I_F = 0.5 mA**
- **High-Speed Switching . . . 100 kbit/s Typ**
- **High Common-Mode Transient Immunity . . . 500 V/μs Typ**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High Output Current Rating of 60 mA**
- **UL Recognized . . . File Number 65085**

description

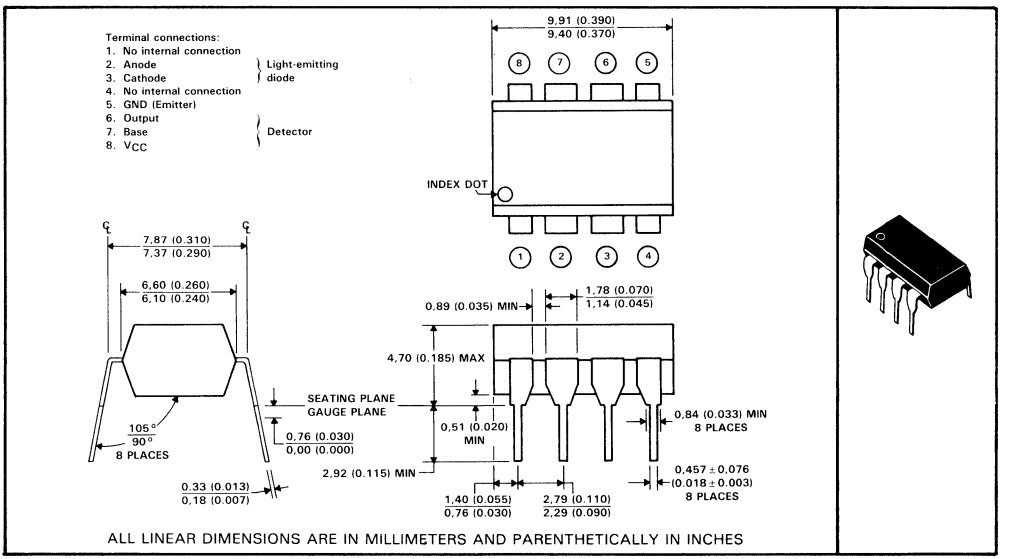
These devices are useful where large common-mode input signals exist, and in applications that require high-voltage isolation between circuits. Applications include line receivers, telephone ring detectors, power line monitors, high-voltage status indicators, and circuits that require isolation between input and output.

The 6N138 and 6N139 high-gain optocouplers each consists of a GaAsP light-emitting diode and an integrated high-gain photon detector composed of a photodiode and a split-Darlington output stage. The V_{CC} and output terminals may be tied together to achieve conventional photodarlington operation. A separate base access terminal allows gain-bandwidth adjustments.

The 6N138 is designed for use primarily in TTL applications. An LED input current of 1.6 milliamperes and a current-transfer ratio of 300% from 0°C to 70°C allows operation with one TTL load input and one TTL load output utilizing a 2.2-kΩ pullup resistor.

The 6N139 is designed for use in CMOS, LSTTL, or other low-power applications. This device has a minimum current-transfer ratio of 400% for only 0.5 milliampere input current over an operating temperature range of 0°C to 70°C.

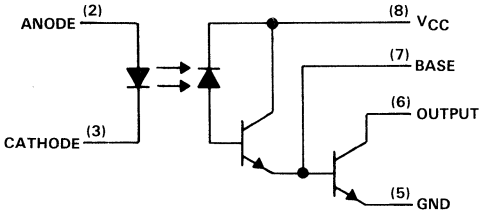
*mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

schematic



***absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Supply and output voltage range, V_{CC} and V_O: 6N138	−0.5 V to 7 V
6N139	−0.5 to 18 V
Reverse input voltage	5 V
Emitter-base reverse voltage	0.5 V
Peak input forward current (pulse duration = 1 ms, 50% duty cycle)	40 mA
Peak transient input forward current (pulse duration ≤ 1 μs, 300 pps)	1 A
Average forward input current at (or below) 50°C free-air temperature (see Note 1)	20 mA
Output current at (or below) 25°C free-air temperature (see Note 2)	60 mA
Input power dissipation at (or below) 50°C free-air temperature (see Note 3)	35 mW
Output power dissipation at (or below) 25°C free-air temperature (see Note 4)	100 mW
Storage temperature range	−55°C to 125°C
Operating temperature range	0°C to 100°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Derate linearly above 50°C free-air temperature at a rate of 0.4 mA/°C.
2. Derate linearly above 25°C free-air temperature at a rate of 0.8 mA/°C.
3. Derate linearly above 50°C free-air temperature at a rate of 0.7 mW/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 1.33 mW/°C.

*JEDEC registered data.

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electrical characteristics over operating free-air temperature range of 0 °C to 70 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	6N138			6N139			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
*V_F	Input forward voltage	I_F = 1.6 mA, T_A = 25°C		1.5	1.7		1.5	1.7	V
αV_F	Temperature coefficient of forward voltage	I_F = 1.6 mA		−1.8			−1.8		mV/°C
*V_{BR}	Input breakdown voltage	I_R = 10 μA, T_A = 25°C	5			5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_F = 1.6 mA, I_{OL} = 4.8 mA, I_B = 0		0.1	0.4				V
		V_{CC} = 4.5 V, I_F = 1.6 mA, I_{OL} = 6.4 mA, I_B = 0					0.1	0.4	
		V_{CC} = 4.5 V, I_F = 5 mA, I_{OL} = 15 mA, I_B = 0					0.1	0.4	
		V_{CC} = 4.5 V, I_F = 12 mA, I_{OL} = 24 mA, I_B = 0					0.2	0.4	
*I_{OH}	High-level output current	V_{CC} = 7 V, V_O = 7 V, I_F = 0, I_B = 0		0.1	250				μA
		V_{CC} = 18 V, V_O = 18 V, I_F = 0, I_B = 0					0.05	100	
*I_{CCH}	Supply current, high-level output	V_{CC} = 5 V, V_O open, I_F = 0, I_B = 0		10			10		nA
I_{CCL}	Supply current, low-level output	V_{CC} = 5 V, V_O open, I_F = 1.6 mA, I_B = 0		0.2			0.2		mA
*CTR	Current transfer ratio	V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 0.5 mA, I_B = 0, See Note 5				400%	1650%		
		V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 1.6 mA, I_B = 0, See Note 5	300%	1300%		500%	1400%		
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 6		10^{12}			10^{12}		Ω
*I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, t = 5 s, RH = 45%, See Note 6			1			1	μA
C_i	Input capacitance	V_F = 0, f = 1 MHz		60			60		pF
C_{io}	Input-output capacitance	f = 1 MHz, See Note 6		0.6			0.6		pF

*JEDEC registered data
†All typical values are at V_{CC} = 5 V, T_A = 25°C, unless otherwise noted.
NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.

*switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	6N138			6N139			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
*t_{PHL}	Propagation delay time, high-to-low level output	I_F = 1.6 mA, R_L = 2.2 kΩ, See Figure 1		2	10				μs
		I_F = 0.5 mA, R_L = 4.7 kΩ, See Figure 1					4	25	
		I_F = 12 mA, R_L = 270 Ω, See Figure 1					0.3	1	
*t_{PLH}	Propagation delay time, low-to-high-level output	I_F = 1.6 mA, R_L = 2.2 kΩ, See Figure 1		4	35				μs
		I_F = 0.5 mA, R_L = 4.7 kΩ, See Figure 1					10	60	
		I_F = 12 mA, R_L = 270 Ω, See Figure 1					3.5	7	
$\frac{dV_{CM}}{dt}$(H)	Common-mode input Transient immunity, high-level output	V_{CM} = 10 Vp-p, I_F = 0, R_L = 2.2 kΩ, See Figure 2 See Notes 7 and 8,		500			500		V/μs
$\frac{dV_{CM}}{dt}$(L)	Common-mode input transient immunity, low-level output	V_{CM} = Vp-p, R_L = 2.2 kΩ, See Figure 2, See Notes 7 and 8		−500			−500		V/μs

*JEDEC registered data

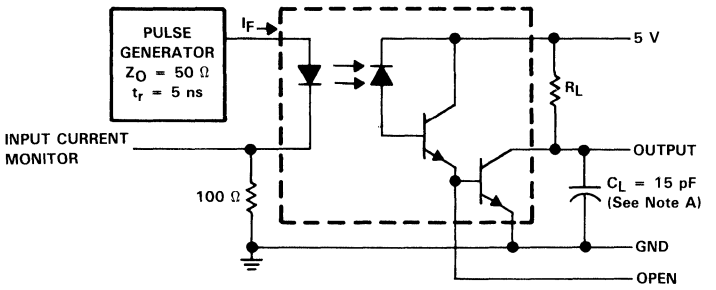
NOTES: 7. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

8. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is:

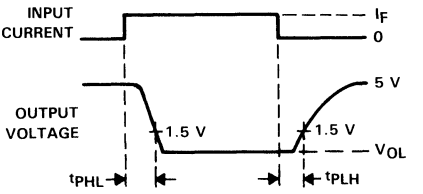
$$R_{CC} \approx \frac{1}{0.15\ I_F\ (mA)}\ k\Omega$$

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

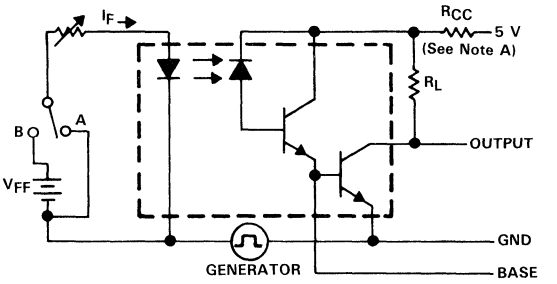


WAVEFORMS

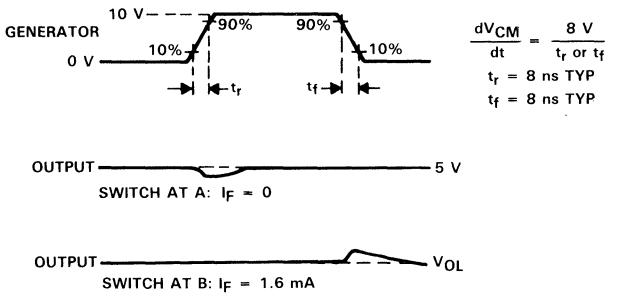
NOTE A: C_L includes probe and stray capacitances.

FIGURE 1. SWITCHING TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is:

$$R_{CC} \approx \frac{1}{0.15\ I_F\ (mA)}\ k\Omega$$

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

6N138
CURRENT TRANSFER CHARACTERISTICS

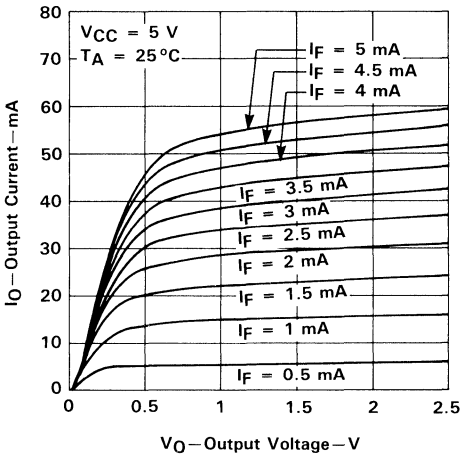


FIGURE 3

6N139
CURRENT TRANSFER CHARACTERISTICS

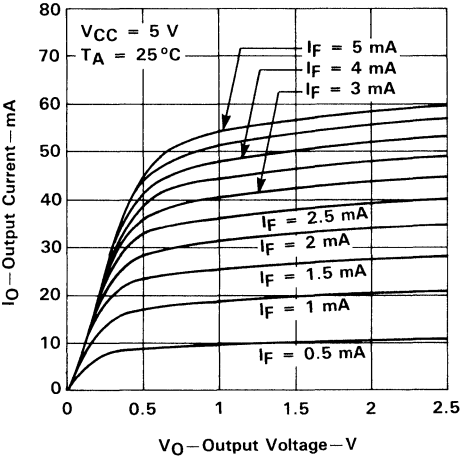


FIGURE 4

6N138
CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

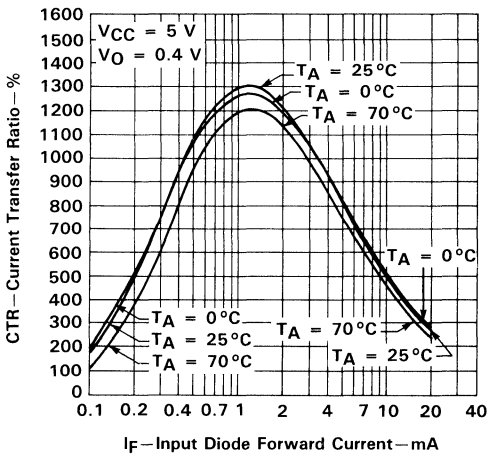


FIGURE 5

6N139
CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

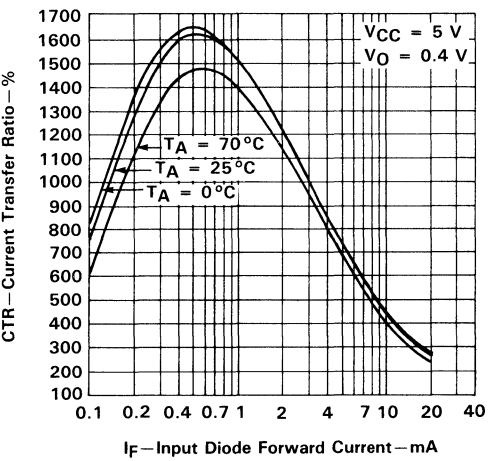


FIGURE 6

3 Optocouplers (Isolators)

TYPICAL CHARACTERISTICS

6N138
OUTPUT CURRENT
vs
INPUT DIODE FORWARD CURRENT

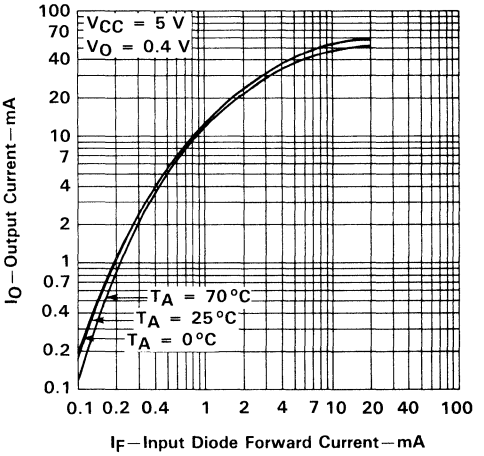


FIGURE 7

6N139
OUTPUT CURRENT
vs
INPUT DIODE FORWARD CURRENT

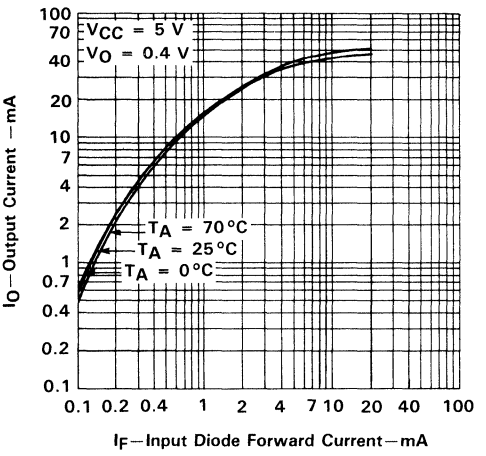


FIGURE 8

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

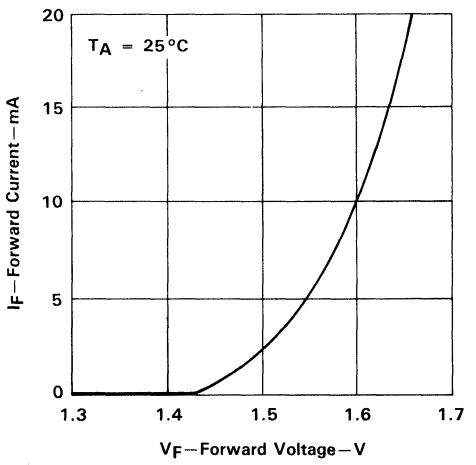


FIGURE 9

6N138
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

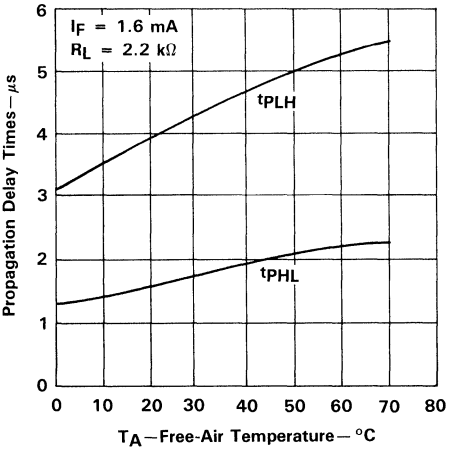


FIGURE 10

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

6N139
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

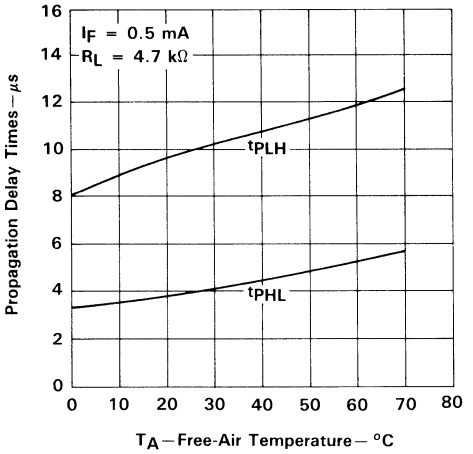


FIGURE 11

6N139
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

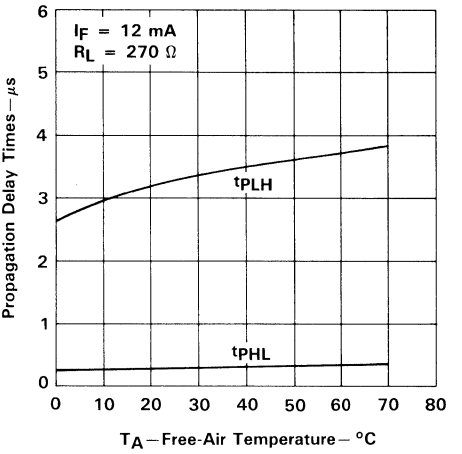


FIGURE 12

D2963, NOVEMBER 1986

- **Compatible with TTL Inputs**
- **High-Speed Switching . . . 1 Mbit/s Typ**
- **Narrow CTR Range**
- **Bandwidth . . . 2 MHz Typ**
- **High Common-Mode Transient Immunity . . . 1000 V/μs Typ**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **Open-Collector Output**
- **UL Recognized . . . File Number E65085**
- **Directly Interchangeable with Hewlett Packard HCPL2502**

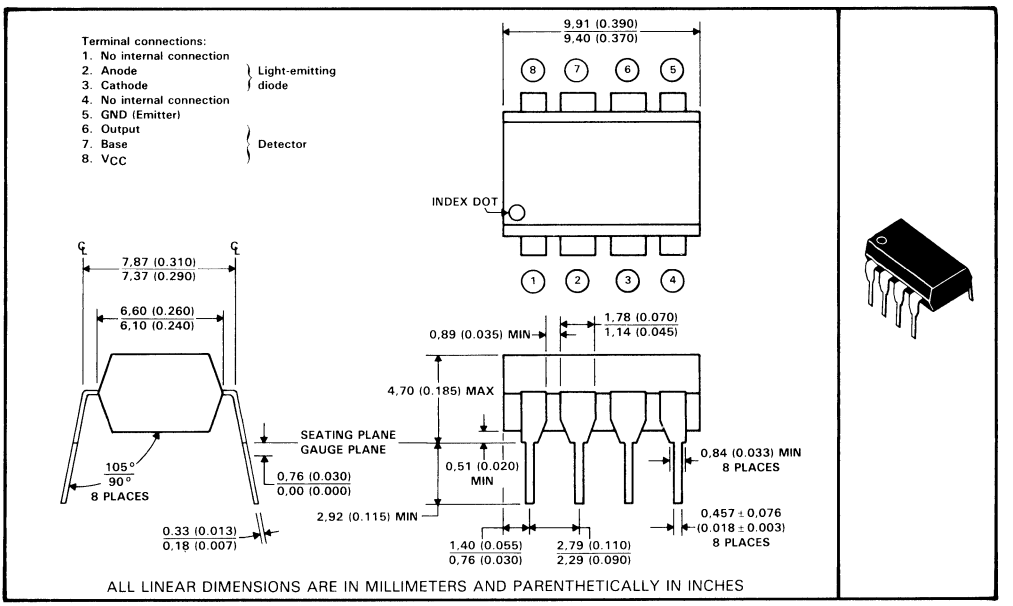
description

These high-speed optocouplers are designed for use in analog or digital interface applications that require high-voltage isolation between the input and output. Applications include line receivers that require high common-mode transient immunity, and analog or logic circuits that require input-to-output electrical isolation.

The HCPL2502 optocoupler consists of a light-emitting diode and an integrated photon detector composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor collector output. This feature, which reduces the transistor base-to-collector capacitance, results in speeds up to one hundred times that of a conventional phototransistor optocoupler.

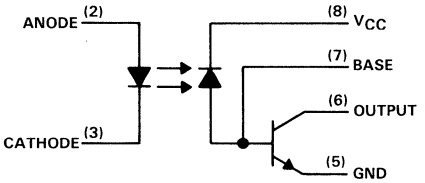
The HCPL2502 is designed for high-speed TTL/TTL applications where matched or known CTR is desired. CTR is 15 to 22% at I_F = 16 mA.

mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

schematic



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply and output voltage range, V_{CC} and V_O	−0.5 V to 15 V
Reverse input voltage	5 V
Emitter-base reverse voltage	5 V
Peak input forward current (pulse duration = 1 ms, 50% duty cycle, see Note 1)	50 mA
Peak transient input forward current (pulse duration 1 μs, 300 Hz)	1 A
Average forward input current (see Note 2)	25 mA
Peak output current	16 mA
Average output current	8 mA
Base current	5 mA
Input power dissipation at (or below) 70°C free-air temperature (see Note 3)	45 mW
Output power dissipation at (or below) 70°C free-air temperature (see Note 4)	100 mW
Operating free-air temperature range	−55°C to 100°C
Storage temperature range	−55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Derate linearly above 70°C free-air temperature at the rate of 1.67 mA/°C.
2. Derate linearly above 70°C free-air temperature at the rate of 0.83 mA/°C.
3. Derate linearly above 70°C free-air temperature at the rate of 1.50 mW/°C.
4. Derate linearly above 70°C free-air temperature at the rate of 3.33 mW/°C.

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electrical characteristics over operating free-air temperature range of 0 °C to 70 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_F	Input forward voltage	I_F = 16 mA,	T_A = 25°C		1.6	1.7	V
α_{VF}	Temperature coefficient of forward voltage	I_F = 16 mA			−1.8		mV/°C
V_{BR}	Input breakdown voltage	I_R = 10 μA,	T_A = 25°C	5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 2.4 mA,	I_F = 16 mA, I_B = 0		0.1	0.4	V
I_{OH}	High-level output current	I_F = 0, I_B = 0, T_A = 25°C	V_{CC} = VO = 5.5 V		3	500	nA
			V_{CC} = V_O = 15 V		0.01	1	μA
I_{OH}	High-level output current	V_{CC} = 15 V, I_F = 0,	V_O = 15 V, I_B = 0			50	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 15 V, I_F = 0, T_A = 25°C	I_O = 0, I_B = 0,		0.02	1	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 15 V, I_F = 0,	I_O = 0, I_B = 0			2	μA
I_{CCL}	Supply current, low-level output	V_{CC} = 15 V, I_F = 16 mA,	I_O = 0, I_B = 0		40		μA
h_{FE}	Transistor forward current transfer ratio	V_O = 5 V,	I_O = 3 mA		100		
CTR	Current transfer ratio	V_{CC} = 4.5 V, I_F = 16 mA, T_A = 25°C,	V_O = 0.4 V, I_B = 0, See Note 5	15%		22%	
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 6	T_A = 25°C,		10^{12}		Ω
I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, See Note 6	t = 5 s, RH = 45%,			1	μA
C_i	Input capacitance	V_F = 0,	f = 1 MHz		60		pF
C_{io}	Input-output capacitance	f = 1 MHz,	See Note 6		0.6		pF

† All typical values are at T_A = 25°C.

NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.

operating characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Bandwidth (−3 dB)	R_L = 100 Ω, See Note 7		2		MHz

NOTE 7: Bandwidth is the range of frequencies within which the ac output voltage is not more than 3 dB below the low-frequency value.

switching characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C (unless otherwise noted)

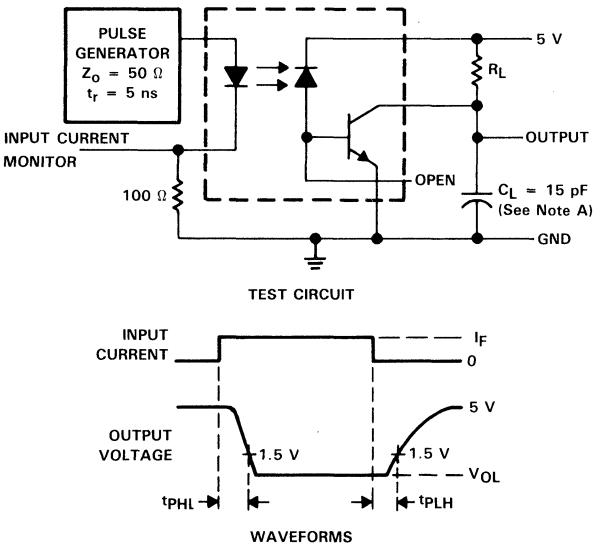
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 1.9 kΩ, See Note 8, See Figure 1		0.6	0.8	μs
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 1.9 kΩ, See Note 8, See Figure 1		0.6	0.8	μs
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, I_F = 0, R_L = 1.9 kΩ, See Notes 8 and 9, See Figure 2	−1000			V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = −10 V, I_F = 16 mA, R_L = 1.9 kΩ, See Figure 2, See Notes 8 and 9	−1000			V/μs

NOTES: 8. The 1.9-kΩ load represents one TTL unit load of 1.6 mA and a 5.6-kΩ pullup resistor.
9. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

3

Optocouplers (Isolators)

PARAMETER MEASUREMENT INFORMATION

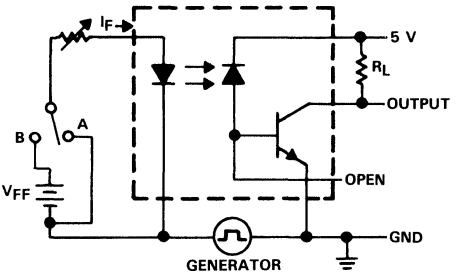


NOTE A: C_L includes probe and stray capacitance.

FIGURE 1. SWITCHING TEST CIRCUIT AND WAVEFORMS

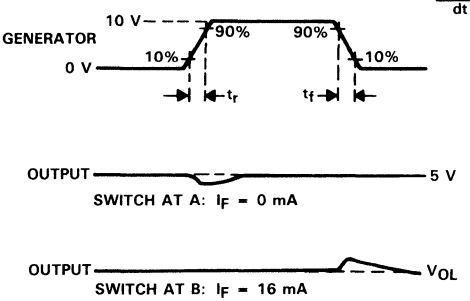
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

$$\frac{dV_{CM}}{dt} = \frac{8\ V}{t_r \text{ or } t_f}$$



VOLTAGE WAVEFORMS

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

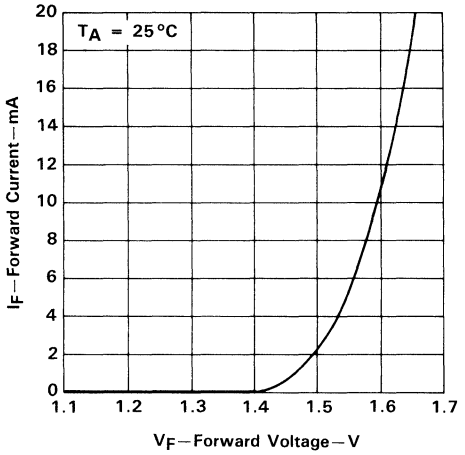


FIGURE 3

CURRENT TRANSFER CHARACTERISTICS

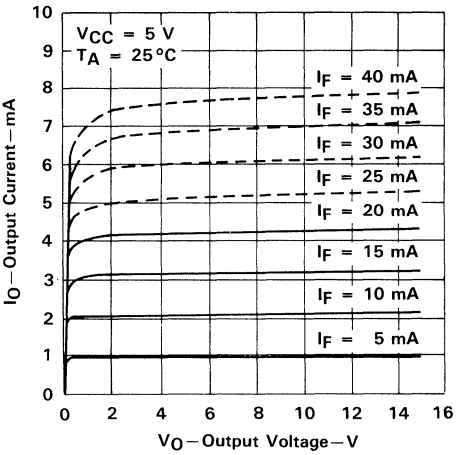


FIGURE 4

NORMALIZED CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

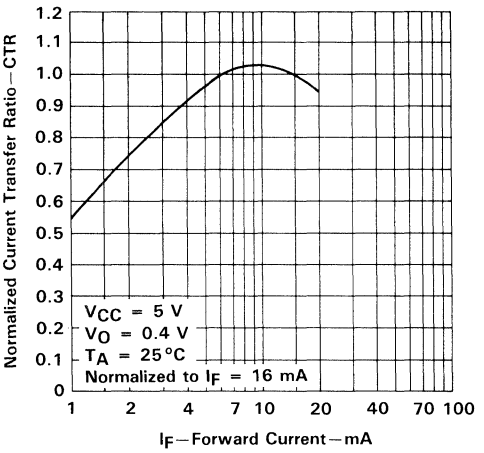


FIGURE 5

NORMALIZED CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

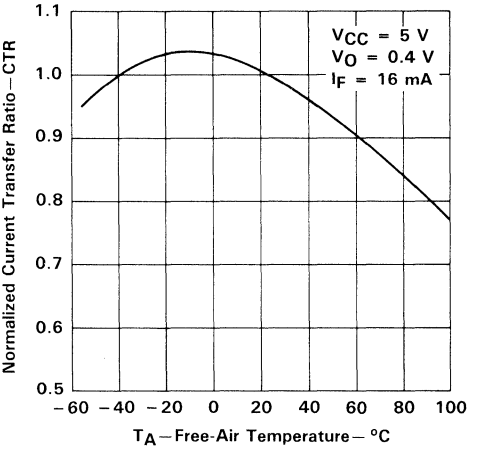


FIGURE 6

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

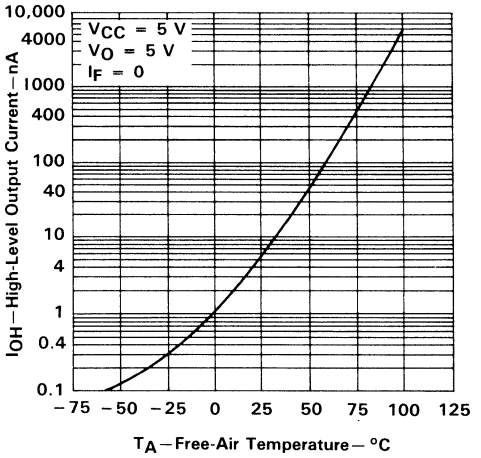


FIGURE 7

DIFFERENTIAL CURRENT TRANSFER RATIO
vs
INPUT DIODE QUIESCENT FORWARD CURRENT

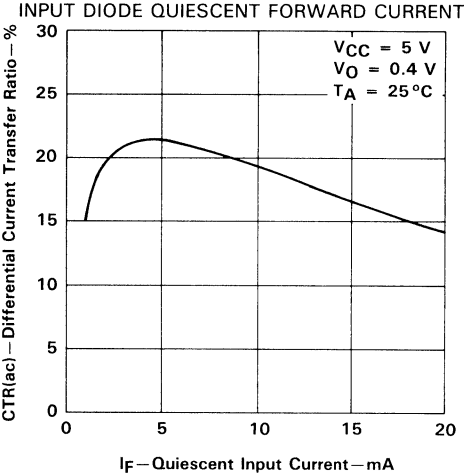


FIGURE 8

NORMALIZED FREQUENCY RESPONSE
vs
LOAD RESISTANCE

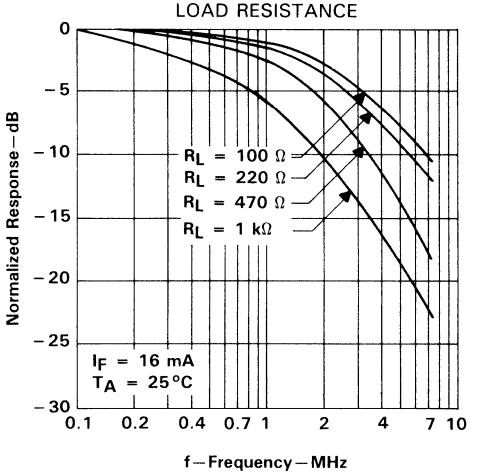


FIGURE 9

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

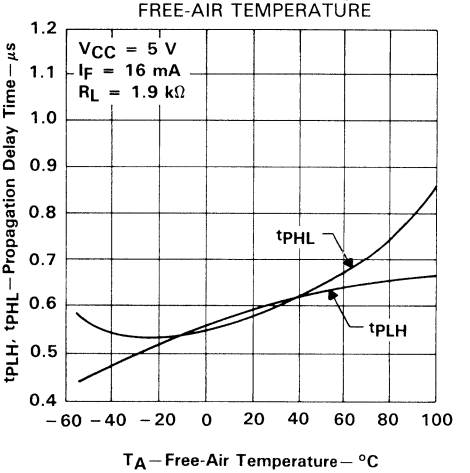


FIGURE 10

D3115, APRIL 1988

- Compatible with TTL Inputs
- High-Speed Switching . . . 1 Mbit/s Typ
- Bandwidth . . . 2 MHz Typ
- High Common-Mode Transient Immunity . . . 1000 V/μs Typ
- High-Voltage Electrical Insulation . . . 3000 V DC Min
- Open-Collector Output
- UL Recognized . . . File Number 65085

description

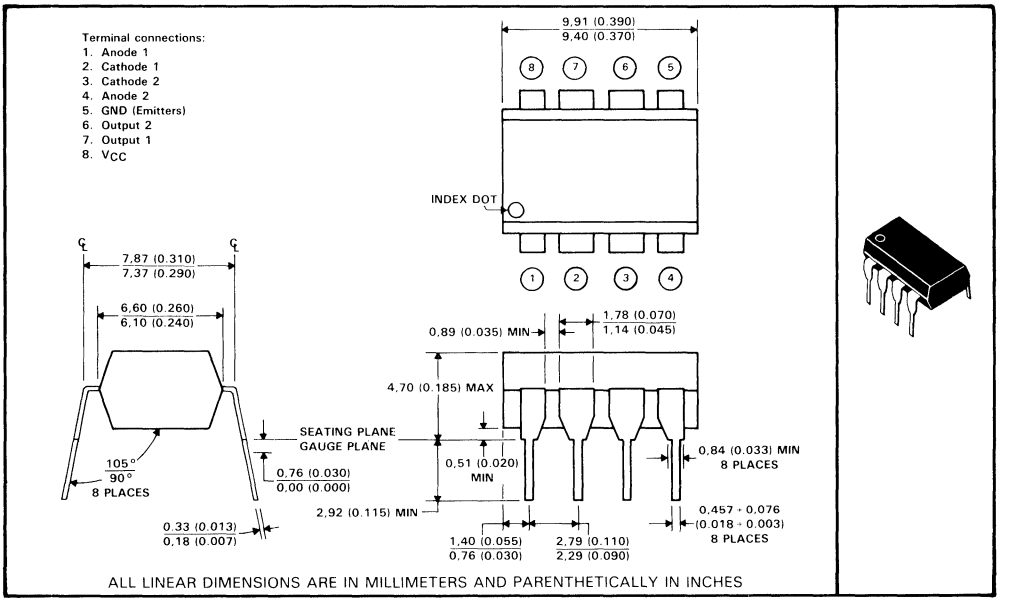
These high-speed optocouplers are designed for use in analog or digital interface applications that require high-voltage isolation between the input and output. Applications include line receivers that require high common-mode transient immunity, and analog or logic circuits that require input-to-output electrical isolation.

Each HCPL2530 and HCPL3531 optocoupler consists of two light-emitting diodes and two integrated photon detectors. Each detector is composed of a photodiode and an open-collector output transistor. Separate connections are provided for the photodiode bias and the transistor collector output. This feature, which reduces the transistor base-to-collector capacitance, results in speeds up to one hundred times that of a conventional phototransistor optocoupler.

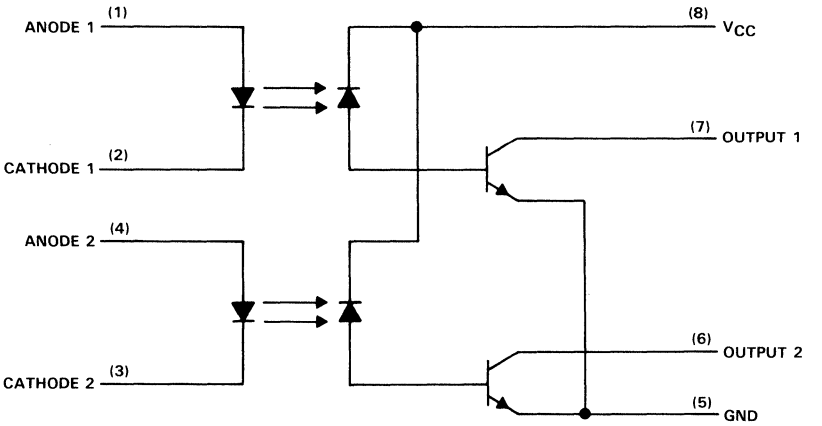
The HCPL2530 is designed for TTL/CMOS, TTL/LSTTL, and wide-band analog applications.

The HCPL2531 is designed for high-speed TTL/TTL applications.

mechanical data



schematic



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply and output voltage range, V_{CC} and V_O . . . . . −0.5 V to 15 V
Reverse input voltage (each channel) . . . . . 5 V
Peak input forward current (each channel) (pulse duration = 1 ms, 50% duty cycle, see Note 1) 50 mA
Peak transient input forward current (each channel) (pulse duration = 1 μs, f = 300 Hz) . . . . . 1 A
Average forward input current (each channel) (see Note 2) . . . . . 25 mA
Peak output current (each channel) . . . . . 16 mA
Average output current (each channel) . . . . . 8 mA
Input power dissipation at (or below) 70°C free-air temperature
(each channel) (see Note 3) . . . . . 45 mW
Output power dissipation at (or below) 70°C free-air temperature
(each channel) (see Note 4) . . . . . 35 mW
Storage temperature range . . . . . −55°C to 125°C
Operating free-air temperature range . . . . . −55°C to 100°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Derate linearly above 70°C free-air temperature at the rate of 1.67 mA/°C.
2. Derate linearly above 70°C free-air temperature at the rate of 0.83 mA/°C.
3. Derate linearly above 70°C free-air temperature at the rate of 1.50 mW/°C.
4. Derate linearly above 70°C free-air temperature at the rate of 1.17 mW/°C.

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electrical characteristics over operating free-air temperature range of 0 °C to 70 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		HCPL2530			HCPL2531			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_F	Input forward voltage	I_F = 16 mA,	T_A = 25°C		1.6	1.7		1.6	1.7	V
VF	Temperature coefficient of forward voltage	I_F = 16 mA			−1.8			−1.8		mV/°C
V_{BR}	Input breakdown voltage	I_R = 10 μA,	T_A = 25°C	5			5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 1.1 mA		0.1	0.5				V
		I_F = 16 mA	I_{OL} = 2.4 mA					0.1	0.5	
I_{OH}	High-level output current	I_{F1} = I_{F2} = 0, T_A = 25°C	V_{CC} = V_{O1} = V_{O2} = 5.5 V		3	500		3	500	nA
		V_{CC} = V_{O1} = V_{O2} = 15 V, I_{F1} = I_{F2} = 0				50			50	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 15 V, I_{F1} = I_{F2} = 0	I_{O1} = I_{O2} = 0,			4			4	μA
I_{CCL}	Supply current, low-level output	V_{CC} = 15 V, I_{F1} = I_{F2} = 16 mA	I_{O1} = I_{O2} = 0,		80			80		μA
CTR	Current transfer ratio	V_{CC} = 4.5 V, I_F = 16 mA, See Note 5	V_O = 0.5 V, T_A = 25°C,	7%	18%		19%	24%		
CTR	Current transfer ratio	V_{CC} = 4.5 V, I_F = 16 mA,	V_O = 0.5 V, See Note 5	5%			15%			
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 6	T_A = 25°C,		10^{12}			10^{12}		Ω
I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, See Note 6	t = 5 s, RH = 45%,			1			1	μA
C_i	Input capacitance	V_F = 0,	f = 1 MHz		60			60		pF
C_{io}	Input-output capacitance	f = 1 MHz,	See Note 6		0.6			0.6		pF
r_{ii}	Input-input resistance	V_{ii} = 500 V, See Note 7	T_A = 25°C		10^{11}			10^{11}		Ω
I_{ii}	Input-input insulation leakage current	V_{ii} = 500 V, T_A = 25°C, See Note 7	t = 5 5, R_h = 45%,		0.005			0.005		μA
c_{ii}	Input-input capacitance	f = 1 MHz, See Note 7	T_A = 25°C,		0.25			0.25		pF

†All typical values are at T_A = 25°C.

NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.
7. These parameters are measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.

operating characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C

PARAMETER		TEST CONDITIONS	HCPL2530			HCPL2531			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Bandwidth (−3 dB)	R_L = 100 Ω, See Note 8		2			2		MHz

NOTE 7: Bandwidth is the range of frequencies within which the ac output voltage is not more than 3 dB below the low-frequency value.

switching characteristics at V_{CC} = 5 V, I_F = 16 mA, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	HCPL2530			HCPL2531			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 4.1 kΩ, See Note 9, See Figure 1		1.0	1.5				μs
		R_L = 1.9 kΩ, See Note 10, See Figure 1					0.6	0.8	
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 4.1 kΩ, See Note 9, See Figure 1		0.7	1.5				μs
		R_L = 1.9 kΩ, See Note 10, See Figure 1					0.6	0.8	
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, I_F = 0, R_L = 4.1 kΩ, See Notes 9 and 10, See Figure 2		1000					V/μs
		ΔV_{CM} = 10 V, I_F = 0, R_L = 1.9 kΩ, See Notes 10 and 11, See Figure 2					1000		
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = 10 V, R_L = 4.1 kΩ, See Figure 2, See Notes 9 and 11,		−1000					V/μs
		ΔV_{CM} = 10 V, R_L = 1.9 kΩ, See Figure 2, See Notes 10 and 11					−1000		

NOTES: 9. The 4.1-kΩ load represents one LSTTL unit load of 0.36 mA and a 6.1-kΩ pullup resistor.
10. The 1.9-kΩ load represents one TTL unit load of 1.6 mA and a 5.6-kΩ pullup resistor.
11. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

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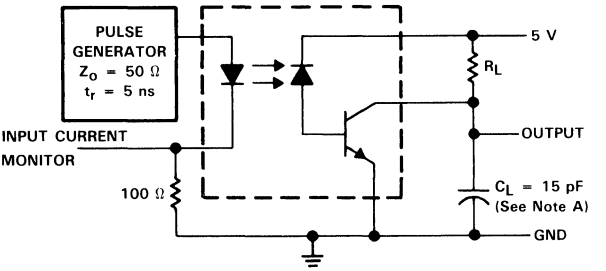
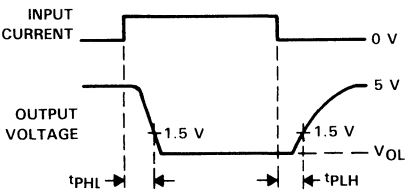
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT (EACH CHANNEL)

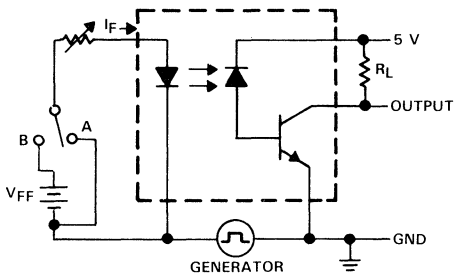


WAVEFORMS

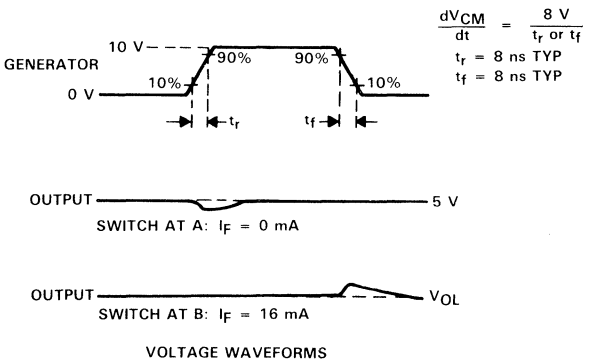
NOTE A: C_L includes probe and stray capacitance.

FIGURE 1. SWITCHING TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT (EACH CHANNEL)



VOLTAGE WAVEFORMS

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

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INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

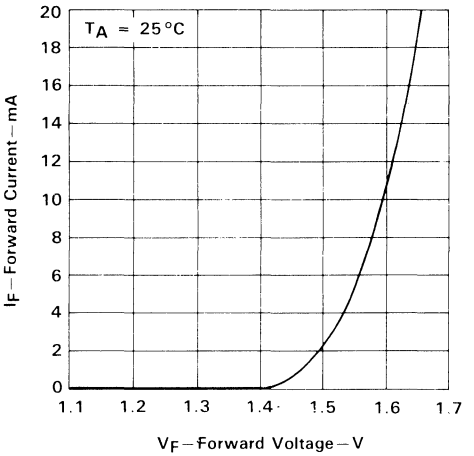

FIGURE 3

HCPL2530
CURRENT TRANSFER CHARACTERISTICS

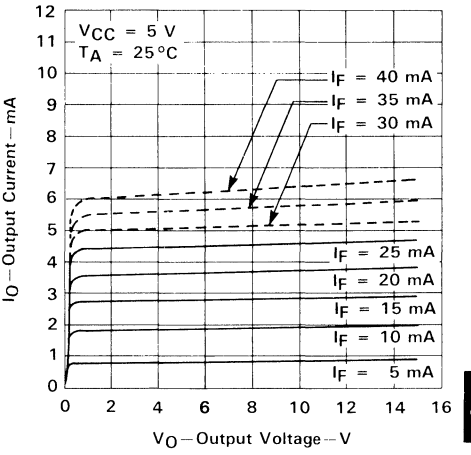

FIGURE 4

NORMALIZED CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

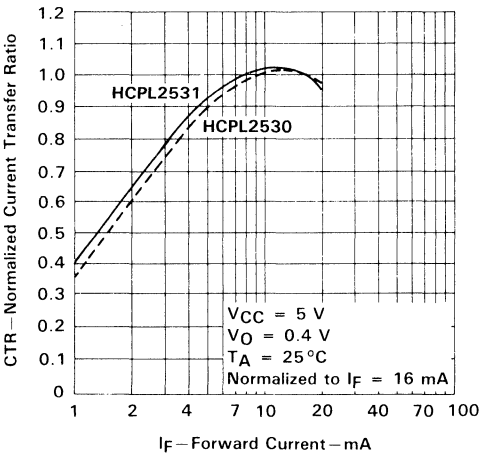

FIGURE 5

NORMALIZED CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

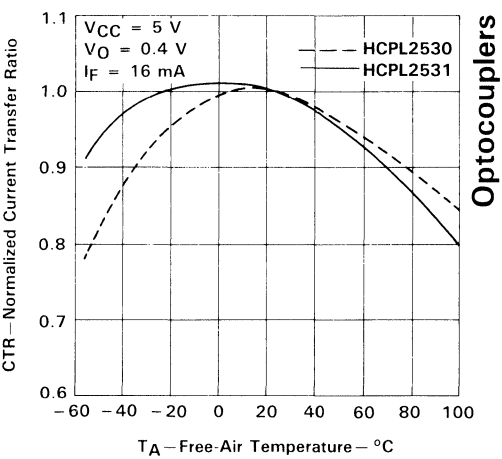

FIGURE 6

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

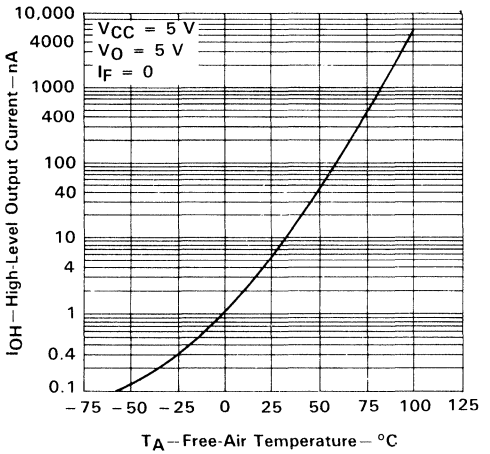

FIGURE 7

DIFFERENTIAL CURRENT TRANSFER RATIO
vs
INPUT DIODE QUIESCENT FORWARD CURRENT

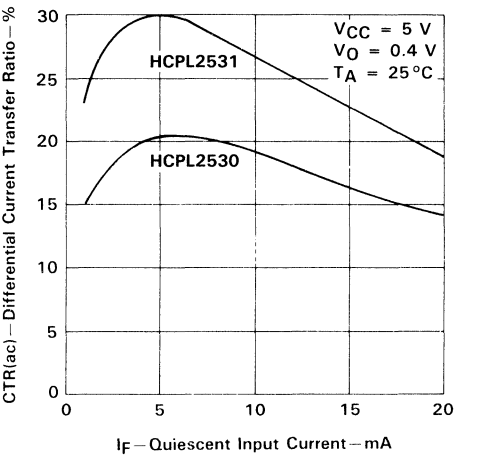

FIGURE 8

NORMALIZED FREQUENCY RESPONSE
vs
LOAD RESISTANCE

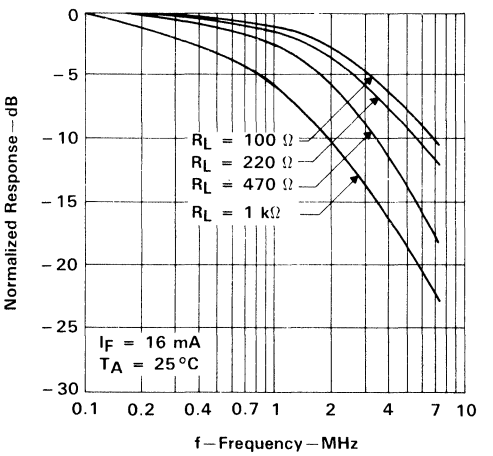

FIGURE 9

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

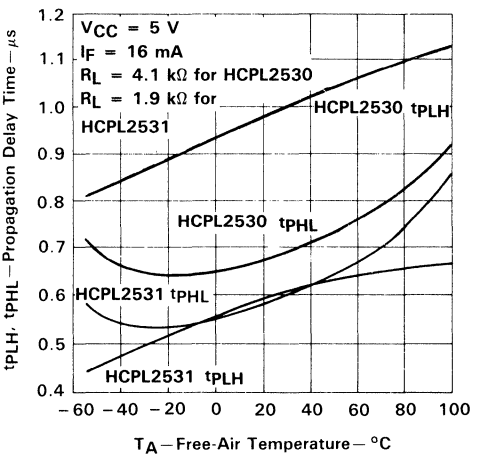

FIGURE 10

TEXAS INSTRUMENTS
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D2968, NOVEMBER 1986

- **Gallium Arsenide Phosphide LED Optically Coupled to an Integrated Circuit Detector**
- **Internal Shield for Common-Mode Rejection**
- **Compatible with TTL and LSTTL Inputs**
- **Low Input Current Required to Turn Output On . . . 5 mA Max**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High-Speed Switching . . . 75 ns Max**
- **UL Recognized . . . File Number E65085**
- **Directly Interchangeable with Hewlett Packard HCPL2601**

description

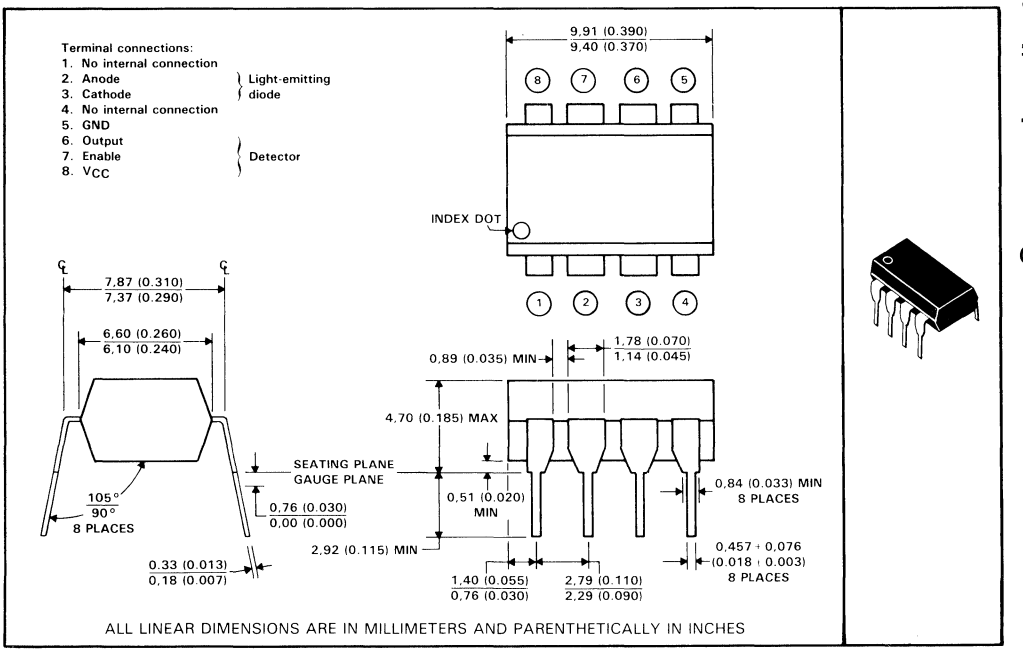
The HCPL2601 optocoupler is designed for use in high-speed digital interfacing applications that require high-voltage isolation between the input and output. It is recommended for use in extremely high ground-noise and induced-noise environments. Applications include line receivers, microprocessors or computer interface, digital programming of floating power supplies, motors, and other control systems.

The HCPL2601 high-speed optocoupler consists of a GaAsP light-emitting diode and an integrated light detector composed of a photodiode, a high-gain amplifier, and a Schottky-clamped open-collector output transistor. An input diode forward current of 5 milliamperes will switch the output transistor low, providing an on-state drive current of 13 milliamperes (eight 1.6-milliampere TTL loads). A TTL-compatible enable input is provided for applications that require output-transistor gating.

The HCPL2601 is mounted in a standard 8-pin dual-in-line plastic package.

The HCPL2601 is characterized for operation over the temperature range of 0°C to 70°C. The internal shield provides a guaranteed common-mode transient immunity of 1000 volts/microsecond minimum.

mechanical data

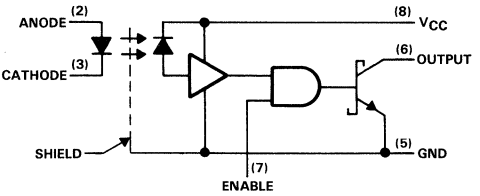


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FUNCTION TABLE

INPUT	ENABLE	OUTPUT
$I_{F(on)}$	H	L
$I_{F(off)}$	X	H
X	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Reverse input voltage . . . . . 5 V
Enable input voltage (not to exceed V_{CC} by more than 500 mV) . . . . . 5.5 V
Output voltage . . . . . 7 V
Peak forward input current (≤ 1 ms duration) . . . . . 40 mA
Average forward input current . . . . . 20 mA
Output current . . . . . 25 mA
Output power dissipation . . . . . 40 mW
Storage temperature range . . . . . −55°C to 125°C
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Output supply voltage (see Note 1)	4.5	5	5.5	V
$V_{IH(EN)}$	High-level enable input voltage (see Note 2)	2		V_{CC}	V
$V_{IL(EN)}$	Low-level enable input voltage	0		0.8	V
$I_{F(on)}$	Input forward current to turn output on	6.3		15	mA
$I_{F(off)}$	Input forward current to turn output off	0		250	μA
I_{OL}	Low-level (on-state) output current			13	mA
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. All voltage values are with respect to GND (pin 5).
2. No external pullup is required at the enable input; an open circuit will establish the high level.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_F	Input forward voltage	I_F = 10 mA,	T_A = 25°C		1.6	1.75	V
αV_F	Temperature coefficient of forward voltage	I_F = 10 mA			−1.8		mV/°C
V_{BR}	Input reverse breakdown voltage	I_R = 10 μA,	T_A = 25°C	5			V
V_{OL}	Low-level output voltage	V_{CC} = 5.5 V, I_F = 5 mA,	$V_{(EN)}$ = 2 V, I_{OL} = 13 mA		0.23	0.6	V
I_{OH}	High-level output current	V_{CC} = 5.5 V, $V_{(EN)}$ = 2 V,	V_O = 5.5 V, I_F = 250 μA			250	μA
$I_{IH(EN)}$	High-level enable input current	V_{CC} = 5.5 V,	$V_{(EN)}$ = 2 V		−0.2		mA
$I_{IL(EN)}$	Low-level enable input current	V_{CC} = 5.5 V,	$V_{(EN)}$ = 0.5 V		−0.5	−2	mA
I_{CCH}	Supply current, high-level output	V_{CC} = 5.5 V, I_F = 0	$V_{(EN)}$ = 0.5 V,		10	15	mA
I_{CCL}	Supply current, low-level output	V_{CC} = 5.5 V, I_F = 10 mA	$V_{(EN)}$ = 0.5 V,		13	19	mA
I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, See Note 1	t = 5 s, RH = 45%,			1	μA
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 1	T_A = 25°C,		10^{12}		Ω
C_i	Input capacitance	V_F = 0,	f = 1 MHz		60		pF
C_{io}	Input-output capacitance	f = 1 MHz, See Note 1	T_A = 25°C,		0.6		pF

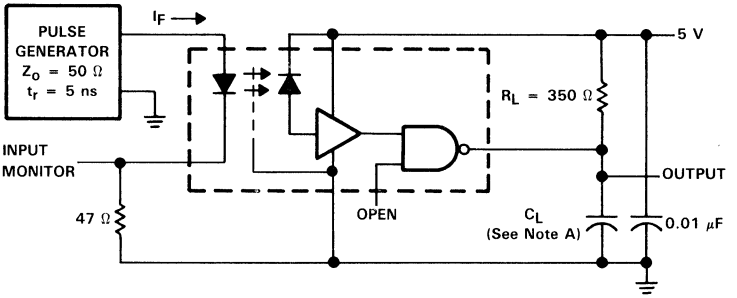
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7, and 8 shorted together.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

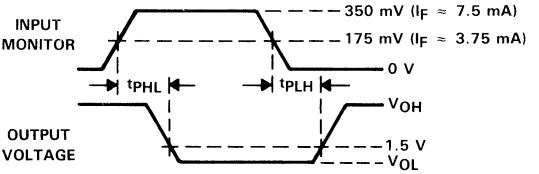
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output, from LED input	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 1		42	75	ns
t_{PHL}	Propagation delay time, high-to-low level output, from LED input	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 1		42	75	ns
$t_{PLH(EN)}$	Propagation delay time, low-to-high level output, from enable	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 2		40		ns
$t_{PHL(EN)}$	Propagation delay time, high-to-low level output, from enable	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 2		25		ns
t_r	Rise time	I_F = 7.5 mA, C_L = 15 pF	R_L = 350 Ω,		20		ns
t_f	Fall time	I_F = 7.5 mA, C_L = 15 pF	R_L = 350 Ω,		30		ns
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 50 V, R_L = 350 Ω,	I_F = 0, See Note 2 and Figure 3	1000	10000		V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = −50 V, R_L = 350 Ω,	I_F = 7.5 mA, See Note 2 and Figure 3	−1000	−1000		V/μs

NOTE 2: Common-mode input transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

PARAMETER MEASUREMENT INFORMATION

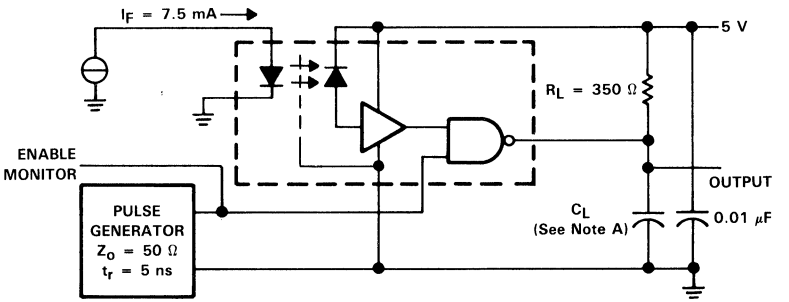


TEST CIRCUIT

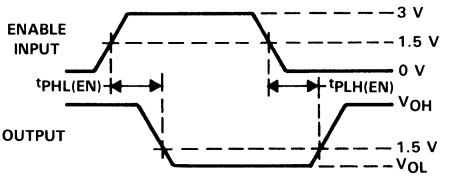


WAVEFORMS

FIGURE 1. t_{PLH} AND t_{PHL} FROM LED INPUT TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. $t_{PLH(EN)}$ AND $t_{PHL(EN)}$ FROM ENABLE TEST CIRCUIT AND WAVEFORMS

NOTE A: C_L is approximately 15 pF, which includes probe and stray wiring capacitances.

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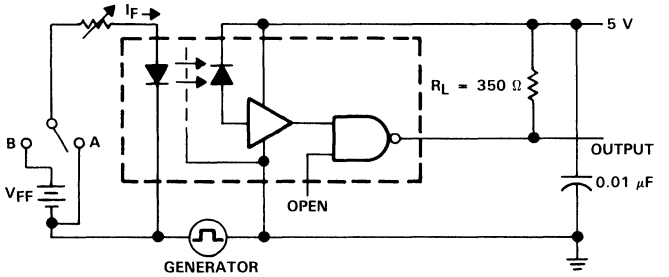
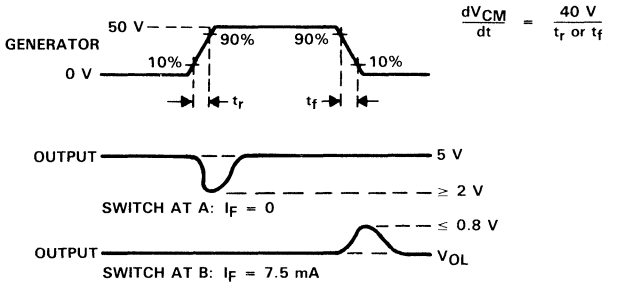
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION INFORMATION

A ceramic capacitor (0.01 μF to 0.1 μF) should be connected between pins 8 and 5 to stabilize the high-gain amplifier. The total lead length between the capacitor and the optocoupler should not exceed 20 mm (0.8 inches). Failure to provide a bypass capacitor may result in impaired switching characteristics.

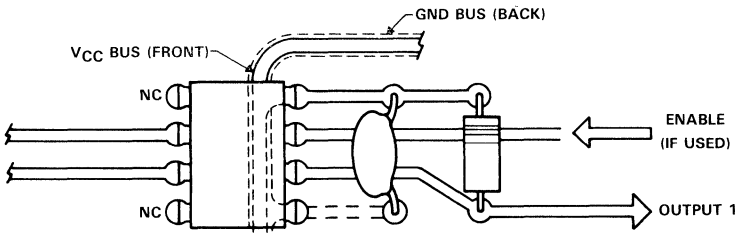


FIGURE 4. RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

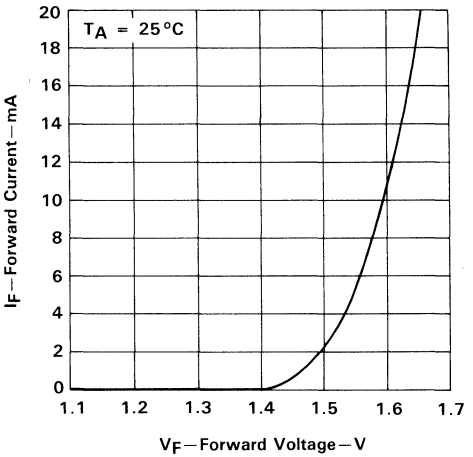


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE—AIR TEMPERATURE

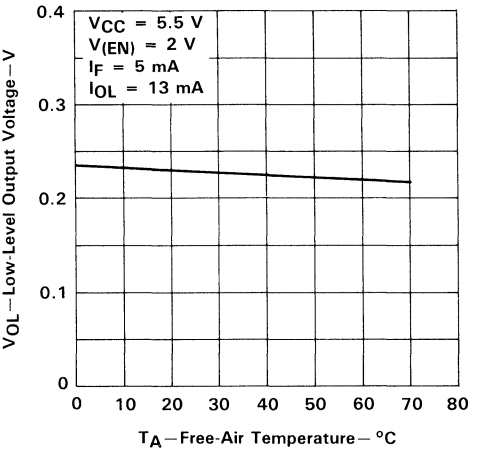


FIGURE 6

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

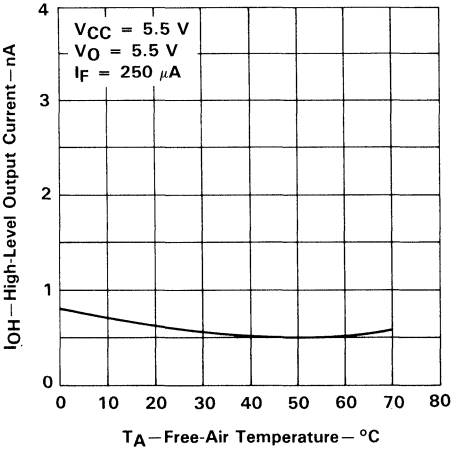


FIGURE 7

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME FROM LED INPUT
vs
PULSE FORWARD CURRENT

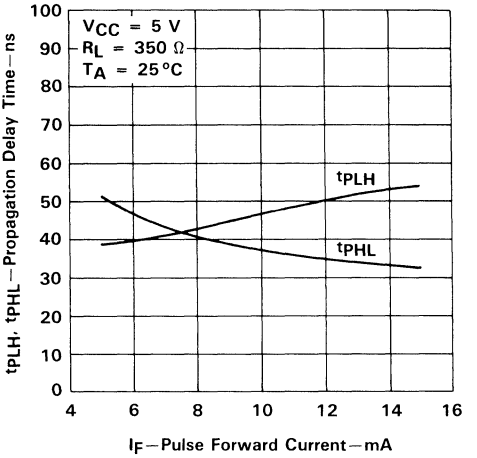


FIGURE 8

PROPAGATION DELAY TIME FROM LED INPUT
vs
LOAD RESISTANCE

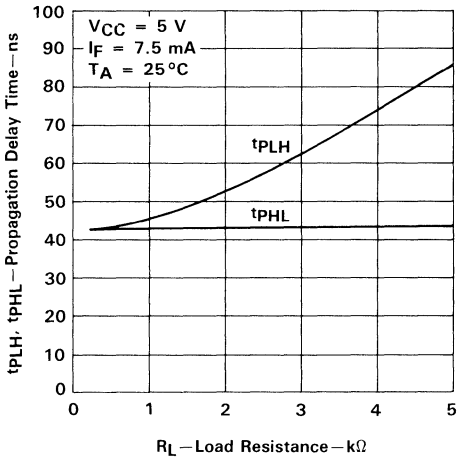


FIGURE 9

D2969, NOVEMBER 1986

- **Gallium Arsenide Phosphide LED Optically Coupled to an Integrated Circuit Detector**
- **Compatible with TTL and LSTTL Inputs**
- **Low Input Current Required for On-State Output . . .5 mA Max**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High-Speed Switching . . . 75 ns Max**
- **Directly Interchangeable with Hewlett Packard HCPL2630**
- **UL Recognized . . . File Number E65085**

description

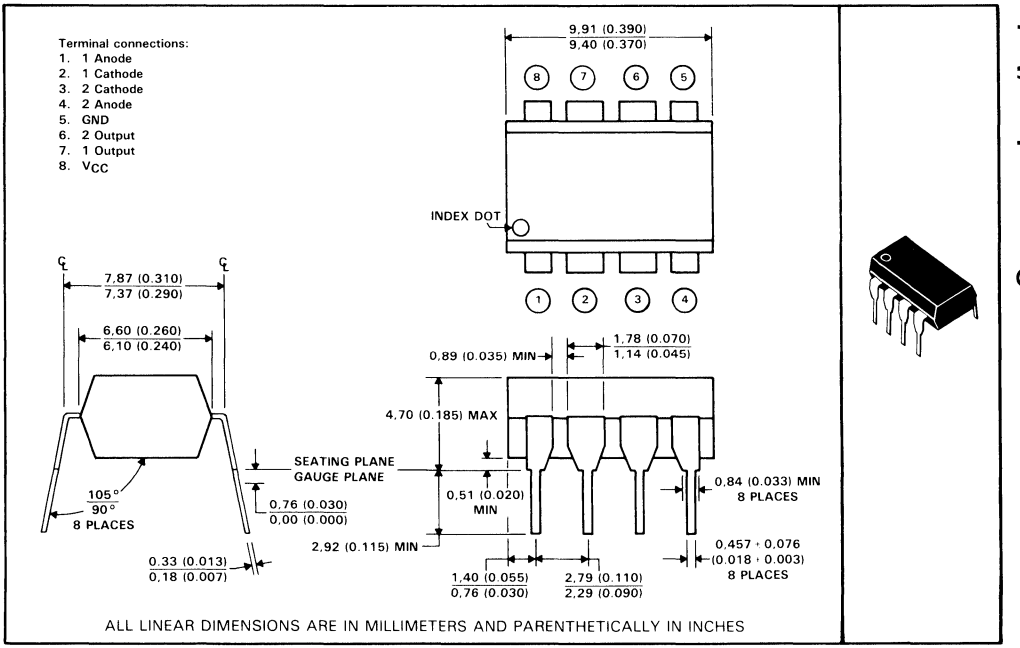
The HCPL2630 is a dual optocoupler designed for use in high-speed digital interfacing applications that require high-voltage isolation between the input and output. Applications include line receivers, microprocessors or computer interface, and other control systems.

Each channel of the HCPL2630 optocoupler consists of a GaAsP light-emitting diode and an integrated light detector composed of a photodiode, a high-gain amplifier, and a Schottky-clamped open-collector output transistor. An input diode forward current of 5 milliamperes will switch the output transistor low, providing an on-state drive current of 13 milliamperes (eight 1.6-milliampere TTL loads).

The device is mounted in a standard 8-pin dual-in-line plastic package.

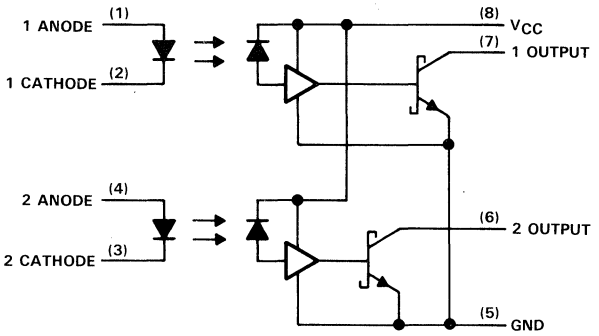
The HCPL2630 is characterized for operation over the temperature range of 0°C to 70°C.

mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Reverse input voltage	5 V
Output voltage	7 V
Peak forward input current, each channel (≤1 ms duration)	30 mA
Average forward input current, each channel	15 mA
Output current, each channel	16 mA
Output power dissipation	85 mW
Storage temperature range	−55°C to 125°C
Operating free-air temperature range	0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Output supply voltage (see Note 1)	4.5	5	5.5	V
$I_{F(on)}$	Input forward current to turn output on	6.3		15	mA
$I_{F(off)}$	Input forward current to turn output off	0		250	μA
I_{OL}	Low-level (on-state) output current			13	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 1: All voltage values are with respect to GND (pin 5).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_F	Input forward voltage	I_F = 10 mA,	T_A = 25°C		1.6	1.75	V
αV_F	Temperature coefficient of forward voltage	I_F = 10 mA			−1.8		mV/°C
V_{BR}	Input reverse breakdown voltage	I_R = 10 μA,	T_A = 25°C	5			V
V_{OL}	Low-level output voltage	V_{CC} = 5.5 V, I_{OL} = 13 mA	I_F = 5 mA,		0.23	0.6	V
I_{OH}	High-level output current	V_{CC} = 5.5 V, I_F = 250 μA	V_O = 5.5 V,			250	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 5.5 V,	I_F = 0		20	30	mA
I_{CCL}	Supply current, low-level output	V_{CC} = 5.5 V,	I_F = 10 mA		26	36	mA
I_{II}	Input-input insulation leakage current	V_{II} = 500 V, T_A = 25°C See Note 2	t = 5 s, RH = 45%,		0.005		μA
I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, T_A = 25°C, See Note 1	t = 5 s, RH = 45%,			1	μA
r_{II}	Input-input resistance	V_{II} = 500 V, See Note 2	T_A = 25°C,		10^{11}		Ω
r_{IO}	Input-output resistance	V_{IO} = 500 V, See Note 1	T_A = 25°C,		10^{12}		Ω
C_i	Input capacitance	V_F = 0,	f = 1 MHz		60		pF
C_{ii}	Input-input capacitance	V_F = 0,	f = 1 MHz		0.25		pF
C_{io}	Input-output capacitance	f = 1 MHz, See Note 1	T_A = 25°C,		0.6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

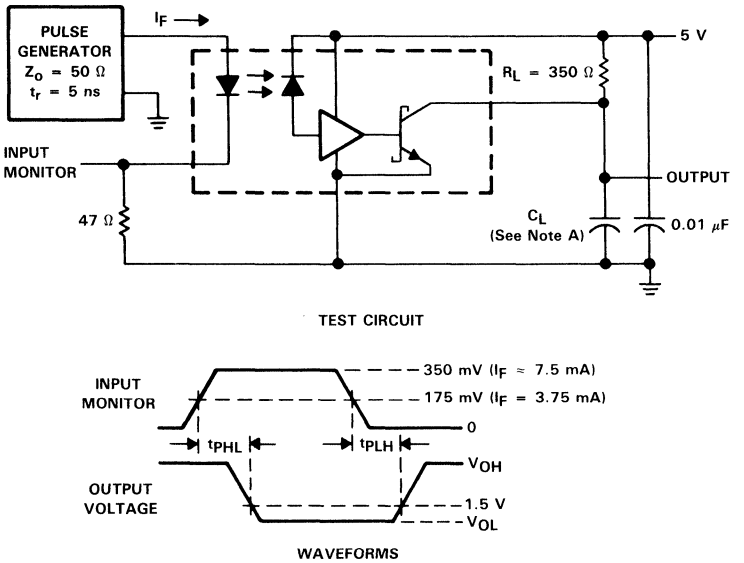
NOTES: 1. These parameters are measured between pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
2. These parameters are measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from LED input	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 1		42	75	ns
t_{PHL}	Propagation delay time, high-to-low level output, from LED input	I_F = 7.5 mA, C_L = 15 pF,	R_L = 350 Ω, See Figure 1		42	75	ns
t_r	Rise time	I_F = 7.5 mA, C_L = 15 pF	R_L = 350 Ω,		20		ns
t_f	Fall time	I_F = 7.5 mA, C_L = 15 pF	R_L = 350 Ω,		30		ns
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 10 V, R_L = 350 Ω, See Note 3 and Figure 2	I_F = 0,		50		V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = −10 V, R_L = 350 Ω, See Note 3 and Figure 2	I_F = 5 mA,		−150		V/μs

NOTE 3: Common-mode input transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

PARAMETER MEASUREMENT INFORMATION
(EACH CHANNEL)



NOTE A: C_L is approximately 15 pF, which includes probe and stray wiring capacitances.

FIGURE 1. t_{PLH} AND t_{PHL} FROM LED INPUT TEST CIRCUIT AND WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION (EACH CHANNEL)

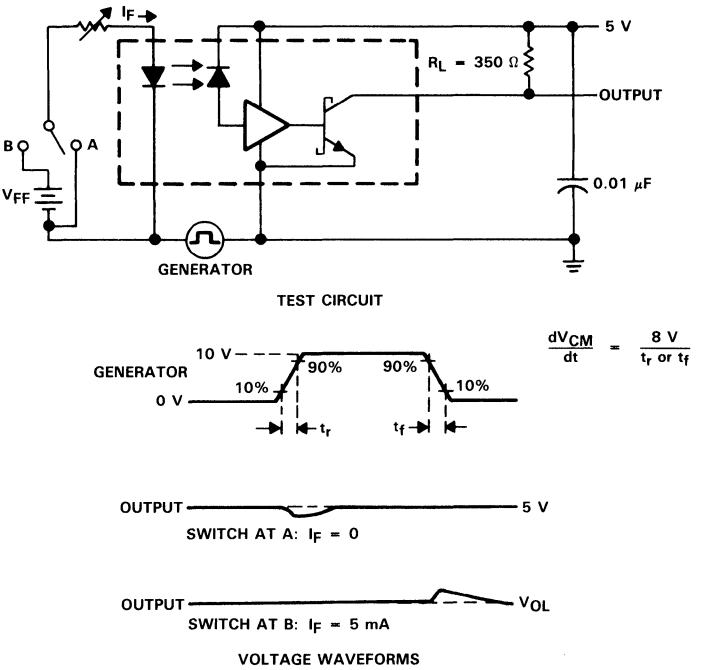


FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION INFORMATION

A ceramic capacitor (0.01 μF to 0.1 μF) should be connected between pins 8 and 5 to stabilize the high-gain amplifier. The total lead length between the capacitor and the optocoupler should not exceed 20 mm (0.8 inches). Failure to provide a bypass capacitor may result in impaired switching characteristics.

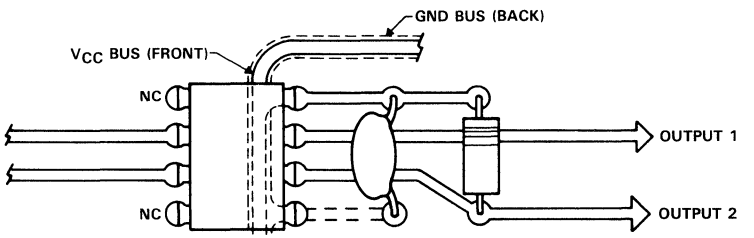


FIGURE 3. RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

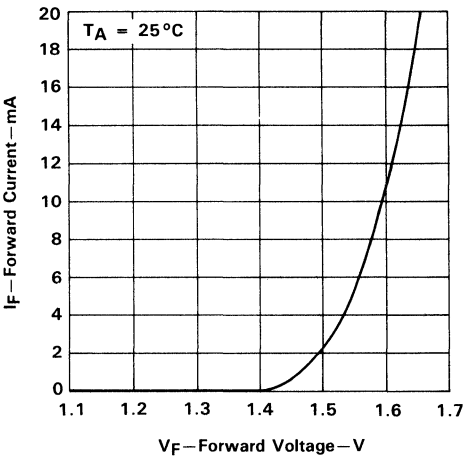


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

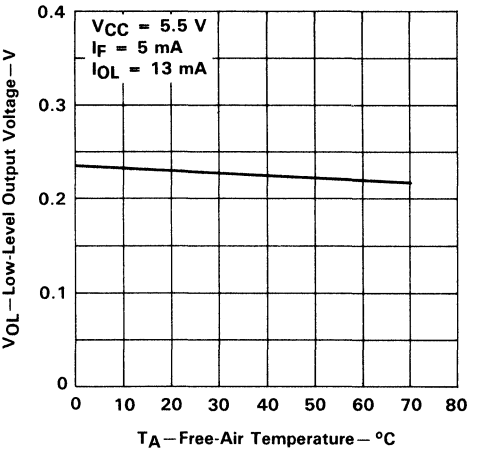


FIGURE 5

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

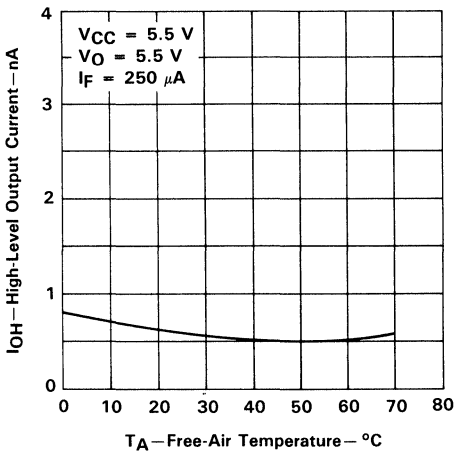


FIGURE 6

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME FROM LED INPUT
vs
PULSE FORWARD CURRENT

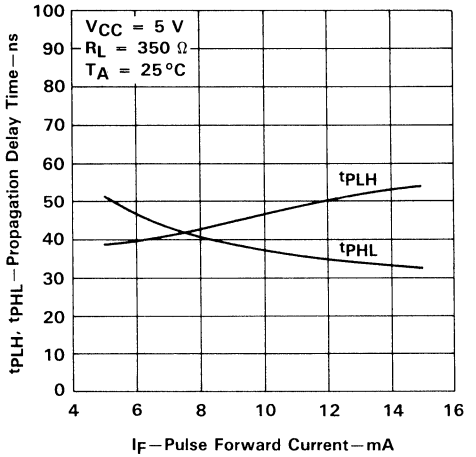


FIGURE 7

PROPAGATION DELAY TIME FROM LED INPUT
vs
LOAD RESISTANCE

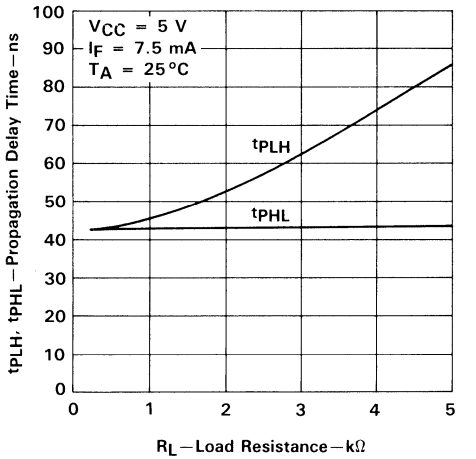


FIGURE 8

Optocouplers (Isolators)

D3114, APRIL 1988

- **Gallium Arsenide Phosphide LED Optically Coupled to an Integrated Circuit Detector**
- **Compatible with TTL and LSTTL Inputs**
- **Low Input Current Required for On-State Output . . .5 mA Max**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High-Speed Switching . . . 75 ns Max**
- **Directly Interchangeable with Hewlett Packard HCPL2631**
- **UL Recognized . . . File Number E65085**
- **Internal Shield for High Common-Mode Rejection**

description

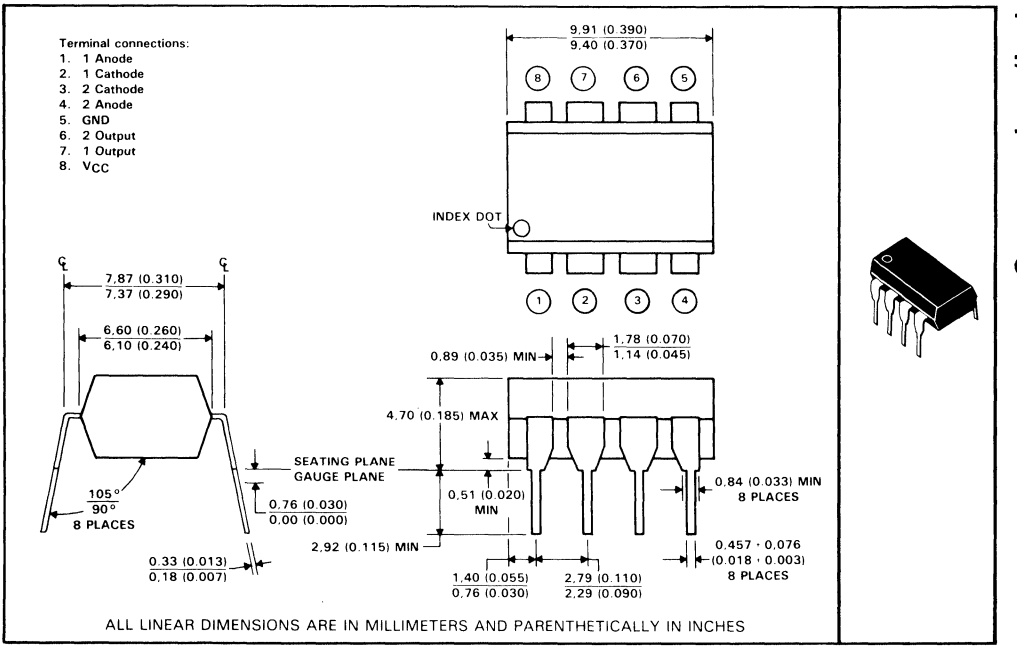
The HCPL2631 is a dual optocoupler designed for use in high-speed digital interfacing applications that require high-voltage isolation between the input and output. Applications include line receivers, microprocessors or computer interface, and other control systems.

Each channel of the HCPL2631 optocoupler consists of a GaAsP light-emitting diode and an integrated light detector composed of a photodiode, a high-gain amplifier, and a Schottky-clamped open-collector output transistor. An input diode forward current of 5 mA will switch the output transistor low, providing an on-state drive current of 13 mA (eight 1.6-mA TTL loads).

The device is mounted in a standard 8-pin dual-in-line plastic package. The internal shield provides a guaranteed common-mode transient immunity of 1000 v/μs minimum.

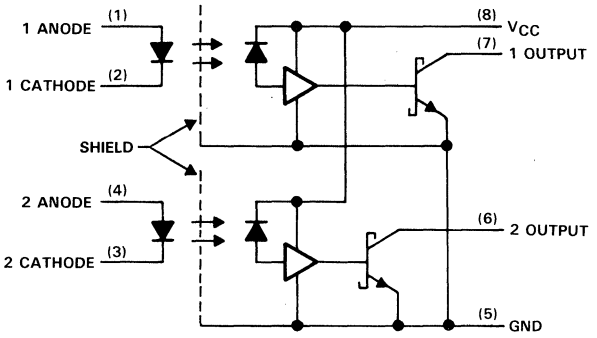
The HCPL2631 is characterized for operation over the temperature range of 0°C to 70°C.

mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Reverse input voltage . . . . . 5 V
Output voltage . . . . . 7 V
Peak forward input current, each channel (≤1 ms duration) . . . . . 30 mA
Average forward input current, each channel . . . . . 15 mA
Output current, each channel . . . . . 16 mA
Output power dissipation . . . . . 85 mW
Storage temperature range . . . . . −55°C to 125°C
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Output supply voltage (see Note 1)	4.5	5	5.5	V
$I_{F(on)}$	Input forward current to turn output on	6.3		15	mA
$I_{F(off)}$	Input forward current to turn output off	0		250	μA
I_{OL}	Low-level (on-state) output current			13	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 1: All voltage values are with respect to GND (pin 5).

TEXAS INSTRUMENTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_F	Input forward voltage	I_F = 10 mA, T_A = 25°C		1.6	1.75	V
αV_F	Temperature coefficient of forward voltage	I_F = 10 mA		−1.8		mV/°C
V_{BR}	Input reverse breakdown voltage	I_R = 10 μA, T_A = 25°C	5			V
V_{OL}	Low-level output voltage	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} = 13 mA		0.23	0.6	V
I_{OH}	High-level output current	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 μA			250	μA
I_{CCH}	Supply current, high-level output	V_{CC} = 5.5 V, I_F = 0		20	30	mA
I_{CCL}	Supply current, low-level output	V_{CC} = 5.5 V, I_F = 10 mA		26	38	mA
I_{II}	Input-input insulation leakage current	V_{II} = 500 V, t = 5 s, T_A = 25°C RH = 45%, See Note 2		0.005		μA
I_{IO}	Input-output insulation leakage current	V_{IO} = 3000 V, t = 5 s, T_A = 25°C, RH = 45%, See Note 1			1	μA
r_{II}	Input-input resistance	V_{II} = 500 V, T_A = 25°C, See Note 2		10^{11}		Ω
r_{IO}	Input-output resistance	V_{IO} = 500 V, T_A = 25°C, See Note 1		10^{12}		Ω
C_i	Input capacitance	V_F = 0, f = 1 MHz		60		pF
C_{ii}	Input-input capacitance	V_F = 0, f = 1 MHz		0.25		pF
C_{io}	Input-output capacitance	f = 1 MHz, T_A = 25°C, See Note 1		0.6		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

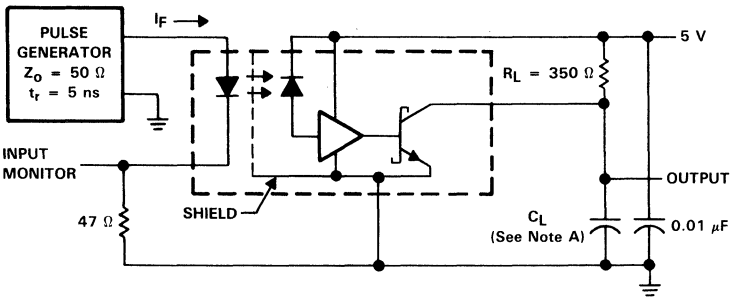
NOTES: 1. These parameters are measured between pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
2. These parameters are measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

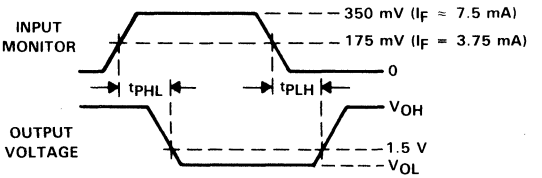
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from LED input	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 1		42	75	ns
t_{PHL}	Propagation delay time, high-to-low level output, from LED input	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF, See Figure 1		42	75	ns
t_r	Rise time	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF		20		ns
t_f	Fall time	I_F = 7.5 mA, R_L = 350 Ω, C_L = 15 pF		30		ns
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	ΔV_{CM} = 50 V, I_F = 0, R_L = 350 Ω, See Note 3 and Figure 2	1000	10 000		V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	ΔV_{CM} = −50 V, I_F = 5 mA, R_L = 350 Ω, See Note 3 and Figure 2	−1000	−10 000		V/μs

NOTE 3: Common-mode input transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

PARAMETER MEASUREMENT INFORMATION
(EACH CHANNEL)



TEST CIRCUIT



WAVEFORMS

NOTE A: C_L is approximately 15 pF, which includes probe and stray wiring capacitances.

FIGURE 1. t_{PLH} AND t_{PHL} FROM LED INPUT TEST CIRCUIT AND WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION (EACH CHANNEL)

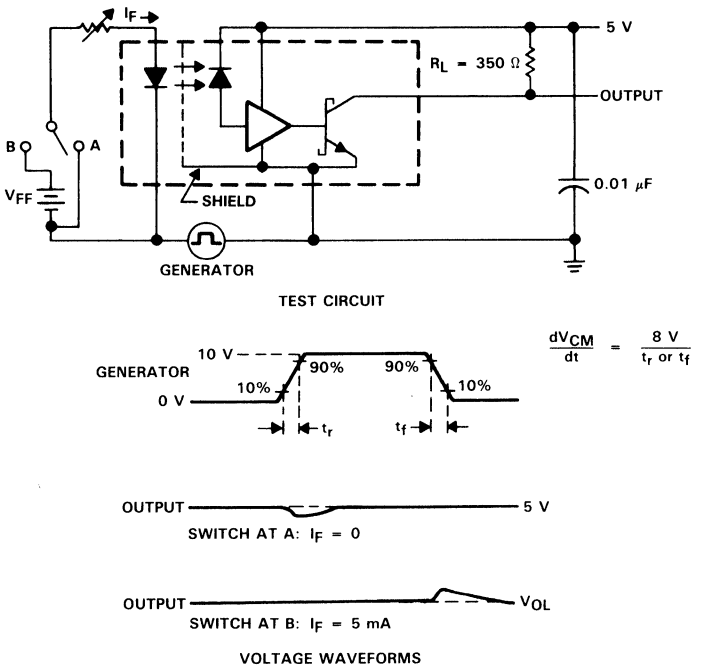

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION INFORMATION

A ceramic capacitor (0.01 μF to 0.1 μF) should be connected between pins 8 and 5 to stabilize the high-gain amplifier. The total lead length between the capacitor and the optocoupler should not exceed 20 mm (0.8 inches). Failure to provide a bypass capacitor may result in impaired switching characteristics.

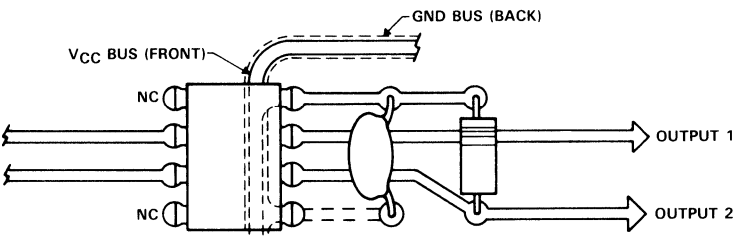

FIGURE 3. RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

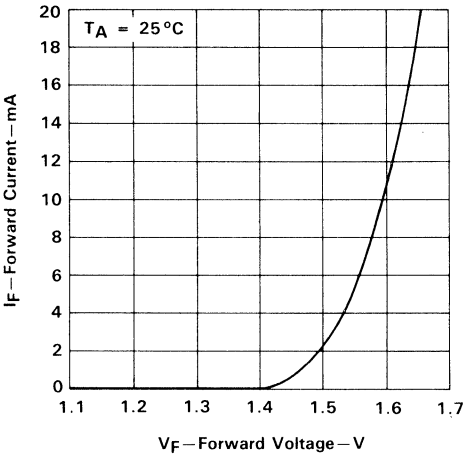

FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

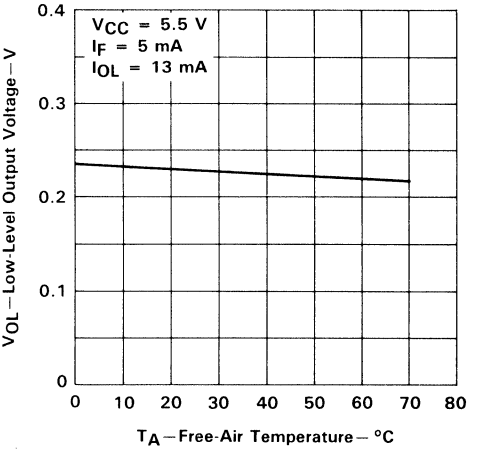

FIGURE 5

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

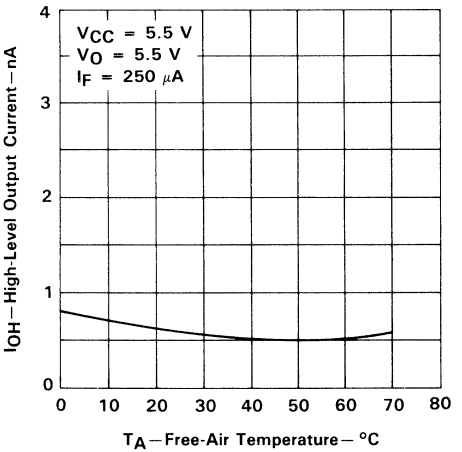

FIGURE 6

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME FROM LED INPUT
VS
PULSE FORWARD CURRENT

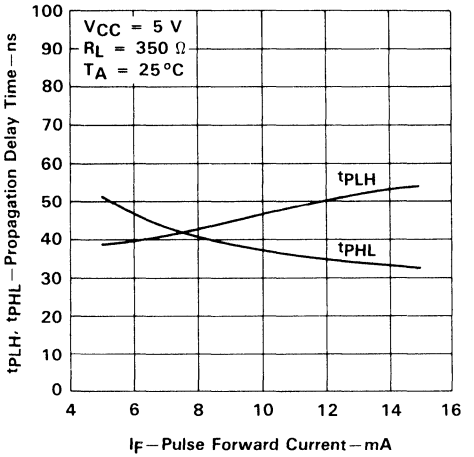


FIGURE 7

PROPAGATION DELAY TIME FROM LED INPUT
VS
LOAD RESISTANCE

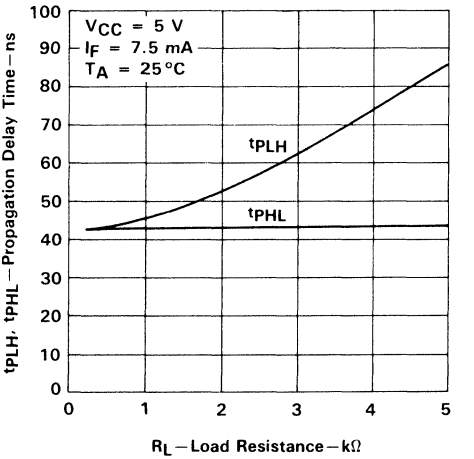


FIGURE 8

Optocouplers (Isolators)

D3262, JUNE 1989

- **Dual-Channel Optocouplers**
- **High Current Transfer Ratio . . . 1800% Typ at I_F = 0.5 mA**
- **Low Input Current Requirement . . . 0.5 mA**
- **High-Speed Switching . . . 100 kbit/s Typ**
- **High Common-Mode Transient Immunity . . . 500 V/μs Typ**
- **High-Voltage Electrical Insulation . . . 3000 V DC Min**
- **High Output Current Rating of 60 mA**
- **UL Recognized . . . File Number 65085**

description

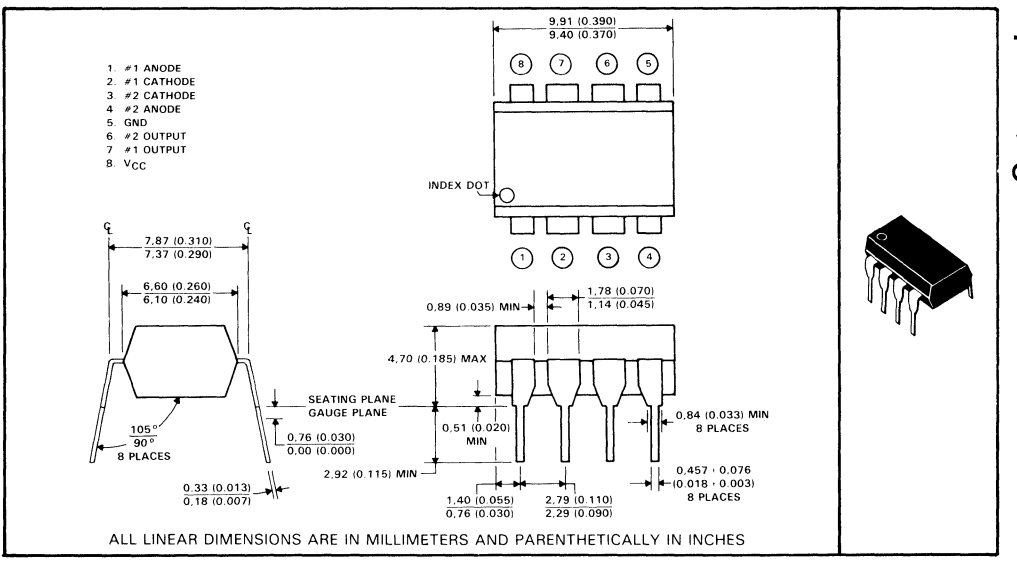
These devices are useful where large common-mode input signals exist, and in applications that require high-voltage isolation between circuits. Applications include line receivers, telephone ring detectors, power line monitors, high-voltage status indicators, and circuits that require isolation between input and output.

The HCPL2730 and HCPL2731 dual-channel high-gain optocouplers each consists of a pair of light-emitting diodes and integrated high-gain photon detectors. The V_{CC} and output terminals may be tied together to achieve conventional photodarlington operation. An integrated emitter-base bypass resistor is provided for low leakage.

The HCPL2730 is designed for use primarily in TTL applications. An LED input current of 1.6 mA and a minimum current-transfer ratio of 300% from 0°C to 70°C allow operation with one TTL-load input and one TTL-load output utilizing a 2.2-kΩ pullup resistor.

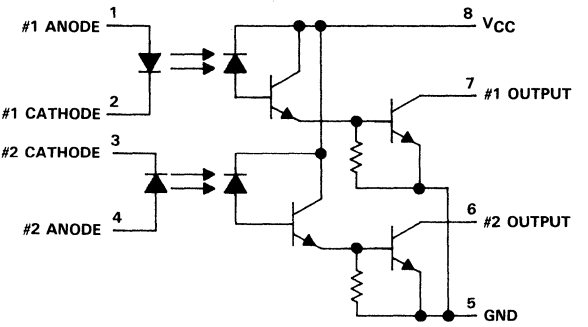
The HCPL2731 is designed for use in CMOS, LSTTL, or other low-power applications. This device has a minimum current-transfer ratio of 400% for only 0.5-mA input current over an operating temperature range of 0°C to 70°C.

mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

schematic



absolute maximum ratings at 25°C free-air temperature range (unless otherwise noted)

Supply and output voltage range, V_{CC} and V_O: HCPL2730 . . . . . −0.5 V to 7 V
HCPL2731 . . . . . −0.5 to 18 V
Reverse input voltage . . . . . 5 V
Peak input forward current per channel (pulse duration = 1 ms, 50% duty cycle) . . . . . 40 mA
Average forward input current per channel at (or below) 50°C free-air temperature (see Note 1) . . . . . 20 mA
Output current per channel at (or below) 35°C free-air temperature (see Note 2) . . . . . 60 mA
Input power dissipation per channel at (or below) 50°C free-air temperature (see Note 3) . . . 35 mW
Output power dissipation per channel at (or below) 35°C free-air temperature (see Note 4) . . . . . 100 mW
Operating temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Derate linearly above 50°C free-air temperature at a rate of 0.57 mA/°C.
2. Derate linearly above 35°C free-air temperature at a rate of 1.2 mA/°C.
3. Derate linearly above 50°C free-air temperature at a rate of 1.0 mW/°C.
4. Derate linearly above 35°C free-air temperature at a rate of 2.0 mW/°C.

TEXAS INSTRUMENTS
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electrical characteristics over operating free-air temperature range of 0 °C to 70 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	HCPL2730			HCPL2731			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_F	Input forward voltage	I_F = 1.6 mA, T_A = 25°C		1.5	1.7		1.5	1.7	V
α_{VF}	Temperature coefficient of forward voltage	I_F = 1.6 mA		−1.8			−1.8		mV/°C
V_{BR}	Input breakdown voltage	I_R = 10 μA, T_A = 25°C	5			5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_F = 1.6 mA, I_{OL} = 4.8 mA, I_B = 0		0.1	0.4				V
		V_{CC} = 4.5 V, I_F = 1.6 mA, I_{OL} = 8 mA, I_B = 0					0.1	0.4	
		V_{CC} = 4.5 V, I_F = 5 mA, I_{OL} = 15 mA, I_B = 0					0.1	0.4	
		V_{CC} = 4.5 V, I_F = 12 mA, I_{OL} = 24 mA, I_B = 0					0.2	0.4	
I_{OH}	High-level output current	V_{CC} = 7 V, V_O = 7 V, I_F = 0, I_B = 0		0.1	250				μA
		V_{CC} = 18 V, V_O = 18 V, I_F = 0, I_B = 0					0.05	100	
I_{CCH}	Supply current, high-level output	V_{CC} = 7 V, I_O = 0, I_F = 0, I_B = 0		4					nA
		V_{CC} = 18 V, I_O = 0, I_F = 0, I_B = 0					5		
I_{CCL}	Supply current, low-level output	V_{CC} = 7 V, I_O = 0, I_{F1} = 1.6 mA, I_{F2} = 1.6 mA I_B = 0		0.4					mA
		V_{CC} = 18 V, I_O = 0, I_{F1} = 1.6 mA, I_{F2} = 1.6 mA I_B = 0					0.6		
CTR	Current transfer ratio	V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 0.5 mA, I_B = 0, See Note 5				400%	1800%		
		V_{CC} = 4.5V, V_O = 0.4 V, I_F = 1.6 mA, I_B = 0, See Note 5	300%	1000%		500%	1600%		
r_{ii}	Input-input resistance	V_{ii} = 500 V		10^{11}			10^{11}		Ω
r_{io}	Input-output resistance	V_{io} = 500 V, See Note 6		10^{12}			10^{12}		Ω
I_{ii}	Input-input insulation leakage current	V_{ii} = 500 V, t = 5 s, RH = 45%		0.005			0.005		μA
I_{io}	Input-output insulation leakage current	V_{io} = 3000 V, t = 5 s, T_A = 25°C, RH = 45%, See Note 6			1			1	μA
C_i	Input capacitance	V_F = 0, f = 1 MHz		60			60		pF
C_{ii}	Input-input capacitance	f = 1 MHz		0.25			0.25		pF
C_{io}	Input-output capacitance	f = 1 MHz, See Note 6		0.6			0.6		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C, unless otherwise noted.

NOTES: 5. Current transfer ratio is defined as the ratio of output collector current I_O to the forward LED input current I_F times 100%.
6. These parameters are measured between pins 2 and 3 shorted together and pins 5, 6, 7 and 8 shorted together.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	HCPL2730			HCPL2731			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation delay time, high-to-low level output	I_F = 1.6 mA, R_L = 2.2 kΩ, See Figure 1		2	20		2	20	μs
		I_F = 0.5 mA, R_L = 4.7 kΩ See Figure 1					7	100	
		I_F = 12 mA, R_L = 270 Ω, See Figure 1		0.4	2		0.4	2	
t_{PLH}	Propagation delay time, low-to-high-level output	I_F = 1.6 mA, R_L = 2.2 kΩ See Figure 1		4	35		5	35	μs
		I_F = 0.5 mA, R_L = 4.7 kΩ See Figure 1					6	60	
		I_F = 12 mA, R_L = 270 Ω, See Figure 1		3	10		2	10	
$\frac{dV_{CM}}{dt}$ (H)	Common-mode input transient immunity, high-level output	V_{CM} = 10 Vp-p, I_F = 0, R_L = 2.2 kΩ, See Notes 7 and 8, See Figure 2		500			500		V/μs
$\frac{dV_{CM}}{dt}$ (L)	Common-mode input transient immunity, low-level output	V_{CM} = 10 Vp-p, I_F = 1.6 mA, R_L = 2.2 kΩ, See Figure 2 See Notes 7 and 8		−500			−500		V/μs

NOTES: 7. Common-mode transient immunity, high-level output, is the maximum rate of rise of the common-mode input voltage that does not cause the output voltage to drop below 2 V. Common-mode input transient immunity, low-level output, is the maximum rate of fall of the common-mode input voltage that does not cause the output voltage to rise above 0.8 V.

8. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is:

$$R_{CC} \approx \frac{1}{0.15\ I_F\ (mA)}\ k\Omega$$

TEXAS INSTRUMENTS
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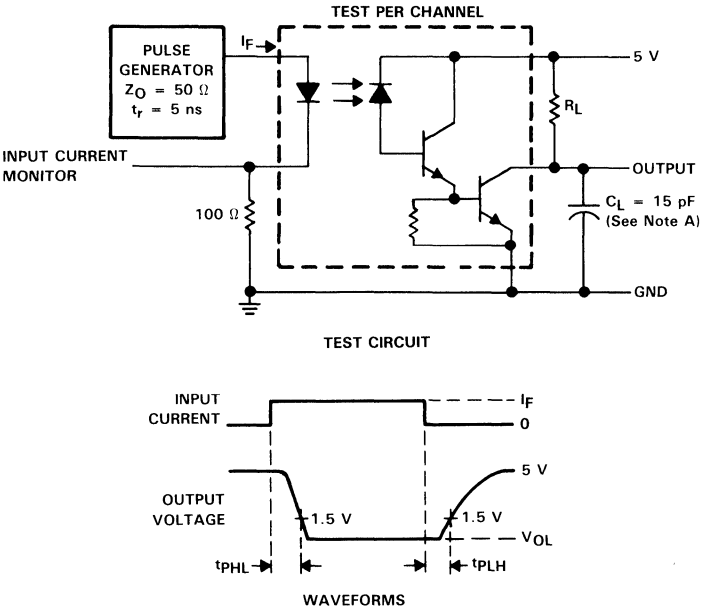
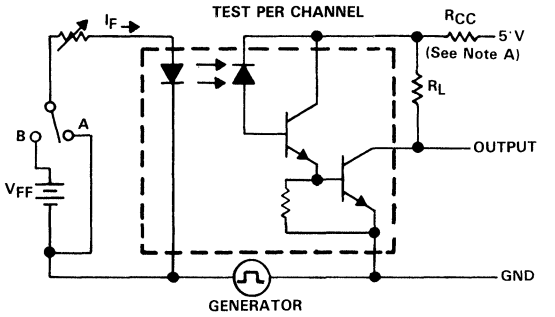
PARAMETER MEASUREMENT INFORMATION



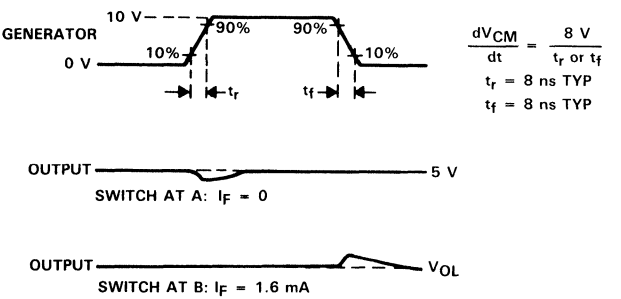
NOTE A: C_L includes probe and stray capacitances.

FIGURE 1. SWITCHING TEST CIRCUIT AND WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

NOTE A: In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is:

$$R_{CC} \approx \frac{1}{0.15\ I_F\ (\text{mA})}\ \text{k}\Omega$$

FIGURE 2. TRANSIENT IMMUNITY TEST CIRCUIT AND WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

HCPL2730
CURRENT TRANSFER CHARACTERISTICS

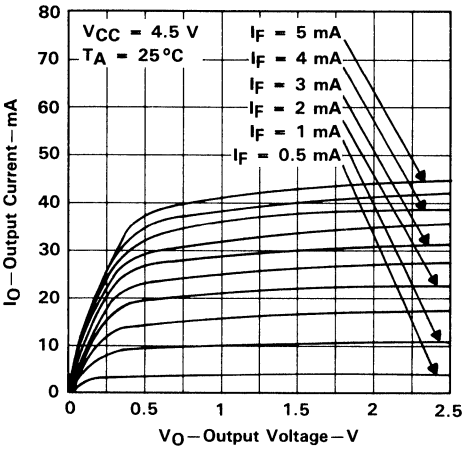


FIGURE 3

HCPL2731
CURRENT TRANSFER CHARACTERISTICS

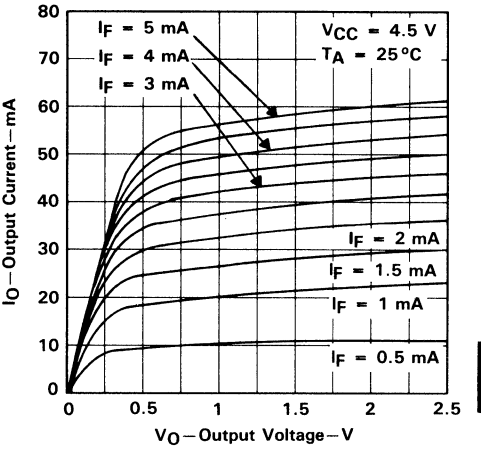


FIGURE 4

INPUT DIODE FORWARD CURRENT
vs
FORWARD VOLTAGE

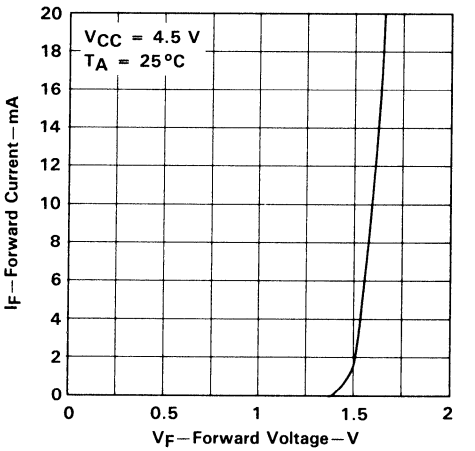


FIGURE 5

OUTPUT CURRENT
vs
INPUT DIODE FORWARD CURRENT

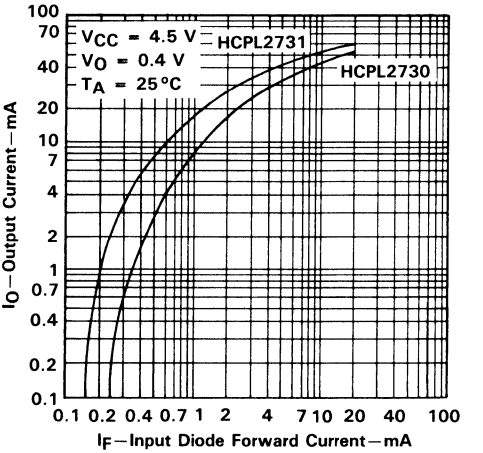


FIGURE 6

3 Optocouplers (Isolators)

TYPICAL CHARACTERISTICS

CURRENT TRANSFER RATIO
vs
INPUT DIODE FORWARD CURRENT

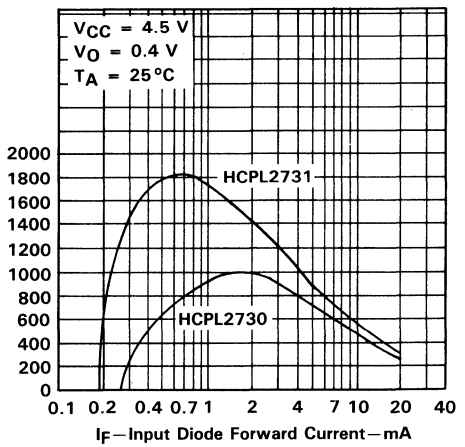


FIGURE 7

HCPL2730
RELATIVE CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

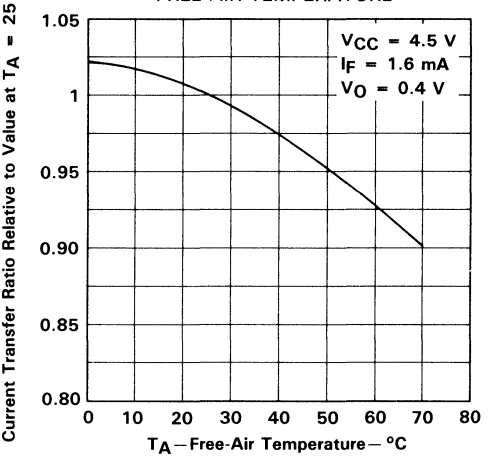


FIGURE 8

HCPL2731
RELATIVE CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

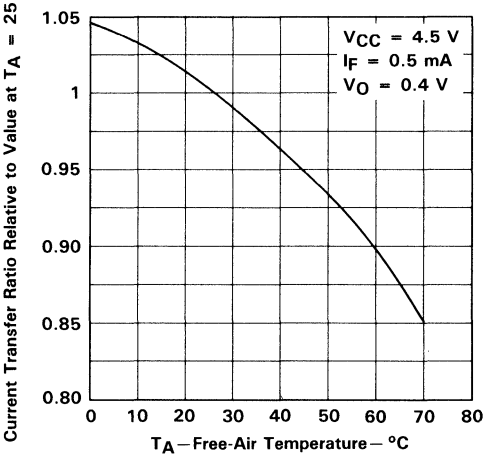


FIGURE 9

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

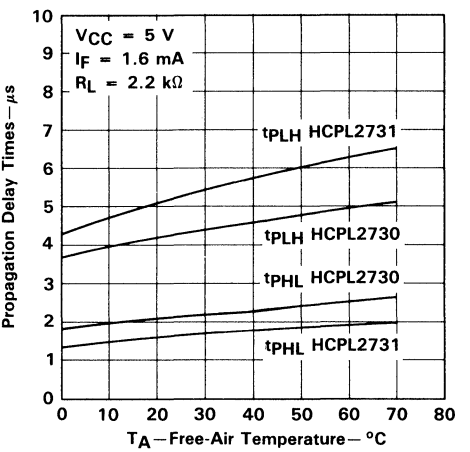


FIGURE 10

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

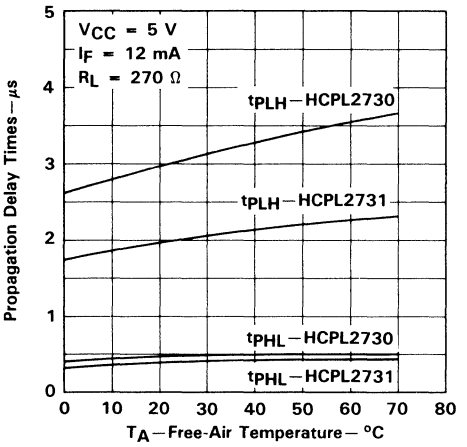


FIGURE 11

HCPL2731
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

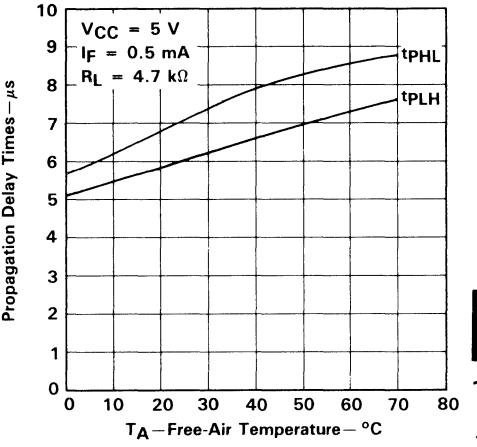


FIGURE 12

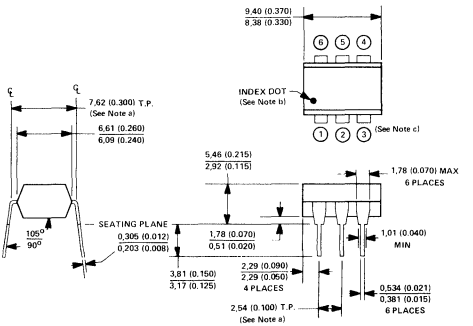
D2731, MARCH 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **Base Lead Provided for Conventional Transistor Biasing**
- **High-Voltage Electrical Isolation . . . 1.5-kV or 3.55-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 5 μs, t_f = 5 μs Typical**
- **Designed to be Interchangeable with General Instruments MCT2 and MCT2E**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:

a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

b. Pin 1 identified by index dot.

c. Terminal connections:

1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage: MCT2	±1.5 kV
MCT2E	±3.55 kV
Collector-Base Voltage	70 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current	60 mA
Input-Diode Peak Forward Current ($t_w \leq 1$ ns, PRF ≤ 300 Hz)	3 A
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature	
Infrared-Emitting Diode (See Note 2)	200 mW
Phototransistor (See Note 2)	200 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 3)	250 mW
Operating Free-Air Temperature Range	−55°C to 100°C
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 2.67 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS		MCT2, MCT2E MIN	MCT2, MCT2E TYP	MCT2, MCT2E MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		I_C = 10 μA, I_F = 0	I_E = 0,	70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		I_C = 1 mA, I_F = 0	I_B = 0,	30			V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage		I_E = 100 μA, I_F = 0	I_B = 0,	7			V
I_R	Input Diode Static Reverse Current		V_R = 3 V				10	μA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_B = 0	I_F = 10 mA,	2	5		mA
		Photodiode Operation	V_{CB} = 10 V, I_E = 0	I_F = 10 mA,		20		μA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_B = 0	I_F = 0		1	50	nA
		Photodiode Operation	V_{CB} = 10 V, I_E = 0	I_F = 0,		0.1	20	
h_{FE}	Transistor Static Forward Current Transfer Ratio		V_{CE} = 5 V, I_C = 100 μA, I_F = 0	MCT2		250		
				MCT2E	100	300		
V_F	Input Diode Static Forward Voltage		I_F = 20 mA			1.25	1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		I_C = 2 mA, I_B = 0	I_F = 16 mA,		0.25	4	V
r_{IO}	Input-to-Output Internal Resistance		V_{in-out} = ±1.5 kV for MCT2 ±3.55 kV for MCT2E See Note 4		10^{11}			Ω
C_{io}	Input-to-Output Capacitance		V_{in-out} = 0, See note 4	f = 1 MHz,		1		pF

NOTE 4: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MCT2, MCT2E MIN	MCT2, MCT2E TYP	MCT2, MCT2E MAX	UNIT
t_r	Rise Time	Phototransistor Operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5		μs
t_f	Fall Time						
t_r	Rise Time	Photodiode Operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall Time						

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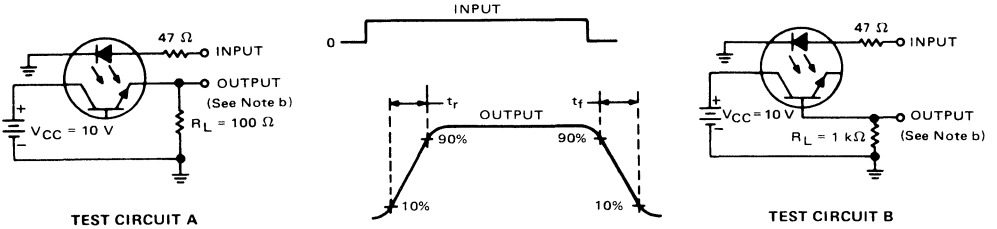
PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

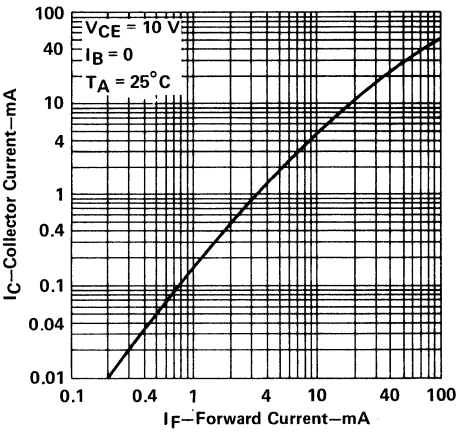


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

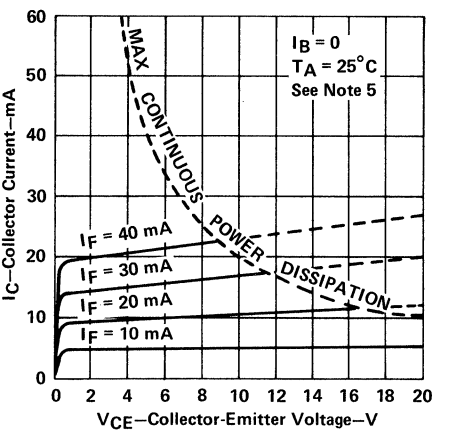


FIGURE 3

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

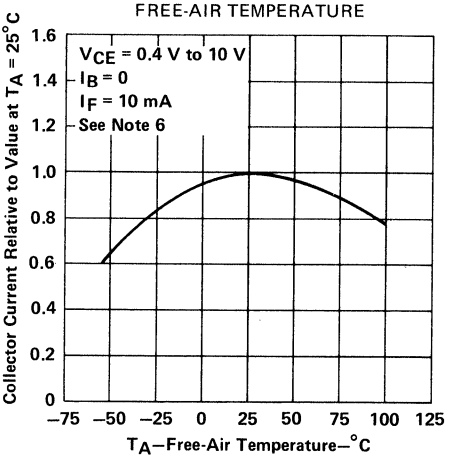


FIGURE 4

NOTES: 5. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
6. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

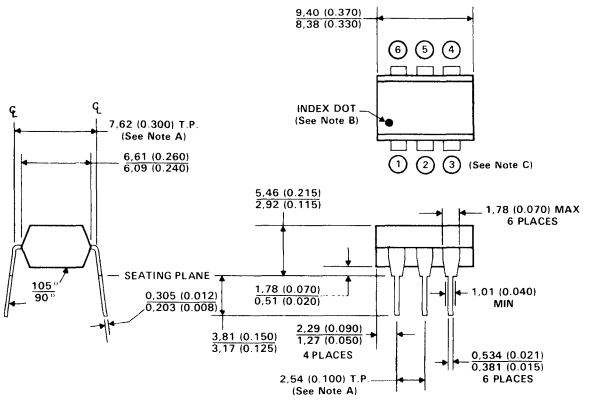
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2998, AUGUST 1985

- 250 V Phototriac Driver Output
- Gallium Arsenide Diode Infrared Source and Optically Coupled Silicon Triac Driver (Bilateral Switch)
- UL Recognized . . . File Number E65085
- High Isolation . . . 7500 V Peak
- Output Driver Designed for 115 V AC
- Standard 6-Pin Plastic DIP
- Directly Interchangeable with Motorola MOC3009, MOC3010, MOC3011, and MOC3012
- Direct Replacements for: TRW Optron OPI3009, OPI3010, OPI3011, and OPI3012; General Instrument MCP3009, MCP3010, MCP3011; General Electric GE3009, GE3010, GE3011, and GE3012

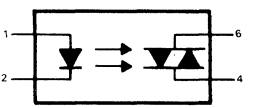
mechanical

Each device consists of a gallium arsenide infrared emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:

1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Main terminal
5. Triac substrate (DO NOT connect) } Phototriac
6. Main terminal



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1) . . . . . 7.5 kV
Input diode reverse voltage . . . . . 3 V
Input diode forward current, continuous . . . . . 50 mA
Output repetitive peak off-state voltage . . . . . 250 V
Output on-state current, total rms value (50-60 Hz, full sine wave):
  T_A = 25°C . . . . . 100 mA
  T_A = 70°C . . . . . 50 mA
Output driver nonrepetitive peak on-state current
  (t_W = 10 ms, duty cycle = 10%, see Figure 7) . . . . . 1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:
  Infrared-emitting diode (see Note 2) . . . . . 100 mW
  Phototriac (see Note 3) . . . . . 300 mW
  Total device (see Note 4) . . . . . 330 mW
Operating junction temperature range . . . . . −40°C to 100°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	μA
V_F	Static forward voltage		I_F = 10 mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		V_{DRM} = 250 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		12		V/μs
dv/dt(c)	Critical rate of rise of commutating voltage		I_O = 15 mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current, either direction	MOC3009	Output supply voltage = 3 V		15	30	mA
		MOC3010			8	15	
		MOC3011			5	10	
		MOC3012				5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.8	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied within dv/dt rating.

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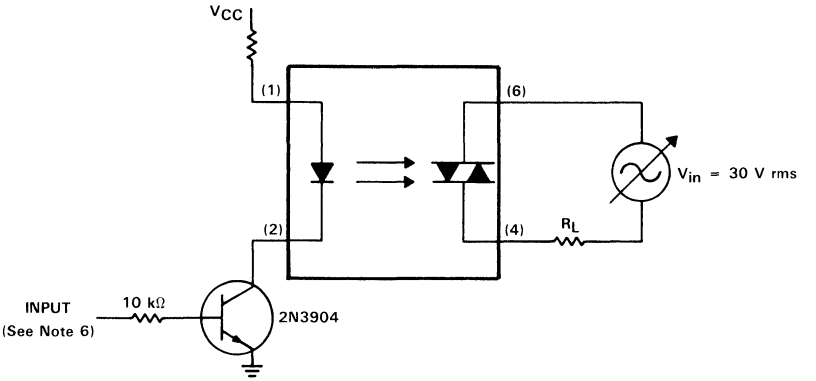
PARAMETER MEASUREMENT INFORMATION



NOTE 6: The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 volts. The frequency of V_{in} is increased until the phototriac just turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

FIGURE 1. CRITICAL RATE OF RISE TEST CIRCUIT

TYPICAL CHARACTERISTICS

EMITTING DIODE NORMALIZED TRIGGER CURRENT
vs
FREE-AIR TEMPERATURE

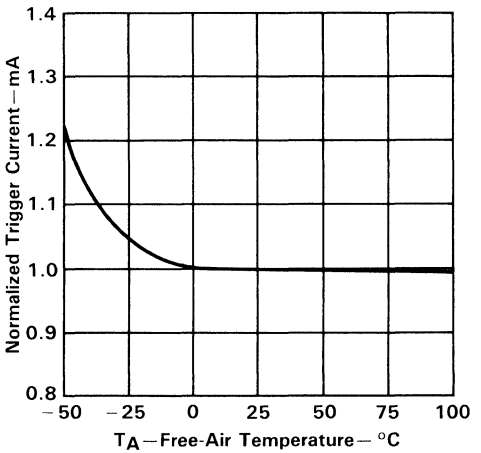


FIGURE 2

ON-STATE CHARACTERISTICS

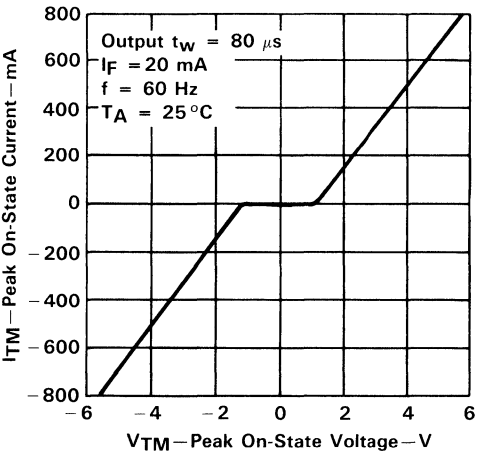


FIGURE 3

TYPICAL CHARACTERISTICS

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
vs
LOAD RESISTANCE

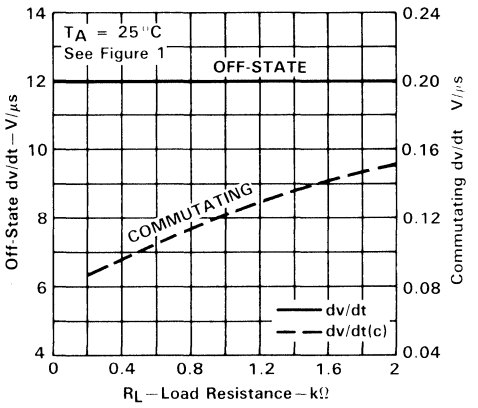


FIGURE 4

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

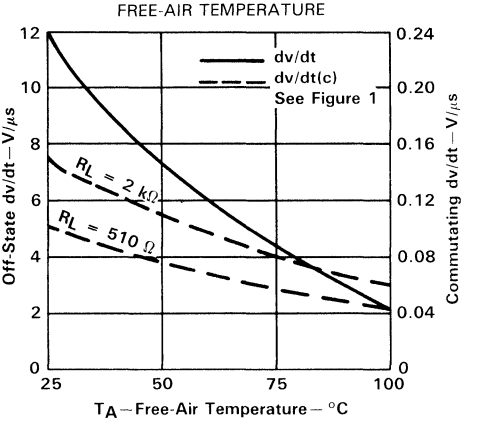


FIGURE 5

RMS APPLIED VOLTAGE
(FOR dv/dt(c) = 0.15 V/μs)
vs
FREQUENCY

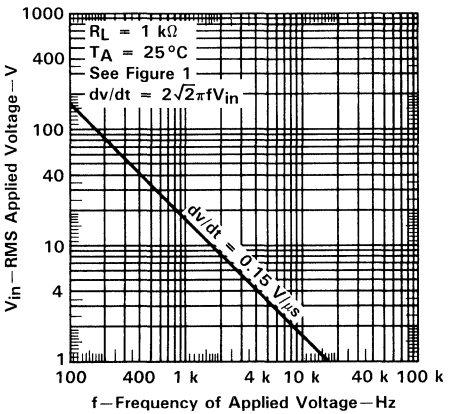


FIGURE 6

TEXAS INSTRUMENTS
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MAXIMUM RATINGS

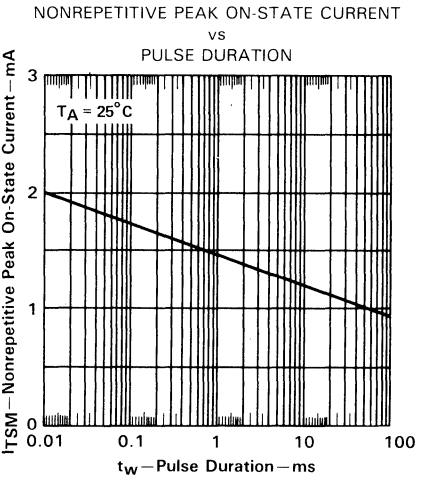


FIGURE 7

TYPICAL APPLICATIONS

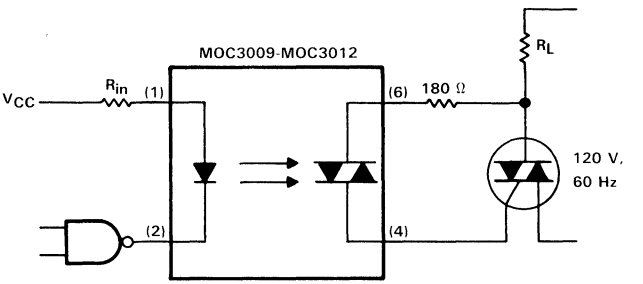


FIGURE 8. RESISTIVE LOAD

TYPICAL APPLICATIONS

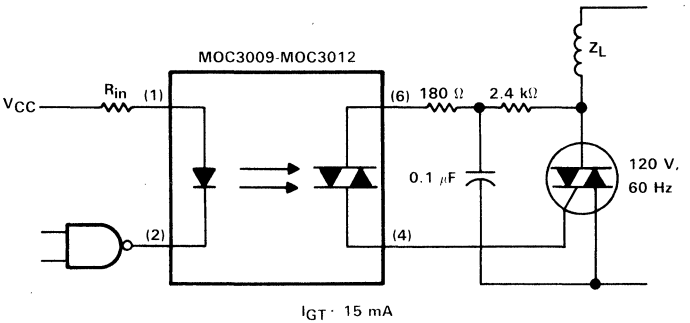


FIGURE 9. INDUCTIVE LOAD WITH SENSITIVE-GATE TRIAC

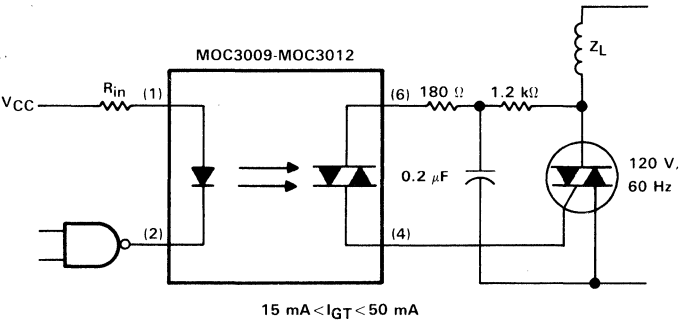


FIGURE 10. INDUCTIVE LOAD WITH NONSENSITIVE-GATE TRIAC

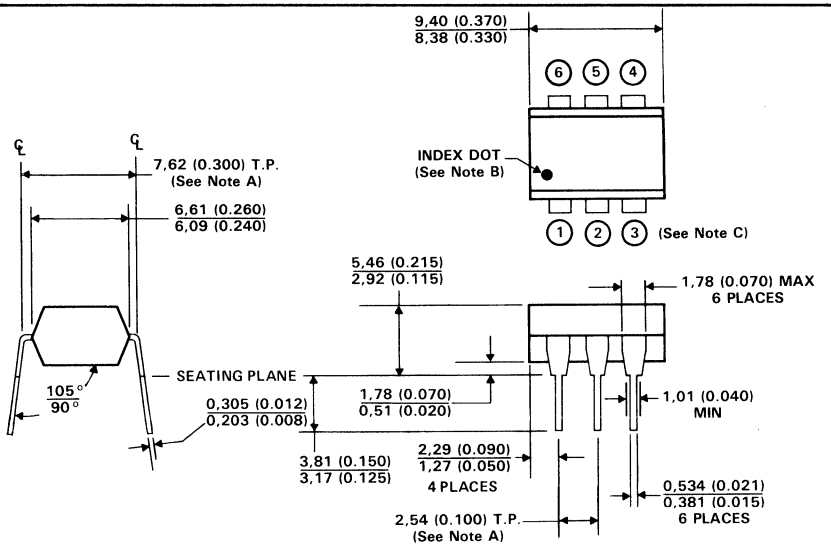
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2899, OCTOBER 1986

- 400-V Phototriac Driver Output
- Gallium Arsenide Diode Infrared Source and Optically Coupled Silicon Triac Driver (Bilateral Switch)
- UL Recognized . . . File Number E65085
- High Isolation . . . 7500 V Peak
- Output Driver Designed for 220 V AC
- Standard 6-Pin Plastic DIP
- Directly Interchangeable with Motorola MOC3020, MOC3021, MOC3022, and MOC3023
- Direct Replacements for:
  TRW Optron OPI3020, OPI3021, OPI3022, and OPI3023;
  General Instrument MCP3020, MCP3021, MCP3022;
  General Electric GE3020, GE3021, GE3022, and GE3023

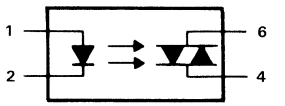
mechanical

Each device consists of a gallium arsenide infrared emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.



FALLS WITHIN JEDEC MO-001 AM DIMENSIONS

NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Main terminal
5. Triac Substrate (DO NOT connect) } Phototriac
6. Main terminal



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1) . . . . . 7.5 kV
Input diode reverse voltage . . . . . 3 V
Input diode forward current, continuous . . . . . 50 mA
Output repetitive peak off-state voltage . . . . . 400 V
Output on-state current, total rms value (50-60 Hz, full sine wave):
  T_A = 25°C . . . . . 100 mA
  T_A = 70°C . . . . . 50 mA
Output driver nonrepetitive peak on-state current
  (t_W = 10 ms, duty cycle = 10%, see Figure 7) . . . . . 1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:
  Infrared-emitting diode (see Note 2) . . . . . 100 mW
  Phototriac (see Note 3) . . . . . 300 mW
  Total device (see Note 4) . . . . . 330 mW
Operating junction temperature range . . . . . −40°C to 100°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	μA
V_F	Static forward voltage		I_F = 10 mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		V_{DRM} = 400 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		100		V/μs
dv/dt(c)	Critical rate of rise of commutating voltage		I_O = 15 mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current, either direction	MOC3020	Output supply voltage = 3 V		15	30	mA
		MOC3021			8	15	
		MOC3022			5	10	
		MOC3023			3	5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.4	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied at a rate no higher than 12 V/μs.

TEXAS INSTRUMENTS
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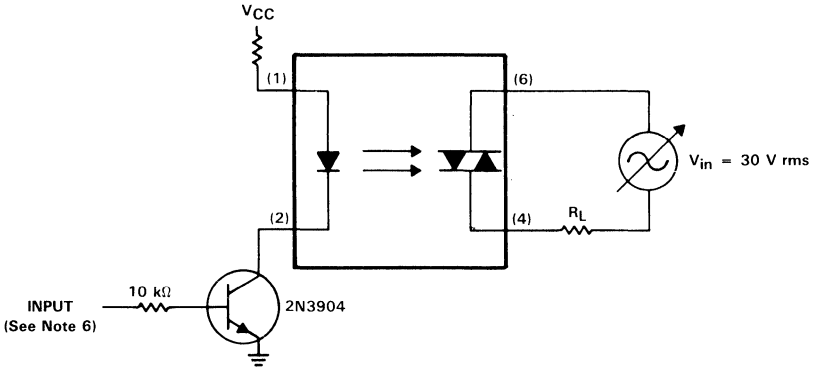
PARAMETER MEASUREMENT INFORMATION



NOTE 6: The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 volts. The frequency of V_{in} is increased until the phototriac just turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

FIGURE 1. CRITICAL RATE OF RISE TEST CIRCUIT

TYPICAL CHARACTERISTICS

EMITTING DIODE NORMALIZED TRIGGER CURRENT
vs
FREE-AIR TEMPERATURE

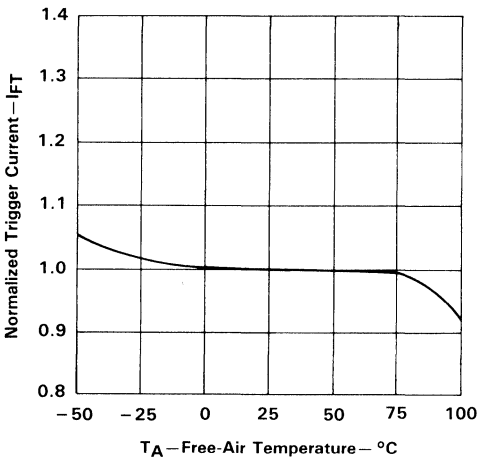


FIGURE 2

ON-STATE CHARACTERISTICS

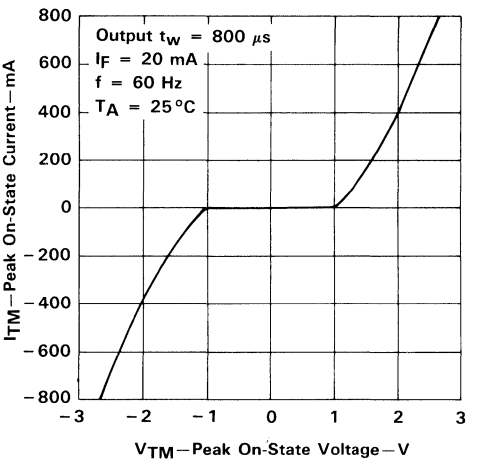


FIGURE 3

MAXIMUM RATINGS

NONREPETITIVE PEAK ON-STATE CURRENT
vs
PULSE DURATION

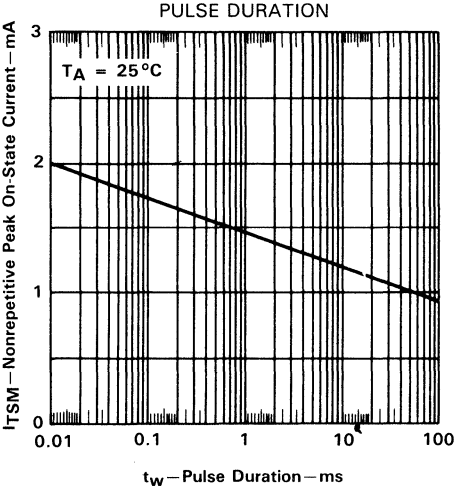


FIGURE 4

TYPICAL APPLICATIONS

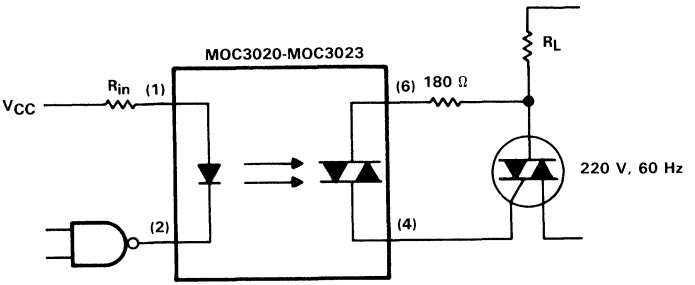


FIGURE 5. RESISTIVE LOAD

TEXAS INSTRUMENTS
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TYPICAL APPLICATIONS

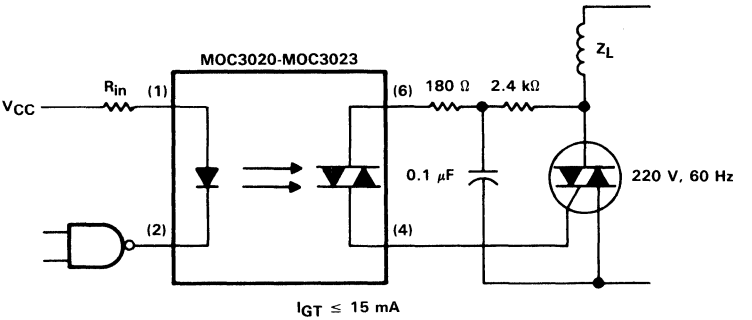


FIGURE 6. INDUCTIVE LOAD WITH SENSITIVE-GATE TRIAC

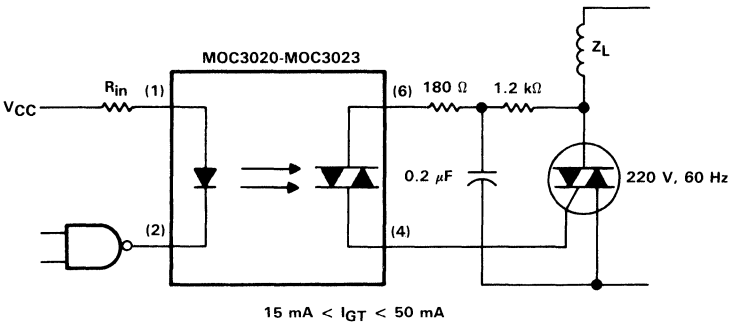


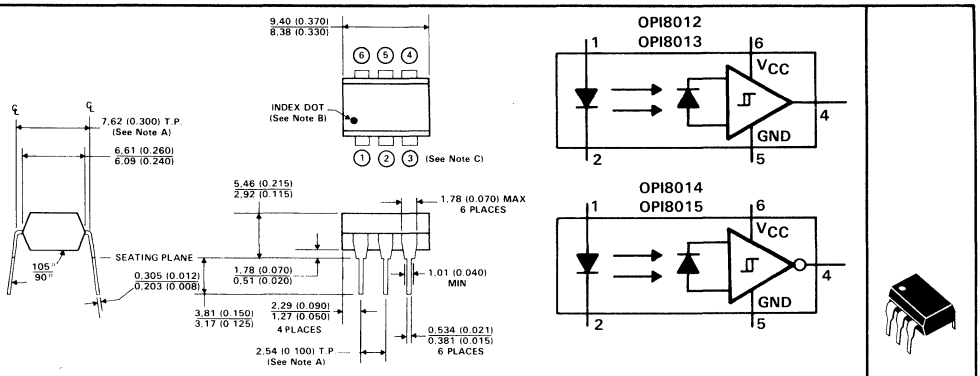
FIGURE 7. INDUCTIVE LOAD WITH NONSENSITIVE-GATE TRIAC

D2961, SEPTEMBER 1986

- **Gallium Arsenide Emitter Optically Coupled to a Photo-Detector Integrated Circuit**
- **Output Compatible with TTL/LSTTL Logic Levels**
- **Fan-Out of 8 TTL Loads**
- **Four Output Versions:**
  - **OPI8012 Buffer Totem-Pole**
  - **OPI8013 Buffer Open-Collector**
  - **OPI8014 Inverter Totem-Pole**
  - **OPI8015 Inverter Open-Collector**
- **High-Voltage Electrical Isolation . . . 3540-V Peak Rating**
- **Directly Interchangeable with TRW Optron OPI8012, OPI8013, OPI8014, OPI8015**
- **Standard 6-Pin Dual-In-Line Package**
- **Schmitt Trigger Stage with Hysteresis for High Noise Immunity**
- **200-kilobaud Data Rate**
- **70-ns Maximum Rise Time or Fall Time**
- **UL Recognized — File Number E65085**

mechanical data

Each device consists of a gallium arsenide infrared emitting diode and a silicon monolithic photo-detector integrated circuit. The device is mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The photo-detector IC incorporates a photodiode, a linear amplifier, a Schmitt Trigger hysteresis stage, and a digital output stage.



FALLS WITHIN JEDEC MO 001 AM DIMENSIONS

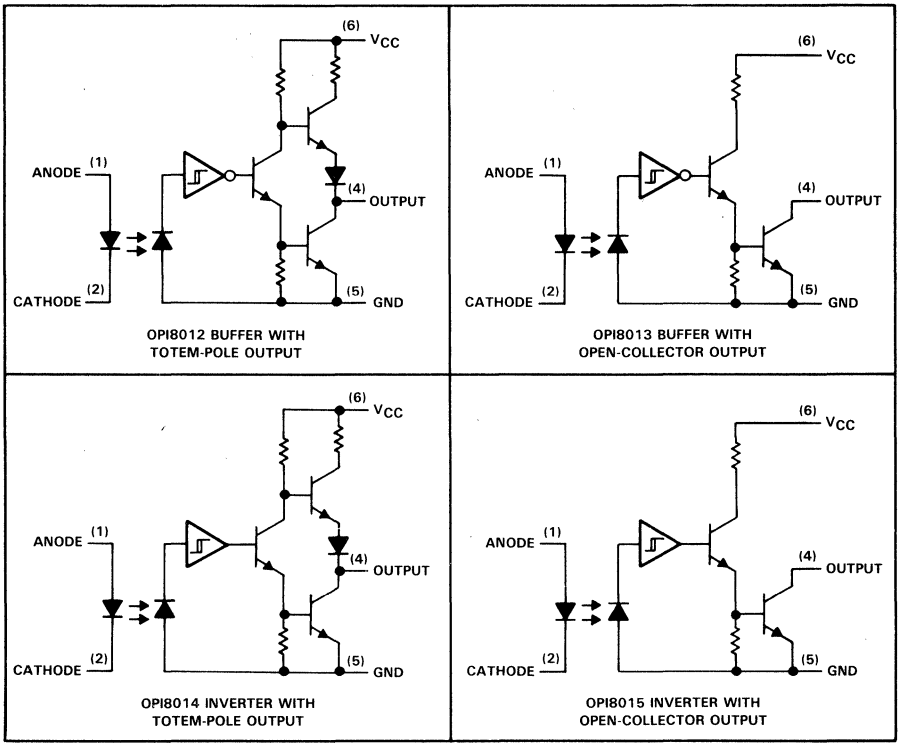
NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:

1. Anode	Infrared-emitting diode	4. Output	Photo-detector IC
2. Cathode		5. GND	
3. No internal connection		6. Supply Voltage, V_{CC}	

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

schematic diagrams



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC}	10 V
Peak input-to-output isolation voltage (see Note 1)	3540 V
Output voltage (OPI8013, OPI8015)	35 V
Input diode reverse voltage	3 V
Input diode continuous forward current	25 mA
Continuous total power dissipation at (or below) 25°C free-air temperature:	
Input diode (see Note 2)	100 mW
Output IC (see Note 3)	200 mW
Total (input diode plus output IC, see Note 4)	250 mW
Duration of output short to V_{CC} or GND (OPI8012, OPI8014)	1 s
Duration of output short to V_{CC} (OPI8013, OPI8015)	1 s
Storage temperature range	−55°C to 150°C
Operating free-air temperature range	−55°C to 100°C
Lead temperature 1,6 mm (1/16 inch) from the case for 1 second	260°C

NOTES: 1. This rating applies between the input leads (pins 1 and 2) shorted together and the output, V_{CC}, and GND leads (pins 4, 5, and 6) shorted together.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C
3. Derate linearly to 100°C free-air temperature at the rate of 2.67 mW/°C
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C

recommended operating conditions

	OPI8012 OPI8014			
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−800	μA
Low-level output current, I_{OL}			12.8	mA
Operating free-air temperature, T_A	−40		70	°C

electrical characteristics, T_A = −40°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		OPI8012			OPI8014			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_F	Input diode forward voltage	I_F = 10 mA, T_A = 25°C			1.2	1.5		1.2	1.5	V
I_R	Input diode reverse current	V_R = 3 V, T_A = 25°C				100			100	μA
I_{FT+}	Input diode positive-going threshold current	V_{CC} = 5 V			1.5	10		1.5	10	mA
I_{FT+}/I_{FT-}	Hysteresis ratio	V_{CC} = 5 V			1.4			1.4		
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_F = 0				2.4	3.2		V
		I_{OH} = −800 μA	I_F = 10 mA	2.4	3.2					
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_F = 0		0.2	0.4				V
		I_{OL} = 12.8 mA	I_F = 10 mA					0.2	0.4	
I_{OS}	Short-circuit output current	V_{CC} = 5.25 V,	I_F = 0				−30	−50	−100	mA
		V_O = 0	I_F = 10 mA	−30	−50	−100				
I_{CC}	Supply current	V_{CC} = 5.25 V	I_F = 0		8	15		4	15	mA
			I_F = 10 mA		10	15		9	15	

†Typical values are at T_A = 25°C.

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	OPI8012			OPI8014			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_{CC} = 5 V, I_F = 10 mA, See Figure 1 Output load: 8 TTL equivalent circuits		25	70		25	70	ns
t_f	Fall time			9	70		9	70	ns
t_{PLH}	Propagation delay time, low-to-high-level output			1	5		3	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output			3	5		1	5	μs

recommended operating conditions

	OPI8013 OPI8015			
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output voltage, V_{OH}			30	V
Low-level output current, I_{OL}			12.8	mA
Operating free-air temperature, T_A	−40		70	°C

electrical characteristics, T_A = −40°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		OPI8013			OPI8015			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_F	Input diode forward voltage	I_F = 10 mA,	T_A = 25°C		1.2	1.5		1.2	1.5	V
I_R	Input diode reverse current	V_R = 3 V,	T_A = 25°C			100			100	μA
I_{FT+}	Input diode positive-going threshold current	V_{CC} = 5 V			1.5	10		1.5	10	mA
I_{FT+}/I_{FT-}	Hysteresis ratio	V_{CC} = 5 V			1.4			1.4		
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{OH} = 30 V	I_F = 0					0.02	100	μA
			I_F = 10 mA		2	100				
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 12.8 mA	I_F = 0		0.2	0.4				V
			I_F = 10 mA					0.2	0.4	
I_{CC}	Supply current	V_{CC} = 5.25 V	I_F = 0		8	15		4	15	mA
			I_F = 10 mA		10	15		9	15	

†Typical values are at T_A = 25°C.

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		OPI8013			OPI8015			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_{CC} = 5 V, R_L = 360 Ω,	I_F = 10 mA, See Figure 1		30	70		30	70	ns
t_f	Fall time				9	70		9	70	ns
t_{PLH}	Propagation delay time, low-to-high-level output				1	5		3	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output				3	5		1	5	μs

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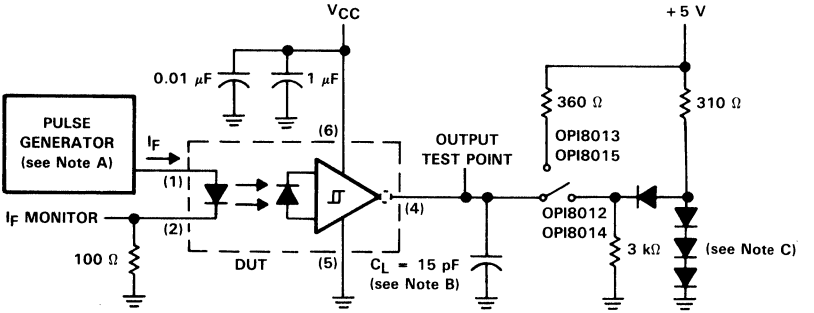
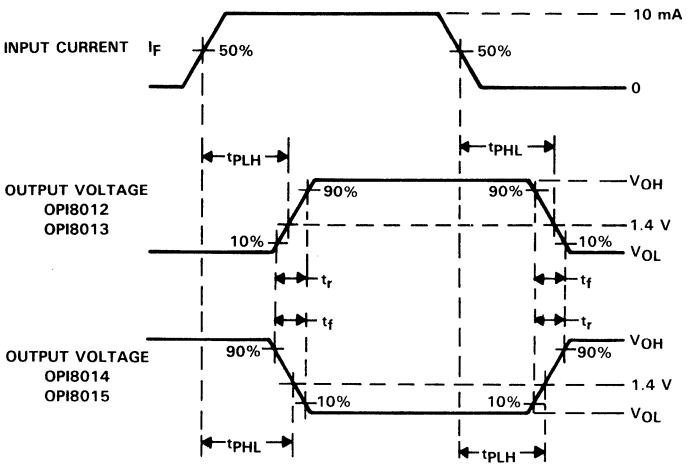
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

NOTES: A. The input pulse is supplied by a pulse generator with the following characteristics: PRF = 10 kHz, duty cycle = 50%, t_r < 20 ns, t_f < 20 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.

FIGURE 1. SWITCHING TIMES

POSITIVE-GOING THRESHOLD CURRENT
vs
FREE-AIR TEMPERATURE

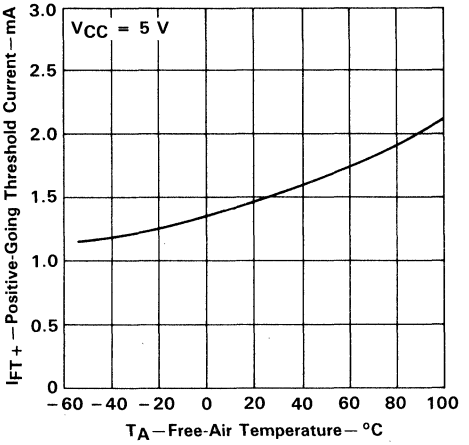


FIGURE 2

HYSTERESIS RATIO
vs
FREE-AIR TEMPERATURE

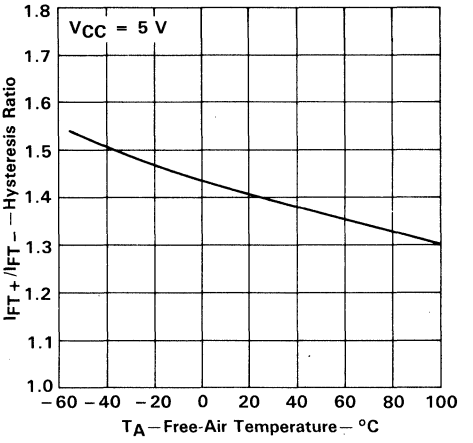


FIGURE 3

OPI8012, OPI8014
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

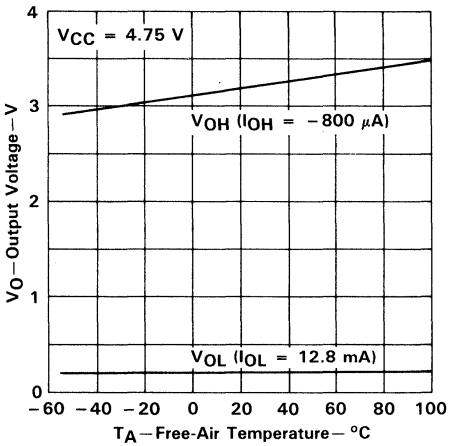


FIGURE 4

OPI8013, OPI8015
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

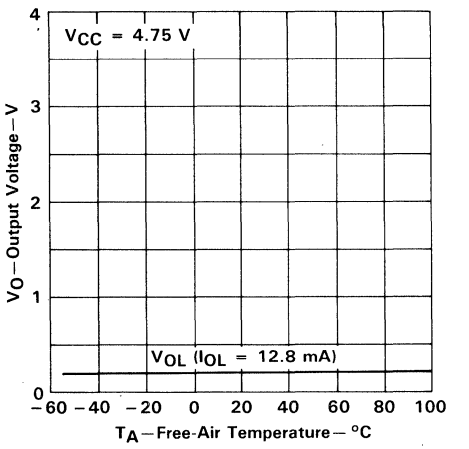


FIGURE 5

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TYPICAL CHARACTERISTICS

OPI8013, OPI8015
HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

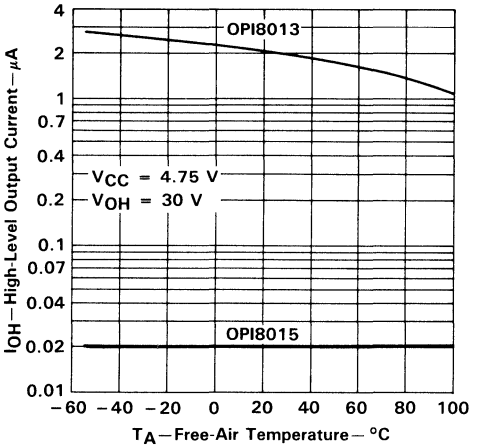


FIGURE 6

OPI8012, OPI8014
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

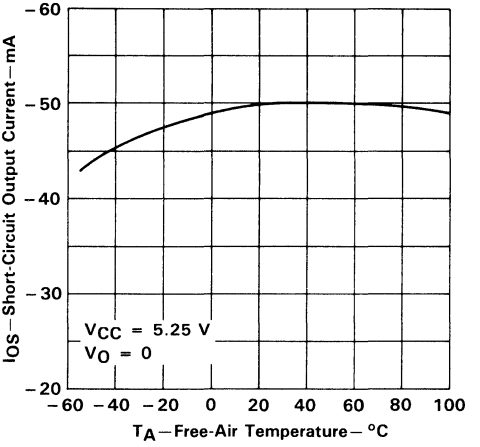


FIGURE 7

OPI8012, OPI8013
NORMALIZED SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

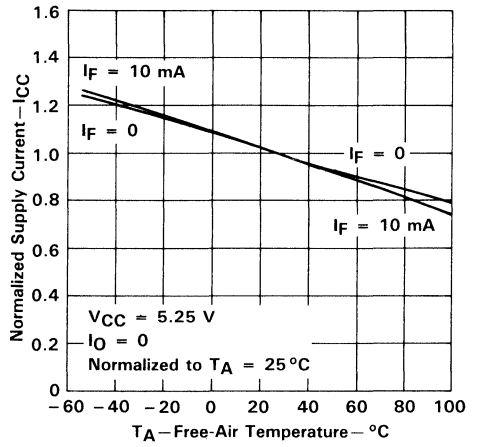


FIGURE 8

OPI8014, OPI8015
NORMALIZED SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

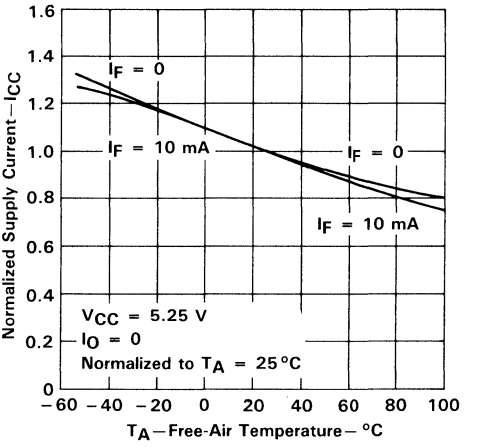


FIGURE 9

OPI8012, OPI8014
RISE TIME AND FALL TIME
vs
FREE-AIR TEMPERATURE

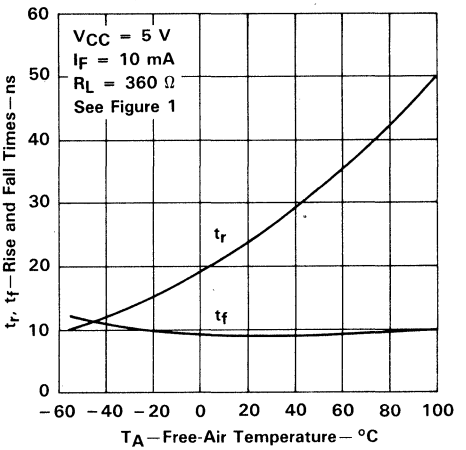


FIGURE 10

OPI8013, OPI8015
RISE TIME AND FALL TIME
vs
FREE-AIR TEMPERATURE

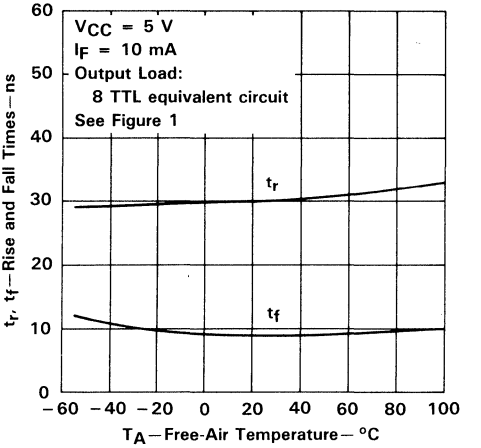


FIGURE 11

OPI8012, OPI8013
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

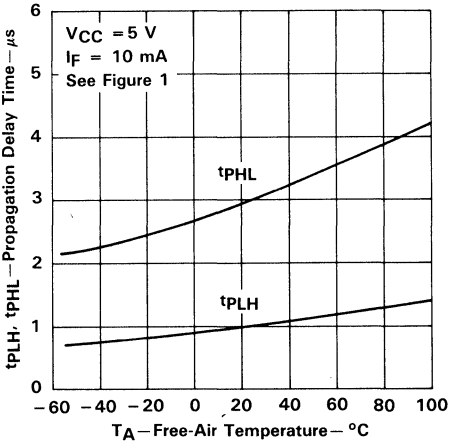


FIGURE 12

OPI8014, OPI8015
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

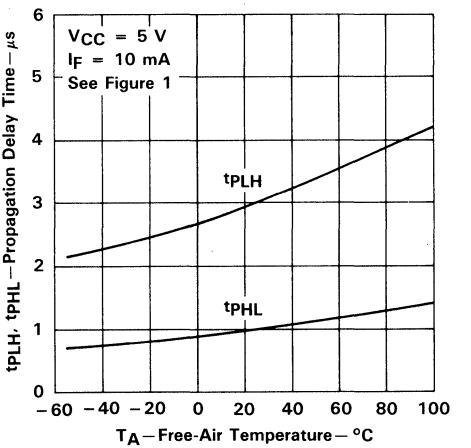


FIGURE 13

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

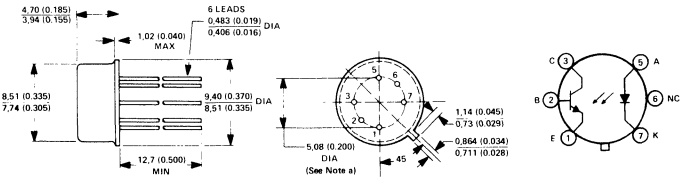
D910, SEPTEMBER 1970—REVISED NOVEMBER 1974

GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

- Photon Coupling for Isolator Applications
- Base Lead Provided for Conventional Transistor Biasing
- High Overall Current Gain . . . 1.5 Typ (TIL103)
- High-Voltage Transistor . . . $V_{(BR)CEO}$ = 35 V Min
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable over Wide Temperature Range

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



NOTE a: Leads having maximum diameter shall be with 0,18 mm (0.007 inches) of true position relative to a maximum-width tab when measured in the gaging plane between 1,371 mm (0.054 inches) and 1,397 mm (0.055 inches) below the seating plane.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±1 kV
Collector-Emitter Voltage	35 V
Collector-Base Voltage	35 V
Emitter-Base Voltage	4 V
Input Diode Reverse Voltage	2 V
Input Diode Continuous Forward Current at (or below) 65°C Free-Air Temperature (See Note 1)	40 mA
Continuous Collector Current	50 mA
Continuous Transistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	300 mW
Storage Temperature Range	−55°C to 125°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	240°C

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. Derate linearly to 125°C free-air temperature at the rate of 3 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TIL102			TIL103			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		I_C = 100 μA, I_E = 0, I_F = 0	35			35			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		I_C = 1 mA, I_B = 0, I_F = 0	35			35			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage		I_E = 100 μA, I_C = 0, I_F = 0	4			4			V
I_R	Input Diode Static Reverse Current		V_R = 2 V			100			100	μA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	V_{CE} = 5 V, I_B = 0, I_F = 10 mA	2.5	6		10	15		mA
		Photodiode Operation	V_{CB} = 5 V, I_E = 0, I_F = 10 mA		40			40		μA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	V_{CE} = 20 V, I_B = 0, I_F = 0		6	100		6	100	nA
			V_{CE} = 20 V, I_B = 0, I_F = 0, T_A = 100°C		4			4		μA
		Photodiode Operation	V_{CB} = 20 V, I_E = 0, I_F = 0		0.1			0.1		nA
h_{FE}	Transistor Static Forward Current Transfer Ratio		V_{CE} = 5 V, I_C = 10 mA, I_F = 0		300			500		
V_F	Input Diode Static Forward Voltage		I_F = 10 mA			1.3			1.3	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		I_C = 2.5 mA, I_B = 0, I_F = 20 mA			0.3				V
			I_C = 10 mA, I_B = 0, I_F = 20 mA						0.3	
r_{IO}	Input-to-Output Internal Resistance		V_{in-out} = ±1 kV, See Note 3	10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance		V_{in-out} = 0, f = 1 MHz, See Note 3		2.5			2.5		pF

NOTE 3: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

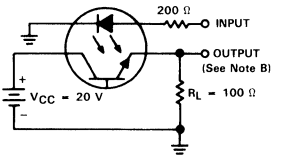
switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL102	TIL103	UNIT
				TYP	TYP	
t_r	Rise Time	Phototransistor Operation	V_{CC} = 20 V, I_B = 0, $I_{C(on)}$ = 5 mA, R_L = 100 Ω, See Test Circuit A of Figure 1	3	6	μs
t_f	Fall Time			3	6	
t_r	Rise Time	Photodiode Operation	V_{CC} = 20 V, I_E = 0, $I_{C(on)}$ = 50 μA, R_L = 100 Ω, See Test Circuit B of Figure 1	150	150	ns
t_f	Fall Time			150	150	

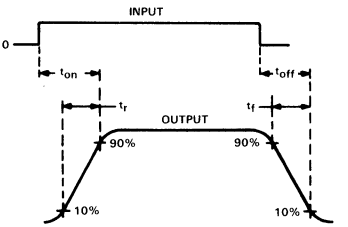
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

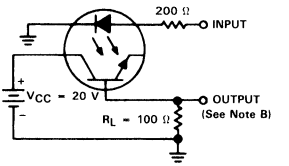
Adjust amplitude of input pulse for:
$I_{C(on)}$ = 5 mA (Test Circuit A) or
$I_{C(on)}$ = 50 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS



TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%. For Test Circuit A, t_w = 100 μs. For Test Circuit B, t_w = 1 μs.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL102
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

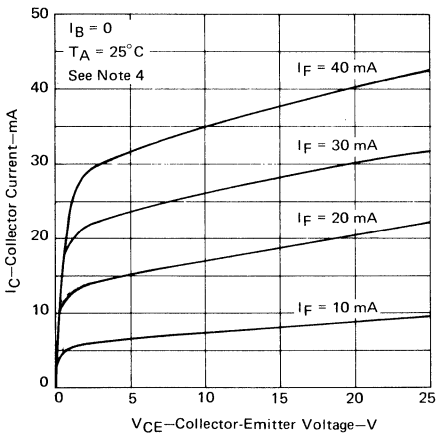


FIGURE 2

TIL103
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

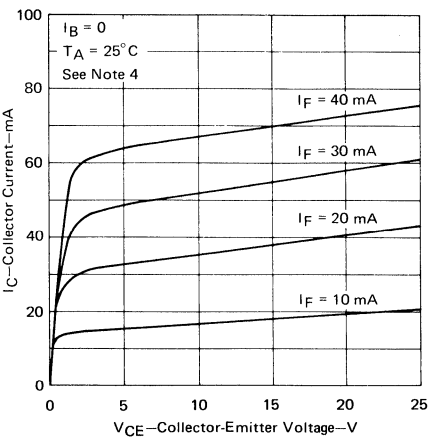


FIGURE 3

NOTE 4: This parameter was measured using pulse techniques. t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

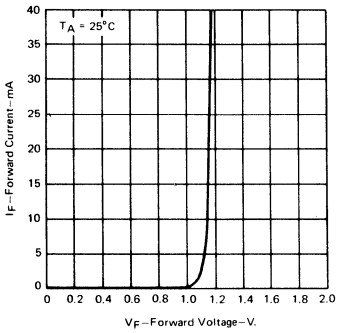
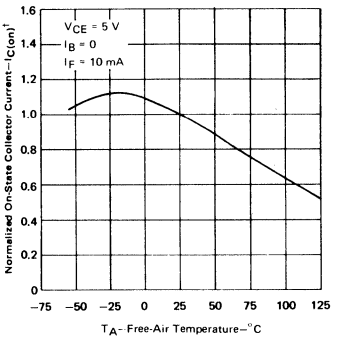


FIGURE 4

NORMALIZED ON-STATE COLLECTOR CURRENT†
vs
FREE-AIR TEMPERATURE



†Normalized to value at T_A = 25°C

FIGURE 5

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

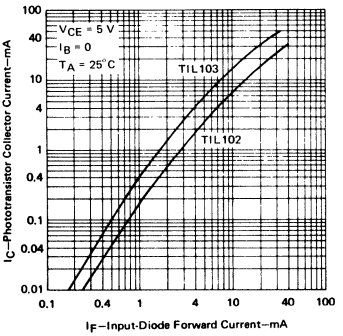


FIGURE 6

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

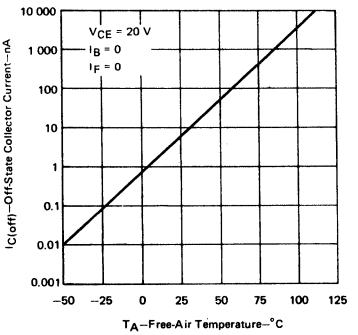


FIGURE 7

TIL102
AVERAGE SWITCHING TIME
vs
LOAD RESISTANCE

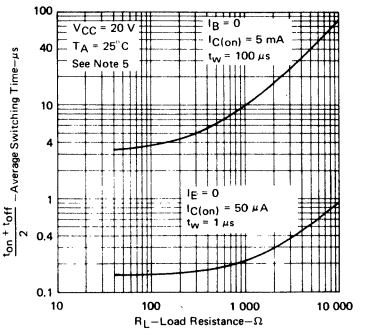


FIGURE 8

NOTE 5: These parameters were measured in Test Circuits A and B of Figure 1 with R_L varied between 40 Ω and 10 kΩ.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

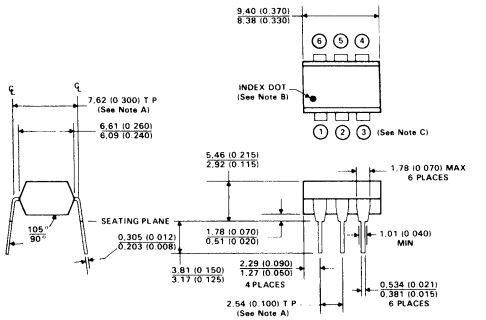
D1607, NOVEMBER 1973—REVISED FEBRUARY 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor
- High Direct-Current Transfer Ratio
- High-Voltage Electrical Isolation . . . 1.5-kV or 2.5-kV Rating
- Plastic Dual-In-Line Package
- High-Speed Switching: t_r = 5 μs, t_f = 5 μs Typical

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:

a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.
c. Terminal connections:

1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage: TIL111	±1.5 kV
TIL114, TIL116, TIL117	±2.5 kV
Collector-Base Voltage	70 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	100 mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 3)	150 mW
Phototransistor (See Note 4)	150 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 5)	250 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL111 TIL114			TIL116			TIL117			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		I_C = 10 μA, I_E = 0, I_F = 0	70			70			70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		I_C = 1 mA, I_B = 0, I_F = 0	30			30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage		I_E = 10 μA, I_C = 0, I_F = 0	7			7			7			V
I_R	Input Diode Static Reverse Current		V_R = 3 V			10			10			10	μA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	V_{CE} = 0.4 V, I_F = 16 mA, I_B = 0	2	7								mA
			V_{CE} = 10 V, I_F = 10 mA, I_B = 0				2	5		5	9		
		Photodiode Operation	V_{CB} = 0.4 V, I_F = 16 mA, I_E = 0	7	20		7	20		7	20		μA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_F = 0, I_B = 0		1	50		1	50		1	50	nA
		Photodiode Operation	V_{CB} = 10 V, I_F = 0, I_E = 0		0.1	20		0.1	20		0.1	20	
h_{FE}	Transistor Static Forward Current Transfer Ratio		V_{CE} = 5 V, I_C = 10 mA, I_F = 0	100	300					200	550		
			V_{CE} = 5 V, I_C = 100 μA, I_F = 0				100	300					
V_F	Input Diode Static Forward Voltage		I_F = 16 mA		1.2	1.4					1.2	1.4	V
			I_F = 60 mA					1.25	1.5				
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		I_C = 2 mA, I_F = 16 mA, I_B = 0		0.25	0.4							V
			I_C = 2.2 mA, I_F = 15 mA, I_B = 0					0.25	0.4				
			I_C = 0.5 mA, I_F = 10 mA, I_B = 0								0.25	0.4	
r_{IO}	Input-to-Output Internal Resistance		V_{in-out} = ±1.5 kV for TIL111, ±2.5 kV for all others, See Note 6	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance		V_{in-out} = 0, f = 1 MHz, See Note 6		1	1.3		1	1.3		1	1.3	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL111 TIL114			TIL116			TIL117			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	Phototransistor Operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5	10		5	10		5	10	μs
t_f	Fall Time				5	10		5	10		5	10	
t_r	Rise Time	Photodiode Operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1			1			1		μs
t_f	Fall Time				1			1			1		

TEXAS INSTRUMENTS
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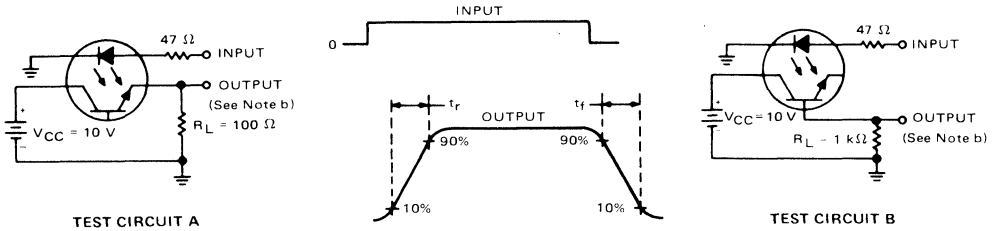
PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, t_r ≤ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL111, TIL114

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

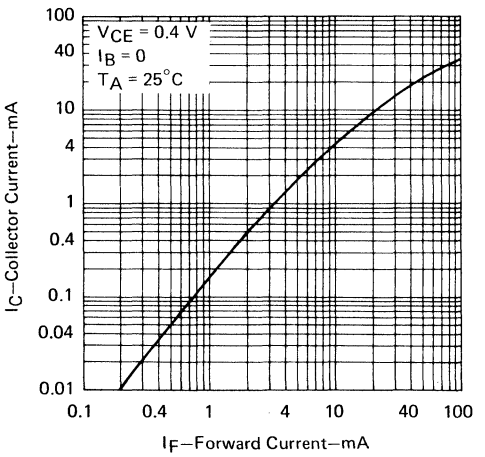


FIGURE 2

TIL116, TIL117

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

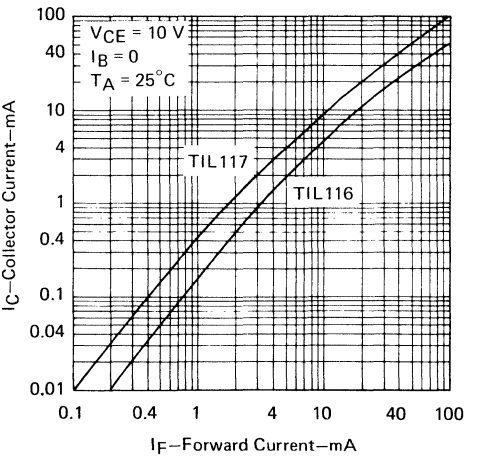


FIGURE 3

TYPICAL CHARACTERISTICS

TIL111, TIL114

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

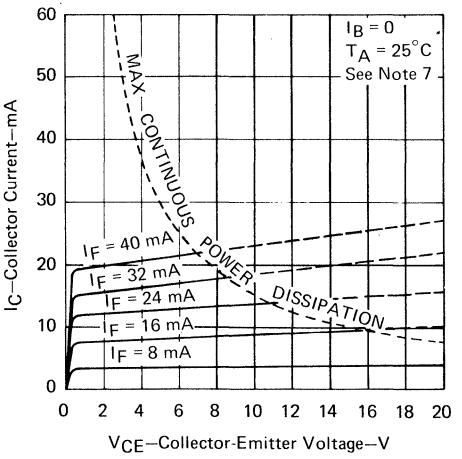


FIGURE 4

TIL116

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

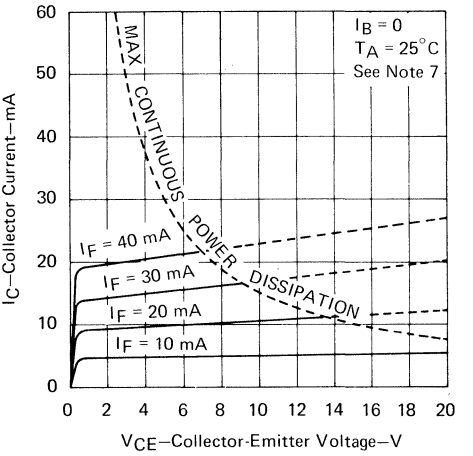


FIGURE 5

TIL117

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

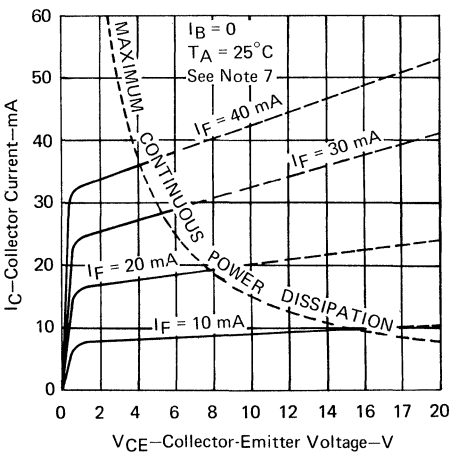


FIGURE 6

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

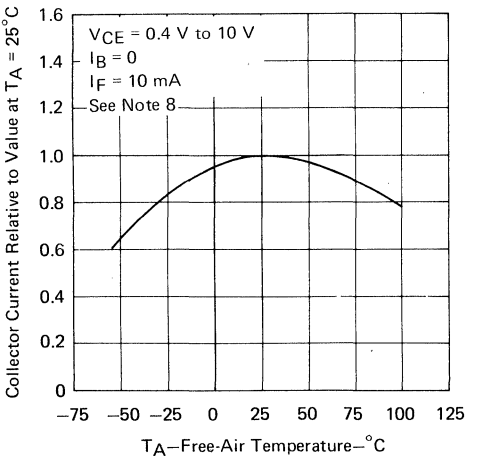


FIGURE 7

NOTES: 7. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
8. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

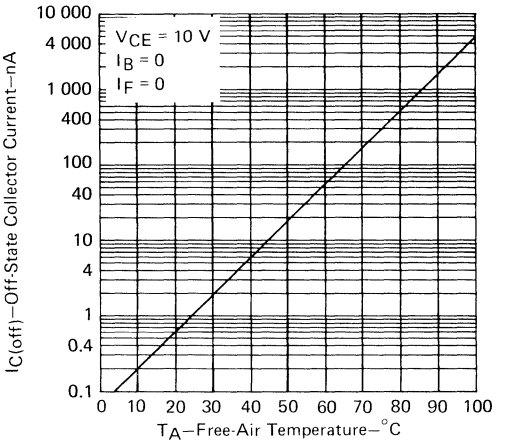


FIGURE 8

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
ON-STATE COLLECTOR CURRENT

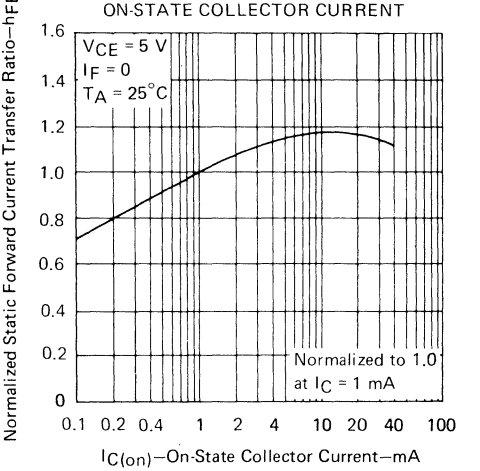


FIGURE 9

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

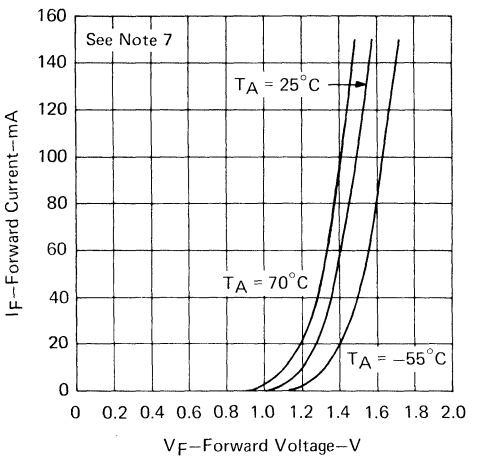


FIGURE 10

COLLECTOR CURRENT
vs
MODULATION FREQUENCY

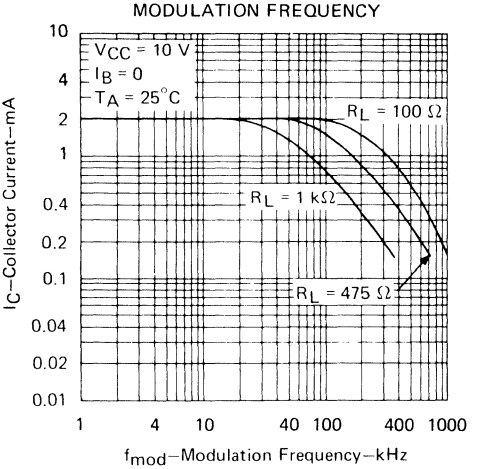


FIGURE 11

NOTE 7: These parameters were measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 2%

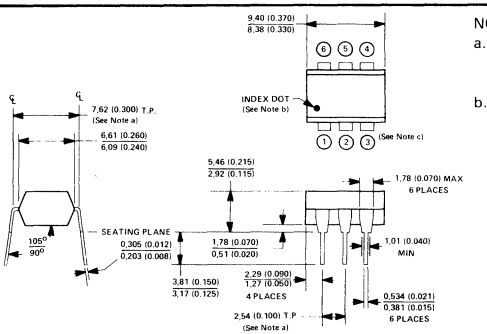
Optocouplers (Isolators)

D1499, AUGUST 1981 – REVISED JUNE 1989

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Darlington-Connected Phototransistor**
- **High Direct-Current Transfer Ratio . . . 300% Minimum at 10 mA**
- **High-Voltage Electrical Isolation . . . 1500-Volt Rating**
- **Plastic Dual-In-Line Package**
- **Base Lead Provided on TIL113 for Conventional Transistor Biasing**
- **No Base Lead Connection on TIL119A for High-EMI Environments**
- **Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays, and Pulse Transformers**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon darlington-connected phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.

Terminal connections:
1. Anode
2. Cathode
3. No internal connection

} Infrared-emitting diode

4. Emitter
5. Collector
6. TIL113 base
   TIL119A no internal connection

} Photo-transistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±1.5 kV
Collector-Base Voltage (TIL113)	30 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage (TIL113)	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	100 mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 3)	150 mW
Phototransistor (See Note 4)	150 mW
Total (Infrared-Emitting Diode plus Phototransistor, See Note 5)	250 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

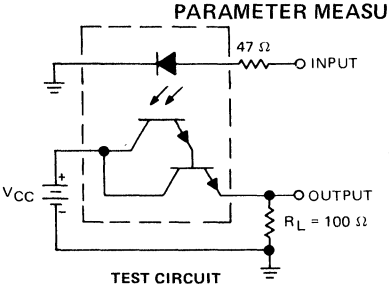
PARAMETER		TEST CONDITIONS†			TIL113			TIL119A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA,	I_E = 0,	I_F = 0	30						V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA,	I_B = 0,	I_F = 0	30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA,	I_C = 0,	I_F = 0	7						V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 10 μA,	I_F = 0					7			V
$I_{C(on)}$	On-State Collector Current	V_{CE} = 1 V,	I_B = 0,	I_F = 10 mA	30	100					mA
		V_{CE} = 1 V,	I_F = 10 mA					30	160		
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 10 V,	I_B = 0,	I_F = 0			100			100	nA
h_{FE}	Transistor Static Forward Current Transfer Ratio	V_{CE} = 1 V,	I_C = 10 mA,	I_F = 0		15,000					
V_F	Input Diode Static Forward Voltage	I_F = 10 mA					1.5			1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 125 mA,	I_B = 0,	I_F = 50 mA			1.2				V
		I_C = 30 mA,	I_F = 10 mA							1	
r_{IO}	Input-to-Output Internal Resistance	V_{in-out} = ±1.5 kV,	See Note 6		10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0,	f = 1 MHz,	See Note 6		1	1.3		1	1.3	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.
†Reference to the base are not applicable to TIL119A.

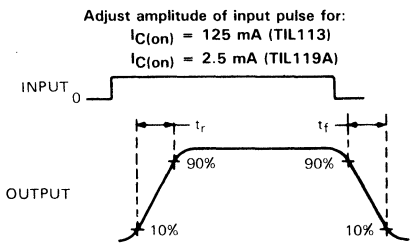
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		TL113			TIL119A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 15 V,	$I_{C(on)}$ = 125 mA,		300					μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1		300					
t_r	Rise Time	V_{CC} = 10 V,	$I_{C(on)}$ = 2.5 mA,					300		μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1					300		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 500 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

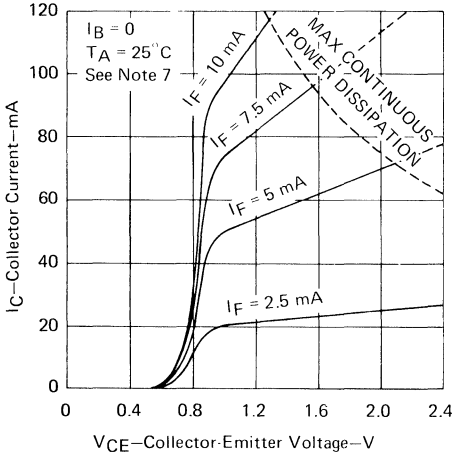


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

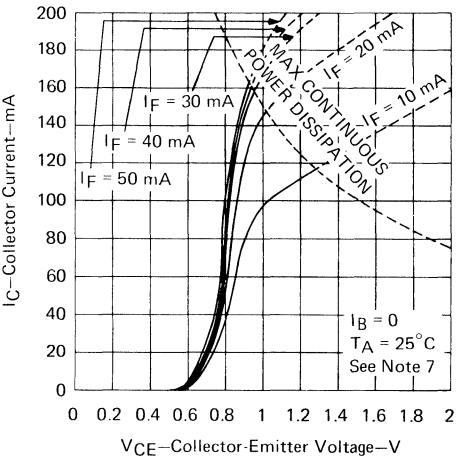


FIGURE 3

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

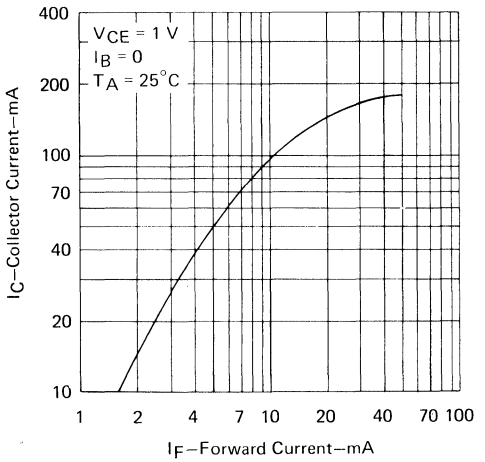


FIGURE 4

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

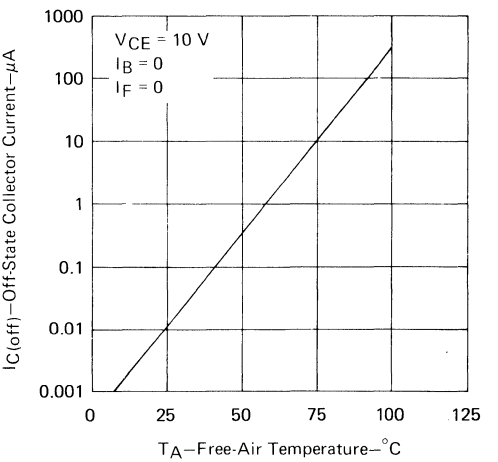


FIGURE 5

NOTE 7: Pulse operation of input diode is required for operation beyond limits shown by dotted line.

TYPICAL CHARACTERISTICS

RELATIVE COLLECTOR-EMITTER SATURATION VOLTAGE VS FREE-AIR TEMPERATURE

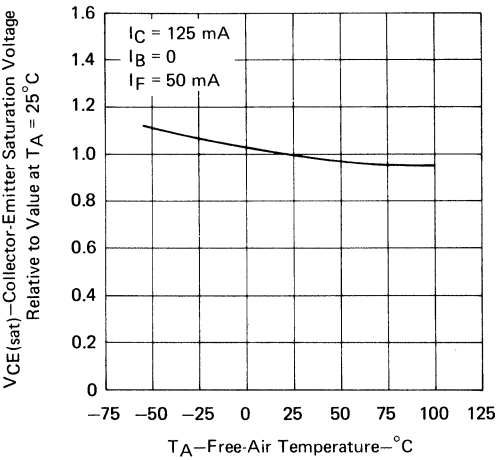


FIGURE 6

TIL113

TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO VS COLLECTOR CURRENT

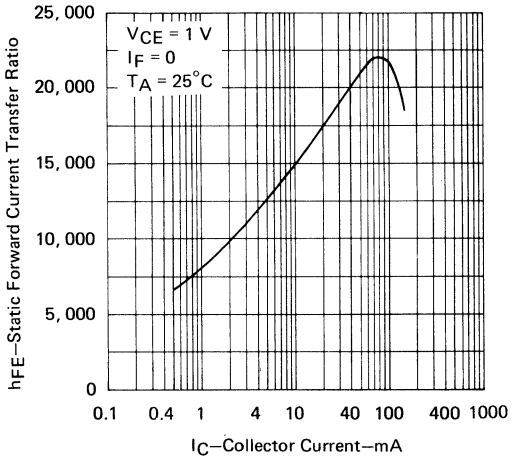


FIGURE 7

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

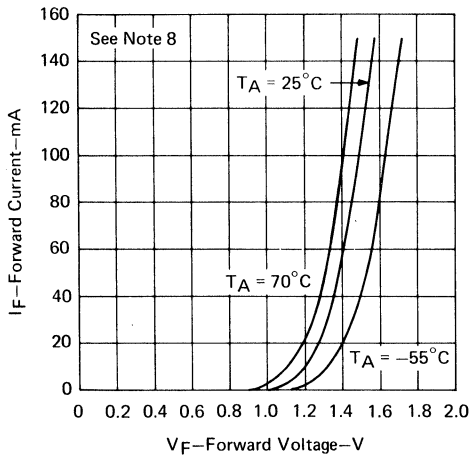


FIGURE 8

NOTE 8: This parameter was measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

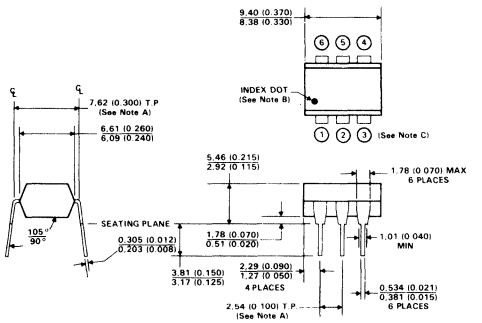
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

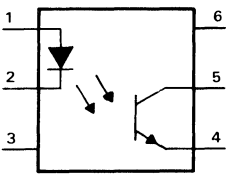
D1607, NOVEMBER 1973—REVISED JULY 1989

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 3.53 kV**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 2 μs, t_f = 2 μs Typical**
- **Choice of Three Current Transfer Ratios**
- **No Base Lead Connection for High EMI Environment**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.





NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

B. Pin 1 identified by index dot.

Terminal connections:

1. Anode	Infrared-emitting diode
2. Cathode	
3. No internal connection	
4. Emitter	Phototransistor
5. Collector	
6. Base	

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage . . . . . ±3.535 kV peak or dc (±2.5 kV rms)
Collector-emitter voltage (see Note 1) . . . . . 30 V
Emitter-collector voltage . . . . . 7 V
Input diode reverse voltage . . . . . 3 V
Input diode continuous forward current at (or below)
25°C free-air temperature (see Note 2) . . . . . 100 mA
Continuous power dissipation at (or below) 25°C free-air temperature:
Infrared-emitting diode (see Note 3) . . . . . 150 mW
Phototransistor (see Note 3) . . . . . 150 mW
Total, infrared-emitting diode plus phototransistor, (see Note 4) . . . . . 250 mW
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. This value applies when the base-emitter diode is open circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage			I_C = 1 mA, I_B = 0, I_F = 0	30			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage			I_E = 10 μA, I_F = 0	7			V
$I_{C(on)}$	On-state collector current	Photo-transistor operation	TIL118-1	V_{CE} = 5 V, I_F = 10 mA, I_B = 0	2			mA
			TIL118-2		5			
			TIL118-3		10			
$I_{C(off)}$	Off-state collector current	Phototransistor operation		V_{CE} = 5 V, I_F = 0, I_B = 0		1	100	nA
V_F	Input diode static forward voltage			I_F = 10 mA		1.2	1.5	V
$V_{CE(sat)}$	Collector-emitter saturation voltage			I_C = 2 mA, I_F = 10 mA, I_B = 0			0.4	V
r_{IO}	Input-to-output internal resistance			V_{in-out} = ±500 V, See Note 5	10^{11}			Ω
C_{io}	Input-to-output capacitance			V_{in-out} = 0, f = 1 MHz, See Note 5		1	2	pF

NOTE 5: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Figure 1		2	15	μs
t_f	Fall time				2	15	

TEXAS INSTRUMENTS
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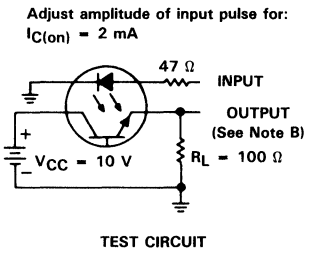
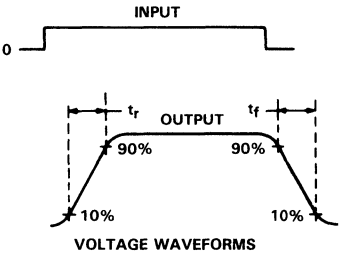
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, t_r ≤ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

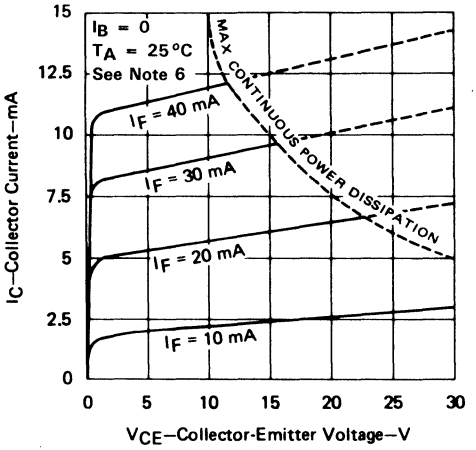


FIGURE 2

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

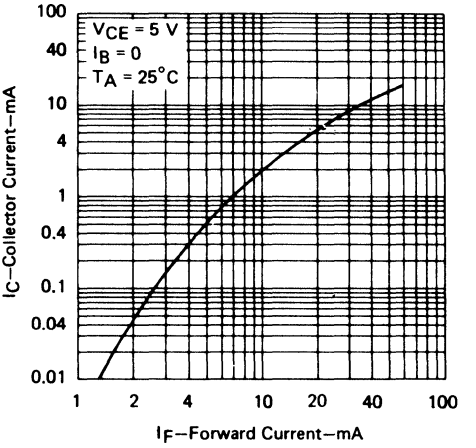


FIGURE 3

NOTE 6: Pulse operation of input diode is required for operation beyond limits shown by dotted lines.

TYPICAL CHARACTERISTICS

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

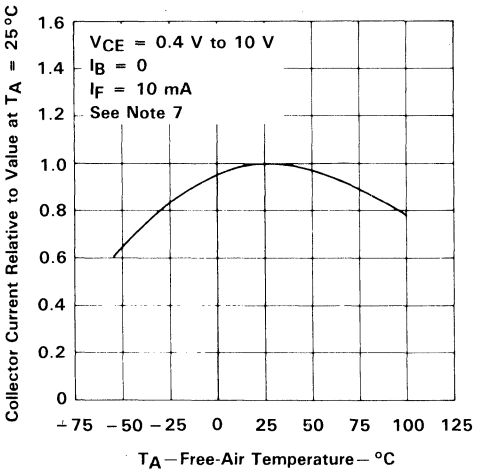


FIGURE 4

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

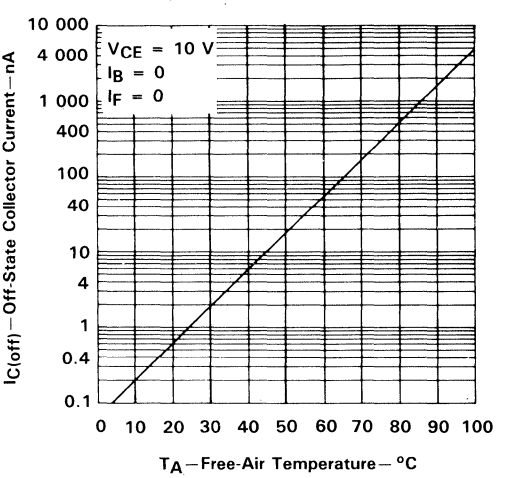


FIGURE 5

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

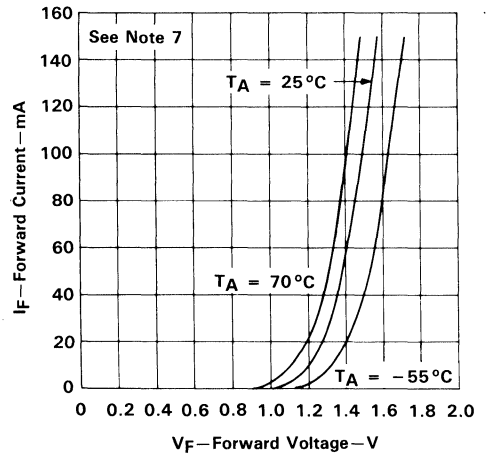


FIGURE 6

COLLECTOR CURRENT
vs
MODULATION FREQUENCY

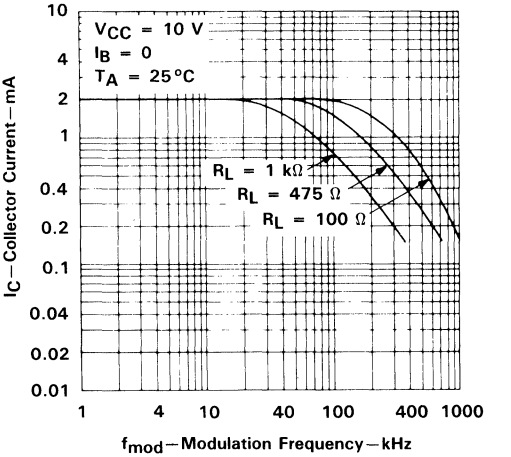


FIGURE 7

NOTE 7: These parameters were measured using techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

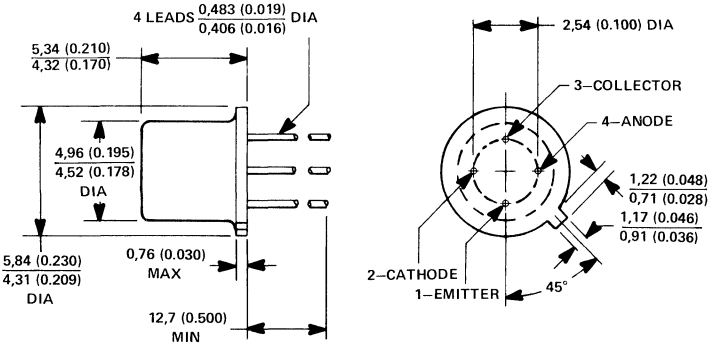
D1956, NOVEMBER 1974

GALLIUM ARSENIDE DIODE INFRARED SOURCE OPTICALLY COUPLED TO A HIGH-GAIN N-P-N SILICON PHOTOTRANSISTOR

- Photon Coupling for Isolator Applications
- High Overall Current Gain . . . 1.0 Typ (TIL121)
- High-Gain, High-Voltage Transistor . . . $V_{(BR)CEO}$ = 35 V Min
- High-Voltage Electrical Isolation . . . 1-kV Rating
- Stable Over Wide Temperature Range

mechanical data

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.
ALL JEDEC TO-72 DIMENSIONS AND NOTES ARE APPLICABLE

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±1 kV
Collector-Emitter Voltage	35 V
Emitter-Collector Voltage	7 V
Input Diode Reverse Voltage	3 V
Input Diode Continuous Forward Current at (or below) 65°C Free-Air Temperature (See Note 1)	40 mA
Continuous Collector Current	50 mA
Continuous Transistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	190 mW
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	240°C

NOTES: 1. Derate linearly to 125°C free-air temperature at the rate of 0.67 mA/°C.
2. Derate linearly to 125°C free-air temperature at the rate of 1.9 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TIL120			TIL121			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_F = 0	35			35			V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 100 μA, I_F = 0	7			7			V
I_R	Input Diode Static Reverse Current	V_R = 3 V			100			100	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 5 V, I_F = 10 mA	2.5	6		5	10		mA
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 20 V, I_F = 0		6	100		6	100	nA
		V_{CE} = 20 V, I_F = 0, T_A = 100°C		4			4		μA
V_F	Input Diode Static Forward Voltage	I_F = 10 mA			1.3			1.3	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 2.5 mA, I_F = 20 mA			0.3				V
		I_C = 10 mA, I_F = 20 mA						0.3	
r_{io}	Input-to-Output Internal Resistance	V_{in-out} = ±1 kV, See Note 3	10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, f = 1 MHz, See Note 3		2.5			2.5		pF

NOTE 3: These parameters are measured between both input diode leads shorted together and both phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TIL120			TIL121			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 20 V, $I_{C(on)}$ = 5 mA		3	20		6	20	μs
t_f	Fall Time	R_L = 100 Ω, See Figure 1		3	20		6	20	

TEXAS INSTRUMENTS
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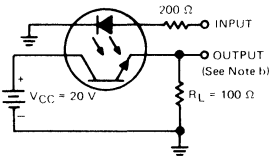
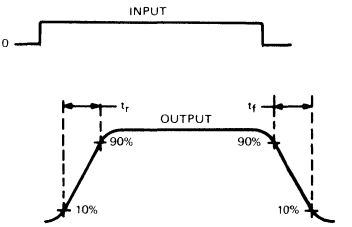
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

Adjust amplitude of input pulse for
$I_{C(on)}$ = 5 mA



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL120
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

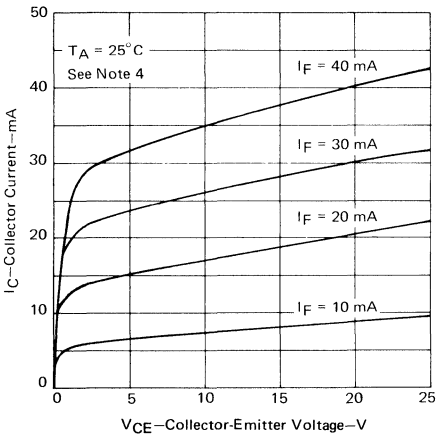


FIGURE 2

TIL121
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

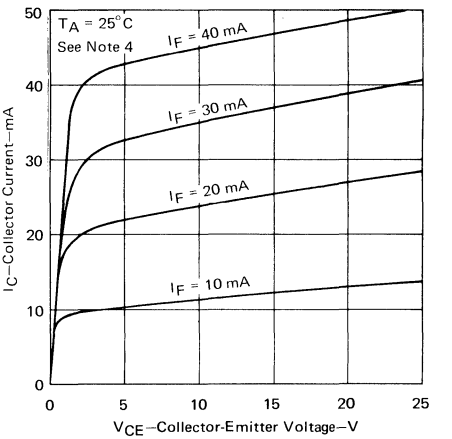


FIGURE 3

NOTE 4: This parameter was measured using pulse techniques. t_w = 100 μs, duty cycle = 1%.

TYPICAL CHARACTERISTICS

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

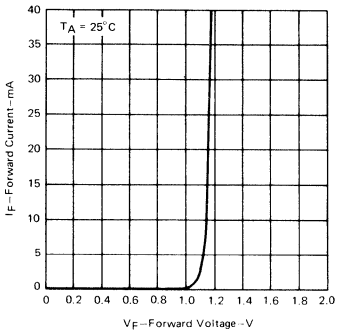


FIGURE 4

NORMALIZED ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

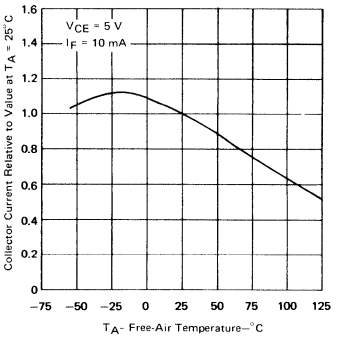


FIGURE 5

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

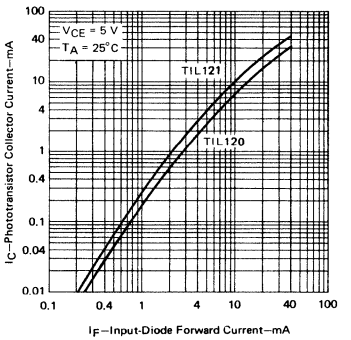


FIGURE 6

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

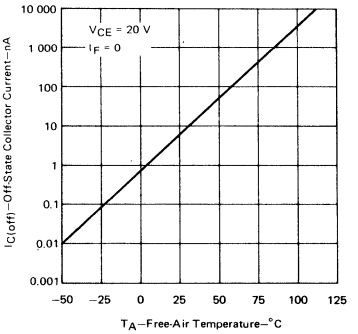


FIGURE 7

TIL120
AVERAGE SWITCHING TIME
vs
LOAD RESISTANCE

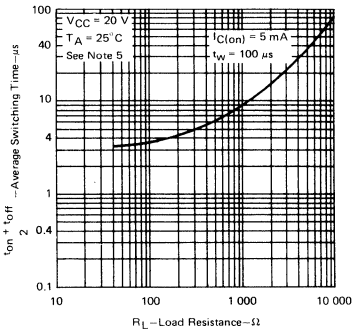


FIGURE 8

NOTE 5: These parameters were measured in the test circuit of Figure 1 with R_L varied between 40 Ω and 10 kΩ.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

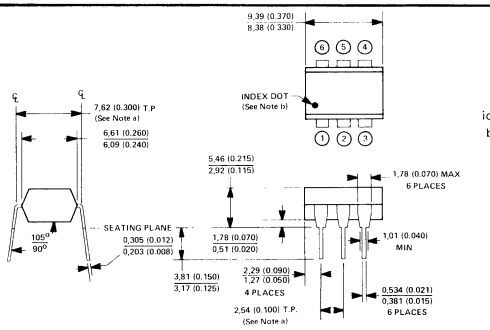
D2227, MAY 1977–REVISED DECEMBER 1982

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor
- High Direct-Current Transfer Ratio
- High-Voltage Electrical Isolation . . . 5000-V Rating
- Plastic Dual-In-Line Package
- High-Speed Switching: t_r = 2 μs, t_f = 2 μs Typical
- Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays, and Pulse Transformers

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



ion Leads are within 0,13 mm (0.005 inch) radius of
b. true position (T.P.) with maximum material condition and unit installed.
Pin 1 identified by index dot.
Terminal connections:

1. Anode
2. Cathode
3. No internal connection

Infrared-emitting diode

4. Emitter
5. Collector
6. Base

Phototransistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±5 kV
Collector-Base Voltage	70 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current	100 mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 2)	150 mW
Phototransistor (See Note 3)	150 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 4)	250 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL124			TIL125			TIL126			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		I_C = 10 μA, I_E = 0, I_F = 0	70			70			70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		I_C = 1 mA, I_B = 0, I_F = 0	30			30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage		I_E = 10 μA, I_C = 0, I_F = 0	7			7			7			V
I_R	Input Diode Static Reverse Current		V_R = 3 V			10			10			10	μA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_F = 10 mA, I_B = 0	1	3		2	5		5	9		mA
		Photodiode Operation	V_{CB} = 10 V, I_F = 10 mA, I_E = 0	5	20		5	20		5	20		μA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_F = 0 I_B = 0		1	50		1	50		1	50	nA
		Photodiode Operation	V_{CB} = 10 V, I_F = 0, I_E = 0		0.1	20		0.1	20		0.1	20	
h_{FE}	Transistor Static Forward Current Transfer Ratio		V_{CE} = 5 V, I_C = 10 mA, I_F = 0	50	100		100	200		100	550		
V_F	Input Diode Static Forward Voltage		I_F = 10 mA		1.2	1.4		1.2	1.4		1.2	1.4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		I_C = 1 mA, I_F = 10 mA, I_B = 0		0.25	0.4		0.25	0.4		0.25	0.4	V
r_{io}	Input-to-Output Internal Resistance		V_{in-out} = 500 V, See Note 5	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance		V_{in-out} = 0, f = 1 MHz, See Note 5		1	1.3		1	1.3		1	1.3	pF

NOTE 5: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise Time	Phototransistor Operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5	10	μs
t_f	Fall Time				5	10	
t_r	Rise Time	Photodiode Operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall Time				1		

TEXAS INSTRUMENTS
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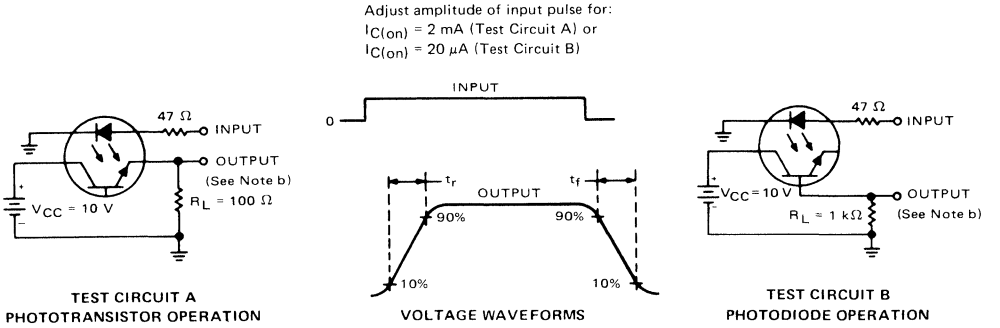
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

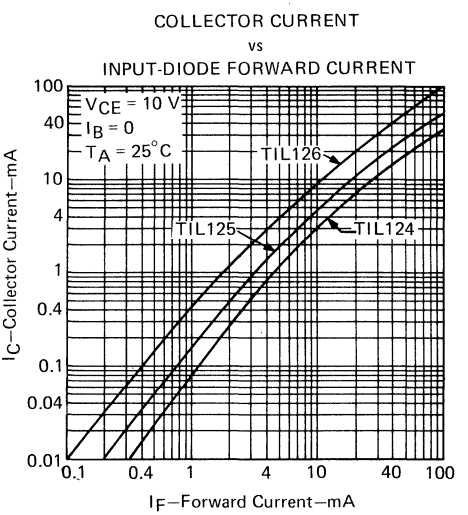


FIGURE 2

TYPICAL CHARACTERISTICS

TIL124

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

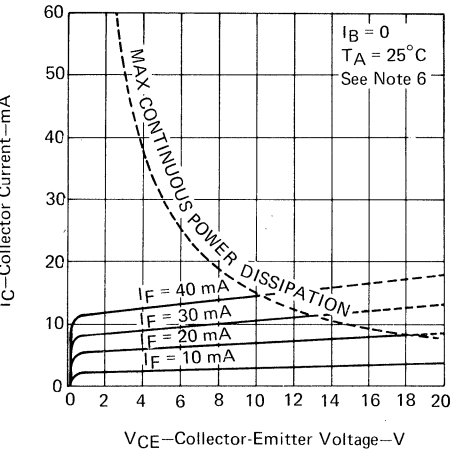


FIGURE 3

TIL125

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

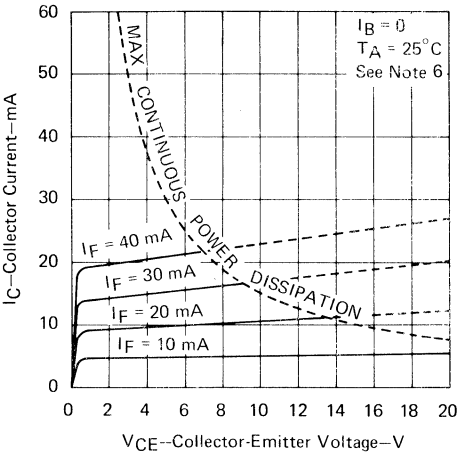


FIGURE 4

TIL126

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

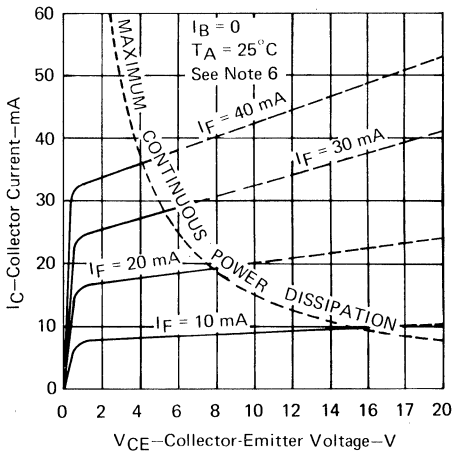


FIGURE 5

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

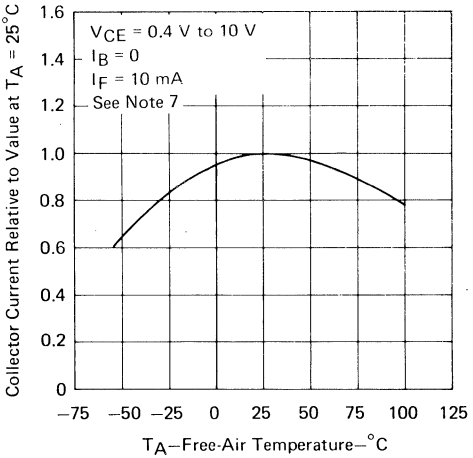


FIGURE 6

NOTES: 6. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
7. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

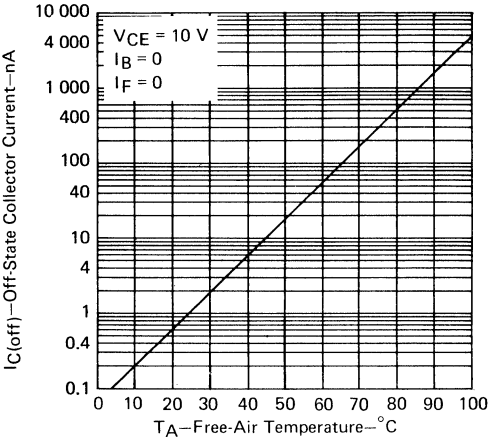


FIGURE 7

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
ON-STATE COLLECTOR CURRENT

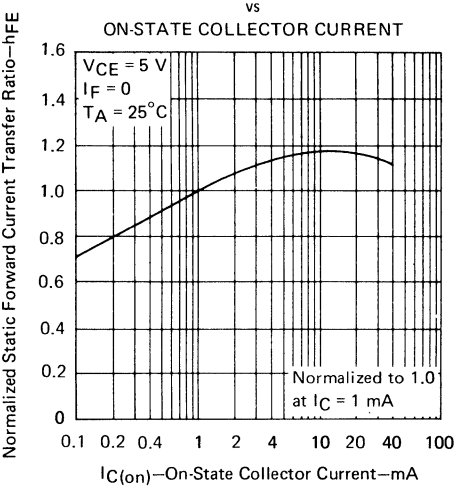


FIGURE 8

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

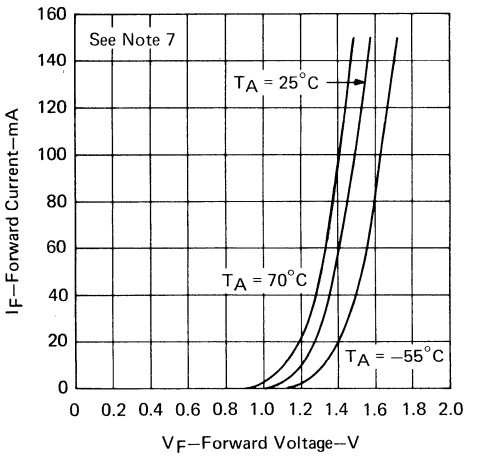


FIGURE 9

COLLECTOR CURRENT
vs
MODULATION FREQUENCY

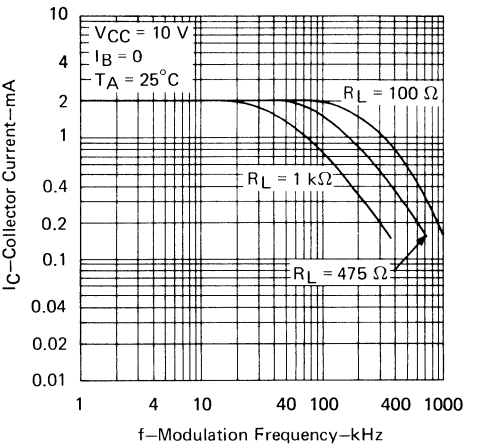


FIGURE 10

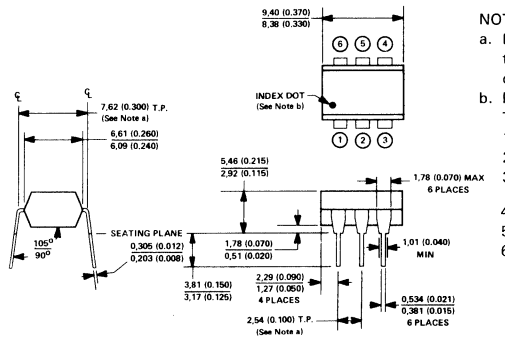
NOTE 7: These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ⩽ 2%.

D2328, MAY 1977—REVISED JUNE 1989

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Darlington-Connected Phototransistor**
- **High Direct-Current Transfer Ratio . . . 300% Minimum at 10 mA**
- **High-Voltage Electrical Isolation . . . 5000-Volt Rating**
- **Plastic Dual-In-Line Package**
- **Typical Applications Include Remote Terminal Isolation, SCR and Triac Triggers, Mechanical Relays, and Pulse Transformers**
- **No Base Connection on TIL128A for Environments with High Electromagnetic Interference**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation,and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.

Terminal connections:
1. Anode
2. Cathode
3. No internal connection

} Infrared-emitting diode

4. Emitter
5. Collector
6. TIL127: Base
   TIL128A: No internal connection

} Photo-transistor

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.
FALLS WITHIN JEDEC MO-001AM DIMENSIONS

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output Voltage	±5 kV
Collector-Base Voltage (TIL127)	30 V
Collector-Emitter Voltage (See Note 1)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage (TIL127)	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current	100 mA
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 2)	150 mW
Phototransistor (See Note 3)	150 mW
Total (Infrared-Emitting Diode plus Phototransistor, See Note 4)	250 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 10 Seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

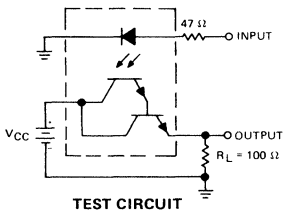
PARAMETER		TEST CONDITIONS†			TIL127			TIL128A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA,	I_E = 0,	I_F = 0	30						V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA,	I_B = 0,	I_F = 0	30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA,	I_C = 0,	I_F = 0	7						V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 10 μA,	I_F = 0					7			V
I_R	Input Diode Static Reverse Current	V_R = 3 V					10			10	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 1 V,	I_B = 0,	I_F = 10 mA	30	100					mA
		V_{CE} = 1 V,	I_F = 10 mA					30	160		
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 10 V,	I_B = 0,	I_F = 0			100			100	nA
h_{FE}	Transistor Static Forward Current Transfer Ratio	V_{CE} = 1 V,	I_C 10 mA,	I_F = 0		15 000					
V_F	Input Diode Static Forward Voltage	I_F = 10 mA					1.5			1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C 125 mA,	I_B = 0,	I_F = 50 mA			1.2				V
		I_C = 30 mA,	I_F = 10 mA							1	
r_{IO}	Input-to-Output Internal Resistance	V_{in-out} = 500 V,	See Note 5		10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0,	f = 1 MHz,	See Note 5		1	1.3		1	1.3	pF

NOTE 5: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.
†References to the base are not applicable to the TIL128A.

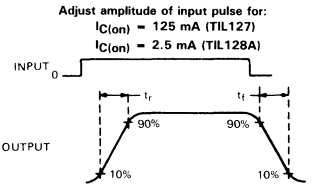
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†		TIL127			TIL128A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 15 V,	$I_{C(on)}$ = 125 mA,		300					μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1		300					
t_r	Rise Time	V_{CC} = 10 V,	$I_{C(on)}$ = 2.5 mA,					300		μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1					300		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 500 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

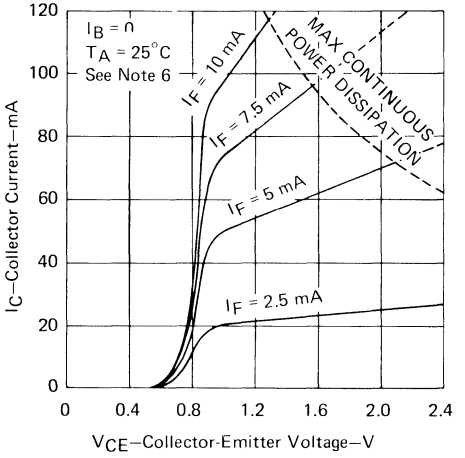


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

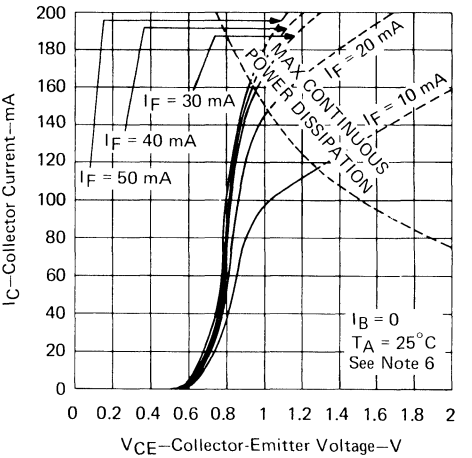


FIGURE 3

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

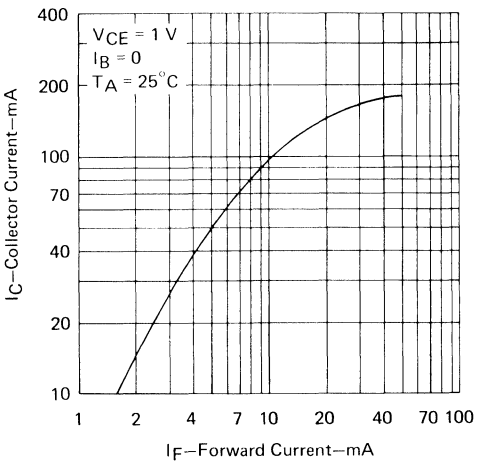


FIGURE 4

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

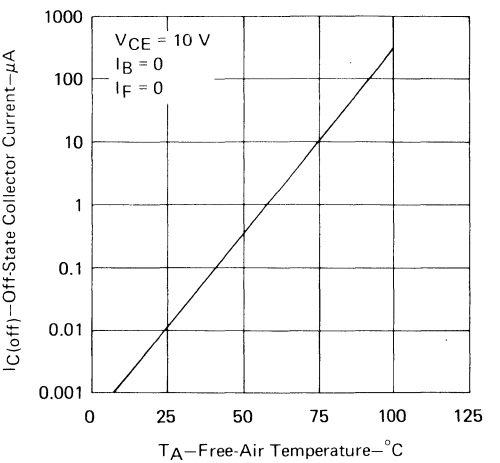


FIGURE 5

NOTE 6: Pulse operation of input diode is required for operation beyond limits shown by dotted line.

TYPICAL CHARACTERISTICS

RELATIVE COLLECTOR-EMITTER SATURATION VOLTAGE VS FREE-AIR TEMPERATURE

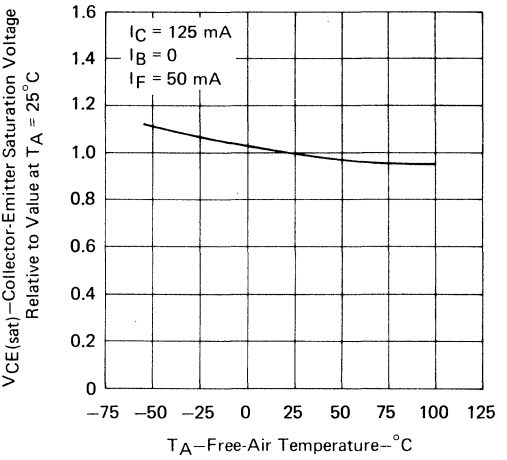


FIGURE 6

TIL127

TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO VS COLLECTOR CURRENT

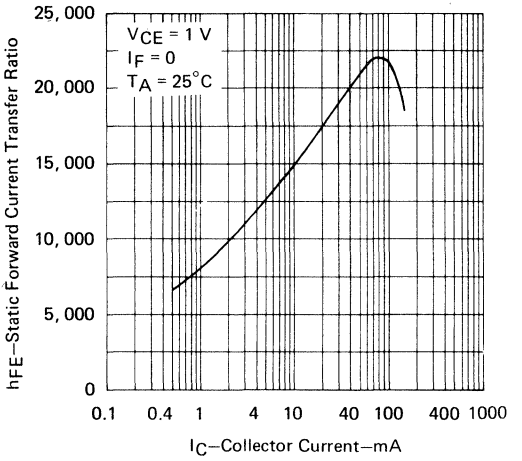


FIGURE 7

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

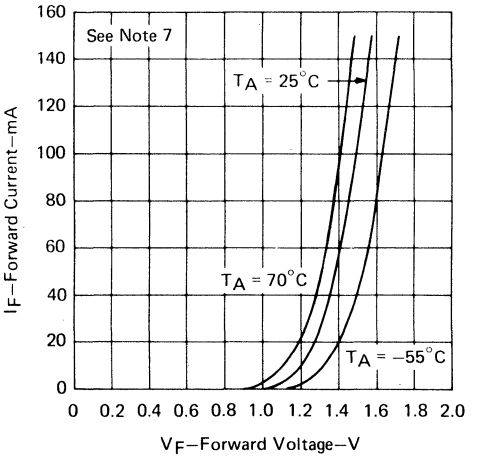


FIGURE 8

NOTE 7: This parameter was measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

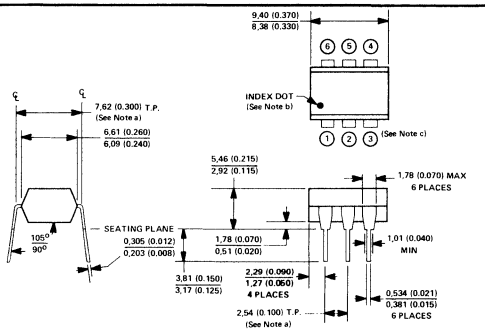
D2491, SEPTEMBER–REVISED DECEMBER 1982

UL LISTED – FILE # E65085

- GaAs-Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor
- Direct-Current Transfer Ratio . . . 10% to 50%
- Plug-In Replacements for TIL111 Series
- High-Voltage Electrical Isolation . . . 2500 V RMS (3535 V Peak)

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:

a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

b. Pin 1 identified by index dot.

Terminal connections:

1. Anode
2. Cathode

} Infrared-emitting diode

3. No internal connection
4. Emitter
5. Collector
6. Base

} Phototransistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output RMS Voltage (See Note 1)	2500 V
Collector-Base Voltage	70 V
Collector-Emitter Voltage (See Note 2)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 3)	100 mA
Continuous Phototransistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	150 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

NOTES: 1. This rating applies for sine-wave operation at 50 or 60 Hz. Service capability is verified by testing in accordance with UL requirements.

2. This value applies when the base-emitter diode is open-circuited.
3. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	TIL153			TIL154			TIL155			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage		I_C = 10 μA, I_E = 0, I_F = 0	70			70			70			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage		I_C = 1 mA, I_B = 0, I_F = 0	30			30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage		I_E = 10 μA, I_C = 0, I_F = 0	7			7			7			V
I_R	Input Diode Static Reverse Current		V_R = 3 V			10			10			10	μA
$I_{C(on)}$	On-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_F = 10 mA, I_B = 0	1	3		2	5		5	9		mA
		Photodiode Operation	V_{CB} = 10 V, I_F = 10 mA, I_E = 0		10			10			10		μA
$I_{C(off)}$	Off-State Collector Current	Phototransistor Operation	V_{CE} = 10 V, I_F = 0, I_B = 0		1	50		1	50		1	50	nA
		Photodiode Operation	V_{CB} = 10 V, I_F = 0, I_E = 0		0.1	20		0.1	20		0.1	20	
h_{FE}	Transistor Static Forward Current Transfer Ratio		V_{CE} = 5 V, I_C = 10 mA, I_F = 0	50	100		100	200		100	550		
V_F	Input Diode Static Forward Voltage		I_F = 10 mA		1.2	1.4		1.2	1.4		1.2	1.4	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage		I_C = 1 mA, I_F = 10 mA, I_B = 0		0.25	0.4		0.25	0.4		0.25	0.4	V
r_{IO}	Input-to-Output Internal Resistance		V_{in-out} = 500 V, See Note 5	10^{11}			10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance		V_{in-out} = 0, f = 1 MHz, See Note 5		1	1.3		1	1.3		1	1.3	pF

NOTE 5: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together.

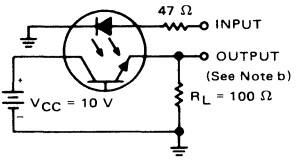
switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r Rise Time	Phototransistor Operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		5	10	μs
t_f Fall Time				5	10	
t_r Rise Time	Photodiode Operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f Fall Time				1		

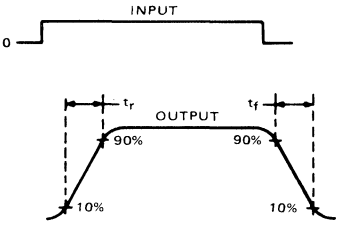
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

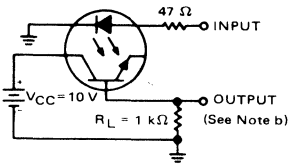
Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS



TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

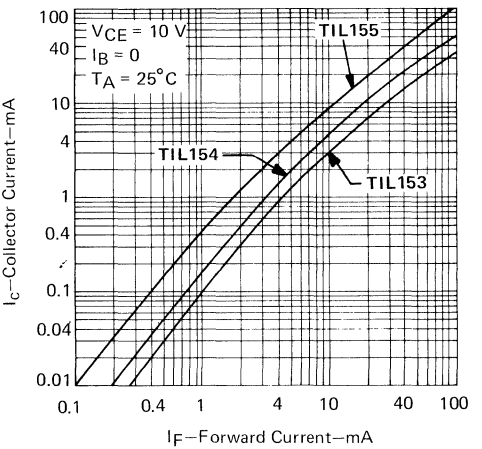


FIGURE 2

TYPICAL CHARACTERISTICS

TIL153

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

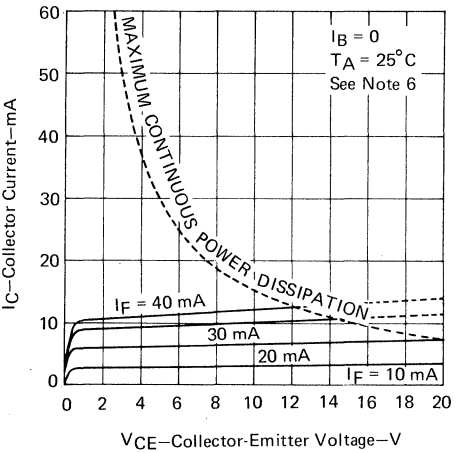


FIGURE 3

TIL154

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

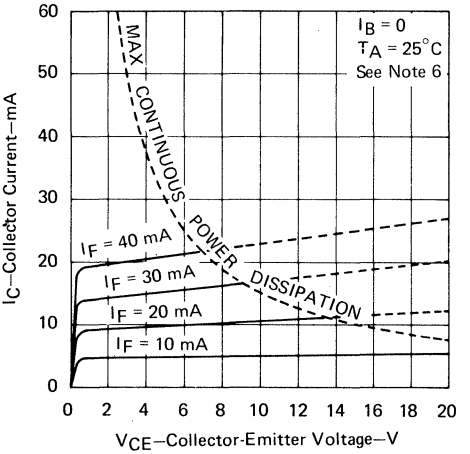


FIGURE 4

TIL155

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

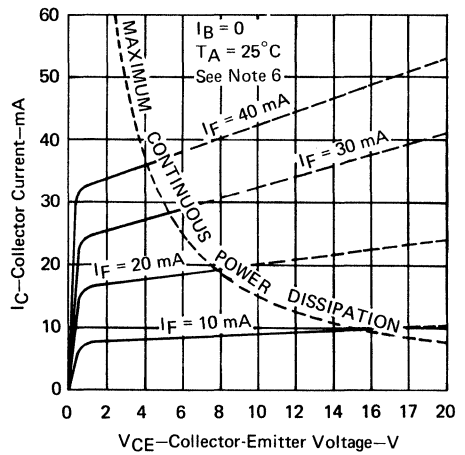


FIGURE 5

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

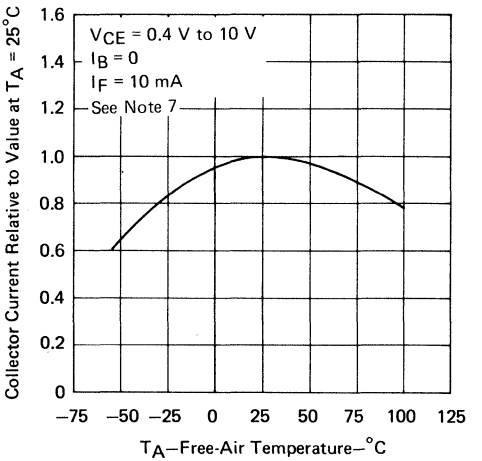


FIGURE 6

NOTES: 6. Pulse operation of input diode is required for operation beyond limits shown by dotted lines.
7. These parameters were measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

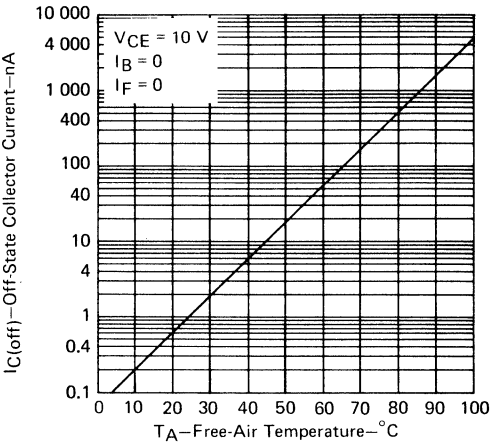


FIGURE 7

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
ON-STATE COLLECTOR CURRENT

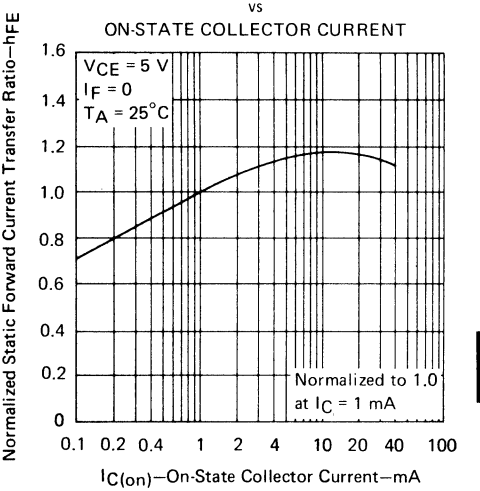


FIGURE 8

INPUT DIODE FORWARD
CONDUCTION CHARACTERISTICS

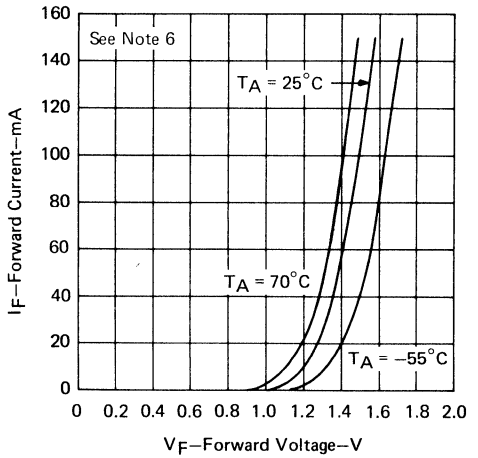


FIGURE 9

COLLECTOR CURRENT
vs
MODULATION FREQUENCY

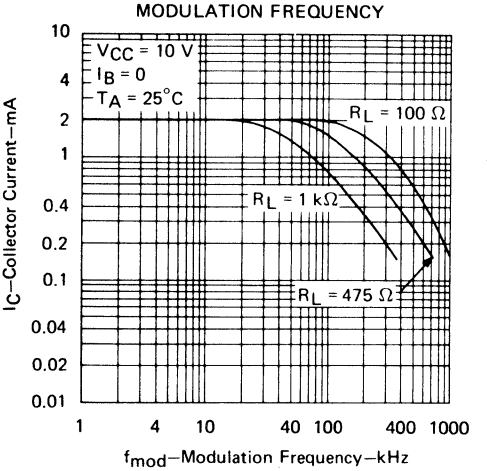


FIGURE 10

NOTE 6: These parameters were measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 2%

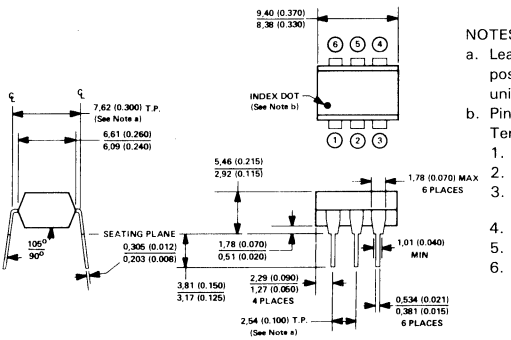
D2492, SEPTEMBER 1978—REVISED JUNE 1989

UL LISTED — FILE #E65085

- **GaAs-Diode Light Source Optically Coupled to a Silicon N-P-N Darlington-Connected Phototransistor**
- **High Direct-Current Transfer Ratio . . . 300% Minimum at 10 mA**
- **Plug-In Replacement for TIL113 and TIL119A**
- **High-Voltage Electrical Isolation . . . 2500 V RMS (3535 V Peak)**
- **No Base Connection on TIL157A for Environments with High Electromagnetic Interference**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon darlington-connected phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.

Terminal connections:
1. Anode
2. Cathode
3. No internal connection
4. Emitter
5. Collector
6. TIL156 base
   TIL157A no internal connection

Infrared-emitting diode

Photo-transistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-Output RMS Voltage (See Note 1)	2500 V
Collector-Base Voltage (TIL156)	30 V
Collector-Emitter Voltage (See Note 2)	30 V
Emitter-Collector Voltage	7 V
Emitter-Base Voltage (TIL156)	7 V
Input-Diode Reverse Voltage	3 V
Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 3)	100 mA
Continuous Phototransistor Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	150 mW
Storage Temperature Range	−55°C to 150°C
Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

NOTES: 1. This rating applies for sine-wave operation at 50 or 60 Hz. Service capability is verified by testing in accordance with UL requirements.
2. This value applies when the base-emitter diode is open-circuited.
3. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.

electrical characteristics at 25°C free-air temperature

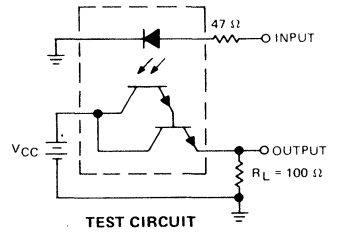
PARAMETER		TEST CONDITIONS†			TIL156			TIL157A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA,	I_E = 0,	I_F = 0	30						V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA,	I_B = 0,	I_F = 0	30			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA,	I_C = 0,	I_F = 0	7						V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 10 μA,	I_F = 0					7			V
I_R	Input Diode Static Reverse Current	V_R = 3 V					10			10	μA
$I_{C(on)}$	On-State Collector Current	V_{CE} = 1 V,	I_B = 0,	I_F = 10 mA	30	100					mA
		V_{CE} = 1 V,	I_F = 10 mA					30	160		
$I_{C(off)}$	Off-State Collector Current	V_{CE} = 10 V,	I_B = 0,	I_F = 0			100			100	nA
h_{FE}	Transistor Static Forward Current Transfer Ratio	V_{CE} = 1 V,	I_C = 10 mA,	I_F = 0		15 000					
V_F	Input Diode Static Forward Voltage	I_F = 10 mA					1.5			1.5	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 125 mA,	I_B = 0,	I_F = 50 mA			1.2				V
		I_C = 30 mA,	I_F = 10 mA							1	
r_{IO}	Input-to-Output Internal Resistance	V_{in-out} = 500 V,	See Note 5		10^{11}			10^{11}			Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0,	f = 1 MHz,	See Note 5		1	1.3		1	1.3	pF

Note 5: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.
†References to the base are not applicable to the TIL157A.

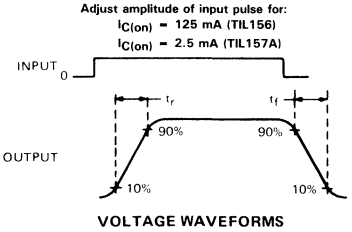
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†		TIL156			TIL157A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise Time	V_{CC} = 15 V,	$I_{C(on)}$ = 125 mA,		300					μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1		300					
t_r	Rise Time	V_{CC} = 10 V,	$I_{C(on)}$ = 2.5 mA,					300		μs
t_f	Fall Time	R_L = 100 Ω,	See Figure 1					300		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 500 μs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1–SWITCHING TIMES

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

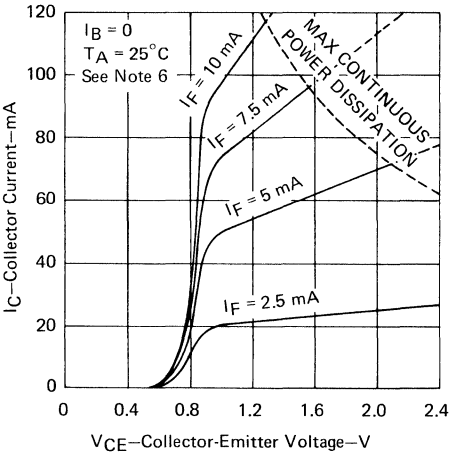

FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

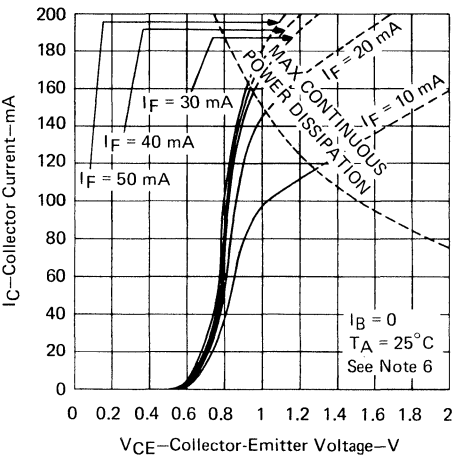

FIGURE 3

COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

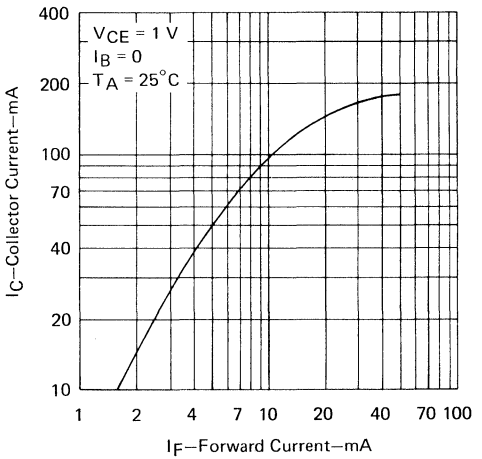

FIGURE 4

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

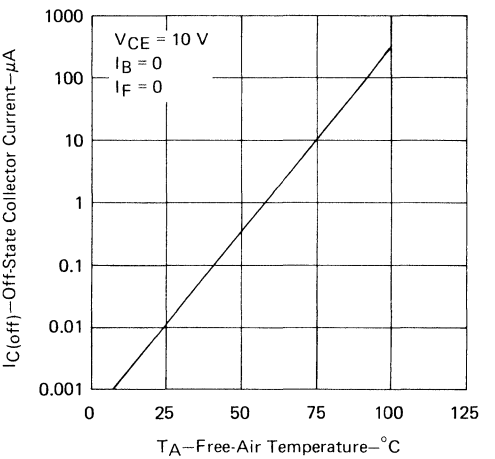

FIGURE 5

NOTE 6: Pulse operation of input diode is required for operation beyond limits shown by dotted line.

TYPICAL CHARACTERISTICS

RELATIVE COLLECTOR-EMITTER SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

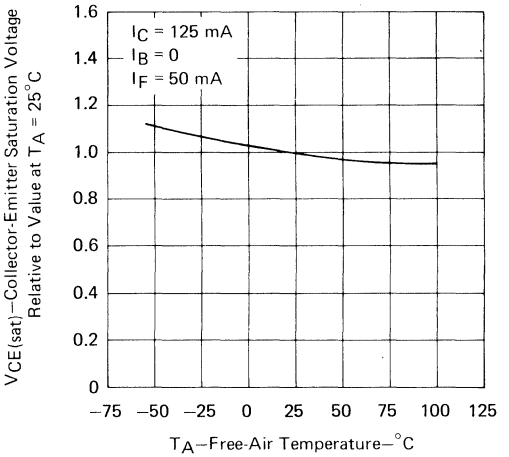

FIGURE 6

TIL156
TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT

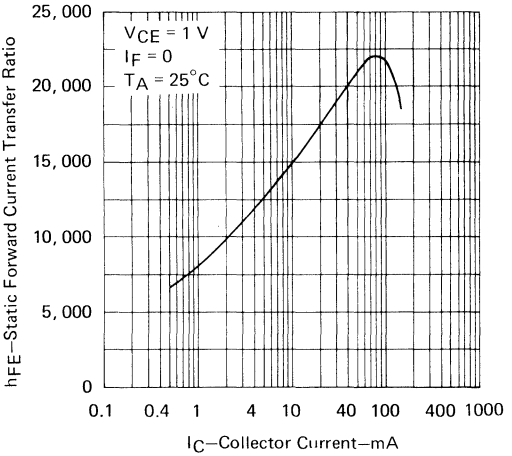

FIGURE 7

INPUT DIODE FORWARD CONDUCTION CHARACTERISTICS

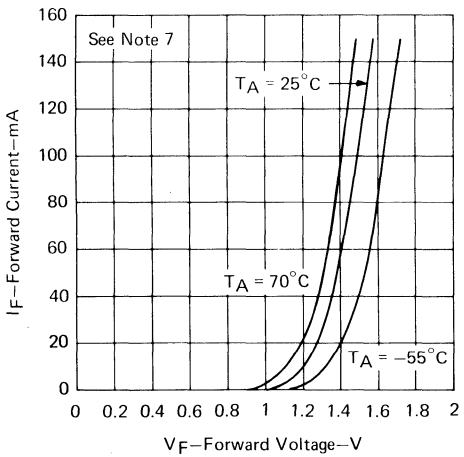

FIGURE 8

NOTE 7: This parameter was measured using pulse techniques. t_w = 1 ms, duty cycle ≤ 2%.

TEXAS INSTRUMENTS
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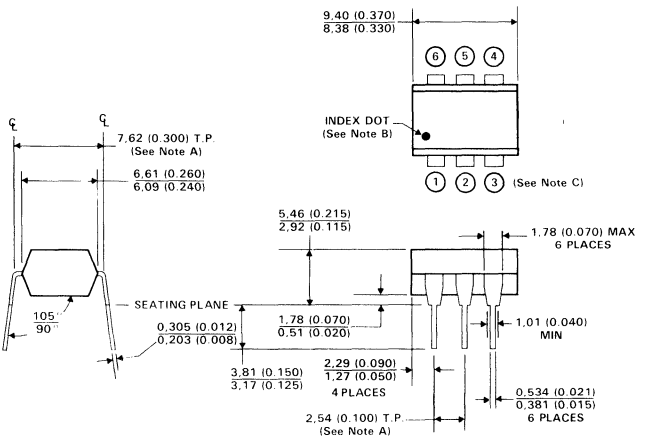
D2906, OCTOBER 1985—REVISED MARCH 1988

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 2.5 kV rms (3.535 kV peak)**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 2 μs Typ, t_f = 2 μs Typ**
- **UL Recognized — File #E65085**
- **Primarily Used with Telephone Ring Detector TCM1520A and Tone Drivers TCM1501B, TCM1506B, TCM1512B, TCM1531, TCM1532, TCM1536, and TCM1539**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode
2. Cathode
} Infrared-emitting diode
3. No internal connection
4. Emitter
5. Collector
6. Base
} Phototransistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage . . . . . ±2.5 kV rms (±3.535 kV peak)
Collector-base voltage . . . . . 70 V
Collector-emitter voltage (see Note 1) . . . . . 30 V
Emitter-collector voltage . . . . . 7 V
Emitter-base voltage . . . . . 7 V
Input-diode reverse voltage . . . . . 3 V
Input-diode continuous forward current at (or below) 25°C free-air temperature (see Note 2) . . . . . 100 mA
Continuous power dissipation at (or below) 25°C free-air temperature
Infrared-emitting diode (see Note 3) . . . . . 150 mW
Phototransistor (see Note 4) . . . . . 150 mW
Total, infrared-emitting diode plus phototransistor (see Note 5) . . . . . 250 mW
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA,	I_E = 0,	I_F = 0	70			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA,	I_B = 0,	I_F = 0	30			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA,	I_C = 0,	I_F = 0	7			V
I_R	Input diode static reverse current		V_R = 3 V					10	μA
$I_{C(on)}$	On-state collector current	Phototransistor operation	V_{CE} = 0.4 V,	I_F = 0.8 mA,	I_B = 0	100			μA
			V_{CE} = 0.4 V,	I_F = 10 mA,	I_B = 0	5			mA
		Photodiode operation	V_{CB} = 0.4 V,	I_F = 16 mA,	I_E = 0	7	20		μA
$I_{C(off)}$	Off-state collector current	Phototransistor operation	V_{CE} = 10 V,	I_F = 0,	I_B = 0		1	50	nA
		Photodiode operation	V_{CB} = 10 V,	I_F = 0,	I_E = 0		0.1	20	
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V,	I_C = 10 mA,	I_F = 0	200	550		
V_F	Input diode static forward voltage		I_F = 16 mA				1.2	1.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 5 mA,	I_F = 10 mA,	I_B = 0		0.25	0.4	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V,	See Note 6		10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0,	f = 1 MHz,	See Note 6		1	1.3	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

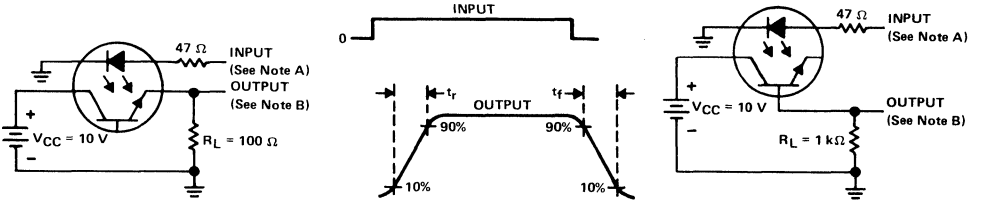
switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		2	10	μs
t_f	Fall time				2	10	
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall time				1		

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION

VOLTAGE WAVEFORMS

TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

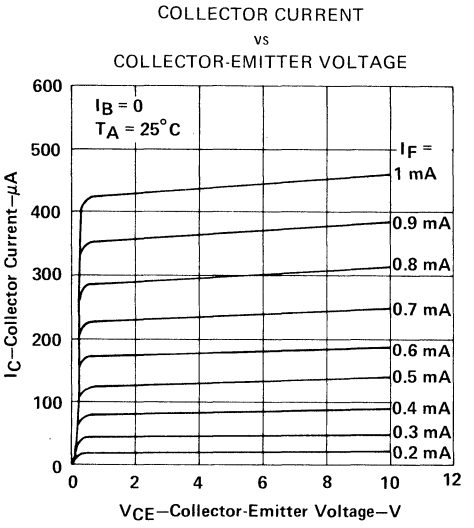


FIGURE 2

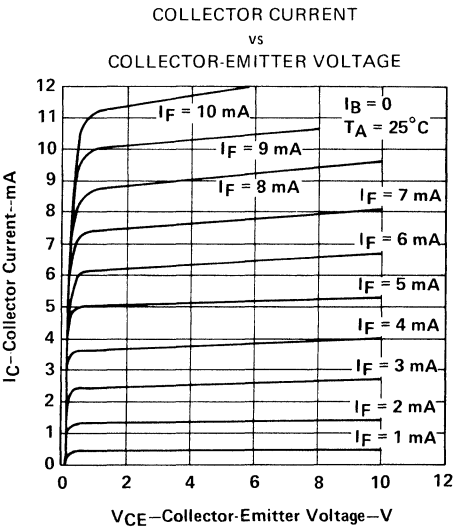


FIGURE 3

TYPICAL CHARACTERISTICS

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

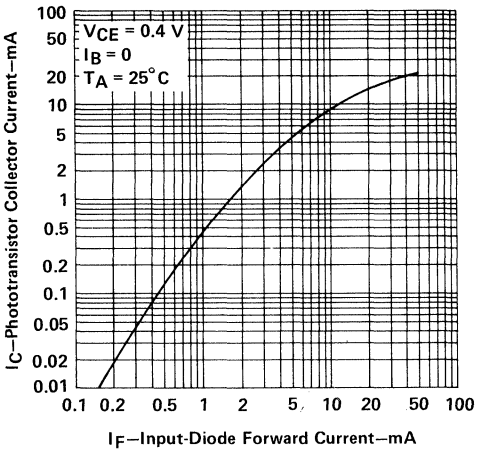


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

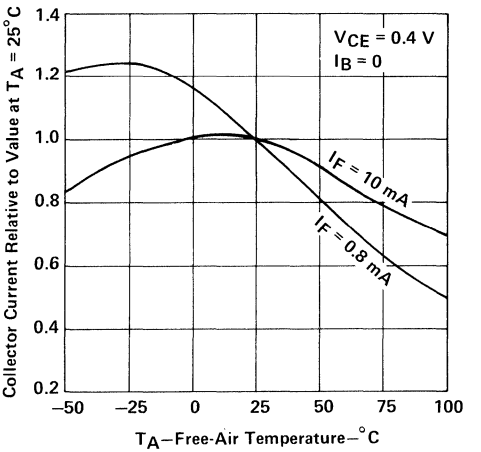


FIGURE 5

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

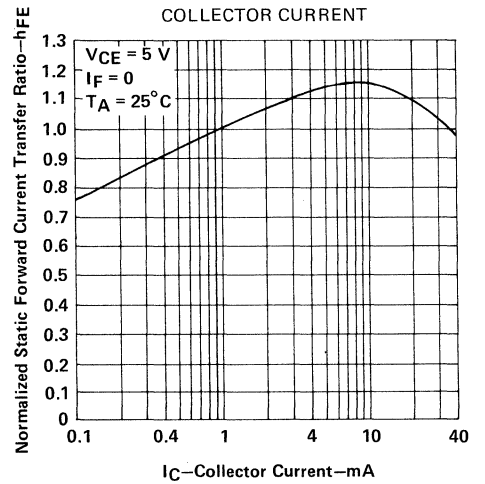


FIGURE 6

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

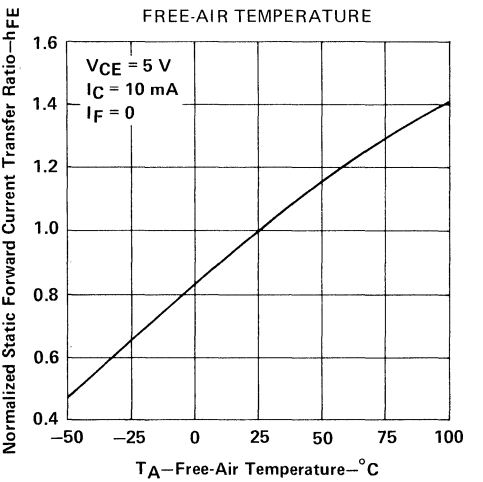


FIGURE 7

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2981, DECEMBER 1986—REVISED JUNE 1989

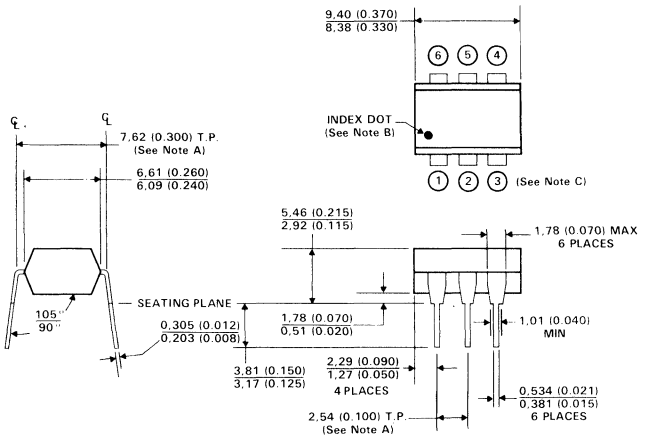
- **A-C Signal Input**
- **Gallium Arsenide Dual-Diode Infrared Sources Coupled to a Silicon NPN Photo-Transistor**
- **Plastic Dual-In-Line Package**
- **UL-Recognized — File # E65085**
- **Choice of Four Current Transfer Ratios**
- **High-Voltage Electrical Isolation 3.535 kV Peak (2.5 kV rms)**
- **High-Speed Switching . . . t_f = 4 μs Typ**

description

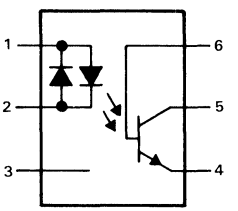
The TIL186 optocoupler is designed for use in ac input signal applications that require high-voltage isolation between input and output. Users can select from four different current gains (TIL186-1 through TIL186-4). These optocouplers consist of two GaAs light-emitting input diodes connected in a reverse-parallel configuration for ac input applications and a silicon npn output phototransistor.

mechanical data

The package is mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation. Device performance characteristics will remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage	±3.535 kV peak (±2.5 kV rms)
Collector-base voltage	100 V
Collector-emitter voltage (see Note 1)	55 V
Emitter-collector voltage	7 V
Emitter-base voltage	7 V
Input-diode continuous forward current at (or below) 25°C free-air temperature (see Note 2)	100 mA
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 3)	150 mW
Phototransistor (see Note 3)	150 mW
Infrared-emitting diode plus phototransistor (see Note 4)	250 mW
Storage temperature range	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA,	I_E = 0,	I_F = 0	100			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA,	I_B = 0,	I_F = 0	55			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA,	I_C = 0,	I_F = 0	7			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		I_E = 100 μA,	I_B = 0,	I_F = 0	7			V
$I_{C(on)}$†	On-state collector current	Phototransistor operation	V_{CE} = 10 V, I_B = 0	I_F = 2 mA,	TIL186-1	0.1			mA
					TIL186-2	0.2			
					TIL186-3	0.5			
					TIL186-4	1			
			V_{CE} = 10 V, I_B = 0	I_F = 10 mA,	TIL186-1	1			
					TIL186-2	2			
					TIL186-3	5			
					TIL186-4	10			
		Photodiode operation	V_{CB} = 10 V,	I_F = 10 mA,	I_E = 0	5	12		μA
$I_{C(off)}$	Off-state collector current		V_{CE} = 50 V,	I_F = 20 mA,	I_B = 0		2	200	nA
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V,	I_C = 10 mA,	I_F = 0	100	550		
V_F†	Input diode static forward voltage		I_F = 10 mA			1	1.16	1.5	V
$V_{CE(sat)}$†	Collector-emitter saturation voltage		I_C = 1 mA,	I_F = 10 mA,	I_B = 0		0.14	0.4	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V,	See Note 5		10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0,	f = 1 MHz,	See Note 5		1	2	pF
$\frac{I_{C(on)1}}{I_{C(on)2}}$	On-state collector current symmetry ratio (see Note 6)		V_{CE} = 10 V,	I_F = 10 mA,	I_E = 0	1		3	

†These parameters apply for either direction of the input current.

NOTES: 5. These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

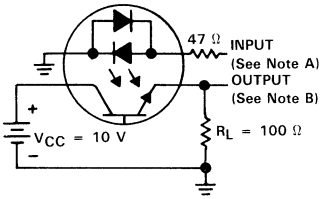
6. The higher of the two $I_{C(on)}$ values generated by the two diodes is taken as $I_{C(on)1}$.

switching characteristics at 25°C free-air temperature

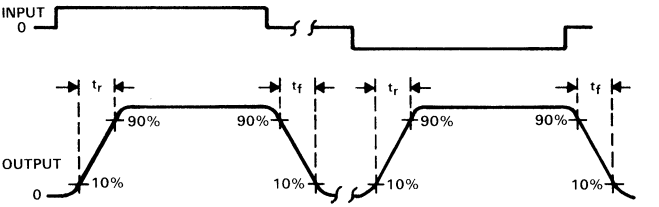
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Figure 1		4	10	μs
t_f	Fall time			4	10	μs

PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse is for $I_{C(on)}$ = 2 mA



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_r = ≤15 ns, duty cycle = 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_I ≥ 1 MΩ, C_I ≤ 20 pF.

FIGURE 1. SWITCHING TIMES

3

Optocouplers (Isolators)

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

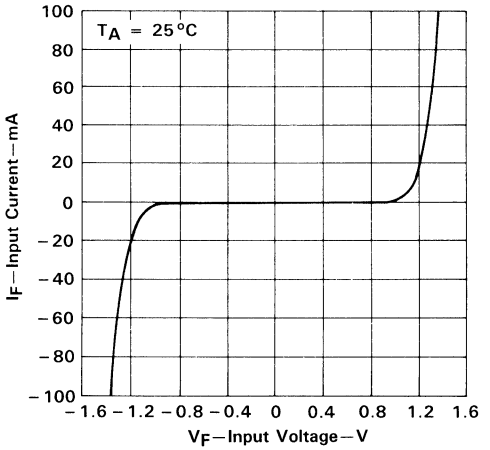


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

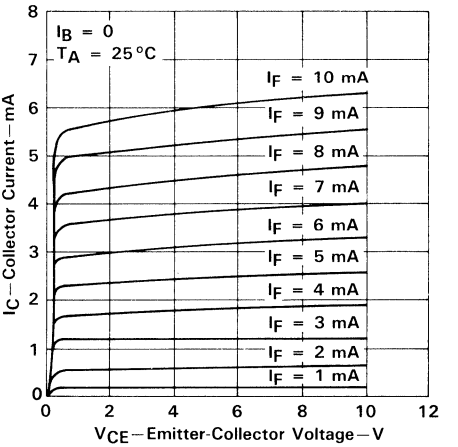


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

NORMALIZED ON-STATE COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

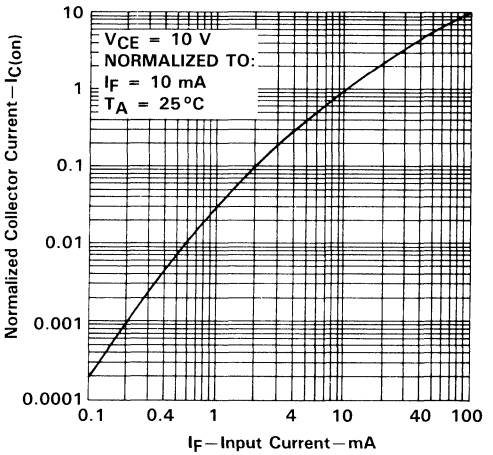


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

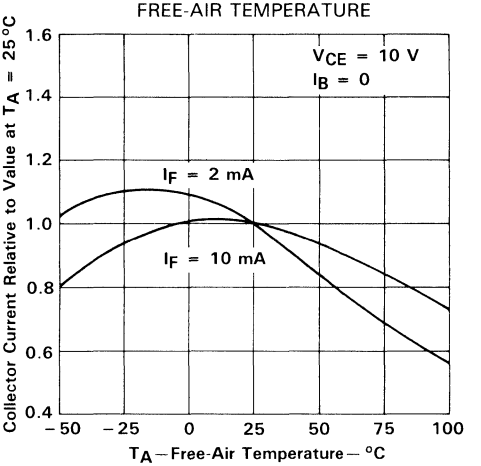


FIGURE 5

NORMALIZED TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

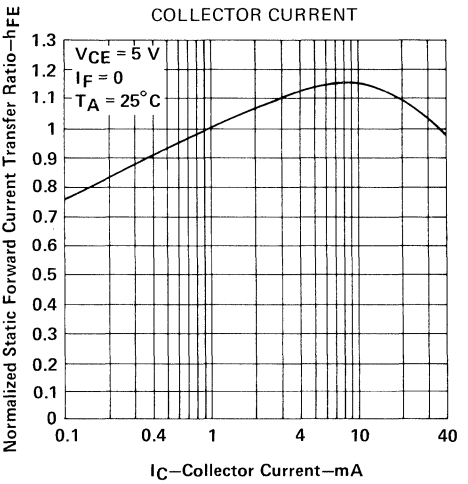


FIGURE 6

NORMALIZED TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

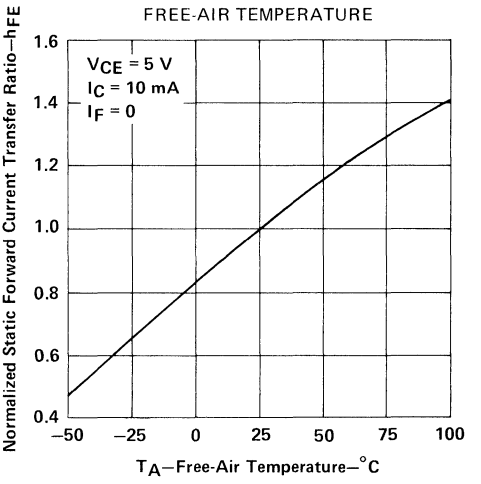


FIGURE 7

AC-INPUT OPTOCOUPLERS/OPTOISOLATORS

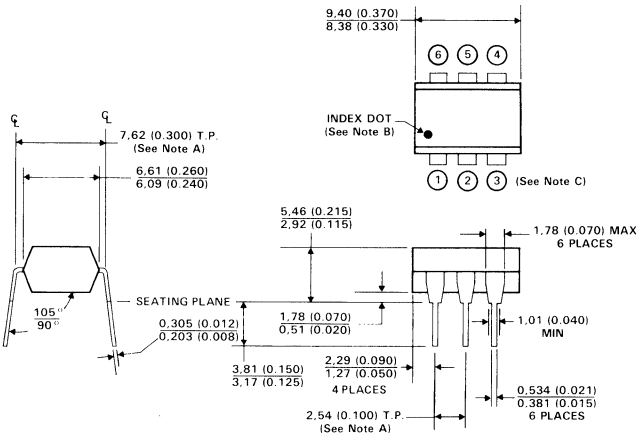
D2980, JANUARY 1987—REVISED JULY 1989

- AC Signal Input
- Gallium Arsenide Dual-Diode Infrared Source Optically Coupled to a Silicon N-P-N Darlington Phototransistor
- Plastic Dual-In-Line Package
- High-Voltage Electrical Isolation, 3.535 kV Peak (2.5 kV rms)
- High Current Transfer Ratio, 500% Minimum at I_F = 10 mA, Up to 1500% Minimum at I_F = 2 mA with Four Categories
- High $V_{(BR)CEO}$, 55 V Min
- UL Recognized — File #E65085
- No Base Lead Connection on TIL188 for High-EMI Environment

description

The TIL187 and TIL188 Optocouplers are designed for use in AC applications that require very high current transfer ratio and high voltage isolation between input and output. These optocouplers consist of two GaAs light-emitting diodes connected in a reverse-parallel configuration and a silicon n-p-n Darlington phototransistor. The TIL187 has the base connected for applications where a base signal or base resistor is required. The TIL188 is designed with no base connected for applications where high base-noise immunity is desired. Users can select from four different current gains (TIL187-1 through TIL187-4 and TIL188-1 through TIL188-4).

mechanical data



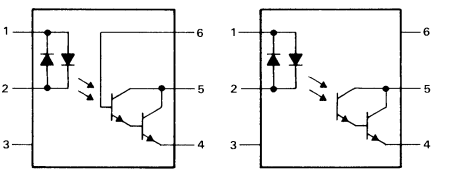
CP 7

NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.

B. Pin 1 identified by index dot.

C. Terminal connections:

1. Input
2. Input — Infrared-emitting diode
3. No internal connection
4. Emitter
5. Collector
6. TIL187: Base — Phototransistor
   TIL188: No internal connection



TIL187 TIL188

FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage	±3.535 kV peak or dc (±2.5 kV rms)
Collector-base voltage (TIL187)	100 V
Collector-emitter voltage (see Note 1)	55 V
Emitter-collector voltage	7 V
Emitter-base voltage (TIL187)	14 V
Input diode continuous forward current at (or below) 25°C free-air temperature (see Note 2)	100 mA
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 3)	150 mW
Phototransistor (see Note 3)	150 mW
Total, infrared-emitting diode plus phototransistor (see Note 4)	250 mW
Storage temperature range	−55°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TIL187			TIL188			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA, I_E = 0, I_F = 0	100						V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA, I_B = 0, I_F = 0	55			55			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA, I_C = 0, I_F = 0	14						V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		I_E = 10 μA, I_F = 0				7			V
$I_{C(on)}$ On-state collector current	Photo-transistor operation	TIL187-1, TIL188-1	V_{CE} = 1 V, I_F = 2 mA, I_B = 0	5			5			mA
		TIL187-2, TIL188-2		10			10			
		TIL187-3, TIL188-3		20			20			
		TIL187-4, TIL188-4		30			30			
			V_{CE} = 1 V, I_F = 10 mA, I_B = 0	50			50			
	Photodiode operation		V_{CB} = 1 V, I_F = 10 mA, I_E = 0		12					μA
$I_{C(off)}$	Off-state collector current		V_{CE} = 10 V, I_F = 0, I_B = 0			100			100	nA
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 1 V, I_C = 10 mA, I_F = 0		25000					
V_F†	Input diode static forward voltage		I_F = 10 mA	1	1.2	1.5	1	1.2	1.5	V
$V_{CE(sat)}$†	Collector-emitter saturation voltage		I_C = 50 mA, I_F = 10 mA, I_B = 0		0.87	1		0.87	1	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V, See Note 5	10^{11}			10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0, f = 1 mHz, See Note 5		1	1.3		1	1.3	pF
$\frac{I_{C(on)1}}{I_{C(on)2}}$	On-state collector current symmetry ratio (see Note 6)		V_{CE} = 1 V, I_F = 2 mA	1		3	1		3	

†These parameters apply for either direction of the input current.

NOTES: 5. These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

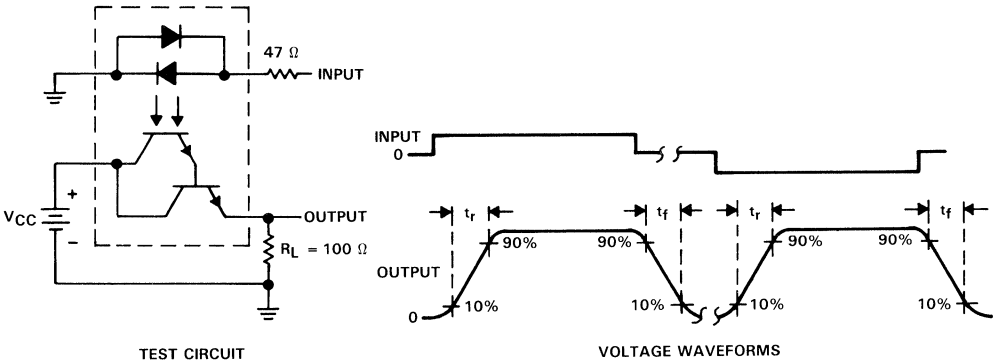
6. The higher of the two $I_{C(on)}$ values generated by the two diodes is taken as $I_{C(on)1}$.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		TIL187			TIL188			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_{CC} = 10 V,	$I_{C(on)}$ = 10 mA,		100			100		μs
t_f	Fall time	R_L = 100 Ω,	see Figure 1		100			100		μs

PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse is for $I_{C(on)}$ = 10 mA



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_r = ≤ 15 ns, duty cycle = 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_1 ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

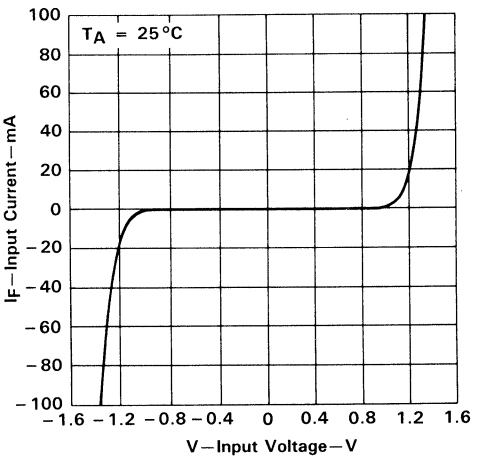


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

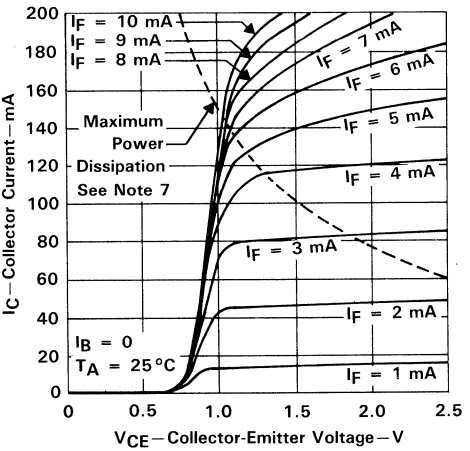


FIGURE 3

Note 7: Pulse operation is required for operation beyond limits shown by the dashed line.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

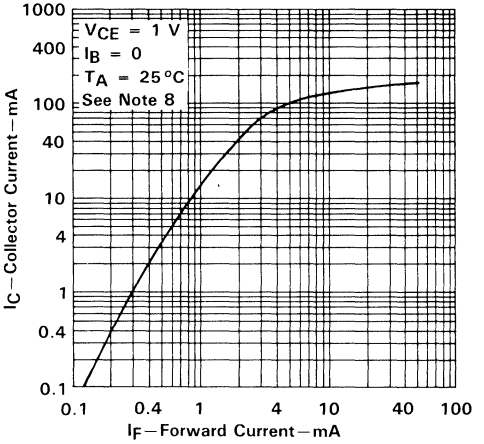


FIGURE 4

NORMALIZED ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

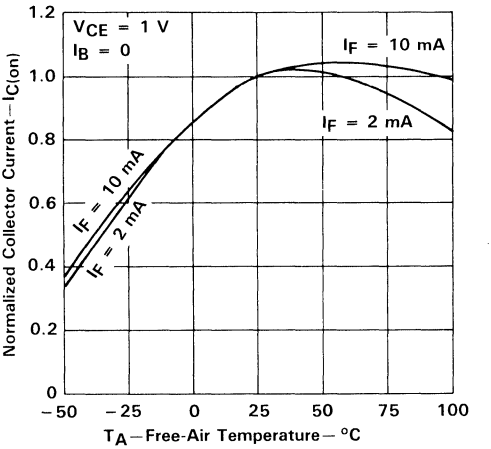


FIGURE 5

TIL187
NORMALIZED TRANSISTOR STATIC
FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

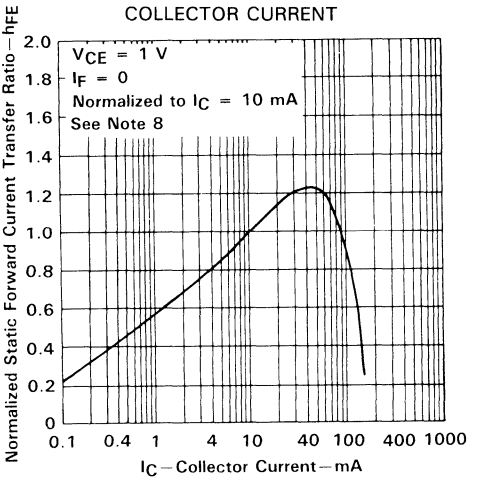


FIGURE 6

TIL187
NORMALIZED TRANSISTOR STATIC
FORWARD CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

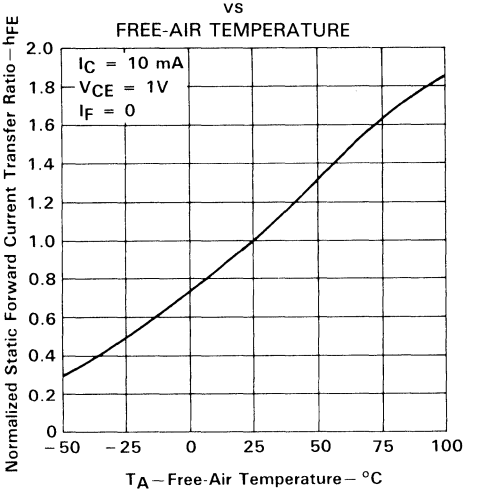


FIGURE 7

NOTE 8: These parameters were measured using pulse techniques t_w = 1 ms, duty cycle ≤ 2%.

TIL187

NORMALIZED ON-STATE COLLECTOR CURRENT
(PHOTODIODE OPERATION)
vs
FREE-AIR TEMPERATURE

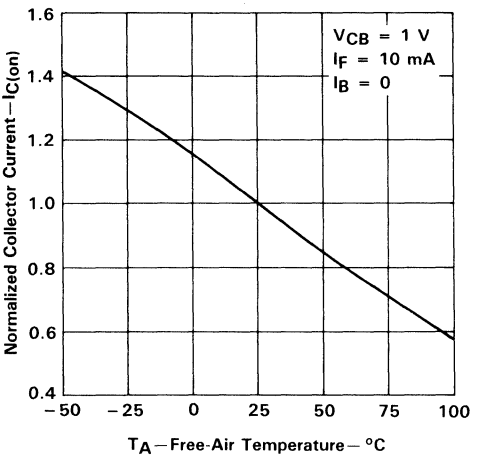


FIGURE 8

NORMALIZED COLLECTOR-EMITTER
BREAKDOWN VOLTAGE
vs
FREE-AIR TEMPERATURE

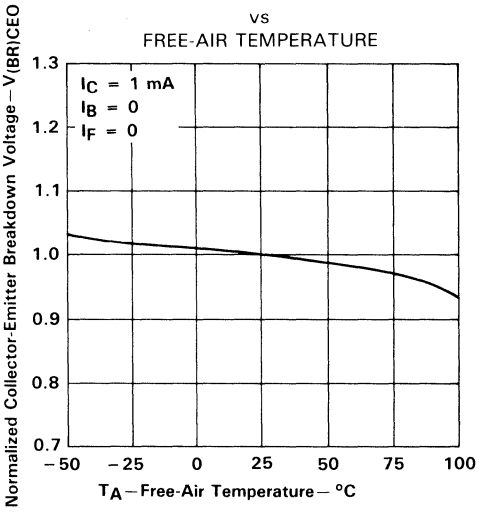


FIGURE 9

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

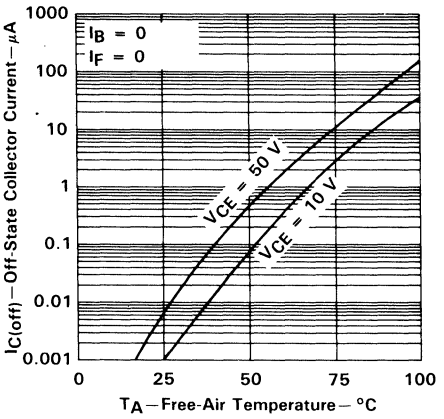


FIGURE 10

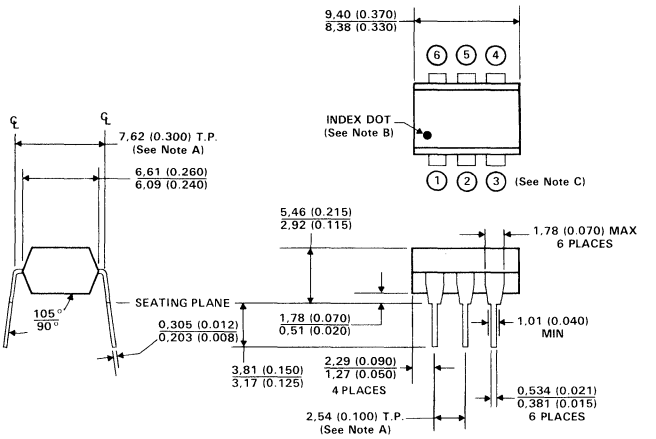
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **High Direct-Current Transfer Ratios, 500% Minimum at I_F = 10 mA and Up to 1500% at I_F = 2 mA with Choice of Four Categories**
- **Plastic Dual-In-Line Package**
- **High-Voltage Electrical Isolation, 3.535 kV Peak (2.5 kV rms)**
- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Darlington Phototransistor**
- **No Base Lead Connection on TIL190 for High-EMI Environment**
- **UL Recognized — File #E65085**

description

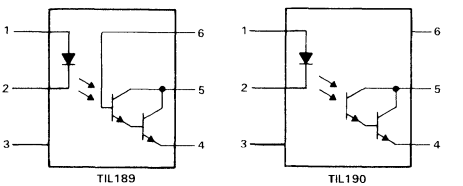
The TIL189 and TIL190 Optocouplers are designed for use in applications that require high current transfer ratio and high voltage isolation between the input and output. The TIL189 has the base connected for applications where a base signal or resistor is required. The TIL190 is designed with no internal base connection for applications where high base-noise immunity is desired. Users can select from four different current gains (TIL189-1 through TIL189-4 and TIL190-1 through TIL190-4).

mechanical data



CP 7

NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode } Infrared-emitting diode
2. Cathode }
3. No internal connection
4. Emitter }
5. Collector } Phototransistor
6. TIL189: Base }
TIL190: No internal connection



FALLS WITHIN JEDEC MO-001AM DIMENSIONS

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage	±3.535 kV peak or dc (±2.5 kV rms)
Collector-base voltage (TIL189)	100 V
Collector-emitter voltage (see Note 1)	55 V
Emitter-collector voltage	7 V
Emitter-base voltage (TIL189)	14 V
Input diode reverse voltage	3 V
Input diode continuous forward current at (or below) 25°C free-air temperature (see Note 2)	100 mA
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 3)	150 mW
Phototransistor (see Note 3)	150 mW
Total, infrared-emitting diode plus phototransistor (see Note 4)	250 mW
Storage temperature range	−55°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260°C

NOTES: 1. This value applies when the base-emitter diode is open circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

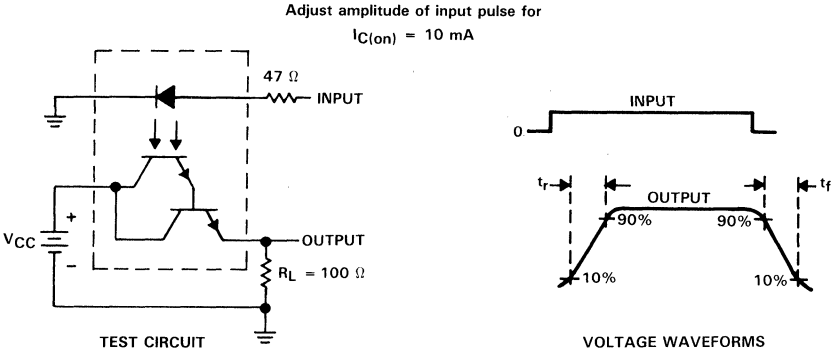
PARAMETER			TEST CONDITIONS	TIL189			TIL190			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA, I_E = 0, I_F = 0	100						V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA, I_B = 0, I_F = 0	55			55			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA, I_C = 0, I_F = 0	14						V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		I_E = 100 μA, I_F = 0				7			V
I_R	Input diode static reverse current		V_R = 3 V			10			10	μA
$I_{C(on)}$	On-state collector current	Photo-transistor operation, TIL189-1, TIL190-1	V_{CE} = 1 V, I_F = 2 mA, I_B = 0	5			5			mA
		Photo-transistor operation, TIL189-2, TIL190-2		10			10			
		Photo-transistor operation, TIL189-3, TIL190-3		20			20			
		Photo-transistor operation, TIL189-4, TIL190-4		30			30			
		Photo-transistor operation	V_{CE} = 1 V, I_F = 10 mA, I_B = 0	50			50			
		Photodiode operation	V_{CB} = 1 V, I_F = 10 mA, I_E = 0	5	15					μA
$I_{C(off)}$	Off-state collector current		V_{CE} = 10 V, I_F = 0, I_B = 0		1	100		1	100	nA
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 1 V, I_C = 10 mA, I_F = 0		25000					
V_F	Input diode static forward voltage		I_F = 10 mA		1.2	1.5		1.2	1.5	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 50 mA, I_F = 10 mA, I_B = 0		0.87	1		0.87	1	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V, See Note 5	10^{11}			10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0, f = 1 mHz, See Note 5		1	1.3		1	1.3	pF

NOTE 5: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		TIL189			TIL190			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_{CC} = 10 V,	$I_{C(on)}$ = 10 mA,		100			100		μs
t_f	Fall time	R_L = 100 Ω,	see Figure 1		100			100		μs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_r = ≤ 15 ns, duty cycle = 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_1 ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

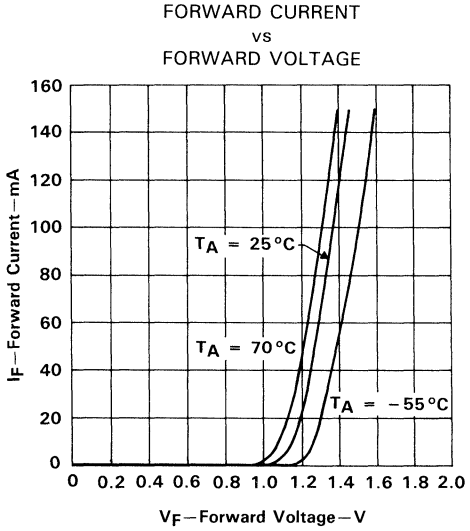


FIGURE 2

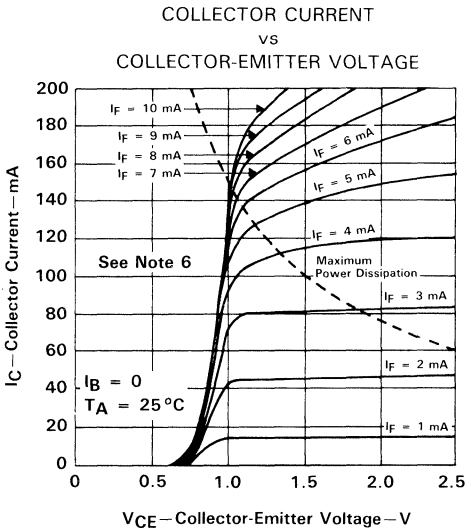


FIGURE 3

NOTE 6: Pulse operation is required for operation beyond limits shown by the dashed line.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

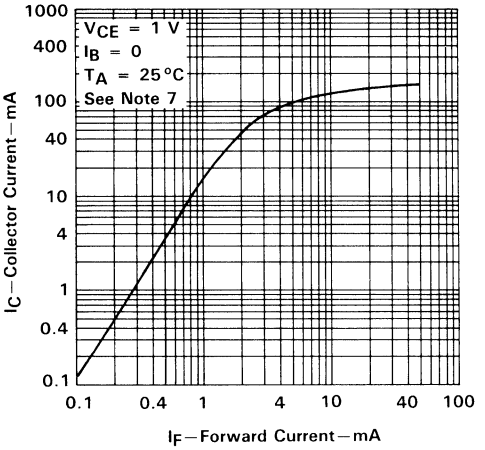


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

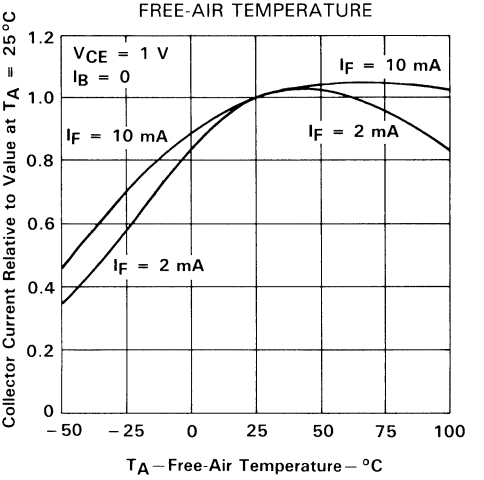


FIGURE 5

TIL189
NORMALIZED TRANSISTOR STATIC
FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

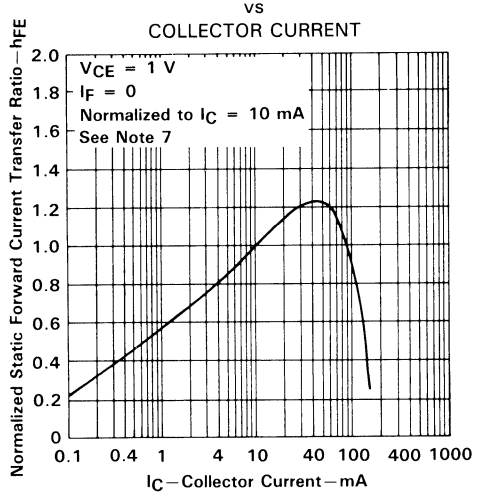


FIGURE 6

TIL189
NORMALIZED TRANSISTOR STATIC
FORWARD CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

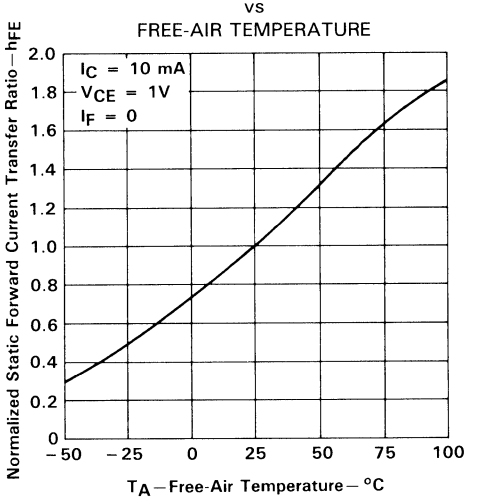


FIGURE 7

NOTE 7: These parameters were measured using pulse techniques t_w = 1 ms, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS

TIL189

RELATIVE ON-STATE COLLECTOR CURRENT
(PHOTODIODE OPERATION)
vs
FREE-AIR TEMPERATURE

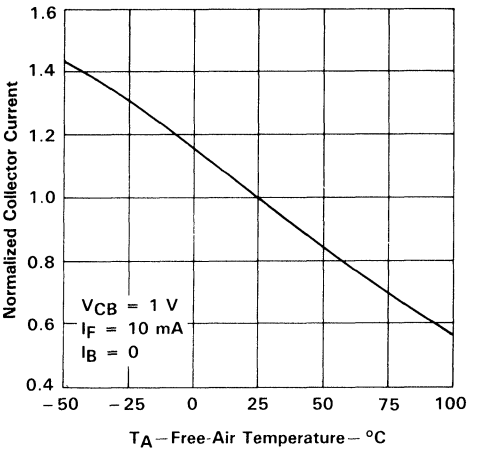


FIGURE 8

RELATIVE COLLECTOR-EMITTER
BREAKDOWN VOLTAGE
vs
FREE-AIR TEMPERATURE

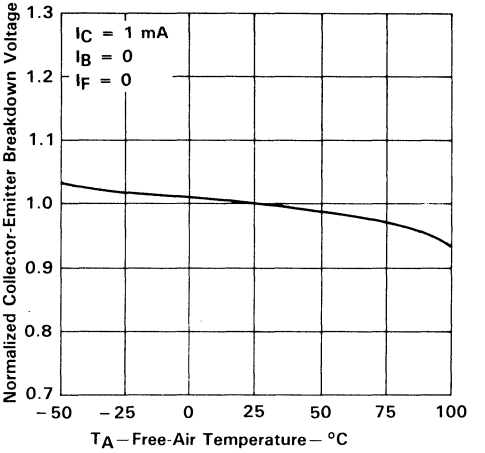


FIGURE 9

OFF-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

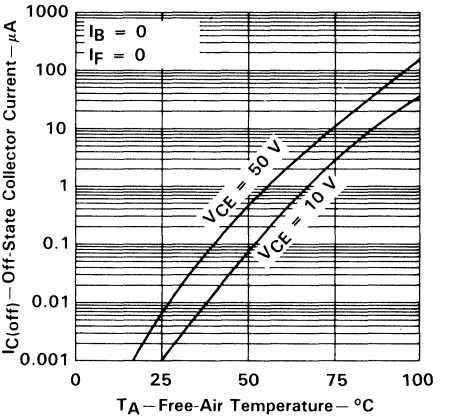


FIGURE 10

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

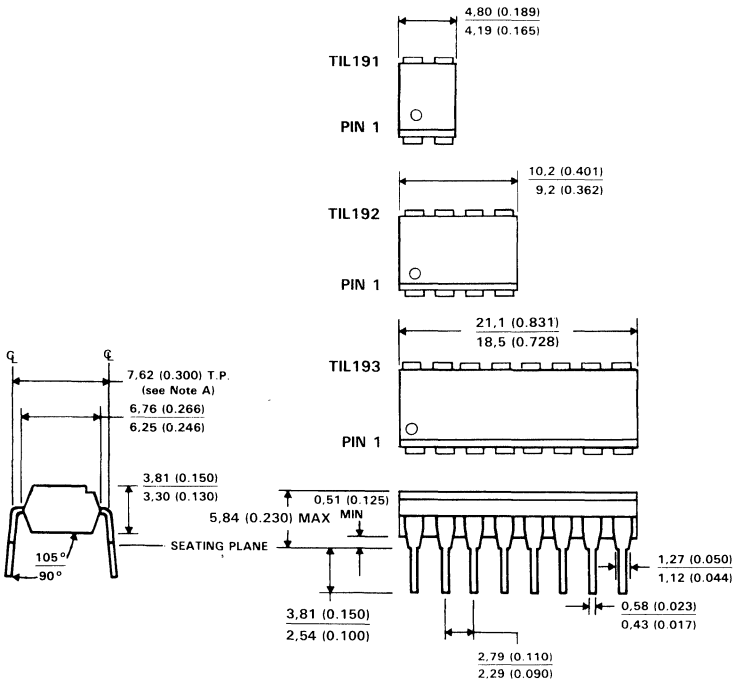
D3263, APRIL 1989—REVISED SEPTEMBER 1989

- Gallium Arsenide Diode Infrared Source
- Source Is Optically Coupled to Silicon N-P-N Phototransistor
- Choice of One, Two, or Four Channels
- Choice of Three Current-Transfer Ratios
- High-Voltage Electrical Isolation 3.535 kV Peak (2.5 kV rms)
- Plastic Dual-In-Line Packages
- UL Listed — File #E65085

description

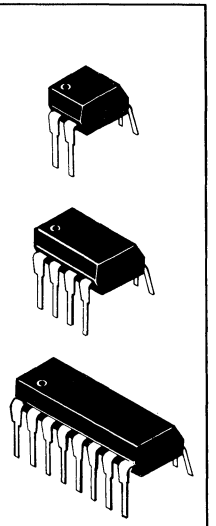
These optocouplers consist of a gallium-arsenide light-emitting diode and a silicon n-p-n phototransistor per channel. The TIL191 has one channel in a 4-pin package, the TIL192 has two channels in an 8-pin package, and the TIL193 has four channels in a 16-pin package. The standard devices, TIL191, TIL192, and TIL193, are tested for a current-transfer ratio of 20% minimum. Devices selected for a current-transfer ratio of 50% and 100% minimum are designated with the suffix A and B respectively.

mechanical data



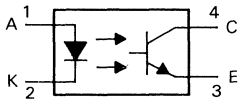
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

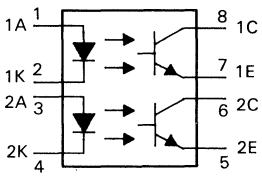


schematic diagrams

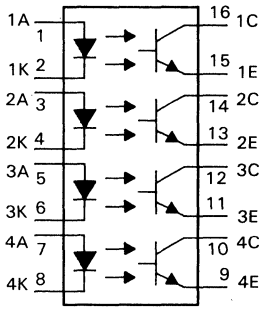
TIL191



TIL192



TIL193



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage (see Note 1) . . . . . ±3.535 kV peak or dc (±2.5 kV rms)
Collector-emitter voltage (see Note 2) . . . . . 35 V
Emitter-collector voltage . . . . . 7 V
Input diode reverse voltage . . . . . 5 V
Input diode continuous forward current at (or below) 25°C free-air temperature (see Note 3) . . . . . 50 mA
Continuous power dissipation at (or below) 25°C free-air temperature:
Phototransistor (see Note 4) . . . . . 150 mW
Input diode plus phototransistor per channel (see Note 5) . . . . . 200 mW
Storage temperature range . . . . . −55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. This rating applies for sine-wave operation at 50 or 60 Hz. Service capability is verified by testing in accordance with UL requirements.
2. This value applies when the base-emitter diode is open circuited.
3. Derate linearly to 100°C free-air temperature at the rate of 0.67 mA/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 2.67 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 0.5 mA, I_F = 0	35			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		I_C = 100 μA, I_F = 0	7			V
I_R	Input diode static reverse current		V_R = 5 V			10	μA
$I_{C(off)}$	Off-state collector current		V_{CE} = 24 V, I_F = 0			100	nA
CTR	Current transfer ratio	TIL191, TIL192, TIL193	I_F = 5 mA, V_{CE} = 5 V	20%			
		TIL191A, TIL192A, TIL193A		50%			
		TIL191B, TIL192B, TIL193B		100%			
V_F	Input diode static forward voltage		I_F = 20 mA			1.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_F = 5 mA, I_C = 1 mA			0.4	V
C_{io}	Input-to-output capacitance		V_{in-out} = 0, f = 1 MHz, See Note 6		1		pF
r_{io}	Input-to-output internal resistance		V_{in-out} = ±1 kV, See Note 6		10^{11}		Ω

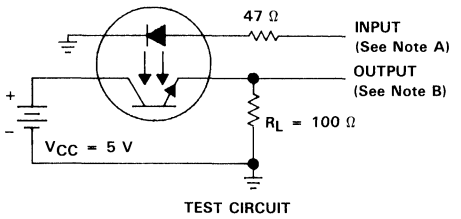
NOTE 6: These parameters are measured between all input-diode leads shorted together and all phototransistor leads shorted together.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

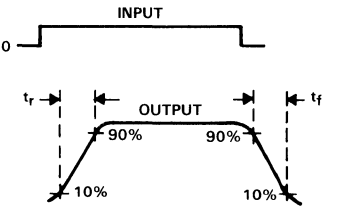
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_r	Rise time	V_{CC} = 5 V, $I_{C\ (on)}$ = 2 mA, R_L = 100 Ω, See Figure 1	6	μs
t_f	Fall time		6	μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



Adjust amplitude of input pulse for $I_{C(on)}$ = 2 mA

VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{OUT} = 50 Ω, $t_r \leq 15$ ns, t_w = 100 μs, duty cycle ≈ 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 12$ ns, $R_{in} \geq 1$ MΩ, $C_{in} \leq 20$ pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

FORWARD CURRENT
vs
FORWARD VOLTAGE

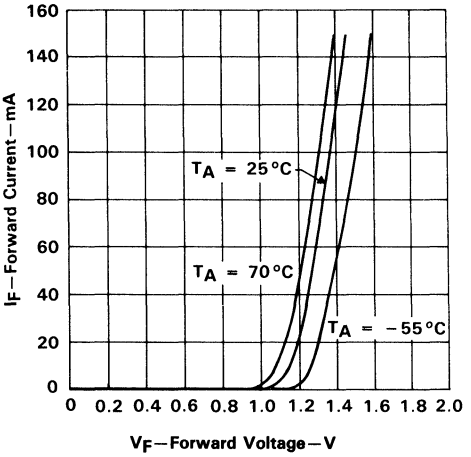


FIGURE 2

TIL191, TIL192, TIL193
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

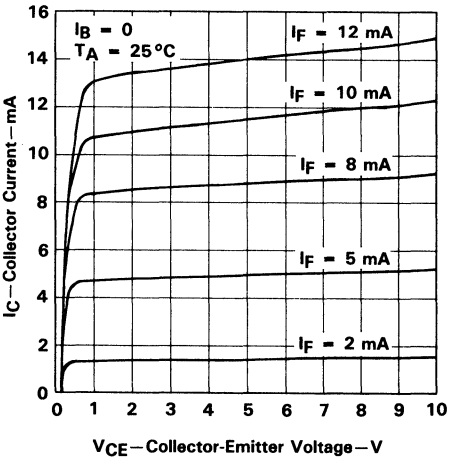


FIGURE 3

NORMALIZED ON-STATE COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

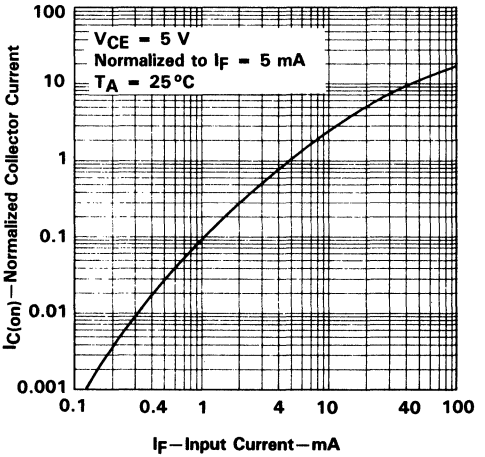


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

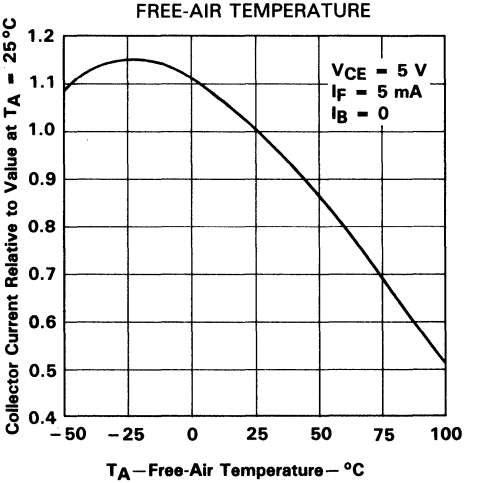


FIGURE 5

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TYPICAL COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

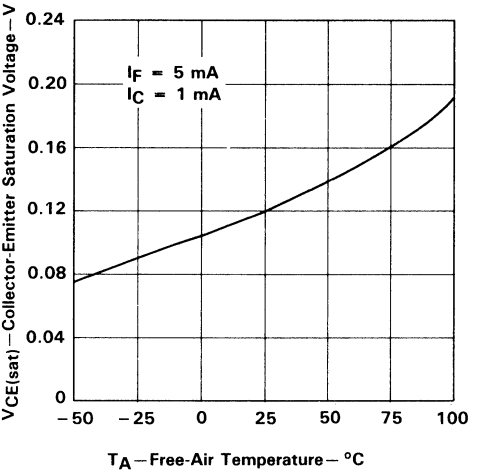


FIGURE 6

TYPICAL APPLICATION DATA

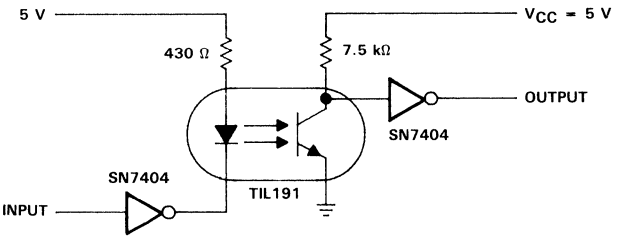


FIGURE 7

AC-INPUT OPTOCOUPLERS

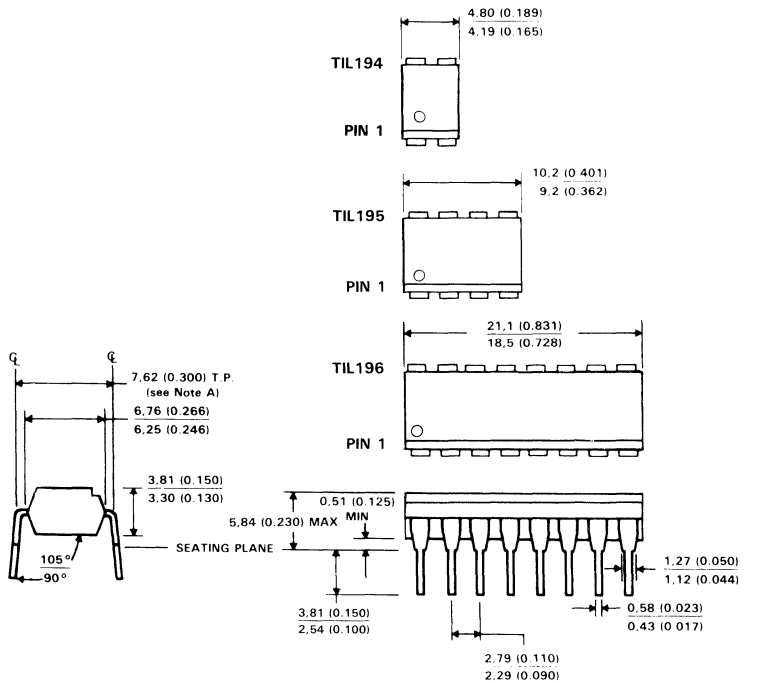
D3287, MAY 1989 – REVISED SEPTEMBER 1989

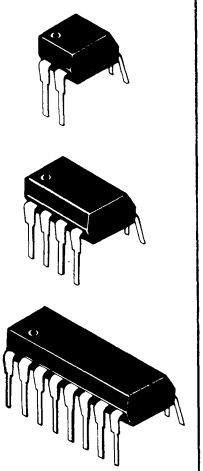
- AC Signal Input
- Gallium-Arsenide Diode Infrared Source
- Source Is Optically Coupled to Silicon N-P-N Phototransistor
- Choice of One, Two, or Four Channels
- Choice of Three Current-Transfer Ratios
- High-Voltage Electrical Isolation 3.535 kV Peak (2.5 kV rms)
- Plastic Dual-In-Line Packages
- UL Listed — File #E65085

description

These optocouplers consist of two gallium-arsenide light-emitting diodes connected in a reverse-parallel configuration for ac-input applications and a silicon n-p-n phototransistor per channel. The TIL194 has one channel in a 4-pin package, the TIL195 has two channels in an 8-pin package, and the TIL196 has four channels in a 16-pin package. The standard devices, TIL194, TIL195, and TIL196, are tested for a current-transfer ratio of 20% minimum. Devices selected for a current-transfer ratio of 50% and 100% minimum are designated with the suffix A and B respectively.

mechanical data



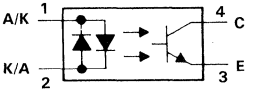


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

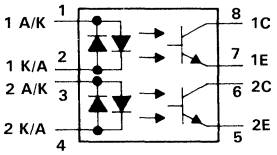
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

schematic diagrams

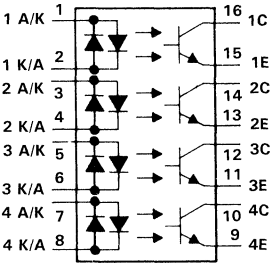
TIL194
(TOP VIEW)



TIL195
(TOP VIEW)



TIL196
(TOP VIEW)



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage (see Note 1) . . . . . ±3.535 kV peak or dc (±2.5 kV rms)
Collector-emitter voltage (see Note 2) . . . . . 35 V
Emitter-collector voltage . . . . . 7 V
Input diode continuous forward current at (or below) 25°C free-air temperature (see Note 3) . . . . . ±50 mA
Continuous power dissipation at (or below) 25°C free-air temperature:
Phototransistor (see Note 4) . . . . . 150 mW
Input diode plus phototransistor per channel (see Note 5) . . . . . 200 mW
Storage temperature range . . . . . −55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. This rating applies for sine-wave operation at 50 or 60 Hz. Service capability is verified by testing in accordance with UL requirements.
2. This value applies when the base-emitter diode is open circuited.
3. Derate linearly to 100°C free-air temperature at the rate of 0.67 mA/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 2.67 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 0.5 mA, I_F = 0	35			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage		I_C = 100 μA, I_F = 0	7			V
$I_{C(off)}$	Off-state collector current		V_{CE} = 24 V, I_F = 0			100	nA
CTR†	Current transfer ratio	TIL194, TIL195, TIL196	I_F = 5 mA, V_{CE} = 5 V	20%			
		TIL194A, TIL195A, TIL196A		50%			
		TIL194B, TIL195B, TIL196B		100%			
V_F†	Input diode static forward voltage		I_F = 20 mA			1.4	V
$V_{CE(sat)}$†	Collector-emitter saturation voltage		I_F = 5 mA, I_C = 1 mA			0.4	V
C_{io}	Input-to-output capacitance		V_{in-out} = 0, f = 1 MHz, See Note 6		1		pF
r_{io}	Input-to-output internal resistance		V_{in-out} = ±1 kV, See Note 6		10^{11}		Ω
$\frac{I_{C(on)1}}{I_{C(on)2}}$	On-state collector current symmetry ratio (see Note 7)		V_{CE} = 5 V, I_F = 5 mA	1		3	

†These parameters apply to either direction of the input current.
NOTES 6: These parameters are measured between all input-diode leads shorted together and all phototransistor leads shorted together.
7. The higher of the two values of $I_{C(on)}$ generated by the two diodes is taken as $I_{C(on)1}$.

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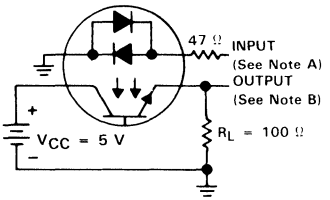
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_r†	Rise time	V_{CC} = 5 V, $I_{C(on)}$ = 2 mA,	6	μs
t_f†	Fall time	R_L = 100 Ω, See Figure 1	6	μs

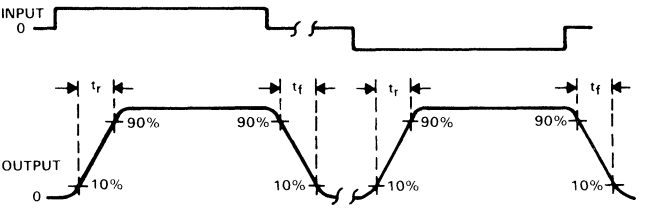
†These parameters apply to either direction of the input current.

PARAMETER MEASUREMENT INFORMATION

Adjust amplitude of input pulse for $I_{C(on)}$ = 2 mA



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, $t_r \leq$ 15 ns, duty cycle = 1%.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_i \geq$ 1 MΩ, $C_i \leq$ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

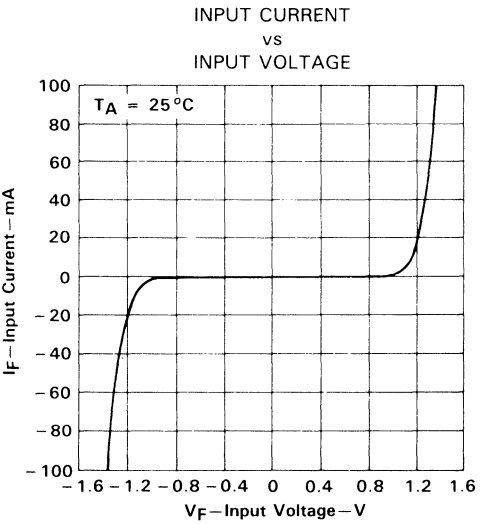


FIGURE 2

TYPICAL CHARACTERISTICS

TIL194, TIL195, TIL196
COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

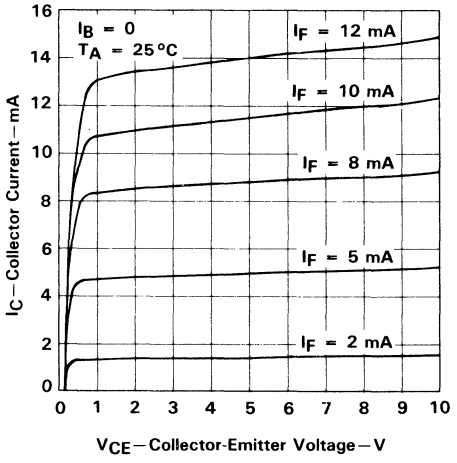


FIGURE 3

NORMALIZED ON-STATE COLLECTOR CURRENT
vs
INPUT-DIODE FORWARD CURRENT

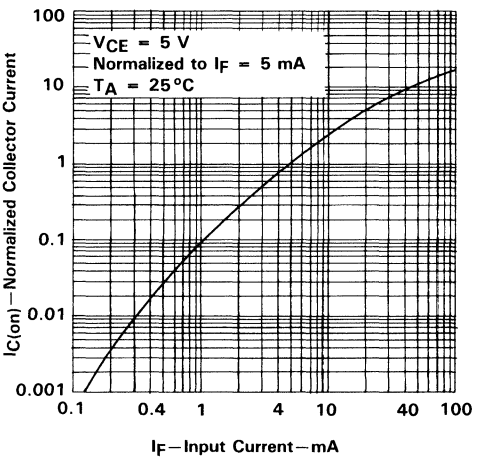


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

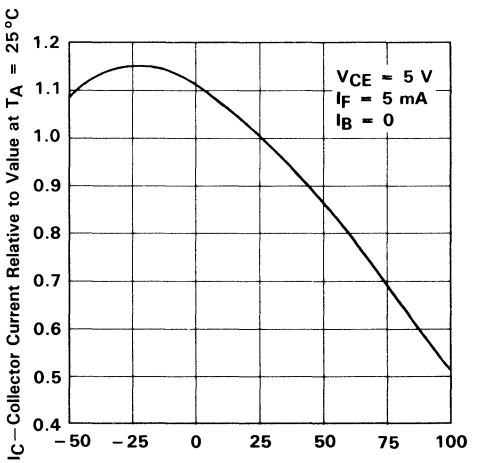


FIGURE 5

TYPICAL COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

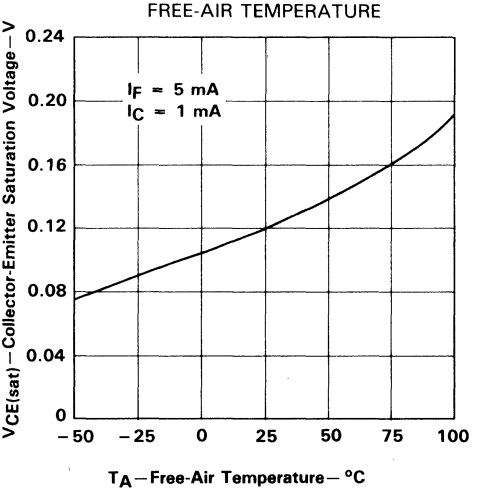


FIGURE 6

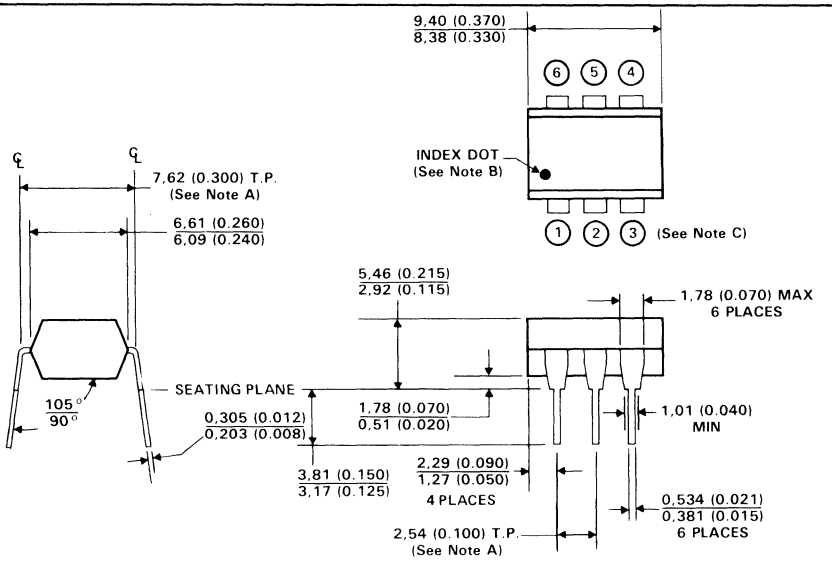
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3064, DECEMBER 1987

- 250-V Phototriac Driver Output
- Gallium Arsenide Diode Infrared Source and Optically Coupled Silicon Triac Driver (Bilateral Switch)
- UL Recognized . . . File Number E65085
- High Isolation . . . 3535 V Peak
- Output Driver Designed for 115 V AC
- Standard 6-Pin Plastic DIP

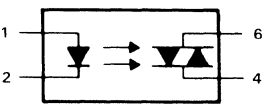
mechanical

Each device consists of a gallium arsenide infrared emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.



FALLS WITHIN JEDEC MO-001 AM DIMENSIONS

NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode } Infrared emitting diode
2. Cathode
3. No internal connection
4. Main terminal
5. Triac Substrate (DO NOT connect) } Phototriac
6. Main terminal



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1) . . . . . 3.535 kV
Input diode reverse voltage . . . . . 3 V
Input diode forward current, continuous . . . . . 50 mA
Output repetitive peak off-state voltage . . . . . 250 V
Output on-state current, total rms value (50-60 Hz, full sine wave):
  T_A = 25°C . . . . . 100 mA
  T_A = 70°C . . . . . 50 mA
Output driver nonrepetitive peak on-state current
  (t_W = 10 ms, duty cycle = 10%, see Figure 7) . . . . . 1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:
  Infrared-emitting diode (see Note 2) . . . . . 100 mW
  Phototriac (see Note 3) . . . . . 300 mW
  Total device (see Note 4) . . . . . 330 mW
Operating junction temperature range . . . . . −40°C to 100°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	μA
V_F	Static forward voltage		I_F = 10 mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		V_{DRM} = 250 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		12		V/μs
dv/dt(c)	Critical rate of rise of commutating voltage		I_O = 15 mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current, either direction	TIL3009	Output supply voltage = 3 V		15	30	mA
		TIL3010			8	15	
		TIL3011			5	10	
		TIL3012				5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.8	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied within dv/dt rating.

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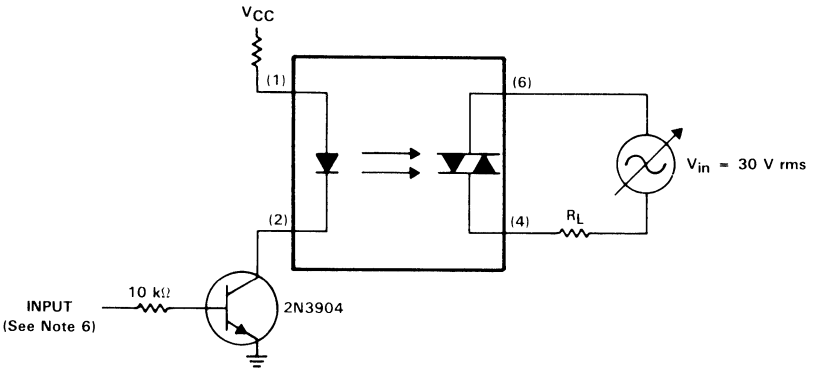
PARAMETER MEASUREMENT INFORMATION



NOTE 6: The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 volts. The frequency of V_{in} is increased until the phototriac just turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

FIGURE 1. CRITICAL RATE OF RISE TEST CIRCUIT

TYPICAL CHARACTERISTICS

EMITTING DIODE NORMALIZED TRIGGER CURRENT
vs
FREE-AIR TEMPERATURE

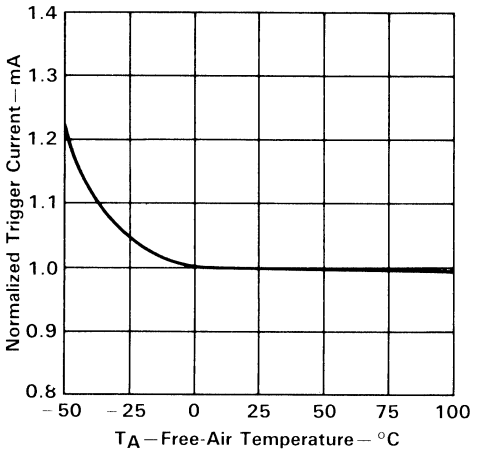


FIGURE 2

ON-STATE CHARACTERISTICS

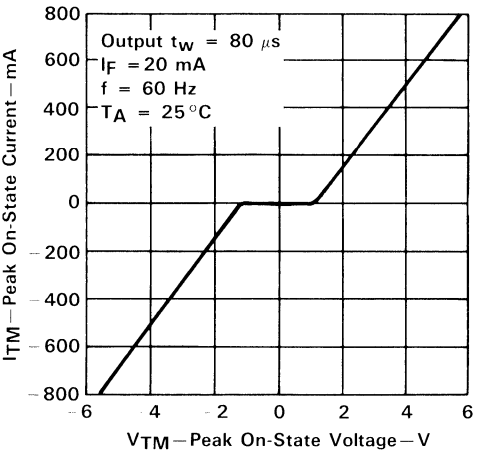


FIGURE 3

TYPICAL CHARACTERISTICS

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
vs
LOAD RESISTANCE

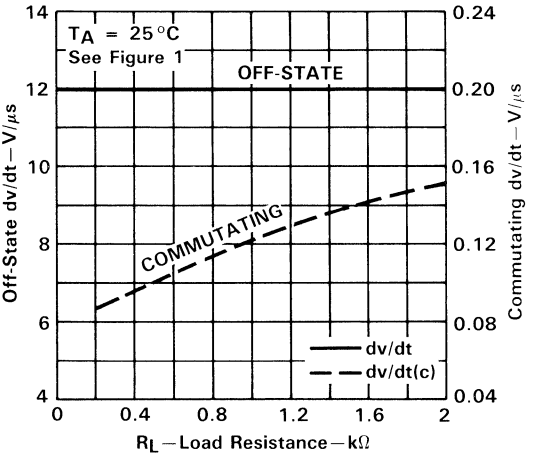


FIGURE 4

CRITICAL RATE OF RISE OF OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

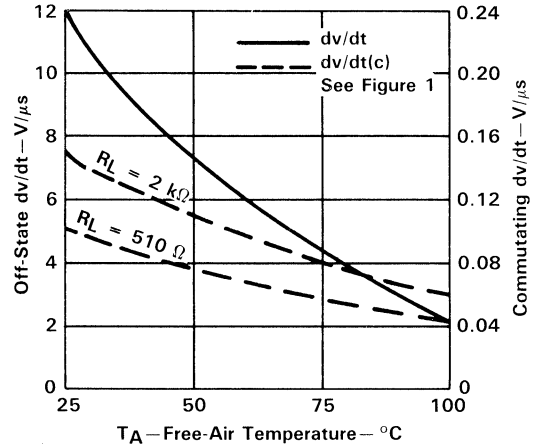


FIGURE 5

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

RMS APPLIED VOLTAGE
(FOR dv/dt(c) = 0.15 V/μs)
vs
FREQUENCY

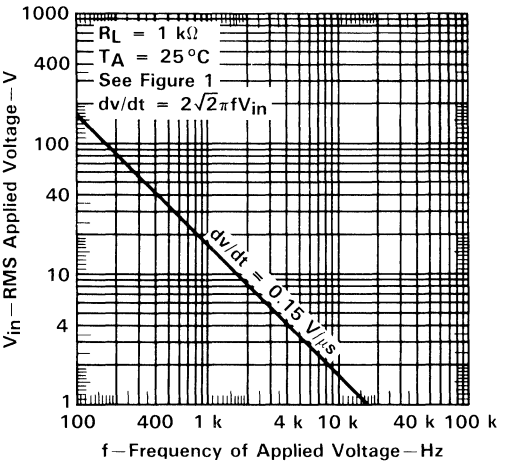


FIGURE 6

MAXIMUM RATINGS

NONREPETITIVE PEAK ON-STATE CURRENT
vs
PULSE DURATION

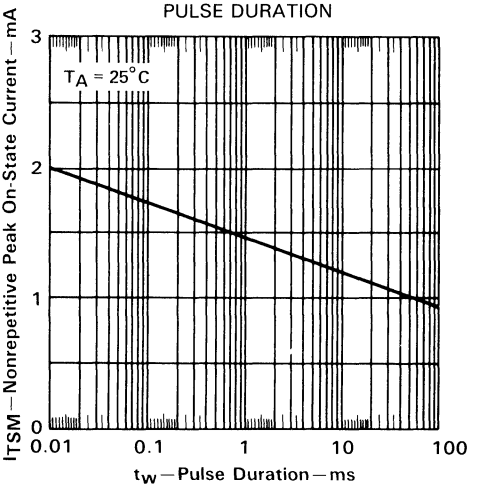


FIGURE 7

TYPICAL APPLICATIONS

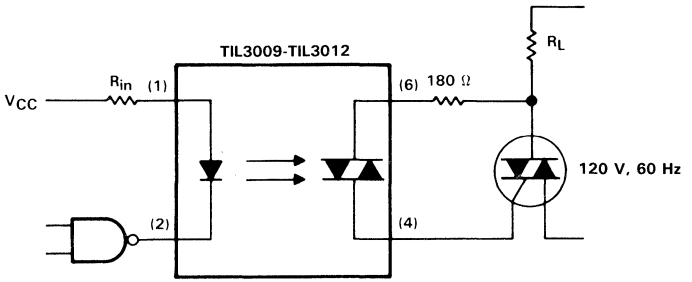


FIGURE 8. RESISTIVE LOAD

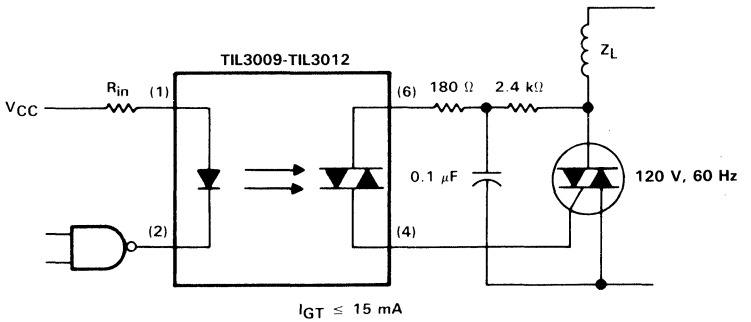


FIGURE 9. INDUCTIVE LOAD WITH SENSITIVE-GATE TRIAC

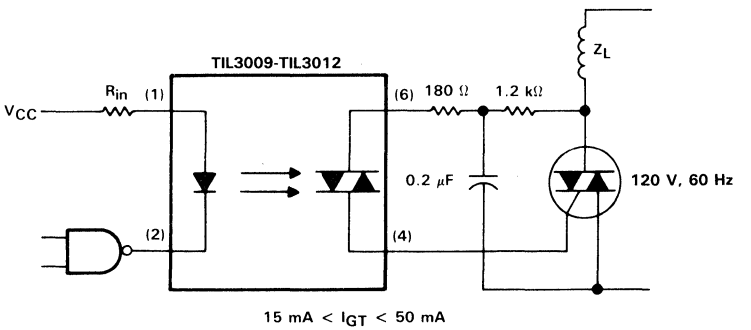


FIGURE 10. INDUCTIVE LOAD WITH NONSENSITIVE-GATE TRIAC

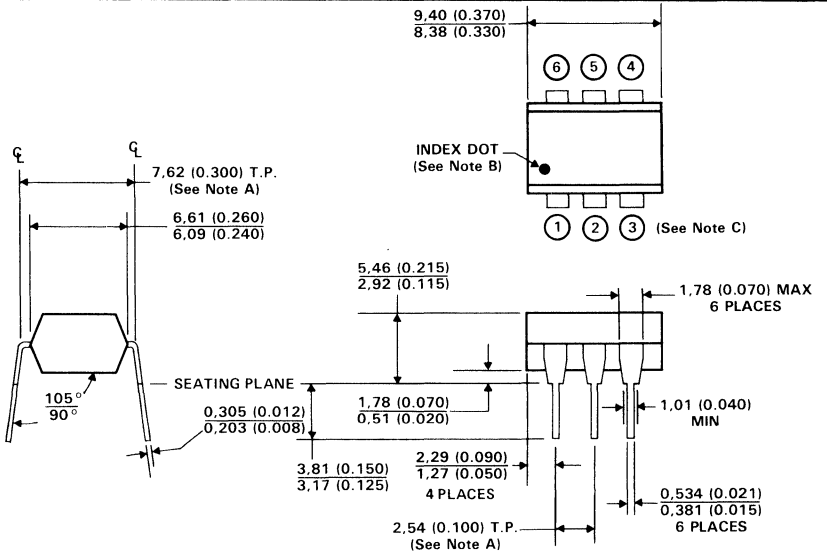
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3065, DECEMBER 1987

- **400-V Phototriac Driver Output**
- **Gallium Arsenide Diode Infrared Source and Optically Coupled Silicon Triac Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 3535 V Peak**
- **Output Driver Designed for 220 V AC**
- **Standard 6-Pin Plastic DIP**

mechanical

Each device consists of a gallium arsenide infrared emitting diode optically coupled to a silicon phototriac mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.

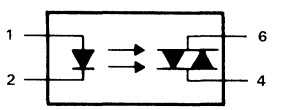


FALLS WITHIN JEDEC MO-001 AM DIMENSIONS

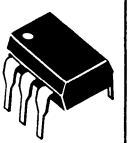
NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode
2. Cathode
3. No internal connection
4. Main terminal
5. Triac Substrate (DO NOT connect)
6. Main terminal

Infrared-emitting diode

Phototriac



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1) . . . . . 3.535 kV
Input diode reverse voltage . . . . . 3 V
Input diode forward current, continuous . . . . . 50 mA
Output repetitive peak off-state voltage . . . . . 400 V
Output on-state current, total rms value (50-60 Hz, full sine wave):
  T_A = 25°C . . . . . 100 mA
  T_A = 70°C . . . . . 50 mA
Output driver nonrepetitive peak on-state current
  (t_W = 10 ms, duty cycle = 10%, see Figure 7) . . . . . 1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:
  Infrared-emitting diode (see Note 2) . . . . . 100 mW
  Phototriac (see Note 3) . . . . . 300 mW
  Total device (see Note 4) . . . . . 330 mW
Operating junction temperature range . . . . . −40°C to 100°C
Storage temperature range . . . . . −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

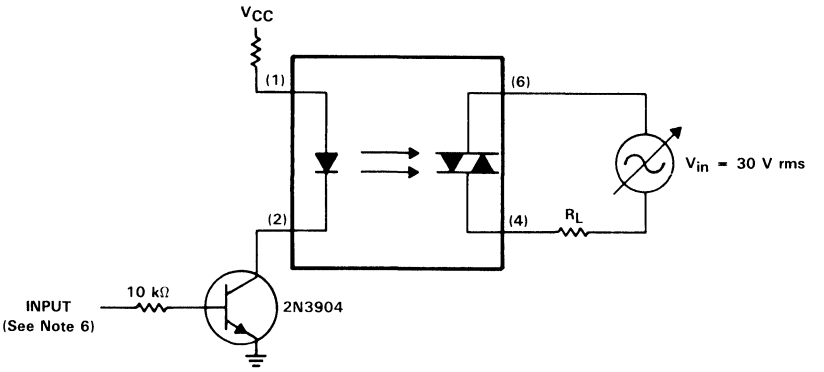
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	μA
V_F	Static forward voltage		I_F = 10 mA		1.2	1.5	V
I_{DRM}	Repetitive off-state current, either direction		V_{DRM} = 400 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		100		V/μs
dv/dt(c)	Critical rate of rise of commutating voltage		I_O = 15 mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current, either direction	TIL3020	Output supply voltage = 3 V		15	30	mA
		TIL3021			8	15	
		TIL3022			5	10	
		TIL3023			3	5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.4	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied at a rate no higher than 12 V/μs.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



NOTE 6: The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 volts. The frequency of V_{in} is increased until the phototriac just turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2}\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-volt pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

FIGURE 1. CRITICAL RATE OF RISE TEST CIRCUIT

TYPICAL CHARACTERISTICS

EMITTING DIODE NORMALIZED TRIGGER CURRENT
vs
FREE-AIR TEMPERATURE

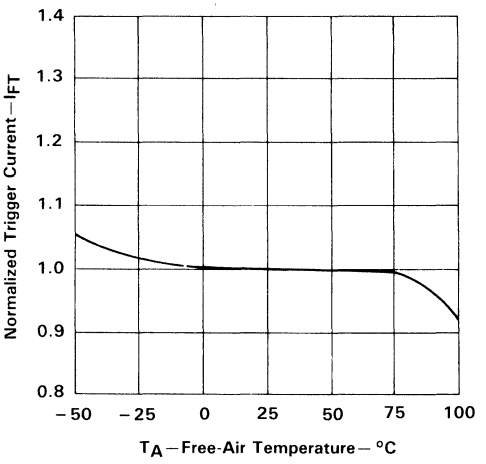


FIGURE 2

ON-STATE CHARACTERISTICS

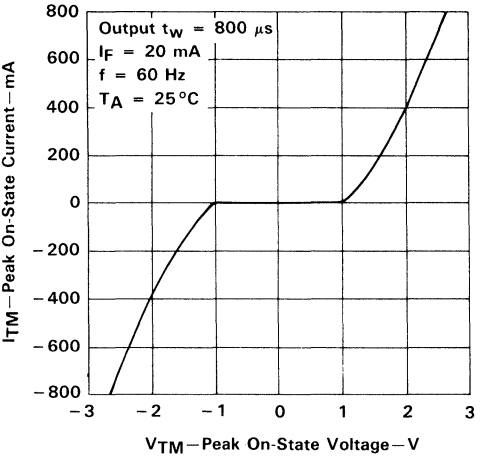


FIGURE 3

MAXIMUM RATINGS

NONREPETITIVE PEAK ON-STATE CURRENT
vs
PULSE DURATION

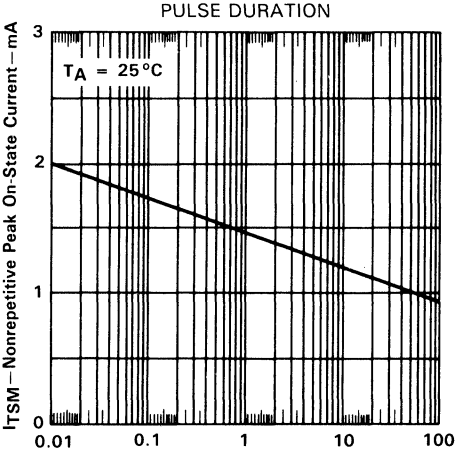


FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL APPLICATIONS

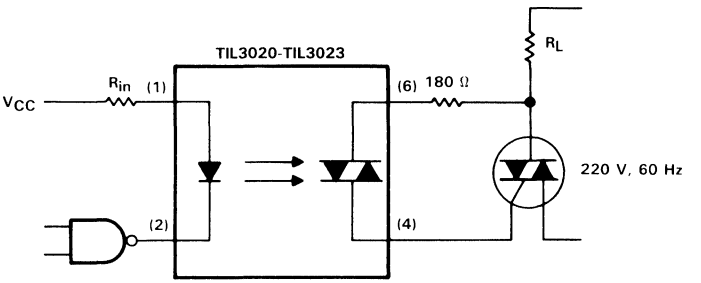


FIGURE 5. RESISTIVE LOAD

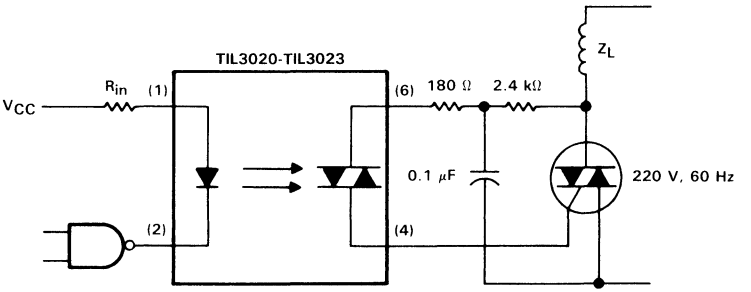


FIGURE 6. INDUCTIVE LOAD WITH SENSITIVE-GATE TRIAC

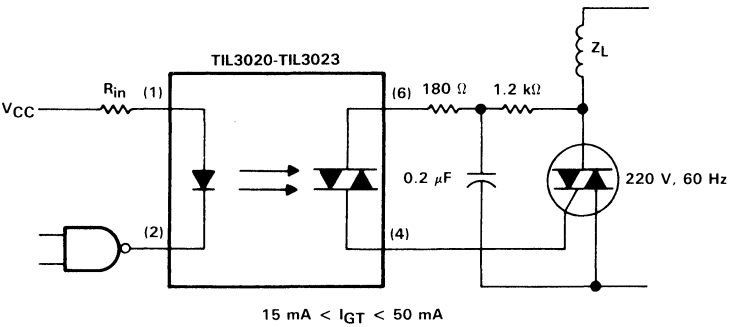


FIGURE 7. INDUCTIVE LOAD WITH NONSENSITIVE-GATE TRIAC

Intelligent LED Displays

D1021, APRIL 1971 – REVISED JUNE 1982

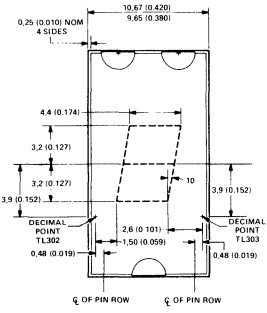
RED SOLID-STATE DISPLAYS

- 6,9-mm (0.270-Inch) Character Height
- High Luminous Intensity
- Low Power Requirements
- Each Unit Visually Checked for Uniformity of Elements
- Sign, Overflow, Left or Right Decimal Capability
- Wide Viewing Angle
- Compatible with Most TTL and DTL Circuits

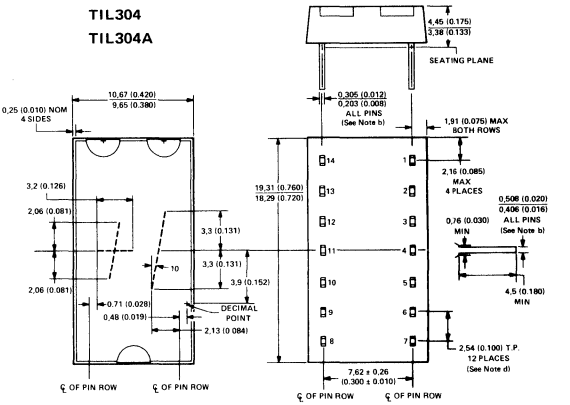
mechanical data

These assemblies consist of display chips mounted on a header with either a red molded plastic body for the TIL302, TIL303, and TIL304 or a red plastic cap for the TIL302A, TIL303A, and TIL304A. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.

TIL302
TIL302A
TIL303
TIL303A

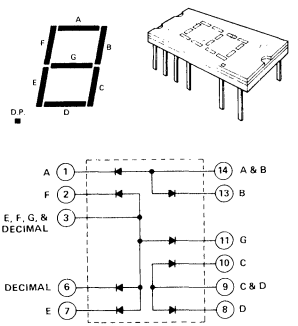


TIL304
TIL304A



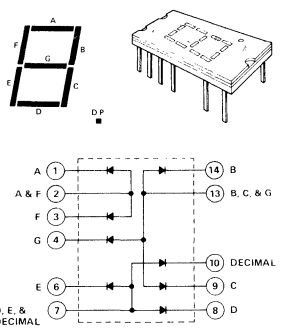
NOTES: a. All linear dimensions are in millimeters and parenthetically in inches.
b. Lead dimensions are not controlled above the seating plane.
c. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.
d. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located within 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 11.
e. On TIL302A, TIL303A, and TIL304A devices, the 3 mold indentations are not present.

TIL302, TIL302A



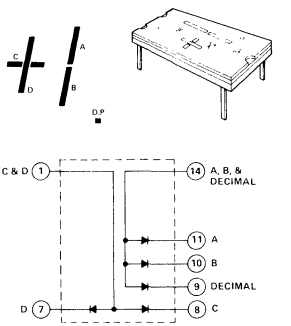
PINS 4, 5, AND 12 OMITTED

TIL303, TIL303A



PINS 5, 11, AND 12 OMITTED

TIL304, TIL304A



PINS 2, 3, 4, 5, 6, 12, AND 13 OMITTED

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Reverse Voltage at 25°C Free-Air Temperature:
- Each Segment . . . . . 6 V
- Decimal Point . . . . . 3 V

Peak Forward Current, Each Segment or Decimal Point (See Note 1) . . . . . 200 mA

Continuous Forward Current:
- Each Segment or Decimal Point . . . . . 30 mA
- Total for TIL302, TIL302A, TIL303, TIL303A . . . . . 240 mA
- Total for TIL304, TIL304A . . . . . 150 mA

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . −25°C to 85°C

NOTE 1: This value applies for PRR ≥ 60 Hz, duty cycle ≤ 10%.

operating characteristics of each segment at 25°C free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_V	Luminous Intensity (See Note 2)	I_F = 20 mA	100	275		μcd
λ_p	Wavelength at Peak Emission			660		nm
$\Delta\lambda$	Spectral Bandwidth			20		nm
V_F	Static Forward Voltage		3	3.4	3.8	V
α_{VF}	Average Temperature Coefficient of Static Forward Voltage	I_F = 20 mA, T_A = 0°C to 70°C		−2.7		mV/°C
I_R	Static Reverse Current	V_R = 6 V			100	μA
C	Anode-to-Cathode Capacitance	V_R = 0, f = 1 MHz		85		pF

operating characteristics of decimal point at 25°C free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_V	Luminous Intensity (See Note 2	I_F = 20 mA	40	110		μcd
λ_p	Wavelength at Peak Emission			660		nm
$\Delta\lambda$	Spectral Bandwidth			20		nm
V_F	Static Forward Voltage		1.5	1.65	2	V
α_{VF}	Average Temperature Coefficient of Static Forward Voltage	I_F = 20 mA, T_A = 0°C to 70°C		−1.4		mV/°C
I_R	Static Reverse Current	V_R = 3 V			100	μA
C	Anode-to-Cathode Capacitance	V_R = 0, f = 1 MHz		120		pF

NOTE 2: Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

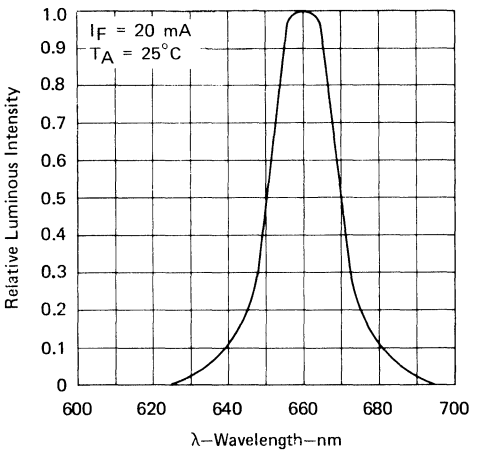


FIGURE 1

RELATIVE LUMINOUS INTENSITY
vs
FREE-AIR TEMPERATURE

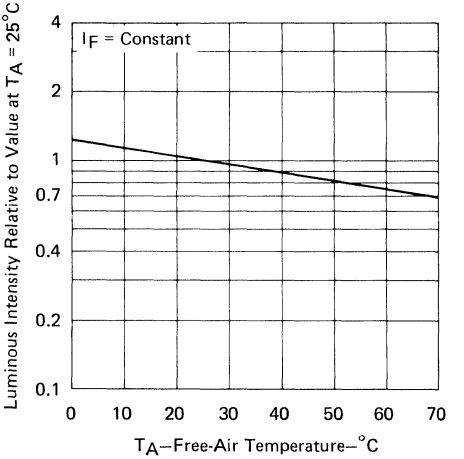


FIGURE 2

RELATIVE LUMINOUS INTENSITY
vs
FORWARD CURRENT

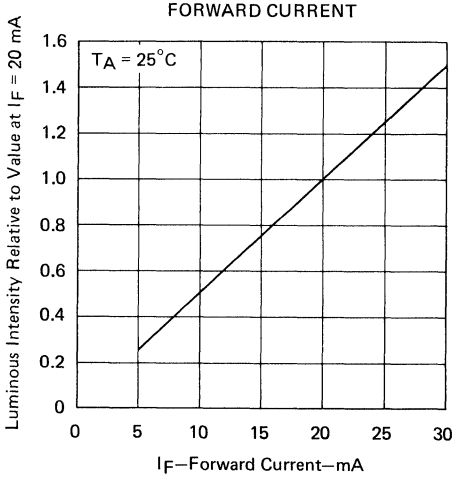


FIGURE 3

FORWARD CONDUCTION CHARACTERISTICS

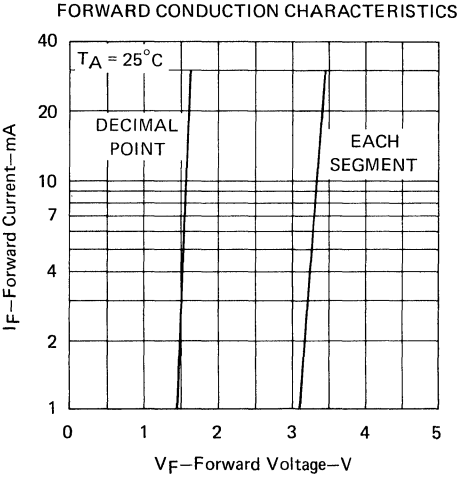
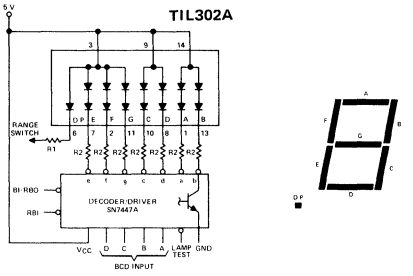


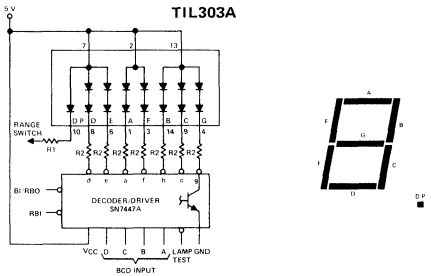
FIGURE 4

TYPICAL APPLICATION DATA

TIL302
TIL302A



TIL303
TIL303A



NOTE: R1 and R2 are selected for desired brightness.

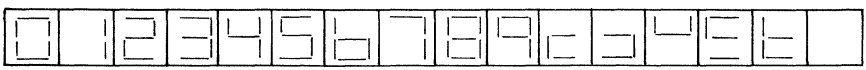
FUNCTION TABLE
SN7447A

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	SEGMENTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	1
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	1
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	1
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	1
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	1
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	1
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	1
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	1
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	1
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	1
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	1
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level (logic 1 in positive logic), L = low level (logic 0 in positive logic), X = irrelevant.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of any other input.
3. When the ripple-blanking input (RBI) and inputs A, B, C, and D are at a low logic level with the lamp test input high, all segment outputs are off and the ripple-blanking output (RBO) of the decoder goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segments are illuminated.



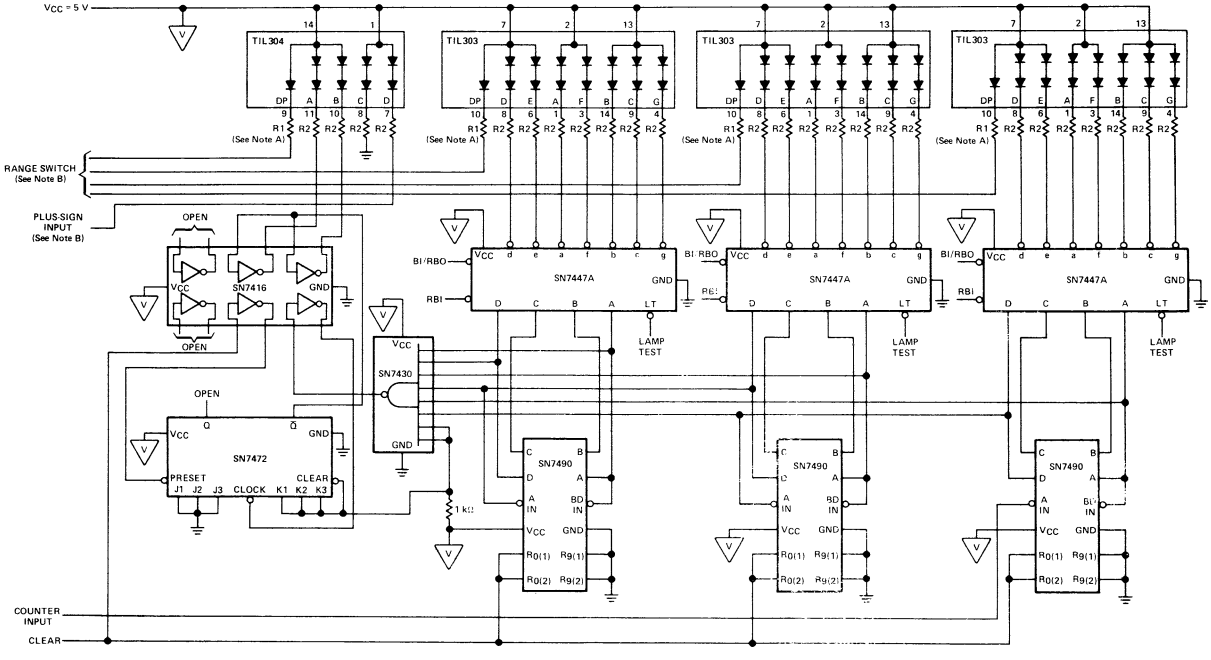
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

NUMERICAL DESIGNATIONS—RESULTANT DISPLAYS

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

The TIL303, TIL303A, TIL304, and TIL304A are used in this application to make a three-digit display with sign, which is capable of 100% overrance ("1" plus three digits). The decimal point is located via an external range switch. The clear function will blank the overflow digit and reset the three digits to zero. Following resetting, input pulses will be counted, decoded, and displayed.



NOTES: A. R1 and R2 are selected for desired brightness.
B. Grounding of any of these lines will illuminate the associated function.

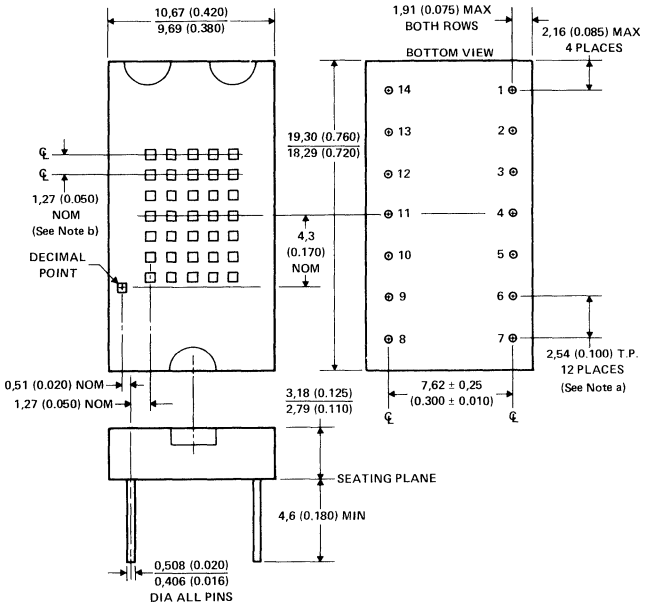
▽ . . . V_{CC} bus

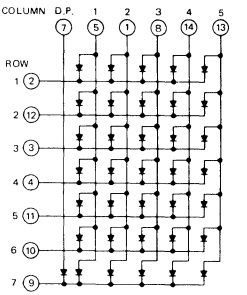
SOLID-STATE DISPLAY WITH RED TRANSPARENT PLASTIC ENCAPSULATION

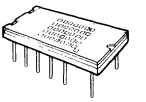
- 7,62-mm (0.300-inch) Character Height
- High Luminous Intensity
- Low Power Requirements
- Wide Viewing Angle
- 5 X 7 Array with X-Y Select and Decimal
- Compatible with USASCII and EBCDIC Codes

mechanical data

This assembly consists of a display chip mounted on a printed circuit board with a red molded plastic body. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.







NOTES: a. The true-position spacing is 2,54 mm (0.100 inch) between lead centerlines. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal position.

b. Vertical and horizontal spacing between centerlines of rows and columns nominally 1,27 mm (0.050 inch).

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CL-37

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Reverse Voltage at 25°C Free-Air Temperature	3 V
Peak Forward Current, Each Diode	100 mA
Average Forward Current (see Note 1):	
Each Diode	10 mA
Total	200 mA
Operating Free-Air Temperature Range	0° to 70°C
Storage Temperature Range	−25°C to 85°C

operating characteristics of each diode at 25°C free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_V	Luminous Intensity (see Note 2)	I_F = 10 mA	40	110		μcd
λ_p	Wavelength at Peak Emission			660		nm
$\Delta\lambda$	Spectral Bandwidth			20		nm
V_F	Static Forward Voltage		1.5	1.65	2	V
α_{VF}	Average Temperature Coefficient of Static Forward Voltage	I_F = 10 mA, T_A = 0°C to 70°C		−1.4		mV/°C
I_R	Static Reverse Current	V_R = 3 V		10		μA
C	Anode-to-Cathode Capacitance	V_R = 0, f = 1 MHz		80		pF

NOTES: 1. This average value applies for any 1-ms period.
2. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.

TYPICAL CHARACTERISTICS

RELATIVE LUMINOUS INTENSITY
vs
FREE-AIR TEMPERATURE

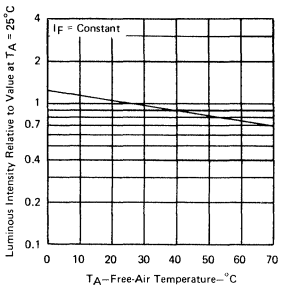


FIGURE 1

RELATIVE LUMINOUS INTENSITY
vs
FORWARD CURRENT

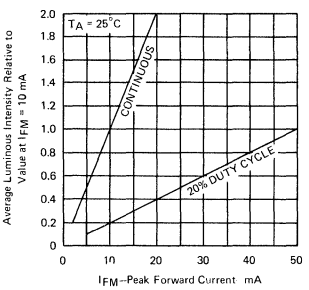


FIGURE 2

FORWARD CONDUCTION
CHARACTERISTICS

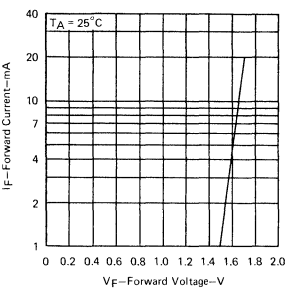


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

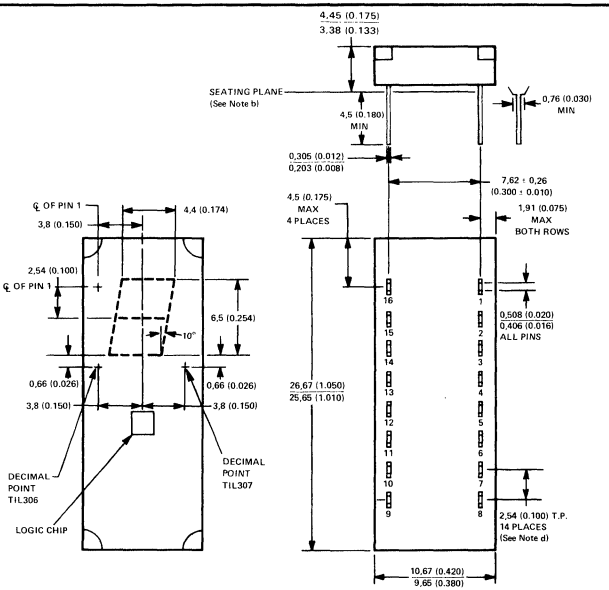
D1034, REVISED JUNE 1982

SOLID-STATE DISPLAYS WITH INTEGRAL TTL MSI CIRCUIT CHIP FOR USE IN ALL SYSTEMS WHERE THE DATA TO BE DISPLAYED IS THE PULSE COUNT

- 6,9-mm (0.270-Inch) Character Height
- High Luminous Intensity
- TIL306 and TIL306A Have Left Decimal
- TIL307 and TIL307A Have Right Decimal
- Easy System Interface
- Wide Viewing Angle
- Internal TTL MSI Chip and Counter, Latch, Decoder, and Driver
- Constant-Current Drive for Light-Emitting Diodes

mechanical data

These assemblies consist of display chips and a TTL MSI chip mounted on a header with either a red molded plastic body for the TIL306 and TIL307 or a red plastic cap for the TIL306A and TIL307A. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.

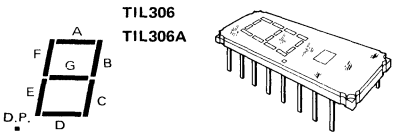


PIN ASSIGNMENTS

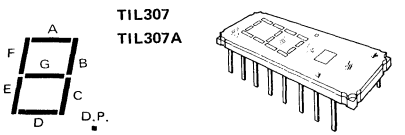
PIN 1	LATCH OUTPUT Q_B (BINARY WEIGHT 2)
PIN 2	LATCH OUTPUT Q_C (BINARY WEIGHT 4)
PIN 3	LATCH OUTPUT Q_D (BINARY WEIGHT 8)
PIN 4	LATCH OUTPUT Q_A (BINARY WEIGHT 1)
PIN 5	LATCH STROBE INPUT
PIN 6	RIPPLE-BLANKING INPUT
PIN 7	MAXIMUM-COUNT OUTPUT
PIN 8	GROUND
PIN 9	PARALLEL COUNT ENABLE INPUT
PIN 10	SERIAL COUNT ENABLE INPUT
PIN 11	RIPPLE-BLANKING OUTPUT
PIN 12	CLEAR INPUT
PIN 13	DECIMAL POINT INPUT
PIN 14	BLANKING INPUT
PIN 15	CLOCK INPUT
PIN 16	SUPPLY VOLTAGE, V_{CC}

NOTES: a. All linear dimensions are in millimeters and parenthetically in inches.
b. Lead dimensions are not controlled above the seating plane.
c. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.
d. The true-position pin spacing is 2,54 mm (0,100 inch) between centerlines. Each centerline is located with 0,26 mm (0,010 inch) of its true longitudinal position relative to pins 1 and 16.
e. On TIL306A and TIL307A devices, the 4 mold indentations are not present.

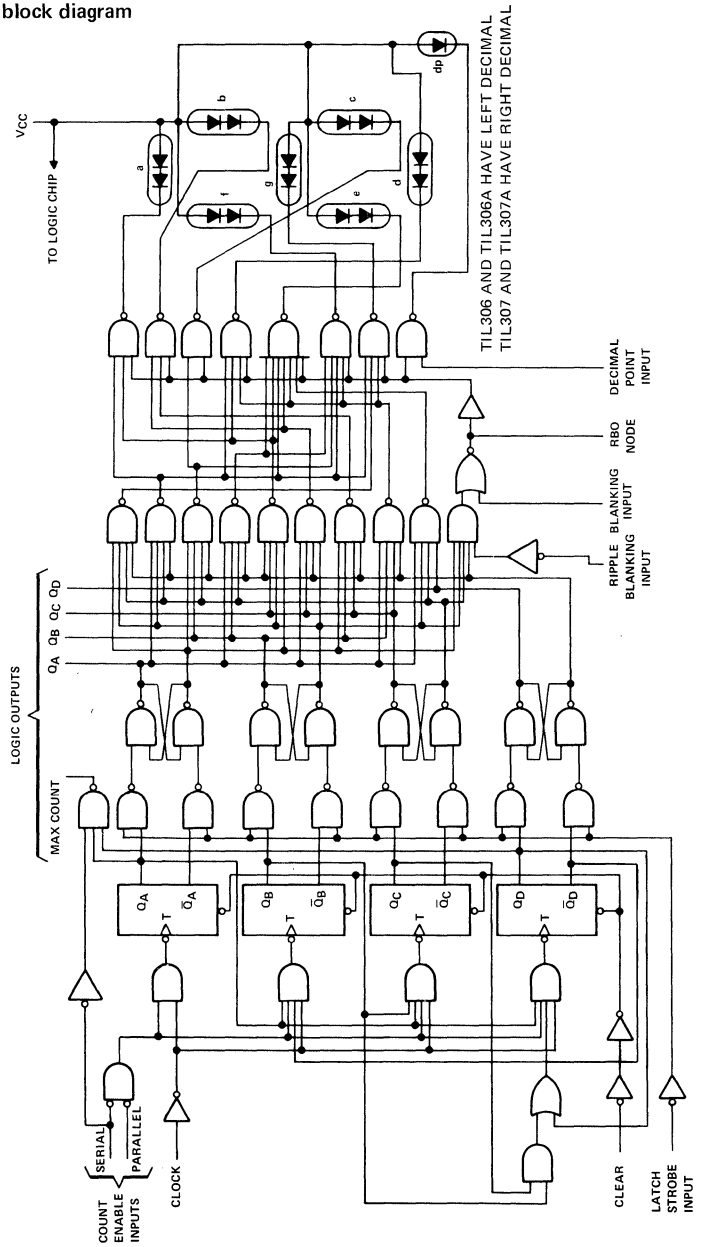
TIL306
TIL306A



TIL307
TIL307A



functional block diagram



SYNCHRONOUS BCD COUNTER, 4-BIT LATCH, DECODER/DRIVER, SEVEN-SEGMENT LED DISPLAY WITH DECIMAL POINT

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description

These internally-driven seven-segment light-emitting-diode (LED) displays contain a BCD counter, a four-bit latch, and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices follows:

FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	12	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	15	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	9	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	10	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	7	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	5	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	4, 1, 2, 3	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	13	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	14	When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	6	When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	11	Supplies ripple-blanking information for the ripple-blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches is BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.

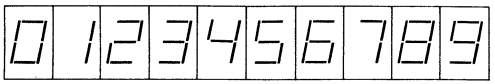
The TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-carry input, actually two internal loads, is rated as one standard series 54/74 load.

description (continued)

The logic outputs, except RBO, are active pull-up, and the latch outputs Q_A, Q_B, Q_C, and Q_D are each capable of driving three standard Series 54/74 loads at a low logic level or six loads at a high logic level while the maximum-count output is capable of driving five Series 54/74 loads at a low logic level or ten loads at a high logic level. The RBO node with passive pull-up serves as a ripple-blanking output with the capability to drive three Series 54/74 loads.

The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately seven milliamperes through each LED segment and decimal point. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 600 milliwatts with all segments on.

The display format is as follows:



The displays may be interconnected to produce an n-digit display with the following features:

- Ripple-blanking input and output for blanking leading or trailing zeroes
- Floating-decimal-point logic capability
- Overriding blanking for suppressing entire display or pulse-modulation of LED brightness
- Dual count-enable inputs for parallel look-ahead and serial ripple logic to build high-speed fully synchronous, multidigit counter systems with no external logic, minimizing total propagation delay from the clock to the last latch output
- Provision for ripple-count cascading between packages
- Positive-edge-triggered synchronous BCD counter
- Parallel BCD data outputs available to drive logic processors or remote slaved displays simultaneously with data being displayed
- Latch strobe input allows counter to operate while a previous data point is displayed
- Reset-to-zero capability with clear input.

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1): Continuous . . . . . 5.5 V
Nonrepetitive Peak, $t_w \leqslant 100$ ms . . . . . 7 V
Input Voltage (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range (See Note 2) . . . . . 0°C to 85°C
Storage Temperature Range . . . . . −25°C to 85°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}			4.75	5	5.25	V
Normalized Fan-Out from Each Output, N (to Series 54/74 Integrated Circuits)	Low Logic Level	Q_A, Q_B, Q_C, Q_D, RBO			3	
		Maximum Count			5	
	High Logic Level	RBO			3	
		Q_A, Q_B, Q_C, Q_D			6	
		Maximum Count			10	
Clock Pulse Duration, $t_{w(clock)}$		High Logic Level	25			ns
		Low Logic Level	55			
Clear Pulse Duration, $t_{w(clear)}$			25			ns
Latch Strobe Pulse Duration, $t_{w(latch\ strobe)}$			45			ns
Setup Time, t_{su}		Serial Carry and Parallel Carry	30			ns
		Clear Inactive State	60			

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

operating characteristics at 25°C case temperature

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_V	Luminous Intensity (See Note 3)	Figure 8	V_{CC} = 5 V	700	1200		μcd
		Decimal Point		40	70		μcd
λ_p	Wavelength at Peak Emission		V_{CC} = 5 V, See Note 4		660		nm
$\Delta\lambda$	Spectral Bandwidth		V_{CC} = 5 V, See Note 4		20		nm
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-Level Output Voltage	RBO	V_{CC} = 4.75 V, I_{OH} = −120 μA	2.4			V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75 V, I_{OH} = −240 μA				
		Maximum Count	V_{CC} = 4.75 V, I_{OH} = −400 μA				
V_{OL}	Low-Level Output Voltage (See Note 5)	Q_A, Q_B, Q_C, Q_D, RBO	V_{CC} = 4.75 V, I_{OL} = 4.8 mA			0.4	V
		Maximum Count	V_{CC} = 4.75 V, I_{OL} = 8 mA				
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-Level Input Current	Serial Carry	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
		RBO Node		−0.12	−0.5		mA
		Other Inputs				20	μA
I_{IL}	Low-Level Input Current	Serial Carry	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
		RBO Node			−1.5	−2.4	
		Other Inputs				−0.8	
I_{OS}	Short-Circuit Output Current	Q_A, Q_B, Q_C, Q_D	V_{CC} = 5.25 V	−9		−27.5	mA
		Maximum Count		−15		−55	
I_{CC}	Supply Current		V_{CC} = 5.25 V, See Note 4		120	200	mA

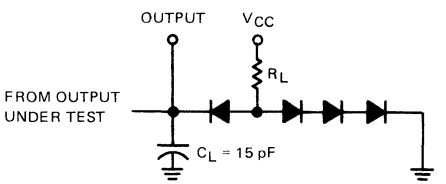
‡All typical values are at V_{CC} = 5 V.

NOTES: 3. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.
4. These parameters are measured with all LED segments and the decimal point on.
5. This parameter is measured with the display blanked.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				12	18		MHz
t_{PLH}	Serial Look-Ahead	Maximum Count	C_L = 15 pF, R_L = 560 Ω, See Figure 1		12		ns
t_{PHL}					23		
t_{PLH}	Clock	Maximum Count			26		ns
t_{PHL}					29		
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D	C_L = 15 pF, R_L = 1.2 kΩ, See Figure 1		28		ns
t_{PHL}					38		
t_{PHL}	Clear	Q_A, Q_B, Q_C, Q_D			57		ns

§f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

LOAD CIRCUIT–FIGURE 1

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

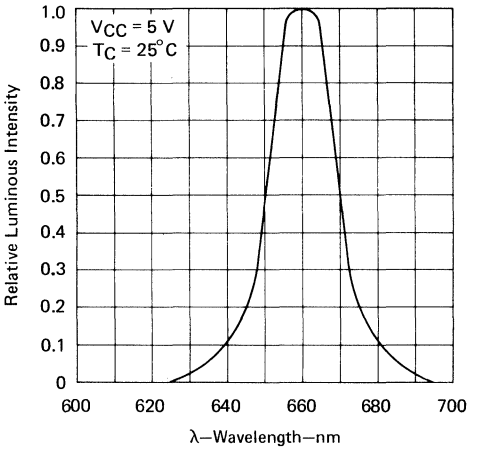


FIGURE 2

RELATIVE LUMINOUS INTENSITY
vs
CASE TEMPERATURE

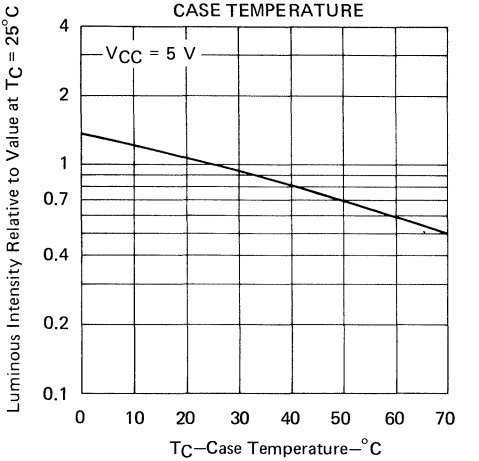


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

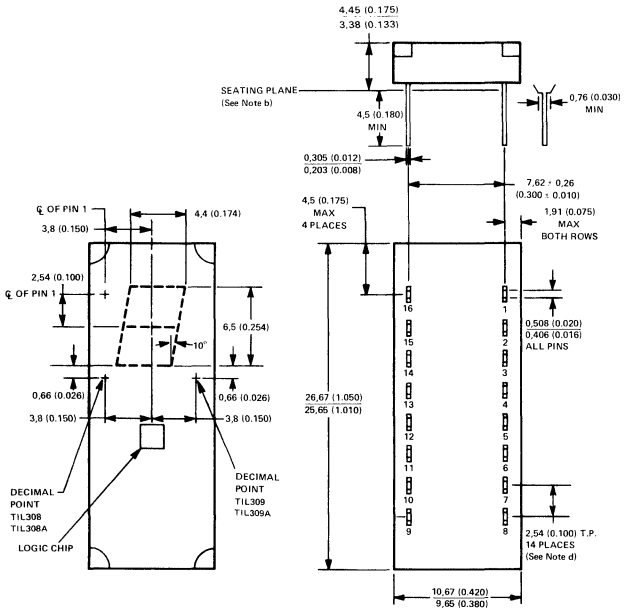
D1096, MARCH 1972—REVISED JUNE 1982

SOLID-STATE DISPLAYS WITH INTEGRAL TTL MSI CIRCUIT CHIP FOR USE IN ALL SYSTEMS REQUIRING A DISPLAY OF BCD DATA

- 6,9-mm (0.270-Inch) Character Height
- TIL308 and TIL308A Have Left Decimal
- TIL309 and TIL309A Have Right Decimal
- Easy System Interface
- Wide Viewing Angle
- Internal TTL MSI Chip with Latch, Decoder, and Driver
- Constant-Current Drive for Light-Emitting Diodes

mechanical data

These assemblies consist of display chips and a TTL MSI chip mounted on a header with either a red molded plastic body for the TIL308 and TIL309 or a red plastic cap for the TIL308A and TIL309A. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.

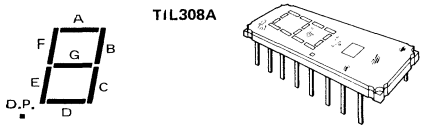


PIN ASSIGNMENTS FOR BOTH TYPES

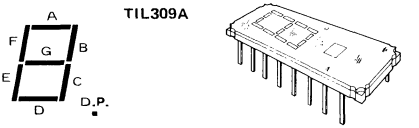
PIN 1	LATCH OUTPUT Q_B (BINARY WEIGHT 2)
PIN 2	LATCH OUTPUT Q_C (BINARY WEIGHT 4)
PIN 3	LATCH OUTPUT Q_D (BINARY WEIGHT 8)
PIN 4	LATCH OUTPUT Q_A (BINARY WEIGHT 1)
PIN 5	LATCH STROBE INPUT
PIN 6	LATCH DATA INPUT C (BINARY WEIGHT 4)
PIN 7	LATCH DATA INPUT D (BINARY WEIGHT 8)
PIN 8	GROUND
PIN 9	NO INTERNAL CONNECTION
PIN 10	LATCH DATA INPUT B (BINARY WEIGHT 2)
PIN 11	BLANKING INPUT
PIN 12	LATCH DATA INPUT DP
PIN 13	LED TEST
PIN 14	LATCH OUTPUT DP
PIN 15	LATCH DATA INPUT A (BINARY WEIGHT 1)
PIN 16	SUPPLY VOLTAGE, V_{CC}

NOTES: a. All linear dimensions are in millimeters and parenthetically in inches.
b. Lead dimensions are not controlled above the seating plane.
c. Centerlines of character segments and decimal points are shown as dashed lines. Associated dimensions are nominal.
d. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located within 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 16.
e. On TIL308A and TIL309A devices, the 4 mold indentations are not present.

TIL308
TIL308A



TIL309
TIL309A



TEXAS INSTRUMENTS
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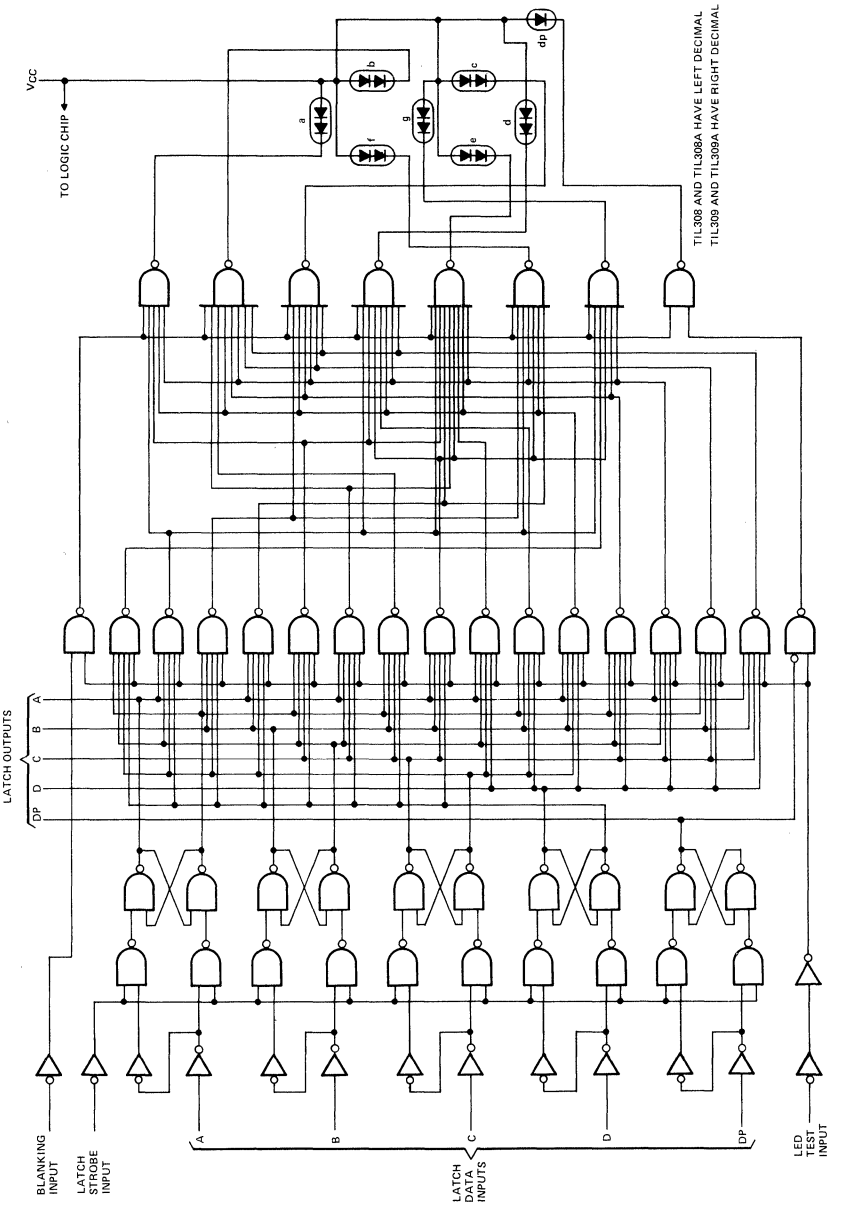
functional block diagram



TEXAS INSTRUMENTS
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description

These internally-driven seven-segment light-emitting-diode (LED) displays contain a five-bit latch and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices follows:

FUNCTION	PIN NO.	DESCRIPTION
LATCH STROBE INPUT	5	When low, the data in the latches follow the data on the latch inputs. When high, the data in the latches are held constant and are unaffected by new data on the latch inputs.
LATCH DATA INPUTS A, B, C, D, DP	15, 10, 6, 7, 12	Data on these inputs are entered into the latches under the control of the latch strobe input. The binary weights of the inputs are: A = 1, B = 2, C = 4, D = 8. DP is decimal point latch data input.
LATCH OUTPUTS Q_A, Q_B, Q_C, Q_D, Q_{DP}	4, 1, 2, 3, 14	The BCD data that drives the decoder is stored in the five latches and is available at these outputs. The binary weights of the outputs are: Q_A = 1, Q_B = 2, Q_C = 4, Q_D = 8. Q_{DP} is decimal point latch output.
BLANKING INPUT	11	When low, will blank (turn off) the entire display. Must be high for normal operation of the display.
LED TEST INPUT	13	When low, will turn on the entire display, overriding the data in the latches and the blanking input. Must be high for normal operation of the display.

FUNCTION TABLE

FUNCTION	LATCH INPUTS						BLANKING INPUT	LED TEST	LATCH OUTPUTS					DISPLAY	
	D	C	B	A	DP	STROBE			Q_D	Q_C	Q_B	Q_A	Q_{DP}	TIL308	TIL309
0	L	L	L	L	L	L	H	H	L	L	L	L	L	0	0
1	L	L	L	H	H	L	H	H	L	L	L	H	H	1	1
2	L	L	H	L	L	L	H	H	L	L	H	L	L	2	2
3	L	L	H	H	H	L	H	H	L	L	H	H	H	3	3
4	L	H	L	L	L	L	H	H	L	H	L	L	L	4	4
5	L	H	L	H	H	L	H	H	L	H	L	H	H	5	5
6	L	H	H	L	L	L	H	H	L	H	H	L	L	6	6
7	L	H	H	H	H	L	H	H	L	H	H	H	H	7	7
8	H	L	L	L	L	L	H	H	H	L	L	L	L	8	8
9	H	L	L	H	H	L	H	H	H	L	L	H	H	9	9
A	H	L	H	L	L	L	H	H	H	L	H	L	L	A	A
MINUS SIGN	H	L	H	H	H	L	H	H	H	L	H	H	H	-	-
C	H	H	L	L	L	L	H	H	H	H	L	L	L	C	C
BLANK	H	H	L	H	H	L	H	H	H	H	L	H	H		
E	H	H	H	L	L	L	H	H	H	H	H	L	L	E	E
F	H	H	H	H	H	L	H	H	H	H	H	H	H	F	F
BLANK	X	X	X	X	X	X	L	H	X	X	X	X	X		
LED TEST	X	X	X	X	X	X	X	L	X	X	X	X	X	8	8

H = high level, L = low level, X = irrelevant.
DP input has arbitrarily been shown activated (high) on every other line of the table.

description (continued)

The TTL MSI circuits contain the equivalent of 78 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input.

Some of the additional features of these displays are as follows:

- Latched BCD and decimal point logic outputs provided to drive logic processors simultaneously with the displayed data
- Minimum number of inputs required . . . 4-line BCD plus decimal point
- Overriding blanking for suppressing entire display or for pulse-modulation of LED brightness
- LED test input to simultaneously turn on all display segments and decimal point
- Can be operated in a real-time mode or latched-update-only mode by use of the latch strobe input
- Displays numbers 0 thru 9 as well as A, C, E, F, or minus sign
- Can be blanked by entry of BCD 13 or by use of the blanking input
- Decimal point controlled independently with decimal-point latch
- Constant-current-source TTL-LED interface for optimum performance.

The latch outputs except Q_{DP} are active pull-up, and each one, except Q_{DP}, is capable of driving three standard Series 54/74 loads. The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately seven milliamperes through each LED segment and decimal point. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 575 milliwatts with all segments on.

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1): Continuous . . . . . 5.5 V
Nonrepetitive Peak, $t_w \leq 100$ ms . . . . . 7 V
Input Voltage (See Note 1) . . . . . 5.5 V
Operating Case Temperature Range (See Note 2) . . . . . 0°C to 85°C
Storage Temperature Range . . . . . −25°C to 85°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}			4.75	5	5.25	V
Normalized Fan-out from each output, N (to Series 54/74 Integrated Circuits)	Low Logic Level	Q_{DP}			1	
		Q_A, Q_B, Q_C, Q_D			3	
	High Logic Level	Q_{DP}			3	
		Q_A, Q_B, Q_C, Q_D			6	
Latch Strobe Pulse Duration, t_w			45			ns
Setup Time, t_{su}			60			ns
Hold Time, t_h			0			ns

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

operating characteristics at 25°C case temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_v	Luminous Intensity (See Note 3)	Figure B	V_{CC} = 5 V	700	1200		μcd
		Decimal Point		40	70		
λp	Wavelength at Peak Emission		V_{CC} = 5 V, See Note 4		660		nm
Δλ	Spectral Bandwidth		V_{CC} = 5 V, See Note 4		20		nm
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
V_{OH}	High-Level Output Voltage	Q_{DP}	V_{CC} = 4.75 V, I_{OH} = −120 μA	2.4			V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75 V, I_{OH} = −240 μA				
V_{OL}	Low-Level Output Voltage (See Note 5)	Q_{DP}	V_{CC} = 4.75 V, I_{OL} = 1.6 mA			0.4	V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75 V, I_{OL} = 4.8 mA				
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-Level Input Current		V_{CC} = 5.25 V, V_I = 2.4 V			20	μA
I_{IL}	Low-Level Input Current		V_{CC} = 5.25 V, V_I = 0.4 V			−0.8	mA
I_{OS}	Short-Circuit Output Current	Q_A, Q_B, Q_C, Q_D	V_{CC} = 5.25 V	−9		−27.5	mA
		Q_{DP}		−1		−3.2	
I_{CC}	Supply Current		V_{CC} = 5.25 V, All Inputs at 0 V		115	180	mA

†All typical values are at V_{CC} = 5 V.

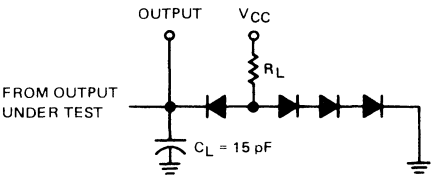
NOTES: 3. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.
4. These parameters are measured with all LED segments and the decimal point on.
5. This parameter is measured with the display blanked.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C, D, DP	$Q_A, Q_B, Q_C, Q_D, Q_{DP}$	C_L = 15 pF, R_L = 1.2 kΩ, See Figure 1		35		ns
t_{PHL}					40		ns

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. Measurements made with latch strobe input grounded.

LOAD CIRCUIT–FIGURE 1

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

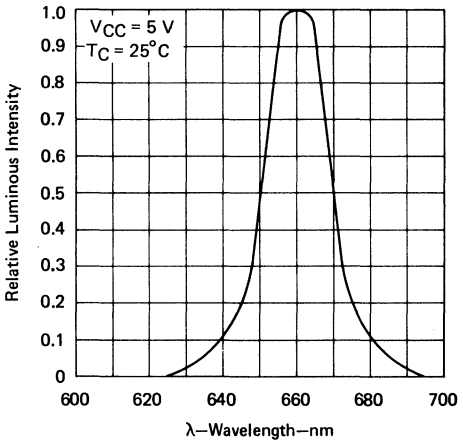


FIGURE 2

RELATIVE LUMINOUS INTENSITY
vs
CASE TEMPERATURE

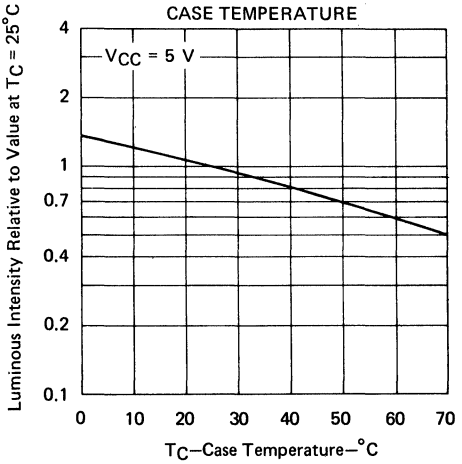


FIGURE 3

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

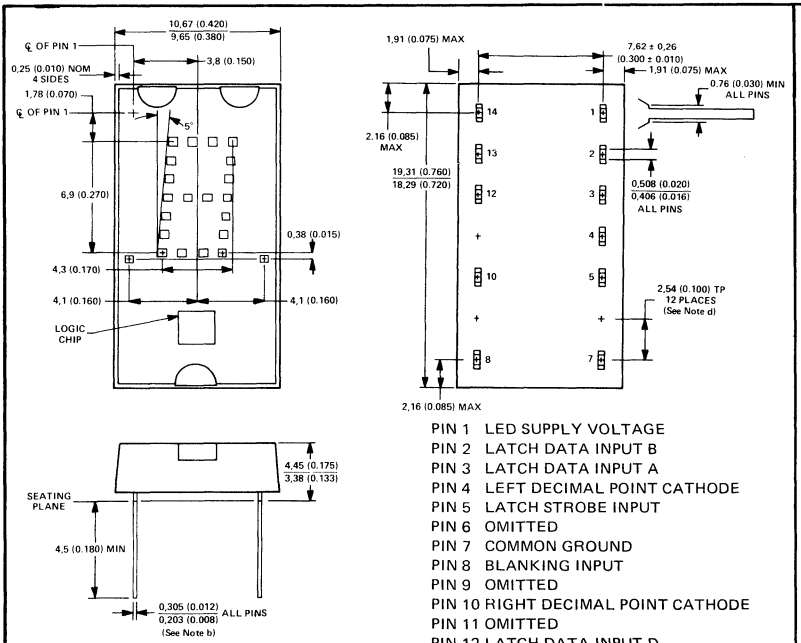
D1176, MARCH 1972—REVISED APRIL 1987

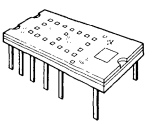
SOLID-STATE HEXADECIMAL DISPLAY WITH INTEGRAL TTL CIRCUIT TO ACCEPT, STORE, AND DISPLAY 4-BIT BINARY DATA

- 7,62-mm (0.300-Inch) Character Height
- High Brightness
- Left-and-Right-Hand Decimals
- Separate LED and Logic Power Supplies May Be Used
- Wide Viewing Angle
- Internal TTL MSI Chip with Latch, Decoder, and Driver
- Operates from 5-Volt Supply
- Constant-Current Drive for Hexadecimal Characters
- Easy System Interface

mechanical data

These assemblies consist of display chips and a TTL MSI chip mounted on a header with either a red molded plastic body for the TIL311 or a red plastic cap for the TIL311A. Multiple displays may be mounted on 11,43-mm (0.450-inch) centers.





PIN 1 LED SUPPLY VOLTAGE
PIN 2 LATCH DATA INPUT B
PIN 3 LATCH DATA INPUT A
PIN 4 LEFT DECIMAL POINT CATHODE
PIN 5 LATCH STROBE INPUT
PIN 6 OMITTED
PIN 7 COMMON GROUND
PIN 8 BLANKING INPUT
PIN 9 OMITTED
PIN 10 RIGHT DECIMAL POINT CATHODE
PIN 11 OMITTED
PIN 12 LATCH DATA INPUT D
PIN 13 LATCH DATA INPUT C
PIN 14 LOGIC SUPPLY VOLTAGE, V_{CC}

NOTES: a. All linear dimensions are in millimeters and parenthetically in inches.
b. Lead dimensions are not controlled above the seating plane.
c. Centerlines of character seqments and decimal points are shown as dashed lines. Associated dimensions are nominal.
d. The true-position pin spacing is 2,54 mm (0.100 inch) between centerlines. Each centerline is located within 0,26 mm (0.010 inch) of its true longitudinal position relative to pins 1 and 14.
e. On TIL311A devices, the 3 mold indentations are not present.

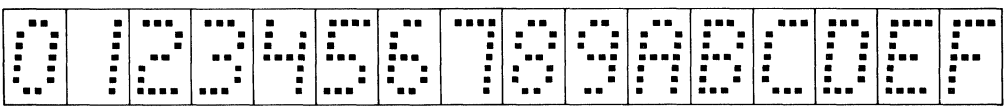
description

This hexadecimal display contains a four-bit latch, decoder, driver, and 4 X 7 light-emitting-diode (LED) character with two externally-driven decimal points in a 14-pin package. A description of the functions of the inputs of this device follows.

FUNCTION	PIN NO.	DESCRIPTION
LATCH STROBE INPUT	5	When low, the data in the latches follow the data on the latch data inputs. When high, the data in the latches will not change. If the display is blanked and then restored while the enable input is high, the previous character will again be displayed.
BLANKING INPUT	8	When high, the display is blanked regardless of the levels of the other inputs. When low, a character is displayed as determined by the data in the latches. The blanking input may be pulsed for intensity modulation.
LATCH DATA INPUTS (A, B, C, D)	3, 2, 13, 12	Data on these inputs are entered into the latches when the enable input is low. The binary weights of these inputs are A = 1, B = 2, C = 4, D = 8.
DECIMAL POINT CATHODES	4, 10	These LEDs are not connected to the logic chip. If a decimal point is used, an external resistor or other current-limiting mechanism must be connected in series with it.
LED SUPPLY	1	This connection permits the user to save on regulated V_{CC} current by using a separate LED supply, or it may be externally connected to the logic supply (V_{CC}).
LOGIC SUPPLY (V_{CC})	14	Separate V_{CC} connection for the logic chip.
COMMON GROUND	7	This is the negative terminal for all logic and LED currents except for the decimal points.

The LED driver outputs are designed to maintain a relatively constant on-level current of approximately five milliamperes through each of the LED's forming the hexadecimal character. This current is virtually independent of the LED supply voltage within the recommended operating conditions. Drive current varies slightly with changes in logic supply voltage resulting in a change in luminous intensity as shown in Figure 2. This change will not be noticeable to the eye. The decimal point anodes are connected to the LED supply; the cathodes are connected to external pins. Since there is no current limiting built into the decimal point circuits, this must be provided externally if the decimal points are used.

The resultant displays for the values of the binary data in the latches are as shown below.



TEXAS INSTRUMENTS
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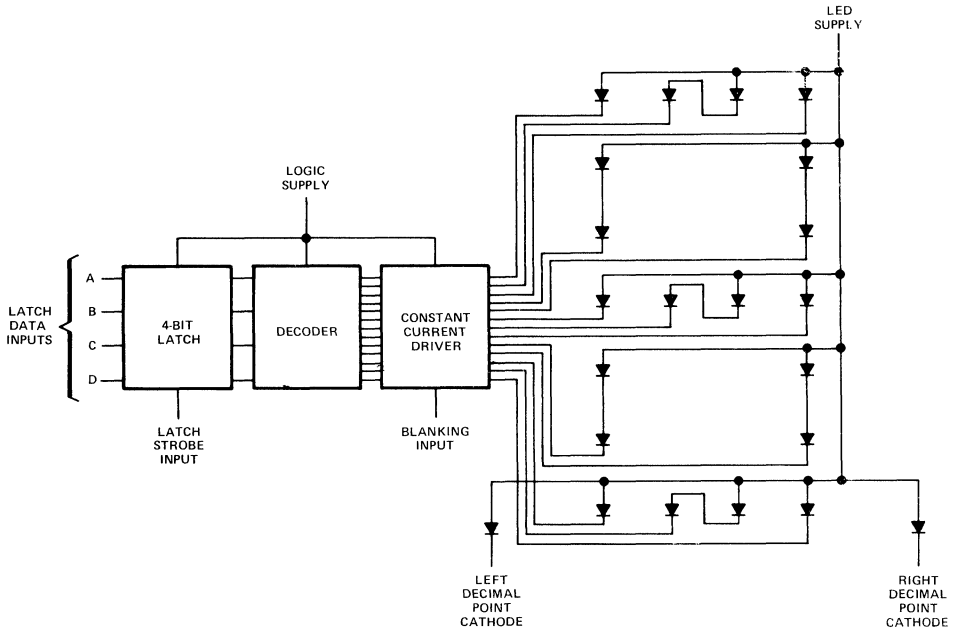
functional block diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Logic Supply Voltage, V_{CC} (See Note 1)	7 V
LED Supply Voltage (See Note 1)	7 V
Input Voltage (Pins 2, 3, 5, 8, 12, 13; See Note 1)	5.5 V
Decimal Point Current	20 mA
Operating Case Temperature Range (See Note 2)	0°C to 85°C
Storage Temperature Range	−25°C to 85°C

NOTES: 1. Voltage values are with respect to common ground terminal.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit. Forced-air cooling may be required to maintain this temperature.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic Supply Voltage, V_{CC}	4.5	5	5.5	V
LED Supply Voltage, V_{LED}	4	5	5.5	V
Decimal Point Current, $I_{F(DP)}$		5		mA
Latch Strobe Pulse Duration, t_w	40			ns
Setup Time, t_{su}	50			ns
Hold Time, t_h	40			ns

operating characteristics at 25°C case temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_v	Luminous Intensity (See Note 3)	Average Per Character LED	V_{CC} = 5 V, V_{LED} = 5 V, See Note 4	35	100		μcd
		Each decimal	$I_{F(DP)}$ = 5 mA	35	100		μcd
λ_p	Wavelength at Peak Emission		V_{CC} = 5 V, V_{LED} = 5 V,		660		nm
$\Delta\lambda$	Spectral Bandwidth		$I_{F(DP)}$ = 5 mA, See Note 5		20		nm
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = 4.75 V, I_I = −12 mA			−1.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}	High-Level Input Current		V_{CC} = 5.5 V, V_I = 2.4 V			40	μA
I_{IL}	Low-Level Input Current		V_{CC} = 5.5 V, V_I = 0.4 V			−1.6	mA
I_{CC}	Logic Supply Current		V_{CC} = 5.5 V, V_{LED} = 5.5 V,		60	90	mA
I_{LED}	LED Supply Current		$I_{F(DP)}$ = 5 mA, All inputs at 0 V		45	90	mA

NOTES: 3. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on Illumination) eye-response curve.

4. This parameter is measured with 8 displayed, then again with blank displayed.
5. These parameters are measured with 8 displayed.

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

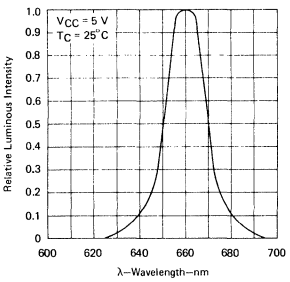


FIGURE 1

RELATIVE LUMINOUS INTENSITY vs LOGIC SUPPLY VOLTAGE

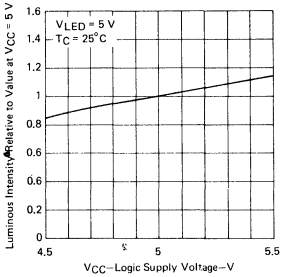


FIGURE 2

RELATIVE LUMINOUS INTENSITY vs CASE TEMPERATURE

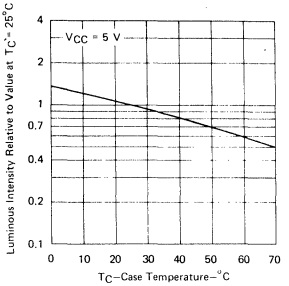


FIGURE 3

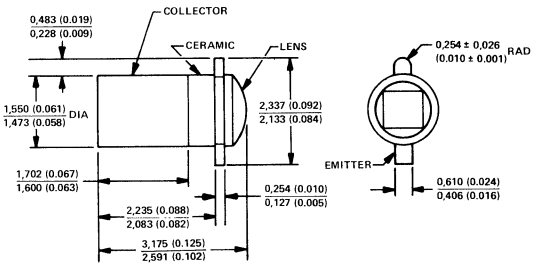
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D974, MARCH 1972—REVISED APRIL 1987

JEDEC-REGISTERED VERSIONS OF TIL601 THRU TIL604

- Recommended for Application in Character Recognition, Tape and Card Readers, Velocity Indicators, and Encoders
- Unique Package Design Allows for Assembly into Printed Circuit Boards

*mechanical data



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FOUR TIMES ACTUAL SIZE

*absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-Emitter Voltage	50 V
Emitter-Collector Voltage	7 V
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 1)	50 mW
Operating Case Temperature Range	−65°C to 125°C
Storage Temperature Range	−65°C to 150°C
Soldering Temperature (10 seconds)	240°C

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, E_e = 0	ALL	50			V
$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 100 μA, E_e = 0	ALL	7			V
I_D	Dark Current	V_{CE} = 30 V, E_e = 0	ALL			25	nA
		V_{CE} = 30 V, E_e = 0, T_C = 100°C	ALL		1		μA
I_L	Light Current	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 2	1N5722	0.5		3	mA
			1N5723	2		5	
			1N5724	4		8	
			1N5725	7			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 0.4 mA, E_e = 20 mW/cm², See Note 2	ALL		0.15		V

NOTES: 1. Derate linearly to 125°C at the rate of 0.5 mW/°C.
2. Irradiance (E_e) is the radiant power per unit area incident upon a surface. For this measurement the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

*JEDEC registered data. This data sheet contains all applicable JEDEC registered data in effect at the time of publication.

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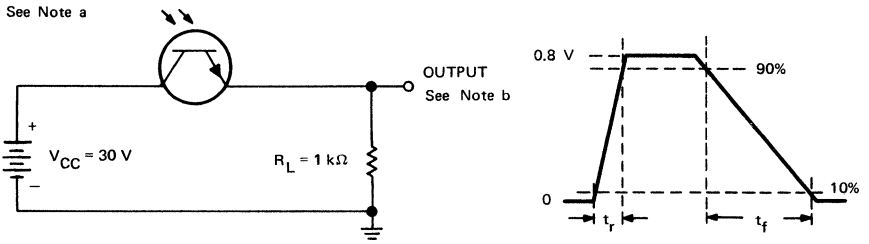
*switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r Rise Time	V_{CC} = 30 V, I_L = 800 μA,		1.5	2.5	μs
t_f Fall Time	R_L = 1 kΩ, See Figure 1		15	25	

*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

OUTPUT VOLTAGE WAVEFORM

FIGURE 1

NOTES: a. Input irradiance is supplied by a pulsed xenon bulb source. Incident irradiation is adjusted for I_L = 800 μA.

b. Output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 25$ ns, $R_{in} \geq 1$ MΩ, $C_{in} \leq 20$ pF.

*JEDEC registered data

TYPICAL CHARACTERISTICS

COUPLING CHARACTERISTICS
vs
OF 1N5723 WITH TIL23 OR TIL24

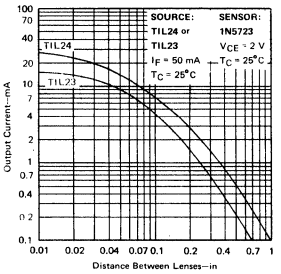


FIGURE 2

RELATIVE OUTPUT
vs
CASE TEMPERATURE OF SOURCE AND SENSOR

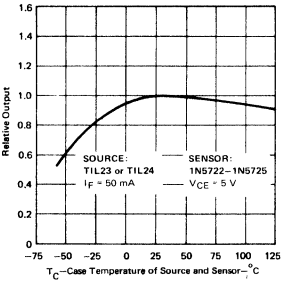


FIGURE 3

NORMALIZED LIGHT CURRENT
vs
ANGULAR DISPLACEMENT

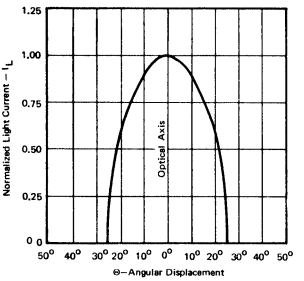


FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

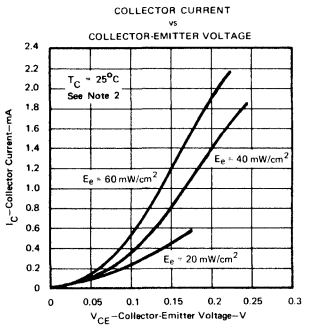


FIGURE 5

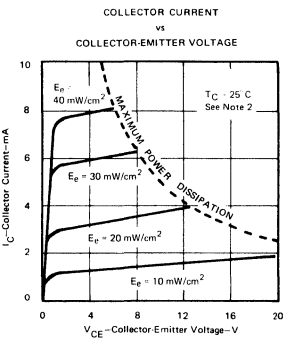


FIGURE 6

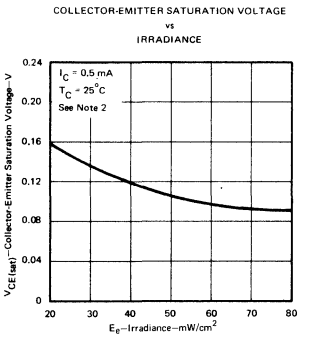


FIGURE 7

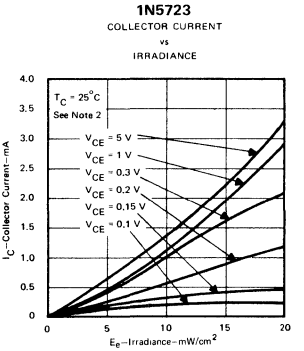


FIGURE 8

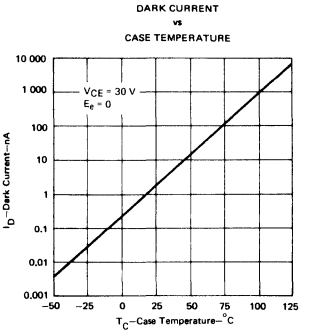


FIGURE 9

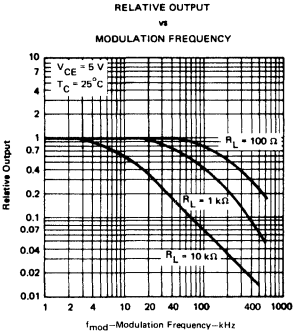


FIGURE 10

NOTE 2: Irradiance (E_e) is the radiant power per unit area incident upon a surface. For this measurement the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL CHARACTERISTICS

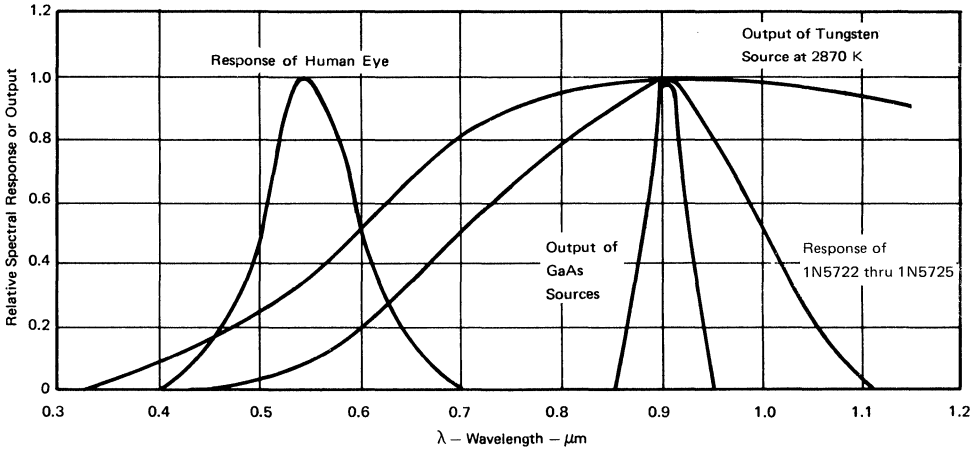


FIGURE 11

TEXAS INSTRUMENTS CUSTOMIZED OPTOELECTRONIC ARRAYS

The 1N5722 through 1N5725 series is available mounted in printed circuit boards for custom-designed array or matrix applications. The array is a complete unit, without the problems associated with small, difficult-to-handle components. These arrays can be designed for punched-card or tape readers, position indicators, pattern and character recognition, shaft encoders, and many other special applications.

Texas Instruments custom-array techniques offer many advantages:

- The arrays are pre-assembled and tested, ready for installation.
- Custom arrays can be manufactured in almost any configuration to allow maximum design flexibility.
- Sensitivity across an entire array will be matched to within 50%.
- GaAs sources can be furnished to give complete solid-state matched sets for specific applications.
- Arrays with components firmly soldered into place on both sides of a printed circuit board are more rugged than individually wired sensing devices.

Specifying optoelectronic arrays is easy; all that is required is a print of the array and the desired specifications.

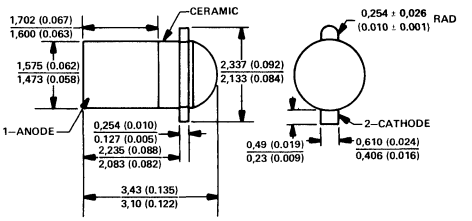
TI sales engineers will assist in developing specifications for special applications.

D2132, FEBRUARY 1970—REVISED APRIL 1987

DESIGNED TO EMIT NEAR-INFRARED RADIATION WHEN FORWARD BIASED

- **Output Spectrally Compatible with Silicon Sensors**
- **High Power Efficiency**
- **High Power Output**
- **Small Size Permits Matrix Assembly Directly into Printed Circuit Boards**
- **High Radiant Intensity**
- **TIL24HR2* Includes High-Reliability Processing and Lot Acceptance (Refer to TIL24HR2 for Summary of Processing)**

mechanical data



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4 TIMES ACTUAL SIZE

absolute maximum ratings

Reverse Voltage at 25°C Case Temperature	2 V
Continuous Forward Current at 25°C Case Temperature (See Note 1)	100 mA
Operating Case Temperature Range	−65°C to 125°C
Storage Temperature Range	−65°C to 150°C
Soldering Temperature (10 seconds)	240°C

*All electrical and mechanical specifications for the TIL24 also apply for TIL24HR2.

NOTE 1: Derate linearly to 125°C case temperature at the rate of 1 mA/°C. For pulsed operation at higher currents, see Figures 8 and 9.

operating characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TIL23			TIL24			TIL25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
P_O	Radiant Power Output	I_F = 50 mA	0.4			1			0.75			mW
λ_p	Wavelength at Peak Emission			940			940			940		nm
$\Delta\lambda$	Spectral Bandwidth			50			50			50		nm
θ_{HI}	Half-Intensity Beam Angle			35°			35°			35°		
V_F	Static Forward Voltage			1.25	1.5			1.5			1.5	V

TYPICAL CHARACTERISTICS

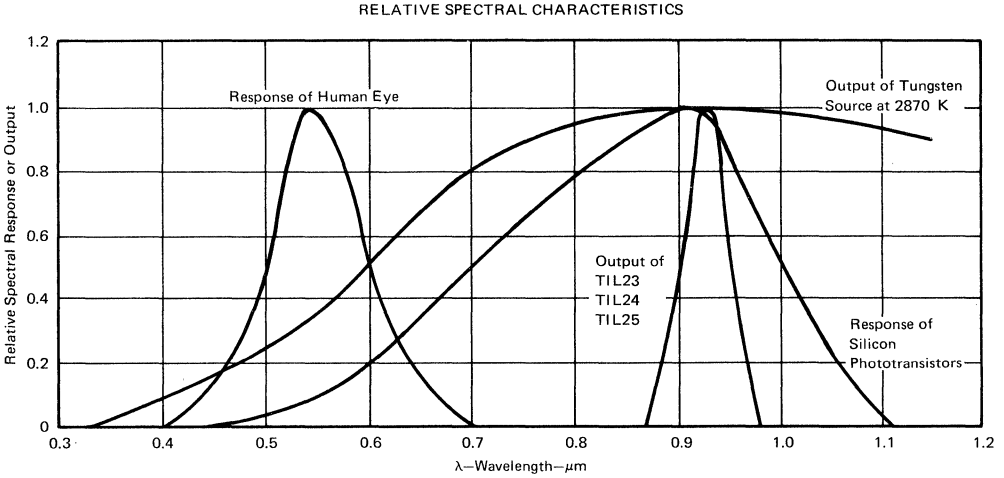


FIGURE 1

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

RELATIVE PHOTON INTENSITY
vs
ANGULAR DISPLACEMENT

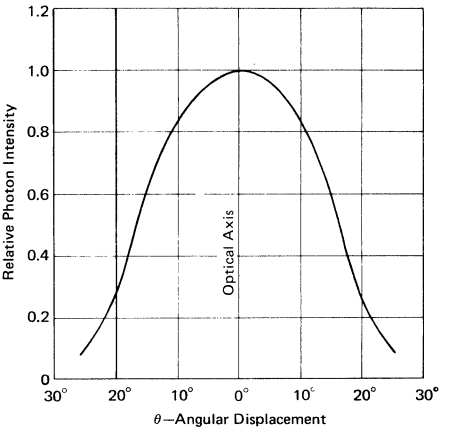


FIGURE 2

RELATIVE POWER OUTPUT
vs
CASE TEMPERATURE

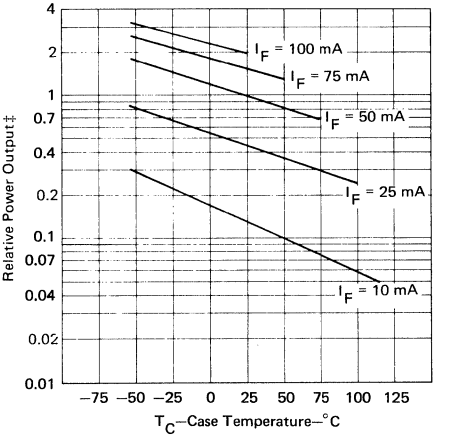


FIGURE 3

CHANGE IN WAVELENGTH OF PEAK INTENSITY
vs
CASE TEMPERATURE

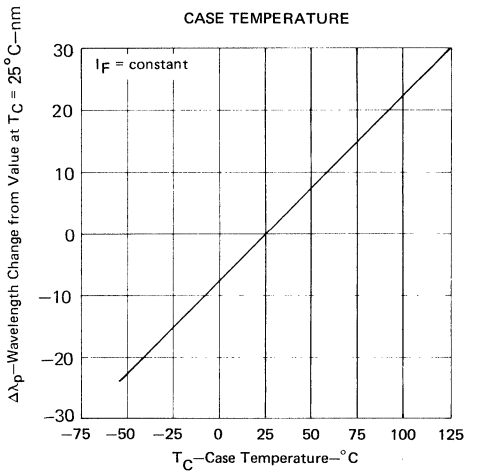


FIGURE 4

RELATIVE POWER OUTPUT
vs
FORWARD CURRENT

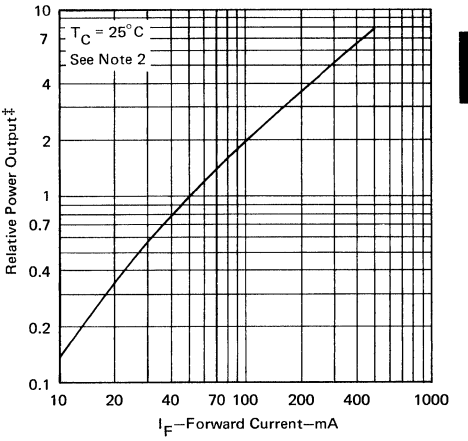


FIGURE 5

NOTE 2: These parameters must be measured using pulse techniques: t_w = 0.04 ms, duty cycle ≤ 10%.
‡Normalized to output at I_F = 50 mA, T_C = 25°C.

TYPICAL CHARACTERISTICS

TIL23

FORWARD CONDUCTION CHARACTERISTICS

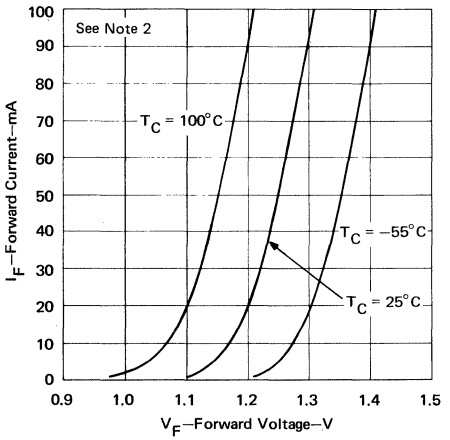


FIGURE 6

COUPLING CHARACTERISTICS OF TIL23, TIL24, AND TIL25 WITH TIL602

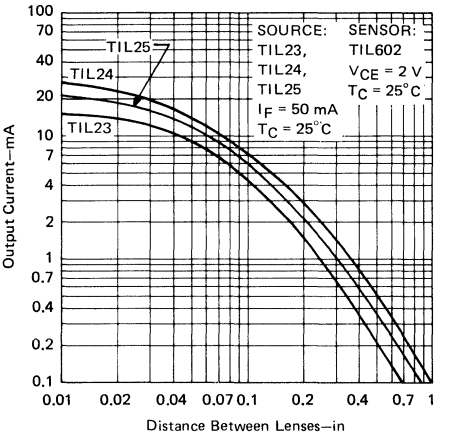


FIGURE 7

NOTE 2: These parameters must be measured using pulse techniques: t_w = 0.04 ms, duty cycle ⩽ 10%.

THERMAL CHARACTERISTICS

MAXIMUM PULSE WIDTH
vs
FORWARD CURRENT

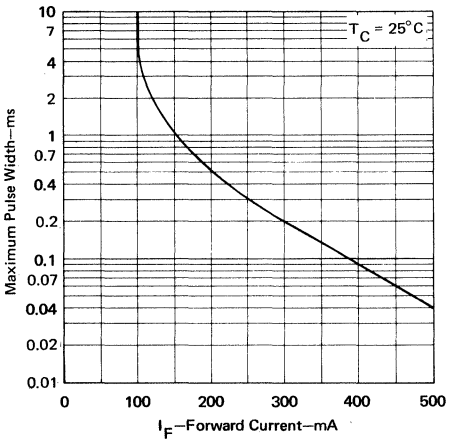


FIGURE 8

MAXIMUM DUTY CYCLE
vs
FORWARD CURRENT

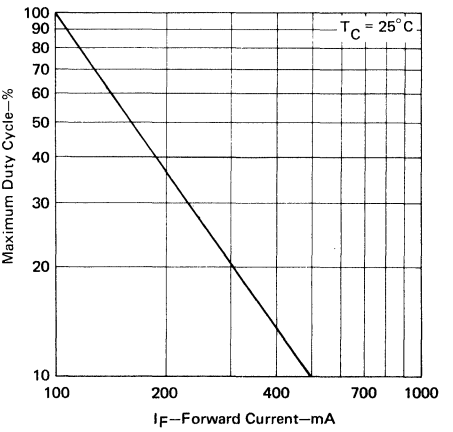


FIGURE 9

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **This processing applies only to devices ordered under the part number TIL24HR2**
- **For electrical and mechanical specifications, refer to TIL24 data sheet**

This processing and lot acceptance follow the sequence of tests in MIL-S-19500 for JANTX types. This is not to be construed to be a JANTX-qualified part. A detail specification is available upon request through your TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
LITERATURE RESPONSE CENTER
P.O. Box 809066
Dallas, Texas 75380-9066

TEST	MIL-STD-750 TEST METHOD
100% Processing	
Storage: T_A = 125°C, t = 24 h	1032
Temperature Cycle: −55°C to 125°C, 10 cycles	1051
Constant Acceleration: 20,000 G, Y_1 axis	2006
Power Burn-in: I_F = 50 mA, t = 168 h	1039
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
External Visual	2071
Product Acceptance	
Group A: LTPD = 5	
External Visual	2071
Electrical: T_A = 25°C	per detail spec
Group B-1: LTPD = 15	
Solderability	2026
Group B-2: LTPD = 10	
Thermal Shock	1051 Cond. B-1
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
Group B-3: LTPD = 5	
Steady-State Operating Life: t = 340 h	1027
Group B-4:	
Decap, Internal Visual; Design Verification	
1 Device/0 Failure	2075
Bond Strength LTPD = 20 (C = 0)	2037 Cond. A
Group B-5: Not Applicable	
Group B-6: LTPD = 7	
High-Temperature Life (Nonoperating) t = 340 h	1032

TEST	MIL-STD-750 TEST METHOD
(Group C Tests are run on one lot every six months)	
Group C-1: LTPD = 15	
Physical Dimensions	2066
Group C-2: LTPD = 10	
Thermal Shock (Glass Strain)	1056 Cond. A
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
Moisture Resistance	1021
External Visual	2071
Group C-3: LTPD = 10	
Shock: 1500 G	2016
Vibration: 50 G	2056
Acceleration: 2000 G (X_1, Y_1, Y_2 axis)	2006
Group C-4: LTPD = 15	
Salt Atmosphere	1041
Group C-5: Not Applicable	
Group C-6: λ = 10	
Steady-State Operating Life: t = 1000 h	1026

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D1092, SEPTEMBER 1971—REVISED SEPTEMBER 1989

TIL131 . . . 9-ELEMENT GALLIUM ARSENIDE IRED ARRAY

TIL132 . . . 9-ELEMENT PHOTOTRANSISTOR ARRAY

TIL133 . . . 9-CHANNEL PAIR

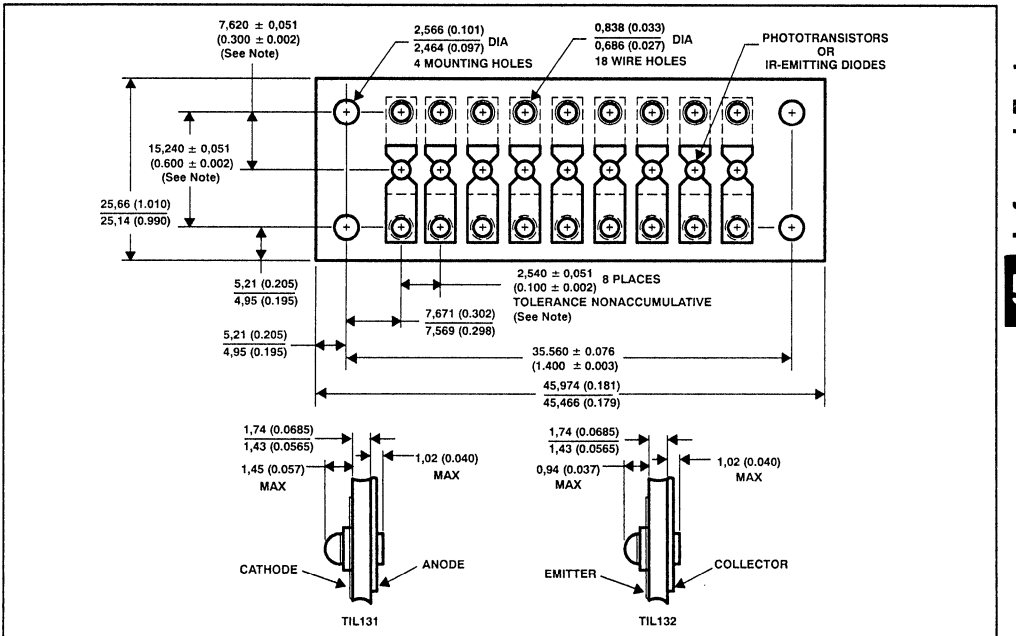
- **Center-to-Center Spacing of 2,54 mm (0.100 inch) for Tape Reading**
- **Reliable Solid-State Components**
- **IREDs Eliminate Lamp-Filament-Sag Problems**
- **Spectrally Matched for Improved Performance**
- **Printed Circuit Board Construction Allows Precise Alignment**

description

The TIL131 is an array of nine TIL23 gallium arsenide infrared-emitting diodes mounted in a printed circuit board. The TIL132 is an array of nine selected LS600 phototransistors. The TIL133 is a pair of selected arrays comprising a TIL131 and TIL132 and offering specified channel performance.

mechanical data

The printed circuit board material is glass-base NEMA standard FR-4, class II, 0.6-kg/m^2 (2-oz/ft^2) copper-clad on each side. The approximate weight of the TIL131 and TIL132 is 3.7 grams each.



SIDE VIEWS OF ACTIVE ELEMENTS

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: The tolerances shown for these dimensions apply to location of the mounting holes and the active elements only. Tolerance of ± 0,13 mm (0.005 inch) applies for location dimensions of the wire holes.

TIL131 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Reverse voltage ..... 2 V
Continuous forward current at (or below) 25°C free-air temperature (see Note 1) ..... 100 mA
Operating free-air temperature range ..... −65°C to 125°C
Storage temperature range ..... −65°C to 150°C
Soldering temperature (10 seconds) ..... 240°C

NOTE 1: Derate linearly to 125°C free-air temperature at the rate of 1 mW/°C.

TIL131 operating characteristics of each element at 25°C free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Radiant power output	I_F = 50 mA	0.4		1	mW
λ_p	Wavelength at peak emission			930		nm
$\Delta\lambda$	Spectral bandwidth			50		nm
θ_{HI}	Half-intensity beam angle			35°		
V_F	Static forward voltage			1.25	1.5	V

TIL132 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage ..... 50 V
Emitter-collector voltage ..... 7 V
Continuous device dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 50 mW
Operating free-air temperature range ..... −65°C to 125°C
Storage temperature range ..... −65°C to 150°C
Soldering temperature (10 seconds) ..... 240°C

NOTE 2: Derate linearly to 125°C free-air temperature at the rate of 0.5 mW/°C.

TIL132 electrical characteristics at 25°C free-air temperature

individual element characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 100 μA, E_e = 0	50			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage	I_E = 100 μA, E_e = 0	7			V
I_D	Dark current	V_{CE} = 30 V, E_e = 0			100	nA
I_L	Light current	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 3	2		12	mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 0.4 mA, E_e = 20 mW/cm², See Note 3		0.15		V

element matching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\frac{I_L min}{I_L max}$	Light current matching factor	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 3	0.5			

NOTE 3: Irradiance (E_e) is the radiant power per unit area incident upon a surface. For this measurement, the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TIL133 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Maximum ratings of TIL131 and TIL132 apply.

TIL133 electrical characteristics at 25°C free-air temperature

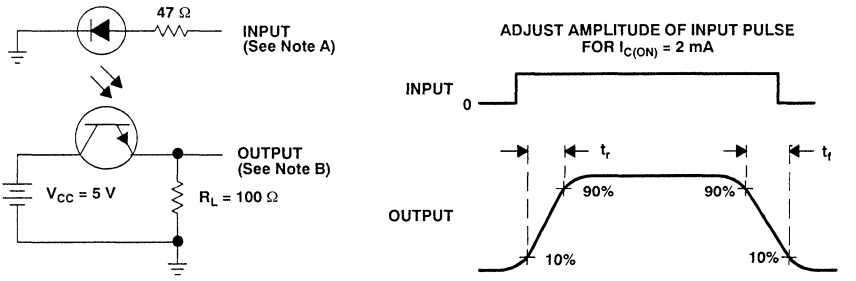
PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_C	Output collector current	I_F = 50 mA,	V_{CE} = 5 V	2.5	4	10	mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_F = 50 mA,	I_C = 2 mA		0.4	0.7	V

TIL133 switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 5 V,	$I_{C(on)}$ = 2 mA,		1.5		μs
t_f	Fall time	R_L = 100 Ω,	See Figure 1		1.5		μs

† These parameters are measured at a lens-to-lens distance of 0.100 inch.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, t_r ≤ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL133
COUPLING CHARACTERISTICS

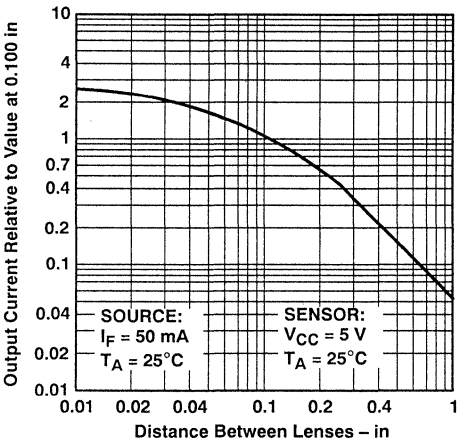


FIGURE 2

TIL131
FORWARD CONDUCTION CHARACTERISTICS

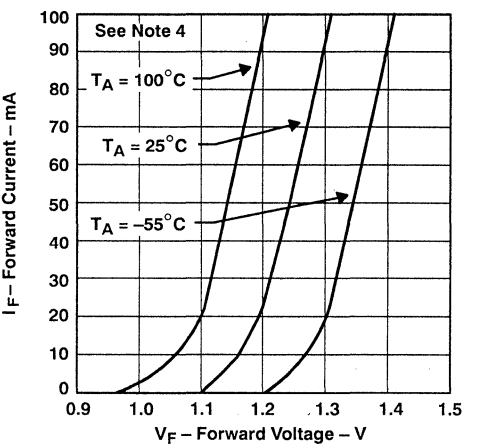


FIGURE 3

TIL131
RELATIVE POWER OUTPUT
VS
FORWARD CURRENT

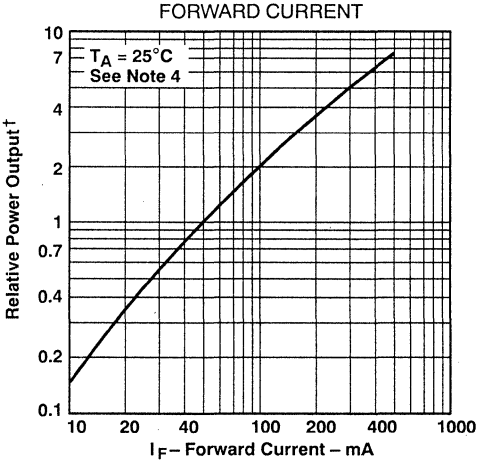


FIGURE 4

TIL131
RELATIVE PHOTON INTENSITY
VS
ANGULAR DISPLACEMENT

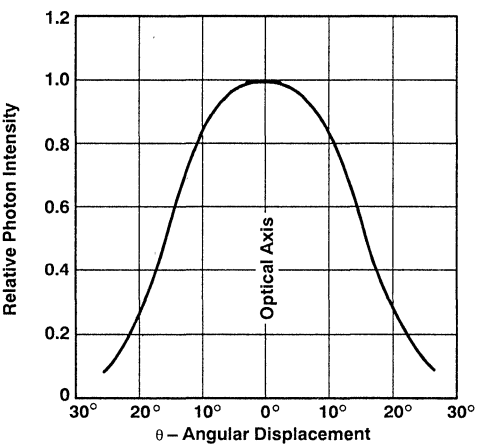


FIGURE 5

† Normalized to output at I_F = 50 mA, T_C = 25°C.
NOTE 4: These parameters were measured using pulse techniques: t_w = 0.04 ms, duty cycle ≤ 10%.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TIL131
CHANGE IN WAVELENGTH OF PEAK INTENSITY
VS
FREE-AIR TEMPERATURE

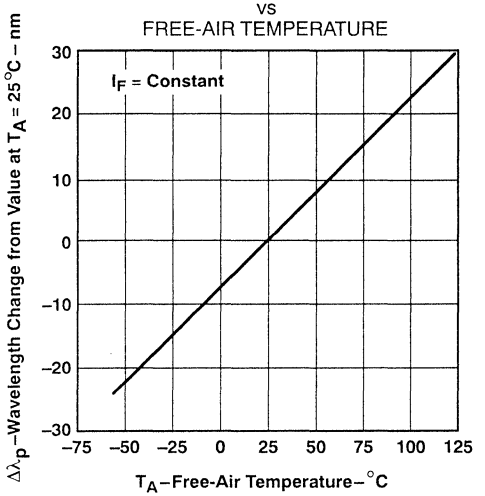


FIGURE 6

TIL132
NORMALIZED LIGHT CURRENT
VS
ANGULAR DISPLACEMENT

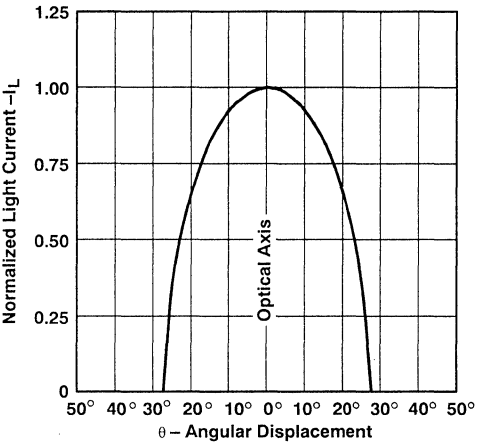


FIGURE 7

TIL132
DARK CURRENT
VS
FREE-AIR TEMPERATURE

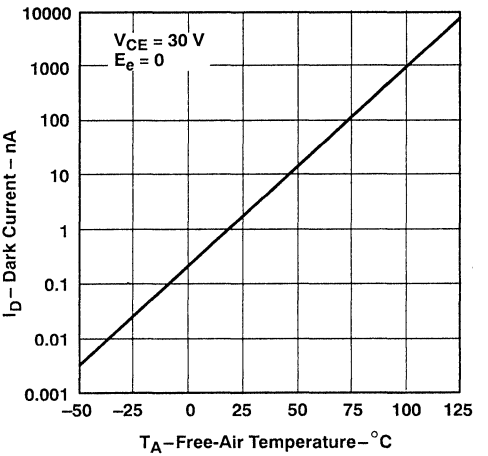


FIGURE 8

D1093, SEPTEMBER 1971—REVISED SEPTEMBER 1989

TIL134 . . . 12-ELEMENT GALLIUM ARSENIDE IRED ARRAY
TIL135 . . . 12-ELEMENT PHOTOTRANSISTOR ARRAY
TIL136 . . . 12-CHANNEL PAIR

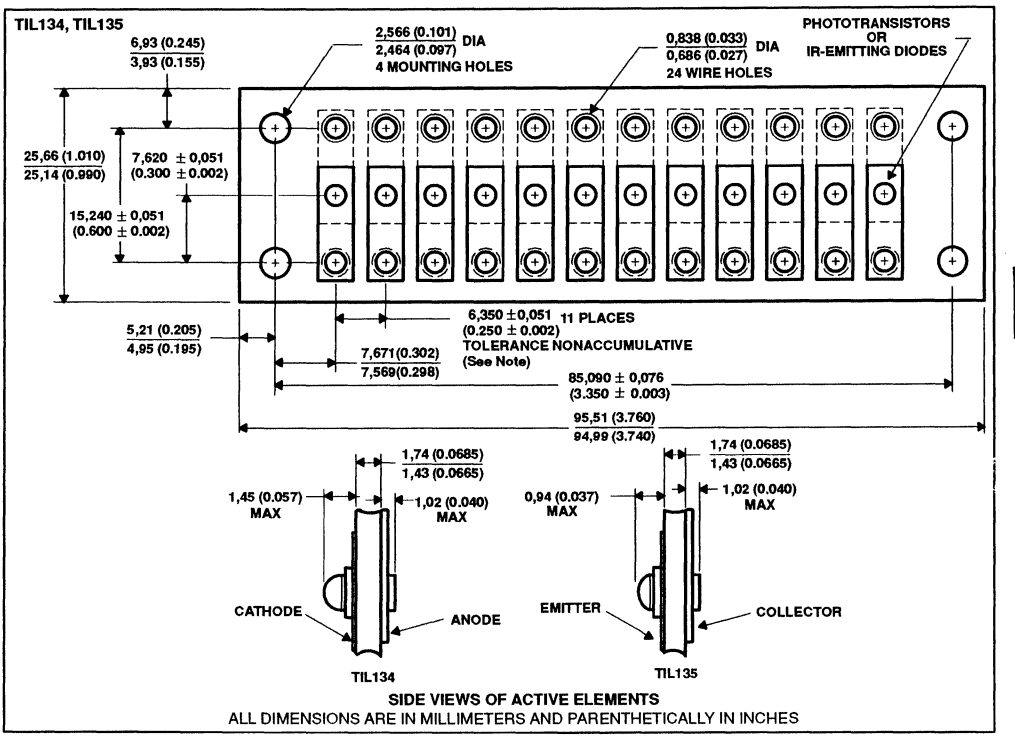
- **Center-to-Center Spacing of 6,3 mm (0.250 inch) for Tape Reading**
- **Reliable Solid-State Components**
- **IREDs Eliminate Lamp-Filament-Sag Problems**
- **Spectrally Matched for Improved Performance**
- **Printed Circuit Board Construction Allows Precise Alignment**

description

The TIL134 is an array of twelve TIL23 gallium arsenide infrared-emitting diodes mounted in a printed circuit board. The TIL135 is an array of twelve selected LS600 phototransistors. The TIL136 is a pair of selected arrays comprising a TIL134 and TIL135 and offering specified channel performance.

mechanical data

The printed circuit board material is glass-base NEMA standard FR-4, class II, 0.6-kg/m^2 (2-oz/ft^2) copper-clad on each side. The approximate weight of the TIL134 and TIL135 is 8.5 grams each.



SIDE VIEWS OF ACTIVE ELEMENTS
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: The tolerances shown for these dimensions apply to location of the mounting holes and the active elements only. Tolerance of ±0,13 mm (0.005 inch) applies for location dimensions of the wire holes.

TIL134 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Reverse voltage ..... 2 V
Continuous forward current at (or below) 25°C free-air temperature (see Note 1) ..... 100 mA
Operating free-air temperature range ..... −65°C to 125°C
Storage temperature range ..... −65°C to 150°C
Soldering temperature (10 seconds) ..... 240°C

NOTE 1: Derate linearly to 125°C free-air temperature at the rate of 1 mW/°C.

TIL134 operating characteristics of each element at 25°C free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Radiant power output	I_F = 50 mA	0.4		1	mW
λ_p	Wavelength at peak emission			0.93		μm
$\Delta\lambda$	Spectral bandwidth			500		Å
θ_{HI}	Half-intensity beam angle			35°		
V_F	Static forward voltage			1.25	1.5	V

TIL135 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage ..... 50 V
Emitter-collector voltage ..... 7 V
Continuous device dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 50 mW
Operating free-air temperature range ..... −65°C to 125°C
Storage temperature range ..... −65°C to 150°C
Soldering temperature (10 seconds) ..... 240°C

NOTE 2: Derate linearly to 125°C free-air temperature at the rate of 0.5 mW/°C.

TIL135 electrical characteristics at 25°C free-air temperature

individual element characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 100 μA, E_e = 0	50			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage	I_E = 100 μA, E_e = 0	7			V
I_D	Dark current	V_{CE} = 30 V, E_e = 0			100	nA
I_L	Light current	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 3	2		12	mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 0.4 mA, E_e = 20 mW/cm², See Note 3		0.15		V

element matching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\frac{I_L min}{I_L max}$	Light current matching factor	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 3	0.5			

NOTE 3: Irradiance (E_e) is the radiant power per unit area incident upon a surface. For this measurement, the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

TIL136 absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Maximum ratings of TIL134 and TIL135 apply.

TIL136 electrical characteristics at 25°C free-air temperature

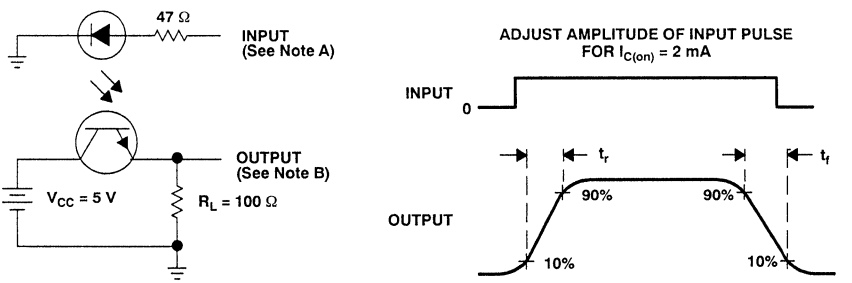
PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_C	Output collector current	I_F = 50 mA,	V_{CE} = 5 V	2.5	4	10	mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_F = 50 mA,	I_C = 2 mA		0.4	0.7	V

TIL136 switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 5 V,	$I_{C(on)}$ = 2 mA,		1.5		μs
t_f	Fall time	R_L = 100 Ω,	See Figure 1		1.5		μs

† These parameters are measured at a lens-to-lens distance of 0.100 inch.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \le 15$ ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \le 12$ ns, $R_{in} \ge 1$ MΩ, $C_{in} \le 20$ pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

TIL136
COUPLING CHARACTERISTICS

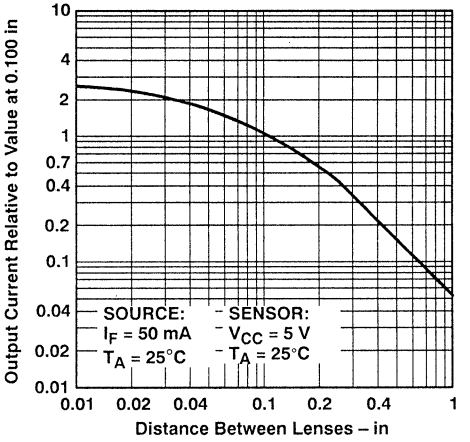


FIGURE 2

TIL134
FORWARD CONDUCTION CHARACTERISTICS

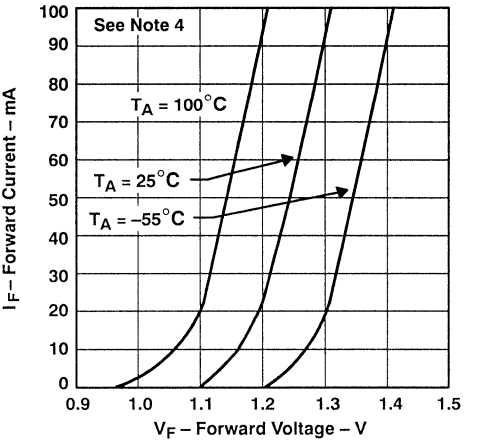


FIGURE 3

TIL134
RELATIVE POWER OUTPUT
VS
FORWARD CURRENT

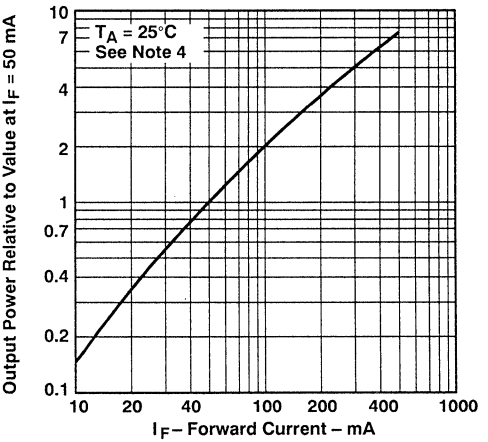


FIGURE 4

TIL134
RELATIVE PHOTON INTENSITY
VS
ANGULAR DISPLACEMENT

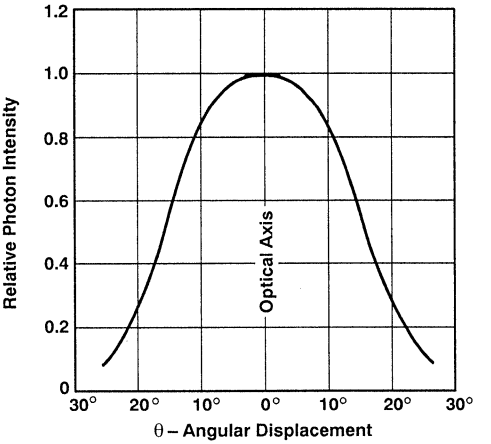


FIGURE 5

NOTE 4: These parameters were measured using pulse techniques: t_w = 0.04 ms, duty cycle ≤ 10%.

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TYPICAL CHARACTERISTICS

TIL134
CHANGE IN WAVELENGTH OF PEAK INTENSITY
VS
FREE-AIR TEMPERATURE

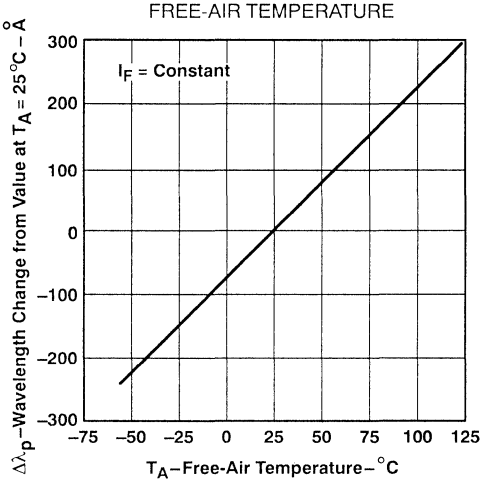


FIGURE 6

TIL135
NORMALIZED LIGHT CURRENT
VS
ANGULAR DISPLACEMENT

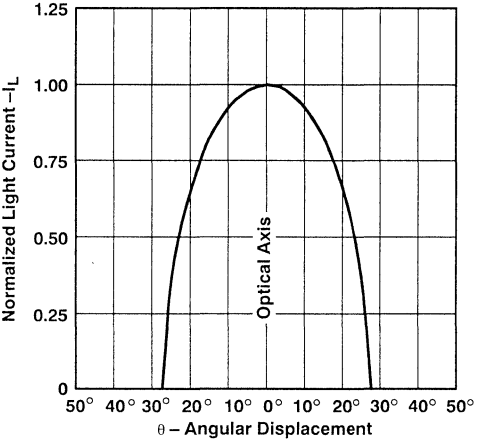


FIGURE 7

TIL135
DARK CURRENT
VS
FREE-AIR TEMPERATURE

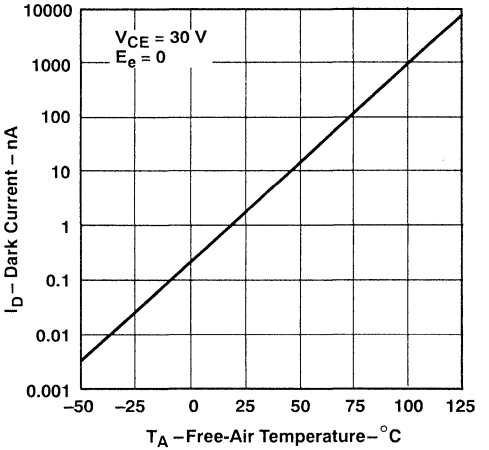


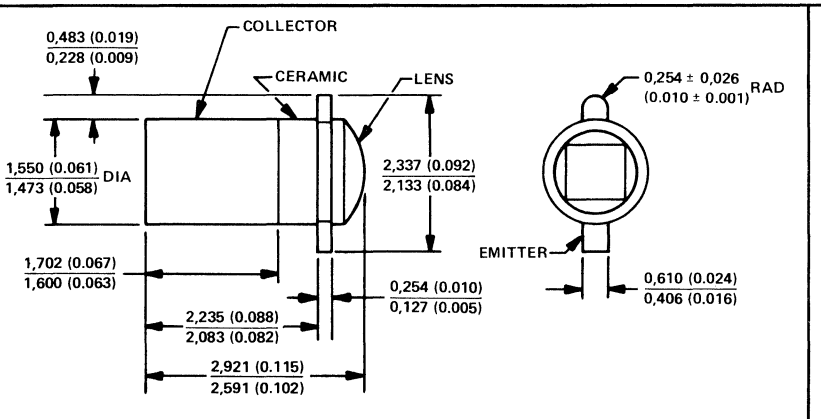
FIGURE 8

D1971, NOVEMBER 1974—REVISED SEPTEMBER 1989

DESIGNED FOR HIGH-DENSITY READ OUT

- Hermetically-Sealed Pill Package
- Recommended for Application in Character Recognition, Tape and Card Readers, Velocity Indicators, and Encoders
- Unique Package Design Allows for Assembly into Printed Circuit Boards
- Spectrally and Mechanically Compatible with TIL23 thru TIL25
- Saturation Level Directly Compatible with Most TTL
- TIL604HR2† Includes High-Reliability Processing and Lot Acceptance (See TIL604HR2 for Summary of Processing)

mechanical data



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FOUR TIMES ACTUAL SIZE

†All electrical and mechanical specifications for the TIL24 also apply for TIL24HR2.

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Collector-emitter voltage . . . . . 50 V
Emitter-collector voltage . . . . . 7 V
Continuous device dissipation at (or below) 25°C case temperature (see Note 1) . . . . . 50 mW
Operating case temperature range . . . . . −65°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Soldering temperature (10 seconds) . . . . . 240°C

electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYPE	MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C = 100 μA, E_e = 0	All	50			V
$V_{(BR)ECO}$	Emitter-collector breakdown voltage	I_E = 100 μA, E_e = 0	All	7			V
I_D	Dark current	V_{CE} = 30 V, E_e = 0	All			25	nA
		V_{CE} = 30 V, E_e = 0, T_C = 100°C	All		3		μA
I_L	Light current	V_{CE} = 5 V, E_e = 20 mW/cm², See Note 2	TIL601	0.5		3	mA
			TIL602	2		5	
			TIL603	4		8	
			TIL604	7			
			LS600	0.8			
			LS602	0.5			
			LS611	0.5	1	2	
			LS612	1	2	3	
			LS613	2	3	4	
			LS614	3	4	5	
			LS615	4	5	6	
			LS616	5	6	7	
			LS617	6	7	8	
			LS618	7	8	9	
			LS619	8	9		
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 0.4 mA, E_e = 20 mW/cm², See Note 2	All		0.15		V

NOTES: 1. Derate linearly to 125°C at the rate of 0.5 mW/°C.
2. Irradiance (E_e) is the radiant power per unit area incident upon a surface. For this measurement, the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_r	Rise time	V_{CC} = 30 V, I_L = 800 μA, R_L = 1 kΩ, See Figure 1	8	μs
t_f	Fall time		6	

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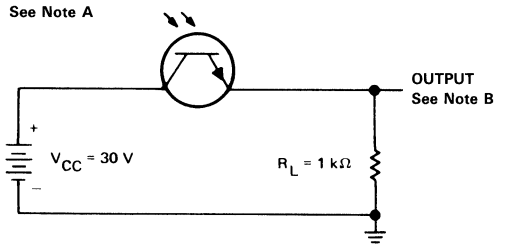
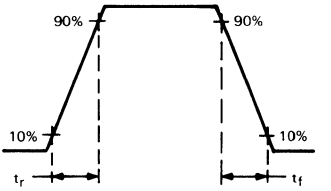
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



OUTPUT VOLTAGE WAVEFORM

NOTES: A. Input irradiance is supplied by a pulsed gallium arsenide infrared emitter with rise and fall times of less than 50 ns. Incident irradiation is adjusted for I_L = 800 μA.
B. Output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq 25$ ns, $R_{in} \geq 1$ MΩ, $C_{in} \leq 20$ pF.

FIGURE 1

TYPICAL APPLICATION DATA

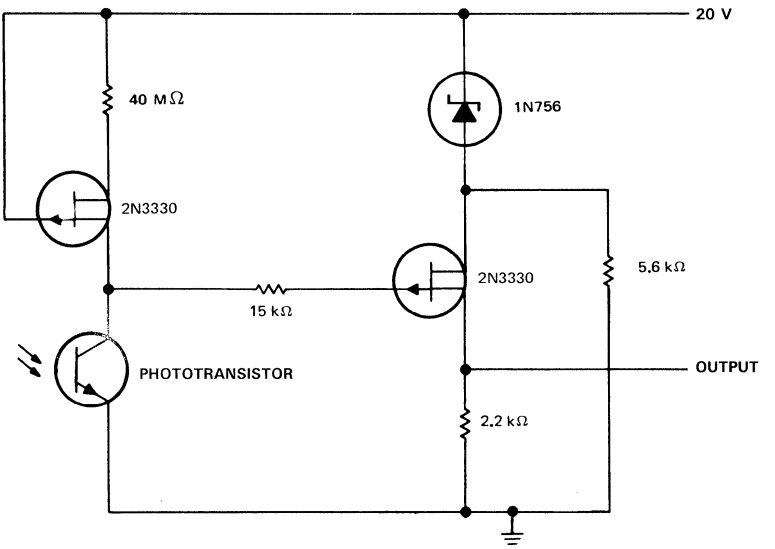


FIGURE 2. LOW-LEVEL DETECTOR AND PREAMPLIFIER

TYPICAL APPLCIATION DATA

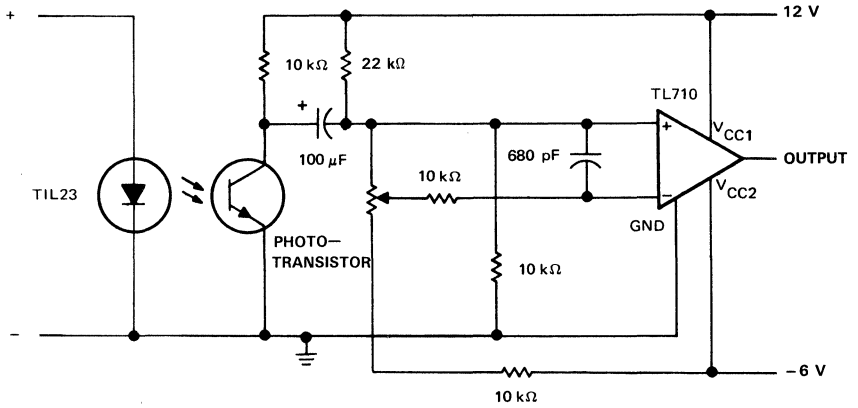


FIGURE 3. OPTICALLY COUPLED AMPLIFIER

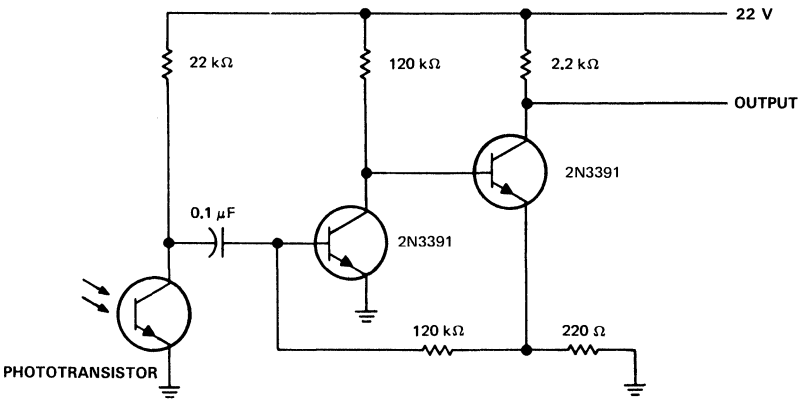


FIGURE 4. LIGHT PULSE DETECTOR

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TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

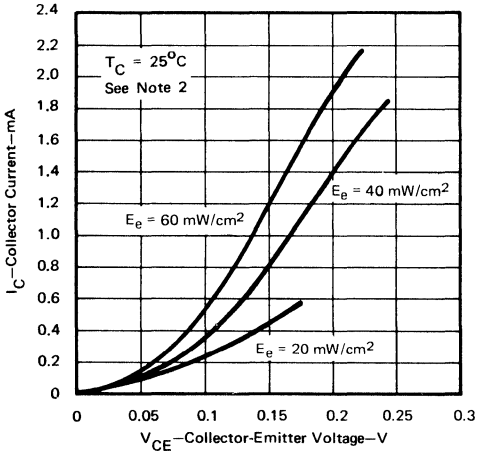

FIGURE 5

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

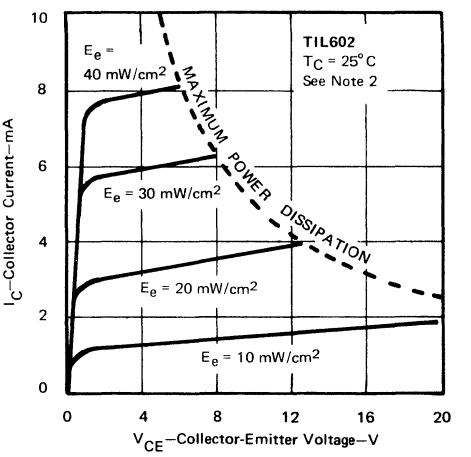

FIGURE 6

COLLECTOR-EMITTER SATURATION VOLTAGE
vs
IRRADIANCE

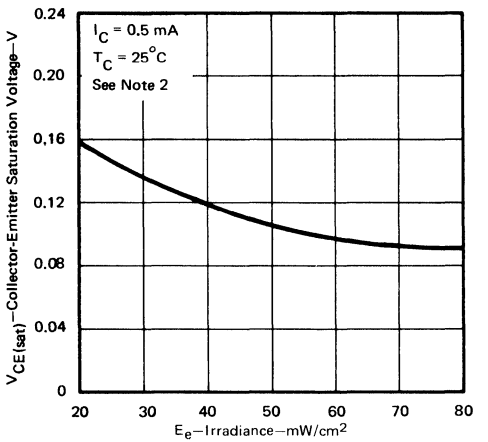

FIGURE 7

COLLECTOR CURRENT
vs
IRRADIANCE

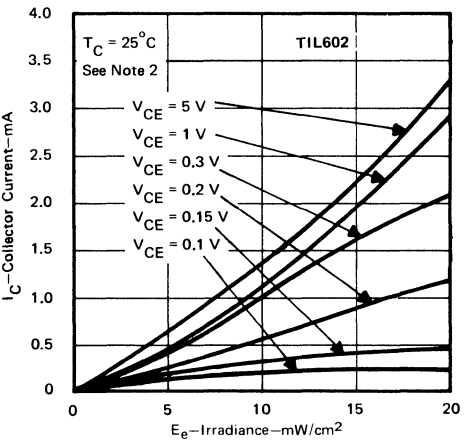

FIGURE 8

NOTE 2. Irradiance (E_e) is the radiant power unit area incident upon a surface. For this measurement, the source is an unfiltered tungsten linear-filament lamp operating at a color temperature of 2870 K.

TYPICAL CHARACTERISTICS

DARK CURRENT
vs
CASE TEMPERATURE

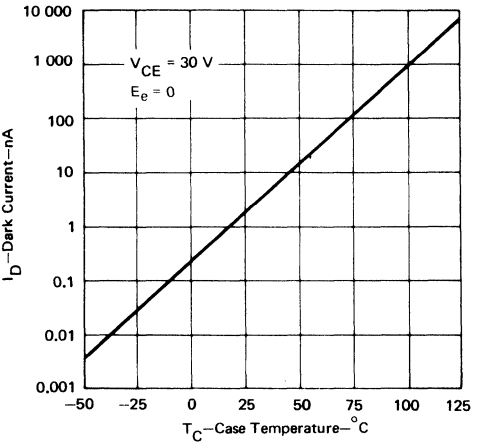

FIGURE 9

RELATIVE OUTPUT
vs
MODULATION FREQUENCY

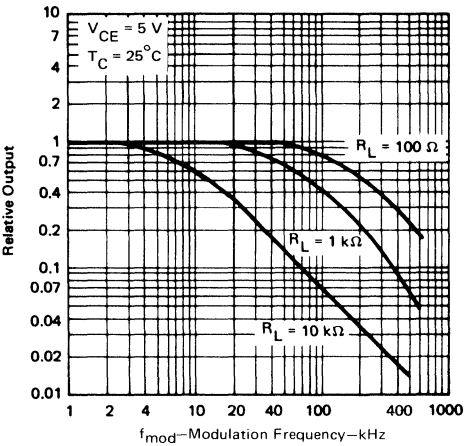

FIGURE 10

COUPLING CHARACTERISTICS
OF TIL23 OR TIL24 WITH TIL602

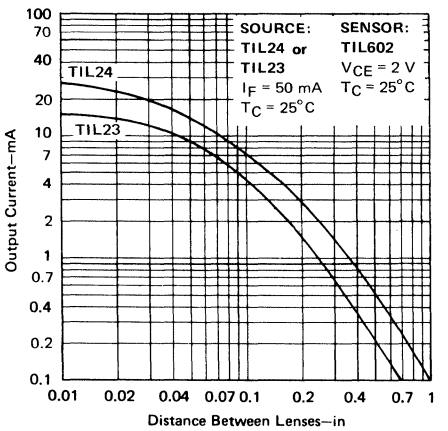

FIGURE 11

RELATIVE OUTPUT
vs
CASE TEMPERATURE OF SOURCE AND SENSOR

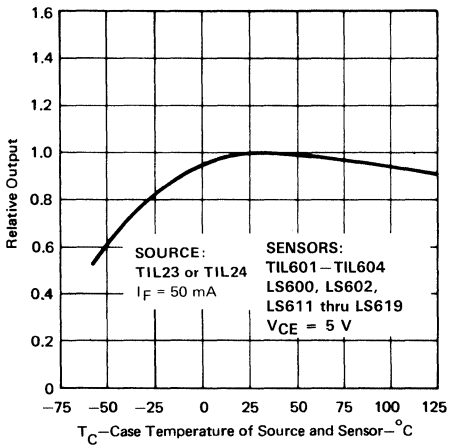

FIGURE 12

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TYPICAL CHARACTERISTICS

NORMALIZED LIGHT CURRENT
vs
ANGULAR DISPLACEMENT

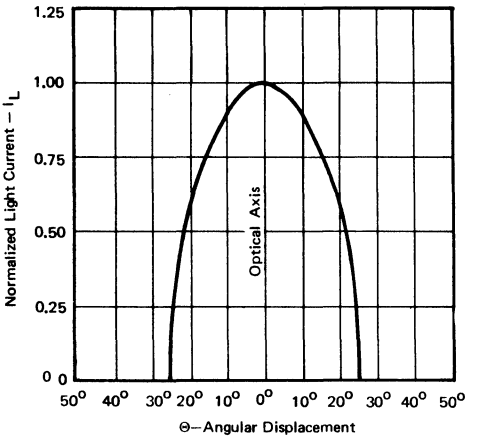

FIGURE 13

RELATIVE SPECTRAL CHARACTERISTICS

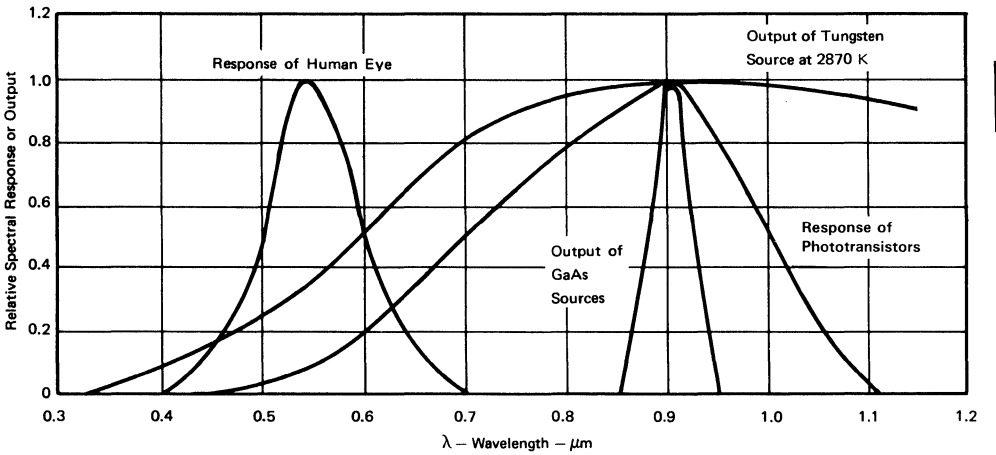

FIGURE 14

- **This processing applies only to devices ordered under the part number TIL604HR2**
- **For electrical and mechanical specifications, refer to TIL604 data sheet**

This processing and lot acceptance follow the sequence of tests in MIL-S-19500 for JANTX types. This is not to be construed to be a JANTX-qualified part. A detail specification is available upon request through your TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
LITERATURE RESPONSE CENTER
P.O. Box 809066
Dallas, Texas 75380-9066

TEST	MIL-STD-750 TEST METHOD
100% Processing	
Storage: T_A = 125°C, t = 24 h	1032
Temperature Cycle: −55°C to 125°C, 10 cycles	1051
Constant Acceleration: 20,000 G, Y_1 axis	2006
High-Temperature Reverse Bias:	
V_{CE} = 30 V, T_A = 125°C, t = 48 h	1039
Power Burn-in: P_D = 50 mW, t = 168 h	1039
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
External Visual	2071
Product Acceptance	
Group A: LTPD = 5	
External Visual	2071
Electrical: T_A = 25°C	
Electrical: T_A = 100°C	
Group B-1: LTPD = 15	
Solderability	2026
Group B-2: LTPD = 10	
Thermal Shock	1051 Cond. B-1
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
Group B-3: LTPD = 5	
Steady-State Operating Life: t = 340 h	1027

TEST	MIL-STD-750 TEST METHOD
Group B-4:	
Decap, Internal Visual; Design Verification	
1 Device/0 Failure	2075
Bond Strength LTPD = 20 (C = 0)	2037 Cond. A
Group B-5: Not Applicable	
Group B-6: LTPD = 7	
High-Temperature Life (Nonoperating)	1032
t = 340 h	
(Group C Tests are run on one lot every six months)	
Group C-1: LTPD = 15	
Physical Dimensions	2066
Group C-2: LTPD = 10	
Thermal Shock (Glass Strain)	1056 Cond. A
Hermetic Seal, Fine	1071 Cond. G or H
Hermetic Seal, Gross	1071 Cond. C or D
Moisture Resistance	1021
External Visual	2071
Group C-3: LTPD = 10	
Shock: 1500 G	2016
Vibration: 50 G	2056
Acceleration: 2000 G (X_1, Y_1, Y_2 axis)	2006
Group C-4: LTPD = 15	
Salt Atmosphere	1041
Group C-5: Not Applicable	
Group C-6: λ = 10	
Steady-State Operating Life: t = 1000 h	1026

TEXAS INSTRUMENTS
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Contents

QUALITY/RELIABILITY PROGRAM FOR OPTOELECTRONICS AND IMAGE-SENSING COMPONENTS

Texas Instruments has an extensive commitment to produce semiconductor products with the highest quality and reliability performance possible. TI monitors/controls the entire semiconductor process, from the earliest stages of device processing through completion of the final device. These monitored processes, which follow rigid quality standards, are illustrated in Table 1. To further emphasize this quality thrust, TI incorporates quality reviews with many of our major customers. These reviews incorporate comparisons between customer incoming and TI outgoing inspection reports and in many cases have gained the customer confidence required for ship-to-stock implementation. Our continuing goal is to be the Number 1 supplier in the industry, and we have set up our QA program to meet this challenge.

The broad spectrum of industrial/military applications demands that our products operate under adverse conditions and prolonged use. Please refer to Table 2 for our overall testing capability and to Table 3 for specific military standard test capability available at TI.

Extensive facilities are used in our failure analysis laboratory to analyze in-house and field failures of TI devices. Inputs from this lab are instrumental in generating the actions necessary for continuous improvement of our products. Table 4 outlines our Failure Analysis Procedures and our test facilities.

In summary, this chapter includes the following tables:

TEXAS INSTRUMENTS QUALITY POLICY

For every product or service we offer
we shall define the requirements that solve
the customers' problems, and

WE SHALL CONFORM TO THOSE REQUIREMENTS WITHOUT EXCEPTION.

For every job each TIer performs
the performance standard is:

DO IT RIGHT THE FIRST TIME.

Table 1. Typical Standard Device Flow

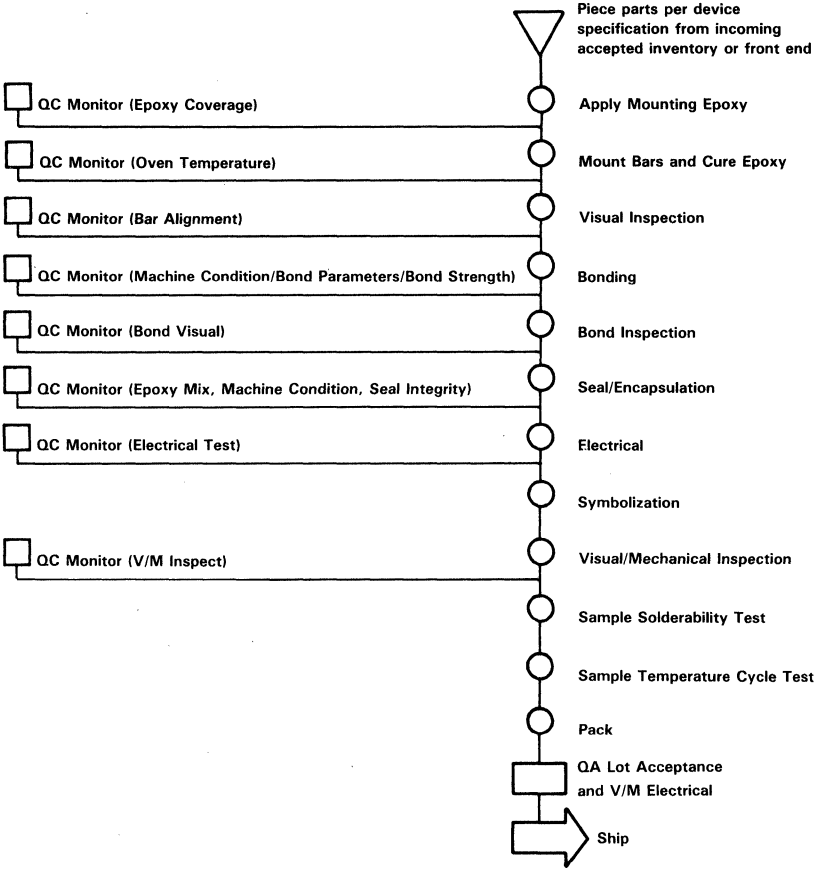

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Table 2. Overall Test Capability

Test	Capability
Acceleration, Sustained (Centrifuge)	50 to 50,000 G (standard)
Bond Strength	0 to 25 grams
Altitude (Barometric Pressure, Reduced)	150,000 ft simulated altitude
Electrostatic Susceptibility	MIL-STD-883, Method 3015
Flammability	800°C to 1100°C
Moisture Resistance	+2°C to 96°C, 40% RH to 100% RH
H.A.S.T.	+85°C to +138°C, 40% RH to 100% RH
Particle Detection	
Acoustical (PIND)	≥ 1 microgram
Electrical	Intermittency ≥ 1 μs with 100-mV amplitude
Pressure Cooker (Autoclave)	0 to 15 psig of steam pressure
Radiographic Inspection (X-Ray)	
Film	Resolution to 0.001 inch, 150 kV, 5 mA
Salt Atmosphere/Spray	25°C to 45°C, up tp 20% salt solution
Seal	
Gross Leak	
Bubble	$\geq 1 \times 10^{-5}$ atm cm^3/s
Dye Penetrant	$\geq 5 \times 10^{-6}$ atm cm^3/s
Weight Gain	$> 2 \times 10^{-6}$ atm cm^3/s
Radioactive Tracer Gas	$\geq 1 \times 10^{-10}$ atm cm^3/s
Symbolization (Resistance to Solvents)	
Shock (Mechanical)	To limits of: MIL-STD-202, Method 213 MIL-STD-750 MIL-STD-810, Method 516 MIL-STD-883
Solderability, Meniscograph	MIL-STD-883, Method 2022
Solderability/Soldering	Up to 280°C
Temperature Cycling	−65°C to +200°C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Torque
Thermal Shock	−65°C to +200°C
Ultrasonics	0 to 100 psi at 40 kHz or 25 kHz
Vibration, Fatigue	10 to 100 Hz, 5 to 70 G
Vibration, Random	20 to 2000 Hz, Power Spectral Density 1.3 G^2/Hz
Vibration, Variable	5 to 2000 Hz as limited by 1 inch double amplitude and 60 inches/second velocity. 0 to 70 G (standard), 70 to 100 G (nonstandard)*

*Limited fixture availability.

Table 3. Military Standard Test Capability

TEST CATEGORY	MIL-STD-202	MIL-STD-750	MIL-STD-883
Altitude	All Conditions except G	All Conditions except G	All Conditions except G
Bond Strength		Conditions A or B	Conditions A, C, or D
Dew Point		All Conditions	All Conditions
Flammability	All Conditions		
Immersion	All Conditions	All Conditions	All Conditions
Insulation Resistance	All Conditions	All Conditions	All Conditions
Meniscograph Solderability			All Conditions
Moisture Resistance	All Conditions	All Conditions	All Conditions
Resistance to Solvents (Symbolization)	All Conditions	All Conditions	All Conditions
Salt Atmosphere		All Conditions	All Conditions
Salt Spray	All Conditions	All Conditions	
Seal	All Conditions	All Conditions	All Conditions
Solderability	All Conditions	All Conditions	All Conditions
Soldering Heat	All Conditions	All Conditions	
Temperature Cycling	All Conditions except Method 107, Conditions D & E	All Conditions except Method 1051, Conditions D & E	All Conditions except E
Temperature Storage			Conditions A thru F
Terminal Strength (Lead Integrity)	All Conditions	All Conditions	All Conditions
Axial Lead Tensile Test		All Conditions	
Thermal Shock (Glass Strain)		All Conditions	All Conditions except E & F
Acceleration, Sustained (Centrifuge)	All Conditions	All Conditions	All Conditions Method 2001, except G, H, & J
Particle Impact Noise Detection (PIND)		All Conditions	All Conditions
Forward Instability Shock (FIST)		All Conditions	
Backward Instability Shock (BIST)		All Conditions	
Shock (Mechanical)†	All Conditions	All Conditions	All Conditions Method 2002, Conditions F and G, may require special fixturing.‡

† Also perform mechanical shock per MIL-STD-8108, Method 516.
‡ Call Physical Test supervisor for available fixtures.

Table 3. Military Standard Test Capability (Continued)

TEST CATEGORY	MIL-STD-202	MIL-STD-750	MIL-STD-883
Vibration, Fatigue		All Conditions	All Conditions
Vibration, Noise		All Conditions	All Conditions
Vibration, Random†	All Conditions		
Vibration, Variable Frequency†	All Conditions	All Conditions	All Conditions
X-Ray, Film‡	All Conditions	All Conditions	All Conditions

† Also perform random vibration and variable frequency vibration per MIL-STD-8108, Method 514.1, procedures I, II, III, IV, V, VI, and VII. Omit paragraph 4.5.1.1, Resonant Search, and paragraph 4.5.1.2, Resonant Dwell.

‡ Radiographic inspection is performed in accordance with many government and customer specifications. Before any new radiographic specification is accepted or deemed acceptable for use as a test standard within the Semiconductor Group, it must be approved by Environmental Test Services.

Table 4. Failure Analysis Capabilities

I. Nondestructive Techniques
- A. Hermeticity evaluation
- B. X-ray interpretation of bonding and die mount
- C. Electrical characterization
  1. Breakdown, leakage, and functional tests run at temperature extremes
  2. Polaroid documentation of curve traces and/or oscilloscope traces

II. Destructive Techniques
- A. Decapsulation/Delid of devices
- B. Probe and isolation of electrical defects
- C. Layer-by-layer removal of device levels by selective etching
- D. Microsection analysis
  1. Sections taken at shallow to 90° angles — sample sizes to 1.5 inches
  2. Selective staining to delineate diffusions, dielectrics, etc.
  3. Thickness measurements by SEM or optical microscopy
- E. Optical microphotography — magnifications to 5000X
- F. Infrared microscopy — transmission and reflection
- G. Nanometrics
- H. Planar plasma etching
- I. Scanning electron microscopy — SEM
  1. Routine magnification to 50,000X
  2. 50-Å resolution
  3. Back-scattered electron detector
  4. Military product lot acceptance of metallization
  5. Voltage contrast
  6. Specimen current amplifier
- J. Electron microprobe
  1. Chemical detection of elements with atomic number greater than 11
  2. Typical 4- to 5-μm beam penetration
  3. Spot size typically 1000 to 2000 Å
- K. Auger spectroscope
- L. Ion microprobe mass analysis
- M. Gas and/or plastic composition analysis

OPTOCOUPLER RELIABILITY DATA

INTRODUCTION

Texas Instruments designs and builds quality and reliability into all the products it offers to the electronic marketplace. The quality control organization is uniquely responsible for coordinating the total effort and for providing direct action necessary to insure that quality and reliability objectives are met.

The reliability data shown in this report is indicative of the extensive testing performed by Texas Instruments on all components to assure continued leadership in quality and reliability. Included in this report is a summary of 1987 through June 1989 reliability testing on the 4N22 and 4N47, parent devices for the JAN, JANTX, and JANTXV metal can optocoupler products, and typifies results of product built to the standard device product flow.

OPERATING LIFE TEST

Data was summarized from monthly and semi-annual Group B and Group C quality conformance inspections according to MIL-S-19500/486A (4N22) and MIL-S-19500/548 (4N47) plus additional testing deemed necessary by TI Quality Assurance to guarantee process integrity. Life testing was performed under the following conditions:

T_A = 25°C
I_F = 20 mA
V_{CE} = 10 V
P_D = 275 mW

Test duration varied from 340 hours to 1000 hours to allow data accumulation on 8545 devices exercised for a total of 4,074,160 device hours. No critical failures were observed.

In addition, 4801 device type 4N24 optocouplers have been placed on continuous life test at the above referenced conditions for long-term monitoring of performance characteristics. These devices are read and recorded at 1000 hour intervals, and have accumulated 14,735,100 device hours with no critical failures. This data also applies to JAN, JANTX, and JANTXV products.

STORAGE LIFE TESTS

Devices were stored in ovens at 125°C for 340 or 1000 hours (depending on requirement). Readings of all parameters included in the device specifications were made with zero failures in the sample of 4372 devices for a total of 1,822,560 device hours.

ENVIRONMENTAL TESTS

The tests listed in Table 1 were performed on samples of the product with the catastrophic or degradation failures as shown. The test conditions shown represent requirements imposed on the product by our customers and do not necessarily represent maximum capability of the component. Inquiries concerning response to the specific requirements should be addressed to your TI sales representitive.

Table 1. Environmental Test Results

MIL-STD-750 TEST METHOD	TEST	QUANTITY TESTED	FAILURES
1016	High Temperature Isolation Voltage, V_{IO} = 150 V, T_A = 125°C, T_D = 24 hr.	1493	0
1051	Temperature Cycling, −65°C to +125°C, 15 minutes at extremes (25 cycles)	1304	1
1056	Thermal Shock (Glass Strain), 100°C to −5°C, 5 cycles		
1021	Moisture Resistance		
2016	Mechanical Shock, 1500 G, 0.5 ms, X_1, Y_1, Y_2	1786	1
2050	Vibration, Variable Frequency, 50 G minimum		
2066	Constant Acceleration, 30 kG, 1 minute X_1, Y_1, Y_2		

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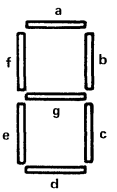
APPLICATIONS SUMMARY

MULTIPLEXING DISPLAYS

seven-segment displays

To display numbers and symbols an array of display elements is required. Two common configurations are shown in Figure 1. Figure 1a shows the seven-segment display that can be used to display the decimal numerals and some alphabetical characters by turning on appropriate segment patterns. Figure 1b shows a 5 × 7 dot matrix that can be used to display any alphanumeric symbol by turning on the appropriate dot pattern. The pattern required for each



a. SEVEN-SEGMENT LED DISPLAY

b. 5 X 7 DOT MATRIX DISPLAY

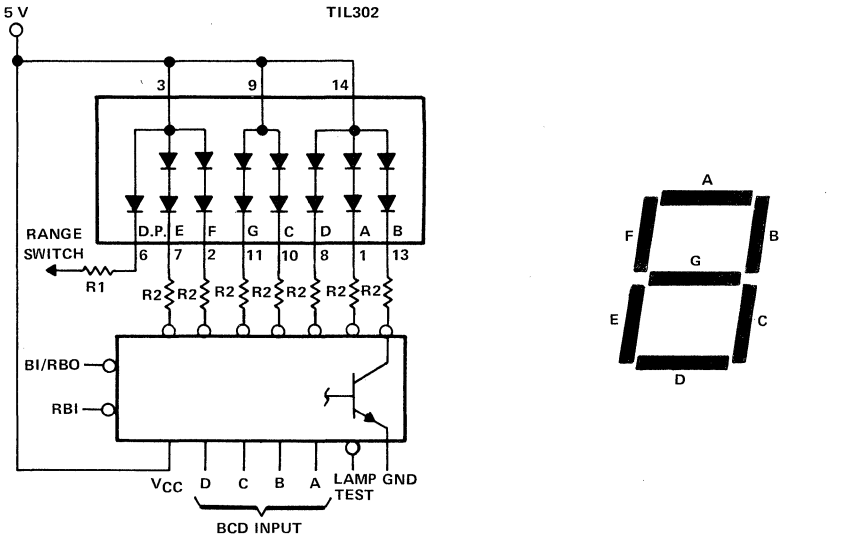
Figure 1. Display Matrices

number, character, or symbol to be displayed must be stored in a read-only memory or a display decoder in order to properly display a desired character. The interface to a seven-segment display is the BCD-to-seven-segment decoder driver like the SN7446 shown in Figure 2a. The input to the decoder is the BCD code for the number to be displayed. The RBI and BI signals can be taken low to turn off all segments, regardless of the input code. When BI is high, the LT (amp test) input can be brought low to turn on all segments to perform a lamp test operation. The BI/RBO can serve as an output for ripple blanking to other decoders. When RBI is brought low, RBO as an output will go low for rippling a blanking signal to other display decoders. The segment drivers A through H are connected to the LED's of the display to control which LED's are turned on.

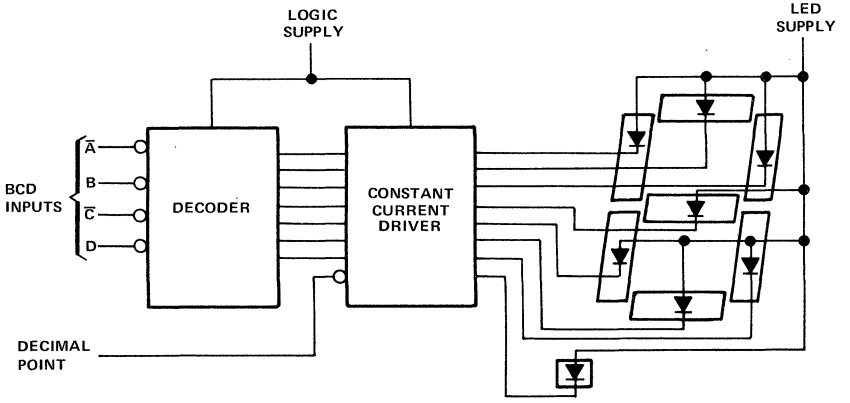
The entire circuit and display is available as a single device, the TIL306, shown in Figure 2b. This device has the 4-bit BCD code input, a decimal point input, and depends on a non-BCD code to provide blanking. Devices also exist that include a register as well as a decoder/driver and display in the same unit. The TIL308 shown in Figure 2c is one of those. It stores the four BCD inputs in a quadruple S-R flip-flop whose outputs are available from the device. There is a latch strobe input that, when low, stores the BCD code in the 4-bit register. There is a blanking input, BI, that, when low turns off all segments, and an LED test input that, when low, turns on all segments. If the LED test and the BI inputs are both high, the display shows the number whose code is latched in the device data register. Such a register simplifies the I/O requirements of the microcomputer since it can be treated as a complete storage location. It may be connected to either the data bus or any special system I/O bus.

The interface to a 5 × 7 or other dot matrix is handled in much the same way as the seven-segment device. The simplest device of this type is the TIL311, which displays hexadecimal characters using LEDs arranged on a 4 × 7 dot matrix pattern as shown in Figure 3a. It includes a 4-bit data register with a latch strobe input that causes the 4-bit input data to be entered while the strobe is low. As long as the strobe stays high, the information displayed and stored will not change. Thus, one could treat the strobe as a rising-edge latch signal. The overall structure of the TIL311 is shown in Figure 3. There is a blanking input that, when high, causes the display to be blanked. There is a left and right decimal point input available.

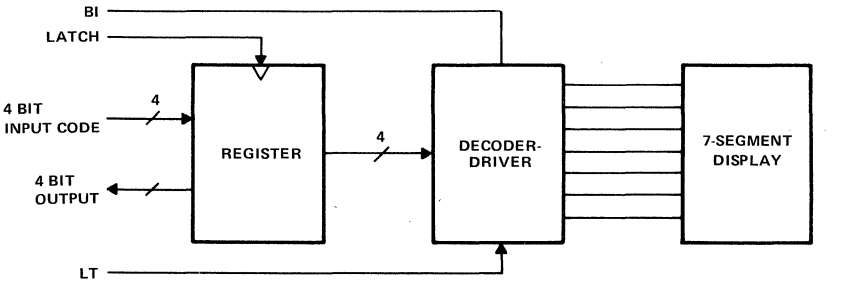
The control of a 5 × 7 dot matrix display device like the TIL305 requires a ROM or EPROM in which the display pattern for each character to be displayed is stored. The basic circuit structure is shown in Figure 4 for an individual interface to a TIL305. The TTL signals from the seven input lines (ASCII code inputs) are connected to the inputs I1 through I7. The current-drive capability is provided by SN75491 drivers acting as sink drivers from the output lines 01 through 07 and as source drivers for the column lines on the TIL305. At the time a column line is driven with current, the column select code CA through CE must simultaneously be applied to the column select lines of the EPROM. The EPROM outputs the seven row signals for a



a. SEVEN-SEGMENT DISPLAY INTERFACE

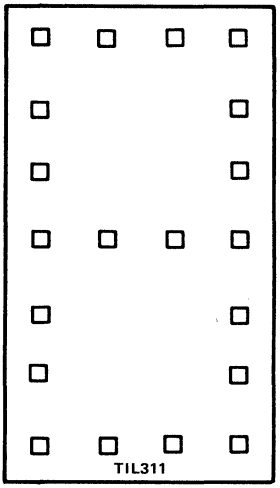


b. TIL306

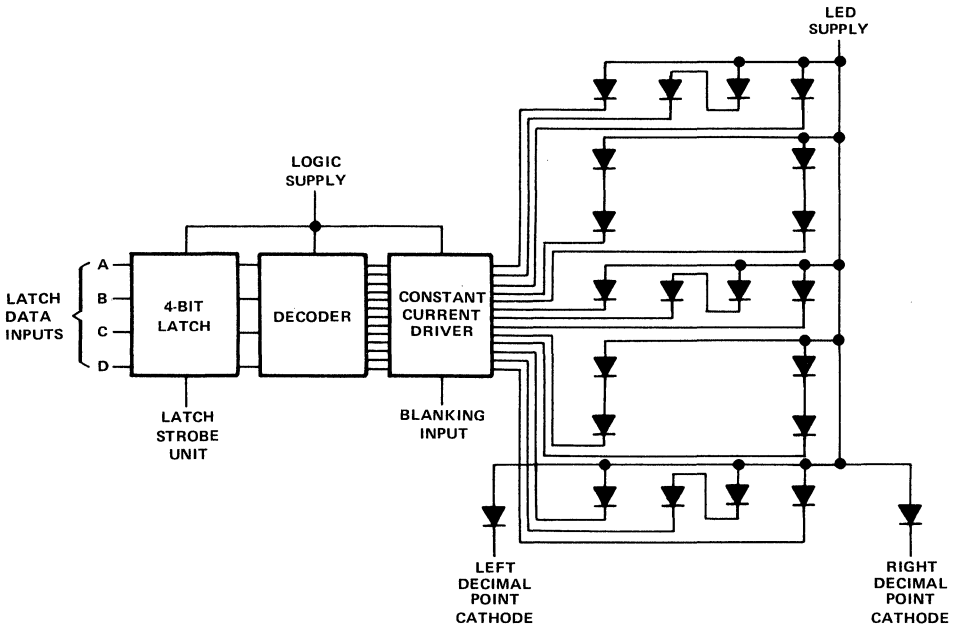


c. TIL308

Figure 2. Seven-Segment Displays



a. MATRIX 4 X 7 PATTERN.



b. SCHEMATIC

Figure 3. 4 X 7 Matrix

selected character for a selected column. Thus, the circuitry must scan through the columns at an appropriate rate by using either a ring counter or a counter-decoder combination.

In the example of Figure 4, an SN75496 5-bit ring counter is set up so that only one bit position will have a 1 at any given time. This is achieved with the wired-NAND control (SN7416) on the serial input. For example, if all outputs A through E (all bits) in the register are 0, the serial input line will be at the 1 level, and a 1 will be shifted into the first bit position. This 1 (in the A position) causes the serial input line to go low (to a 0), which will be shifted in to fill the lower bits with zeroes. The original 1 will propagate through to E with each rising edge of the clock. When the 1 is at E, a 1 will again be generated at the serial input to insert a new 1 into A when the 1 is shifted out of E. Thus, there is only one 1 in the shift register at any time. Only one column of the EPROM is addressed at any time, and only one column of LED drivers is turned on at any time. Also in the example of Figure 4, the unijunction oscillator is set to provide a clock pulse sequence at a frequency of about 1,000 pulses per second. A new column is selected and turned on for about a millisecond, and a column is on 20 percent of the time.

The circuit of Figure 4 provides only a single-character display position. If a multiple-position character display is required, it is not reasonable to provide a separate EPROM for each display unit. In other words, it is not feasible to repeat the circuit of Figure 4 for each character in the multiple position display. A circuit that shares the EPROM resource must be used. This means that the display must provide a RAM for storage of the character codes to be displayed and a sequence controller that will sequence through the codes stored in RAM while the different TIL305s are activated. The basic structure is shown in Figure 5 for a 16-character display.

There must be 16-location RAM, and each location must store a 6-bit ASCII code. There must be a modulo-16 counter that determines which RAM code and character position is to be used at any given time. The TIL305 that is activated is selected by the output of a 4-to-16 decoder. The decoder turns on one group of the SN75493 sink drivers for the selected character position. The sink drivers for all other character positions are turned off, and the associated TIL305s for those positions remain off. The modulo-16 counter is incremented by the trailing edge of output E from the central 5-bit ring counter, since that marks the beginning of the new column 1 display. There must be a provision for writing into the RAM from the processor and a write control signal, $\overline{W}$, that will switch the RAM address from the modulo-16 counter to the processor address lines. The SN74LS245 for each bit provides the switching required. This connection allows the information being displayed to be controlled by processor memory write or output operations. The overall structure of Figure 5 is somewhat complicated, but it can be cost effective in both power dissipation and parts costs. A similar approach can be used for time multiplexing of 7-segment displays to save power consumption.

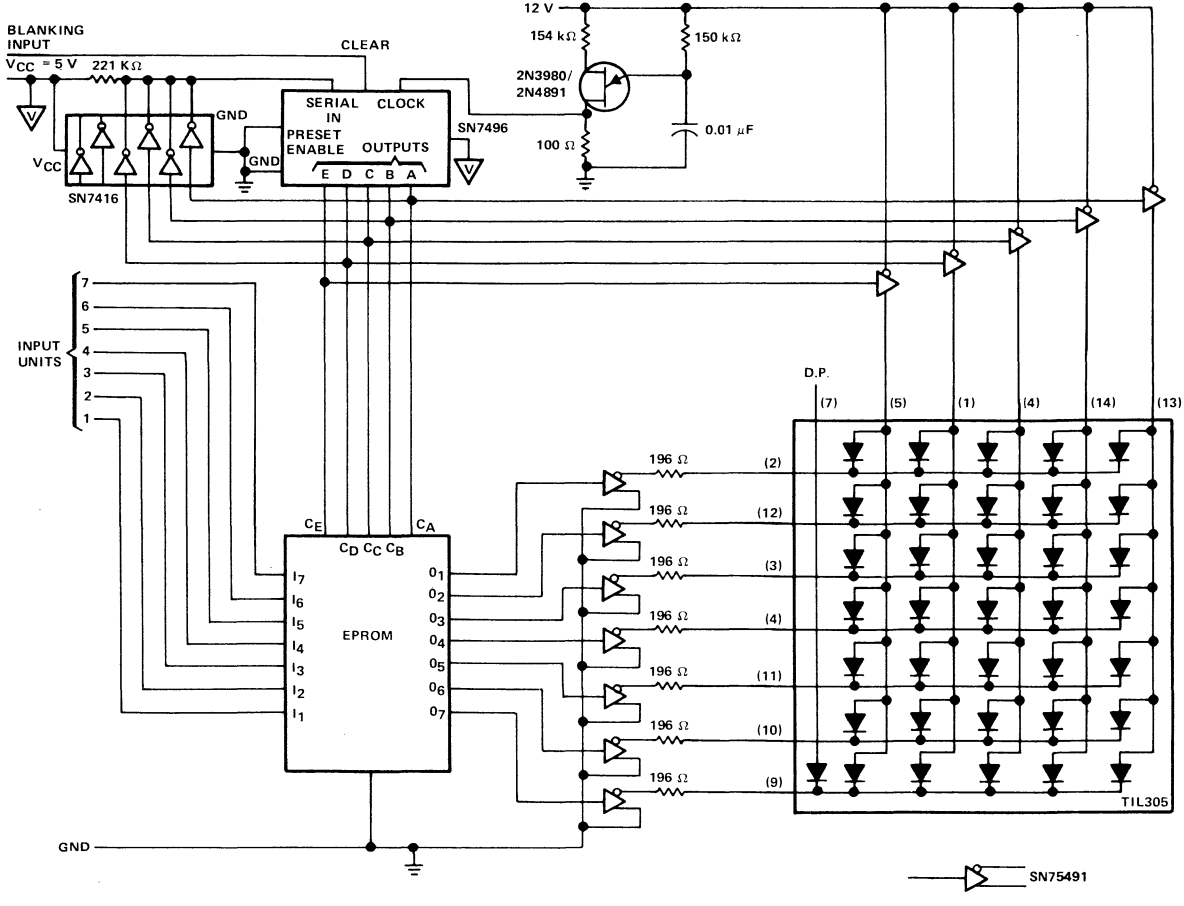


Figure 4. 5 X 7 Matrix

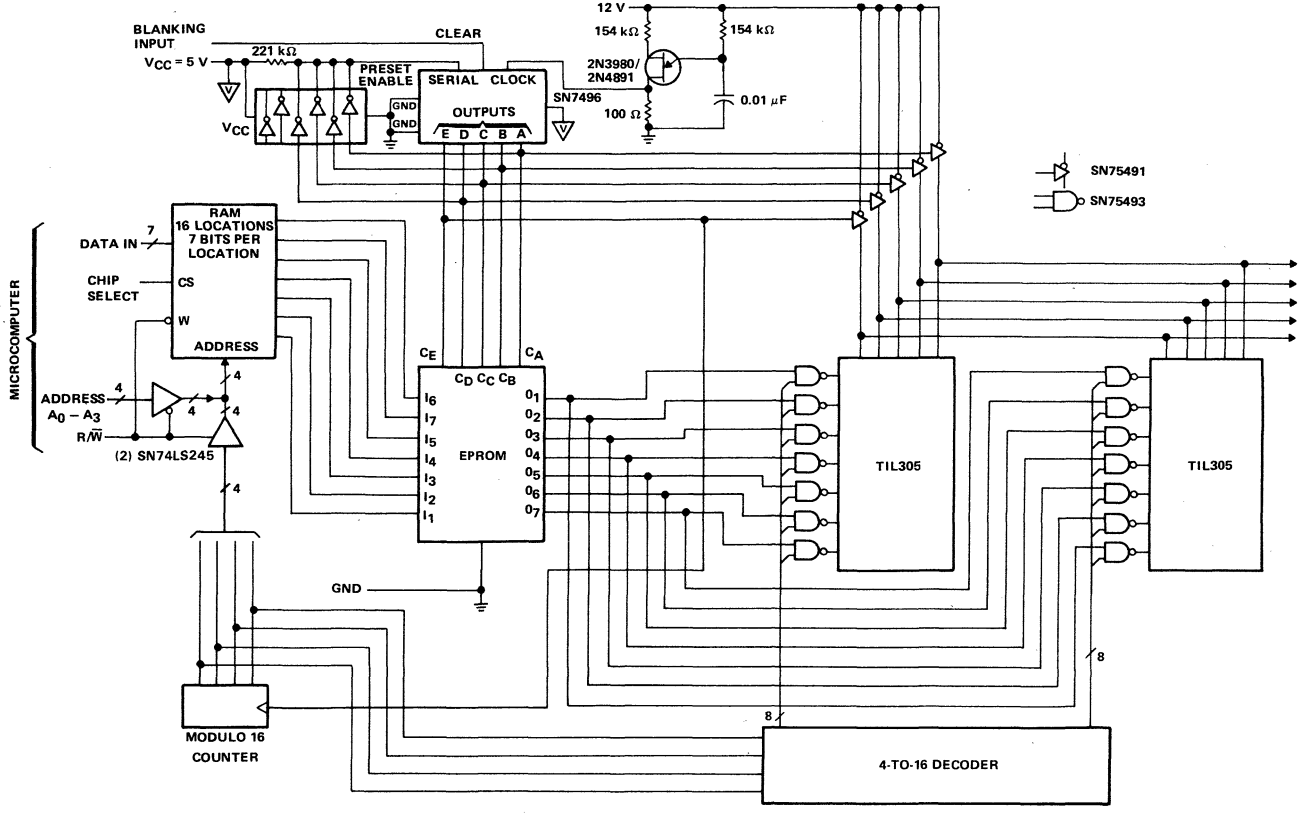


Figure 5. 16-Character Display

TIL311 HEXADECIMAL LED DISPLAY

The TIL311 is designed to store and display decimal and hexadecimal data. The device consists of an MSI logic chip to perform logic and storage functions plus a light emitting diode (LED) display in a single 14-pin dual in-line package.

It accepts parallel 8-4-2-1 data on four input lines and displays the corresponding decimal or hexadecimal character on a 4-by-7 dot matrix. Figure 1 illustrates the hexadecimal character representation for the decimal numbers 0 through 15. The logic levels are designed to be TTL compatible: a high level is 2 V to 5 V, a low level is 0 V to 0.8 V.

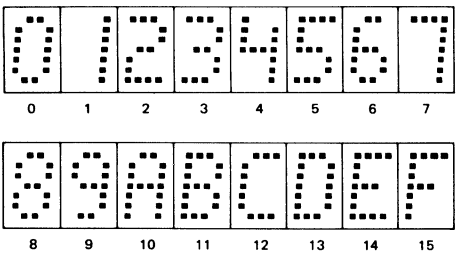


FIGURE 1. TIL311 Hexadecimal Character Configuration

The block diagram in Figure 2 shows the major sections of the TIL311: latches, decoder, current driver, and LED display. The inputs are DATA, LATCH STROBE, BLANKING, and DP. DATA is parallel 8-4-2-1 coded data. When LATCH STROBE is low, the data in the latches follow the data inputs. When LATCH STROBE goes high, the data on the input lines at strobe time is stored in the latches.

The 4-bit code is decoded and the required diodes are turned on via the constant-current drivers to display the proper character.

The LED display contains two decimal points: one to the left and one to the right of the character. A low input to one of the DP inputs will turn that decimal point on.

BLANKING must be low to display the character. When BLANKING goes high, the character is turned off regardless of the inputs. The BLANKING input does not change the data stored in the latches. BLANKING may be pulsed to intensity-modulate the display. The apparent brightness of the display is proportional to the duty cycle of the modulating signal, assuming a frequency high enough to avoid visible flicker. For example, at 1 kHz, a 50% duty

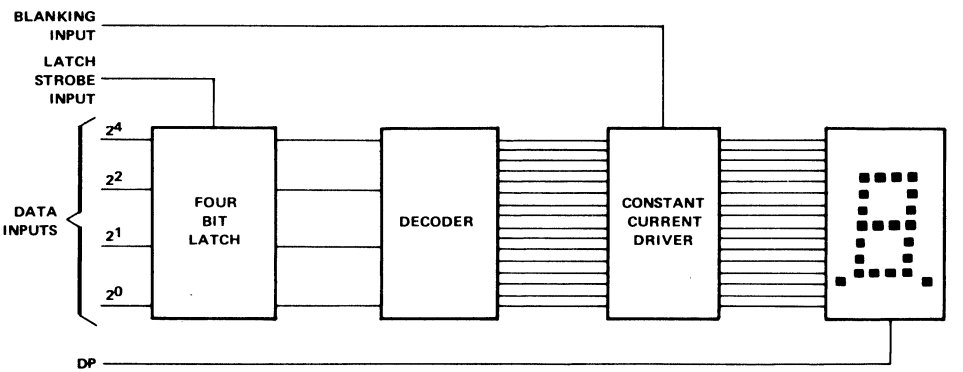


FIGURE 2. TIL311 Hexadecimal Display Block Diagram

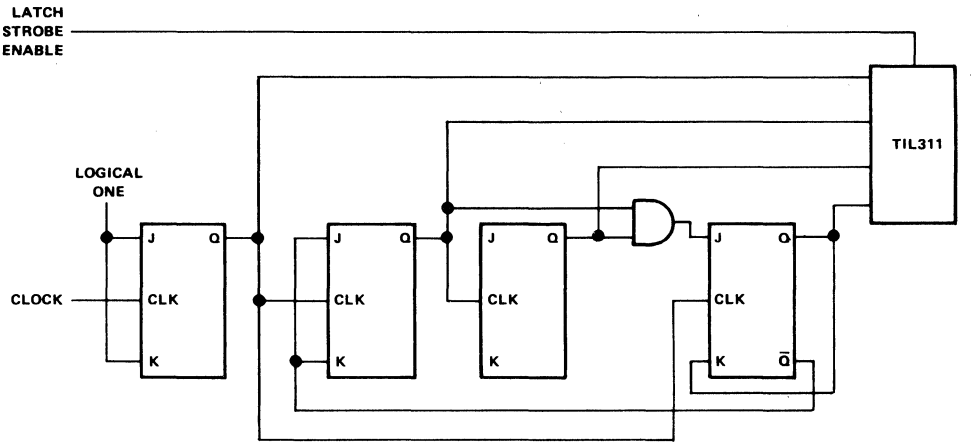


FIGURE 3. TIL311 Used As Counter Display

FIGURE 4. Discrete Light Display for a 16-Bit Register

cycle would cause an apparent brightness of 50% of the steady-state brightness.

Figure 3 illustrates the use of the TIL311 as a decimal display. The JK flip-flops are connected as a count-by-ten counter and represent one decade position in a multi-decade counter. The four Q outputs of the four flip-flops furnish the data inputs to the TIL311. Normally LATCH STROBE will be held high so that the display does not follow the counting. When counting is complete for a given time base, LATCH STROBE is pulsed with a negative-going pulse. The new data is then transferred from the decade counter into the latches and displayed.

Another application for the TIL311 is to display register information on computer control panels and service panels. Figure 4 illustrates the use of discrete lights to display the contents of a 16-bit register. The length of the display can easily lead to errors in interpretation of the data. Figure 5 illustrates the use of the TIL311 to display the same data in the same 16-bit register. The 16 register positions are divided into four 4-bit groups. The four bits in each group provide the inputs to each of four TIL311 displays. The resulting four hexadecimal character display provides a more concise interpretation of the register data.

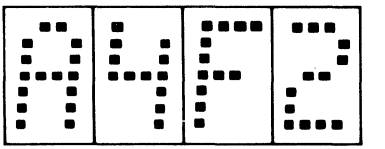


FIGURE 5. Hexadecimal Display for a 16-Bit Register

COUNTING CIRCUITS USING TIL306 AND TIL308 LEDs

Digital instruments have experienced a constant evolution since 1960. Counters that once occupied several inches of rack space in a 19-inch rack have been replaced by units the size of a text book with performance characteristics surpassing the older models. A major contribution to these changes is the continued advances in solid-state devices: integrated circuits have replaced the tubes and transistors and light-emitting diodes (LEDs) have replaced the incandescent displays.

Texas Instruments has introduced a new product that simplifies further the design of systems utilizing counters or digital read-outs. By combining an IC chip to perform the logic function and an LED display in a single 16-pin dual in-line package, Texas Instruments has provided the designer a device that reduces the complexity of his system without reducing flexibility of design. Two of these devices are the TIL306 and TIL308. The TIL306 and TIL308 have decimal points to the left side of the character. The TIL307 and TIL309 have decimal points to the right side of the character, but are otherwise identical to the TIL306 and TIL308, respectively. They can be combined to count, store, and display data in multiple decade positions.

CIRCUIT DESCRIPTION

The TIL306, as shown in Figure 1, consists of four major sections: counter, latches, decoder/driver, and LED display.

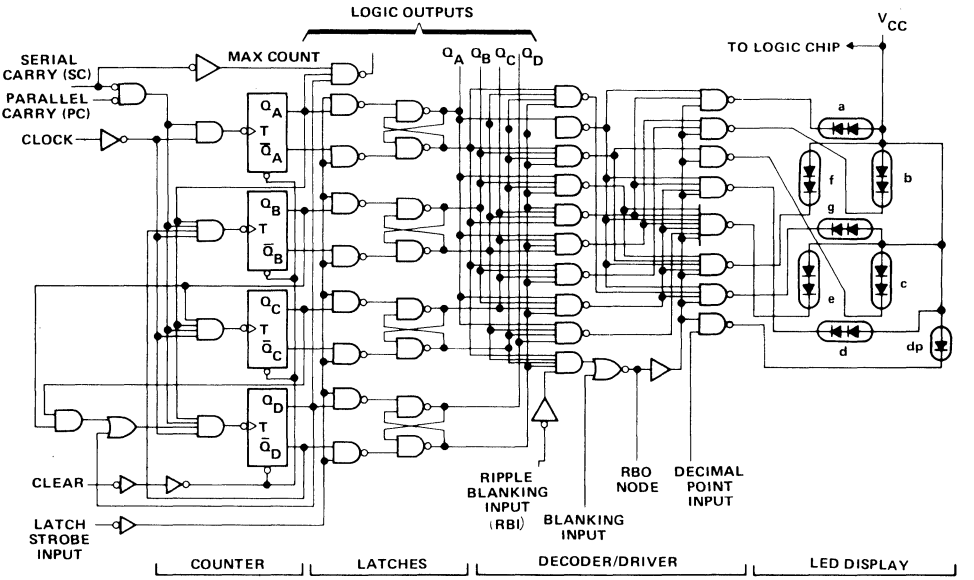


FIGURE 1. Functional Block Diagram of TIL306

The counter is connected as a synchronous counter. This configuration takes advantage of the minimal propogation delay to give maximum speed capability. Inputs to the counter are CLEAR, CLOCK, SERIAL CARRY, and PARALLEL CARRY. The counter and its inputs generate an output, MAX COUNT. Additional connections are LATCH STROBE, BLANKING, RIPPLE BLANKING, RBO, DECIMAL POINT and LOGIC OUTPUTS. All inputs and outputs are designed to be TTL compatible. A high level is a minimum of 2 V and a low level is a maximum of 0.8 V. A low input to CLEAR will reset the counter to zero independently of any other input. As long as the input remains low the counter remains at zero. A high is required to allow the counter to count.

The CLOCK input is the signal to be counted. With an input the counter will advance from 0 to 9. At a count of 9 the counter automatically resets to 0 with the next pulse. The counter changes state on the positive-going edge of the clock pulse. The clock pulse to the counter is controlled by SERIAL CARRY and PARALLEL CARRY.

The MAX COUNT output goes low when the counter reaches a count of 9, and then goes high when the counter progresses to 0 on the next clock input. This output can be connected to the CLOCK input of the next decade position for asynchronous operation or to the SERIAL CARRY input of the next decade position for synchronous operation.

A high on SERIAL CARRY inhibits the counter and forces MAX COUNT to go high regardless of the state of the counter stages. When SERIAL CARRY and PARALLEL CARRY go low, the CLOCK is enabled to the counter stages and the MAX COUNT gate is allowed to sense the status of the counter. The logic level of SERIAL CARRY must not be allowed to change while CLOCK is low or erroneous counts may result.

PARALLEL CARRY permits look ahead carry inputs from lower order decade positions. A high input inhibits the clock to the counter stages. When PARALLEL CARRY and SERIAL CARRY go low the clock to the counter stages is enabled. The logic level of PARALLEL CARRY must not be allowed to change while CLOCK is low or erroneous counts may result.

LATCH STROBE transfers the data in the counter stages to the latch storage to be displayed. With LATCH STROBE low, the latch flip-flops follow the states of the counter flip-flops. When LATCH STROBE goes high, the counter data is stored in the latch flip-flops. The counter can continue to count while the previous information is stored in the latches.

The DECIMAL POINT input controls the display of the decimal point. A high is required to turn on the LED decimal point display.

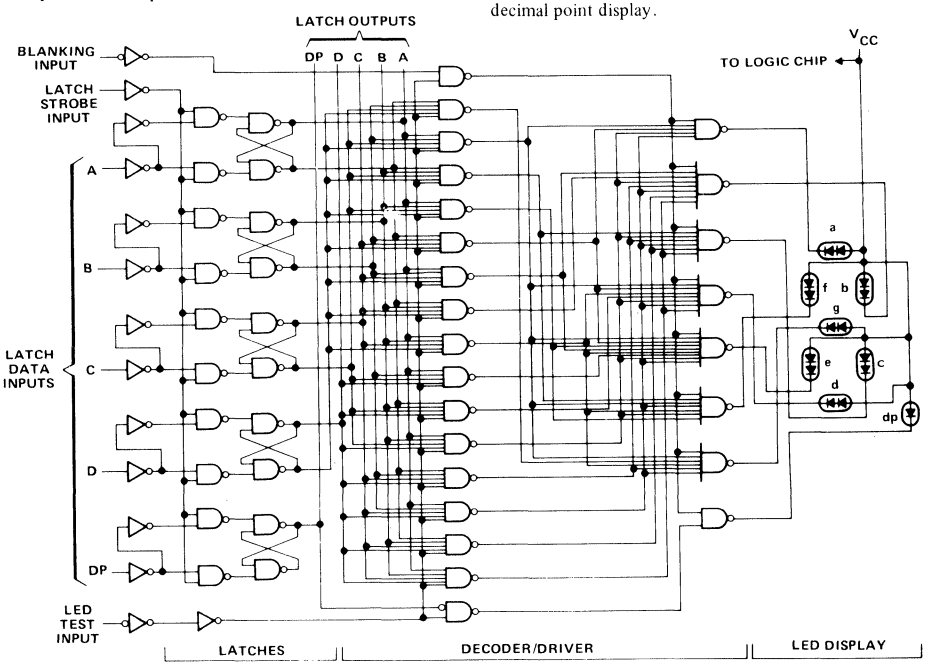


FIGURE 2. Functional Block Diagram of TIL308

A high on BLANKING inhibits the driver and gates and blanks the LED display. For normal operation, the BLANKING input must be low.

A low on RIPPLE BLANKING blanks the display if the latch flip-flops contain a count of zero. This combination also forces the RBO NODE to go low. By connecting the RBO NODE of one decade position to the RIPPLE BLANKING input of the next decade position, zero suppression can be achieved. This is discussed in detail in a later portion of this report, Counter Circuit Description. The RBO NODE has a resistor pullup, which allows this output to be used as an input. A low level applied to RBO will blank the LED display independently of other input.

The TIL308 looks physically identical to the TIL306. However, the TIL306 contains a counter section: the TIL308 does not. The TIL308 accepts 8-4-2-1 BCD code from external sources, stores it in latches, and displays the stored character by means of an LED display. As shown in Figure 2, the TIL308 consists of the three major sections: latch, decoder/driver, and LED display.

The inputs and outputs, designed to be TTL compatible, consist of DATA INPUTS, DATA OUTPUTS, LATCH STROBE, BLANKING, and LED TEST.

The BCD data and decimal point on the DATA INPUT lines are transferred into the latch flip-flops when LATCH STROBE is low. The BCD data and decimal point data stored in the latches are available at DATA OUTPUT. With LATCH STROBE high the DATA INPUT lines can change without effecting the data stored in the latches.

BLANKING must be high to display the data stored in the latches. When BLANKING goes low, the decoder drivers are inhibited and LED display is turned off. The data stored in the latches are not effected by BLANKING.

LED TEST can be used to test the LED display. A low to LED TEST will override all other signals and turn all of the LEDs on. LED TEST does not change the status of the latches.

With the basic operation of the circuits outlined, two typical interconnection methods are shown in Figure 3 and 4. Figure 3 shows the TIL306 connected in the synchronous mode. Figure 4 shows the TIL306 in the asynchronous mode. The asynchronous mode will be used in the following example of a counter.

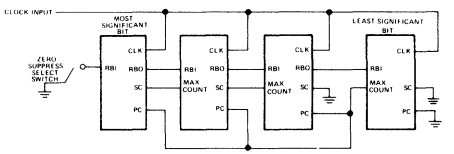


FIGURE 3. TIL306 Interconnections for Synchronous-Count Mode and High-Order-Zero Suppression.

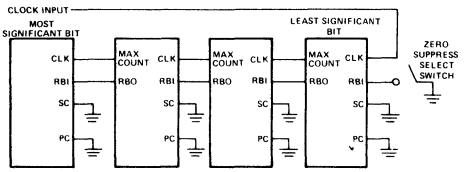


FIGURE 4. TIL306 Interconnections for Asynchronous-Counting Mode and Low-Order-Zero Suppression.

COUNTER CIRCUIT DESCRIPTION

The counter is a major constituent in digital instruments. Digital voltmeters, frequency counters, event counters, and period counters all have a circuit in common, very much like the one shown in Figure 4.

The circuit to be discussed in detail in this report incorporates both the TIL306 and the TIL308. One of the limiting factors of the TIL306 is that the counter typically does not count faster than 18 MHz. Combining the TIL306 with a TIL308 and feeding the TIL308 from a high-speed counter expands the system to a much higher frequency. Figure 5 shows a BCD counter capable of working at 100 MHz. The circuit consists of two SN74S112 Schottky

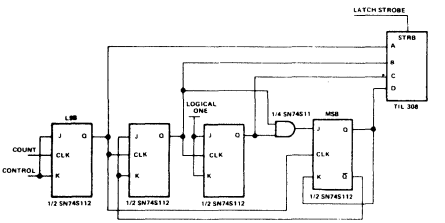


FIGURE 5. 100 MHz Decade Counter Using Texas Instruments Schottky TTL Logic and A TIL308 Display.

TTL circuits and one SN74S11 Schottky TTL circuit. This configuration results in an asynchronous BCD counter capable of dividing a 100-MHz signal down to 10 MHz. The speed is a result of Texas Instruments Schottky TTL devices that allow flip-flops to toggle in excess of 100 MHz. The Q outputs of the four flip-flops are fed into one TIL308, resulting in a decade with readout. The following decade position consists of a TIL306, which is capable of handling the 10 MHz rate. This circuit can be expanded even further by preceeding the Schottky counter stage with an ECL counter stage. ECL IC flip-flops with a 400-*MHz* toggle rate and discrete built ECL flip-flops with a toggle rate of 800 MHz are possible. Figure 6 shows a block diagram of a stage which is capable of counting up to 800 MHz. Since ECL levels do not coincide with TTL levels, an ECL-TTL converter is necessary. The output of the converter will drive the TIL308 without any interference caused by switching speed problems.

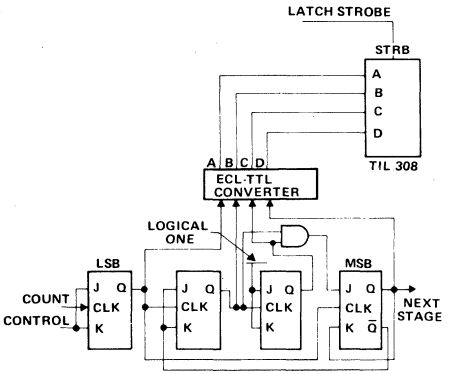


FIGURE 6. 800-MHz Decade Counter Using ECL Logic and A TIL308 Display.

TIL306 devices shows a big empty surface in the middle of the board and considerably fewer interconnects to the display. The cost savings resulting from using such a counter are quite obvious.

Figure 9 is a photo of a 100-MHz counter using seven TIL306 devices and two TIL308 devices. A compact assembly technique reduced the total size.

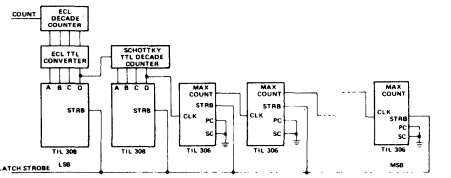
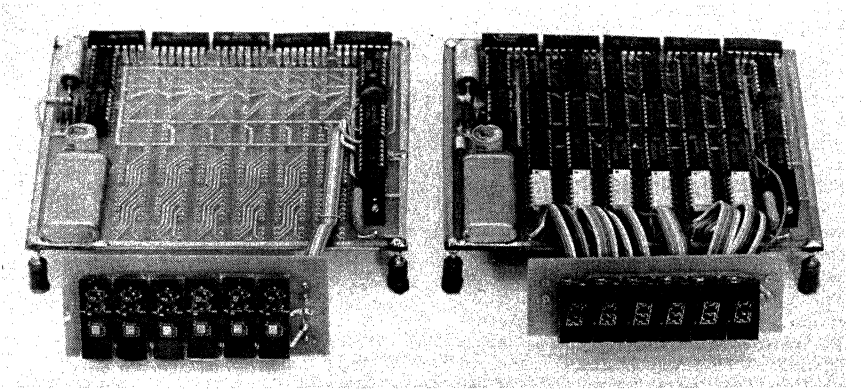


FIGURE 7. Nine-Digit Counter



A *B*

FIGURE 8. Two Counters with Identical Performance. Counter (A) Uses TIL306 Devices; Counter (B) Does not. Note how many less Components are Needed in the Counter Using TIL306 Devices.

Figure 7 is a block diagram representation of a nine-digit readout, consisting of an ECL decade counter with a TIL308 display and a Schottky TTL decade counter with a TIL308 display, as just described, and seven TIL306 devices. Part count is minimal, and the complexity of the PC Board is minimized.

Figure 8 is a photo of two counters with identical performance illustrating the difference in component count between a conventional counter consisting of SN7490, SN7475, and SN7447 TTL integrated circuits, resistors, with a display using TIL302 devices, and a counter using TIL306 devices. Both counters are specified to operate up to 15 MHz, using a six-digit readout. The counter using

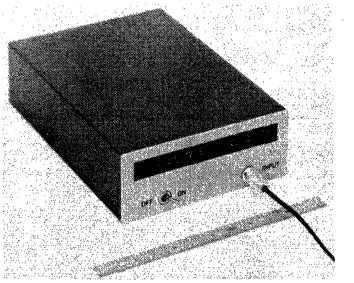


FIGURE 9. A Portable 100-MHz Counter Using Seven TIL306 Devices.

Figure 10 shows all of the basic circuit boards and components used in the counter shown in Figure 9 and shown schematically in Figure 12. The upper board is timebase. The center board is control. The bottom board is counter and display.

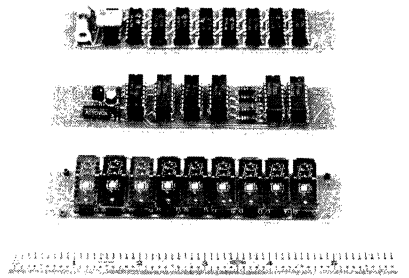


FIGURE 10. The Three Basic Circuit Boards of the Portable Counter.

in Figure 5 and seven TIL306 devices. This counter is capable of measuring frequencies up to 100 MHz and time with 10-nanosecond resolution. Again minimum part count and simplicity have been the major objectives. The unit is universal and the counter can be expanded into other functions by adding circuits to the basic building block.

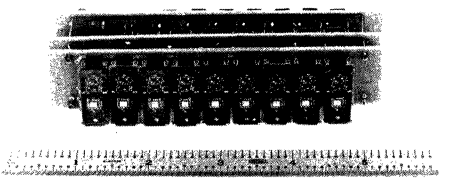


FIGURE 11. The Three Basic Circuit Boards Fastened Together into A Compact, High-Density Unit

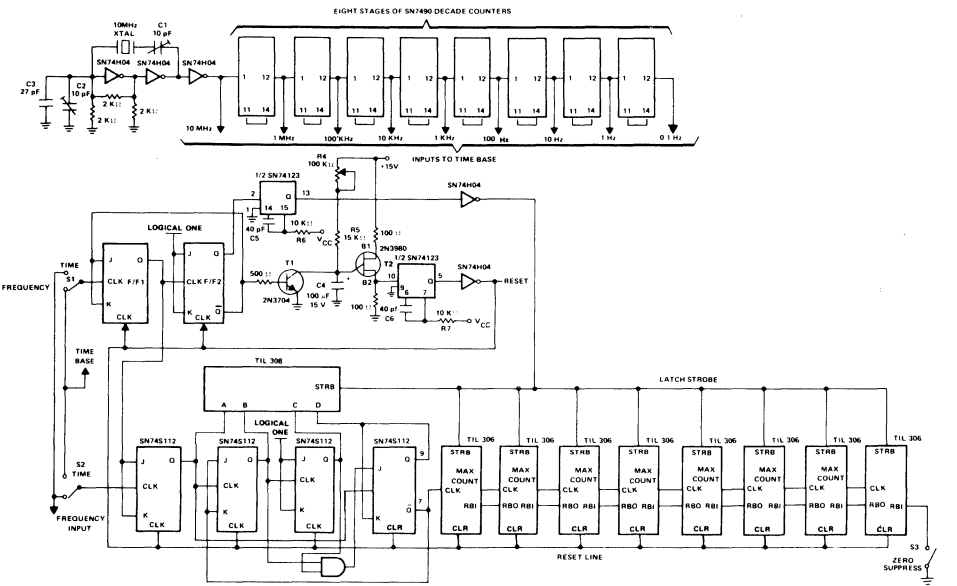


FIGURE 12. Schematic of A Frequency and Time Counter

Figure 11 shows the assembly technique for high density component packing. The total size is 1.2 inches high, 1.2 inches deep and 4.25 inches wide. This counter can be incorporated in a lightweight and portable instrument. Total power dissipation is 9 watts.

Figure 12 shows a complete schematic of a frequency and time counter incorporating the 100-MHz stage shown

The counter has three main functional sections: timebase, control, and counter.

The top part of Figure 12 is the time base. A 10-MHz oscillator is formed using two SN74H04 TTL high-speed inverters. The output is coupled through a third inverter to

isolate the oscillator from the rest of the circuit. Capacitor C1 is a coarse adjust and capacitor C2 is a fine adjust. C2 should be a piston capacitor to allow finer resolution during adjustment. For more accurate requirements, a separate oscillator in a temperature-controlled oven with AGC circuitry can replace this circuit. The output of the oscillator is fed into a divider chain consisting of eight SN7490 decade dividers. Timing signals from 10 MHz to 0.1 Hz are generated and switch selectable as the time base. In the middle of the schematic in Figure 10 is the control circuit. The purpose of the control circuit is to gate the counter, and to generate latch strobe, and reset signals.

The input of F/F1 is the time base signal in the frequency measuring mode or the unknown time period in the time measuring mode.

With all circuits reset, the $\overline{Q}$ output of F/F2 holds a high level at the JK inputs of F/F1. With a pulse coming into the F/F1, Q of F/F1 changes from 0 to 1 on the negative-going edge. This 1 is applied to the first stage of the counter, allowing it to count. F/F2 does not change state since it changes only on a negative-going edge. With the next pulse to the clock input of F/F1, F/F1 changes state on the negative-going edge, changing the Q output from logical 1 to logical zero. This negative-going transition sets F/F2 and at the same time stops the counter from counting. With F/F2 set, $\overline{Q}$ of F/F2 is a 0. A 0 at the JK inputs of F/F1 inhibits change with any additional pulses coming into its clock input. The Q output of F/F2 is connected to the input of a monostable multivibrator, 1/2 SN74123. This multivibrator generates a short positive-going pulse at the Q output. The pulse width is determined by the RC combination R6C5 and is set in this application to 150 nanoseconds. The output signal is inverted and applied to the Latch Strobe inputs of the TIL306 and TIL308 devices. This pulse transfers the data from the counters into the latches to be displayed.

The $\overline{Q}$ of F/F2 is connected to the JK inputs of F/F1 and also through a resistor to transistor T1. During counting operation $\overline{Q2}$ is high, turning T1 on and preventing C4 from charging. At the end of the count cycle, the $\overline{Q}2$ is low, turning T1 off. The capacitor C4 begins charging through resistors R4 and R5. R4 is adjustable and allows a variation in the display time. R5 prevents the charging current and the current through T1 from exceeding 1 mA when R4 is turned to zero. Once the charge across C4 reaches the firing potential of the unijunction, T2, the unijunction generates a positive pulse at Base 2, which is coupled into the monostable multivibrator, SN74123. The positive pulse determined by R7C6, 150 nanoseconds wide, is inverted by an inverter, 1/6 of SN74H04, and applied to the reset input of the TIL306 devices, the four F/Fs of the first counter stage, and the two F/Fs in the control section. With F/F1 and F/F2 reset the JK inputs are reset to a high level by F/F2 and the circuit is again ready to handle the incoming signal.

The bottom part of the schematic in Figure 10 shows the counter section. The first stage is made up of two SN74S112, one SN74S11, and one TIL308. The two SN74S112 circuits and one SN74S11 circuit form a decade counter consisting of four flip-flops and one gate. Schottky TTL devices are used because of the speed requirement. If only a 70-MHz counting rate is required, this circuit could be a single SN74196 circuit. The $\overline{Q}$ output of the fourth F/F is connected to the clock input of the first TIL306. The maximum count of the TIL306 is connected to the clock input of the next TIL306. This operation is the asynchronous mode, which is acceptable for counter purposes.

The counter is controlled by the two inputs to the first F/F of the first decade. The clock input is the unknown frequency in the frequency mode, or the known time pulses from the time base in the time-measuring mode. The JK inputs are connected to the Q output of the control F/F. This signal gates the counter. As already explained, a high level to the JK inputs allows the F/F to change state on a negative edge of a pulse applied to the clock input. With the JK inputs low, the clock input does not affect the F/F.

To complete the operation of the counter, the Latch Strobe and the Reset are applied to the circuit as shown. S3 allows choosing between suppression or displaying of zeroes to the left of the most significant digit. With the switch closed, a ground is applied to the ripple blanking input of the most significant digit. If this digit is a zero, the display is blanked and the ripple blanking output goes zero. This output is connected to the next digit and the process repeated until all leading zeroes are suppressed. If switch S3 is opened the high-order zeroes are displayed. All that is necessary for operation of the counter now is to provide a power supply and a signal to be counted.

optocouplers in circuits

There are many situations in which information must be transmitted between switching circuits electrically isolated from each other. This isolation has been commonly provided by relays, isolation transformers, and line drivers and receivers. There is, however, another device that can be used quite effectively to solve these problems. This device is the optocoupler. The need for the optocoupler is most prominent in areas where high voltage and noise isolation, as well as small size, are considered important. By coupling two systems together with the transmission of radiant energy (photons), the necessity for a common ground is eliminated — the main purpose of the optocoupler — and the systems can be effectively isolated.

Four Texas Instruments optocoupler devices, the TIL102, TIL103, TIL120, and TIL121, are discussed in this report. How these devices can be used in various circuits to provide proper isolation in many systems will be a key part of this discussion. There are many circuit applications for optocouplers; however, the ones offered in this report are just several which can be of special use. Complete specifications for these devices are not included here but are available elsewhere in this book.

description of an optocoupler

Basically, a Texas Instruments optocoupler consists of a GaAs (gallium arsenide) infrared-emitting diode (IRED) as the input stage and a silicon n-p-n phototransistor as the output stage. The coupling medium between diode and sensor is an infrared-transmitting (''IR'') glass, as used in the TIL102/TIL103, TIL120/TIL121. Photons emitted from the diode (emitter) have wavelengths of about 900 nanometers. The sensor transistor responds most efficiently to photons having this same wavelength. Consequently, the input and output devices are spectrally matched for optimum transfer characteristics.

Equivalent circuits for the TIL102/TIL103 and TIL120/TIL121 are shown in Figures 1 and 2. For both families of devices, a current source between the collector and base of the sensor is used to represent the virtual base current generated by incident photons striking the base. This base current is proportional to the amount of radiation emitted from the diode. The collector-base and base-emitter junction capacitances are shown for both devices since they are used to determine the rise and fall times of the output current waveform. Because a relatively large transistor base area is necessary for increased sensor efficiency, the collector-base junction capacitance is fairly large.

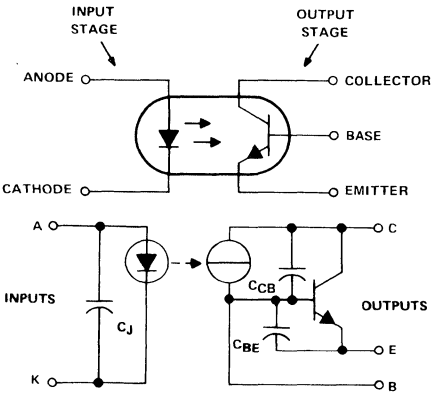


FIGURE 1. Terminal Connections and Equivalent Circuit for the TIL102/TIL103

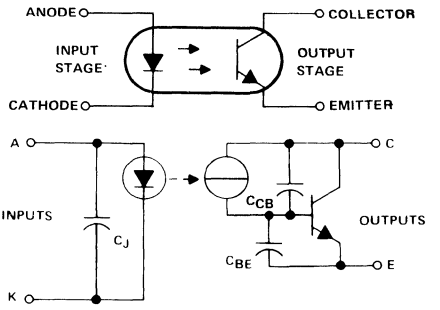


FIGURE 2. Terminal Connections and Equivalent Circuit for the TIL120/TIL121

characteristics of an optocoupler

To fully utilize the advantages offered by an optocoupler, it is necessary that the circuit designer become aware of some of its characteristics. The difference in characteristics between the families is attributed mainly to the difference in construction.

The characteristics most useful to the designer are as follows:

1. High-voltage isolation. High-voltage isolation between the inputs and outputs is obtained by the physical separation between emitter and sensor. This isolation is possibly the most important advantage of the optocoupler. These devices can withstand large potential differences, depending on the type of coupling medium and construction of the package. The IR glass separating the emitter and sensor in the TIL102/TIL103 and TIL120/TIL121 has an isolation capability of 1000 V. The isolation resistance is greater than 10^{12} Ω.
2. Noise isolation. Electrical noise in digital signals received at the input of the optocoupler is isolated from the output by the coupling medium. Since the input is a diode, common-mode noise is rejected.
3. Current gain. The current gain (output current/input current) of an optocoupler is largely determined by the efficiency of the n-p-n sensor and by the type of transmission medium used. For the TIL103, the current gain is greater than unity, which in many cases eliminates the need for current amplifiers in the output. However, both the TIL102/TIL103 and TIL120/TIL121 have output current levels that are compatible with inputs of digital integrated circuits such as 54/74 TTL. Figures 3 and 4 show typical input-to-output current relationships.
4. Small size. The dimensions of these devices enable them to be used on standard printed-wiring boards. The TIL102/TIL103 and TIL120/TIL121 are built in a metal can similar to a transistor package. The physical dimensions of these packages are shown in Figures 5 and 6.

These are some of the prime characteristics of an optocoupler that can be used effectively to isolate two systems.

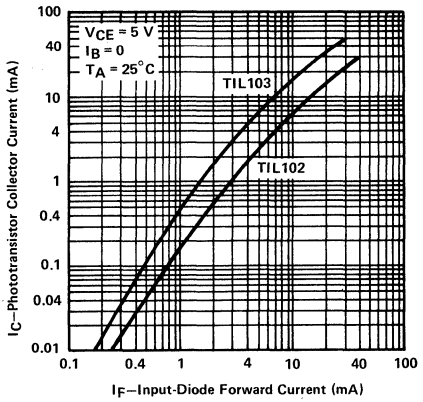


FIGURE 3. Typical Input/Output Current Relationship for the TIL102/TIL103

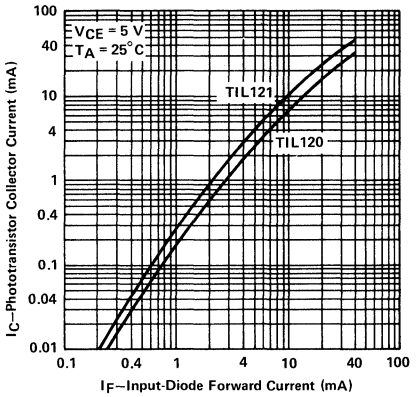
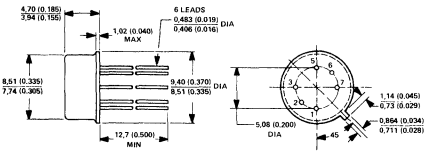
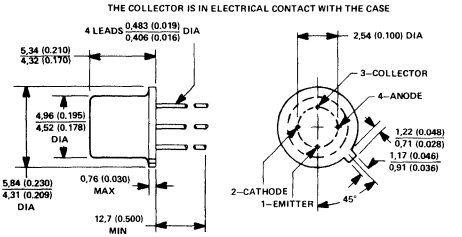


FIGURE 4. Typical Input/Output Current Relationship for the TIL120/TIL121



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FIGURE 5. Dimensions of the TIL102/TIL103



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FIGURE 6. Dimensions of the TIL120/TIL121

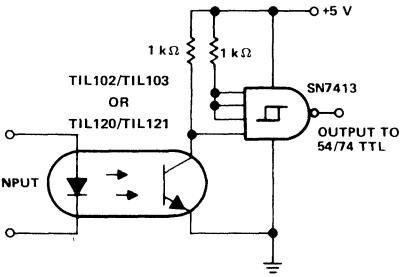
typical circuit applications

The characteristics and advantages of an optocoupler enable the designer to use it in a wide range of circuit applications. Important among the applications of an optocoupler are those involving 54/74 TTL and similar digital integrated-circuit families. As was mentioned previously, an optocoupler has output currents compatible with TTL inputs. This compatibility enables it to be especially attractive as an interface element between digital systems. The device is particularly beneficial in applications where high voltage differences may exist between systems. However, it is not limited only to digital applications, as shown by the following examples.

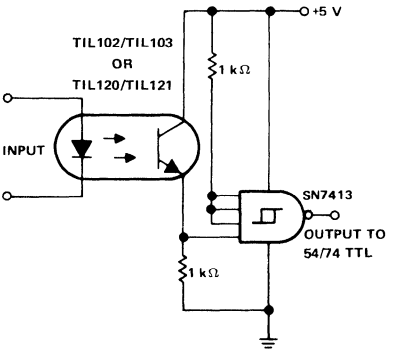
driving 54/74 TTL

An effective method of coupling an optocoupler to TTL circuitry is by using a Schmitt trigger that has an output level compatible with standard TTL devices. By coupling any of the Texas Instruments optocouplers to the SN7413, as shown in Figure 7, the isolated signal at the input can be converted to TTL logic levels. Noise immunity is provided by the coupler as well as by the threshold level of the SN7413.

The optocoupler can also be employed as part of a Schmitt trigger circuit that utilizes discrete components. Because the output of the optocoupler is a transistor, it can be used as the input stage to the



(a) NON-INVERTING FUNCTION



(b) INVERTING FUNCTION

FIGURE 7. Schmitt Trigger Coupling Optocoupler to 54/74 TTL Inputs

trigger as shown in Figure 8. For this circuit, regeneration or positive feedback is provided by the coupled emitters of Q1 and Q2. The output of this circuit is noninverting and is compatible with TTL logic.

Another Schmitt trigger utilizing discrete components that makes use of the base connection of the TIL102/TIL103 is shown in Figure 9. In this circuit, positive feedback is provided from the collector of Q2 to the base of Q1. Resistor R1 limits the base current to Q1 and keeps the device off when there is no signal at the emitter. As with the circuit in Figure 8, the output of this circuit is noninverting and compatible with TTL levels.

transmission-line isolator

By using an optocoupler between two systems coupled by a transmission line, effective line isolation can be achieved. Figure 10 shows a typical interface

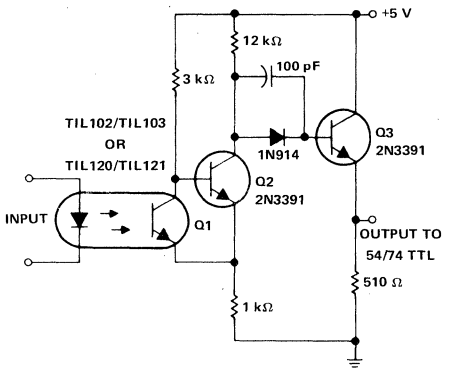


FIGURE 8. Optocoupler with Discrete-Component Schmitt Trigger for Driving 54/74 TTL

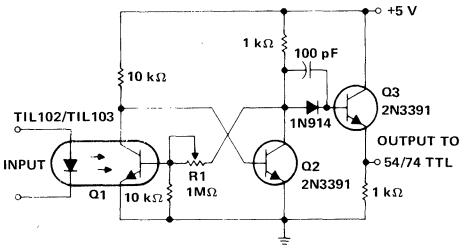


FIGURE 9. TIL102/TIL103 in a Schmitt Trigger for Driving 54/74 TTL

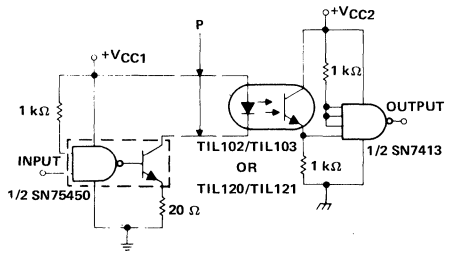


FIGURE 10. Typical Transmission Line Isolator

system using TTL integrated circuitry coupled by a twisted-pair line. The SN75450B is the input stage driving the transmission line and emitter of the optocoupler. The IRED requires about 20 mA during "turn-on," which is well below the maximum current rating of the transistor. At the receiving end of the line, the phototransistor is coupled to an SN7413 for fast pulse generation. The output of this system is a noninverted pulse. However, by rearranging the optocoupler and the SN7413 as shown in Figure 7(a), the output may be inverted.

As simple as it seems, employing an optocoupler this way provides isolation for both noise and high voltage. An isolation transformer or relay could accomplish the task, but it would not be as fast as the optocoupler. Also, a line driver and receiver combination could be used to eliminate the noise and increase the speed, but it would be very ineffective if there were high potential differences between the input and output.

solid-state relay

Through the use of transistor circuits, mechanical relays are slowly being replaced by solid-state relays. In some cases, the solid-state relay (SSR) offers distinct advantages over its mechanical counterpart. For example, an SSR has the advantage that it has neither moving parts nor fragile wires, and it has faster switching speeds and longer operating life. However, one disadvantage of an SSR is that it generally has a lower degree of input/output isolation than a mechanical relay. To overcome this disadvantage in the SSR, an optocoupler can be used as the isolating input stage as shown in the block diagram in Figure 11. The control stage may consist of discrete transistors or integrated circuits, while the output stage consists of high-power switching devices.

A simple isolated latch circuit, which is somewhat of an SSR, is shown in Figure 12. The output of the optocoupler is used to fire the SCR that provides power to the load. To turn off the load current, the supply voltage V_{CC2} must be removed.

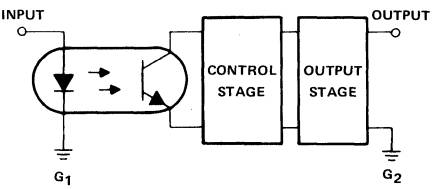


FIGURE 11. Typical Solid-State Relay Using an Optocoupler

isolated chopper circuit

Chopper circuits that use mechanical relays suffer from a speed problem as well as switching transients

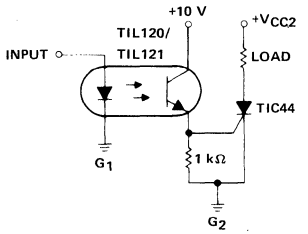


FIGURE 12. Solid-State Latch Using a TIL120/TIL121

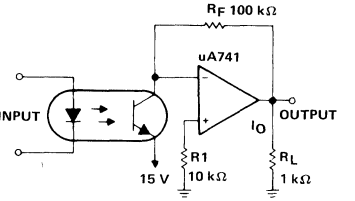


FIGURE 14. Isolated Pulse Amplifier Using Optocoupler uA741 Operational Amplifier

at the load. By using bipolar transistors or FETs as series and shunt switching elements, the speed may be improved; but capacitive coupling to the switching circuitry may still produce transient "spikes" on the output signal. By using an optocoupler to switch the input signal as shown in Figure 13, the switching circuitry can be isolated from the output, thereby

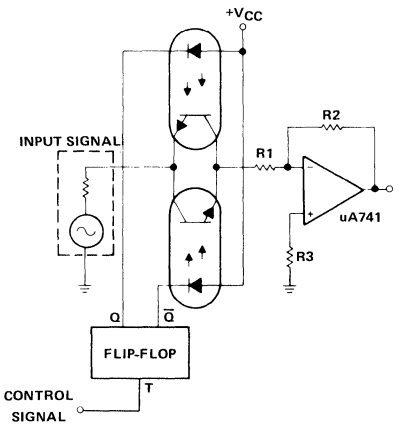


FIGURE 13. Chopper Circuit Using Optocouplers

reducing output "spikes". The use of two couplers in the configuration shown allows chopping of either positive or negative input signals with a frequency of one-half that of the input to the flip-flop. The uA741 operational amplifier is used to increase the output signal with a gain of R2/R1.

pulse amplifiers

Pulse amplification, as well as isolation, can be achieved by using an optocoupler with a pulse amplifier. The circuit shown in Figure 14 uses an isolator with a uA741 operational amplifier to amplify the pulse appearing at the anode of the IRED. The gain of this circuit is controlled by the feedback resistor R_F. An amplifier employing discrete components and that uses the TIL102/TIL103 as part of the current feedback pair is shown in Figure 15. The feedback resistor R1 controls the current gain as well as the output d-c level.

Figure 16 shows an optocoupler with a voltage-feedback amplifier that has a gain of 1 + R2/R1. This type of amplifier offers high input impedance, which will not load the emitter of the sensor transistor.

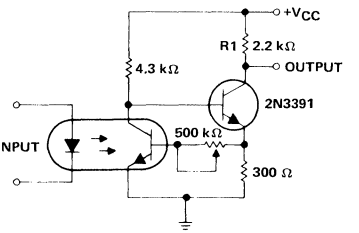


FIGURE 15. Discrete-Component Pulse Amplifier with TIL102/TIL103

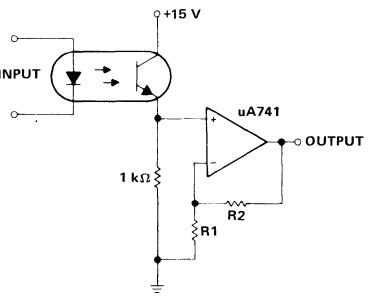
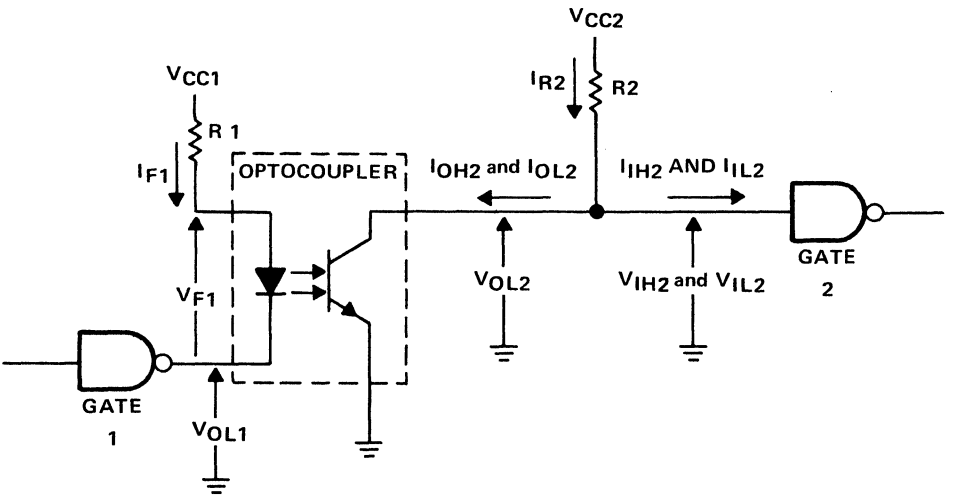


FIGURE 16. Voltage-Feedback Pulse Amplifier with Optocoupler

Interfacing Using Optocouplers

Description

A very useful application of optocouplers is in the interface between different families of digital logic circuits. The worst-case design process should include consideration of data rates, power supply variations, component tolerances, and temperature ranges as well as the characteristics of the digital logic families. Consider the general circuit of Figure 1.



NOTE: V_{OL2} = low-level output voltage of coupler when coupler is on.
V_{IL2} = low-level input voltage specified for GATE 2.

Figure 1. Optocoupler Interface Circuit

When the output of logic circuit 1 is low (V_{OL1}), the output of the optocoupler is also low (V_{OL2}). Since V_{OL2} is the input to logic circuit 2, it must be less than the maximum required logic low input voltage (V_{IL2}), in order to hold logic circuit 2 in a stable state. The criteria that must be met at this point is given in equation (1).

$$V_{OL2}\ (\text{coupler}) \leq V_{IL2}(\text{max})\ (\text{logic circuit}) \quad (1)$$

When the coupler output is in the low state, it must not only sink the current through R2, I_{R2}, but is must also sink any current required out of the logic circuit 2 input in order to hold logic circuit 2 input to V_{IL2} or less.

Using the current directions specified in Figure 1 and with the conditions of equation (1) satisfied, the conditions required for the coupler current, I_{OL2}, can be expressed as in equation (2).

$$I_{OL2} \geq I_{R2} - I_{L2} \tag{2}$$

The first step in the design procedure is to select I_{F1}, the forward current through the emitter of the optocoupler. Then using equation (3), R1 is computed:

$$R1 = \frac{V_{CC1} - V_{F1(typ)} - V_{OL1(typ)}}{I_{F1(typ)}} \tag{3}$$

A standard value resistor for R1 is selected as close to the value computed using equation (3). A tolerance for this resistor is specified from which the maximum and minimum values for R1 are computed using equations (4a) and (4b) as follows:

$$R1(max) = R1\left(1 + \frac{tol}{100}\right) \tag{4a}$$

$$R1(min) = R1\left(1 - \frac{tol}{100}\right) \tag{4b}$$

"tol" is the percent tolerance of the resistor. With the results of operations (4a) and (4b), the maximum and minimum values of I_{F1} and be determined using equations (5a) and (5b).

$$I_{F1(max)} = \frac{V_{CC1(max)} - V_{F1(min)} - V_{OL1(min)}}{R1(min)} \tag{5a}$$

$$I_{F1(min)} = \frac{V_{CC1(min)} - V_{F1(max)} - V_{OL1(max)}}{R1(max)} \tag{5b}$$

The output current of the coupler depends on the current transfer ratio (CTR) of the device. CTR is defined by equation (6a) as the coupler output current, I_{OL2}, divided by the forward current, I_{F1}, of the coupler diode emitter.

$$CTR = \frac{I_{OL2}}{I_{F1}} \tag{6a}$$

If CTR is not given as a data sheet parameter, it can be calculated from other data sheet specifications [e.g., $I_{C(on)}$ at a certain I_F] or from curves of I_{OL} (sometimes called I_C) versus I_F given in the data sheet. In many cases, CTR will be a number less than one, in other cases it will be greater than 1.

Using equation (6a) with CTR converted to a percent, the coupler collector current can be computed using equation (6b).

$$I_{OL2(min)} = \frac{(\%\ CTR) \times I_{F1(min)}}{100} \tag{6b}$$

The minimum value for R2 can be calculated using equation (7).

$$R_{2(min)} = \frac{V_{CC2(max)} - V_{OL2(max)}}{I_{OL2(max)} + I_{L2(max)}} \tag{7}$$

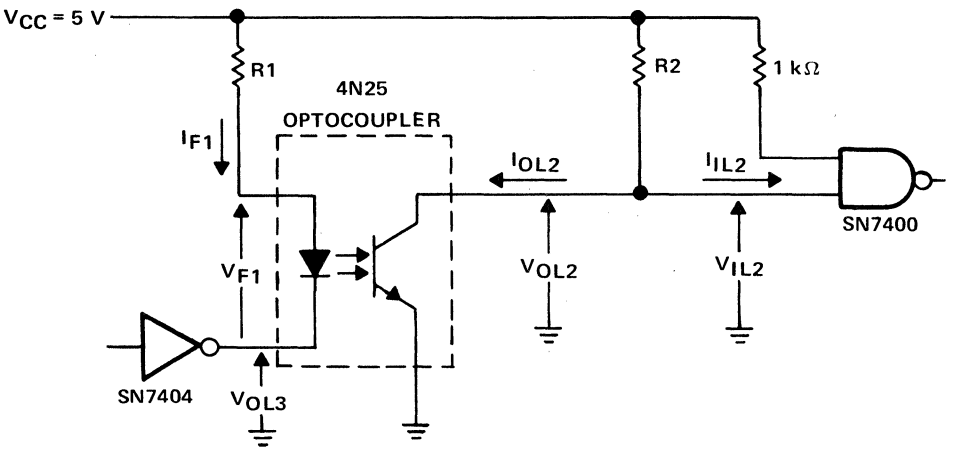
The maximum value of R2 is determined from the condition that exists when the optocoupler output transistor is in the off state. Under these conditions, any off-state current, I_{OH}, and any current into the input of gate 2 must not drop the voltage across R2 to the point where the input to gate 2 goes below its required high-level limit value, V_{IH}. These limit conditions are expressed in equation (8), again using Figure 1. I_{OH2} is the current into the output collector and I_{IH2} is the input current to gate 2 when the gate input is at a voltage equal to or greater than the $V_{IH(min)}$ voltage required. $I_{OH2(max)}$, $V_{IH(min)}$, and $I_{IH2(max)}$ are taken from data sheet specifications.

$$R2(max) = \frac{V_{CC2(min)} - V_{IH2(min)}}{I_{OH2(max)} + I_{IH2(max)}} \tag{8}$$

R2 is selected between the limits of R2(min) and R2(max). Capacitive effects on response time are less when R2 is closer to R2(min), while maintaining the low-logic-level voltage, V_{IL2}. As the CTR of the optocoupler degrades, correct circuit operation will be maintained longer with R2 closer to R2(max). Final selection depends on which parameter is more important in the application.

Example Number 1

In Figure 2, a 4N25 optocoupler is to be driven by an SN7404 gate output and will drive the input of an SN7400 gate. The specifications for the logic levels and input and output currents for the Series 74 logic family are given in Table 1.



NOTE: V_{OL2} = low-level output voltage of coupler when coupler is on.
V_{IL2} = low-level input voltage specified for SN7400.

Figure 2. Optocoupler Interface Circuit

Table 1. Series 74 Family Data

TTL Family	V_{IL} V	I_{IL} mA	V_{IH} V	I_{IH} μA	V_{OL} V	I_{OL} mA	V_{OH} V	I_{OH} μA
74	0.8	−1.6	2	40	0.4	16	2.4	−400
74ALS	0.8	−0.1	2	20	0.5	8	2.4	−400
74AS	0.8	−0.5	2	20	0.5	20	2.5	−2000
74LS	0.8	−0.3	2	20	0.5	8	2.7	−400
74S	0.8	−2	2	50	0.5	20	2.7	−1000

For the particular calculations, the values in Table 2 will be used.

Table 2. Calculation Values

TTL	4N25	POWER SUPPLY
$V_{IH(min)}$ = 2 V	CTR(min) = 20%	V_{CC} = 5 V ±5%
$V_{IL(max)}$ = 0.8 V	$V_{F(min)}$ = 1.2 V @ 10 mA	
$I_{IH(max)}$ = 40 μA	$V_{F(typ)}$ = 1.25 V @ 10 mA	
$I_{IL(max)}$ = −1.6 mA	$V_{F(max)}$ = 1.5 V @ 10 mA	
$I_{OH(max)}$ = 400 μA	$I_{OH(max)}$ = 50 nA	
$V_{OL(typ)}$ = 0.2 V	$V_{OL(max)}$ = 0.5 V	
$V_{OL(max)}$ = 0.4 V		

Calculations

1) Select $I_F = 20$ mA

2) Check equation (1)
V_{OL}(coupler) $\leq V_{IL2}$ (logic circuit) 0.5 V $\leq$ 0.8 V. It checks.

3) From equation (3), assuming the V_F at 20 milliamperes is not 0.05 volt greater than the value at 10 milliamperes.

$$R1 = \frac{5 - 1.25 - 0.2}{20 \text{ mA}}$$

$$R1 = 178\ \Omega$$

4) Select standard value R1 = 180 Ω ± 10%.

Therefore,

R1(max) 180 + 18 = 198 Ω
R1(min) 180 − 18 = 172 Ω

5) From equations (5a) and (5b), using $V_{OL(typ)} = 0.2$ V for $V_{OL(min)}$

$$I_{F1(max)} = \frac{(5.25 - 1.2 \text{ V} - 0.2) \text{ V}}{171\ \Omega} = 21.38 \text{ mA}$$

$$I_{F1(min)} = \frac{(4.75 - 1.5 \text{ V} - 0.4) \text{ V}}{198\ \Omega} = 14.39 \text{ mA}$$

6) The maximum current [$I_{OL2(max)}$] that can be allowed to flow through the coupler output is determined by the minimum current the coupler can supply according to equation (6b), thus

$$I_{OL2(max)} = \frac{14.39 \text{ mA} \times 20}{100} = 2.878 \text{ mA}$$

7) From equation (7),

$$R2(min) = \frac{(5.25 - 0.5) \text{ V}}{2.878 \text{ mA} + (-1.6 \text{ mA})} = 3.72 \text{ k}\Omega$$

8) From equation (8),

$$R2(max) = \frac{4.75 - 2}{50 \text{ nA} + 40\ \mu\text{A}} = 68.66 \text{ k}\Omega$$

8) From equation (8),

$$R2(max) = \frac{4.75 - 2}{50\ nA + 40\ \mu A} = 68.66\ k\Omega$$

A choice of 4.7 Ω ± 10% for R2 is suitable for this design.

Example Number 2

A similar approach can be used when interfacing discrete phototransistors to digital logic circuits. Consider a TIL602 connected in the phototransistor mode to an SN7400 as shown in Figure 3. The data for this situation is shown in Table 3.

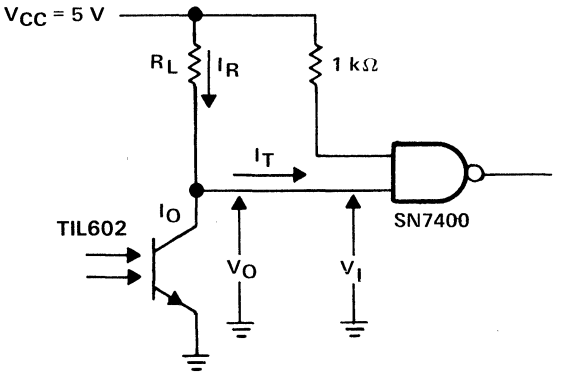


Figure 3. Phototransistor Interface Circuit

Table 3. Calculation Values

SN7400	TIL602	POWER SUPPLY
$V_{IH(min)}$ = 2 V	I_D = 3 μA (dark current)	V_{CC} = 5 V ± 5%
$V_{IL(max)}$ = 0.8 V	$I_{OH} = I_D + (1 - n/100)\ I_{OL}$	
$I_{IH(max)}$ = 40 μA	(where n = % light blocked)	
$I_{IL(max)}$ = −1.6 mA	$V_{OL(max)}$ = 0.8 V	
$I_{OH(max)}$ = 40 μA	$I_{OL(min)}$ = 2 mA	
$V_{OL(typ)}$ = 0.2 V		
$V_{OL(max)}$ = 0.4 V		

Calculations

In this application, the equations before equation (7) are ignored. From equations (7) and (8), the values for R2(min) and R2(max) can be calculated. This application is very sensitive to ambient light. Therefore, care must be taken to shield out ambient light.

Assuming 95% of the ambient light is shielded out,

$$R_{L(min)} = \frac{5.25 - 0.8}{2\ mA + (-1.6\ mA)} = \frac{4.45\ V}{0.4\ mA} = 11.1\ k\Omega$$

$$R_{L(max)} = \frac{(4.75 - 2.0)\ V}{I_{OH} + 40\ \mu A}$$

Substituting $I_{OH} = I_D + [1 - (n/100)]\ I_{OL}$, where n = 95%

$$R_{L(max)} = \frac{4.75 - 2.0}{3\ \mu A + (1 - \frac{95}{100})\ 2\ mA + 40\ \mu A}$$

$$= \frac{2.75\ V}{3\ \mu A + 100\ \mu A + 40\ \mu A}$$

$$= \frac{2.75\ V}{143\ \mu A}$$

$$= 19.2\ k\Omega$$

R_L is chosen as a standard value, 14.7 kΩ.

Example Number 3

If the 74LS series is used with 80% light blocked, from Table 1 $I_{IL(max)} = 0.36$ mA instead of 1.6 mA and $I_{IH(max)} = 20\ \mu A$ instead of 40 μA.

$$R_{L(max)} = \frac{4.75 - 2}{3\ \mu A + (1 - 80/100)\ 2\ mA + 20\ \mu A} = 6.5\ k\Omega$$

and

$$R_{L(min)} = \frac{5.25 - 0.8}{2\ mA + (-0.36\ mA)} = 2.71\ k\Omega$$

Therefore, R_L can be selected between 2.71 kΩ and 6.5 kΩ.

CCD OUTPUT SIGNAL PROCESSING

This application report presents a variety of methods, along with circuit examples, of converting the CCD output pulse-train into usable analog or digital video data. A general block diagram of a complete CCD operating system from clock-drive control through processed signal to output video is provided in Figure 1. Figure 1 illustrates four methods of obtaining analog or digital video. To understand these methods, a discussion of CCD output signal with respect to the desired video output and the data rates is first required. After the output signal discussion, each of the methods is described in detail.

Output Signal Considerations

The normal unprocessed CCD output signal is a voltage pulse-train in which the negative (lower) envelope represents analog video and its positive (upper) envelope is the result of the positive-going reset clock. This upper envelope is generally uniform and is generally representative of the zero or dark signal. The entire voltage pulse-train is displaced from zero volts by the positive quiescent-output operating voltage of the charge-detection amplifier. This output operating voltage is guaranteed to be above 5 V but less than the amplifier drain supply, V_{DD}.

The minimum reset-time interruption in each data-pulse is 50 ns. Since the duration of each data-pulse decreases as the frequency (number of data-pulses per second) increases, the percentage of data time occupied by the reset pulse is variable. For frequencies between 5 MHz and 10 MHz, the percentage varies between 25 and 50%. As the rise and fall times are approximately 10 ns, this percentage increases as the duration of the data-pulse decreases. Figure 2 shows an example of the output of a TC101 operated at 10 MHz. The negative (lower) output voltage waveform is 50 ns or 50%. This time is not always obtainable; however, even at 25 ns, a good output can be processed.

An example of this low duty cycle is shown in the area output of the CCD at 7 MHz (see Figure 3). Ringing is another factor that can reduce the true-data time. Ringing is caused by the reset and transport clocks. This problem can be greatly reduced in the following ways:

1. Making the high-to-low transition of the reset clock coincide with the transition of the transport clock.
2. Use 10 Ω to 20 Ω series transport-clock drive resistors and 50 Ω to 80 Ω reset-clock series resistors.

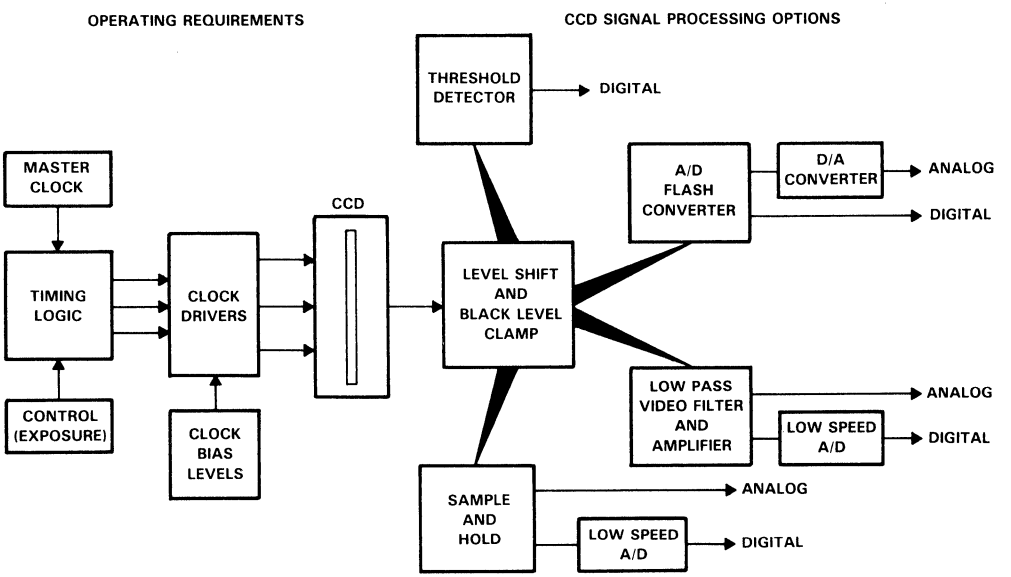


Figure 1. CCD Operating System Block Diagram

3. Using the shortest possible leads, return the clock-driver positive and negative supply bypass capacitors (1 μF for negative and 0.1 μF for positive) to the substrate pin (V_{SS}) nearest the transport or signal-clock pins and by connecting the PC board ground plane to the V_{SS} pin.

For data operating frequencies below 2 MHz, the data pulse is wider and the percentage of reset interruption is reduced (can be 10% or less) and the problem of reduced true data-time decreases (see Figure 4). The CCD output waveforms shown in Figures 2 through 4 cover the data-rate range and lay the groundwork for a discussion of output video requirements.

Positive analog video is a continuously varying signal with white more positive than black. Black should be 0.1 V or less above 0. In the CCD output, the envelope of the pulse train is negative video (white is the negative direction).

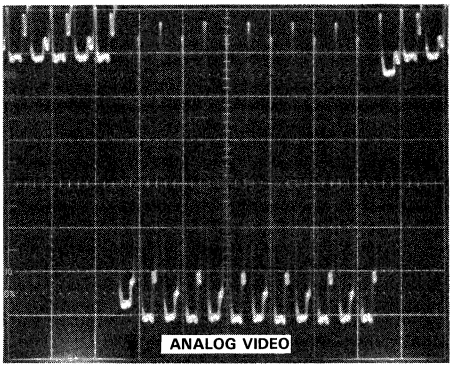


Figure 2. TC101 Output Signal, High-Frequency (10 MHz) Operation

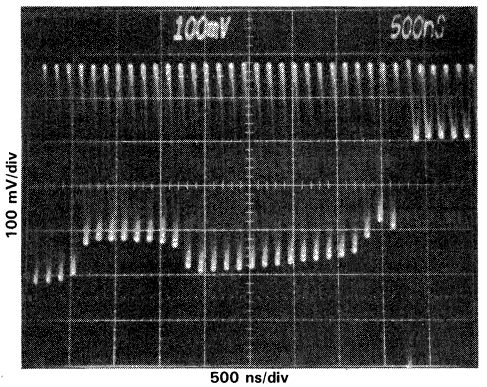


Figure 3. Low Duty Cycle Output (7.16 MHz) Signal

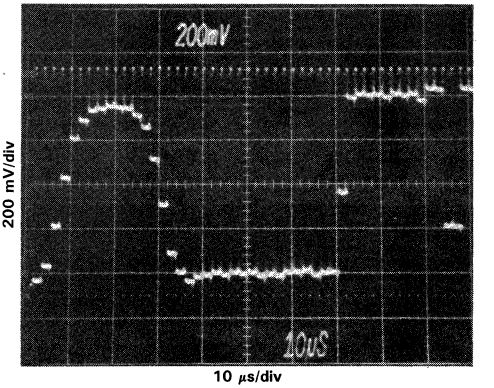


Figure 4. High Duty Cycle Output (0.5 MHz) Signal

Inversion is required after the negative envelope is detected. Also, the black level is the smallest negative output. Since it can be inverted at any time, the signal should be processed as negative video and inverted after processing. This black-level voltage is the reference for all the gray shades of negative voltage below it. The reference level is still needed even if only threshold detection is the required output.

Because the output signal dc operating voltage is variable, a level shift technique that can be keyed to the black level of the CCD output signal is required to establish the desired stable reference. Therefore, all signal processing methods in Figure 1 start with a level shift and black level clamp circuit. Figure 5 shows the level shift accomplished by a coupling capacitor that is large enough so that no significant change in charge occurs during a video-line readout time. Four black reference pulses are placed before

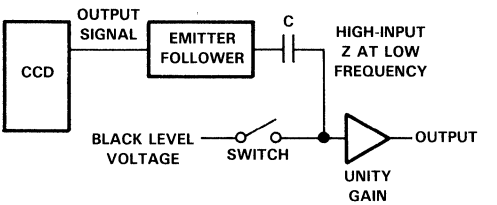


Figure 5. Low-Level Shift and Black Level Clamp Block Diagram

and after four isolation pulses at the beginning and end of the data pulse train. This is done so that, during these black reference pulses, the switch closes so the charge on the capacitor is clamped during the black reference output time of the CCD. The output of the amplifier then becomes the black reference voltage. This method of restoring black to a video data line is called line clamping. This method is widely used in video circuit design.

Another method of providing the level shift and black level clamp employs a programmable reference diode, the TI TL431C (see Figure 6). This method is unique in that it is all direct-coupled and therefore must have automatic drift-correction for the shift in CCD amplifier dc output voltage, as well as for other temperature induced component drifts.

However, like the line-clamped capacitor method, this circuit stores a charge on the capacitor, C. The charge on the capacitor determines the output black reference voltage for the period of one readout line. The basic components in the simplified schematic shown in Figure 6 operate as described in the following paragraphs.

The major output signal path begins with the output voltage of the CCD being applied to the base of the signal-buffer emitter follower (2N3904). The path proceeds through the programmable reference diodes and ends at the level-shifted output. A load resistor and a negative supply provide the operating current so that the output black level can be zero or negative if desired. The FET resistor divider controls the voltage drop through the reference diode and the FET capacitor provides a temporary memory for the gate bias of the FET over a line period. The comparator automatically controls the output for correct FET gate bias voltage. Thus the reference diode drops the correct value so that the output matches the set in black reference voltage during the black reference pulse in the output signal train, which is the strobe time for the comparator. The comparator is strobed on for each of the four black reference pulses so that, during each pulse, charge current to the storage capacitor makes needed corrections. In this manner, the comparator automatically tracks changes to maintain the desired black reference output voltage.

In the actual circuit (Figure 7), the black level is clamped to zero volts within the limits of the offset voltage of the comparator. Also, the charge current sent to the storage capacitor is the difference between the current from the 22 MΩ resistor and the current from the 2N3904 voltage-to-current converter for the comparator. The 1-μF comparator provides good ac coupling.

Threshold Detection

The preceding discussion covers the subjects of level shift black-level clamp. The following is a discussion of the various methods of signal processing. The first method as shown in Figure 1 is threshold detection. The threshold-type processor consists of the following three main elements:

1. The level shift and black-level clamp circuit (see Figure 7)
2. A comparator with a negative threshold reference
3. A data-clocked D Type flip-flop to act as a sample-and-hold.

This threshold-type processor has a true TTL output that is zero for gray shades darker than the preset threshold and a one for gray shades lighter than that threshold (see Figure 8). The timing of the black-level strobe and the data clock for the flip-flop is important in getting correct operation. A complete circuit for a TC102 is presented in Figure 9, starting with a master clock driving the timing logic with exposure control and finishing with CCD clock drivers.

The clock oscillator frequency sets the data rate and the monostable multivibrator triggered by the clock sets the reset clock pulse duration. Dividing the clock oscillator output by two produces the transport clock signal for each transport clock cycle. This signal goes to the preset input of the second flip-flop. There it is synchronously released to the clock-driver level translation transistor on command by the borrow output of the exposure-time down-counter chain to the clock input of the flip-flop.

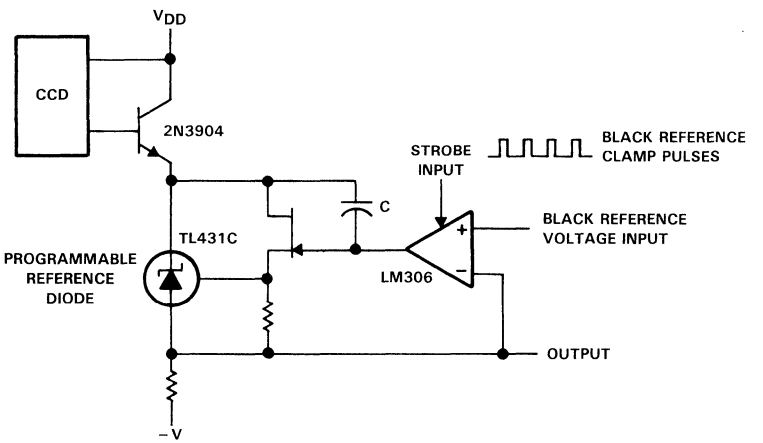


Figure 6. Level-Shift and Black-Level Clamp with Automatic Drift Correction

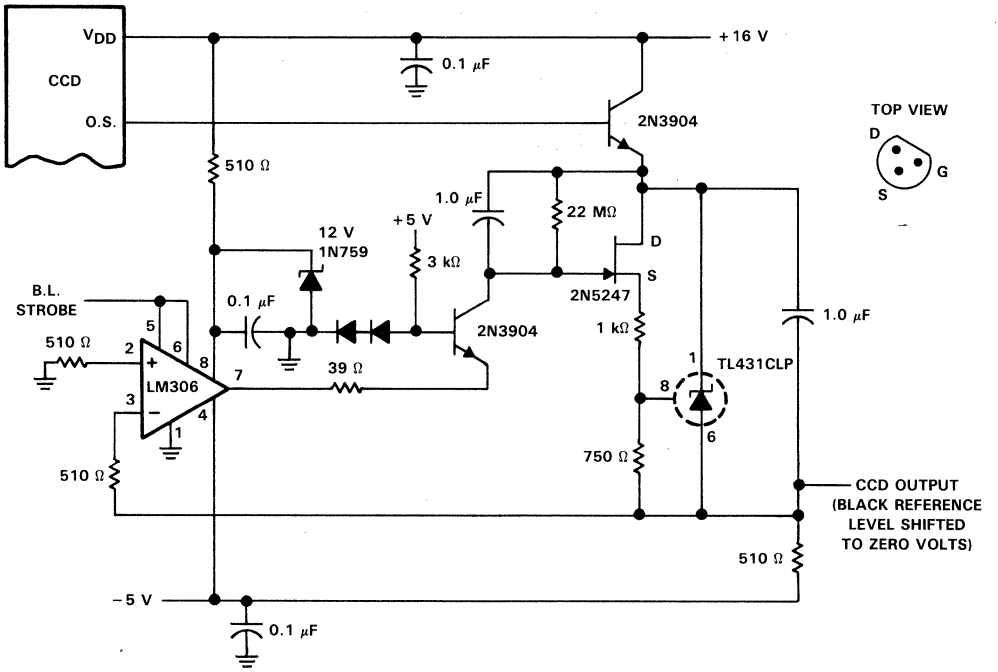


Figure 7. CCD Output Level Shifting Circuit (Black Level Clamp to 0 V)

A series of down-counters is used to generate the exposure time and locate the exact time to send out the strobe to comparator so the pulses will be placed during the beginning black reference pulses in the output of the CCD. The black-reference pulses start exactly on the twelfth data-pulse, beginning with the pulse during the transfer clock period. Thus, the first down-counter is loaded with a count of eleven so that its borrow output will be at the end of the eleventh data-pulse. At this time, the latch changes state and triggers the second monostable multivibrator which sets the gate-time for three or four black-level strobe pulses. These pulses begin on the twelfth data-pulse.

A series of gates delay the opposite phase of the reset clock from the clock oscillator to generate the basic strobe and data-clock pulses. The delay causes the timing to match closely that of the video chain and to fall correctly timed with the data time of the video pulse (see Figure 10). The other down-counter counts the borrows from the first counter and reloads on fourteen, thus giving a total count of 11 × 14 or 154 reset clocks between transfer clocks. In this counting method only seven of the fourteen data-following pulses are allowed to be read out.

For the application in which this circuit is used, there is no need for the remaining black reference pulses or white reference pulses. However, they can be included, if desired, by changing the counter-timing method. Although the counter-timer is a simple fixed-threshold-type processor, the principles are presented here so that variations can be worked out.

Analog-to-Digital Flash Converter

Another method of converting the output of the CCD to digital can be accomplished by using a flash analog-to-digital (A/D) converter. Once again, the problem of interfacing with the A/D converter input requires the establishment of a black reference voltage representing all zeros in the digital output word. The capacity-coupled line-clamped form of level-shift and black-level clamp (see Figure 5), is used in an automatic form shown in Figure 11. To provide continuity and clarity in understanding the automatic method, the complete level-shift and black line-clamp is explained again using Figure 12. Figure 12 shows the CCD output signal pulse train with the dark reference pulse located with four isolation pulses before and four isolation pulses after the optical data stream.

Positive voltage is subtracted from the negative output of the detector. This brings the input bias of the buffer amplifier to the correct level. When the clamp switch is closed, the output of the buffer amplifier is the desired black level (see Figure 13).

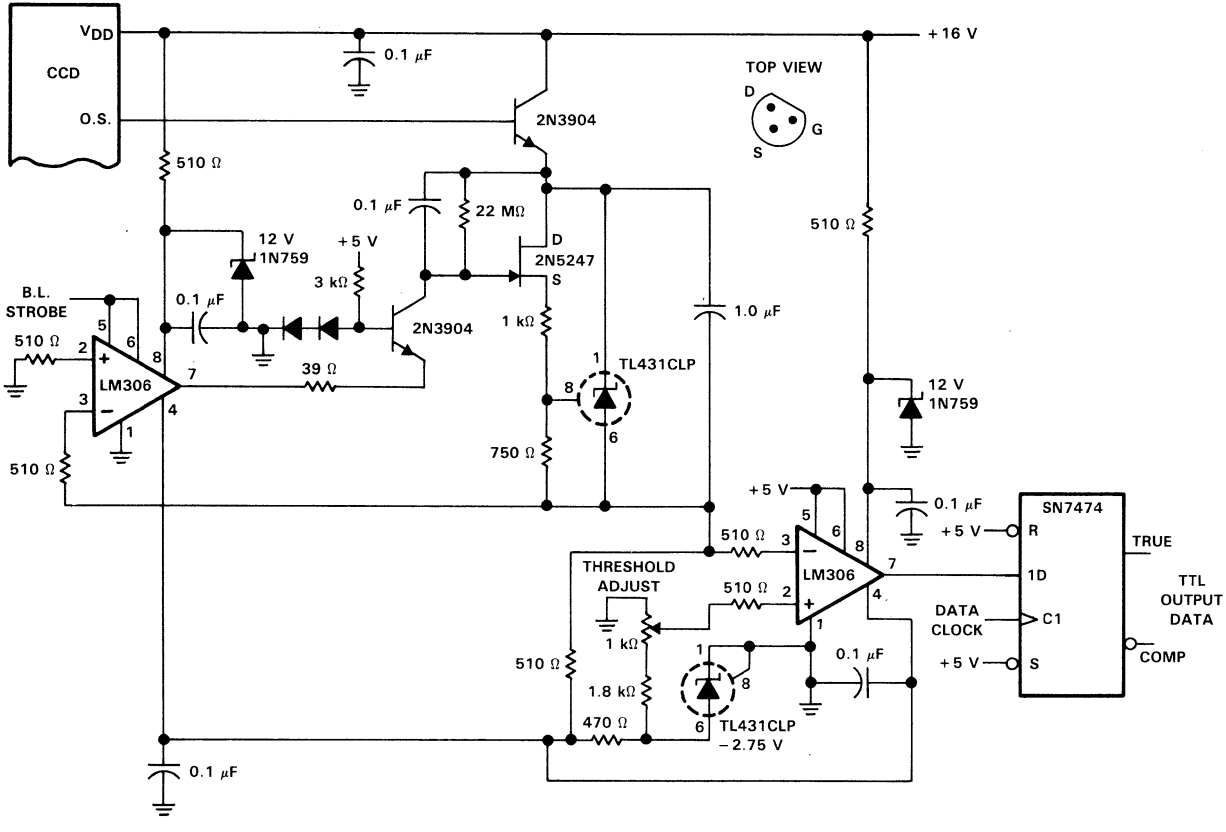


Figure 8. CCD Threshold Type Processor

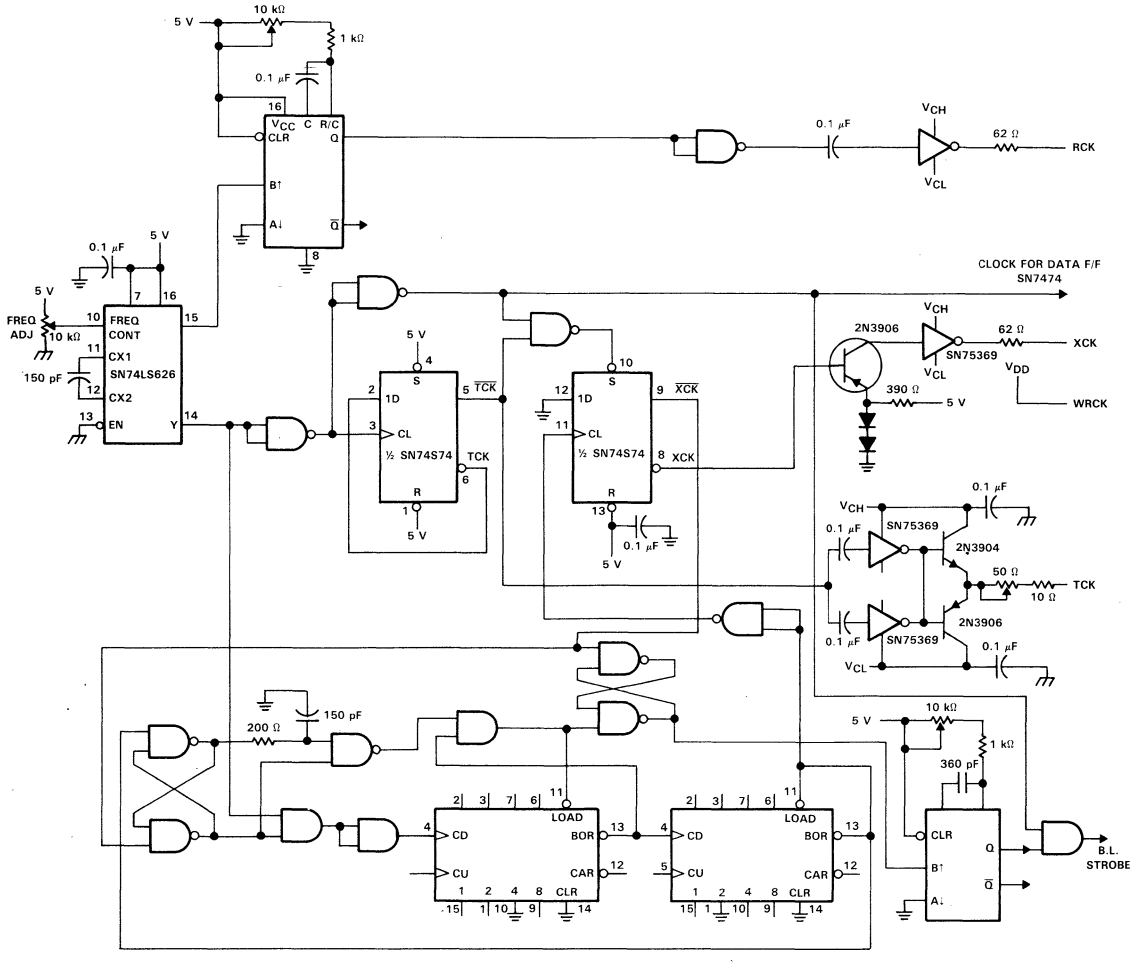


Figure 9. Timing Logic and CCD Clock Drivers

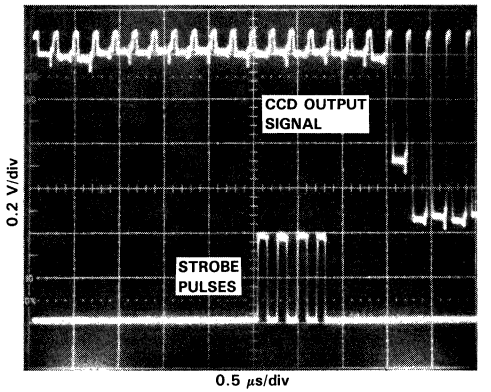


Figure 10. Comparator Strobe Pulse Timing with Output Signal

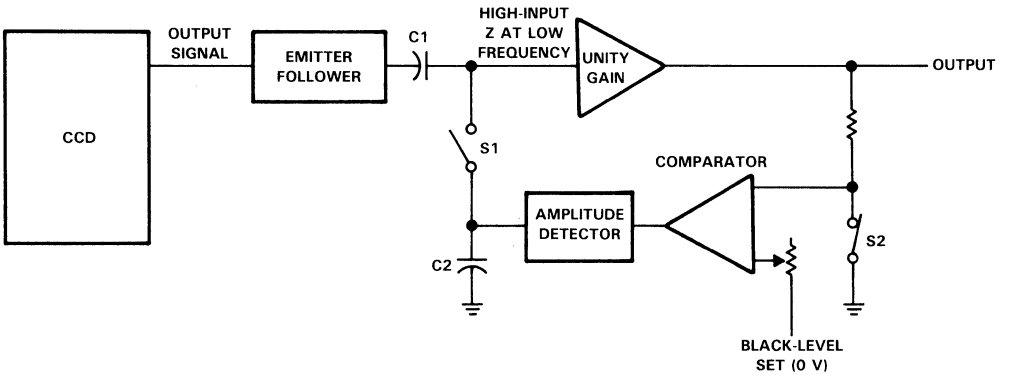


Figure 11. CCD Output Signal Buffering Circuit and Automatic Black Reference Block Diagram

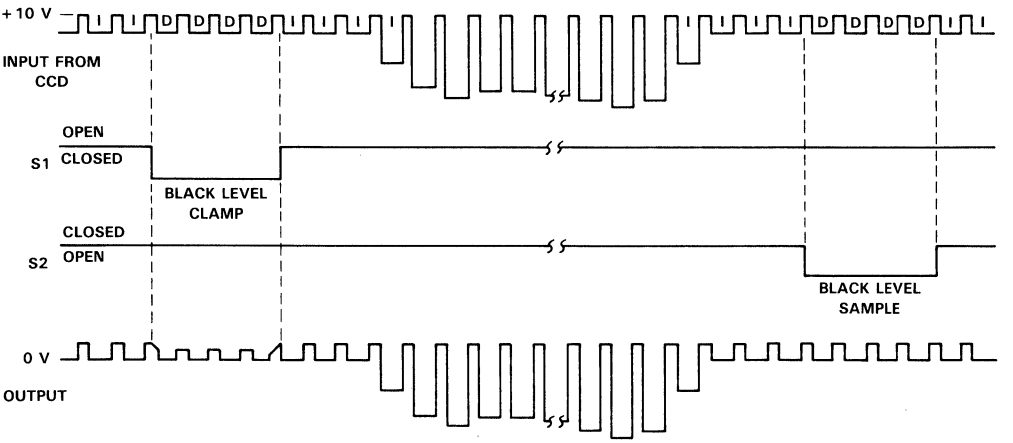


Figure 12. Input/Output and Switch Timing for Automatic Black Reference

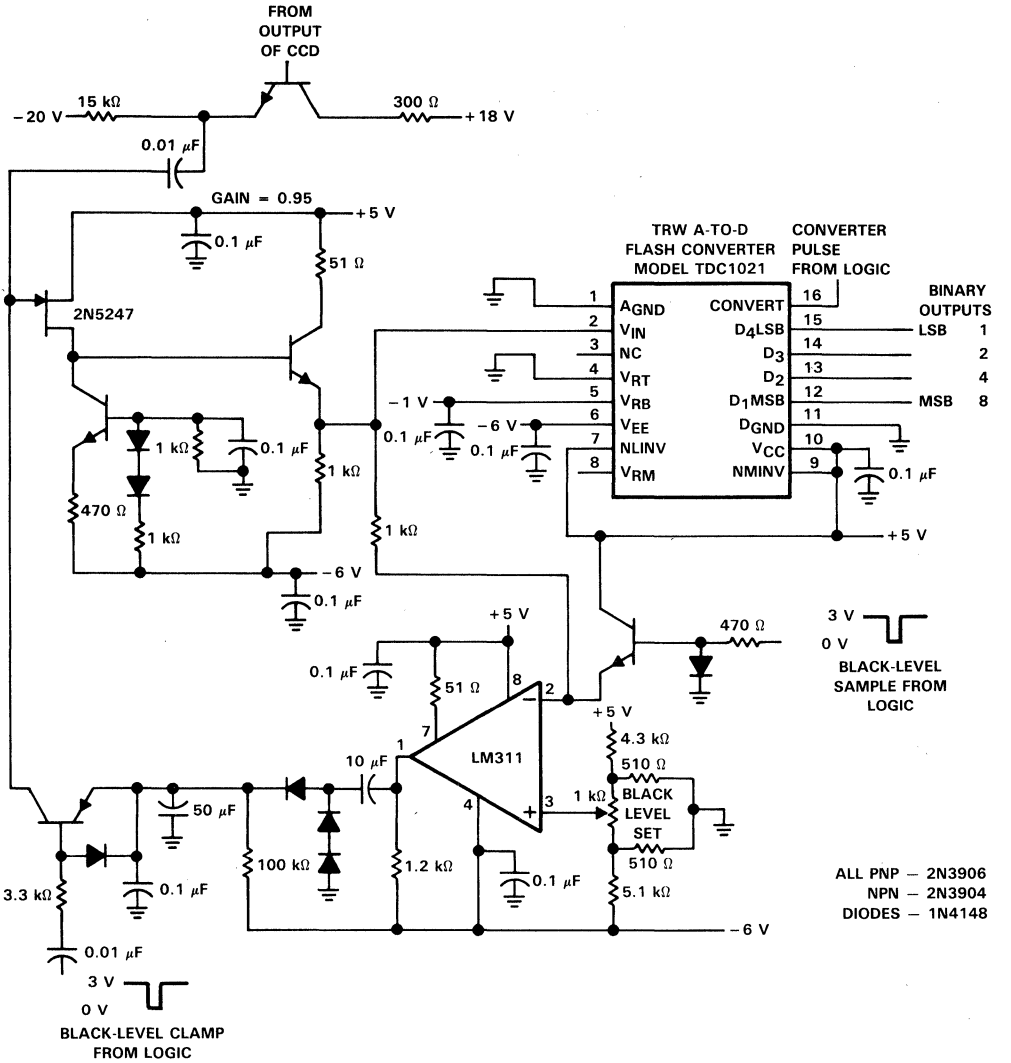


Figure 13. Automatic Black-Level Control and A/D Converter (0.1 to 10 MHz Operation)

The black-level clamp and black-level sample can be timed to occur during the same dark reference pulses time. However, the black-level clamp disturbs the signal and may cause some errors in the black-level sample. The control signals to S1 and S2 are timed by the exposure-time counters so that the switches will be turned on and off at the exact black reference pulse times.

The signal is now conditioned so that it will interface with the A/D converter. For high speed conversion at 10 MHz, the TRW TDC1021 4-bit parallel flash converter is used. It requires no external sample and hold because of its speed and design. The TDC1021 accepts a 0 to −1 V input signal, requires a convert pulse to tell when the analog signal is to be converted, and is powered from +5 V and −6 V supplies. The convert pulse timing as related to the output data of the CCD is important for correct A/D conversion.

As specified in the TDC1021 data sheet, the analog amplitude data sample is read 10 ns after the 50% point of

the convert pulse rising edge. In addition, the pulse is a positive going TTL amplitude and should be nominally 30-ns in duration. From this condition, the convert pulse should be decoded from the timing logic so its leading edge is 10 ns ahead of the desired sample point on the output pixel pulse of the CCD. To approximate where to decode the convert pulse, it is necessary to determine the time delay of the pixel pulse arriving at the analog input of the converter relative to the logic from which the convert pulse is to be decoded. The propagation delay time between the reset clock falling edge and the pixel's falling edge is determined to be 15 ns (see Figure 14).

The reset clock rising edge is located where the transport clock feedthrough starts to disturb the data pixel (see Figure 15). Therefore, the convert pulse ends exactly where the reset pulse starts and exists 30 ns before that point.

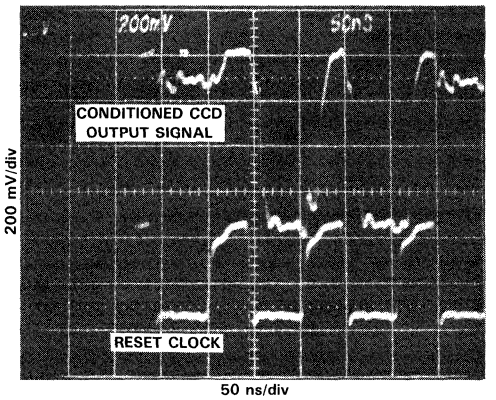


Figure 14. Conditioned CCD Output Signal (Reset Clock)

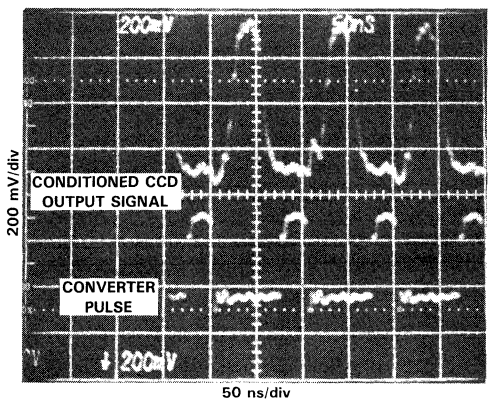


Figure 15. Conditioned CCD Output Signal (Converter Pulse)

With the convert pulse timed correctly with the output data stream, the final result of the converted data is as shown in Figure 16.

The optical input for the CCD is a uniformly illuminated seven-gray shaded and black test pattern. The input uses an incandescent source operated from direct current to prevent 60-cycle modulation. An IR filter cannot be used because there is not enough light output to produce a 1-V CCD output. As a result of the IR plus visible light combined, the gray shades are not uniform changes in intensity. However, this condition does not detract significantly from the presentation. The A/D converter is set up for outputs of 0000 for a 0 V input and 1111 for a -1 V input. Therefore, an analog -0.067 V is equal to a one binary bit state change.

This A/D method is for a linear CCD. However, it can be used with an area CCD by altering the black-level sample and black-level clamp to coincide with black reference pulses or pixels from the data streams of the image sensor. A good example of how black reference pixels of area image-sensors are located in their output data streams is in the processor, consisting of a low-pass video filter and amplifier.

Low-Pass Video Filter and Amplifier

The video information in the output signal from an area image sensor [e.g., a closed circuit television (CCTV) camera] can be extracted with black reference level (pedestal) by a low-pass video-filter type processor. Such a processor (see Figure 17) has an automatic black-level clamp very similar to the scheme used with the A/D converter. In addition, it has an automatic video level control with composite blanking and composite sync to form a near standard composite monochrome video output signal.

The automatic black-level clamp is very similar to the one used with the flash A/D converter. The coupling capacitor and clamp transistor are the same and work into a high input impedance amplifier with a positive gain of approximately four. The video filter (LPF) with a low-pass cutoff of 3.2 MHz (half the serial clock frequency) is driven by this amplifier. The filter recovers the negative video envelope by taking an average of the negative voltage under the amplified output signal from the CCD. This computer-designed filter has a low-overshoot fast-cutoff characteristic so that video up to 3.2 MHz is passed and the serial clock at 6.44 MHz is down 36 to 40 dB. In most cases, the video has a low duty-cycle (see Figure 3). The ratio of time output voltage is the video envelope value divided by time; it is at the reset voltage value.

This low duty-cycle makes the output signal of the filter small compared to the peak-input signal (often 25% or less). Gain is required to produce a reasonable 0.75 V signal. This arrangement works because positive video is required and the amplifier can invert the video while amplifying. The black-level sample is taken from the output of this amplifier before it is blanked. In this circuit, two PNP emitter followers share a common load resistor and serve as a switch. The output is sent to a simple two-transistor comparator. The

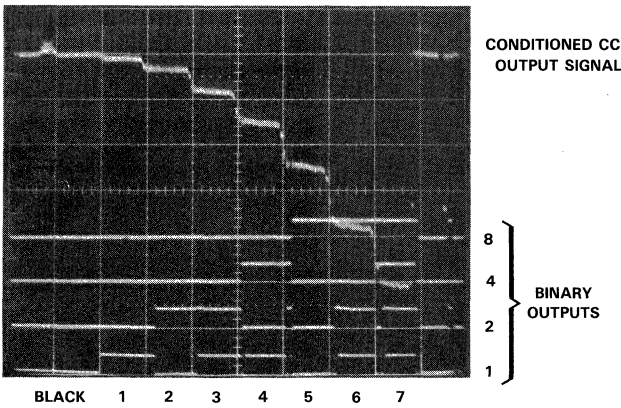


Figure 16. Conditioned CCD Gray Shade Signal and A/D Converter Binary Outputs

comparator compares the level with an adjustable reference to provide output pedestal or black level setting. The positive-going error pulses from the comparator are detected by the positive-peak detector and the current through the 8.2 kΩ resistor is increased to provide the correct bias to the clamp transistor. This process causes the voltage across the 0.01 μF coupling capacitor to be correct during the black reference pixel time in the output signal of the CCD, so that the direct coupled amplifier-filter chains output is the desired pedestal level.

Figure 18 shows the relative timing of the black-level clamp and the sample pulses supplied from the system timing logic that are relative to the output signal of the CCD. In addition, the horizontal blanking and sync with serial clock waveforms have been added to show relation to standard known waveforms supplied by the timing logic. The black-level sample is taken from the output of the CCD when the serial register is over-scanned (more than the pixel stored in the parallel registers). Only dark current is present.

The black-level clamp is taken during the beginning of scan of the serial register. There are blank bits between the charge detection node and where the parallel enters the register. There can be as many as 15 of these beginning bits. However, when the output signal has no video, there are usually only six. These six beginning bits represent only dark current. This clamp action establishes the black reference for the entire video line. This explains the major operation of the processor. However, the automatic-gain control and insertion of blanking and sync circuits are discussed.

Automatic-gain control is applied to the feedback resistor of the second amplifier by making a portion of it a light sensitive CaS resistor and controlling its value by the amount of infrared light applied to it from an LED. This all-in-one device has a wide-band-width resistor that varies from megohms in the dark to only 200 Ω under bright illumination from the diode. The range is limited by the 2.4 kΩ series resistor at the low end (low gain) and by the shunt 33 kΩ resistor at the high value (high gain). Diode control current is obtained from the three transistor-comparator circuits which compare the average positive detected video signal with a gain level set reference. In this manner, automatic control is accomplished.

Blanking is accomplished by placing a simple shunt transistor switch where the positive TTL composite blanking signal is applied. The shunt transistor switch blocks the signal to the output emitter follower. Composite sync is accomplished by summing a negative voltage produced by the drop across a forward diode when it is switched into the circuit by a transistor turned on by the TTL-level positive composite sync voltage.

This automatically-controlled video-filter-type processor is used with a linear CCD to produce a TV picture from a picture scanned on a rotating drum. The only precaution required is to ensure that black level reference signals are available in the output of the CCD when black-level sample and clamp are being activated.

Sample-and-Hold

The last processing method to be discussed employs a high-speed sample-and-hold (S/H) circuit to recover the video envelope from the signal pulse train of the CCD output. Figure 19 illustrates a simplified processor circuit that uses TI's new 15 MHz sample-and-hold integrated circuit (TL1591). The simplified circuit provides the following; first, it shows how the sample signal of the S/H is developed from the reset clock driver logic of the CCD through the use of a single TTL logic IC (SN74265) and second, it shows that three additional components permit it to be inserted into the standard line-clamp black reference circuit (see Figure 5).

Further explanation of the sample clock development with the SN74265 will be helpful. A positive-going TTL-level clock pulse 20 ns wide is needed to enable the S/H to

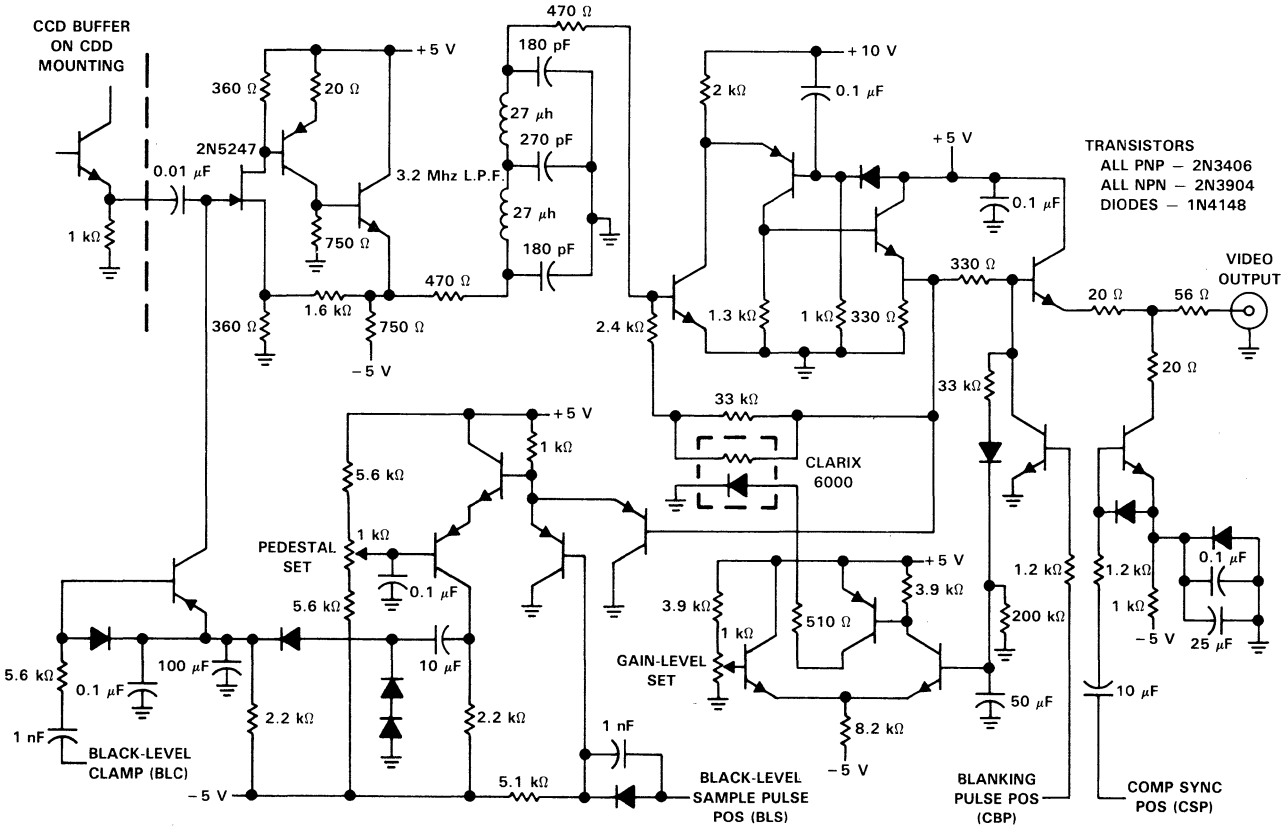


Figure 17. Complete Amplifier and Processor for Monochrome CCD Camera

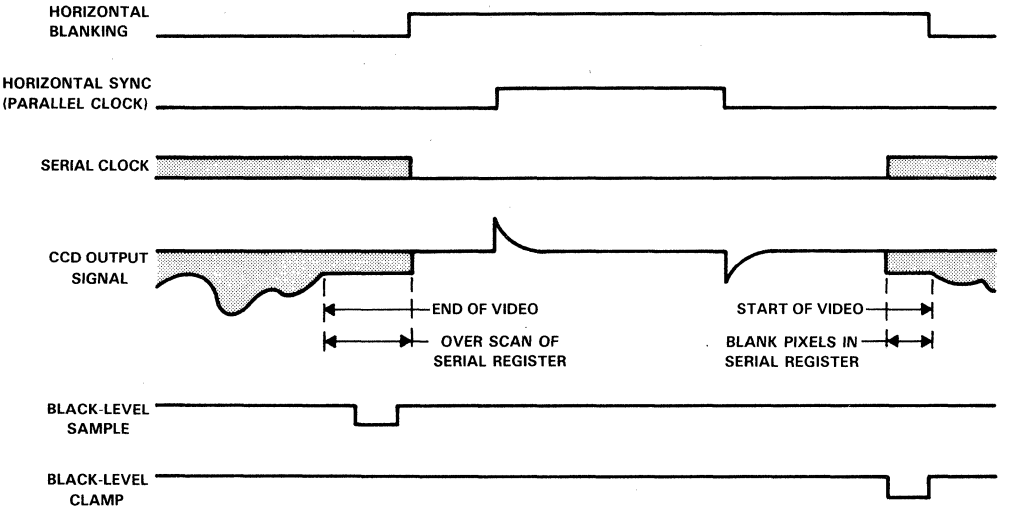


Figure 18. Black-Level Clamp Timing for Area CCD

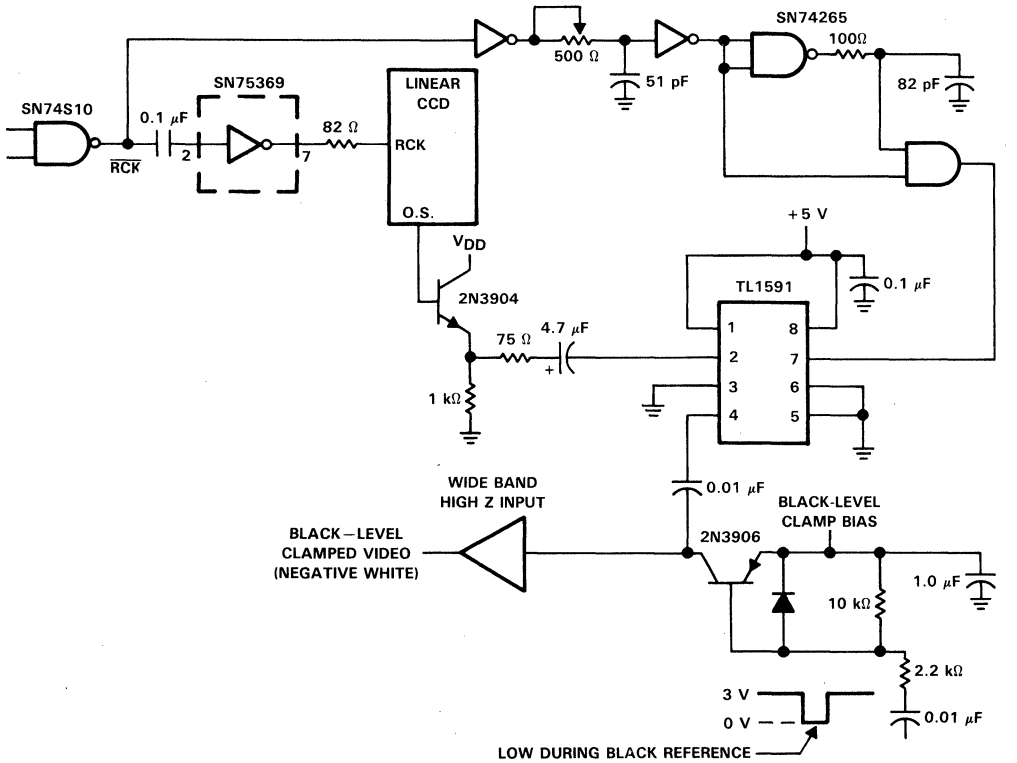


Figure 19. CCD with Sample-and-Hold Black-Level Clamp

take a new sample of the incoming signal. For the output signal train of the CCD, the sample pulse must occur during the data level or low peak of the CCD output signal train.

Figure 20 shows the output signal of the CCD at a 6.67 MHz data rate. In addition, it shows the corresponding sample-and-hold output. The sample-and-hold output changes near the middle of the low peak of the CCD output waveform. Even though the sample clock pulse is not shown, the evidence of its location can be seen. To locate and generate this sample clock, the trailing edge of the TTL-level RCK is delayed by the two inverter gates and the R-C network. The variable resistor allows a small delay time adjustment for optimum timing to improve performance. The sample clock pulse is generated by the logic and function of the delayed RCK and the further delayed RCK pulse. This second delay determines the width of the sample clock pulse.

Figure 21 shows a complete circuit showing the SN76876 processing video from a TC103 operating at 10 MHz with the S/H output level shifted and automatic black level clamped. Figure 22 illustrates output video from this processor circuit. The TL1591 S/H typically recovers 90% of the peak input signal.

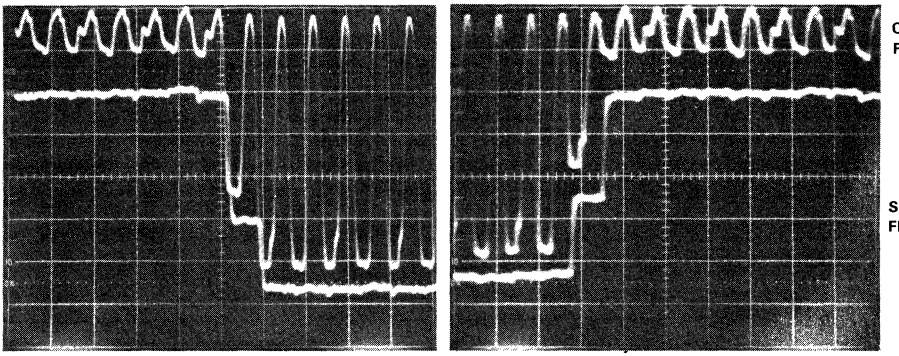


Figure 20. Sample-and-Hold (TL1591) Operated with a TC103 at 6.67 MHz

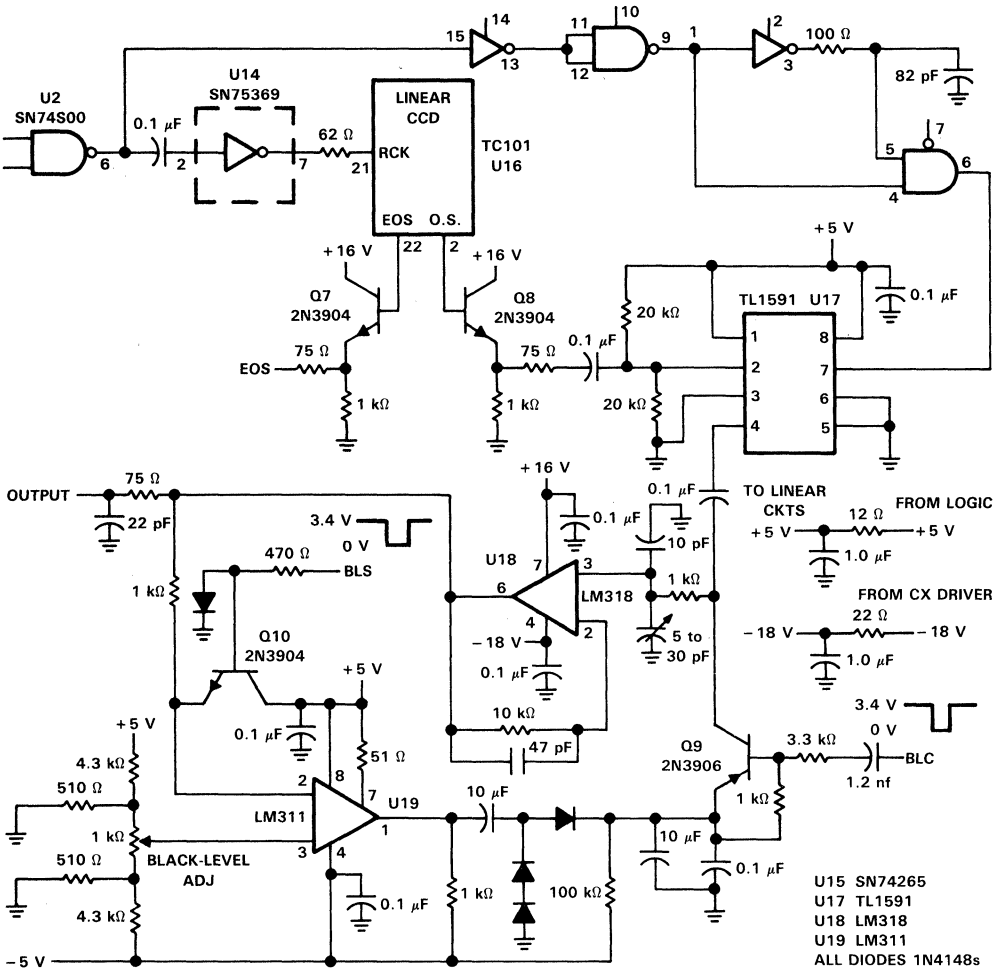


Figure 21. Sample-and-Hold Processor with Automatic Black-Level Control 10-MHz Operation

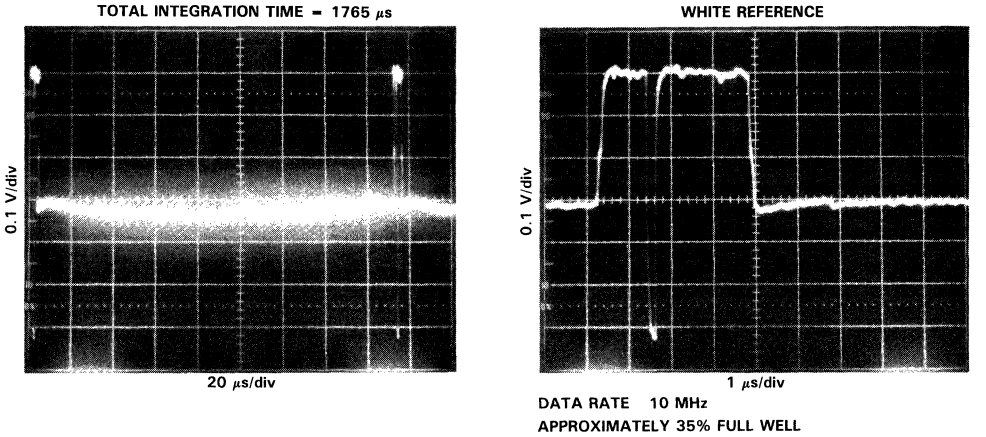


Figure 22. Processed Output

CONCLUSION

The various methods described in the preceding paragraphs are provided to familiarize the prospective CCD user or designer with the requirements for both CCD output signal conditioning and basic signal processing methods. Selection of a particular method or approach will depend on the application. The designer must expand and update these methods based on his system requirements.

LINEAR CCD OPERATION AT 10 MHz

This application report covers the following main topics:

1. The operation of the Texas Instruments TC102 128 × 1 linear image sensor at a 10 MHz data rate
2. Restoration of the black reference to the data using the dark-reference pixels of the CCD
3. Conversion of the output signal into binary data without sample-and-hold

In addition, circuit approaches (with data) to solve the problem of high-frequency clocking and the resulting transport-clock feedthrough into the output signal are discussed

CCD Clocking

Operation of the TC102 at a 10 MHz data rate is affected by the function of each clock relative to the other clocks. The purpose of the CCD clocks is to move the data from the photo sites to the detection circuit. The data is generated at the photo sites in the form of a charge that is proportional to the optical input. At the detection circuit, the charge is converted to a proportional voltage that is applied to the output of the CCD.

The first step in the conversion is to send the charge from the photo sites, via the transfer gate region, to the CCD shift registers, which are adjacent to the photo sites. The transfer is made by applying a high transfer-clock pulse while the transport clock is held high. The relationships among the various clock levels required to move the charge are as follows:

1. When a clock is high, it allows the charge to flow into the area under the clocked region (a well) and when a clock is low or most negative it biocks the charge flow (a barrier).
2. When a clock makes a high-to-low transition, the charge contained in its well is shifted to an adjacent virtual well region.
3. When both clocks are high, the photo site charge flows into the well of the transfer gate.
4. When the transport gate returns to the low state, it acts as a charge barrier in the transport register. The charge is then introduced into the virtual wells of the transport register by the transfer gate.
5. When the transfer gate returns to the low state, it moves the charge into the transport register. When the transport clock goes high to move the charge toward the transport combining region, the transport gate remains low to prevent charge flow back to the photo sites.

The charges from adjacent even and odd photo sites are simultaneously clocked along the even and odd transport shift registers to the combining portion of the transport register. Thus, an even charge packet and an odd charge packet arrive in the region at the same time. To separate the packets into correct numerical order, the reset clock is used for the charge clocking. The reset clock goes high on each half cycle of the transport clock. The reset clock selects each packet in the correct order and applies them to a single register. This single register converts the charge to a voltage that is sent, via the reset MOS switch, to the V_{ref} output.

After the optically generated charge is sent to the output, the white reference portion of the output and the end-of-scan signal are applied to their respective outputs. The charge for both of these signals is introduced by clocked bias on the injection diodes. The white-reference clock controls the reverse bias on the injection diodes. A reduction of the positive bias on these diodes causes a charge to be injected into each transfer region (a clocked barrier-well). These charges are applied at the opposite ends of the two transport and end-of-scan registers from the charge detection diodes. The proper relationship among the clocks must be maintained for charge injection into the registers. The relationships are as follows:

1. The white-reference clock must be low to generate the charge.
2. The transfer clock must be high to form a collecting well.
3. The transport clock must be high to clear all extraneous charge from the virtual well region.

Under these conditions the charge is contained in the transfer gate region (a process known as "fill") and is not transferred to the virtual well region of the registers until the transfer-clock voltage goes low.

However, before the transfer-gate voltage goes low, the transport clock voltage goes low to block out-of-time charge flow down the register. The injection diode voltage goes high to create a deep potential well to prevent further injection and to remove the excess charge contained in the transfer region (a process known as "spill"). The removal of the excess charge produces a charge packet that is controlled by the size of the clocked well portion of the transfer gate. This makes the injected charge to the register dependent upon the well capacity of the CCD or the saturation output level. To complete the transfer into the register, the transfer clock is returned to the low state and provides a high-charge barrier.

High Speed Operation—10 MHz

To provide a suitable clocking method for data rate frequencies ranging from 5 to approximately 10 MHz, the portion of the data period that must be dedicated to the reset clock in order to get satisfactory operation must be determined. The reset-pulse duration at the top 10% should

not be less than 40 ns. In addition, the reset pulse should start coincidentally with the transport-clock transition. Coincidence is necessary because, if the reset pulse rises before the transport-clock transition, there is danger of the charge from a previous pixel being mixed with the charge that is being read out. The purpose of placing the reset pulse in coincidence with the transport-clock transition is to allow as much time as possible for the output signal to settle and data to be acquired.

At 10 MHz, the data period is only 100 ns. If the reset pulse is 40 ns plus rise and fall times, there are fewer than 50 ns for the data time. Two data periods are produced for each period of the transport clock, TCK. A timing-logic circuit that will produce the recommended timing can be derived from the circuit on the data sheet. To derive the circuit, the clock oscillator must be capable of running at four times the data frequency or 40 MHz and the first divider flip-flop must be able to clock at 40 MHz. The circuit shown in Figure 1 is a modified version of the data-sheet circuit. To provide 10-MHz operation, all logic ICs are Schottky-clamped for high speed. As in the data-sheet circuit, the first frequency divider is four. This gives four quadrature-complementary output waveforms (designated A, B, C, and D in Figure 2) which represent the logic timing.

A delayed signal in phase with the A waveform is used for reset clock, RCK. Another frequency division by two provides the TCK that is delayed by the SN75369 drivers. To meet the XKC transfer clock timing as related to the TCK as specified in the data sheet, the decoding of the E waveform must be different from that in the data sheet circuit. This difference causes the XCK to rise with the TCK transition and to fall near the center of the second half-period of the TCK so that the 50-ns minimum is satisfied at 10 MHz. The minimum can be as low as 40 ns to accommodate 12-MHz operation for most of the linear CCDs. The XCK logic signal is used to gate a first half-period of the TCK through the SN75453 white reference driver. Both the XCK and WRCK repetition rates are determined by the SN74LS193 counter chain. The counter chain down counts TCK periods to set the exposure time or XCK repetition rate period. The waveforms (see Figure 2) are simplified in that circuit propagation delay times have not been taken into account.

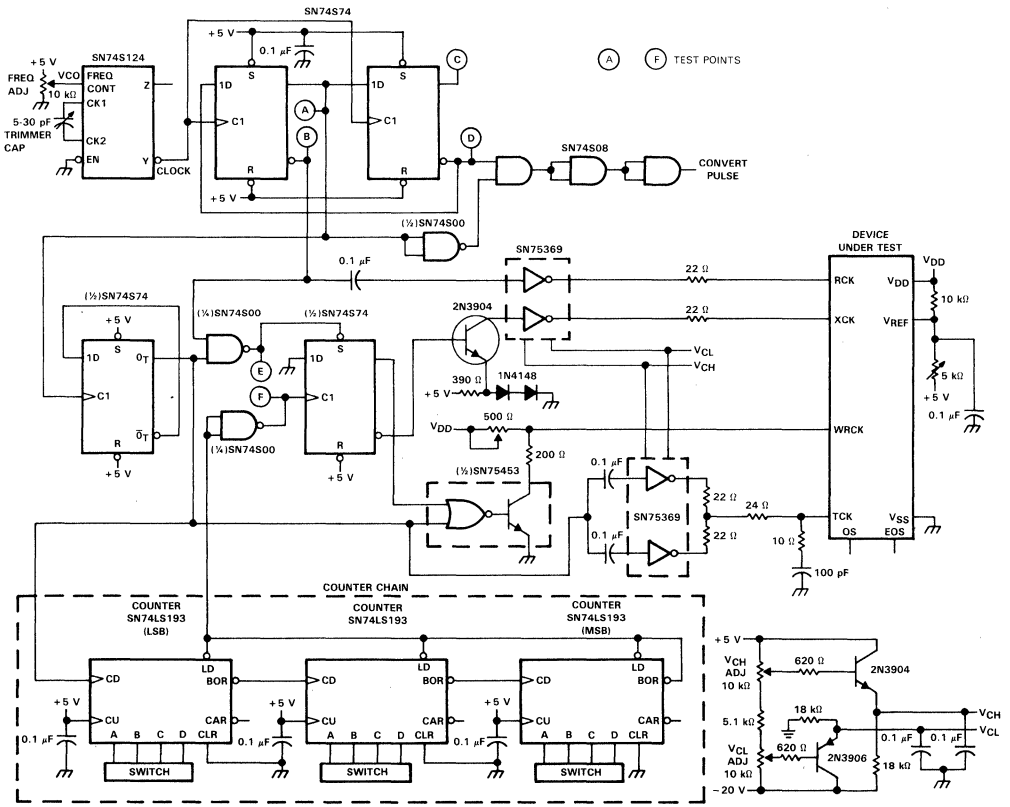


Figure 1. Waveform Generation Circuit for Testing Line Image Sensor (10 MHz)

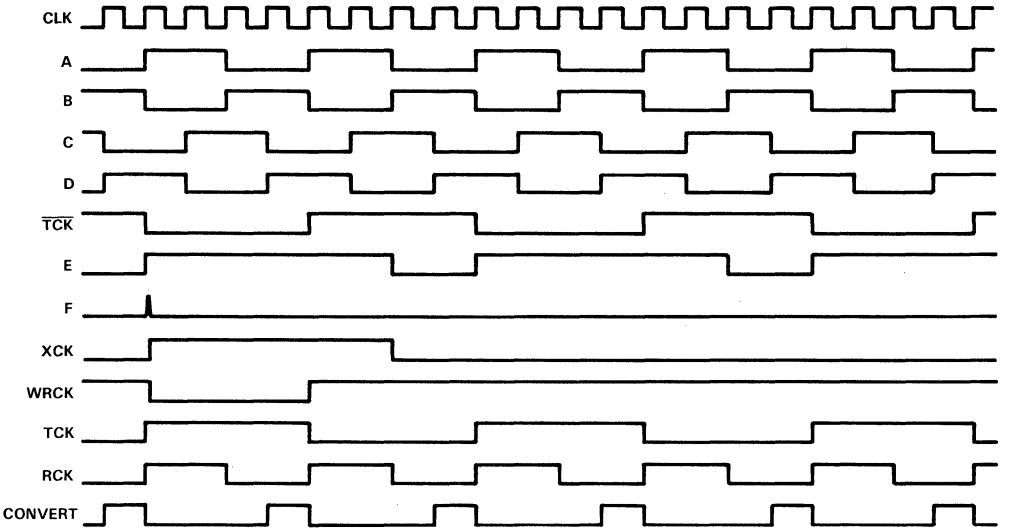


Figure 2. Logic Timing, 10 MHz Operation — TC102

For the exact effect of circuit propagation delay times, Figure 3 shows the TCK, RCK, XCK, and WRCK as seen at the clock inputs of the TC102.

Figure 3 shows that the reset clock rises coincidently with the transport clock transitions. However, because of the delay in the counter chain borrow output (SN74S00 and SN74S74), the rise of the transfer clock is delayed from the rise of the transport clock by 40 ns. The WRCK is delayed by the same amount and the delay is not detrimental as long as both clocks are present at least 30 ns before the TCK goes low. When the reset clock pulse rise time is less than 15 ns, the quantities specified in the data sheet may cause a small increase in dark current. If the dark current increase is detrimental to operation, then additional capacitance or resistance can be added to the clock drive lead to increase the rise time to 15 ns.

Figure 4 illustrates the output-signal delay of the CCD with respect to the input of the clock. The transistor-buffered output signal in the two white-reference regions is shown with the RCK. The waveforms indicate that the delay between the reset clock and the reset interruption in the output signal is approximately 13 ns. This delay is reasonably accurate even though there is a moderate amount of ringing on the waveforms. The ringing is increased by the test equipment.

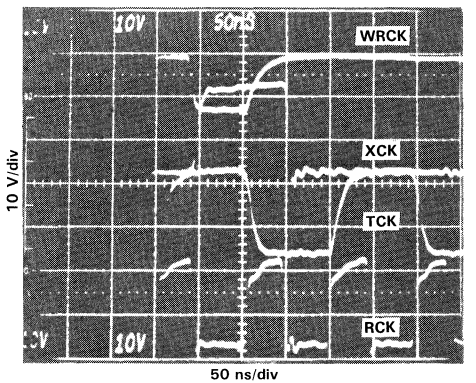


Figure 3. Clock Input to TC102

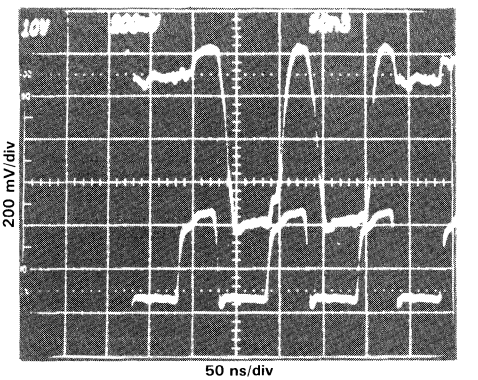


Figure 4. Emitter Follower Buffered Output Signal Showing White Reference (Output Signal with RCK)

Figure 5 illustrates the same signals but with improved test conditions.

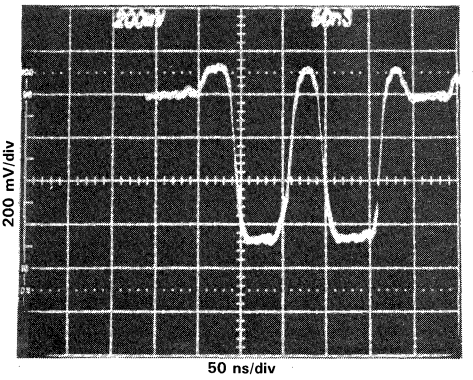


Figure 5. Output Signal Only — Spike Suppression

Transport-Clock Feedthrough Reduction

Transport-clock feedthrough can be a serious data interruption problem with the CCD sensor. However, the problem is eliminated when the transport-clock transition is timed to be coincident with the reset-clock pulse low-to-high transition. This combines the feedthrough in the necessary data interruption caused by the reset clock. This timing allows satisfactory CCD operation and maximizes data output time per pixel. Efforts to minimize the magnitude of the feedthrough noise should also be considered.

As shown in previous figures, the TCK feedthrough noise is reduced by building the circuit on a ground plane PCB and by a rise time reduction circuit on the TCK lead. The rise-time reduction circuit is the 10-ohm resistor and 100-pF capacitor combined with the 22-to-24 ohm series resistor located on the terminals of the SN75369 driver (see Figure 1). This RC network shunts the fast rise currents from the outputs of the SN75369 driver back to its high- and low-supply bypass capacitors. In this manner, the very highest frequency components of current are not allowed to flow into the ground plane. The effect of removing this shunt network is shown by the added feedthrough (see Figure 6). This anti-ringing and rise-time reduction circuit can be accomplished by other RC arrangements, but the method is still the same.

Black-Reference Restoration

In video processing, the output signal reference level for the sensor under a no-light condition (black level) must be known at all times . The dc output signal voltage level of most CCD sensors ranges from 6 V to 14 V and is not stable with temperature or drain voltage variations. Therefore, the signal must be capacitively coupled somewhere in the signal path. This capacitive coupling provides an opportunity to clamp the charge or voltage drop across the capacitor at a time that will represent the black reference level for the signal. This clamping is done over

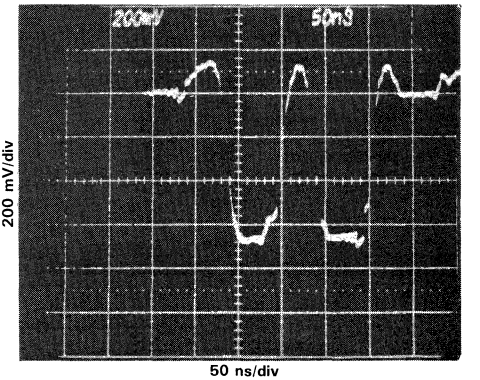


Figure 6. Output Signal Only — No Spike Suppression

a moderate time of perhaps less than 1% of the discharge time constant. A time location in the CCD output signal has been provided for this operation. The time location is called the dark-reference pixels. They occur four isolation pixels before and after the optical-data stream (see Figure 7). This black-level clamping method can be accomplished repetitively in an automatic manner as shown in Figure 8.

In this simplified form of the automatic black-reference circuit, the output of the sensor is buffered through an emitter follower and coupled to a second amplifier. The second amplifier must have a very high input impedance at low frequencies and be direct coupled. However, it may or may not have voltage gain depending upon the requirements of the follow-on circuit. In this case, no more voltage gain is required because of the output of the CCD (over 1 V). The high input impedance of the amplifier allows the use of a small coupling capacitor, C1. This minimizes the charge leak off before all data is read out. A small coupling capacitor is desirable so that the recharge circuit impedance is not unreasonably low due to the short time allowed to recharge or clamp.

The clamp circuit comprises the following components; the emitter follower buffer, switch S1, and capacitor C2. The operation of the circuit (see Figure 7) is as follows:

1. Switch S1 is always open except when the first set or pre-data dark-reference pixels occur in the output signal stream of the CCD.
2. Switch S1 closes and applies the voltage stored on capacitor C2 to the second amplifier side of capacitor C1.
3. Switch S1 opens when the dark-reference time is over and the bias voltage to the second amplifier, and the output, is referenced to the applied level until it is reclamped.

The automatic feature of the circuit (i.e., how the correct voltage is obtained for capacitor C2 and its operation) is as simple as the clamp method. As shown in Figures 7 and 8, switch S2 opens each time the following data dark-reference pixels appear in the data train and a black-level

sample is taken of the output. This sample is compared with a predetermined black-level set voltage by the comparator. The comparator generates an error pulse output to the amplitude detector. This error pulse is transferred by the amplitude detector as an error voltage to correct the voltage stored on capacitor C2 so that, when the voltage on C2 is applied via S1 to the amplifier, the output of the amplifier will be the desired black-level voltage (zero for our application). Since C2 must be quite large to prevent low frequency oscillations, it takes several error pulses to correct the voltage stored on C2 when the circuit is first turned on. However, after the circuit has reached equilibrium, the required correction occurs on each readout cycle.

The block diagram in Figure 8 was arranged to match the circuit in Figure 10. However, there are details about this circuit which are not covered by the block diagram description. The details are helpful in understanding the exact circuit operation. The high-input impedance buffer amplifier is an FET source follower with a constant current source load followed by a standard emitter follower. The FET operates at 6.3 mA and the emitter follower at 6 mA, giving an 0.95 gain with an output impedance of less than 25 Ω. Any FET used in this amplifier must be made to operate at 6.3 mA for a gate to source voltage range from 0 to −2.5 V maximum. This is the maximum negative voltage available from the black-level clamp as supplied from the peak detector.

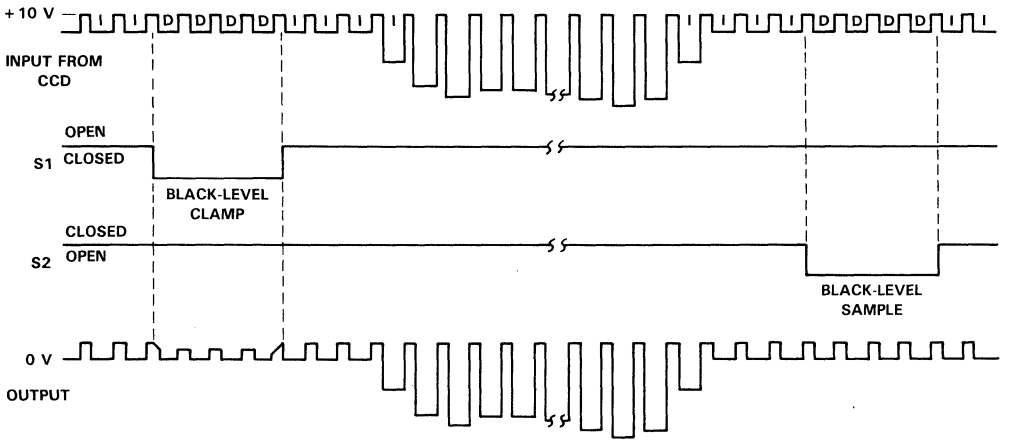


Figure 7. I/O and Switch Timing for Automatic Black Reference

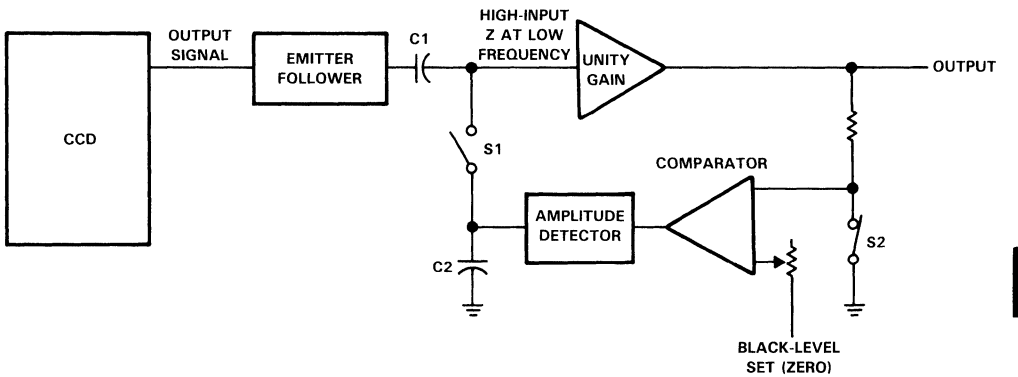


Figure 8. CCD Output Signal Buffering Circuit Automatic Black Reference

This limited voltage occurs when there is no positive error signal from the LM311 comparator. The maximum negative output voltage of the positive peak detector is then produced by the three diodes being forward-biased to −6 V by the 100 kΩ resistor. For the automatic black-level correction circuit to function, the −1.9 V input bias to the buffer FET of the amplifier must produce voltage equal to or more negative than the black-level voltage desired at the output of the amplifier—in this case, zero volts. This input bias voltage is necessary so that, when the black-level sample is taken, the comparator will produce a small positive pulse output to be detected. This positive voltage will then be subtracted from the negative output of the detector to bring the input bias of the buffer amplifier to the correct level so that the output is the desired black level when the clamp switch is closed.

The black-level clamp and black-level sample can be timed to occur during the same dark-reference pixels time. However, the black-level clamp disturbs the signal and may cause some errors in the black-level sample. The control signals to S1 and S2 are timed by the exposure time counters so that the switches will be turned on and off at the exact black-reference pixel times.

The exposure-time counters with black-level switch signal decoding are shown in Figure 7. The decoding is taken from the outputs of the first two down counters. The minimum down count is set by the minimum number of data reset clocks to completely read out the CCD from transfer clock to the two white reference output pixels. This count is 19 + 128 + 14 (or 161) but the counter counts transport clock cycles which are half the data frequency. Therefore, the nearest minimum whole number of TCK counts is 81. To decode a pulse for the black-level clamp four pixels wide and 12 counts from the beginning (81 for down counter), the decode numbers are 75 and 74. In Figure 9, 128 was added for increased exposure time, so 202 was used. By the same reasoning, the decode count for the black level sample was determined to be 4 + 128 (or 132). Other decode intervals can be determined to fit the desired exposure time. The black-level correction cycle may be applied at regular intervals during the exposure time as long as the interval matches the dark-reference pixel repetition rate.

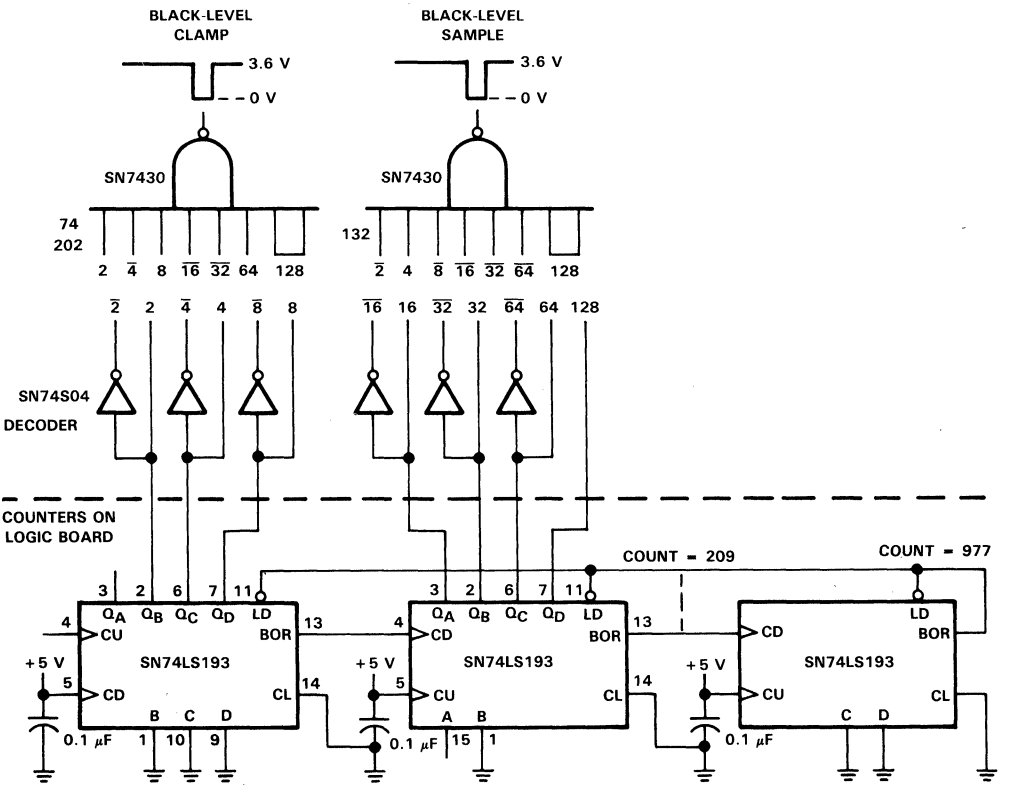


Figure 9. Black-Level Sample and Clamp Decoding

Analog to Binary Signal Conversion

The signal is conditioned so it will interface with the analog-to-digital converter (see Figure 10). For high-speed conversion at 10 MHz, the TRW TD1021 4-bit parallel flash converter is used. It requires no external sample-and-hold because of its speed and design. It accepts a 0 to −1 V input signal, requires a convert pulse to tell when the analog signal is to be converted, and is powered from 5 V and −6 V supplies. The convert-pulse timing as related to the output data of the CCD is important for correct A/D conversion.

The TD1021 analog amplitude data sample is read 10 ns after the 50% point of the convert pulse rising edge. In addition, the pulse is a positive TTL amplitude and should be nominally 30 ns wide. From these conditions, the convert pulse should be decoded from the timing logic so its leading edge is 10 ns ahead of the desired sample point on the output

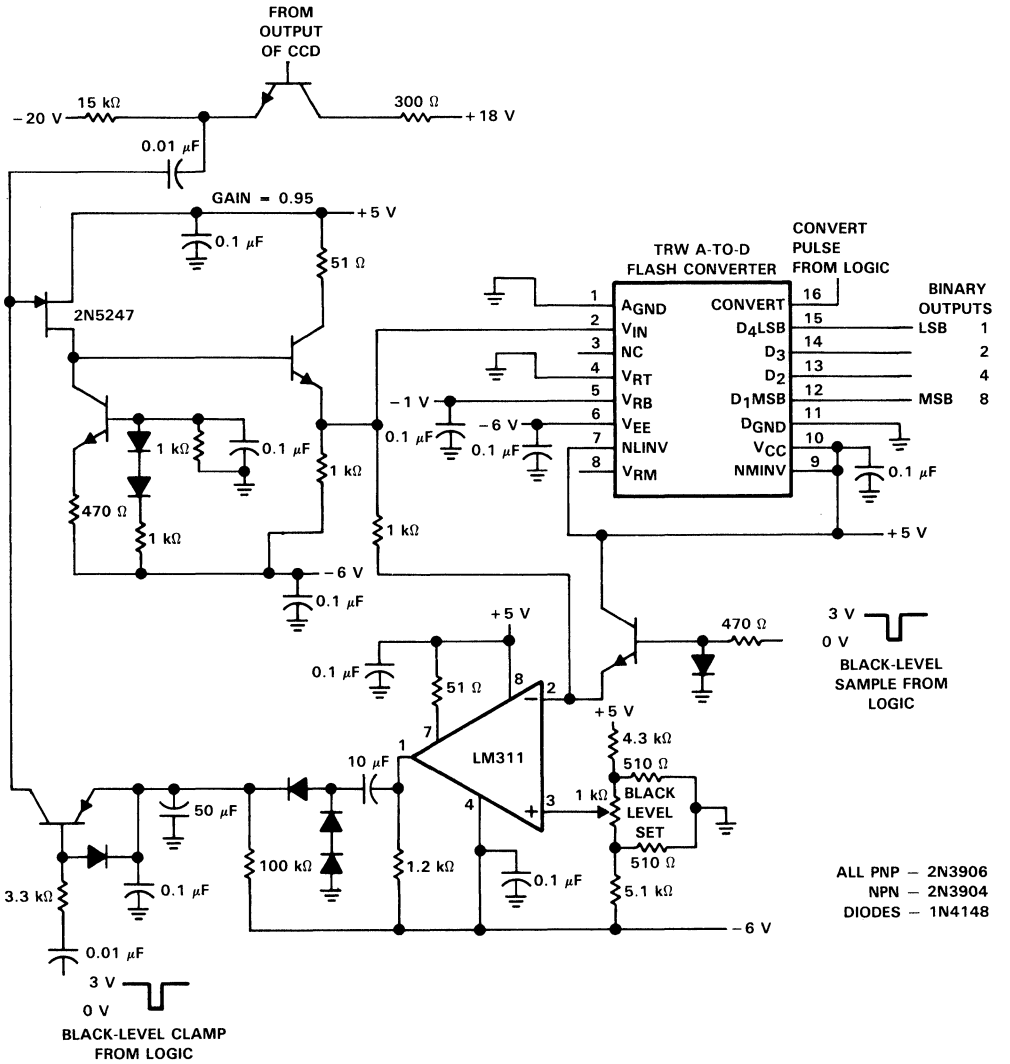


Figure 10. Automatic Black-Level Control and A/D Converter (0.1 to 10 MHz Operation)

pixel pulse of the CCD. In order to approximate where to decode the convert pulse, it is necessary to determine the time delay of the pixel pulse arriving at the analog input of the converter relative to the logic from which the convert pulse is to be decoded. The propagation delay time between the reset clock high-to-low transition and the high-to-low transition of the pixel is 15 ns (see Figure 11).

In addition, as shown in Figure 12, the reset clock rising edge is located where the transport clock feedthrough starts to disturb the data pixel. Therefore, the convert pulse should end exactly where the reset pulse starts and should exist 30 ns before that point. The timing diagram in Figure 2 indicates that this is the location shown for the convert pulse and it is decoded from the logic symbols by an AND function of logic signals D and delayed B as shown in Figure 1. Logic signal B is delayed by one gate delay to narrow the convert pulse by 10 ns so that pulse will be 40 ns or less wide. Since the pixel delay was also taken with respect to the reset clock, which is delayed from the logic signals used for decoding, additional delay would be needed to place the convert signal exactly as required. Two SN74S08 AND gates were added to provide this delay. Figure 12 shows the CCD pixel data entering the A/D converter and the convert pulse show how well this timing method works.

The results of this design approach are represented in Figure 13. This optical input for the CCD is a uniform illuminated seven-gray shade and black using an incandescent source operated from direct current to prevent 60-cycle modulation. No IR filter is used because there would not be enough light output to produce a 1-V CCD output. As a result

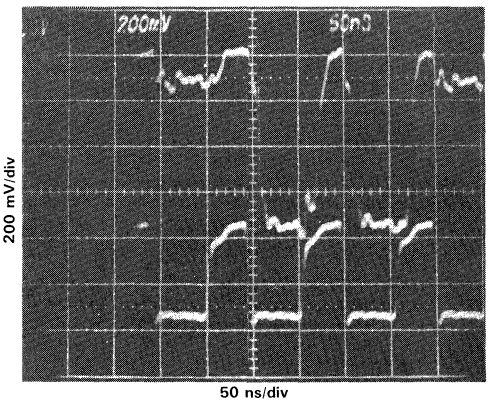


Figure 11. Conditioned CCD Output Signal Time Related to Reset Clock

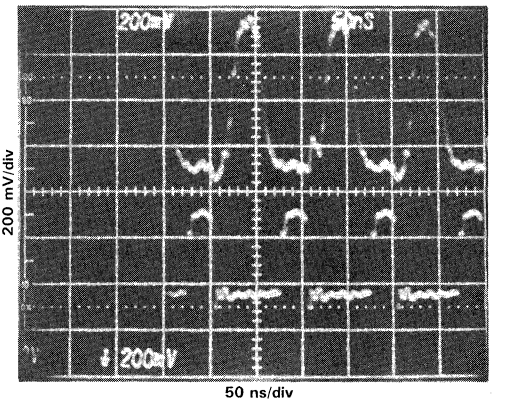


Figure 12. Conditioned CCD Output Signal Time Related to Convert Pulse

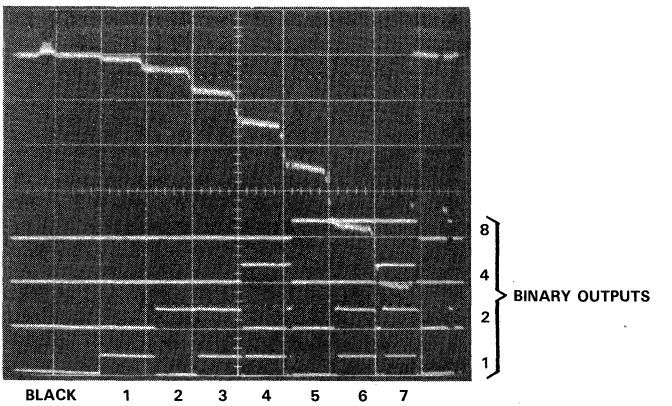


Figure 13. Conditioned CCD Gray Shade Signal and A/D Converter Binary Outputs

of the IR plus visible light combined, the gray shades are not uniform changes in intensity. However, this does not detract significantly from the presentation. The A/D converter was set up for its output to be 0000 for a 0 V input and 1111 for a −1 V input. Therefore, −0.067 V analog equals one binary bit state change. Combining the digital outputs with the conditioned CCD signal adds ringing and spikes to the signal. The ringing and spikes are undesirable in the final presentation at 10 MHz output. Figures 14, 15, and 16 show relatively clean output signals.

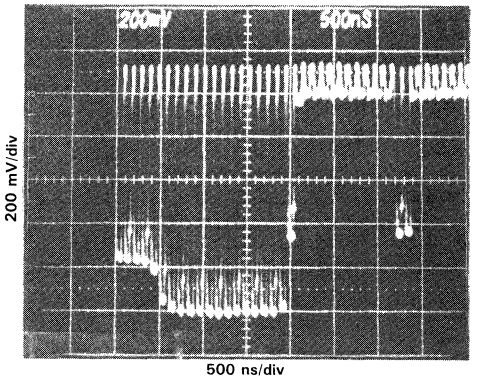


Figure 14. Conditioned CCD Output with Optical Input (10 MHz Operation — 500 ns/div)

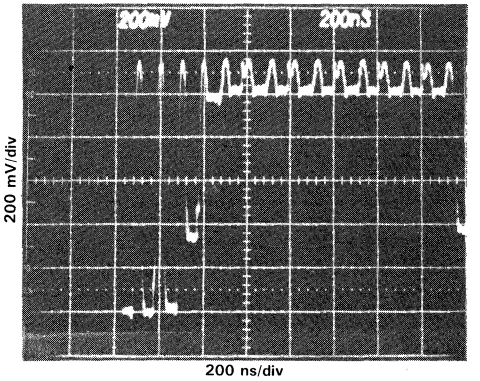


Figure 15. Conditioned CCD Output with Optical Input (10 MHz Operation — 200 ns/div)

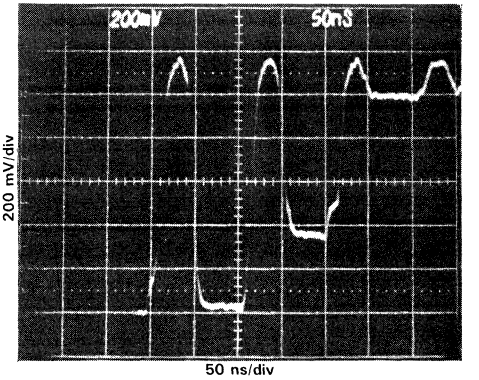


Figure 16. Conditioned CCD Output with Optical Input (10 MHz Operation — 50 ns/div)

CONCLUSION

The methods and circuits presented for 10-MHz operation of the TC102 linear image sensor have been directed at the elimination of the transport clock feedthrough from the output signal, automatically maintaining the output signal black reference, and digitization of each pixel output. Although the TC102 is highlighted in this report, the methods described can be applied to the complete family of virtual phase linear CCD devices for operating frequencies in the range to 10 MHz.

OPERATING INSTRUCTION SET FOR LINEAR CCD IMAGE SENSOR

Introduction

The PC401 and PC402 are the Evaluation Boards designed to facilitate operation of the Texas Instruments CCD linear imager sensors. The PC401 operates the following types of imagers:

TC103	(2048 x 1 pixel organization)	Reference: Evaluation Kit – TCK103
TC104	(3456 x 1 pixel organization)	Reference: Evaluation Kit – TCK104
TC106-1	(2592 x 1 pixel organization)	Reference: Evaluation Kit – TCK106-1

The PC402 operates the following type of imager:

TC102	(128 x 1 pixel organization)	Reference: Evaluation Kit – TCK102

The boards are intended to be used as construction aids for experimental systems using the above-listed CCD line-scan imagers. The necessary electronic systems required to drive the CCD imagers are included. Only the input of power supplies and optics is required. The logic circuitry required to time the drive signals correctly and the drivers that interface the logic to CCD levels is provided on the board.

Clocking control is provided by an internal clock generator that can produce data rates from 200 kilohertz to 2 megahertz and can, if required, be overridden by an external clock input.

Exposure time control is also available internally with provision for exposure times from 2 to 16 milliseconds, and can also be overridden by an external input.

Clock voltages for transport, transfer, and reset clocks are controlled as shown below.

- The low-level voltage levels are directly controlled from one of the external supplies (V_{IL}).
- The high-level voltage levels are supplied from the board and can be adjusted (V_{CH} adjust).

Power Supply Requirements

Three voltage supplies are required:

(1) Logic supply: +5 volts, 300 milliamperes
(2) Imager output amplifier (V_{DD}): +16 volts min, 100 milliamperes
(3) Imager low-level clock (V_{IL}): −16 volts min, 100 milliamperes

Equipment Required for a Typical Setup

(1) Oscilloscope (Tektronix Model 765)
(2) Current-limited power supplies (two HP 6216A, one HP 6214A)
(3) CCD imager being evaluated
(4) Connectors for connecting board to power supplies

Procedure

(1) Adjust the power supplies as follows:
  Supply #1: +5 volts, current limit 250 milliamperes
  Supply #2: +16 volts, current limit 70 milliamperes
  Supply #3: −16 volts, current limit 70 milliamperes
(2) Connect the power supplies to the evaluation board as shown in Figure 1.
(3) Adjust the oscilloscope with the main sweep set to 2 milliseconds per division and vertical sensitivity set to 5 volts per division. Connect the external sync of the scope to the white reference clock (WRCK) test point shown in Figure 1 to synchronize the scope with the exposure time rate.

(4) The following clock voltage amplitudes can be checked at test points shown in Figure 1.

		LOW LEVEL	HIGH LEVEL
WRCK	White reference clock (selected by J2 jumper)	6 to 8 V	15 to 16 V
XCK	Transfer clock†	−16 to −13 V	1 to 5 V
TCK	Transport clock†	−16 to −13 V	1 to 5 V
RCK	Reset clock†	−16 to −13 V	1 to 5 V

†Set per CCD specification in data sheet for the device being evaluated. The high-level voltage for XCK, TCK, and RCK are adjustable using the $V_{CH(ADJ)}$ potentiometer shown in Figure 1. The low level is set by adjusting the −16-volt power supply, V_{IL}.

(5) When the clock levels have been checked, plug the CCD imager to be tested into the test socket and connect the vertical oscilloscope probe to the output-signal test point (see Figure 1). Set the vertical amplifier to "ac coupled" and set the sensitivity to 0.2 V/division. NOTE: Recheck clock levels after inserting CCD into test socket and readjust clock levels if necessary.

(6) Begin with a low light level on the imager and increase the light level until an output level of approximately 0.4 volts is obtained. Note that if a shadow is cast across the imager the amplitude of the output signal is affected in the region of the shadow.

(7) Check the effects of exposure time by adjusting its control (see Figure 1). Observe the time between the white reference output signals (see Figure 2). Set the exposure time to 10 milliseconds. Instructions for external exposure time control are shown in the next section.

(8) Check the output frequency range by setting the frequency-adjust potentiometer to each extreme and observing the frequency range with the oscilloscope. The board should deliver a range of 0.3 to 2 megahertz. Set the frequency to 0.5 megahertz.

(9) With the main sweep set at 1 millisecond per division, and with the expanded sweep set at 10 microseconds per division, look for the output white reference signal. When it is found, move the probe from the output signal test point to the end-of-scan (EOS) test point and verify its presence (see Figure 2).

(10) If the TC103 or TC104 is under evaluation, note that an internal reference voltage pin (pin 5) is provided from the CCD. This pin provides the reference voltage for V_{REF} (pin 1) of the output signal amplifier of the imager. Jumper J4 can be set to connect INT REF and V_{REF} of TC103, TC104, or TC106-1 through a 5.1-kilohm resistor (see Figure 3). For TC102, J4 is set to connect V_{REF} to the 7.2-volt point on the voltage divider between V_{DD} and ground (see Figure 3).

(11) Figure 4 outlines the timing waveforms at test points A through G with appropriate clock pulses.

External Exposure Time

Refer to Figure 3. With jumper J3 set to external position (EXT) and with an appropriate external counter chain, the exposure time can be set as a multiple of transport clock (TCK) period. The output from the external counter is returned to the external exposure time input.

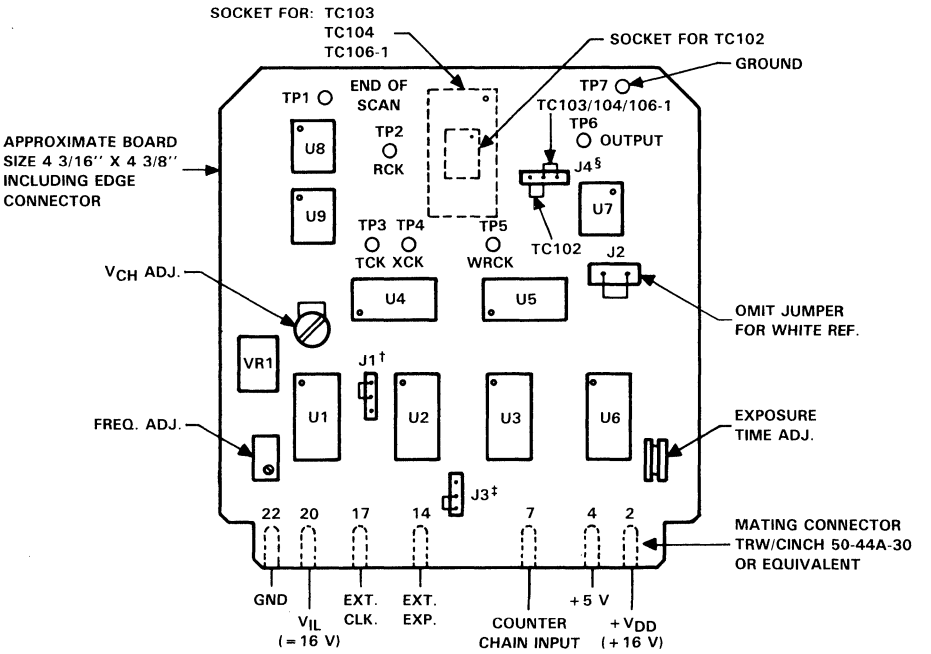
An example of such a circuit is shown in Figure 5. For a data rate of 0.5 megahertz, the time between the white reference outputs (defined as exposure time) for this example is 8188 microseconds. This time may be varied in increments of 4 microseconds (2/data rate) by changing the input to the preset input lines. (Data rate = RCK frequency = 2 X TCK frequency.) Therefore:

TCK = data rate/2 = 500,000/2 = 250,000

Since the preset input down count = 111111111110 = 2047, time per count = 4 microseconds.

Thus:

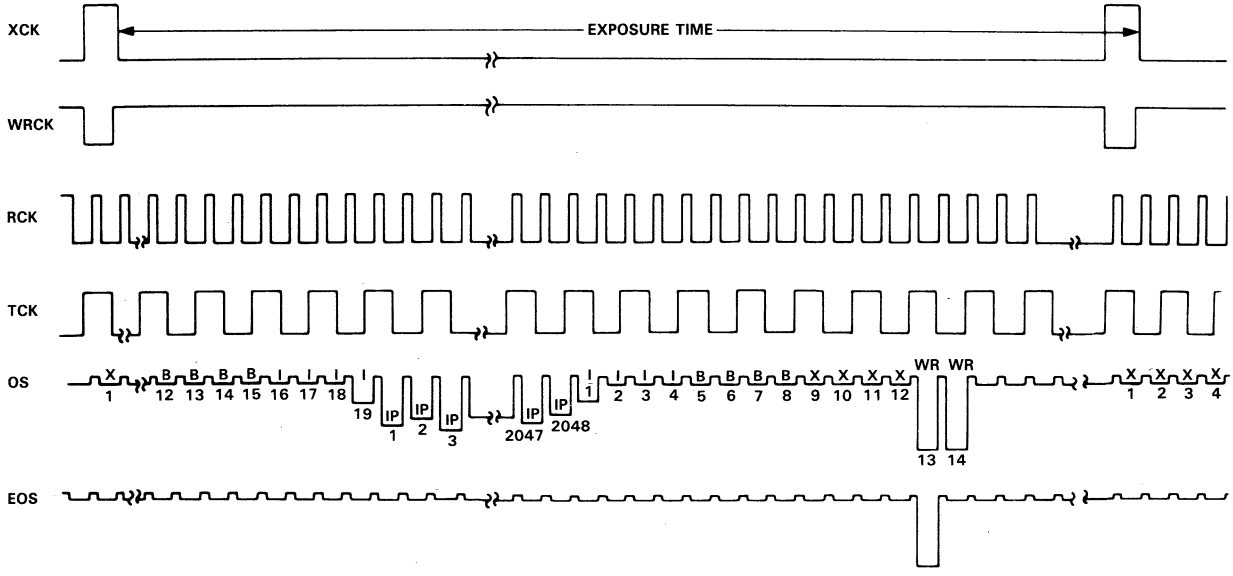
Exposure time = 2047 counts X 4 microseconds/count = 8188 microseconds



(J1 & J3 SHOWN IN INTERNAL SELECT POSITION)

†J1 = INTERNAL/EXTERNAL CLOCK SELECT
‡J3 = INTERNAL/EXTERNAL EXPOSURE TIME SELECT
§J4 = INTERNAL/EXTERNAL REFERENCE VOLTAGE (V_{REF}) SELECT

FIGURE 1. LINEAR CCD EVALUATION BOARD



Output Signal (OS) pulse identification: I = Isolation pixel, IP = Image pixel, B = Black reference pixel, WR = White reference pixel, X = Empty pixel.

FIGURE 2. OPERATING INPUT AND OUTPUT VOLTAGE WAVEFORMS (TC103 SHOWN)

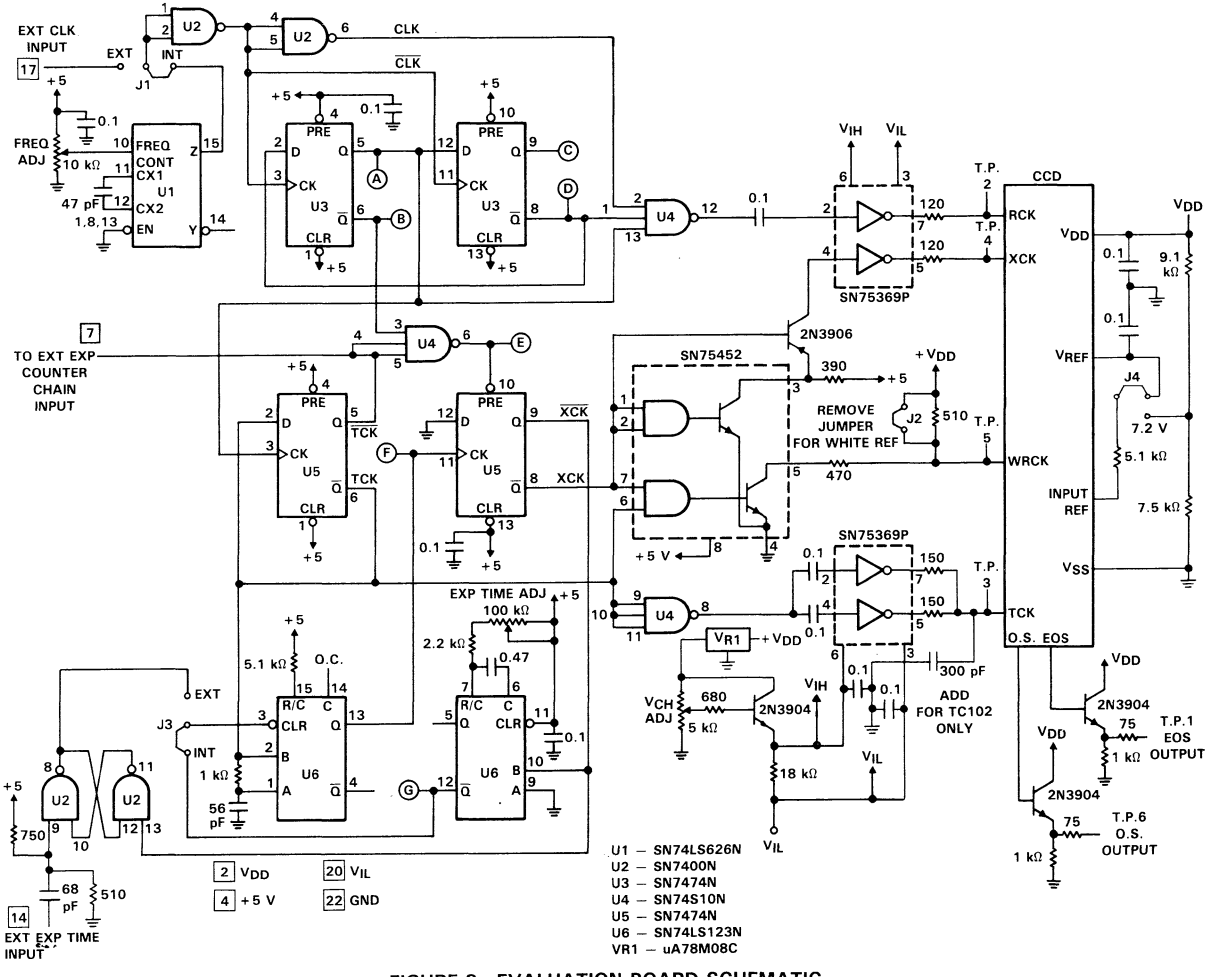


FIGURE 3. EVALUATION BOARD SCHEMATIC

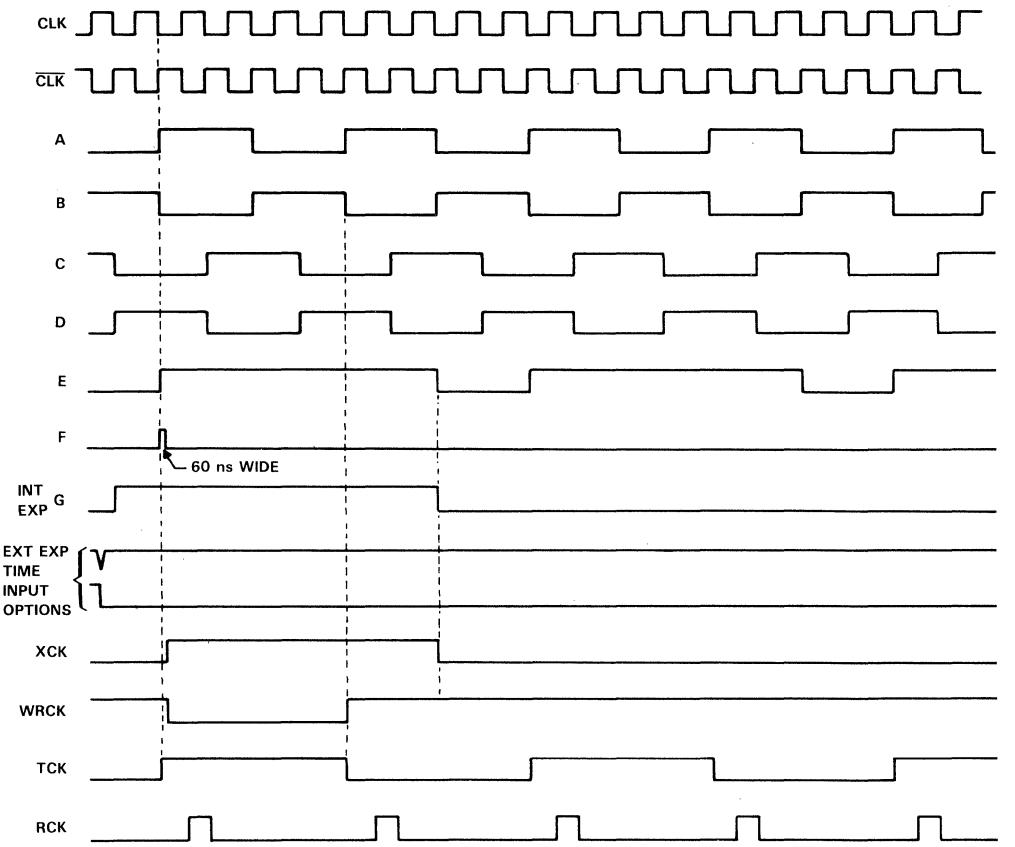


FIGURE 4. LOGIC TIMING WAVEFORMS

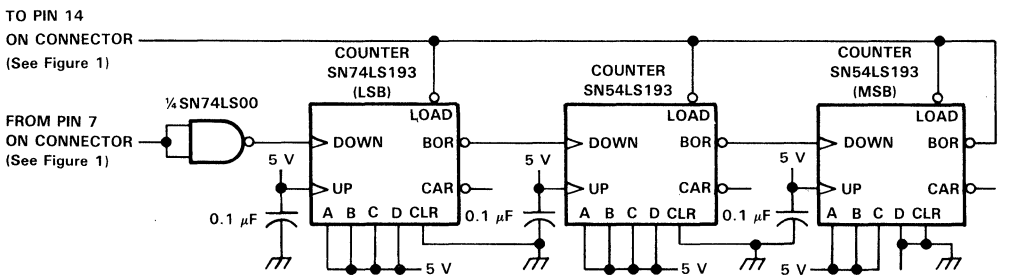


FIGURE 5. EXTERNAL TIME EXPOSURE CIRCUIT

A SIMPLE METHOD OF CONDITIONING THE OUTPUT OF A CCD IMAGER FOR INTERFACING TO A DIGITAL SYSTEM

introduction

For applications such as bar-code reading or optical character reading, it may be desirable to convert the analog output of a Charge-Coupled Device (CCD) imager into a binary waveform in which one logic level represents "black" and the other "white". The resulting binary waveform could then be used as a data input to a digital processing system for decoding (a microprocessor, for example). A simple, low-cost method of producing such a waveform is described below.

In the circuit shown in Figure 1, the voltage output of a CCD imager is amplified, filtered, rectified, and "digitized" to produce a simple serial representation of the image. The input of the circuit is required to be at standard video level (approximately 1 volt peak-to-peak), and the output is a TTL-compatible signal. Following is a detailed description of how the circuit operates.

description of circuit

The signal from the CCD imager is first amplified by the LM318 (U2). C1 removes the DC offset from the input, and R1 and R2 determine the gain of the amplifier. The gain of the amplifier is approximately −200 and severely clips the signal. Because the circuit needs only to distinguish "black" from "white", no information is lost, and in fact the clipping is actually beneficial to the performance of the circuit. This benefit is gained by clipping because it partially removes some of the undesired transfer clock components from the signal. Next, the inverted and amplified signal is rectified by CR1. This limits the negative swing of the rectifier output to one diode drop below ground. At this point, the "black" level is at or slightly below zero volts. Next, the signal is integrated by R3 and C3. This acts as a low-pass filter, removing most of the transfer-clock component from the signal. The final stage is a comparator, U2, with hysteresis (provided by the combination of R4 and R5) that squares the filtered and rectified signal and provides the final TTL-level output. Because the transfer clock cannot be completely removed from the signal with only a single-order integrator, there is still some high-frequency noise riding on the signal at the input to the comparator. The hysteresis allows the comparator to ignore the effects of this noise. Without the hysteresis, spurious pulses would appear at the output.

evaluation

This circuit was breadboarded and tested using the TCK103 evaluation board to provide the necessary timing signals and preamplification of the CCD imager output. The TCK103 uses a Texas Instruments TC103 imager, a 2048-element linear imager that is capable of providing resolution up to 240 points per inch. It was found that there was some degradation of the imager resolution due to the coarseness of the integration. It is believed that a higher order integrator might improve resolution. One factor to consider in analyzing the value of this circuit implementation in a practical application would be to weight the low cost and minimal parts count of this solution against a more complicated and expensive solution yielding less degradation of resolution.

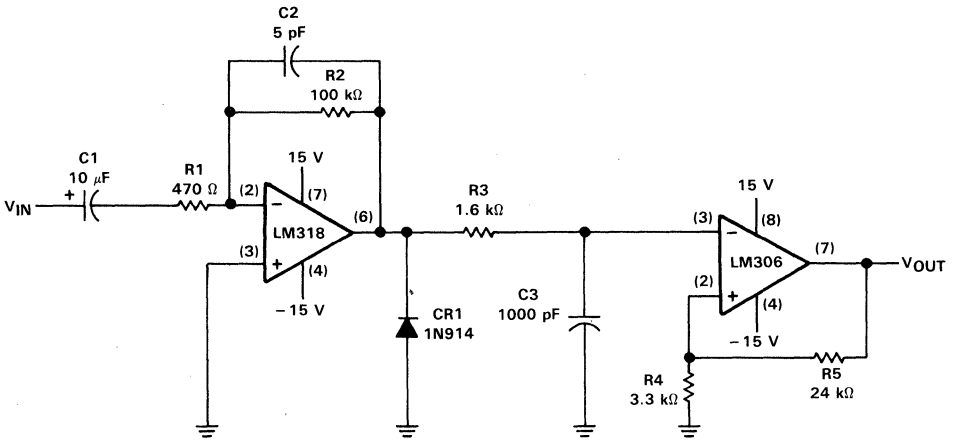


FIGURE 1. SCHEMATIC DIAGRAM OF CCD IMAGER SIGNAL CONDITIONING CIRCUIT

TC103-ISM Interfacing Circuit

Introduction

Features of TC103

- 2048 × 1 Sensor Element Organization
- Virture-Phase Technology
- Enhanced Blue Response
- Output Signal Approximately . . . 1 V Peak-to-Peak
- Maximum Operating Frequency . . . 10 MHz
- Effective Sensing Length . . . 254 nm (A4, B4 size)

TC103-ISM Scanner Module

The TC103-ISM is used to evaluate the TC103 CCD. It contains the optical system, the driving circuit for the CCD, and a TC103 CCD, itself. The operating frequency is 2 MHz. The output data rate is 500 kHz. The resolution is 200 dots per inch and there are 2048 sensing elements. Hence, the time required to scan a line is 4.096 ms.

The illumination source for the TC103-ISM is a white fluorescent lamp. The wavelength is between 390 nm and 600 nm. The effective optical path is 333 nm.

The output signals from the TC103-ISM are the Output Signal (OS) and the Transfer Clock (XCK). The waveform of OS can be observed with an ocsilloscope.

Interfacing Circuit

The interfacing circuit is designed to interface the CCD Scanner Module and a PC. The image is first scanned by the scanner and the data is sent to the PC. The resulting image is printed by a laser printer such as the TI Omnilaser 2115.

The input signals consist of the Master Clock (MCLK), the Transfer Clock (XCK), and the Scanner Output Signal (OS). The analog signal is sent through the threshold comparator (U1, LM311) and becomes a digital signal. The threshold voltage is set by observing the comparator output waveform (U1, pin 7). A flip-flop (U2A, SN74LS74) is used to clock the data and a serial-to-parallel shift register (U3, SN74LS164) is used to convert 8 bits of data into one byte. Since there are 2048 bits of data for one image line, a total of 256 bytes of memory space needed.

The XCK is used to indicate at which point the image data starts. When this signal goes from low to high, OS contains the beginning of the image data. Hence, a flip-flop (U2B, SN74LS74) is used to start the reading sequence.

From the timing diagram of the scanner module, it is found that the first valid data appears after 87 Master Clock (MCLK) cycles. An 8-bit counter (U8, SN74LS590) is used to do the counting. As seen in Figure 2, 89 MCLK cycles are then chosen to be the delay time before reading any data into memory. When the counter counts to 89, it will trigger the CCDPAL1 (U9) and a Start-Of-Scan (SOS) signal will, in turn, trigger another flip-flop (U12B, SN74LS74), which will reset the CCDPAL2 (U10). The input clock to CCDPAL2 is MCLK divided by 4 and this clock is further divided by 8 and becomes the counter clock for the second counter (U6, SN74LS590). A write-enable signal will also be generated and fed to the SRAM chip (U5, IDT6116). The addresses for the SRAM chip are produced by the second counter with increment for every 32 MCLK cycles. Therefore, all the 256 bytes of data will be stored into the SRAM without any software control.

When the second counter counts to 256, a Ripple-Carry-Over (RCO) pulse will be sent to the TMS7742 microcontroller. This pulse will interrupt the microcontroller and an interrupt service routine will begin.

TMS7742 Program

There are 4 I/O ports in the TMS7742. In this circuit, ports A and B are used as I/O controller ports. Port C is used as the data/address port and port D controls the upper 3 bits of the SRAM address.

When the program is initialized, I/O signals are sent to clear and disable all flip-flops and counters. Next, the flip-flops and counters are enabled and the TMS7742 enters the idle state until interrupted by RCO signal from the second counter (U6). When interrupted, the address is placed on port C and latched (U7, SN74LS373). A read-enable signal is then sent to the SRAM and read from port C. After reading all 256 bytes of data, the data is sent to a computer via the on-chip serial port and a data-level converter (U14, MC1488). A laser printer then prints the resulting image.

It should be noted that the TMS7742 is operated in the single-chip mode. The operating frequency is 5 MHz. Only 174 bytes are used to write the interfacing program.

Application

The CCD scanner and the interfacing circuit are designed to be used as an optical reader. Applications include facsimile scanner, optical recognition, and PC scanner.

The interfacing circuit is capable of producing a correctly scanned line of image on a laser printer and a thermal head printer. Demonstrations were performed with good results.

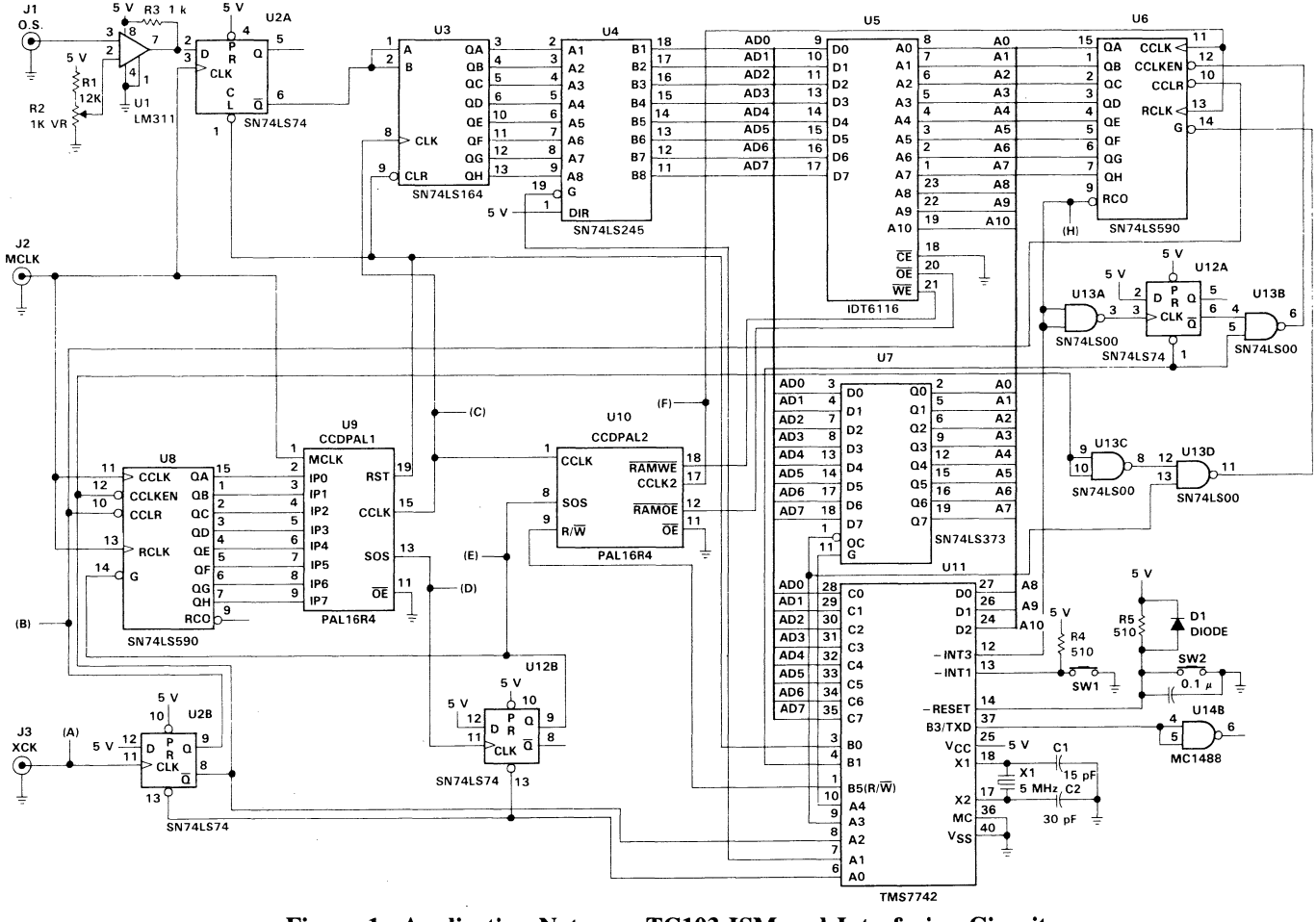


Figure 1. Application Notes on TC103-ISM and Interfacing Circuit

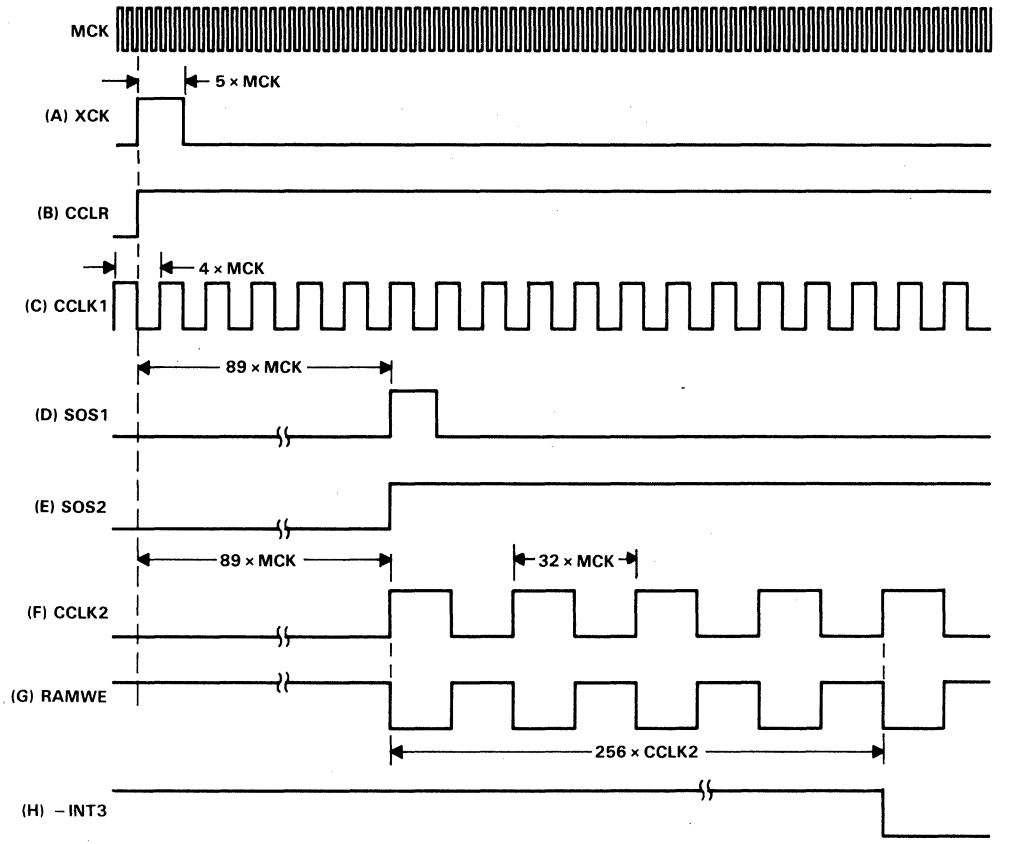


Figure 2. Timing Diagram for CCD Scanner Interface Circuit

Scanner Module Timing Descriptions

Timing Diagram No. 1

This timing diagram shows the scanner module input logic and the PAL® IC output logic.

Scanner Module Logic Inputs

SIGNAL NAME	DESCRIPTION
MCLK	Master clock for all input logic and PAL® logic. This clock operates at 2 MHz at 50% duty cycle.
XCK	This signal provides the clock logic for the CCD transfer clock input. The period of this signal determines the integration time for the CCD. This period has been set to 5 ms for the scanner module.
CLMP	This signal provides the clamp logic for the video processing circuitry.

PAL® IC Output Logic

SIGNAL NAME	DESCRIPTION
TCK	This signal provides the clock logic for the CCD transport clock input. The frequency of this signal is 1/2 the data rate.
RCK	This signal provides the clock logic for the CCD reset clock input. The frequency of this signal (500 kHz) determines the data rate.
S/H	This signal provides the sample and hold logic for the TL1591 Sample/Hold IC.
$\overline{\text{RCK}}$	This signal provides the conversion logic for the TL5501 6-bit A/D converter.

Timing Diagram No. 2

This timing diagram shows the relationship between the master clock (MCK) and all the CCD clock signals (XCK, TCK, RCK) for the sample/hold logic (S/H) and the A/D converter logic ($\overline{\text{RCK}}$).

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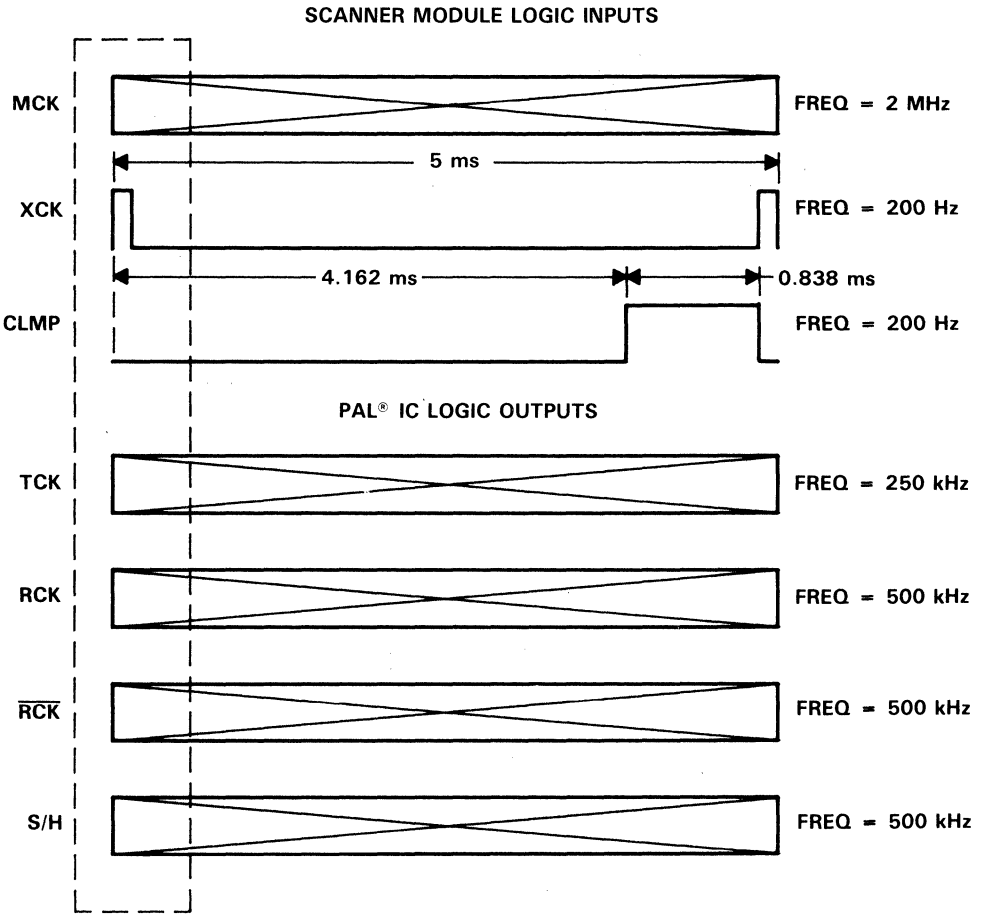


Figure 3. Timing Diagram No. 1

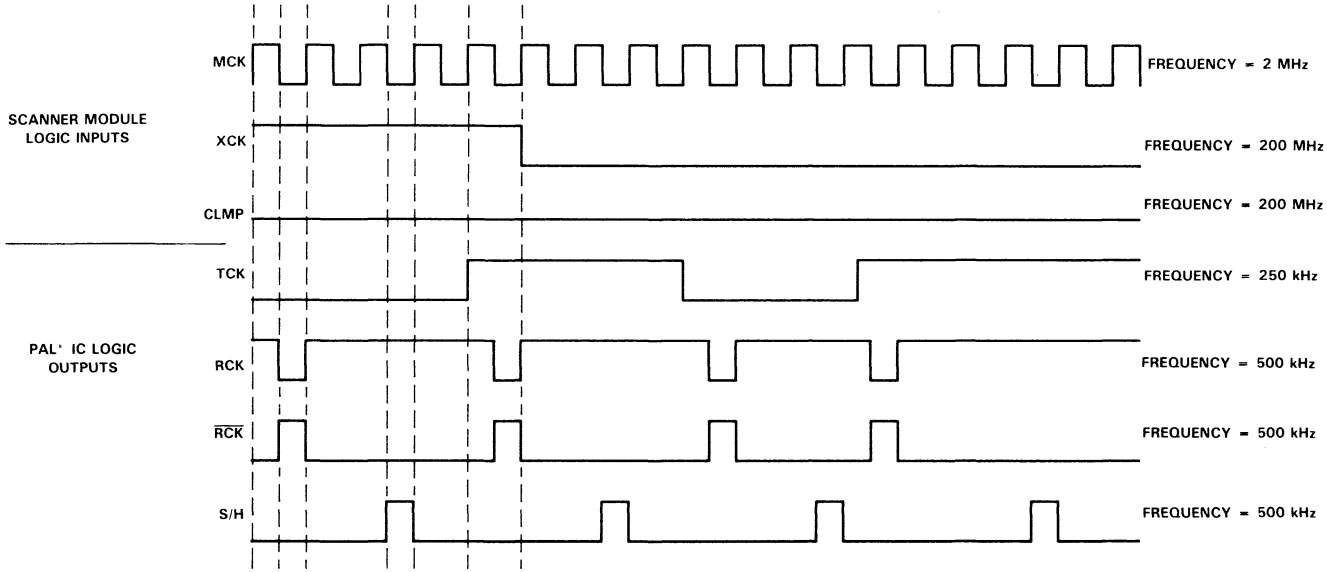
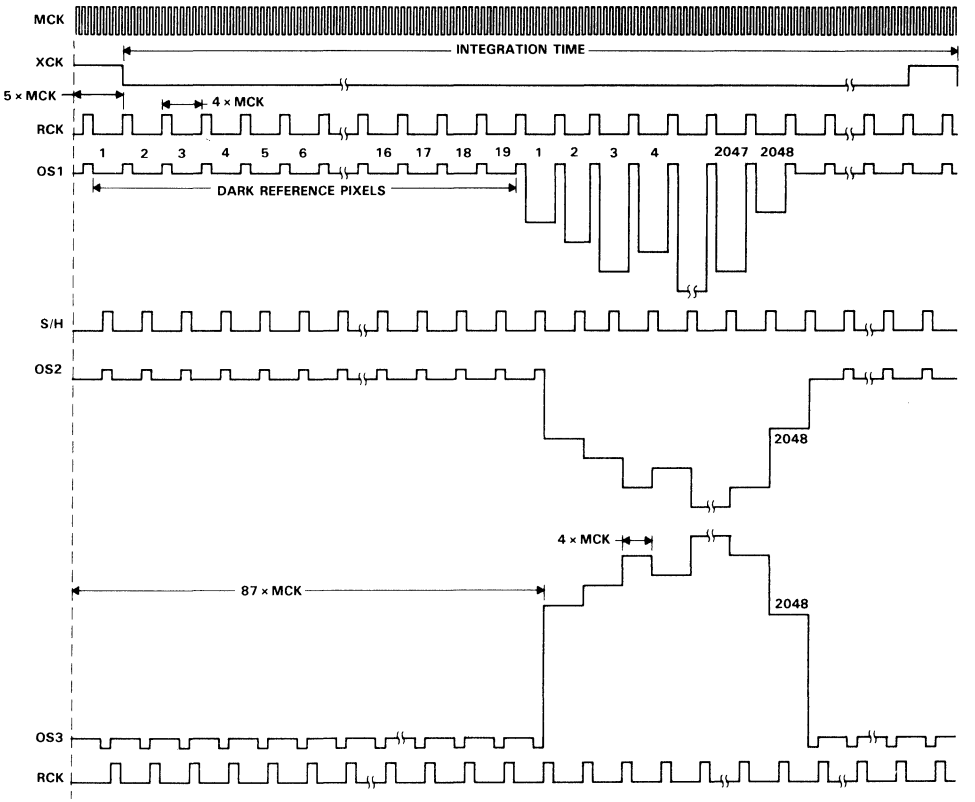


Figure 4. Timing Diagram No. 2

Timing Diagram No. 3

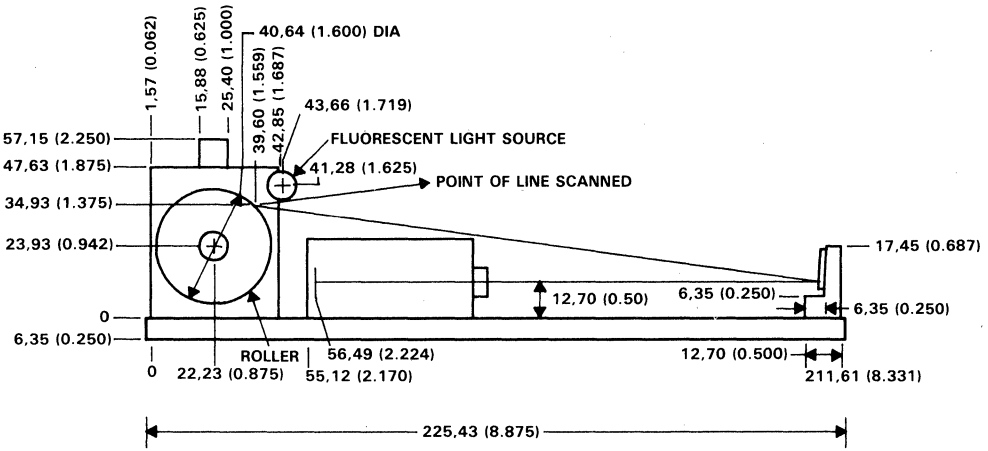
This timing diagram shows the entire frame time for the scanner module. The video signal is shown at various points in the video processing.

SIGNAL NAME	DESCRIPTION
OS1	This is the raw CCD signal. The dark reference pixels (19) precede the active pixels (2048).
OS2	This is the sample and held video signal. The sample and hold removes the reset to zero between pixels.
OS3	This is the amplified, inverted, clamped, and buffered video signal. This signal is available at the output connector of the scanner module. It is also input into the 6-bit A/D for digitizing.



NOTES: $\overline{\text{RCK}}$ logic is the A/D conversion clock
OS1 is the CCD video signal
OS2 is the sample and hold video signal
OS3 is the amplified and inverted video signal

Figure 5. Timing Diagram No. 3



ALL DIMENSIONS ARE NOMINAL IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: Module is attached to demo fixture. TI will supply the module; customer should supply roller and light source in production.

Figure 6. Dimensions of Module

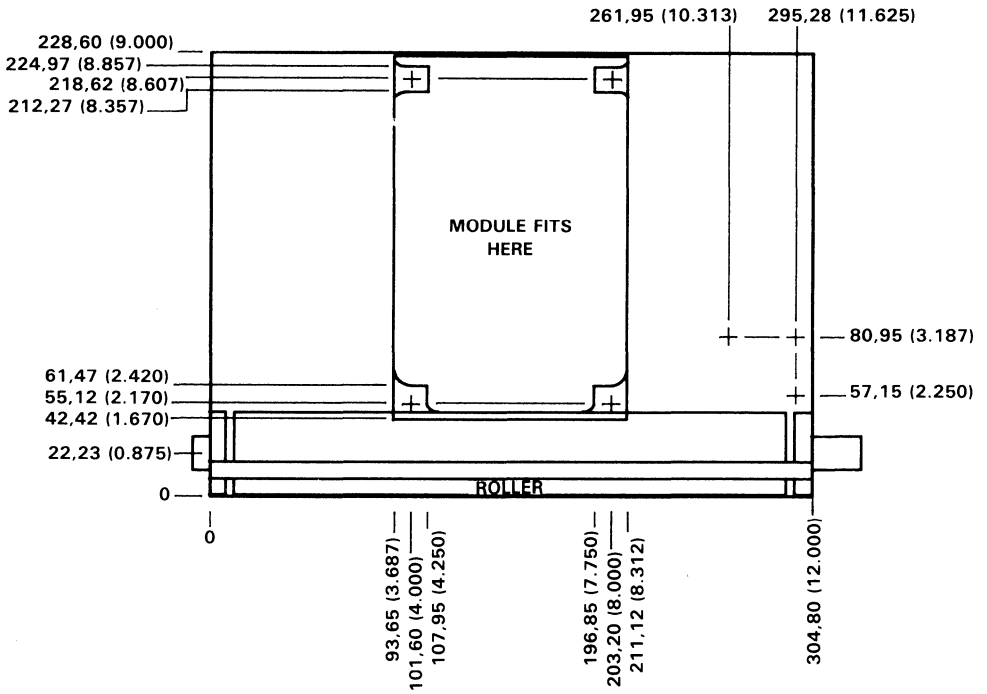


Figure 7. Dimensions of Scanner Demonstration Unit

Parts List for Scanner Board

DEVICE CATEGORY	SCHEMATIC NAME	DEVICE TYPE
Chips†	U1	TIBPAL16R4-10CN (20-pin)
	U2	TL1591CP (8-pin)
	U3	NE5534P (8-pin)
	U4	SN75369 (8-pin)
	U5	SN75369P (8-pin)
	U7	LM310N (8-pin)
	U8	TL5501CN (16-pin)
	U9	LM310N (8-pin)

†All chips have 2.54-mm (0.100 in) center spacing.

Parts List for Scanner Board (Continued)

DEVICE CATEGORY	SCHEMATIC NAME	DEVICE TYPE	WVDC†
Transistors	Q1	2N3906	
	Q2	2N3904	
	Q3	2N3904	
	Q4	SD214DE	
Resistors‡	R1	2.2 kΩ	
	R2	390 Ω	
	R3	120 Ω	
	R4	120 Ω	
	R5	5.1 kΩ	
	R6	150 Ω	
	R7	150 Ω	
	R8	680 Ω	
	R9	18 kΩ	
	R10	1 kΩ	
	R11	75 kΩ	
	CR2	1 kΩ	
	CR1	1 kΩ	
	R20	2.5 kΩ	
	R21	10 kΩ	
Potentiometers§	R16	5 kΩ (3299 W)	
	R16	5 kΩ (3299 W)	
	R16	5 kΩ (3299 W)	
	R16	5 kΩ (3299 W)	
Capacitors (see Notes 1, 2, and 3)	C1	0.1 μF	50 V
	C2	0.1 μF	50 V
	C3	10 μF	35 V
	C4	10 μF	35 V
	C5	0.1 μF	50 V
	C6	0.1 μF	50 V
	C7	0.1 μF	50 V
	C8	0.1 μF	50 V

†WVDC—Working dc voltage
‡All resistors are 1/4 W and have a 5% tolerance.
§Potentiometers are 1/2 W @ 70°C and are three-lead, in-line potentiometers with 2,54-mm (0.100 in) center spacing and are adjusted from the top.

NOTES: 1. Use 5-mm (0.200 in) spacing between leads of each capacitor.
2. The 10-μF and 100-μF capacitors are tantalum.
3. All 0.1-μF capacitors are ceramic.

Parts List for Scanner Board (Concluded)

DEVICE CATEGORY	SCHEMATIC NAME	DEVICE TYPE	WVDC†
Capacitors (see Note 1, 2, and 3)	C9	0.1 μF	50 V
	C10	0.1 μF	50 V
	C11	0.1 μF	50 V
	C13	0.1 μF	50 V
	C14	0.1 μF	50 V
	C15	10 μF	35 V
	C16	10 μF	35 V
	C17	0.1 μF	50 V
	C18	0.1 μF	50 V
	C19	10 μF	35 V
	C22	100 μF	20 V
	C23	0.1 μF	50 V
	C24	0.1 μF	50 V
	C27	0.1 μF	50 V
	C28	10 μF	35 V
	C29	0.1 μF	50 V
	C30	0.1 μF	50 V
	C32	100 pF	200 V
	C33	100 pF	200 V
	C34	22 pF	200 V
Inductors	L1	470 μH	
	L2	1 mH	
	L3	1 mH	
Connectors	J1‡	102444-5	
	J2§	1-102445-6	
Test point pins	TP1-TP9	T49	

†WVDC—Working dc voltage

‡J1 10-pin straight post, double-row header connector with 2,54-mm (0.100 in) center spacing.

§J2 16-pin right-angle post, single-row connector with 2,54-mm (0.100 in) center spacing.

NOTES: 1. Use 5-mm (0.200 in) spacing between leads of each capacitor.
2. The 10-μF and 100-μF capacitors are tantalum.
3. All 0.1-μF capacitors are ceramic.

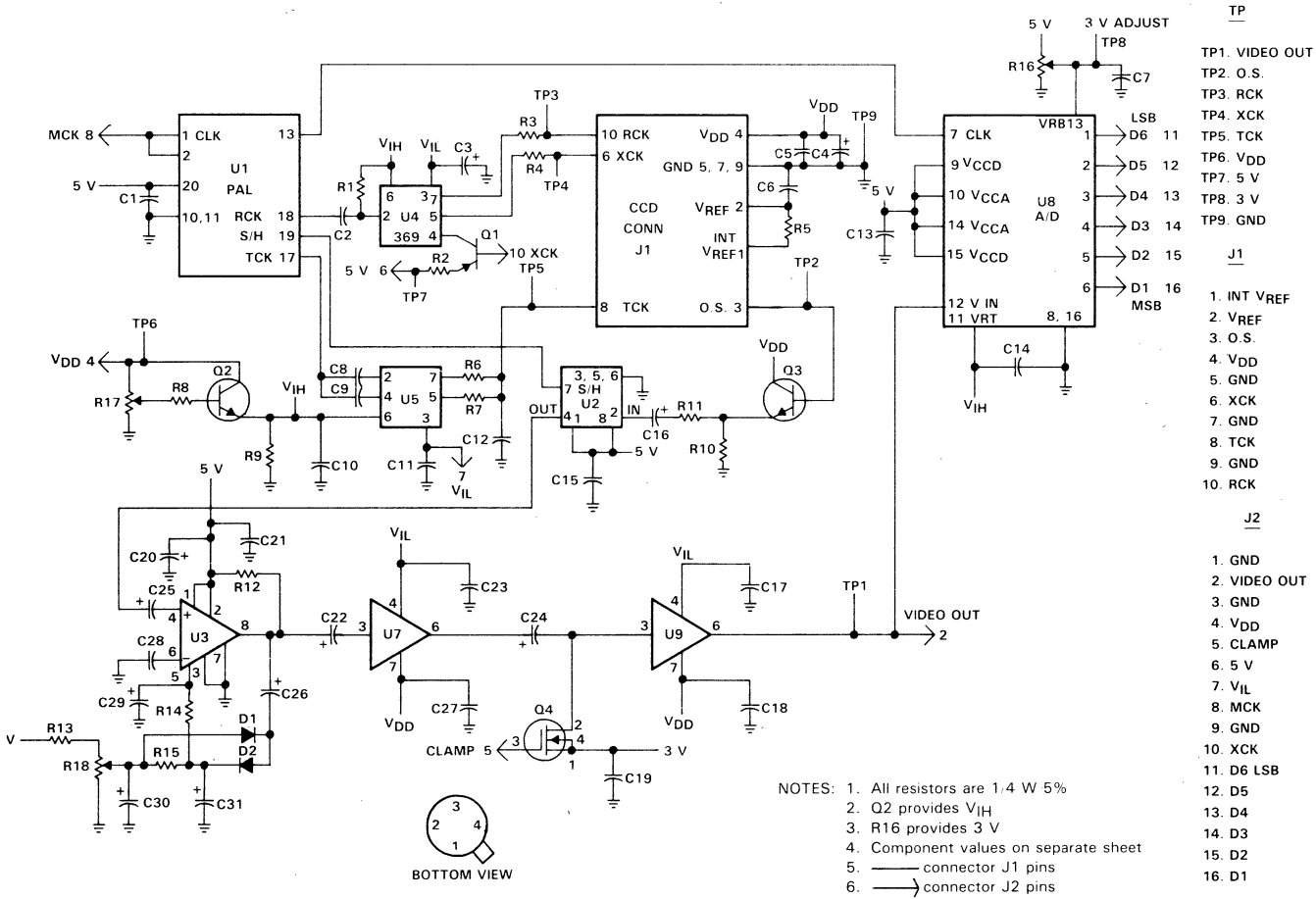


Figure 8. Scanner Board SB1

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