



Advanced Logic and Bus Interface Logic

Data Book

Data Book

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INTRODUCTION

The new advanced logic and bus interface logic solutions from Texas Instruments can help you design today's high-performance, low-power bus interface while addressing important design issues such as enhancing speed and conserving board space.

Solutions include:

- ACL LSI for high-speed, low-power logic requirements
- ACL Widebus™ Series doubles I/O count in the same board area
- BiCMOS and submicron BiCMOS bus-interface logic families offering drivers, transceivers, latches, registers, and registered and latched transceivers
- Bus-termination arrays for an effective termination solution
- · Clock drivers minimize skew
- ECL translators for fast, low-power ECL/TTL translations
- FIFOs help accelerate overall system performance
- Futurebus+ transceivers with logic voltage levels selected to optimize bus performance
- Low-impedance line drivers with speed and power characteristics similar to those of BCT octals and drive capability of 188 mA
- SCOPE[™] products providing on-chip testability
- 64 Series BiCMOS designed for the telecommunications-or industrial-equipment market to withstand extended temperature ranges and hot-card insertion

This book provides pertinent technical information on available and planned advanced logic and bus interface logic devices. Additionally, the General Information Section contains an alphanumerical index, functional index, and other useful information.

For more information on Texas Instruments advanced logic and bus interface logic products, please contact your local TI field sales office or authorized distributor, or call Texas Instruments at 1-800-232-3200.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i Input capacitance

The internal capacitance at an input of the device.

Co Output capacitance

The internal capacitance at an output of the device.

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

fmax Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

ICC Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

ΔICC Supply current change (ACT devices only)

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input.

IIL Low-level input current

The current into* an input when a low-level voltage is applied to that input.

IOH High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

IOL Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

IOZ Off-state (high-impedance-state) output current (of a three-state output)

The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

^{*}Current out of a terminal is given as a negative value.



ta Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

Disable time (of a three-state or open-collector output) tdis

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, tdis = tpHz or tpl z. Open-collector outputs will change only if they are low at the time of disabling so this = tpl H.

ten Enable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., G). For 3state outputs, ten = tpzH or tpzL. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, ten = tpHI.

Hold time th

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is quaranteed.
 - The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Propagation delay time tpd

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (tpd = tpHI or tpi H).

tPHL Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tPHZ Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

tpLH Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.



tpLZ Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

tрун Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

tpzL Enable time (of a three-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{SU} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

VIH High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

VOH High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

VOL Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} Positive-going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-} .

V_T — Negative-going threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{\rm T}$ +.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

= transition from low to high level

→ = value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)

Z = off (high-impedance) state of a 3-state-output

a..h = the level of steady-state inputs at inputs A through H respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 \overline{Q}_0 = complement of Q_0 or level of \overline{Q} before the indicated steady-state input conditions were established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or \uparrow

□ = one low-level pulse

TOGGLE = each output changes to the complement of its previous level on each active transition indicated by \downarrow or \uparrow .

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, \Box or \Box , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)



Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

	INPUTS								OUT	PUTS			
CLEAD	MO	DE	CLOCK	SE	RIAL	P	ARA	LLE	L	٥.	Λ-	^-	^-
CLEAR	S1	SO	CLOCK	LEFT	RIGHT	Α	В	С	D	QA	QB	QC	QD
L	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
Н	Х	Х	L	Х	Х	Х	Х	Χ	Х	Q _{A0}	Q _{B0}	Q_{C0}	Q_{D0}
н	Н	Н	1	х	X	а	b	С	d	а	b	С	ď
н	L	Н	1	х	н	Х	Х	Χ	Х	Н	QAn	Q_{Bn}	QCn
н	L	Н	1	×	L	Х	Χ	Χ	Χ	L	Q_{An}	Q_{Bn}	QCn
н	н	L	1	н	X	Х	Х	Χ	Χ	QBn	QCn	Q_{Dn}	Н
н	н	L	. 1	L	X	Х	Х	Χ	Х	QBn	QCn	Q_{Dn}	L
н	L	L	×	×	Х	Х	Х	Х	Х	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output QA, data entered at B will be at QB, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B , the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is not at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

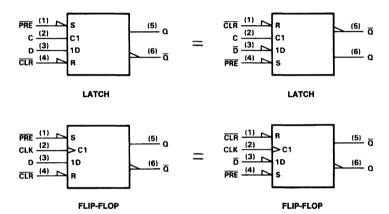
The function table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called \overline{Q} and those producing complementary data are called \overline{Q} . An input that causes a \overline{Q} output to go high or a \overline{Q} output to go low is called Preset (PRE). An input that causes a \overline{Q} output to go high or a \overline{Q} output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parentheses.



The figures show that when Q and \overline{Q} exchange names, the Preset and Clear pins also exchange names. The polarity indicators (\blacktriangleright) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_{.I} = R_{\theta.IA} \times P_T + T_A \tag{1}$$

where

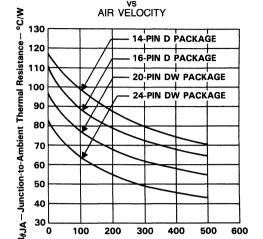
T.i virtual junction temperature

 $R_{\theta,1A}$ = thermal resistance, junction to free air

total power dissipation of the device

ТΔ free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.



JUNCTION-TO-AMBIENT THERMAL RESISTANCE

FIGURE 1

300

Air Velocity - Feet/Min

400

500

600

$$P_{T} = V_{CC} \times I_{CC} + (C_{pd} \times V_{CC}^{2} \times f_{i}) + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o})$$
(2)

30

100

$$P_{T} = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + (C_{pd} \times V_{CC}^{2} \times f_{i}) + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o})$$
(3)

where

V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) see Note 1

ICC = quiescent supply current (specified on device data sheet)

C_{nd} = Power dissipation capacitance (from the device data sheet)

fi = input frequency

C_I = output load capacitance

f₀ = output frequency

N = number of inputs driven by a TTL device

dc = duty cycle

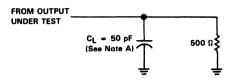
 ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than V_{CC} – 1 V for V_{IH} and input rise and fall times less than 15 ns.

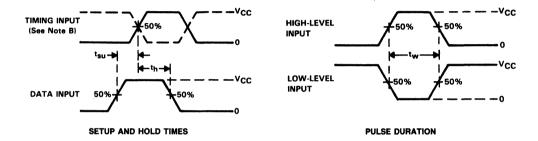
EPIC is a trademark of Texas Instruments Incorporated.

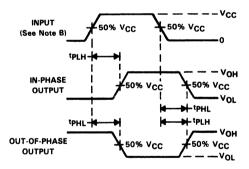


SERIES 54AC11XXX AND 74AC11XXX DEVICES SERIES 54AC16XXX AND 74AC16XXX DEVICES



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



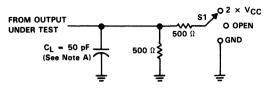


PROPAGATION DELAY TIMES

NOTES: A. CL includes probe and jig capacitance.

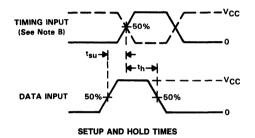
- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f = 3~ns$, $t_f = 3~ns$. For testing pulse duration: $t_f = 1$ to 3 ns, $t_f = 1$ to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low. C. The outputs are measured one at a time with one input transition per measurement.

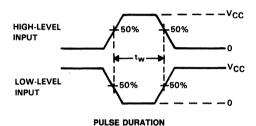
SERIES 54AC11XXX AND 74AC11XXX DEVICES SERIES 54AC11XXX AND 74AC11XXX DEVICES

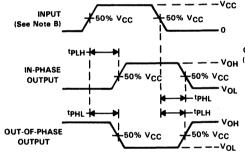


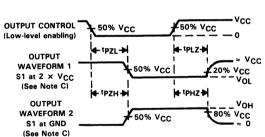
TEST	S1
tPLH/tPHL	OPEN
tPLZ/tPZL	2 × V _{CC}
tPHZ/tPZH	GND

LOAD CIRCUIT FOR THREE-STATE OUTPUTS









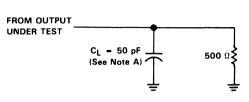
PROPAGATION DELAY TIMES

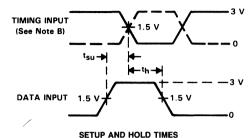
ENABLE AND DISABLE TIMES

NOTES: A. Cl includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 3$ ns, $t_f = 3$ ns. For testing pulse duration: $t_f = 1$ to 3 ns, $t_f = 1$ to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

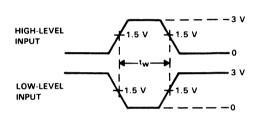
SERIES 54ACT11XXX AND 74ACT11XXX DEVICES SERIES 54ACT16XXX AND 74ACT16XXX DEVICES

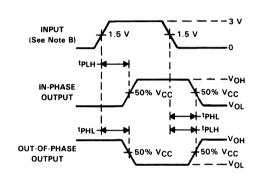




LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS







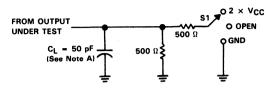
PULSE DURATION

PROPAGATION DELAY TIMES

NOTES: A. C. includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$. For testing pulse duration: $t_f = 1 \ to 3 \ ns$, $t_f = 1 \ to 3 \ ns$. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
- C. The outputs are measured one at a time with one input transition per measurement.

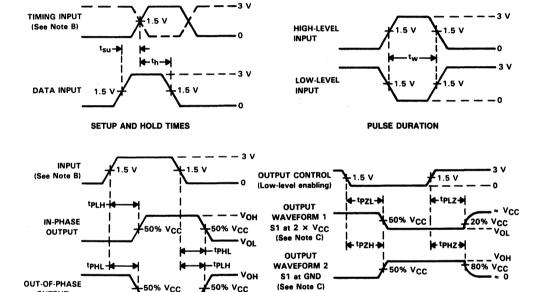
SERIES 54ACT11XXX AND 74ACT11XXX DEVICES SERIES 54ACT16XXX AND 74ACT16XXX DEVICES



TEST	S1
tplH/tpHL	OPEN
tPLZ/tPZL	2 × VCC
tPHZ/tPZH	GND

ENABLE AND DISABLE TIMES

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



NOTES: A. C. includes probe and jig capacitance.

PROPAGATION DELAY TIMES

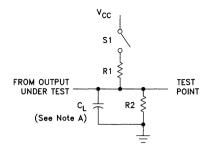
- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 3$ ns, $t_f = 3$ ns. For testing pulse duration: $t_f = 1$ to 3 ns, $t_f = 1$ to 3 ns. Pulse polarity may be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

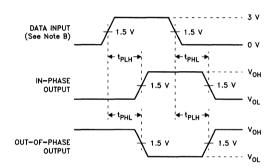
--Val

OUTPUT

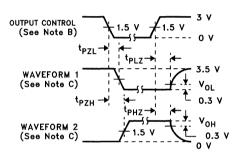
SERIES SN54BCT25XXX AND SN74BCT25XXX DEVICES



LOAD CIRCUIT



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



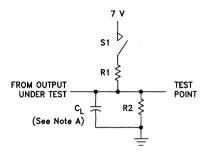
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

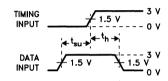
- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$. For testing pulse duration: $t_f = 1 \text{ to } 3 \text{ ns}$, $t_f = 1 \text{ to } 3 \text{ ns}$. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

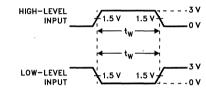
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN54BCT8XXX AND SN74BCT8XXX DEVICES

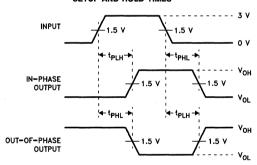


LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

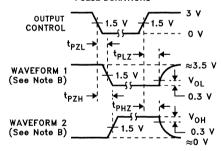




VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



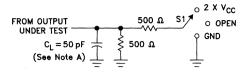
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

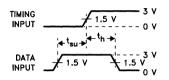
NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0=50~\Omega$, $t_f\leq$ 2.5 ns, $t_f\leq$ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

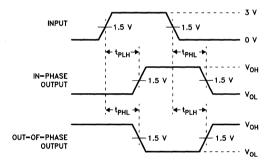
SERIES SN54ACT8XXX AND SN74ACT8XXX DEVICES



LOAD CIRCUIT



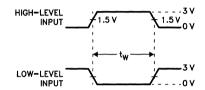
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



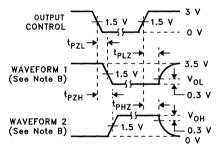
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

SWITCH POSITION TABLE

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 x V _{CC}
tPHZ/tPZH	GND



VOLTAGE WAVEFORMS PULSE DURATIONS

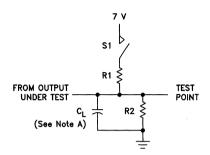


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

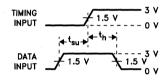
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z $_{O}$ = 50 $\Omega,$ tr $_{f}$ = 3 ns, tf $_{f}$ = 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN64BCT8XXX DEVICES

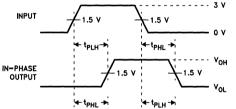


LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

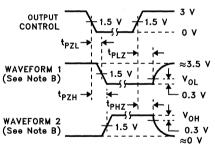


LOW-LEVEL 1.5 V 1.

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. CL includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

VOH

VOL

D. The outputs are measured one at a time with one input transition per measurement.

OUT-OF-PHASE

OUTPUT

SERIES SN54FXXX AND SN74FXXX DEVICES

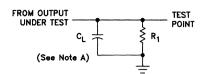


FIGURE 1. LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

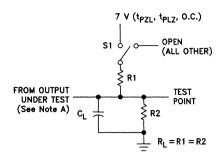
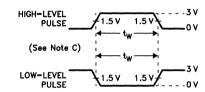


FIGURE 2. LOAD CIRCUIT FOR THREE STATE AND OPEN-COLLECTOR OUTPUTS



A. SETUP AND HOLD TIMES

1.5

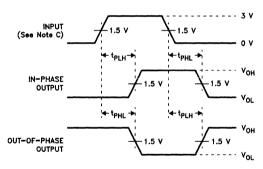
nν

TIMING

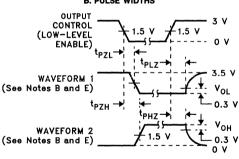
INPUT

DATA

INPUT



B. PULSE WIDTHS



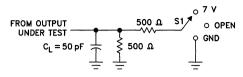
C. PROPAGATION DELAY TIMES

D. THREE-STATE OUTPUT ENABLE TIMES

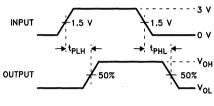
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics; PRR = 1 MHz, $t_f=t_f\leq 2.5$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of three-state outputs, switch S1 is open.
- E. The outputs are measured one at a time with one input transition per measurement.

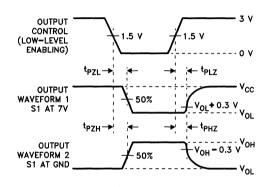
SERIES SN54BCTXXX AND SN74BCTXXX DEVICES



LOAD CIRCUIT FOR OUTPUTS

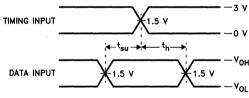


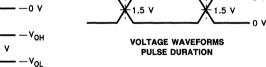
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- 3 V

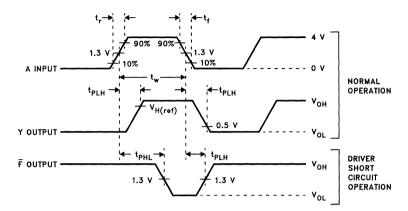




VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

- NOTES: A. CL includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O=50~\Omega$, $t_f=2.5~ns$, $t_f=2.5~ns$.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN55ALSXXX AND SN75ALSXXX DEVICES

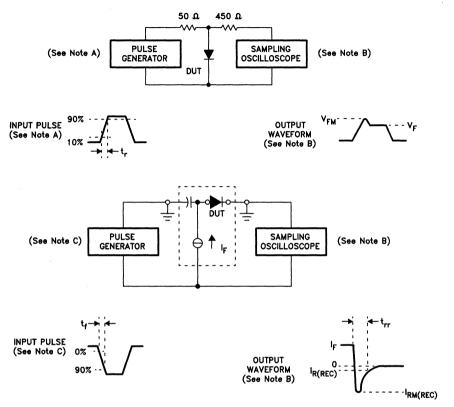


NOTE: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_{\text{f}} \le 6$ ns, $t_{\text{f}} \ge 6$ ns, $t_{\text{f}} \le 6$ ns, $t_{\text{f}} \ge 6$ ns, t_{f



NOTE: A. CL includes probe and stray capacitance.

SERIES SN54S10XX AND SN74S10XX DEVICES

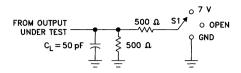


NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_{OUt} = 50 \Omega$, $f_{PR} = 500$ Hz, duty cycle = 0.01.

B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \le 350$ ps, $R_{in} = 50 \Omega$, $C_{in} = \le 5$ pF.

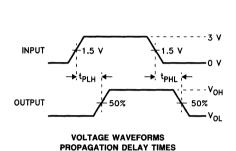
C. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_{out} = 50 Ω, t_w = ≤ 50 ns, duty cylce ≤ 0.01.

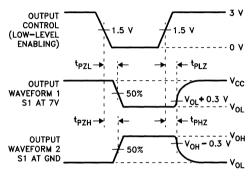
SERIES SN54ABTXXX AND SN74ABTXXX DEVICES



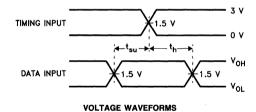
TEST	S1
tPLH/tPHL	OPEN
tPLZ/tPZL	7 V
tPHZ/tPZH	GND

LOAD CIRCUIT FOR OUTPUTS

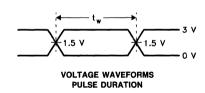




VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



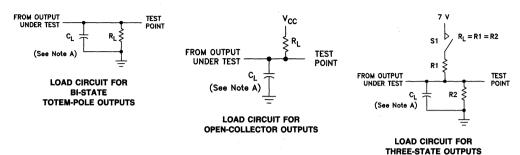
SETUP AND HOLD TIMES



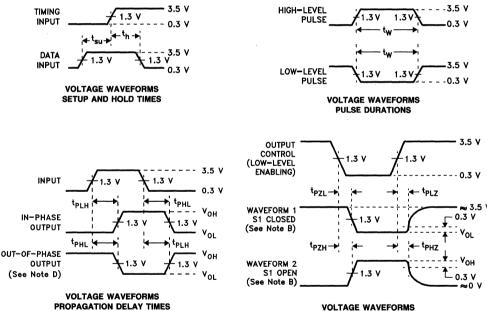
NOTES: A. C_L includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O=50~\Omega$, $t_f=2.5~ns$, $t_f=2.5~ns$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

SERIES SN54ASXXX AND SN74ASXXX DEVICES



NOTE: A. C₁ includes probe and jig capacitance.



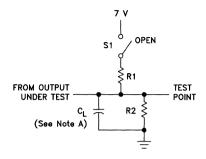
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses have the following characteristics: PRR \leq 1 MHz, $t_{\Gamma} = t_{\Gamma} = 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- E. The outputs are measured one at a time with one input transition per measurement.

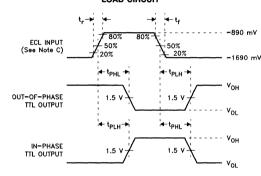
SERIES SN10KHT ECL-TO-TTL TRANSLATOR



SWITCH POSITION TABLE

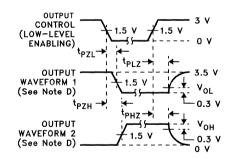
TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed

LOAD CIRCUIT

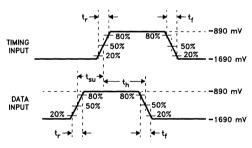


HIGH-LEVEL 50% -890 mV -1690 mV LOW-LEVEL 50% 50% -890 mV -1690 mV

VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS TTL ENABLE AND DISABLE TIMES

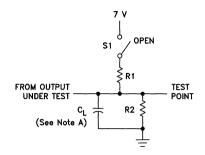
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

NOTES: A. CL includes probe and jig capacitance.

- B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 1.5 ns, $t_f \leq$ 1.5 ns.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. The outputs are measured one at a time with one transition per measurement.



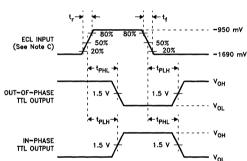
SERIES SN100KT ECL-TO-TTL TRANSLATOR

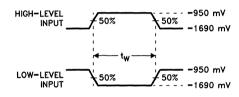


SWITCH POSITION TABLE

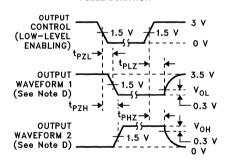
TEST	\$1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
t _{PHZ}	Open
tPLZ	Closed

LOAD CIRCUIT

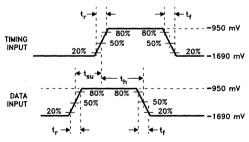




VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

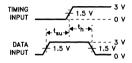
- NOTES: A. CL includes probe and jig capacitance.
 - B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$ tf $\leq 2.5 \text{ ns.}$
 - C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 0.7 ns, $t_f \leq$ 0.7 ns.
 - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. The outputs are measured one at a time with one transition per measurement.

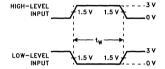


SERIES SN100KT TTL-TO-ECL TRANSLATOR



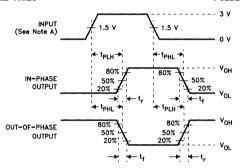
OUTPUT LOAD CIRCUIT



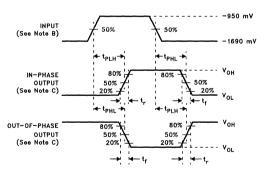


SETUP AND HOLD TIMES

PULSE DURATION



TTL-INPUT PROPAGATION DELAY TIMES



ECL-INPUT PROPAGATION DELAY TIMES

NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

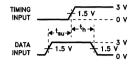
- B. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq 0.7$ ns, $t_f \leq 0.7$ ns.
- C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by OE.
- D. The outputs are measured one at a time with one input transition per measurement.

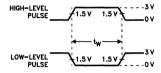


SERIES SN10KHT OCTAL TTL-TO-ECL TRANSLATOR



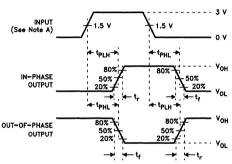
OUTPUT LOAD CIRCUIT



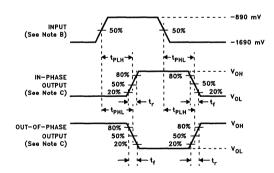


SETUP AND HOLD TIMES

PULSE DURATION



TTL-INPUT PROPAGATION DELAY TIMES



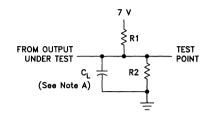
ECL-INPUT PROPAGATION DELAY TIMES

NOTES: A. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.

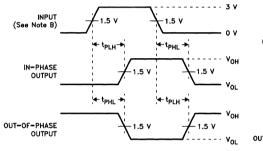
- B. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_{\Gamma} \leq$ 1.5 ns, $t_{f} \leq$ 1.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by OE.
- D. The outputs are measured one at a time with one input transition per measurement.

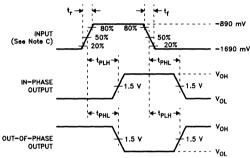


SERIES SN10KHT ECL-TO-TTL TRANSLATORS WITH OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT





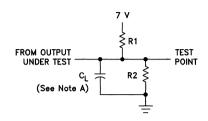
TTL-INPUT PROPAGATION DELAY TIMES

ECL-INPUT PROPAGATION DELAY TIMES

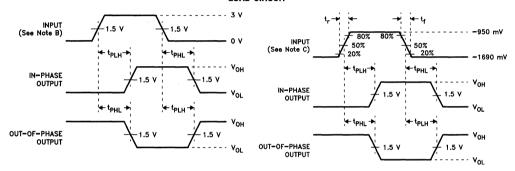
NOTES: A. C_L includes probe and jig capacitance.

- B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq 2.5 \text{ ns. } t_f \leq 2.5 \text{ ns.$
- C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f \leq$ 1.5 ns, $t_f \leq$ 1.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

SERIES SN10KT ECL-TO-TTL TRANSLATORS WITH OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT



VOLTAGE WAVEFORMS TTL-INPUT PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ECL-INPUT PROPAGATION DELAY TIMES

NOTES: A. CL includes probe and jig capacitance.

- B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
- C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_{f} \leq$ 0.7 ns, $t_{f} \leq$ 0.7 ns.
- D. The outputs are measured one at a time with one transition per measurement.

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type, and list all options available or planned of that function. The technology columns identify the appropriate family and identify a particular data book, where more information can be found. The applicable literature number, composed of either seven or eight digits, can be found on the back cover at the lower right-hand corner of each publication.

List of Applicable Data Books:

AC and ACT Devices	Advanced CMOS Logic Data Book	SCAD001B
Advanced Logic	Advanced Logic and Bus	SCYD001
Devices	Interface Logic Data Book	
AS and ALS Devices	ALS/AS Logic Data Book	SDAD001B
BCT Devices	BiCMOS Bus Interface Logic Data Book	SCBD001A
F Devices	F Logic (54/75F) Data Book	SDFD001A
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
Std TTL, LS, and S Devices	Standard TTL Logic Data Book	SDLD001A

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GATES

Positive-NAND Gates

DECODIDETON							TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-Input		′30	•	•	•	•					
		11030						•	•		
13-Input		′133	•			•					
Dual 2-Input		'8003	•								
Dual 4-Input		′11013					•		A		
		′20	•	•	•	•					
		′40	•		•						
		′1020	•								
		′11020			 			•	•		
Triple 3-Input		′10	•	•	•	•					
		′1010	•								
		′11010						•	•		
Quad 2-Input		′00	•	•	•	•	•				
		′11000						•	•		
		'37	•		•				<u> </u>		
	oc	'38	•		•				<u> </u>		
		′132				•					
		111132						A	A		
		′1000	•	•							
Hex 2-Input		'804	•	•							
		′1804	•	•							
Dual 4-Input	ОС	'22	•								
Triple 3-Input	ОС	′12	•								
Quad 2-Input	oc	′01	•			•					
	ОС	′03	•		1	•					
	ОС	′1003	•								

- Product available in technology indicated
 New Product planned in technology indicated

GATES (continued)

Positive-AND Gates

DECODIDATION	OUTDUT	TVDE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Triple 3-Input	ОС	′15	•								
Quad 2-Input	ОС	′09	•		•	•					
		′7001				•					
Dual 4-Input		′21	•	•	•	•					
		′11021						•	•		
Triple 3-Input		'11	•	•	•	•					
		′11011						•	•		
Quad 2-Input		′08	•	•	•	•	•				
		′1008	•	•							
		′11008						•	•		
Hex 2-Input		′808	•	•		•					
		′1808	•	•							

Positive-OR/NOR Gates

DECODINE							TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Triple 3-Input		'4075				•					
Quad 2-Input		′32	•	•	•	•	•				
		′1032	•	•							
		′11032				1		•	•		
Quad 2-Input		′7032				•					
Hex 2-Input		′832	•	•		•					
		′1832	•	•							
Dual 4-Input		'4002				•					
Dual 5-Input		′260			•						
Triple 3-Input		'27	•	•	•	•					
		′11027						•	•		
Quad 2-Input		′02	•	•	•	•	•				
		′28	•								
	ОС	′33	•								
		′36			•	•					
		′1002	•								
		′1036		•	İ						
		′7002				•					
		′11002						•	•		
Hex 2-Input		′805	•	•		•					
		′1805	•	•							

- Product available in technology indicated
- ▲ New Product planned in technology indicated

GATES (continued)

OR/NOR Gates

DUCCELLEGA							TECHNO	LOGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-Input		′4078				•					
Quad 2-Input		′86	•	•	•	•					
Exclusive OR Gates with		′11086						•	•		
Toten-Pole Outputs		′386				•			1		
Quad 2-Input	ОС	′136	•	•							
Exclusive OR Gates											
Quad 2-Input		′810	•	•							
Exclusive-NOR Gates		′7266				•					
Quad 2-Input	OC	'811	•	•							
Exclusive-NOR Gates											

AND-NOR Gates

DESCRIPTION	OUTDUT	TVDE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Wide 4-2-3-2		′64			•						
Input		′11064						A	A		
Dual 2-Wide		′51			•	•					
2-Input, 3-Input		′11051						A	A		

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

							TECI	HNOLOGY	,			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	HCU	AC	ACT	BCT	ABT
Hex Inverters		′04	•	•	•	•	•	•				
		11004							•	•		
	ОС	′05	•			•						
		′14				•						
		′11014							A	A		
		′1004	•	•								
		′1005	•									
Hex Noninverters		′34	•	•								
		′11034							•	•		
	ОС	′35	•									
		′1034	•	•								
	ОС	′1035	•							İ		

- Product available in technology indicated
 New Product planned in technology indicated



BUFFER/DRIVERS AND BUS TRANSCEIVERS

Drivers

ALS AS F HC HCT AC ACT BCT AB	DESCRIPTION	OUTPUT	TYPE				·	TECHNOL				
Drivers 3S			i	ALS	AS			HCT	AC	ACT	BCT	ABT
Noninverting Hex 3S '365			L									
Buffers/Drivers 3S '386			L			•					•	
Inverting Hex 3S	•		L									
Buffers/Drivers 3S '368												
Noninverting Octal Buffers/Drivers	-											
11241												
25241	-	38		•	•	•	•	•			•	^
1/1244									•	•		
11244	Buffers/Drivers										A	
1/244 0				•	•	•	•	•			•	A
Part									•	•		
1465				•								
1											A	
Inverting Octal Buffers/Drivers				•								
1				•		•	•	•			•	A
Inverting Octal 3S '240 • • • • • • • • • • • • • • • • • •		ОС		•	•						•	
Inverting Octal Buffers/Drivers Sample S			′760	•	•						•	
11240			′25760								A	
1240	Inverting Octal	38	′240	•	•	•	•	•			•	A
1/25240	Buffers/Drivers		′11240						•	•		
1466			′1240	•								
1540			'25240		1						A	
OC '756 • • •			′466	•								
1763 • • •		İ	′540	•	İ	•	•	•			•	A
Inverting and 3S '230 •		ОС	′756	•	•		<u> </u>				A	
Noninverting Octal Buffers/Drivers OC 7762			′763	•	•		<u> </u>					
Buffers/Drivers S	Inverting and	38	′230		•							
Noninverting 10-Bit 3S	Noninverting Octal	ОС	′762		•							
Duffers/Drivers 19827												
Duffers/Drivers 19827	Noninverting 10-Bit	38	′11827	1					•	•		
Inverting 10-Bit 3S			'29827	•	<u> </u>				 		•	A
Duffers/Drivers 129828		38	111828						•	•		ļ
Noninverting 16-bit 3S	-			•							•	ļ
Buffers/Drivers		38			t		 	 	A	•		†
Inverting 16-bit 3S							1					
Buffers/Drivers		38	16240	<u> </u>	-		i		A			
Noninverting 18-bit 3S	-											
Buffers/Drivers		38	16825				-	 	_	_	<u> </u>	
Inverting 18-bit 3S	-									1		
Buffers/Drivers		35	16826	+	 	 	 	 	A	_	 	+
Noninverting 20-bit 3S '16827 A A Buffers/Drivers	•											
Buffers/Drivers		38	16827	-	 	 	 	1	A	A	1	-
	-		10027									
mivorang 20-bit 00 10020 = =		26	116929	+	-	-		1	_	_	-	
Buffers/Drivers	-	33	10020						-	_		

- Product available in technology indicated
 New Product planned in technology indicated



BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Drivers (continued)

DECODIDEION	OUTPUT	TYPE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	НС	HCT	AC	ACT	BCT	ABT
Octal Buffers/		′746	•								
Drivers with Input		′747	•								
Pull-up Resistors			1		1			1			

Bus Transceivers

							TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Noninverting Quad	ос	′759		•							
Transceivers	38	′243	•	•	•		•				
Inverting Quad	ОС	′758	•								
Transceivers	38	'242	•	•	•		•				
Noninverting	38	′245	•	•	•	•	•			•	A
Octal Transceivers		′1245	•								
		111245						•	•		
		'25245								•	
	oc	'621	•		•						
	38	'623	•	•	•	•	•			•	•
		′11623						•	•		
	OC/3S	'639	•	•							
	ОС	'641	•	•							
	38	'645	•	•		•	•				
	38	′1640	•								
		′1645	•	i							
Inverting	35	'620	•	•	•					•	•
Octal		′11620						•	•		
Transceivers		′25620								A	
	ос	'622	•		•						
	OC/3S	′638	•	•							
	38	'640	•	•		•	•			•	A
		′11640						•	•		
		′25640			·					A	
	OC	'642	•	•			<u> </u>			A	
		′25642								•	
True and	38	'643	•	•	····		•				
Inverting Octal		′11643						•	•		
Transceivers	ОС	′644		•	1						
Noninverting 9-Bit	38	′11863						A	A		
Transceivers		'29863	•		 					•	
Inverting 9-Bit	38	′11864						A	A		
Transceivers		'29864	•		-					•	
Noninverting 10-Bit	38	′11861						A	A		
Transceivers		′29861	•		 					•	
Inverting 10-Bit	38	′11862						A	A		
Transceivers		'29862	•							•	<u> </u>
Noninverting 16-Bit	38	′16245	 					•	•		
Transceivers		16623	 				 	A	A	 	

- Product available in technology indicated
 New Product planned in technology indicated



BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE					TECHNOL	.OGY			
			ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Inverting 16-Bit	38	′16640						A	•		
Transceivers		′16620						•	A		
Noninverting 18-Bit	38	′16863						A	A		
Transceivers											
Inverting 18-Bit	38	′16864						A	•		
Transceivers											
Noninverting 20-Bit	38	′16861						^	A		
Transceivers											
Inverting 20-Bit	38	′16862		1				A	A	1	l
Transceivers											
Noninverting	38	′543			A					•	A
Octal Registered		′11543						A	A		
Transceivers		′646	•	•		•	•			•	A
	:	′11646						•	•		
		′25646								A	
	ОС	′647	•								
	38	′652	•	•		•	•			•	•
		′11652						•	•		
		′25652								A	
	OC/3S	′653	•								
		′654	•								
	3S	′2952								A	A
Inverting Octal	38	′544			A					•	A
Registered		′11544						A	A		
Transceivers	1	′648	•	•		•	•			A	•
		′11648						•	•		
		′651	•	•		•	•			A	A
		111651						A	A		
		'2953								A	A
Noninverting	38	′16470						A	A		
16-Bit Registered		′16543						A	•		
Transceivers		′16646						A	•		
		′16652			T			A	•		
		16952						_	A		
Inverting	38	′16471						A	A		
16-Bit Registered		16544			 			A	•		
Transceivers		16648			1			A	A		
		16651			T			A	A	1	
		16953						A	_		
Noninverting	38	16472			 	 	†	A	A	 	T
18-Bit Registered		16474		l	 	 	 		A	 	†
Transceivers											
Inverting	38	′16473	 	<u> </u>	†	!	 	A	A	 	<u> </u>
18-Bit Registered		16475	†	<u> </u>	 	t		_	A	 	
Transceivers		1	1		1	1	1				1

- Product available in technology indicated
 New Product planned in technology indicated



BUFFER/DRIVERS AND BUS TRANSCEIVERS (continued)

Bus Transceivers (continued)

DECODIDEION	OUTDUT	TVDE					TECHNOL	OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
8-/9-Bit Bus	3S	'657			A					A	A
Transceivers		′11657						A	A		
with Parity		′658				•	•				
Checker/		'659				•	•				
Generator		′664					•				
		'665					•				
	3S/OC	′11833						A	A		
		′29833	•							•	
		′11834						A	A		
		′29834								•	
		111853						A	A		
		'29853	•							•	
		′11854						A	A		
		′29854	•							•	
Universal	38	'11852						A	A		
Transceivers/		′856		•							
Port Controllers		′877		•							

MOS Memory Drivers/Transceivers

DECODINE	01170117		I				TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal	38	'2623		•							
Transceivers		′2640		•							
w/ Series		′2645		•							
Resistors on											
Output											
Octal Buffers/	38	′2240	•							•	
Drivers w/		′2241								•	
Series Resistors		′2244	•							•	
on Output		′2540	•								
		′2541	•								
Octal	38	′2245								A	
Bidirectional											
Transceiver w/											
Series Resistors	ļ	1			1						
on A-port											
Octal Latch w/	38	′2574								A	
Series Resistors											
on Output				Į	ĺ						
10-Bit Buffers/	38	′2827								•	
Drivers w/		′2828								•	
Series Resistors	ĺ								1		
11-Bit Buffers/	38	′2410								A	
Drivers w/		′2411	Ĭ							A	
Series Resistors											

- Product available in technology indicated
- ▲ New Product planned in technology indicated



TESTABILITY BUS INTERFACE CIRCUITS

SCOPE™ Testability Circuits (3-State Output)

						TECHNOL	OGY			
OUIPUI	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
38	'8244								•	
38	'8245								•	
38	'8373								•	
									l	
3S	'8374								•	
	3S 3S	3S '8244 3S '8245 3S '8373	3S '8244 3S '8245 3S '8373	3S '8244	3S '8244 S F S S S S S S S S S S S S S S S S S	OUTPUT TYPE ALS AS F HC 3S '8244 3S '8245 3S '8373	OUTPUT TYPE ALS AS F HC HCT 3S '8244 3S '8245 3S '8373	3S '8244	OUTPUT TYPE ALS AS F HC HCT AC ACT 3S '8244 3S '8245 3S '8373	OUTPUT TYPE ALS AS F HC HCT AC ACT BCT 3S '8244 - - - - - - 3S '8245 - - - - - - - 3S '8373 -

FLIP-FLOPS/LATCHES

Flip-Flops

DECODIDEION	QUEDUT	TVDE					TECHNOL	OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Dual J-K Edge		′73				•					
Triggered		′76				•					
		′107				•					
		′109	•	•	•	•					
		′11109						•	•		
		′112	•		•	•					
		′11112						•	•		
		′113	•		•	•					
		′114	•		•						
Dual D-Type		′74	•	•	•	•	•				
		′11074						•	•		
Dual D-Type		′7074				•					
with 2-Input		′7075				•					
NAND/NOR Gates		′7076				•					
Dual 4-Bit		′874	•	•							
D-Type		′11874					1	•	•		
Edge-Triggered		′876	•	•							
	3S	′878	•	•							
		′879	•	•							
Quad D-Type		′173				•					
		′175	•	•	•	•					
		′11175						•	•		
		′379			•	•					
		′11379						•	A		
Hex D-Type		′174	•	•	A	•					
		′11174						A	A		
		′378	1		A	•					
		′11378	1					A	A		
Octal D-Type	3-S	′374	•	•	•	•	•			•	A
True Data		′11374						•	•		
		′574	•	•	A	•	•			A	A

- Product available in technology indicated
 New Product planned in technology indicated



FLIP-FLOPS/LATCHES (continued)

Flip-Flops (continued)

DESCRIPTION	OUTPUT	TYPE					TECHNOL				
	001101		ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal D-Type True		′273	•		A	•	•				
Data with Clear		′11273						A	A		
	3-S	'575	•	•							
	İ	′874	•	•							
		′878	•	•							
Octal D-Type True		′377			•	•	•				A
Data with Enable		′11377						•	•		
Octal D-Type	3-S	′534	•	•	•	•	•			•	A
Inverting		′11534						•	•		
		′564	•		•	•	•			A	
		′576	•	•			1		<u> </u>		
		′826		•							
		′11826						A	A		
		′29826	•							A	
Octal Dual Ranked	3-S	′4374		•							
True Data		′11478						•	A		
Octal Inverting	3-S	′577	•	•							
with Clear		′879	•	•							
Octal Inverting	3-S	'876	•	•							
with Preset											
Octal True	3-S	'825		•							
Data		11825						A	A		
		'29825	A	1				1		A	
9-Bit True	3-S	′823		•			· · · · · · · · · · · · · · · · · · ·				A
Data		′11823				1		A	A		
		′29823	•							•	
9-Bit	3-S	′824		•					1		
Inverting	j	′11824				·		A	A		
ŭ		′29824	•	1						A	
10-Bit True	3-S	'821		•							A
Data		′11821		1		1		A	A		
		′29821	•	†				†	<u> </u>	•	
10-Bit	3-S	'822		•				<u> </u>			
Inverting		′11822		 		<u> </u>	 	•	•		
8-Bit Diagnostic		′29818	•	 	-	†			 		
Pipeline Register						1		1	1		
16-Bit	3-S	′16374		 	-			A	•	 	
Noninverting			1			-		1	1		
16-Bit Inverting	3-S	′16534	 	 		†		A	A	 	
18-Bit	3-S	16823	+	 	 	 	-	A	A	 	-
Noninverting		1.0020									
18-Bit Inverting	3-S	′16824	 	 		 	 	_	_		
20-Bit	3-S	16821	+	 		 	 	_		 	
Noninverting	""	10021							1		
20-Bit Inverting	3-S	′16822	+	 		 	 	_	_	 	
EO-DIL IIIVOLUNG	J-0	10022	1	1	I	1	ł		1 -	1	i

Product available in technology indicated
 New Product planned in technology indicated



FLIP-FLOPS/LATCHES (continued)

Latches

DE0001071011	NO. OF							TECHNOL	.OGY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Bistable	4-Bit		′75				•					
			′375				•					
D-Type Edge-Triggered Inverting and Noninverting	Octal		′996	•								
D-Type Transparent Readback Latch True	Octal	38	′990	•								
	9-Bit	38	'992	•								
	10-Bit	3S	′994	•								
D-Type Transparent Readback Latch Inverting	Octal	3S	′991	•								
	9-Bit	38	'993	•								
D-Type Transparent with Clear True Outputs	Octal	38	′666	•								
D-Type Transparent with Clear Inverting Outputs	Octal		'667	•								
D-Type	Octal	3-S	′373	•	•	•	•	•			•	A
Transparent		1	′11373						•	•		
True			′573	•	•	•	•	•			A	A
	16-Bit	38	′16373						A	•		
D-Type	Octal	3-S	′873	•	•			l				
Dual 4-Bit Transparent True			′11873						•	•		

- Product available in technology indicated
 New Product planned in technology indicated

FLIP-FLOPS/LATCHES (continued)

Latches (continued)

DESCRIPTION	NO. OF	OUTDUT	TVDE					TECHNO	OGY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
D-Type	Octal	3-S	′533	•	•	•	•				A	
Transparent			111533						•	•		
Inverting			′563	•		•	•	•			A	
			′580	•	•							
	16-Bit	38	′16533						A	A		
Dual 4-Bit	Octal	3-S	'880	•	•							
Transparent												
Inverting				ļ						İ		
2-Input	Octal	3-S	′604				•					
Multiplexed												
Addressable	Octal	2-S	′259	•			•					
		Q	'4724				•					
D-Type	10-Bit	3-S	′841	•	•							A
True		•	′11841						A	A		
Inputs			′29841	•							A	
	9-Bit	3-S	'843	•	•		<u> </u>					A
			′11843						A	A		
			'29843	•							•	
	Octal	3-S	'845	•	•							A
			′11845						A	A		
			′29845	•							A	
	18-Bit	3S	′16843						A	A		-
	20-Bit	38	′16841						A	A		
D-Type	10-Bit	3-S	'842	•	•							
Inverting			′11842						A	A		
Inputs		1	'29842	•							A	
	9-Bit	3-S	′844	•	•							
		1	′11844						A	A		
			'29844	•							Δ	
	Octal	3-S	'846	•		T						
			′11846			l	1		_	A		1
			′29846	•	 -	†					•	†
	18-Bit	38	′16844						A	A		
	20-Bit	38	′16842				1		A	A		t

- Product available in technology indicated
 New Product planned in technology indicated

REGISTERS

Shift Registers

DECODINE	NO. OF							TECHNO	LOGY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ	ABT
Parallel-In	4		′194		•		•					
Parallel-Out			′11194						•	A		
Bidirection	8		′198									
		1	′299	•		•	•				A	
]	′11299						A	A		
		1	′323	•		•					A	
•			′11323						A	A		
Parallel-In	4		′195		•		•					
Parallel-Out			1									
Serial-In	8		′164	•			•					
Parallel-Out						ł						
Parallel-In	8		′165	•			•					
Serial-Out			′166	•			•					
Serial-In	8	3-S	′594			†	•		1			
Parallel-Out		1	′595				•					
with Output						1					-	
Latches												

Register Files

DECODIDEION	OUTDUT	TVDE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 16 Word x	3-S	'870	•	•							
4 Bits		11870						A	A		
		′871		•							

- Product available in technology indicated
 ▲ New Product planned in technology indicated

COUNTERS

Synchronous Counters—Positive-Edge Triggered

DECODIDATIO:	PARALLEL	TVDE				TECH	INOLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	HC	HCT	AC	ACT	ВСТ
4-Bit	Sync	′160	•	•	•	•				
Decade		′11160						•	A	
		′162	•	•	•					
		′11162						•	A	
		'560	•							
4-Bit	Sync	′168	•		•					
Decade Up/		′11168						A	A	
Down	Async	′190	•		A	•				
		′11190						A	A	
		′192	•		A	•				
		′11192						A	A	
	Sync	'568	•		•					
	i	′11568						A	A	
4-Bit	Sync	′161	•	•	•	•				
Binary	ļ	′11161						A	A	
		′163	•	•	•	•				
		′11163						A	A	
		′561	•							
8-Bit	Sync	11579						A	A	
Binary										
4-Bit Binary	Async	'191	•		A	•				
Up/Down		′11191						A	A	
		′193	•		A	•				
		′11193						A	A	
	Sync	′169	•	•	•					
		′11169						A	A	
		′569	•		•					1
		′11569						A	A	1
		'8169	•							
8-Bit	Async CLR	'867	•	•						
Up/Down		′11867						A	A	
•	Sync CLR	′869	•	•						
		′11869						A	A	
Divide-by-10	Sync	′4017				•				
Counter	•									Į

- Product available in technology indicated
 New Product planned in technology indicated

COUNTERS (continued)

Asynchronous Counters (Ripple Clock)—Negative-Edge Triggered

DECODINE	PARALLEL					TECH	INOLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT
Dual 4-Bit Decade	None	′390				•				
	Set-to-9	′490				•				
Dual 4-Bit	None	′393				•				
Binary										
7-Bit	Sync	'4024				•				
Binary										
12-Bit	Sync	′4040				•				
Binary										
14-Bit	Sync	′4020				•				
Binary		′4060				•				
		′4061				•				

8-Bit Binary Counters with Registers

D=0001071011	PARALLEL					TECI	INOLOGY			
DESCRIPTION	LOAD	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT
Parallel	3-State	′590				•				
Register		′11590						A	A	
Outputs										
Parallel	2-State	′11592						A	A	
Register			1							
Inputs						1				
Parallel I/O	3-State	′11593						A	A	

- · Product available in technology indicated
- ▲ New Product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT		ALS	AS	F	HC	HCT	AC	ACT	BCT	ABI
Quad 2-to-1		′157	•	•	•	•					
		′11157						A	A		
		′158	•	•	•	•					
		′11158						•	A		
		′298		•		•					
	3-S	'257	•	•	•	•					
		111257						•	•		
		′258	•	•	•	•					
		′11258						•	•		
Dual 4-to-1		′153	•	•	•	•					
		′11153						A	A		
	3-S	′253	•	•	•	•					
		′11253		-				•	•		
		′352	•	•	•	•					
		′11352						A	A		1
	3-S	'353	•	•	•	•					
	3-S	111353						•	•		
Hex 2-to-1	3-S	'857	•	•				-			
Universal											
Multiplexer		1				1					Ì
8-to-1		′151	•	•	•	•					
		′11151			 			•	•		
	3-S	′251	•		•	•					
		′11251						•	•		†
		′354				•		1			
16-to-1		′11150						_	A		†
	3-S	′250		•					<u> </u>		
		11250		 				A	_		
		'850		•	<u> </u>	 					
		′851		•	 						
Full BCD		′147			-	•					†
Cascadable		′148			 	•			 	-	†
Octal		1									

NOTES:

Product available in technology indicated

▲ New Product planned in technology indicated



DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS (continued)

Decoders/Demultiplexers

DECODINE	01170117						TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 2-to-4		′239				•					
		′11239						•	A		
		′139	•		A	•	•				
		′11139						•	A		
	1	′155	•								
	OC	′156	•								
3-to-8		′138	•	•	•	•	•				
	1	′11138						•	•		
3-to-8		'237				•	•				
		′238				•	•				
		′11238						•	•		
3-to-8 with		′131	•	•							
Address		′137	•	•		•	•				
Registers											
4-to-10		'42				•					
BCD-to-Decimal											İ
4-to-16		′154	•								
		′11154						A	A		
4-to-16 with		'4514				•					
Address Latches		'4515				•					
Dual 2-to-4 for		′2414								A	
Battery Backed-											
Up Memories		1		1							

NOTES:

- Product available in technology indicated
 New Product planned in technology indicated

Shifters

DESCRIPTION	OUTPUT	TVDE					TECHNOL	OGY			
DESCRIPTION	OUIPUI	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	3-S	′350			•						

COMPARATORS AND PARITY GENERATOR/CHECKERS

Comparators

			DESC	RIPTION	1			TVD5				TEC	HNOLO	GY		
INPUT	P = Q	P = Q	P>Q	P>Q	P <q< th=""><th>OUTPUT</th><th>ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>F</th><th>HC</th><th>HCT</th><th>AC</th><th>ACT</th><th>BCT</th></q<>	OUTPUT	ENABLE	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit/	Yes		Yes	No		2-S	No	'85				•				
8-Bit				ļ								1	1			ļ
20 kΩ	Yes	No	No	No	No	ОС	Yes	′518	•		•					
Pull-up	No	Yes	No	No	No	2-S	Yes	′520	•		•					
		}		1	1			′11520						•	•	
	No	Yes	No	No	No	ОС	Yes	'522	•							
	No	Yes	No	Yes	No	2-S	No	'682				•				
Standard	Yes	No	No	No	No	ОС	Yes	′519	•		•					
	No	Yes	No	No	No	2-S	Yes	′521	•		•					
		ĺ						′11521						•	•	
	No	Yes	No	Yes	No	2-S	No	′684				•				
	No	Yes	No	No	No	2-S	Yes	′688	•			•				
	No	Yes	No	No	No	OC	Yes	′689	•							
Latched P	No	No	Yes	No	Yes	2-S	Yes	'885		•						
Latched	Yes	No	Yes	No	Yes	L	Yes	'866		•						
P and Q			ļ		1											

COMPARATORS AND PARITY GENERATOR/CHECKERS

Address Comparators

DECODINE	OUTPUT	LATCHED					TECH	HNOLOGY			
DESCRIPTION	ENABLE	ENABLE	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT
16-Bit to 4-Bit	Yes		'677	•							
			′11677						A	A	
		Yes	′11678						A	A	
12-Bit to 4-Bit	Yes		'679	•			•				
		Yes	'680	•							

Parity Generators/Checkers

DESCRIPTION	NO. OF	OUTDUT	TVDE					TECHNO	LOGY			
DESCRIPTION	BITS	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Odd/Even	9		'280	•	•	•	•					
Generators/			111280						•	•		
Checkers			′286		•							
			′11286						•	•		

Fuse-Programmable Comparators

DECODIDETON	OUTDUT	TVDE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16-Bit Identity	,	′526	•								
Comparator						}					
12-Bit Identity		′528	•								
Comparator	l				Ì				,		
8-Bit Identity		'527	•								
Comparator and					ļ						
4-Bit Comparator				1	1				1	1	1

- Product available in technology indicated
 New Product planned in technology indicated

ARITHMETIC CIRCUITS AND FIFO MEMORIES

Parallel Binary Adders

1	DECORIDATION	OUTPUT	TYPE					TECHNOL	OGY			
1	DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
	4-Bit		′283			•	•					

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DECORPTION	CUTPUT	TVDE					TECHNOL	.OGY			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic		′181		•							
Logic Units:		′11181						•	•		
Function		′381			•						
Generators		′881		•							
		′11881						A	A		
4-Bit Arithmetic		′382			•						
Logic Unit With					l			1		ļ.	1
Ripple Carry							į			}	Í
Look Ahead 32-Bit		'882		•							
Carry		′11882						A	A		
Generators		1									

First-In First-Out Memories (FIFOs)

PERCEIPTION	CUITOUT						TEC	HNOLO	GY			
DESCRIPTION	OUTPUT	TYPE	LS	S	ALS	AS	F	HC	HCT	AC	ACT	ВСТ
16 Words x	3-S	′222	•									
4 Bits	3-S	′224	•									
	3-S	′232			•							
	OC	'227	•									
	OC	′228	•									
16 Words x	3-S	'225		•								
5 Bits	3-S	'229B			•							
	3-S	'233B			•							
64 Words x	3-S	′236			•							
4 Bits	3-S	′234			•							
64 Words x	3-S	′235			•							
5 Bits			1	ł		1		1			Ì	
64 Words x	3-S	'2232A	1		•							
8 Bits			1		ę	1			1		Ì	1
64 Words x	3-S	'2233A			•					1		
9 Bits				1	}	1	1	j		ì		
32 Words x	3-S	'2238			•							
9 Bits			1	1	1			1			}	
Bidirectional			1	ł	}	ĺ				ĺ		
1k Words x		′7801									•	
18 Bits		′7802									A	
1k Words x		'2235	T								A	
9 Bits	1		1	1	1			1		1	1	
Bidirectional	1				Í	1	1	1]

- Product available in technology indicated
- ▲ New Product planned in technology indicated



CLOCK DRIVER CIRCUITS

Clock Driver

DECODINE	TVDE				TEC	HNOLOGY			
DESCRIPTION	TYPE	ALS	AS	F	HC	HCT	AC	ACT	BCT
Hex Inverting Clock	′11204						•		
Drivers/Buffers									
Dual 1-to-4 Clock	′11208						•	•	
Drivers/Buffers	1							j	
Triple 4-Input AND/NAND	′11800						A	A	
Clock Drivers									
Triple 4-Input OR/NOR	′11802						A	A	
Clock Drivers				İ					
Octal Divide-by-2	′303		•						
Clock Drivers							1		
(6 Invert, 9 Noninvert)			ļ				}		
Octal Divide-by-2	′305		•						
Clock Drivers (8 Noninvert)			ŀ	ļ					
Octal Divide-by-2	′304		A						
Clock Drivers	1								1
(4 Invert, 4 Noninvert)			ļ						

NOTES:

- Product available in technology indicated
 New Product planned in technology indicated

ECL TRANSLATORS

ECL-to-TTL or TTL-to-ECL Translators

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE	AVAILABILITY
Octal Bus Driver	ECL-to-TTL	OC	10KHT5538	•
Inverting			100KT5538	•
		3S	10KHT5540	•
			100KT5540	•
	TTL-to-ECL	OE	10KHT5542	•
			100KT5542	•
Octal Bus Driver	ECL-to-TTL	OC	10KHT5539	•
Noninverting	rerting	1	100KT5539	•
		38	10KHT5541	•
		1	100KT5541	•
	TTL-to-ECL	OE	10KHT5543	•
			100KT5543	•
Octal Bus Transceiver	ECL-to-TTL	OE/3S	10KHT5563	A
Inverting	TTL-to-ECL		100KT5563	A
			10KHT5562	A
			100KT5562	A
Octal Bus Transceiver	ECL-to-TTL	OE/3S	10KHT5564	A
Noninverting	TTL-to-ECL		100KT5564	A
			10KHT5565	A
			100KT5565	A

ECL TRANSLATORS (continued)

ECL-to-TTL or TTL-to-ECL Translators (continued)

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE	AVAILABILITY
Octal D-Type Latch	ECL-to-TTL	38	10KHT5575	A
Inverting			100KT5575	A
	TTL-to-ECL	OE	10KHT5579	A
			100KT5579	A
Octal D-Type Latch	ECL-to-TTL	38	10KHT5573	A
True			100KT5573	A
	TTL-to-ECL	OE	10KHT5577	A
		į	100KT5577	A
Octal D-type Flip-Flop	ECL-to-TTL	38	10KHT5576	A
Inverting			100KT5576	A
	TTL-to-ECL	OE	10KHT5580	A
			100KT5580	A
Octal D-Type Flip-Flop	ECL-to-TTL	38	10KHT5574	•
True			100KT5574	•
	TTL-to-ECL	OE	10KHT5578	•
		1	100KT5578	•
Octal Registered	ECL-to-TTL	OE/3S	10KHT5591	A
Transceiver Inverting			100KT5591	A
		Ĺ	10KHT5593	A
			100KT5593	A
			10KHT5648	A
			100KT5648	A
Octal Registered	ECL-to-TTL	OE/3S	10KHT5590	A
Transceiver Noninverting			100KT5590	A
			10KHT5592	A
			100KT5592	A
			10KHT5646	A
			100KT5646	A

- Product available in technology indicated
- ▲ New Product planned in technology indicated

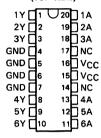
EPIC™ ACL PINOUTS

'AC11000, 'ACT11000 QUADRUPLE 2-INPUT **POSITIVE-NAND GATES** (TOP VIEW) 1A 1 U16 1B 15 2A 1Y 2 2Y 🛚 3 14 2B GND □4 13 VCC GND 75 12 VCC 3Y 🛮 6 11 3A 4Y 🛮 7 10 3B 4B ∏8 9 4A 'AC11008, 'ACT11008 **QUADRUPLE 2-INPUT POSITIVE-AND GATES** (TOP VIEW)

'AC11002, 'ACT11002 QUADRUPLE 2-INPUT POSITIVE-NOR GATES (TOP VIEW)

1A 🗌	1	U 16] 1B
17	2	15] 2A
2Y 🗌	3	14] 2B
GND 🗌	4	13]] Vcc
GND 🗌	5	12] Vcd
3Y 🗌	6	11]3A
4Y 🗌	7	10] 3B
4B 🗌	8	9] 4A

'AC11004, 'ACT11004 HEX INVERTERS (TOP VIEW)



U ₁₆] 1В
15] 2A
14] 2B
13	□vcc
12	□vcc
11] 3A
10] 3B
9	Ď4A
	15 14 13 12

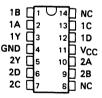
'AC11010, 'ACT11010 TRIPLE 3-INPUT POSITIVE-NAND GATES (TOP VIEW)

1A [ſī	U ₁₆] 1B
1Y [2	15] 1C
2Y []3	14] 2A
GND []4	13	□vcc
GND []5	12	□vcc
3Y []6	11	☐ 2B
3C []7	10] 2C
3B [18	9] 3A

'AC11011, 'ACT11011 TRIPLE 3-INPUT POSITIVE-AND GATES (TOP VIEW)

1A	Œ٦	U_{16}] 1B
1Y	\Box_2	15] 1C
2Y	[]₃	14] 2A
GND	□4	13	□vco
GND	□ 5	12	□ vcc
3Y	∏ 6	11] 2B
3C	Ū۶	10] 2C
3B	[8	9] 3A

'AC11013, 'ACT11013 DUAL 4-INPUT GATES (TOP VIEW)



'AC11014, 'ACT11014 HEX INVERTERS (TOP VIEW)

1Y	П	1	U 20		1A
2Y	d	2	19	6	2A
3Y	П	3	18	6	ЗА
GND		4	17	b	NC
GND		5	16	0	Vcc
GND		6	15	0	Vcc
GND		7	14		NC
4Y	П	8	13	5	4A
5Y		9	12	5	5A
6Y	₫	10	11		6A

'AC11020, 'ACT11020 DUAL 4-INPUT POSITIVE-NAND GATES (TOP VIEW)

1B 🗆	1	U 14		NC
1A 🗌	2	13	Б	1C
17	3	12		1D
GND 🗌	4	11	٥	Vcc
2Y [5	10	D	2A,
2D [6	9		2B
2C 🗀	7	8		NC

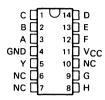




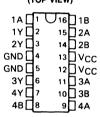
'AC11027, 'ACT11027 TRIPLE 3-INPUT POSITIVE-NOR GATES (TOP VIEW)

1 A [ſτ	U ₁₆ 1B
1Y[2	15 🗖 1 C
2Y[]3	14 🛮 2A
GND[4	13 □ V _{CC}
GND[5	12 VCC
3Y[6	11 🔲 2B
3C[7	10 🛮 2C
3в[18	9 🗌 3A

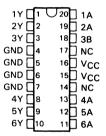
'AC11030, 'ACT11030 8-INPUT POSITIVE-NAND GATES (TOP VIEW)



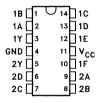
'AC11032, 'ACT11032 QUADRUPLE 2-INPUT POSITIVE-OR GATES (TOP VIEW)



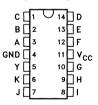
'AC11034, 'ACT11034 HEX NONINVERTERS (TOP VIEW)



'AC11051, 'ACT11051 DUAL 2-INPUT AND-OR GATE (TOP VIEW)



'AC11064, 'ACT11064 QUAD 4-2-3-2-INPUT AND-OR GATE (TOP VIEW)



'AC11074, 'ACT11074
DUAL D-TYPE POSITIVE-EDGE
TRIGGERED FLIP-FLOPS WITH
CLEAR AND PRESET
(TOP VIEW)

1PRE	1	U14] 1CLK
10 [2	13] 1D
10 [3	12	1CLR
GND [4	11	□vcc
20 [5	10	2CLR
20 [6	9] 2D
2PRE	7_	8	2CLK

'AC11086, 'ACT11086 QUAD 2-INPUT EXCLUSIVE-OR GATE (TOP VIEW)

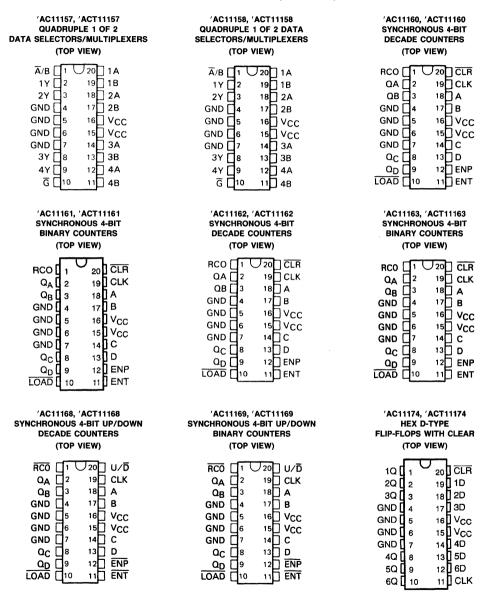
	_		_	
1A[1	U	16	1B
1Y[2		15	2A
2Y[3		14	2B
GND[4		13] v _{cc}
GND[5		12	l vcc
3Y[6		11	3Ă
4Y[7		10	3B
4B	8		9	4A
7	ĺ			Γ

'AC11109, 'ACT11109 'AC11112, 'ACT11112 'AC11132, 'ACT11132 **DUAL J-K DUAL J-K NEGATIVE QUADRUPLE 2-INPUT** POSITIVE-EDGE-TRIGGERED **EDGE-TRIGGERED FLIP-FLOPS** POSITIVE-NAND SCHMITT TRIGGERS FLIP-FLOPS WITH CLEAR AND PRESET WITH CLEAR AND PRESET (TOP VIEW) (TOP VIEW) (TOP VIEW) 1A 🔯 U16∏ 1B 1PRE 1 1016 1CLK 15 2A 1Y ∏2 1PRE 1 1 16 1J 10 \square_2 15 1K 10 2 15 1K 2Y ∏3 14 2B 1**□** □3 14∏ 1J GND □4 13 VCC 10 [13 14 1 1CLK GND □4 13 1 1 CLR GND 75 GND ∏4 13 1 1 CLR 12 VCC 20 05 11 3A 12 VCC **3Y** □6 20 ∏5 12 VCC 20 □6 11 2CLR 10 3B 4Y 🛛 7 20 □6 11 2CLR 2PRE 7 10 2J 2PRE □7 **4B** ∏8 9 AA 10 2CLK 2CLK 8 9∏ 2K 2J 🛮 8 9 2K 'AC11138, 'ACT11138 'AC11139, 'ACT11139 'AC11150, 'ACT11150 3-LINE TO 8-LINE **DUAL 2-LINE TO 4-LINE** 1-OF-16 DATA DECODERS/DEMULTIPLEXERS GENERATOR/MULTIPLEXERS DECODERS/DEMULTIPLEXERS (TOP VIEW) (TOP VIEW) (TOP VIEW) E4 🗍 1 ∪24∏E5 U16 1Y0 Y1 □1 ∪16□ Y0 1Y1 ∏1 1Y2 [2 15 1A E3 ∏2 23 | E6 Y2 1 2 15 A **Y3** □3 14 B 173 □3 14 1B E2 ∏3 22 E7 GND 4 13 C GND ☐4 E1 □4 21 E8 13 📗 1 G Y4 🗍 5 2Y0 5 12 VCC 12 VCC E0 ∏5 20 E9 11 G1 11 2G Y5 ∏6 2Y1 ∏6 GND ∏6 19 E10 10 G2A 2Y2 17 10 2A Y6 ∏7 w ∏ 7 18 V_{CC} Y7 🗖8 9 T G2B 2Y3 8 эĦ 2B 17 E11 A ∏8 в Пэ 16∏ E12 15 E13 с П10 D 🛮 11 14 E14 13 E15 'AC11151, 'ACT11151 'AC11153, 'ACT11153 'AC11154, 'ACT11154 1 OF 8 DATA **DUAL 4-LINE TO 1-LINE DATA** 4-TO-16 LINE SELECTORS/MULTIPLEXERS SELECTORS/MULTIPLEXERS DECODER/DEMULTIPLEXER (TOP VIEW) (TOP VIEW) (TOP VIEW) DO [[1] U16[] D1 **∪24**∏3 A □1 ∪16∏ 1C0 ਰ **ੀ**2 15 D2 5 T2 23 2 **B** □2 15 1C1 Y ∏3 14 D3 1Y 🛮 3 6 ∏3 22 1 14∏ 1C2 GND [4 13 D4 7 ∏4 GND □4 13 1C3 21 🗆 0 12 VCC W ∏5 2Y 🛮 5 12 VCC 8 ∏ 5 20 G1 A □6 11 D5 ₫6 19 G2 1Ğ 11 2CO GND □ вΓ 2Ğ 🗖 7 7 10 D6 18 V_{CC} 10 2C1 9 ∏7 C ∐8 9 D7 9 7 2C2 2C3 ∏8 10 ∏8 17 A 11∏9 16 B 12 10 15 C 13 11 14∏ D

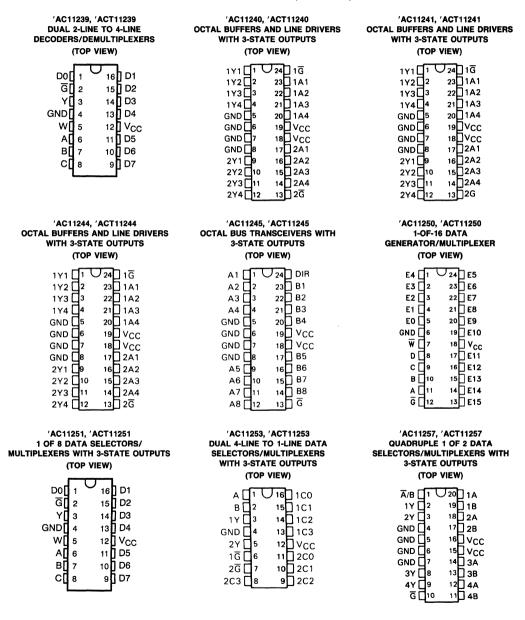


13 15

14 112



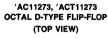
'AC11175, 'ACT11175 'AC11181, 'ACT11181 'AC11190, 'ACT11190 QUADRUPLE D-TYPE ARITHMETIC LOGIC UNITS/ SYNCHRONOUS 4-BIT UP/DOWN **FLIP-FLOPS WITH CLEAR FUNCTION GENERATORS DECADE COUNTERS** (TOP VIEW) (TOP VIEW) (TOP VIEW) $C_n \begin{bmatrix} 1 & \bigcup 28 \end{bmatrix} \overline{A}0$ $M \begin{bmatrix} 2 & 27 \end{bmatrix} \overline{A}1$ 1Q 1 20 1 1Q RCO I 20 D/Ū 19 CLR 2Q 🛛 2 QA [2 19 CLK 26 A2 A = B □3 2Q [3 18 TD 18 🛮 A Q_B 3 25∏ Ā3 Fo ∏4 GND [] 4 17 2D 24 BO GND 1 4 17 B F1 ∏5 23 B1 GND II 5 GND T6 GND 5 16 V_{CC} 16 VCC GND 🗗 22 VCC GND 6 15 VCC GND 6 15 VCC 21 VCC GND 18 GND 7 14 🛮 C GND 1 7 14 N 3D 20 T B 2 GND [19 3Q [8 13 AD 13 D Q_C [] 8 F2 | 10 19 T B3 12 CTEN 3<u>Q</u> [] 9 12 CLK QD [] 9 F3 ∏11 18 SO 11 1 4Q 11 LOAD MAX/MIN 10 4Q 🛮 10 P 112 17 T S1 G ∏13 16 T S2 15Fi S3 Cn + 4 114 'AC11191, 'ACT11191 'AC11192, 'ACT11192 'AC11193, 'ACT11193 SYNCHRONOUS 4-BIT UP/DOWN SYNCHRONOUS 4-BIT UP/DOWN DECADE SYNCHRONOUS 4-BIT UP/DOWN BINARY **COUNTERS (DUAL CLOCK WITH CLEAR) BINARY COUNTERS** COUNTERS (DUAL CLOCK WITH CLEAR) (TOP VIEW) (TOP VIEW) (TOP VIEW) BO T 20 DOWN BO T 20 DOWN 20 D/Ū RCO I 1 19 UP Q_A ∏2 19 UP 19]] CLK QA [2 18∏ A **QB** □3 **QB** □3 18 A 17[] B Q_B [] 3 18 A GND 14 GND 14 17 B GND 4 16∏ VCC 17 N B GND TIS GND T 5 16 VCC 15 VCC GND [] 5 GND □6 16 VCC 14∏ C GND □6 15 VCC GND 7 GND 6 15 VCC GND 17 13 D oc □s 14 C GND 7 14 T C QD ∏9 12 CLR QC []8 13 D 13 D Q_C 8 CO 110 11 LOAD σ_D [9 12 CLR 12 CTEN QD [] 9 CO □10 11 LOAD 11 LOAD MAX/MIN [] 10 'AC11194, 'ACT11194 'AC11208, 'ACT11208 'AC11238, 'ACT11238 4-BIT BIDIRECTIONAL UNIVERSAL **DUAL 1-TO-4 CLOCK DRIVER** 3-LINE TO 8-LINE SHIFT REGISTERS DECODERS/DEMULTIPLEXERS (TOP VIEW) (TOP VIEW) (TOP VIEW) 1Y2 | 1 U 20 | 1Y1 Y1 □1 16∏ YO 1Y3 🛮 2 SR SER 20 S0 19**П** 1A 15 A Y2 ∏2 19 🛮 S1 Q_A 1Y4 🛮 3 18 1G1 2 14 🛭 B Y3 □3 18 🛮 A Q_B [] 3 GND 14 17 1G2 13 C GND □4 GND [] 4 17 B 16 V_{CC} GND II 5 Y4 🛮 5 12 VCC GND [16 VCC 15 V_{CC} 5 GND [] 6 Y5 ∏6 11 G1 15 VCC GND [6 GND 17 14 2A Y6 □ 7 10 ☐ G2A GND II 7 14 🛛 C 2Y1 🛮 8 13 2G1 Y7∏8 9 ∏ G2B 13 D Q_C [] 8 2Y2 🛛 12 2G2 9 12 CLR $Q_D \square 9$ 2Y3 10 11 2Y4 SL SER [10 11 T CLK

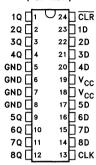


EPIC™ ACL PINOUTS (continued) AC11258, 'AC11258 QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS TOP VIEW)

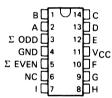
(TOP VIEW) A/B 1 20 1A 17 12 19 1B 2Y 13 18 2A 17 2B GND ☐4 16∐ V_{CC} GND 05 15 VCC GND ∏6 GND □7 14 3A 37 🛮 8 13 3B 4Y 🛮 9 12 AA ਰ **□**10 11 AB

(TOP VIEW)						
CLK Q0 Q1 Q2 Q3 GND GND GND Q4 Q5 Q6		1 2 3 4 5 6 7 8 9 10 11 12	28 27 26 25 24 23 22 21 20 19 18 17 16	ומממממממממממ	U/D PE PO P1 P2 P3 VCC P4 P5 P6 P7 CEP	
	ч			μ	CEI	

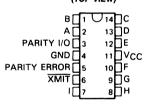




'AC11280, 'ACT11280 9-BIT PARITY GENERATORS/CHECKERS (TOP VIEW)



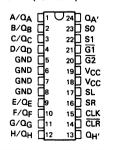
'AC11286, 'ACT11286
9-BIT PARITY GENERATORS/
CHECKERS WITH BUS DRIVER
PARITY I/O PORT
(TOP VIEW)



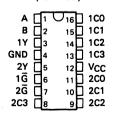
'AC11299, 'ACT11299
8-BIT UNIVERSAL SHIFT/STORAGE
REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)

A/QA []T	U24 QA'
B/QB []2	23 SO
C/QC []₃	22 S1
D/QD []4	21 G1
GND ∐s	20 G2
GND ∏6	19 VCC
GND ∏7	18□ VCC
GND ∐8	17 SL
E∕QE 🗍9	16 SR
F/QF []10	15 CLK
G/QG []11	14 CLR
H/QH ∏12	13 \ QH′

'AC11323, 'ACT11323
8-BIT UNIVERSAL SHIFT/STORAGE
REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)

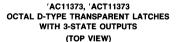


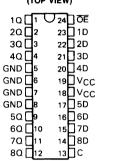
'AC11352, 'ACT11352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS (TOP VIEW)



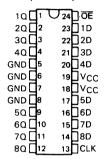
'AC11353, 'ACT11353 DUAL 1 OF 4 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS (TOP VIEW)

A [1 U 16] 1C	Λ
A []¹ U16[] 1C	v
B 🛛 2 15 🗍 1 C	1
1Y 🛛 3 14 🔲 1C	2
GND	3
2Y 🛮 5 12 🕽 V C	С
1G ☐6 11 ☐ 2C	0
2G	1
2C3 8 9 2C	2

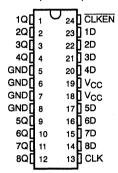




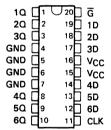
'AC11374, 'ACT11374
OCTAL D-TYPE EDGE-TRIGGERED
FLIP-FLOPS
(TOP VIEW)



'AC11377, 'ACT11377 OCTAL D-TYPE FLIP-FLOP (TOP VIEW)



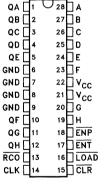
'AC11378, 'ACT11378 **HEX D-TYPE FLIP-FLOPS** WITH CLOCK ENABLE (TOP VIEW)



'AC11379, 'ACT11379 QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR (TOP VIEW)

1Q [1	U	20] 1Q
2Q [19	CLKEN
2 <u>0</u> [18] 1D
GND [4		17] 2D
GND [16] v _{cc}
GND [15] v _{cc}
GND [14] 3D
3Q [13] 4D
3Q [9		12	CLK
4Q [10)	11] 4Q

'AC11461 'ACT11461 8-BIT SYNCHRONOUS BINARY COUNTER (TOP VIEW)



'AC11463 'ACT11463 8-BIT SYNCHRONOUS BINARY COUNTER (TOP VIEW)	'AC11469 'ACT11469 8-BIT SYNCHRONOUS UP/DOWN COUNTER (TOP VIEW)	'AC11470 'ACT11470 OCTAL BUS TRANSCEIVER (TOP VIEW)
QA	QA	GBA 1
'AC11471 'ACT11471 OCTAL BUS TRANSCEIVER (TOP VIEW)	'AC11472 'ACT11472 9-BIT BUS TRANSCEIVER (TOP VIEW)	'AC11473 'ACT11473 9-BIT BUS TRANSCEIVER (TOP VIEW)
GBA	LEAB 1	LEAB 1

AC11474 'AC11475 'AC11520, 'ACT11520 ACT11474 'ACT11475 8-BIT IDENTITY COMPARATOR 9-BIT BUS TRANSCEIVER 9-BIT BUS TRANSCEIVER (TOP VIEW) (TOP VIEW) (TOP VIEW) Q1 1 20 G CLKAB 1 U28 OEBA CLKAB 1 28 OEBA P1 1 2 19 P2 A0 ∏2 27 CLKBA A0 ∏2 27 CLKBA വെ∏ദ 18 02 А1 ∏ 3 26 T BO 26 BO 17 P3 А1 Пз PO 14 25 B1 16 Q3 A2 ∏4 25 B1 A2 | 4 GND 5 A3 ∏5 24 B2 A3 ∏5 24 B2 $P = Q \square 6$ 15 VCC GND ∏6 23 B3 GND □6 23 T B3 Q7 [7 14 P4 22 V_{CC} 22 V_{CC} GND □7 GND T7 P7 🗆 8 13 04 Q6 🗖 9 12 P5 GND □8 21 V_{CC} GND ∏8 21 VCC GND ∏9 P6 🗆 10 11 Q Q 5 20 B4 GND ∏9 20 ∏ B4 19 B5 A4 ∏10 A4 110 19 B5 A5 | 11 A5 | 11 18 B6 18 B6 17 🗌 B7 17 B7 A6 ∏12 A6 ∏12 A7 ☐13 16 B8 16 B8 A7 ∏13 15 OEAB 15 OEAB A8 ∏14 A8 ∏14 'AC11533, 'ACT11533 'AC11521, 'ACT11521 'AC11534, 'ACT11534 8-BIT IDENTITY COMPARATOR OCTAL D-TYPE TRANSPARENT **OCTAL D-TYPE EDGE-TRIGGERED LATCHES WITH 3-STATE OUTPUT** FLIP-FLOPS WITH 3-STATE OUTPUT (TOP VIEW) (TOP VIEW) (TOP VIEW) Q1 🛮 1 ∪20 | G 10 []1 U24] OE 10 🛮 1 P1 ∏2 19 P2 20 2 23 1D 20 02 23 1D 18 Q2 **Q**0∏3 3₫ 🛮 3 3<u>0</u> □3 22 2D P0 □4 17 P3 22 2D 40 ∏4 21 3D 40 ∏4 21 T 3D GND TIS 16 Q3 GND ☐5 20 7 4D GND □5 20 4D $P = Q \cap G$ 15 VCC GND 6 19 VCC GND 6 19 VCC Q7 []7 14 P4 GND IT 18 VCC GND ∏7 18 VCC P7 ∏8 13 Q4 GND □8 Q6∏9 12 P5 17 D 5D GND □8 17 5D 50 ∏e 16 T 6D 50 □9 16 T 6D P6 ☐10 11 Q5 6₫ 🗖10 15 7D 60 □10 15 7D 70 🛮 11 14 8D 70 []11 14 🗌 8D

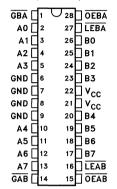
80 712

13 T C

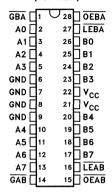
80 12

13 CLK

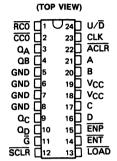
'AC111543, 'ACT11543 OCTAL REGISTERED TRANSCEIVER (TOP VIEW)



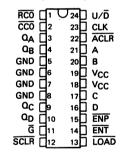
'AC11544, 'ACT11544 OCTAL REGISTERED TRANSCEIVER (TOP VIEW)



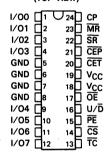
'AC11568, 'ACT11568
SYNCHRONOUS 4-BIT UP/DOWN
DECADE COUNTERS WITH
3-STATE OUTPUTS



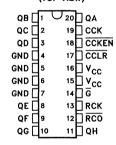
'AC11569, 'ACT11569 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS (TOP VIEW)



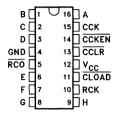
'AC11579, 'ACT11579 8-BIT BIDIRECTIONAL BINARY COUNTER WITH 3-STATE OUTPUTS (TOP VIEW)



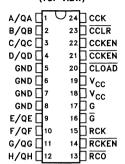
'AC11590, 'ACT11590 8-BIT REGISTERED BINARY COUNTER (TOP VIEW)



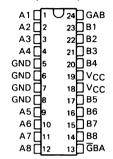
'AC11592, 'ACT11592 8-BIT REGISTERED BINARY COUNTER (TOP VIEW)



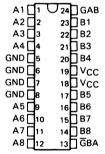
'AC11593, 'ACT11593 8-BIT REGISTERED BINARY COUNTER (TOP VIEW)



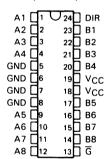
'AC11620, 'ACT11620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTUTS (TOP VIEW)



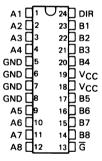
'AC11623, 'ACT11623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

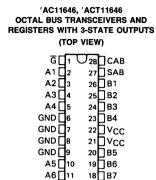


'AC11640, 'ACT11640 OCTAL BUS TRANSCEIVERS (TOP VIEW)



'AC11643, 'ACT11643 OCTAL BUS TRANSCEIVERS (TOP VIEW)





A7 12

A8 13

DIR 14

'AC11648, 'ACT11648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS (TOP VIEW)

<u></u> G[1	28] CAB
A1 [2	27 SAB
A2[3	26 B1
A3[4	25 B2
A4[5	24 B3
GND[6	23 B4
GND[7	22 V _{CC}
GND[8	21 VCC
GND[9	20 B5
A5 [10	19 B6
A6[11	18 B7
A7[12	17 🛮 B8
A8[13	16 CBA
DIR[14	15 SBA

'AC11651, 'ACT11651 OCTAL BUS TRANSCEIVERS AND REGISTERS (TOP VIEW)

1		_	
GAB[₁ O	28] CAB
A1 [2	27] SAB
A2[3	26] B1
A3[4	25] B2
A4[5	24] B3
GND[6	23] B4
GND[7	22] V _{CC}
GND[8	21] V _{CC}
GND[9	20] B5
A5[10	19] B6
A6[11	18	B7
A7[12	17] B8
A8[13	16] CBA
GBA[14	15] SBA
			l

'AC11652, 'ACT11652 OCTAL BUS TRANSCEIVERS AND REGISTERS (TOP VIEW)

17 B8

16∏СВА

15 TSBA

GAB [1	Ј28 ПСАВ	
A1 C	2	27 SAB	
A2 C	3	26 B1	
=	1		
A3 💆	4	25 B2	
A4 L	5	24 🗌 B3	
GND [6	23 🗌 B4	
GND [7	22 VCC	
GND 🗌	8	21 VCC	:
GND [9	20 🗍 B5	
A5 🗌	10	19 🔲 B6	
A6 🗌	11	18 🔲 B7	
A7 [12	17 🛮 B8	
A8 [13	16 CBA	
GBA [14	15 SBA	

'AC11655, 'ACT11655 OCTAL BUS DRIVER WITH PARITY (TOP VIEW)

Q0 [ī	U 28		OER1
Q1 []2	27		OER2
Q2 [3	26		OER3
Q3 [₫4	25		DO
Q4 [5	24		D1
GND [6	23		D2
GND []7	22		v _{cc}
GND [8	21		v _{cc}
GND []9	20	D	D3
Q5 []10	19	р	D4
Q6]11	18		D5
Q7 [12	17		D6
P0 [] 13	16		D7
P0 [14	15	Д	ΡI

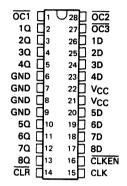
'AC11656, 'ACT11656 OCTAL BUS DRIVER WITH PARITY (TOP VIEW)

Q0 [1	U	28	Ь	ŌĒ	R1
Q1 [2		27		ŌΕ	R2
Q2 [3		26		ŌΕ	R3
Q3 [4		25		DO	
Q4 [5		24		D1	
GND 🗌	6		23		D2	
GND [7		22		٧c	С
GND [8		21		٧c	c
GND [9		20		D3	-
Q5 [10		19	D	D4	
Q6 [11		18	D	D5	
Q7 [12		17		D6	
PO [13		16		D7	
PO [14		15	D	ы	

'AC11657, 'ACT11657 OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 8-BIT PARITY GENERATOR/ CHECKER AND 3-STATE OUTPUTS (TOP VIEW) PARITY/B8	'AC11677, 'ACT11677 16-BIT ADDRESS COMPARATOR (TOP VIEW) PO	'AC11678, 'ACT11678 16-BIT LATCHED ADDRESS COMPARATOR (TOP VIEW) PO
'AC11800, 'ACT11800 TRIPLE 4-INPUT AND/NAND DRIVER (TOP VIEW)	'AC11802, 'ACT11802 TRIPLE 4-INPUT OR/NOR DRIVER (TOP VIEW)	'AC11810, 'ACT11810 QUAD 2-INPUT EXCLUSIVE NOR GATE (TOP VIEW)
1A	1A	1A

AC11818, 'ACT11818 DIAGNOSTIC/PIPELINE REGISTER (TOP VIEW) OC	AC11819, 'ACT11819 DIAGNOSTIC/PIPELINE REGISTER (TOP VIEW) OC	'AC11821, 'ACT11821 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW) 10
'AC11822, 'ACT11822 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11823, 'ACT11823 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11824, 'ACT11824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW)
1Q	1Q	1Q

'AC11825, 'ACT11825 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW)



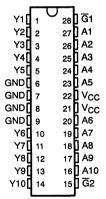
'AC11826, 'ACT11826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS (TOP VIEW)



'AC11827, 'ACT11827 10-BIT BUFFERS WITH 3-STATE OUTPUTS (TOP VIEW)

Y1[1	28] <u>G</u> 1
Y2[2	27] A1
Y3[3	26] A2
Y4[4	25] A3
Y5[5	24] A4
GND[6	23] A5
GND[7	22] Vcc
GND[8	21	Vcc
GND[9	20] A6
Y6[10	19] A7
Y7[11	18] A8
Y8[12	17] A9
Y9[13	16] A10
Y10[14	15] <u>G</u> 2

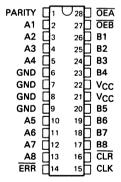
'AC11828, 'ACT11828 10-BIT BUFFERS WITH 3-STATE OUTPUTS (TOP VIEW)



'AC11833, 'ACT11833
PARITY BUS TRANSCEIVERS
(TOP VIEW)

PARITY[70	28 OEA
A1 🛚	2	27 OEB
A2[3	26]] B1
A3[4	25 B2
A4[5	24 B3
GND[6	23 B4
GND[7	22 🛘 V _{CC}
GND[8	21 V _{CC}
GND[9	20 B5
A5[10	19 🛭 B6
A6[]	11	18 B7
A7[12	17 B8
]8A	13	16 CLR
ERR[14	15 CLK

'AC11834, 'ACT11834
PARITY BUS TRANSCEIVERS
(TOP VIEW)



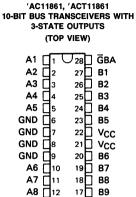
'AC11841, 'ACT11841 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11842, 'ACT11842 10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11843, 'ACT11843 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)
1Q	1Q	1Q
'AC11844, 'ACT11844 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11845, 'ACT11845 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)	'AC11846, 'ACT11846 8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)
1Q	OC1	OC1

'AC11852, 'ACT11852 8-BIT UNIVERSAL PORT CONTROLLER (TOP VIEW) SO	PARITY U 28 OEA A1 2 27 OEB A2 3 26 B1 A3 4 25 B2 A4 5 24 B3 GND 6 23 B4 GND 7 22 VCC GND 8 21 VCC GND 8 21 VCC GND 9 20 B5 A5 10 19 B6 A6 11 18 B7 A7 12 17 B8 A8 13 16 CLR ERR 14 15 LE	AC11854, 'ACT11854 PARITY BUS TRANSCEIVERS (TOP VIEW) PARITY 1 28 0ER A1 2 27 0ET A2 3 26 B1 A3 4 25 B2 A4 5 24 B3 GND 6 23 B4 GND 7 22 VCC GND 8 21 VCC GND 9 20 B5 A5 10 19 B6 A6 11 18 B7 A7 12 17 B8 A8 13 16 CLR ERR 14 15 EN
'AC11856, 'ACT11856 8-BIT UNIVERSAL PORT CONTROLLER (TOP VIEW)	'AC11858, 'ACT11858 DUAL PORT 16 x 5 REGISTER FILE (TOP VIEW)	'AC11859, 'ACT11859 DUAL PORT 32 x 4 REGISTER FILE (TOP VIEW)
OEA	DQA0	AWR 1

8-BIT MAGITUDE COMPARATOR (TOP VIEW) Q0 🗖 1 ∪24∏P1 P0 ∏2 23 01 L/Ā ∐3 22 P2 21 7 02 P=Q_{OUT} □4 20 P3 P>Q_{OUT} ∏5 GND ∏6 19 Q3 18∏ V_{CC} P []7 РΓ 17 P4 16 Q4 Q7 🗆 10 15 P5 14 Q5 P7 □11

Q6 🗆 12

'AC11860, 'ACT11860

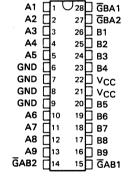


'AC11862, 'ACT11862 O-BIT BUS TRANSCEIVERS WITH			
		OUTPU	
	(TOP	VIEW)	
A1	<u></u> 1	∪ 28	GBA
A2	□ 2	27	B1
A3	\square_3	26	B2
A4	4	25	B3
A5	□ 5	24	B4
GND	□ 6	23	B5
GND	ď٦	22	Vcc
GND	□8	21	Vcc
GND	□ 9	20	B6
A6	1 10	19	B7
A7		18	B8
A8	1 12	17	B9
A9	13	16	B10
A10	14	15	ĞАВ

/AC11060 /ACT11060

'AC11863, 'ACT11863
9-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

13 P6

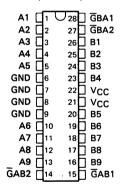


'AC11864, 'ACT11864 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

16 B10 15 GAB

A9 713

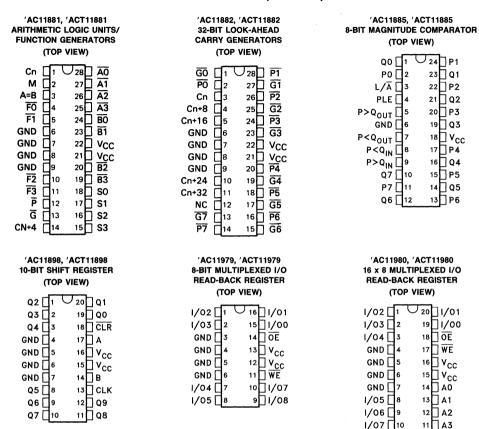
A10 ∏14



'AC11865, 'ACT11865 8-BIT MAGNITUDE COMPARATOR (TOP VIEW)

L/Ā 📑	1	U 16
PLE [2	15 P/Q1
P>Q _{OUT}	3	14 P/Q2
GND 🔲	4	13 P/Q3
P <q<sub>OUT</q<sub>	5	¹² □ V _{CC}
P <q<sub>IN □</q<sub>		11 P/Q4
P>Q _{IN} ☐	7	10 P/Q5
P/Q7 🔲	8	9 P/Q6

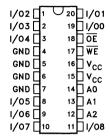
'AC11867, 'ACT11 8-BIT SYNCHRONG UP/DOWN COUNT (TOP VIEW)	OUS 8-BIT SYNCHRO	NOUS DUAL POI NTER 16 x 4 REGISTI	RT ER FILE
QA 1	B	B DQA1 2 2 2 2 3 2 3 2 3 2 3 2 3 2 3 2 3 2 3	28
'AC11873, 'ACT11 DUAL 4-BIT D-TYPE LA WITH 3-STATE OUT (TOP VIEW)	ATCHES DUAL 4-BIT D-TYPE EDG	SE-TRIGGERED 8-BIT UNIVE S PORT CONTR	RSAL OLLER
1C[1 28] 1Q1[2 27] 1Q2[3 26] 1Q3[4 25] 1Q4[5 24] 1Q4[5 24] 1QMD[6 23] 1QND[7 22] 1QND[8 21] 1QND[9 20] 12 2Q1[10 19] 12 2Q2[11 18] 12 2Q4[13 16] 12 2Q4[13 16] 12 2Q4[14 15]	CLR 1Q1	10E	S1 S2 SERIN B1 B2 SECC VCC B4 B5 B6 B7 B8 Q8



16 x 8 MU READ-BA	1, 'ACT11981 LTIPLEXED I/O CK REGISTER P VIEW)
I/02 1	20 1/01
I/03 2	19 1/00
I/04 3	18 0E



'AC11987, 'ACT11987 8 x 9 MULTIPLEXED I/O
READ-BACK REGISTER
(TOP VIEW)



'AC11988, 'ACT11988 8 x 9 MULTIPLEXED I/O READ-BACK REGISTER (TOP VIEW)

1/02	1	U20∏1/01
1/03 🛚	2	19 🗌 1/00
1/04	3	18 🗍 ŌĒ
GND [4	17 WE
GND [5	16 ∨ _{CC}
GND [6	15 V _{CC}
GND [7	14 🗌 AO
1/05	8	13 🗌 A1
1/06	9	12 🗌 A2
1/07 [10	11] 1/08

WIDE BUS™ PINOUTS

54AC16240 WD PACKAGI 74AC16240 DL PACKAGE 16-BIT BUS DRIVERS (TOP VIEW)		54AC/ACT16241 WD PACKAGE 74AC/ACT16241 DL PACKAGE 16-BIT BUS DRIVERS (TOP VIEW)
1 G	1\bar{G} \begin{array}{ c c c c c c c c c c c c c c c c c c c	1G
4G 24 25 3G	4G 24 25 3G	4G [24 25] 3G

54AC16244 WD PACKAGE
74AC16244 DL PACKAGE
54ACT16244 WD PACKAGE
74ACT16244 DL PACKAGE
16-BIT BUS DRIVERS

(TOP VIEW)

1G[1	48]] 2 <u>G</u>
1Y1[2	47 🛛 1A1
1Y2[3	46] 1A2
GND[4	45 GND
1Y3[5	44 🛛 1A3
1Y4[6	43 🛭 1A4
Vcc[7	42 VCC
2Y1[8	41 2A1
2Y2[]	9	40 2A2
GND[10	39 GND
2Y3[11	38] 2A3
2Y4[12	37 2A4
3Y1[13	36 [] 3A1
3Y2[14	35 3A2
GND[15	34 GND
3Y3[16	33 🛮 3A3
3Y4[17	32 3A4
Vcc[18	31 V _{CC}
4Y1[19	30 🛮 4A1
4Y2[20	29 🛮 4A2
GND[21	28 GND
4Y3[22	27 🛮 4A3
4Y4[]	23	26 4A 4
4 <u>G</u> [24	25 🛚 3G

54AC16245 WD PACKAGE
74AC16245 DL PACKAGE
16-BIT BUS TRANSCEIVERS
(TOP VIEW)

1DIR	, U	48]] 1G
1B1	2	47 🛮 1A1
1B2		46 1A2
GND]	4	45 GND
1B3 []	5	44 🛭 1A3
1B4	6	43 🛮 1A4
V _{CC}]	7	42 VCC
1B5 [8	41 1 1A5
1B6 🛚	9	40 1A6
GND [10	39 GND
1B7 [11	38]] 1A7
1B8 [12	37 🕽 1A8
2B1 [13	36 2A1
2B2 [14	35 2A2
GND [15	34 GND
2B3 [16	33 🛮 2A3
2B4 [17	32 2A4
Vcc [18	31 V _{CC}
2B5 [19	30] 2A5
2B6 [20	29] 2A6
GND [21	28] GND
2B7 [22	27 2A7
2B8 [23	26] 2A8
2DIR [24	25 2G

54ACT16245 ... WD PACKAGE 74ACT16245 ... DL PACKAGE 16-BIT BUS TRANSCEIVERS (TOP VIEW)

		_	
1DIR[1	48	1 <u>G</u>
1B1[2	47	1A1
1B2[3	46] 1A2
GND[4	45	GND
1B3[5	44	1A3
1B4[6	43	
Vcc[7	42] V _{CC}
1B5[8	41	1A5
1B6[9	40	
GND[10	39] GND
1B7[11	38	
1B8[12	37	1A8
2B1[13	36	2A1
2B2[14	35] 2A2
GND[15	34] GND
2B3[16	33	2A3
2B4[17	32	2A4
V _{CC} [18	31] V _{CC}
2B5[19	30	2A5
2B6[20	29] 2A6
GND[21	28] GND
2B7[22	27] 2A7
2B8[23	26	2A8
2DIR[24	25] 2 <u>G</u>

54AC16373 WD PACKAGE
74AC16373 DL PACKAGE
16-BIT D-TYPE LATCHES
(TOP VIEW)

10E	, U	48	1C
101	2	47	1D1
1Q2	3		1D2
GND[4	45	GND
1Q3	5		1D3
1Q4	6	43	1D4
Vcc[7	42	Vcc
1Q5[8	41	1D5
1Q6[9	40	1D6
GND[10	39	GND
1Q7[11	38	1D7
1Q8[12	37	1D8
2Q1[13	36	2D1
2Q2[14	35	2D2
GND[15		GND
2Q3[16	33	2D3
2Q4[17	32	2D4
V _{CC} [18	31	Vcc
2Q5[19	30	•
2Q6[20		2D6
GND[21		GND
2Q7[22		2D7
2Q8[23	26	2D8
20E[24	25	2C

54ACT16373	WD	PACKAGE
74ACT16373	. DL	PACKAGE
16-BIT D-TYF	E L	ATCHES
(TOP V	VIEW	n

1		_	
10E[1	48	1C
1Q1[2	47	1D1
1Q2[3	46	1D2
GND[4		GND
1Q3[5	44	1D3
1Q4[6		1D4
V _{CC} [42	Vcc
1Q5[41	1D5
1Q6[]	9		1D6
GND[10		GND
1Q7[11		1D7
1Q8[]	12		1D8
2Q1 [13	36	2D1
2Q2[14		2D2
GND[15] GND
2Q3[16		2D3
2Q4[2D4
V _{CC} [18		V _{CC}
2Q5[19		2D5
2Q6[20		2D6
GND[21		GND
2Q7[22	27	2D7
2Q8[2D8
2OE	24	25	1 2C

54AC16374 ... WD PACKAGE 74AC16374 ... DL PACKAGE 16-BIT D-TYPE FLIP-FLOPS (TOP VIEW)

10E	, U	48	1CLK
1Q1[2	47	1D1
1Q2	3		1D2
GND[]	4	45	GND
1Q3	5	44	1D3
1Q4[6	43	1D4
V _{CC} [7	42	Vcc
1Q5	8	41	1D5
1Q6[9		1D6
GND[10	39	GND
1Q7[11	38	1D7
1Q8[12	37	1D8
2Q1[13	36	2D1
2Q2	14	35	2D2
GND[15	34	GND
2Q3[16	33	2D3
2Q4[17	32	2D4
Vcc			l∨ _{cc}
2Q5[19		2D5
2Q6[20		2D6
GND[21	28	GND
2Q7[]	22		2D7
2Q8[23		2D8
2OE[24	25	2CLK
	L		

54ACT16374 WD PACKAGE
74ACT16374 DL PACKAGE
16-BIT D-TYPE FLIP-FLOPS
(TOP VIEW)

1		
10E[₁	48 1 1CLK
1Q1[2	47 1D1
1Q2[3	46[] 1D2
GND[4	45 GND
1Q3[5	44 🛚 1D3
1Q4[6	43 1D4
V _{CC} [7	42] V _{CC}
1Q5[8	41 🛮 1D5
1Q6[9	40 1D6
GND[10	39]] GND
1Q7[11	38] 1D7
1Q8[12	37] 1D8
2Q1[13	36 2D1
2Q2[14	35 2D2
GND[15	34 GND
2Q3[16	33 2D3
2Q4[17	32 2D4
Vcc[18	31 V _{CC}
2Q5[30 2D5
2Q6[]	20	29 2D6
	21	28 GND
2Q7[]	22	27 2D7
2Q8[23	26]] 2D8
20E[24	25 2CLK

54AC16470, 54ACT16470
WD PACKAGE
74AC16470, 74ACT16470
DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

		_	
10EAB	1 -	56	□ 1 OEBA
1CLKAB	2	55]1CLKBA
1 DEAB	3	54	1 DEBA
GND [4	53	GND
1A1[5	52]1B1
1A2 [6	51	□1B2
V _{cc} □	7	50	□v _{cc}
1A3 [8	49] 1B3
1A4 [9	48]1B4
1A5 [10	47]1B5
GND [11	46	GND
1A6 🗌	12	45]1B6
1A7 [13	44	□1 B7
1A8 🗌	14	43]1B8
2A1	15	42] 2B1
2A2	16	41	□ 2B2
2A3 [17	40	□ 2B3
GND [18	39	GND
2A4 [19	38	□ 2B4
2A5	20	37	2B5
2A6 🗌	21	36] 2B6
V _{cc} □	22	35	□v _{cc}
2A7 [23	34	□ 2B7
2A8	24	33	288
GND	25	32	GND
2DEAB	26	31	2DEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA
_			•

54AC16471, 54ACT16471 ... WD PACKAGE 74AC16471, 74ACT16471 ... DL PACKAGE 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)

			,
10EAB	h 0	56	1 OEBA
1CLKAB	2	55	1CLKBA
1 DEAB	3	54	1 DEBA
GND [4	53	GND
1A1[5	52] 1B1
1A2 [6	51] 1B2
V _{CC} [7	50	□ v _{cc}
1A3 [8	49] 1B3
1A4 [9	48] 1B4
1A5 🗀	10	47]1B5
GND [11	46	GND
1A6 [12	45]1B6
1A7 [13	44] 1 B7
1A8 [14	43]1B8
2A1[15	42	_ 2B1
2A2 [16	41	☐ 2B2
2A3 [17	40] 2B3
GND [18	39	GND
2A4 [19	38	2B4
2A5 [20	37] 2B5
2A6	21	36	2B6
V _{CC}	22	35	□v _{cc}
2A7 🗌	23	34	☐ 2B7
2A8 🗌	24	33	_ 2B8
GND [25	32	GND
2DEAB	26	31	2DEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

54AC16472, 54ACT16472 WD PACKAGE 74AC16472, 74ACT16472 DL PACKAGE 18-BIT REGISTERED TRANSCEIN (TOP VIEW)	54AC16473, 54ACT16473 WD PACKAGE 74AC16473, 74ACT16473 DL PACKAGE /ERS 18-BIT REGISTERED TRANSCEIVERS (TOP VIEW)	54AC16474, 54ACT16474 WD PACKAGE 74AC16474, 74ACT16474 DL PACKAGE 18-BIT REGISTERED TRANSCEIVERS (TOP VIEW)
(TOP VIEW) 10EAB 1	1 <u>0EAB</u>	(TOP VIEW) 1 OEAB
GND 25 32 GND 2A9 26 31 2B9 2LEAB 27 30 2LEBA 2OEAB 28 29 2OEBA		GND ☐ 25 32 ☐ GND 2A9 ☐ 26 31 ☐ 2B9 2CLKAB ☐ 27 30 ☐ 2CLKBA 2ŌEAB ☐ 28 29 ☐ 2ŌEBĀ

54AC16475, 54ACT16475 ...
WD PACKAGE
74AC16475, 74ACT16475 ...
DL PACKAGE
18-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

,	101 1	L ** ,	
1 OEAB	1 0	56	1 OEBA
1CLKAB	2	55	1CLKBA
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
v _{cc} $\bar{\Box}$	7	50	v _{cc}
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND [11	46	GND
1A7 🗌	12	45	1B7
1A8 [13	44	1B8
1A9 🗌	14	43	1B9
2A1	15	42	2B1
2A2 🗌	16	41	2B2
2A3 🗌	17	40	2B3
GND [18	39	GND
2A4 🗌	19	38	2B4
2A5 🗌	20	37	2B5
2A6 🗌	21	36	2B6
v _{cc} [22	35	v _{cc}
2A7	23		2B7
2A8 🗌	24	33	2B8
GND [25	32	GND
2A9 🗌	26		2B9
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

'AC16533, 'ACT16533 16-BIT D-TYPE LATCHES (TOP VIEW)

10E1 [1, 6	48	1 1 C
1Q1 [47	1D1
1Q2	3	46	1D2
GND [4	45	
1 <u>Q</u> 3 [1 <u>Q</u> 4 [5	44	1D3
		43	1D4
V <u>c</u> c[7	42	Vcc
1Q5 [8	41	1D5
1Q6 [9	40	
GND [10	39	
1 <u>0</u> 7 [1 <u>0</u> 8 [2 <u>0</u> 1 [11	38	
1 <u>Q</u> 8 [12	37	
201	13	36	2D1
202	14	35	2D2
GND L	15	34	GND
2 <u>Q</u> 3 [33	
2Q4 [17	32	
۷ <u>c</u> c [18	31 🛛	
2 <u>Q</u> 5		30	2D5
2Q6 [20	29	
GND [21	28	GND
207	22	27	
2 <u>Q</u> 8	23	26	
2OE L	24	25 J	2C

'AC16534, 'ACT16534 16-BIT D-TYPE FLIP-FLOPS (TOP VIEW)

OE1	1	J ₄₈	1 1CLK
<u>Q</u> 1	2	47	101
1Q2 [3	46	11D2
GND [4	45	GND
1Q3 [44	1D3
1Q4 [43	1D4
<u>∨cc [</u>	7	42	ī Vac
1Q5 [8	41	1D5
1Q6 [9	40	1D6
GND [10	39	GND
1Q7 [11	38	1D7
1 <u>Q</u> 8 [12	37	1D8 2D1
1 <u>Q8</u> [2 <u>Q</u> 1 [13	36	2D1
202 [GND [14	35	2D2
GND [15	34	GND
2 <u>Q</u> 3 [16	33	2D3
2Q4 [17	32	2D4
V <u>c</u> c[31	V _{CC} 2D5
2 <u>Q</u> 5 [19	30	2D5
2Q6 [20	29	2D6
GND [21	28	GND 2D7
2Q7 [22	27	2D7
2 <u>Q</u> 8 [26	2D8
20E [24	25] 2CLK

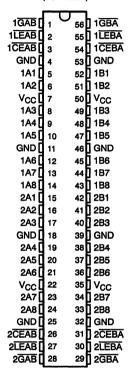
'AC16540, 'ACT16540 16-BIT BUS DRIVERS (TOP VIEW)

1G1 [1 1Y1 [2 1Y2 [3 h 1G2 47 1 1A1 46 1 1A2 GND 4 45 F GND 1Y3 🛮 5 44 1 1A3 1Y4 6 43 1A4 V_{CC} 7 1Y5 8 42 VCC 41 1 1A5 1Y6 [9 GND [10 40 1 1A6 39 **GND** 1Y7 🛮 11 38 T 1A7 1Y8 112 37 1 1A8 2Y1 (13 2Y2 (14 36 2A1 35 D 2A2 GND 115 34 GND GND | 15 2Y3 | 16 2Y4 | 17 VCC | 18 2Y5 | 19 2Y6 | 20 GND | 21 2Y7 | 22 33 D 2A3 32 2A4 31 VCC 30 2A5 29 2A6 28 D GND 27 2A7 2Y8 23 2G1 24 26 2A8 25 2G2

'AC16541, 'ACT16541 16-BIT BUS DRIVERS (TOP VIEW)

1G1 [1 1Y1 [2 1Y2 [3 GND [4 U48 1 1G2 47 🛭 1A1 46 1 1A2 45 1 GND 1Y3 🛮 5 44 T 1A3 43 🛭 1A4 1Y4 []6 V_{CC} 17 1Y5 18 42 0 VCC 41 1 1A5 1Y6 **]** 9 40 T 1A6 GND | 10 1Y7 | 11 1Y8 | 12 2Y1 | 13 39 GND 38 1 1A7 37 1 1A8 36 1 2A1 2Y2 114 GND 115 35 E 2A2 34 GND 2Y3 16 2Y4 17 33 T 2A3 32 D 2A4 V_{CC} 18 2Y5 19 2Y6 20 31 VCC 30 2A5 29 D 2A6 GND | 21 2Y7 | 22 2Y8 | 23 28 GND 27 D 2A7 26 D 2A8 Ī 24 2<u>G1</u> 25 2G2

54AC16543 ... WD PACKAGE 74AC16543 ... DL PACKAGE 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)



54ACT16543 ... WD PACKAGE 74ACT16543 ... DL PACKAGE 16-BIT REGISTERED TRANSSCEIVERS (TOP VIEW)

1GAB	, U	56	1GBA
1LEAB		55	1LEBA
1CEAB		54	1CEBA
GND [GND
1A1 [1B1
1A2[1B2
v _{cc} [Vcc
1A3 [8		1B3
1A4			1B4
1A5			1B5
GND [11		GND
1A6			1B6
1A7 🛚			1B7
1A8 [14		1B8
2A1 []			2B1
2A2 [16	41	2B2
2A3 [17		2B3
GND [18	39	GND
2A4 [19		2B4
2A5 [20	37	2B5
2A6 [21	36	2B6
V _{CC} [22	35	Vcc
2A7 [23		2B7
2A8 [24		2B8
GND [25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27		2LEBA
2GAB	28	29	2GBA

'AC16544, 'ACT16544 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)

10EAB	1	56	10EBA
1LEAB	2	55	
1CEAB	3	54	1CEBA
GND (4	53	GND
1A1 (5		1B1
1A2 [6	51	1B2
	7		VCC
VCC 1A3	8	49	
1A3 4 1A4 1		49	1B3
144 8	3	48	1B4
1A5 [10		1B5
GND [46	GND
1A6 [12	45	1B6
1A7 []	13	44	1B7
1A8 [14	43	1B8
2A1 [15	42	2B1
2A2 [16		2B2
2A3 [17	40	2B3
GND [18		GND
2A4 🛭		38	2B4
2A5 [20	37	
2A6 [21	36	2B6
Vcc (Vcc
2A7	23	34	2B7
2A8 [33	2B8
GND		35	GND
2CEAB	26	32	2CEBA
SUEAD I		31	2LEBA
2LEAB		30	STERY
20EAB	28	29	20EBA
,			

54ACT16620 ... WD PACKAGE 74ACT16620 ... DL PACKAGE 16-BIT BUS TRANSCEIVERS (TOP VIEW)

	-					
1GAB	Ц	1	U	48		1 GBA
1B1	q	2		47		1A1
1B2		3		46		1A2
GND		4		45		GND
1B3	Ճ	5		44		1 A 3
1B4		6		43		1 A 4
Vcc		7		42		v_{cc}
1B5		8		41	D	1 A 5
1B6		9		40	D	1A6
GND		10		39	b	GND
1B7	□	11		38	D	1A7
1B8		12		37		1A8
2B1		13		36		2A1
2B2		14		35		2A2
GND		15		34		GND
2B3		16		33		2A3
2B4		17		32		2A4
Vcc		18		31		V _{CC}
2B5	Ц	19		30		2A5
2B6		20		29		2A6
GND	Ц	21		28		GND
2B7	Ц	22		27		2A7
2B8	Ц	23		26		2A8
2GAB	Ц	24		25		2ĞBA

54AC16620 WD PACKAGE			
74AC16620 DL PACKAGE			
16-BIT BUS TRANSCEIVERS			
(TOP VIEW)			

•		,	
1GAB	1	48	
1B1[2	47 🗌 1 A 1	
1B2 🗌	3	46 🗌 1 A 2	
GND [4	45 GND	
1B3 [5	44 🗌 1 A 3	
1B4 🗌	6	43 1A4	
V _{CC}	7	42 V _{CC}	
1B5 [8	41 1A5	
1B6 🗌	9	40 🗌 1 A 6	
GND [10	39 GND	
1B7 🗌	11	38 🗌 1 A 7	
1B8 🗌	12	37 🗌 1 A 8	
2B1	13	36 2A1	
2B2 [14	35 2A2	
GND [15	34 GND	
2B3 [16	33 2A3	
2B4 🗌	17	32 2A4	
V _{CC} [18	31 🗌 V _{CC}	
2B5 [19	30 2A5	
2B6 [20	29 🗌 2A6	
GND [21	28 GND	
2B7 [22	27 🗌 2A7	
2B8 [23	26 2A8	
2GAB	24	25 2GBA	

'AC16623, 'ACT16623 16-BIT BUS TRANSCEIVERS (TOP VIEW)

1GAB	1	748	1GBA
	2		1A1
1B2	3		1A2
GND	4	45	GND
1B3 [1A3
	6		1A4
Vcc [· · · · •	Vcc
1B5 [8		1A5
1B6			1A6
GND			GND
1B7			1A7
1B8 [1A8
2B1			2A1
2B2 [14		2A2
GND			GND
2B3			2A3
2B4			2A4
Vcc [31	VCC
2B5 [30	2A5
2B6			2A6
GND [GND
2B7			2A7
2B8		26	2A8
2GAB		25	2GBA

54AC16640 ... WD PACKAGE 74AC16640 ... DL PACKAGE 16-BIT BUS TRANSCEIVERS (TOP VIEW)

1 DIR	1	48]1Ē
1B1 [2	47]1A1
1B2	3	46]1A2
GND [4	45	GND
1B3 [5	44] 1A3
1B4 🗌	6	43]1A4
V _{CC} [7	42	□ V _{CC}
1 B5 🗌	8	41	□1A5
1B6	9	40	□1A6
GND [10	39	GND
1B7 🗌	11	38]1A7
1B8 🛚	12	37]1A8
2B1 [13	36	2A1
2B2 🗌	14	35	2A2
GND [15	34	GND
2B3 🗌	16	33	2A3
2B4 [17	32	2A4
V _{cc} [18	31	□ V _{CC}
2B5 🗌	19	30	2A5
2B6 🗌	20	29	☐ 2A6
GND [21	28	GND
2B7 [22	27	2A7
2B8 [23	26] 2A8
2DIR	24	25] 2Ğ

54ACT16640 WD PACKAGE		
74ACT16640 DL PACKAGE		
16-BIT BUS TRANSCEIVERS		
(TOP VIEW)		

1 DIR 🗌	1 0	48
1B1	2	47 1A1
1B2	3	46 1A2
GND 🗌	4	45 GND
1B3 🗌	5	44 🗌 1 A 3
1B4 🗌	6	43 1A4
v _{cc} □	7	42 V _{CC}
1B5	8	41 1 A 5
1B6 🗌	9	40 🗌 1 A 6
GND [10	39 GND
1B7 🗌	11	38 🗍 1 A 7
1B8 🗌	12	37 🗌 1A8
2B1	13	36 2A1
2B2	14	35 2A2
GND [15	34 GND
2B3 🗌	16	33 🗌 2A3
2B4 🗌	17	32 2A4
V _{CC} [18	31 V _{CC}
2B5 🗌	19	30 2A5
2B6	20	29 🗌 2A6
GND [21	28 GND
2B7	22	27 🗌 2A7
2B8 🗌	23	26 2A8
2DIR	24	25 🗌 2G

54AC16646 WD PACKAGE
74AC16646 DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

		\neg	
1DIR[1	56	1G
1CAB[2		1CBA
	3		1SBA
GND[4	53	GND
1A1[5	52	1B1
1A2[6		1B2
V _{CC} [7	50	V _{CC}
1A3[8		1B3
1A4[9	48	1B4
1A5[10		1B5
GND[11		GND
1A6[12] 1B6
1A7[13		1B7
1A8[]	14] 1B8
2A1[2B1
2A2[16		2B2
2A3[17		2B3
GND[l .	39	GND
2A4[]	19		2B4
2A5[2B5
2A6[2B6
V _{CC} [] v _{cc}
2A7[2B7
2A8[2B8
GND[] GND
2SAB[] 2SBA
2CAB[2CBA
2DIR[28	29	12G

54ACT16646 ... WD PACKAGE 74ACT16646 ... DL PACKAGE 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)

,	(IOI VIEW)				
	U	_			
1DIR	1		1G		
	2		1CBA		
1SAB[3		1SBA		
GND[4	53	GND		
1A1[5	52	1B1		
1A2[6		1B2		
V _{CC} [7	50	V_{CC}		
1A3[8	49	1B3		
1A4[9	48	1B4		
1A5[10	47	1B5		
GND[11	46	GND		
1A6[12	45	1B6		
1A7[13	44	1B7		
1A8[14	43	1B8		
2A1	15		2B1		
2A2	16		2B2		
2A3		40	2B3		
GND[18	39	GND		
2A4[2B4		
2A5[20	37	2B5		
2A6[21	36	2B6		
V _{CC} [22	35	V _{CC}		
2A7[23		2B7		
2A8[24	33	2B8		
GND[25	32	GND		
2SAB[26		2SBA		
2CAB	27		2CBA		
2DIR[28	29	2G		
		_	-		

	'AC16648, 'ACT16648			
16-BIT	REGISTERED TRANSCEIVER	S		
(TOP VIEW)				

1DIR 1 1 56 🛮 1G 1CAB [2 55 1 1CBA 1SAB 7 3 54 1 1SBA GND 4 53 T GND 1A1 🛚 5 52 T 1B1 1A2 7 6 51 T 1B2 VCC 7 50 T VCC 1A3 fl 8 49 1 1B3 1A4 🗍 9 48 🛭 1B4 1A5 🛚 10 47 1 1B5 GND 7 11 46 F GND 1A6 🛚 12 45 1B6 1A7 1 13 44 5 1B7 1A8 👖 14 43 🖣 1B8 2A1 1 15 42 1 2B1 2A2 1 16 41 F 2B2 2A3 👖 17 40 🛭 2B3 GND 7 18 39 T GND 2A4 👖 19 38 F 2B4 2A5 👖 20 37 T 2B5 2A6 🕇 21 36 T 2B6 VCC 1 22 35 D VCC 2A7 🛮 23 34 🛭 2B7 2A8 🗍 24 33 Fi 2B8 GND 7 25 32 T GND 2SAB (26 31 T 2SBA 30 F 2CBA 2CAB 7 27 2DIR 7 28 2G 29 1

'AC16651, 'ACT16651 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)

1GAB [1 56 1 1 GBA 1CAB 1 2 55 1 1CBA 1SAB 🛚 3 54 1 1SBA GND 1 4 53 D GND 1A1 🛮 5 52 1 1B1 1A2 6 51 1 1B2 V_{CC} [] 7 1A3 [] 8 50 1 VCC 49 1 1B3 1A4 🛛 9 48 🛮 1B4 1A5 (10 47 1 1B5 GND 1 11 46 1 GND 1A6 🛮 12 45 N 1B6 1A7 1 13 44 D 1B7 1A8 1 14 43 1 1B8 2A1 11 15 42 1 2B1 2A2 16 41 1 2B2 2A3 [17 40 1 2B3 GND [18 39 T GND 2A4 🛮 19 38 2B4 2A5 20 37 N 2B5 2A6 [21 36 🛭 2B6 V_{CC} 22 2A7 23 35 🛛 VCC 34 1 2B7 33 D 2B8 2A8 [24 GND [25 2SAB [26 32 T GND 31 2SBA 2CAB 1 27 30 1 2CBA 2GAB [28 2GBA 29 👖

54AC16652 ... WD PACKAGE 74AC16652 ... DL PACKAGE 16-BIT REGISTERED TRANSCEIVERS (TOP VIEW)

1		_	1
1GAB	₁ U	56	1GBA
1CAB	2		1CBA
1SAB	3	54	1SBA
GND [4	53	GND
1A1 [5] 1B1
1A2 [6	51	1B2
Vcc [7		l v _{cc}
1A3 [49	1B3
1A4 [9	48	1B4
1A5 [10		1B5
GND [11	46	GND
1A6 [12	45	1B6
1A7 [13	44	187
1A8 [14	43] 1B8
2A1 [15	42] 2B1
2A2 [16] 2B2
2A3 [17	40] 2B3
GND [18		GND
2A4 [19	38	2B4
2A5 []	20	37] 2B5
2A6 🛛	21] 2B6
V _{CC}		35] ∨ _{cc}
2A7 🛛		34] 2B7
2A8 []] 2B8
GND [] GND
2SAB[2SBA
2CAB			2CBA
2GAB [28	29	2GBA
			•

54ACT16652 WD PACKAGE
74ACT16652 DL PACKAGE
16-BIT REGISTERED TRANSCEIVERS
(TOP VIEW)

1012 (D 132)	
1GAB 1 56 1GB	
1CAB 2 55 1CBA	
1SAB [] 3 54 [] 1SBA	١.
GND 4 53 GND	
1A1 🛛 5 52 🗎 1B1	
1A2 [] 6 51 [] 1B2	
V _{CC} [] 7 50 [] V _{CC}	
1A3 🛛 8 49 🗍 1B3	
1A4 🛛 9 48 📗 1B4	
1A5 🛛 10 47 🗍 1B5	
GND 1 1 46 GND	
1A6 🛮 12 45 🗓 1B6	
1A7 🛛 13 44 🗍 1B7	
1A8 🛛 14 43 🗍 1B8	
2A1 🛛 15 42 🗍 2B1	
2A2 🛛 16 41 🗍 2B2	
2A3 🛛 17 40 🗍 2B3	
GND [] 18 39 [] GND	
2A4 🛛 19 38 🗓 2B4	
2A5 20 37 2B5	
2A6 21 36 2B6	
V _{CC} [22 35] V _{CC}	
2A7 23 34 2B7	
2A8 🛛 24 33 🗓 2B8	
GND 25 32 GND	
2SAB 26 31 2SBA	
2CAB 27 30 2CB/	
2GAB [28 29] 2GB/	

EAACAGET WD DACKAGE
54AC16657 WD PACKAGE
74AC16657 DL PACKAGE
16-BIT BUS TRANSCEIVERS
WITH PARITY
(TOP VIEW)

	,	• • • •	,
1 OE	1 U	56]1T/R
NC [2	55	10DD/EVEN
1 ERROR	3	54	1 PARITY
GND 🗍	4	53	GND
140	5	52	1B0
1A1 🗌	6	51]1B1
V _{cc} □	7	50]v _{cc}
1A2 [8	49]1B2
1A3 [9	48]1B3
1A4	10	47]1B4
GND 🗌	11	46] GND
1A5 🗌	12	45]1B5
1A6 🗌	13	44]1B6
1A7 🗌	14	43]1B7
2A0 🗌	15	42] 2B0
2A1 🗌	16	41] 2B1
2A2 🗌	17	40] 2B2
GND [18	39] GND
2A3 🗌	19	38] 2B3
2A4 🗌	20	37] 2B4
2A5 🗌	21	36] 2B5
v _{cc} □	22	35] v _{cc}
2A6 🗌	23	34] 2B6
2A7 🗌	24	33] 2B7
GND 🗌	25	32] GND
2ERROR	26	31	2PARITY
NC [27	30	20DD/EVEN
20E	28	29] 2T/Ř

54ACT16657 ... WD PACKAGE 74ACT16657 ... DL PACKAGE 16-BIT BUS TRANSCEIVERS WITH PARITY (TOP VIEW)

1 OE [1 U	56]1T∕R̄
NC [2	55	10DD/EVEN
1ERROR	3	54	1PARITY
GND [4	53	GND
1A0 [5	52]1B0
1A1	6	51]1B1
V _{CC} □	7	50	□ v _{cc}
1A2	8	49]1B2
1A3 [9	48] 1B3
1A4 [10	47]1B4
GND [11	46	GND
1A5 🗌	12	45	☐1B5
1A6	13	44	☐1B6
1A7	14	43]1B7
2A0 🗌	15	42	☐ 2B0
2A1	16	41	☐ 2B1
2A2	17	40	☐ 2B2
GND [18	39	GND
2A3 🗌	19	38	☐ 2B3
2A4 [20	37	☐ 2B4
2A5 🗌	21	36	□ 2B5
v _{cc} [22	35	□ v _{cc}
2A6 🗌	23	34	☐ 2B6
2A7 [24	33	☐ 2B7
GND [25	32	GND
2ERROR	26	31	2PARITY
NC [27	30	20DD/EVEN
20E	28	29	∏ 2T ∕ R̄

54AC16821, 54A WD PAC 74AC16821, 74A DL PAC 20-BIT D-TYPE (TOP V	KAGE ACT16821 KAGE FLIP-FLOPS	54AC16822, 54ACT16822 WD PACKAGE 74AC16822, 74ACT16822 DL PACKAGE 20-BIT D-TYPE FLIP-FL((TOP VIEW)	WD PA 2 74AC16823, 7 DL PA OPS 18-BIT D-TYF	4ACT16823 ACKAGE 4ACT16823 CKAGE PE FLIP-FLOPS VIEW)
10E	56 1 1 CLK 55 1 D1 54 1 D2 53 GND	10Ē	10E 2 2 1Q1 3	56 1 1 CLK 55 1 1 CLKEN 54 1 1 D1 53 1 GND
1Q3 5 1Q4 6 V _{CC} 7	52 1D3 51 1D4 50 V _{CC}	1Q3 5 52 1D 1Q4 6 51 1D V _{CC} 7 50 V _C	i3 1Q2 ☐5 i4 1Q3 ☐6	53 GND 52 1D2 51 1D3 50 V _{CC}
1Q5	49 1D5 48 1D6 47 1D7	1Q5	5 1Q4 ☐8 6 1Q5 ☐9 7 1Q6 ☐10	49 1 D4 48 1 D5 47 1 D6
GND	46 GND 45 1D8 44 1D9 43 1D10	GND	8 1Q7 🗆 12 9 1Q8 🔲 13	46 GND 45 1D7 44 1D8 43 1D9
2Q1	42 2D1 41 2D2 40 2D3	2Q1 15 42 2Ē 2Q2 16 41 2Ē 2Q3 17 40 2Ē	01 2Q1	42 2D1 41 2D2 40 2D3
GND [] 18 2Q4 [] 19 2Q5 [] 20 2Q6 [] 21	39 GND 38 2D4 37 2D5 36 2D6	GND []18 39	04 2Q4 19 05 2Q5 20	39
V _{CC}	35 V _{CC} 34 2D7 33 2D8	V _{CC}	cc V _{CC} 22 07 207 23	35 V _{CC} 34 2D7 33 2D8
GND 25 2Q9 26 2Q10 27 2OE 28	32 GND 31 2D9 30 2D10 29 2CLK	GND	$ \overline{0}9 $ $ \overline{0}10 $ $ \overline{0}10 $ $ \overline{0}20\overline{0} $ $ \overline{0}27 $	32 GND 31 2D9 30 2CLKEN 29 2CLK

54AC16824, 54ACT16824 ... WD PACKAGE 74AC16824, 74ACT16824 ... DL PACKAGE 18-BIT D-TYPE FLIP-FLOPS (TOP VIEW)

	•		
1CLR	1 5	56]1CLK
10E	2	55	1 CLKEN
1Q1[]3	54]1D1
GND [4	53] GND
1Q2 [5	52]1D2
1Q3 [] 6	51]1D̄3
V _{CC} [7	50] v _{cc}
1Q4 []8	49]1D4
1Q5 [9	48]1D̄5
1Q6 [10	47]1D̄6
GND []11	46] GND
1Q7 [12	45] 1 D̄ 7
1Q8 [13	44]1D̄8
1Q9 [14	43]1D9
2Q1[15	42] 2D1
2Q2 [16	41] 2D2
2Q3 [17	40] 2D̃3
GND [18	39] GND
2Q4 [19	38] 2D4
2Q5 [20	37	2D5
2Q6 [21	36	2D6
V _{CC}	22	35	V _{CC}
2Q7 [23	34] 2D7
2Q8 [24	33] 2D̄8
GND [25	32	GND
2Q9 [26	31	2D9
20E [27	30	2CLKEN
2CLR	28	29] 2CLK

'AC16825, 'ACT16825 18-BIT BUS DRIVERS (TOP VIEW)

1	_	_	
1G1 [1	₅₆ し	1 <u>G2</u>
1Y1 🛭	2	55	
1Y2 [3	54	
GND	4	53	GND
1Y3	5	52	
1Y4 [6	51	1A4
Vcc	7	50	
1Y5 [8	49	
1Y6 [9	48	
1Y6 [1Y7 [10	47	
GND [11	46	
1Y8 [12	45	
1Y8 [1Y9 [13	44	
GND [14	43	
GND [15	42	
	16	41	2A1
2Y1 (2Y2 (17	40	
GND [18	39	GND
2Y3 [19	38	GND 2A3
2Y4 [20	37	2A4
2Y5 [21	36	
Vcc [22	35	Vcc
2Y6 [23	34	2A6
2Y7 🛚	24	33	2A7
GND [25	32	GND 2A8
2Y8 🗓	26	31	2A8
2Y9 [27	30	2A9
2G1	28	29	2 G 2
7	L		

'AC16826, 'ACT16826 18-BIT BUS DRIVERS (TOP VIEW)

	$\neg \tau$	τ	
1G1 [1)	− 56 [1 <u>G2</u>
1Y1 [2	55	1A1
1Y2 [3	54	1A2
GND [4	53	
1Y3 [5	52	1A3
1Y4 [6	51	
Vcc [7	50	Vcc
1Y5	8	49	
176	9	48	
177	10	47	
GND	11	46	
178	12	45	
1Y9 [13		
		44	
GND [14	43	GND
GND [15	42	GND
2Y1 [16	41	2A1
2Y2 [GND [17	40	
GND [18	39	GND
2Y3 [19	38	
2Y4	20	37	2A4
2Y5 [21	36	2A5
	22	35	l Vcc
2Y6 [23	34	2A6
2Y7 GND	24	33	2A7
GND	25	32	
2Y8	26	31	2A8
2Y9	27	30	2A9
	28		2G2
2G1 [28	29	202

74AC/ACT16827 DL PACKAGE 54AC/ACT16827 WD PACKAGE 20-BIT BUS DRIVERS (TOP VIEW) 1G1	74AC/ACT16828 DL PACKAGE 54AC/ACT16828 WD PACKAGE 20-BIT BUS DRIVERS (TOP VIEW) 1G1	54AC16833, 54ACT16833 WD PACKAGE 74AC16833, 74ACT16833 DL PACKAGE 16-BIT BUS TRANSCEIVERS WITH PARITY (TOP VIEW) 1 OEB
2G1 <u>[28 29</u>] 2G2	2G1[<u>1</u> 28 29] 2G2	2ERR
		4 P

54AC16834, 54ACT16834 WD PACKAGE 74AC16834, 74ACT16834 DL PACKAGE 16-BIT BUS TRANSCEIVERS WITH PARITY	74AC/ACT16841 DL PACKAGE 54AC/ACT16841 WD PACKAGE 20-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)	74AC/ACT16842 DL PACKAGE 54AC/ACT16842 WD PACKAGE 20-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)
(TOP VIEW)	10E	10E
1CLK	GND	GND
1A1 ☐ 5 52 ☐ 1B1 1A2 ☐ 6 51 ☐ 1B2 Vcc ☐ 7 50 ☐ Vcc	V _{CC}	V _{CC} ☐ 7 50 ☐ V _{CC} 1Q5 ☐ 8 49 ☐ 1 D5
1A3 8 49 1B3 1A4 9 48 1B4 1A5 10 47 1B5	1Q6	1Q6
GND 11 46 GND 1A6 12 45 1B6	1Q8	1Q8
1A7	2Q1	2Q1 15 42 2D1 2Q2 16 41 2D2 2Q8 17 40 2D3
2A2	GND	GND ☐18 39 ☐ GND 2Q4 ☐19 38 ☐ 2D̄4
2A4 19 38 2B4 2A5 20 37 2B5 2A6 21 36 2B6	2Q5	2Q5
V _{CC} 22 35 V _{CC} 2A7 23 34 2B7	2Q7	2Q7
2A8	2Q9 26 31 2D9 2Q10 27 30 2D10 2OE 28 29 2C	2Q9
2CLK	SOF 1750 SATISE	2 0E

74AC/ACT16843 ... DL PACKAGE 54AC/ACT16843 ... WD PACKAGE 18-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)

1 CLR	1	U	56	∐1C
10E	2		55	1 PRE
1Q1	3		54	1D1
GND [4		53	GND
1Q2 🗌	5		52]1D2
1Q3 🗌	6		51]1D3
V _{CC} [7		50	□ v _{cc}
1Q4 🗌	8		49]1D4
1Q5 [9		48]1D5
1Q6 🗌	10		47]1D6
GND [11		46	GND
1Q7 🗌	12		45]1D7
1Q8 🗌	13		44]1D8
1 Q9 🗌	14		43	□1D9
2Q1	15		42] 2D1
2Q2 🗌	16		41	□ 2D2
2Q3 [17		40] 2D3
GND [18		39	GND
2Q4 🗌	19		38	☐ 2D4
2Q5 🗌	20		37	□ 2D5
2Q6 [21		36	2D6
V _{CC} □	22		35	□ ^v cc
2Q7 🗌	23		34	2D7
2Q8 🗌	24		33	□ 2D8
GND [25		32	GND
2Q9 [26		31	2D9
20E	27		30	2PRE
2CLR	28		29] 2C

74AC/ACT16844 ... DL PACKAGE 54AC/ACT16844 ... WD PACKAGE 18-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS (TOP VIEW)

1 CLR	1 U	56]1C
10E [2	55	1 PRE
1Q1 🗌	3	54]1D1
GND [4	53	GND
1Q2 🗌	5	52	1D2
1Q3 🗌	6	51] 1 D̄ 3
V _{cc} □	7	50] V _{CC}
1Q4 🗌	8	49]1D4
1Q5 🗌	9	48] 1 D̄ 5
1Q6 🗌	10	47]1D̄6
GND [11	46	GND
1Q7 🗌	12	45] 1 D̄ 7
1Q8 🗌	13	44] 1 D̄8
1Q9 🗌	14	43] 1 D̄ 9
2Q1 [15	42] 2D1
2Q2 [16	41	2D2
2Q3 🗌	17	40	2D̄3
GND [18	39	GND
2Q4 🗌	19	38	2D4
2Q5 🗌	20	37	2D̄5
2Q6 🗌	21	36	2D6
V _{CC} [22	35] V _{CC}
2Q7 🗌	23	34	2D7
2Q8 🗌	24	33	2D8
GND [25	32	GND
2Q9 🗌	26	31	2D̄9
20E	27	30	2PRE
2CLR	28	29] 2C

54AC16853, 54ACT16853 ... WD PACKAGE 74AC16853, 74ACT16853 ... DL PACKAGE DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS (TOP VIEW)

	•	•
1 OEB	di C	756 10EA
1EN	□ 2	55 1 CLR
1 ERR	 3	54 1PARITY
GND	□ 4	53 GND
1A1	 □5	52 🗌 1 B 1
1A2	∐ 6	51 🗌 1B2
Vcc	□ 7	50∏ V _{CC}
1A3	[]8	49 🗌 1 B 3
1A4	□ 9	48 🗌 1 B 4
1A5	∐ 10	47 🗌 1B5
GND	[]11	46 🗌 GND
1A6	12	45 🗌 1B6
1A7	13	44 🗌 1 B 7
1A8	14	43 🗌 1B8
2A1	15	42 🗌 2B1
2A2	□16	41 🗌 2B2
2A3	[]17	40∏ 2B3
GND	□18	39 🗌 GND
2A4	1 19	38 🗌 2B4
2A5	20	37 🗌 2B5
2A6	21	36 🗌 2B6
vcc	22	35□ V _{CC}
2A7	23	34 🗌 2B7
2A8	24	33 🗌 2B8
GND	25	32 GND
2ERR	□26	31 2PARITY
2EN	27	30 2CLR
20EB	28	29 20EA

74AC/ACT16854 DL PACKAGE			
54AC/ACT16854 WD PACKAGE			
DUAL 8-BIT TO 9-BIT PARITY			
BUS TRANSCEIVERS			
(TOP VIEW)			

_			
10EB [1 U	56	1 OEA
1 EN	2	55	1CLR
1 ERR	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
	6	51	1B2
	7	50	V _{CC}
	8	49	☐ 1B3
	9	48	
	10	47	1B5
	11	46	GND
	12	45]1B6
	13	44]1B7
	14	43	
	15	42	_ 188 72B1
	16	41	2B1 □2B2
-		· · · · · ·	
	17	40	2B3
	18	39	GND
	19	38	_ 2B4
	20	37	_ 2B5
2A6 🗌	21	36	2B6
V _{CC}	22	35	$]$ V_{CC}
2A7 🗌	23	34	2B7
2A8 🗍	24	33] 2B8
GND 🗌	25	32	GND
2ERR	26	31	2PARITY
	27	30	2CLR
	28	29	20EA
4		ٽ	

54AC16861, 54ACT16861
WD PACKAGE
74AC16861, 74ACT16861
DL PACKAGE
20-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

_		
1GAB	ı U	56∐1ĞBA
1B1[2	55 1A1
1B2[3	54 1A2
GND[4	53 GND
1B3[5	52 1A3
1B4[6	51 1A4
v _{cc} □	7	50 \ V _{CC}
1B5	8	49 1A5
1B6	9	48 1A6
1B7	10	47 1A7
GND	11	46 GND
1B8[12	45 1A8
1B9[13	44 🗌 1 A 9
1B10	14	43 1A10
2B1[15	42 2A1
2B2[16	41 2A2
2B3[17	40 2A3
GND[18	39∏GND
2B4[19	38 2A4
2B5[20	37 2A5
2B6[21	36 2A6
V _{cc} [22	35∏V _{CC}
2B7[23	34 2A7
2B8[24	33 2A8
GND	25	32 GND
2B9[26	31 2A9
2B10[27	30 2A10
2ĞAB□	28	29 2 GBA

54AC16862, 54ACT16862 ... WD PACKAGE 74AC16862, 74ACT16862 ... DL PACKAGE 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

(101 11211)				
1GAB	1	56	1 GBA	
1 B1	2	55	1A1	
1B2	3	54	1A2	
GND	4	53	GND	
1B3[5	52	1A3	
184	6	51	1A4	
v _{cc} [7	50	V _{CC}	
1B5	8	49	1A5	
1B6[9	48	1A6	
1B7[10	47	1A7	
GND[11	46	GND	
1 B8	12	45	1A8	
1B9[13	44	1A9	
1B10	14	43	1A10	
2B1	15	42	2A1	
2B2[16		2A2	
2B3[17	40	2A3	
GND[18		GND	
2B4	19	-	2A4	
2B5[20	37	2A5	
2B6[21	-	2A6	
V _{cc} [22	35	v_{cc}	
2B7[23		2A7	
2B8[24	-	2A8	
GND	25	-	GND	
2B9[26		2A9	
2B10[27		2 <u>A</u> 10	
2GAB	28	29	2ĞBA	

54AC16863, 54ACT16863
WD PACKAGE
74AC16863, 74ACT16863
DL PACKAGE
18-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

(TOP VIEW)			
1ĞAB∏	1 0	56	∏1 GBA
1B1	2	55	1A1
1B2	3	54	∏1A2
GND	4	53	GND
1B3	5	52	1A3
1B4[6	51]1A4
Vcc□	7	50	□v _{cc}
1B5	8	49]1A5
1B6[9	48]1A6
1B7[10	47]1A7
GND[11	46]GND
1B8[12	45]1A8
1B9[13	44	□1A9
GND□	14	43]GND
GND□	15	42	□GND
2B1[16	41]2A1
2B2[17	40]2A2
GND	18	39	□GND
2B3	19	38] 2A3
2B4[20	37]2A4
2B5[21	36]2A 5
V _{cc} □	22	35	□v _{cc}
2B6[23	34]2A6
2B7[24	33	□2A7
GND□	25	32	GND
2B8[26	31]2A8
2B9[27	30]2 <u>A</u> 9
2GAB	28	29	∏2ĞBA

54AC16864, 54ACT16864
WD PACKAGE
74AC16864, 74ACT16864
DL PACKAGE
18-BIT BUS TRANSCEIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

-		
1GAB	1	56∐1ĞBA
1 B 1	2	55 1A1
1B2	3	54[]1A2
GND	4	53 GND
1B3	5	52 1A3
1B4[6	51 1A4
V _{CC} [7	50∏V _{CC}
1B5	8	49 1A5
1B6[9	48 🗌 1 A 6
1B7[10	47 🗌 1 A 7
GND	11	46∏GND
1B8	12	45 🗌 1 A 8
1B9[13	44 🗌 1 A 9
GND	14	43 GND
GND	15	42 GND
2B1[16	41 2A1
2B2	17	40 2A2
GND	18	39∏GND
2B3	19	38 2A3
2B4[20	37 2A4
2B5[21	36 2A5
V _{cc} [22	35 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
2B6[23	34 2 46
2B7[24	33 2A7
GND	25	32 GND
2B8[26	31 2A8
2B9	27	30 2A9
2GAB	28	29 2GBA

54AC16952, 54ACT16952... WD PACKAGE 74AC16952, 74ACT16952... DL PACKAGE 16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

1 OEAB	10	56	1 OEBA
1 CLKAB [2	55	1CLKBA
1 CEAB	3	54	1 CEBA
GND [4	53] GND
1A1	5	52]1B1
1A2 [6	51]1B2
V _{cc} [7	50] v _{cc}
1A3 🗌	8	49]1B3
1A4 [9	48]1B4
1A5 [10	47] 1 B5
GND [11	46] GND
1A6 🗌	12	45]1B6
1A7 🗌	13	44	1B7
1A8 🗌	14	43]1B8
2A1	15	42	2B1
2A2 [16	41	2B2
2A3 [17	40	2B3
GND	18	39	GND
2A4 [19	38	2B4
2A5 🛚	20	37	2B5
2A6	21	36	」2B6
V _{CC}	22	35	_ v _{cc}
2A7 [23	34	2B7
2A8 [24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

54AC16953, 54ACT16953...
WD PACKAGE
74AC16953, 74ACT16953...
DL PACKAGE
16-BIT REGISTERED BUS
TRANSCEIVERS WITH 3-STATE
OUTPUTS
(TOP VIEW)

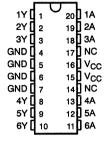
,	IOP V	IE VV	,
10EAB	10	56	1 OEBA
CLKAB	2	55	11CLKBA
1 CEAB	3	54	1 CEBA
GND	4	53	GND
1A1	15	52	1B1
1A2 T	6	51	П 1В2
v _{cc} [7	50	5ν _{cc}
1A3	8	49	11B3
1A4 [9	48	П 1В4
1A5 [10	47	☐1B5
GND []11	46	GND
1A6 [12	45	1B6
1A7	13	44	1B7
1A8 [14	43	_ 1B8
2A1[15	42	2B1
2A2 [16	41] 2B2
2A3 [17	40	☐ 2B3
GND [18	39	GND
2A4 [19	38	2B4
2A5 [20	37	☐ 2B5
2A6 [21	36	□ 2B6
V _{CC}	22	35	□ v _{cc}
2A7	23	34	☐ 2B7
2A8 🗌	24	33	☐ 2B8
GND [25	32	GND
2CEAB	26	31	2CEBA
CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

CLOCK DRIVERS

SN74ABT3337 ... DW OR N PACKAGE CLOCK DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

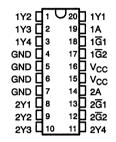
Y3 ∏1 GND 2 19 GND Y4 ∏3 18 Y1 V_{CC} □4 17 Vcc 16 CLK ē ∏5 15 GND CLR C Усс П7 14 Vcc Q4 🛮 8 13 Q1 GND TIS 12 GND Q3 🛮 10 11 Q2

74AC11204 ... DW OR N PACKAGE HEX INVERTERS/CLOCK DRIVERS (TOP VIEW)

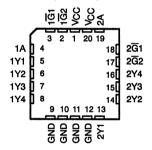


54AC/ACT11208 ... J PACKAGE 74AC/ACT11208 ... DW OR N PACKAGE

DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)



54AC/ACT11208 ... FK PACKAGE DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

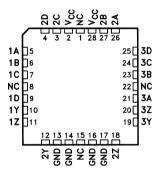


54AC/ACT11800 ... JT PACKAGE 74AC/ACT11800 ... DW OR NT PACKAGE

TRIPLE 4-INPUT AND/NAND CLOCK DRIVERS (TOP VIEW)

1 D 🛮 1	U24]1C
1Y 🛮 2	23] 1 B
1Z 🛮 3	22	□1A
2Y 🛚 4	21] 2D
GND ☐5	20] 2C
GND ☐6	19	□ v _{cc}
GND 🔲 7	18	□ v _{cc}
GND □8	17	☐ 2B
2Z 🗌 9	16] 2A
3Y []10) 15] 3D
3Z 🛮 11	14] 3C
3A 🗌 12	2 13] 3B

54AC/ACT11800 ... FK PACKAGE TRIPLE 4-INPUT AND/NAND CLOCK DRIVERS (TOP VIEW)

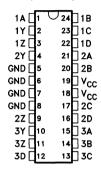


CLOCK DRIVERS (continued)

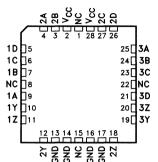
54AC/ACT11802 ... JT PACKAGE 74AC/ACT11802 ... DW OR NT PACKAGE

TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS

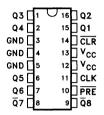
(TOP VIEW)



54AC/ACT11802 ... FK PACKAGE TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS (TOP VIEW)



74AS303 ... D† OR N PACKAGE OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS (TOP VIEW)



†CONTACT FACTORY FOR INFORMATION ON AVAILABILITY OF S.O. PACKAGE.

SN74AS304 ... D OR N PACKAGE OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS

(TOP VIEW)

Q3 🗌	1	O 16	Q2
Q4 [2	15] Q1
GND [3	14	CLR
GND [4	13	□ v _{cc}
GND [5	12	□ v _{cc}
Q5 🗌	6	11	CLK
Q6 🗌	7	10	PRE
Q7 🛚	8	9	Q8

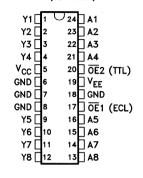
74AS305 ... D OR N PACKAGE OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS

(TOP VIEW)

Q3 [ī	U 16	Q2
Q4 [2	15	□ Q1
GND [3	14	CLR
GND [4	13	□v _{cc}
GND [5	12	□ v _{cc}
Q5 [6	11	CLK
Q6 [7	10	PRE
ō7 ۲	8	9	Пōв

ECL

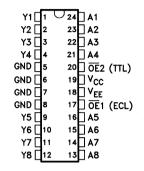
SN10KHT5538 DW OR NT PACKAGE		
SN100KT5538 DW OR NT PACKAGE		
OCTAL ECL-TO-TTL TRANSLATORS		
WITH OPEN-COLLECTOR OUTPUTS		
(TOP VIEW)		



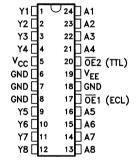
SN10KHT5539 ... DW OR NT PACKAGE SN100KT5539 ... DW OR NT PACKAGE OCTAL ECL-TO-TTL TRANSLATORS WITH OPEN COLLECTOR OUTPUTS (TOP VIEW)

		_		
Y1 🗌	1	24	A1	
Y2 🛚	2	23	A2	
Y3 🗌	3	22	_ A3	
Y4 🗌	4	21	A4	
V _{CC} □	5	20	OE2	(TTL)
GND [6	19] V _{EE}	
GND [7	18	GND	
GND [8	17	OE1	(ECL)
Y5 🗌	9	16	_ A5	
Y6 🗌	10	15] A6	
Y7 🛚	11	14	_ A7	
Y8 🗌	12	13	8A [

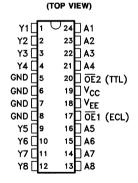
SN10KHT5540 ... DW OR NT PACKAGE SN100KT5540 ... DW OR NT PACKAGE OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS (TOP VIEW)



SN10KHT5541 ... DW OR NT PACKAGE SN100KT5541 ... DW OR NT PACKAGE OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS (TOP VIEW)



SN10KHT5542, SN10KHT5543 ...
DW OR NT PACKAGE
SN100KT5542, SN100KT5543 ...
DW OR NT PACKAGE
OCTAL TTL-TO-ECL TRANSLATORS
WITH OUTPUT ENABLE



SN10KHT5562, SN100KT5562...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

A1 1 24 B1 A2 2 23 B2 A3 3 22 B3	
47 Hz 00 H DZ	
A3 □3 22 □ B3	
A4 🛮 4 21 🗒 B4	
V _{CC}	A
GND [6 19] V _{EI}	Ε
GND []7 18 [] GN	C
GND []8 17 [] ḠA	E
A5 ☐9 16 ☐ B5	
A6 ☐10 15 ☐ B6	
A7 🛮 11 14 🗎 B7	
A8 12 13 B8	

ECL (continued)

SN10KHT5563, SN100KT5563 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

_		
A1 🛛 1	O 24	□ B1
A2 🔲 2	23] B2
A3 ∏3	22	∏ B3
A4	21	□ B4
V _{CC} ☐5	20	GBA
GND 🛮 6	19	VEE
GND 🛮 7	18	GND
GND 🗌	17	ŪĞAB
A5 🗌 9	16	_ B5
A6 ∐1	0 15	В6
A7 🛮 1	1 14	_B7
A8 🛮 1	2 13	□ B8

SN10KHT5564, SN100KT5564 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

A1 [1	24 🗌 B1
A2 🗌	2	23 🗌 B2
A3 [3	22 🗌 B3
A4 [4	21 🗌 B4
V _{cc} [5	20 🗌 DIR
GND [6	19 🗌 V _{EE}
GND [7	18 GND
GND [8	17 🗌 G
A5 [9	16 🗌 B5
A6 [10	15 🗌 B6
A7 [11	14 🗌 B7
A8 [12	13 B8

SN10KHT5565, SN100KT5565 ...
DW OR NT PACKAGE
OCTAL TTL/ECL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

A1 🔲 1	Ú 24∏ B1
A2 □2	23 🗌 B2
A3 ∏3	22 🗌 B3
A4	21 🗌 B4
V _{CC} ☐5	20 🗌 DIR
GND ☐6	19∏ V _{EE}
GND ∏7	18 GND
GND □8	17 🛮 Ğ
A5 ∏9	16 🗌 B5
A6 ☐10) 15∐B6
A7 🛮 11	14∏B7
A8 ∏12	2 13 B8

SN10KHT5573, SN100KT5573...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS
WITH D-TYPE TRANSPARENT
LATCHES AND 3-STATE OUTPUTS
(TOP VIEW)

1Q 🔲 1	¹
2Q 🔲 2	23 🗌 2D
3Q []3	22 🗍 3D
4Q 🛮 4	21 🗌 4D
V _{CC}	20 ☐ OE (TTL)
GND 🗌 6	19 V _{EE}
GND 🛮 7	18 🗌 GND
GND ☐8	17 \(\overline{LE} (ECL)
5Q 🗌 9	16 🗌 5D
6Q 🛮 10	15 🗌 6D
7Q 🛮 11	14 🗌 7D
8Q 🗌 12	13 🗌 8D

SN10KHT5574, SN100KT5574...
DW OR NT PACKAGE
OCTAL ECLTO-TTL TRANSLATORS
WITH D-TYPE EDGE-TRIGGERED FLIPFLOPS AND 3-STATE OUTPUTS
(TOP VIEW)

10 1	J24
2Q 🛮 2	23 2D
3Q	22 🗌 3D
4Q 🗌 4	21 🗌 4D
V _{CC}	20 ☐ OĒ (TTL)
GND ☐6	19 V _{EE}
GND 🔲 7	18 GND
GND ☐8	17 CLK (ECL)
5Q ∏ 9	16 🗌 5 D
6Q 🔲 10	15 🛚 6D
7Q 🛮 11	14 🗌 7D
8Q ∏ 12	13 8D

SN10KHT5575, SN100KT5575 ...
DW OR NT PACKAGE
OCTAL ECL-TO-TTL TRANSLATORS
WITH D-TYPE TRANSPARENT
LATCHES AND 3-STATE OUTPUTS
(TOP VIEW)

1Q [1	24]1D
2Q 🛚	2	23] 2D
3Q 🗀	3	22] 3D
4Q 🗌	4	21] 4D
V _{CC} □	5	20	OE (TTL)
GND [6	19] V _{EE}
GND [7	18] GND
GND [8	17	LE (ECL)
5Q 🛚	9	16]5D
6Q 🗀	10	15] 6D
7Q [11	14] 7D
8Q [12	13]8D

ECL (continued)

SN10KHT5576, SN100KT5576...

DW OR NT PACKAGE

OCTAL ECL-TO-TTL TRANSLATORS
WITH D-TYPE TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

(TOP VIEW)

SN10KHT5578, SN100KT5578...
DW OR NT PACKAGE
OCTAL TTL-TO-ECL TRANSLATORS
WITH D-TYPE EDGE-TRIGGERED FLIPFLOPS AND OUTPUT ENABLE
(TOP VIEW)

1Q □ 1	[∨] 24∏1D
2Q 🔲 2	23 🗌 2D
3Q 🛮 3	22 🗌 3D
4Q 🛮 ₄	21 🗌 4D
V _{CC}	20 ☐ ŌĒ (TTL)
GND ☐6	19 ∨ _{EE}
GND 🛮 7	18 GND
GND ☐8	17 CLK (ECL)
5Q ∏9	16 5D
6Q 🔲 10	15 🗌 6D
7Ō 🛮 11	14 🗌 7D
8Q ∐12	13 🗌 8D

_			
1Q 🛚	1 0	24]1D
2Q 🗌	2	23] 2D
3Q 🔲	3	22] 3D
4Q 🗌	4	21	4D
GND 🗌	5	20	OE (ECL)
GND 🗌	6	19] V _{CC}
GND 🗌	7	18] v _{ee}
GND [8	17	CLK (TTL)
5Q 🗌	9	16]5D
6Q 🗌	10	15]6D
7Q 🛚	11	14]7D
8Q 🔲	12	13] 8D

FIFO

SN74ALS229B ... DW OR N PACKAGE 16 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES (TOP VIEW)

	_	_	
OE [1 U	20	V _{CC}
FULL-2	2	19	EMPTY+2
FULL [3	18	UNCK
LDCK [4	17	EMPTY
D0 🗌	5	16	Q0
D1 [6	15	Q1
D2 [7	14	Q2
D3 [8	13	Q3
D4 [9	12	Q4
GND [10	11	RST

SN74ALS232B ... DW OR N PACKAGE 16 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY (TOP VIEW)

OE 1 FULL 2	U ₁₆	V _{CC}
LDCK 3	14	EMPTY
DO []4	13	QO
D1 🛚 5	12	Q1
D2 🛛 6	11	□ Q2
D3 🔲 7	10	□ Q3
GND ☐8	9	RST

SN74ALS233B ... DW OR N PACKAGE 16 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES (TOP VIEW)

_			
OE 🔲	1 0	20	v_{cc}
FULL-1	2	19	EMPTY+1
FULL []	3	18	UNCK
LDCK 🔲	4	17	EMPTY
D0 🗍	5	16	Q0
D1 🔲	6	15	Q1
D2 🔲	7	14	Q2
D3 🔲	8	13	Q3
D4 []:	9	12	Q4
GND □	10	11	RST

SN54ALS234 ... J PACKAGE SN74ALS234 ... DW OR N PACKAGE 64 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY (TOP VIEW)

ŌE [1	U 16	□ v _{cc}
IR [2	15] ѕні́гт о∪т
SHIFT IN	3	14	OR
D0 [4	13	□ Q 0
	5	12	□ Q1
	6	11] Q2
D3 [GND [7	10	□ Q 3
GND [8	9	☐ RST

SN54ALS235 ... J PACKAGE SN74ALS235 ... DW OR N PACKAGE 64 x 5 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY (TOP VIEW)

ŌE 🛘	1 U	20] V _{cc}
HALF FULL	2	19	ALMOST FULL/EMPTY
IR□	3	18	SHIFT OUT
SHIFT IN	4	17] or
D0 🗆	5	16] Q0
D1 🛚	6	15] Q1
D2 🗌	7	14] Q2
D3 [8	13] Q3
D4 🗌	9	12] Q4
GND 🗌	10	11	RST

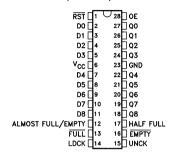
SN54ALS236 ... J PACKAGE SN74ALS236 ... DW OR N PACKAGE 64 x 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY (TOP VIEW)

NC [1 U	16	V _{cc}
IR 🗌	2	15] SHIFT OUT
SHIFT IN	3	14	OR
D0 [4	13] Q0
D1 [5	12]Q1
D2 [6	11] Q2
D3 [7	10] Q3
GND 🗌	8	9	RST

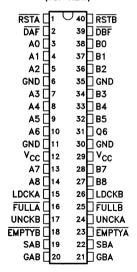
SN74ALS2232A	. NT	PACI	(AGE
64 x 8 ASYNCHRO	NOU	S FIR	ST-IN
FIRST-OUT	MEM	ORY	
(TOP V	IEW)		

RST 🗌	1	24	OE
D0 🗌	2	23	Q0
D1 🛚	3	22	Q1
D2 🗌	4	21	Q2
D3 🗌	5	20	Q3
v _{cc} □	6	19	GND
D4 [7	18	Q4
D5 🗌	8	17	Q5
D6 🗌	9	16	Q6
D7 🗌	10	15	Q7
FULL [11	14	EMPTY
LDCK [12	13	UNCK

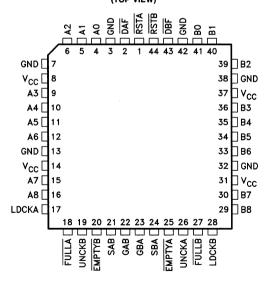
SN74ALS2233A ... N PACKAGE 64 x 9 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORY (TOP VIEW)



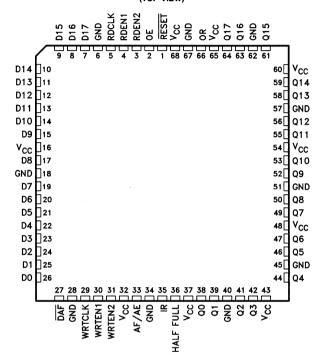
SN74ALS2238 ... N PACKAGE 32 x 9 x 2 ASYNCHRONOUS BIDIRECTIONAL FIRST-IN FIRST-OUT MEMORY (TOP VIEW)



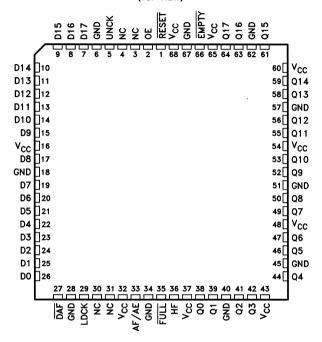
SN74ALS2238 ... FN PACKAGE
32 x 9 x 2 ASYNCHRONOUS BIDIRECTIONAL
FIRST-IN FIRST-OUT MEMORY
(TOP VIEW)



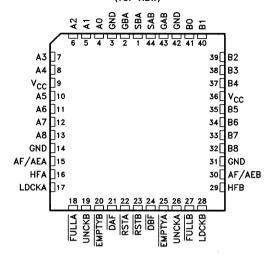
SN74ACT7801 ... FN PACKAGE 1024 x 18 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY (TOP VIEW)



SN74ACT7802 ... FN PACKAGE 1024 x 18 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY (TOP VIEW)



SN74ACT2235 ... FN PACKAGE 1024 x 9 x 2 ASYNCHRONOUS FIRST-IN-FIRST-OUT MEMORY (TOP VIEW)



MEMORY DRIVERS

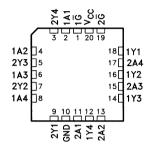
SN54ALS2240 ... J PACKAGE SN74ALS2240 ... DW OR N PACKAGE

SN54ALS2241 ... J PACKAGE SN74ALS2241 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

4 <u>2</u> H	. (Jaah v
1Ğ 🗌	1 ~	⁷²⁰ ∐ V _{CC}
1A1 🗌	2	19 🗌 2 🖥
2Y4 🗌	3	18 🗌 1Y1
1A2 🗌	4	17 🗌 2A4
2Y3 🗌	5	16 🗌 1 Y 2
1A3 🗌	6	15 🗌 2A3
2Y2 🗌	7	14 🗌 1 Y 3
1A4 🗌	8	13 2A2
2Y1 🗌	9	12 1Y4
GND [10	11 2A1

SN54ALS2240 ... FK PACKAGE

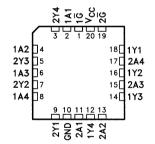
SN54ALS2241 ... J PACKAGE SN74ALS2241 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)



SN54ALS2244 ... J PACKAGE SN74ALS2244 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)



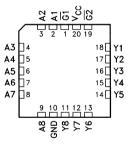
SN54ALS2244 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/
MOS DRIVERS WITH 3-STATE
OUTPUTS
(TOP VIEW)



SN54ALS2540, SN54ALS2541 ... J PACKAGE SN74ALS2540, SN74ALS2541 ... DW OR N PACKAGE (TOP VIEW)

G1 [1	U ₂₀	b v _{cc}
A1 [2	19	☐ <u>G2</u>
A2 [3	18] Y1
A3 [4	17] Y2
A4 [5	16] Y3
A5 [6	15] Y4
A6 [7	14] Y5
A7 [8	13] Y6
A8 [9	12] Y7
GND [10	11] Y8

SN54ALS2540, SN54ALS2541 ... FK PACKAGE (TOP VIEW)



MEMORY DRIVERS (continued)

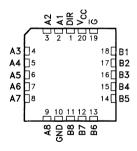
SN54AS2620, SN74AS2620 SN54AS2623, SN74AS2623 OCTAL BUS TRANSCEIVERS/MOS DRIVERS

SN54AS' ... J PACKAGE SN74AS' ... DW OR N PACKAGE (TOP VIEW)

04D -	Uash.	V
GAB 🔲 1	○ 20 🔲	v_{cc}
A1	19	ĞΒΑ
A2 🗌 3	18	B1
A3 🗌 4	17	B2
A4 🗌 5	16 🗌	B3
A5 ∏6	15]	B4
A6 ∐7	14	B5
A7 🛮 8	13	В6
A8	12	B7
GND 11	11	B8

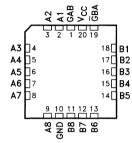
SN54AS2640, SN74AS2640 SN54AS2645, SN74AS2645 OCTAL BUS TRANSCEIVER/ MOS DRIVER

SN54AS' ... FK PACKAGE
(TOP VIEW)



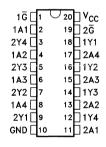
SN54AS2620, SN74AS2620 SN54AS2623, SN74AS2623 OCTAL BUS TRANSCEIVERS/MOS DRIVERS

SN54AS' ... FK PACKAGE (TOP VIEW)



SN54BCT2240 ... J PACKAGE SN74BCT2240 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS

(TOP VIEW)

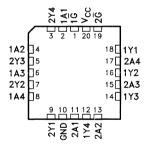


SN54AS2640, SN74AS2640 SN54AS2645, SN74AS2645 OCTAL BUS TRANSCEIVER/ MOS DRIVER

SN54AS' ... J PACKAGE SN74AS' ... DW OR N PACKAGE (TOP VIEW)

DIR [1	¹ 20 1 V _{CC}
A1 [2	19∏ Ĝ
A2 [3	18 🗌 B1
A3 [4	17 🗌 B2
A4 [5	16 🗌 B3
A5 [6	15 🗌 B4
A6 [7	14 🗀 B5
A7 [8	13∏ B6
A8 [9	12 🗌 B7
GND [10	11 B8

SN54BCT2240 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/
MOS DRIVERS WITH 3-STATE
OUTPUTS
(TOP VIEW)

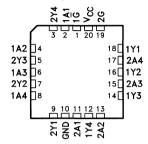


MEMORY DRIVERS (continued)

SN54BCT2241 ... J PACKAGE SN74BCT2241 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

1Ē [[1	∪ ₂₀ v _{cc}
1A1 🗆 2	19 🛘 2G
2Y4 🗌 3	18 🗌 1 Y 1
1A2 🛚 4	17 2A4
2Y3 🛚 5	16 🗌 1 Y 2
1A3 ∏6	15 🗌 2A3
2Y2 🔲 7	14 🗌 1 Y 3
1A4 🏻 8	13 🗌 2A2
2Y1 🛮 9	12 1Y4
GND ☐10	11 2A1

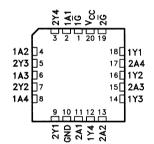
SN54BCT2241 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/
MOS DRIVERS WITH 3-STATE
OUTPUTS
(TOP VIEW)



SN54BCT2244 ... J PACKAGE SN74BCT2244 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS/ MOS DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

_			
1Ē [ı	20 🗌 '	Vcc
1A1 🗌	2	19]	2Ġ
2Y4 🗌	3	18 🛚 '	IY1
1A2 🗌	4	17 🗀 :	2A4
2Y3 🗌	5	16	1Y2
1A3 🗌	6	15 🛚 🖯	2A3
2Y2 🗌	7	14 🛚 1	1 Y 3
1A4 🗍	8	13 🛚 :	2A2
2Y1 🗌	9	12	1 Y 4
GND ☐	10	11]]	2A1

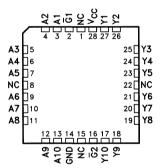
SN54BCT2244 ... FK PACKAGE
OCTAL BUFFERS AND LINE DRIVERS/
MOS DRIVERS WITH 3-STATE
OUTPUTS
(TOP VIEW)



SN54BCT2827A, SN54BCT2828A ...
JT PACKAGE
SN74BCT2827A, SN74BCT2828A ...
DW OR N PACKAGE
8-BIT BUS/MOS MEMORY DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)

Ğ1 [1	724 □ V _{CC}
A1 [2	23 🗌 Y1
A2 [3	22 🗌 Y2
A3 [4	21 🗌 Y3
A4 [5	20 🗌 Y4
A5 [6	19 🗌 Y5
A6 [7	18 🗌 Y6
A7 [8	17 Y7
A8 [9	16 Y8
A9 🗌	10	15 Y9
A10 [11	14 Y10
GND [12	13 \ \ \bar{G}2

SN54BCT2827A, SN54BCT2828A ...
FK PACKAGE
8-BIT BUS/MOS MEMORY DRIVERS
WITH 3-STATE OUTPUTS
(TOP VIEW)



MEMORY DRIVERS (continued)

SN54BCT2410 JT PACKAGE
SN74BCT2410 NT PACKAGE
11-BIT MOS MEMORY DRIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

SN54BCT2411 JT PACKAGE
SN74BCT2411 NT PACKAGE
11-BIT MOS MEMORY DRIVERS WITH
3-STATE OUTPUTS
(TOP VIEW)

A1 [1 6	28 🔲 /	46
A2 [2	27]	47
A3 [3	26]	48
A4 [4	25]	۹9
A5 [5	24] /	410
Ğ1 [6	23]	411
V _{CC} [7	22 🗌 (GND
GND [8	21 🗍 (GND
G 2 [9	20 \	Y11
Y5 [10	19 🛚 🕻	Y10
Y4 [11	18 🛚 `	′ 9
Y3 [12	17 🛚 🕻	/8
Y2 [13	16 🗌 🕻	Y 7
Y1 [14	15 🗆 `	16

A1 [1	28	_ A6
A2 [2	27] A7
A3 [3	26	3A 🗌
A4 [4	25	_ A9
A5 [5	24	_ A10
Ğ1 🗆	6	23	_ A11
V _{CC}	7	22	GND
GND [8	21	GND
Ē2 ☐	9	20	711
Y5	10	19	710
Y4 🗌	11	18	79
Y3 🗍	12	17	_ 7 Y8
Y2 🗏	13	16	¬ γ7
Y1 [14	15	_ Y6

25-OHM LOW-IMPACT SN54BCT25244 ... JT PACKAGE

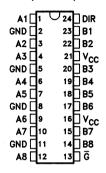
SN74BCT25244 ... NT PACKAGE

OCTAL 25-OHM LINE DRIVERS

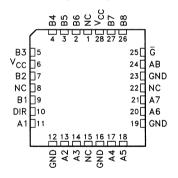
SN54BCT25240 JT PACKAGE SN74BCT25240 NT PACKAGE			
OCTAL 25-OHM LINE DRIVERS			
WITH 3-STATE OUTPUTS			
(TOD VIEW)			

	TE OUTPUTS VIEW)		TE OUTPUTS VIEW)
1Y1 <u>∏</u> 1		1Y1 <u>□</u> 1	J24 ∏1Ğ
GND 🛮 2	23 1A1	GND 🗖 2	23 1A1
1Y2∐3	22 1A2	1Y2 ∐ 3	22 1A2
1Y3∐4	21 V _{CC}	1Y3∐4	21 V _{CC}
GND∏5	20 1A3	GND ☐ 5	20 1A3
1Y4∐6	19 144	1Y4∐6	19∏1A4
2Y1∐7	18 2A1	2Y1∏7	18 🗌 2A1
GND∐8	17 🗌 2A2	GND∐8	17 🗌 2A2
2Y2∐9	16∏∨ _{CC}	2Y2 	16∐V _{CC}
2Y3 🛮 10	15 2A3	2Y3 □ 10	15 2A3
GND∐11	14 🗌 2A4	GND ☐11	14 🗌 2A4
2Y4 🗌 12	13	2Y4 🗆 12	13] 2Ğ

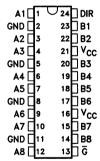
SN54BCT25245 ... JT PACKAGE SN74BCT25245 ... DW or NT PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)



SN54BCT25245 ... FK PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)

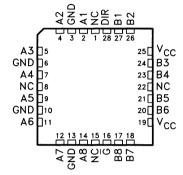


SN54BCT25641 ... JT PACKAGE SN74BCT25641 ... DW OR NT PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)

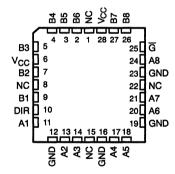


25-OHM LOW-IMPACT (continued)

SN54BCT25641 ... FK PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)



SN54BCT25642 ... FK PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)



SN54BCT25642 ... JT PACKAGE SN74BCT25642 ... DW OR NT PACKAGE 25-OHM OCTAL BUS TRANSCEIVERS (TOP VIEW)

_			_
A1[1	U 24	DIR
GND[2	23	B1
A2[3	22	B2
A3[4	21	D ∨cc
GND[5	20	B3
A4[6	19	B4
A5[7	18	B5
GND[8	17	B6
A6[9	16	Ī∨cc
A7[10	15	B7
GND[11	14	B8
A8[12	13	j ៊ី

SN54BCT25646 ... JT PACKAGE SN74BCT25646 ... NT PACKAGE OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

> ∪28∏SAB 27 T CAB A1 ∏2 26 B1 GND □3 A2 ∏4 25 B2 A3 ☐5 24 □ V_{CC} GND 6 23 B3 A4 ∏7 22 B4 A5 ∏8 21 B5 GND ∏9 20 B6 19 V_{CC} A6 ∐10 A7 []11 18∐ B7 GND 12 17 B8 16 CBA A8 ∏13 DIR 114 15 SBA

25-OHM LOW-IMPACT (continued)

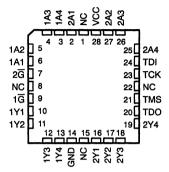
SN54BCT25648 JT PACKAGE SN74BCT25648 NT PACKAGE OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)	SN54BCT25651 JT PACKAGE SN74BCT25651 NT PACKAGE OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)	SN54BCT25652 JT PACKAGE SN74BCT25652 NT PACKAGE OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS (TOP VIEW)
G □ 1	GBA	GBA 1 28 SAB A1 2 27 CAB GND 3 26 B1 A2 4 25 B2 A3 5 24 V _{CC} GND 6 23 B3 A4 7 22 B4 A5 8 21 B5 GND 9 20 B6 A6 10 19 V _{CC} A7 11 18 B7 GND 12 17 B8 A8 13 16 CBA GAB 14 15 SBA
SN54BCT25756 JT PACKAGE SN74BCT25756 NT PACKAGE OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS (TOP VIEW)	SN54BCT25757 JT PACKAGE SN74BCT25757 NT PACKAGE OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS (TOP VIEW)	SN54BCT25760 JT PACKAGE SN74BCT25760 NT PACKAGE OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS (TOP VIEW)
1Y1	1Y1 1	1Y1 1 24 1

SCOPE

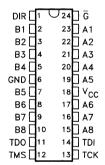
SN54BCT8244 ... JT PACKAGE SN74BCT8244 ... DW OR NT PACKAGE SCAN TEST DEVICE WITH OCTAL BUFFER (TOP VIEW)

1 <u>G</u> [1	\bigcup_{24}	2 <u>G</u>
1Y1[2	23	1A1
1Y2[3	22	1A2
1Y3[4	21	1A3
1Y4[5	20] 1A4
GND[6	19	2A1
	7	18] v _{cc}
2Y2[8	17	2A2
2Y3[9	16	2A3
2Y4[10	15] 2A4
TDO[11	14	וסד [
TMS[12	13] TCK

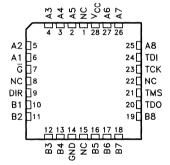
SN54BCT8244 ... FK PACKAGE SCAN TEST DEVICE WITH OCTAL BUFFER (TOP VIEW)



SN54BCT8245 ... JT PACKAGE SN74BCT8245 ... DW OR NT PACKAGE SCAN TEST DEVICE WITH OCTAL BUS TRANSCEIVER (TOP VIEW)



SN54BCT8245 ... FK PACKAGE SCAN TEST DEVICE WITH OCTAL BUS TRANSCEIVER (TOP VIEW)

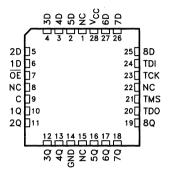


SCOPE (continued)

SN54BCT8373 ... JT PACKAGE SN74BCT8373 ... DW OR NT PACKAGE SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES (TOP VIEW)

c[ſ	U24] ŌĒ
1Q [2	23]1D
2Q [3	22] 2D
3Q []4	21] 3D
4Q []5	20	☐ 4D
GND []6	19	□5D
5Q []7	18	□vcc
6Q []8	17] 6D
7Q [9	16	□7D
8Q [10	15	□8D
TDO [111	14	וסד 🗌
TMS	112	13	Птск

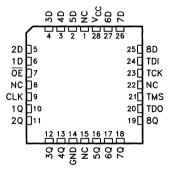
SN54BCT8373 ... FK PACKAGE SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES (TOP VIEW)



SN54BCT8374 ... JT PACKAGE SN74BCT8374 ... DW OR NT PACKAGE SCAN TEST DEVICES WITH OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS (TOP VIEW)

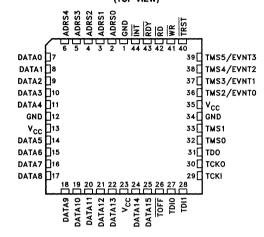
CLK [1	∪24] ōĒ
1Q 🗍	2	23 🗌 1 D
2Q 🗌	3	22 🗌 2D
3Q [4	21 3D
4Q 🗌	5	20 🗌 4D
GND [6	19 🗌 5 D
5Q 🗌	7	18 ☐ V _{CC}
6Q 🗌	8	17 🗌 6D
7Q 🗀	9	16 🗌 7D
8Q [10	15 🗌 8D
TDO [11	14 🗌 TDI
TMS [12	13 TCK

SN54BCT8374 ... FK PACKAGE SCAN TEST DEVICES WITH OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS (TOP VIEW)

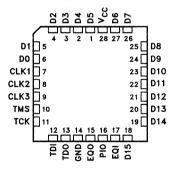


SCOPE (continued)

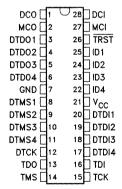
54ACT8990 ... FJ PACKAGE 74ACT8990 ... FN PACKAGE TEST BUS CONTROLLERS (TOP VIEW)



SN54ACT8994 ... FK PACKAGE SN74ACT8994 ... FN PACKAGE DIGITAL BUS MONITORS (TOP VIEW)

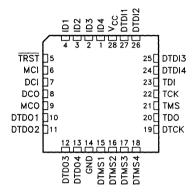


54ACT8997 ... JT PACKAGE 74ACT8997 ... DW OR NT PACKAGE SCAN PATH LINKER WITH 4-BIT IDENTIFICATION BUSES (TOP VIEW)



SCOPE (continued)

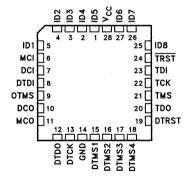
54ACT8997 ... FK PACKAGE SCAN PATH LINKER WITH 4-BIT IDENTIFICATION BUSES (TOP VIEW)



54ACT8999 ... JT PACKAGE 74ACT899 ... DW OR NT PACKAGE SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUS (TOP VIEW)

DTDI [1	
OTMS [2	27 MCI
DCO [3	26 🗌 ID1
мсо [4	25 🗌 ID2
DTDO [5	24 🗌 ID3
DTCK [6	23 🗌 ID4
GND [7	22 🗌 ID5
DTMS1	8	21 V _{CC}
DTMS2	9	20 🗌 ID6
DTMS3	10	19 🗌 ID7
DTMS4	11	18 🗌 ID8
DTRST	12	17 TRST
TDO [13	16 TDI
TMS [14	. 15∐ TCK

54ACT8999 ... FK PACKAGE SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES (TOP VIEW)

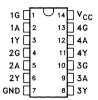


64BCT

SN64BCT125 ... D or N PACKAGE QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS (TOP VIEW)

1 G [1	U14□ V _{CC}
1 A 🗌 2	: 13 ☐ 4 Ġ
1Y 🔲 3	12 4A
2Ğ []4	. 11∏ 4Y
2A 🗌	10 ☐ 3 Ġ
2Y 🗌 6	9 ☐ 3A
GND □	8 3Y

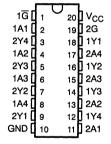
SN64BCT126 ... D or N PACKAGE QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS (TOP VIEW)



SN64BCT240 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

			ı
1 <u>G</u> [1	20	Vcc
	2	19] 2 <u>G</u>
2Y4 🛛	3	18] 1Y1
1A2 [4	17] 2A4
2Y3 🛛	5	16] 1Y2
1A3 [6	15	2A3
2Y2 🛛	7	14] 1Y3
1A4 [8	13	2A2
2Y1 🛛	9	12	1Y4
GND [10	11	2A1

SN64BCT241 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)



SN64BCT244 ... DW OR N PACKAGE OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

1A3 [] 2Y2 []	1	20] 19] 18] 17] 16] 15] 14]	V _C C 2G 1Y1 2A4 1Y2 2A3 1Y3 2A2
1A4 🗍	7 8 9 10	∵ H	

SN64BCT245 ... DW OR N PACKAGE OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS (TOP VIEW)

DIR []1	U 20		Vcc	
A1[]2	19		G	
A2[]3	18		В1	
A3[]4	17		B2	
A4 []5	16		В3	
A5[]6	15		В4	
A6[]7	14		B5	
A7[]8	13		В6	
A8[9	12	b	В7	
GND []10	11		B8	

64BCT (continued)

SN64BCT306 ... D OR P PACKAGE DUAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS (TOP VIEW)

2Ğ 🛛 3	8] 2Y 7] 1A 6] GND 5] 1Y
--------	---------------------------------------

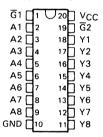
SN64BCT373 ... DW OR N PACKAGE OCTAL D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS (TOP VIEW)

ŌĒ [1	U 20	v _{cc}
1Q [2	19] 8Q
1D [3	18	8D
2D 🗌	4	17]7D
2Q [5	16] 7Q
3Q [6	15] 6Q
3D [7	14]6D
4D [8	13] 5D
4Q [9	12] 5Q
GND [10	11] c

SN64BCT374 ... DW OR N PACKAGE OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUTS (TOP VIEW)

OE [1	\cup_{20}	□ v _{cc}
1Q [2	19] 8Q
1 D 🗌	3	18] 8D
2D [4	17] 7D
2Q 🗌	5	16]7Q
3Q [6	15] 6Q
3D [7	14] 6D
4D 🗌	8	13] 5D
4Q [9	12	5Q
GND [10	11	CLK

SN64BCT541 ... DW OR N PACKAGE OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS (TOP VIEW)



SN64BCT543 ... JT OR NT PACKAGE
OCTAL REGISTERED BUS
TRANSCEIVER WITH 3-STATE
OUTPUTS
(TOP VIEW)

LEBA	1 0	24	□ v _{cc}
GBA	2	23	CEBA
A1 [3	22] B1
A2 [4	21	_ B2
A3 [5	20] B3
A4 [6	19	B4
A5 [7	18	_ B5
A6 [8	17	_ B6
A7 [9	16	B7
8A	10	15] B8
CEAB	11	14	LEAB
GND [12	13	GAB

SN64BCT2240 ... DW OR N PACKAGE OCTAL BUFFER/MOS DRIVER WITH 3-STATE OUTPUTS (TOP VIEW)

1A1 <u>□</u> 2 19□2 <u>G</u>	
2Y4 3 18 1Y1	
1A2 4 17 2A	4
2Y3 5 16 1Y2	2
1A3 6 15 2A	3
2Y2[7 14]1Y3	5
1A4 8 13 2A	2
2Y1[]9 12[]1Y4	ŧ
GND 10 11 2A	1

64BCT (continued)

SN64BCT2241 ... DW OR N PACKAGE OCTAL BUFFER/MOS DRIVER WITH 3-STATE OUTPUTS (TOP VIEW)

1 G 🗆 1	²⁰ □ V _{CC}
1 A 1 🗌 2	19 🗌 2G
2Y4∐3	18] 1 Y 1
1A2[]4	17 🗌 2A4
2Y3[]5	16] 1 Y 2
1A3∐6	15 2A3
2Y2[]7	14 🗌 1 Y 3
1A4∐8	13 2A2
2Y1∏9	12 1Y4
GND 10	11 2A1

SN64BCT2244 ... J OR N PACKAGE OCTAL BUFFER/MOS DRIVER WITH 3-STATE OUTPUTS (TOP VIEW)

1 G 🗌	1	²⁰ V _{CC}
1 A 1	2	19 ∏ 2Ğ
2Y4[3	18 🗌 1 Y 1
1A2[4	17 🗌 2A4
2Y3[5	16 🗌 1 Y 2
1A3[6	15 2A3
2Y2[7	14 🗌 1 Y 3
1A4[8	13 🗌 2A2
2Y1[9	12∐1Y4
GND 🗌	10	11∐2A1

SN64BCT25245 ... DW or NT PACKAGE 25-OHM OCTAL BUS TRANSCEIVER (TOP VIEW)

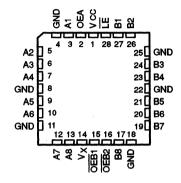
A1 [1	24 DIR
GND [2	23 🗌 B1
A2 [3	22 🗌 B2
A3 [4	21 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
GND [5	20 🗌 B3
A4 [6	19 🗌 B4
A5 [7	18 🗌 B5
GND [8	17 🗌 B6
A6 [9	16∐ V _{CC}
A7 [10	15 B7
GND [11	14 🗌 B8
A8 [12	13 🛚 Ĝ

BTL TRANSCEIVERS

SN54F776 ... JT PACKAGE SN74F776 ... DW OR NT PACKAGE PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS (TOP VIEW)

Vcc[] 1 28 N CE OEAT 2 27 T B1 26 B2 A1 3 GND[] 4 25 GND A21 5 24 T B3 A3[] 6 23 B4 22 GND A4 🛮 7 GND 8 21 B5 **Α5Π** 9 20 T B6 A6[] 10 19N B7 GND[] 11 18 GND A7[12 17 B8 16 OEB2 A8[] 13 15 OEB1

SN54F776 ... FK PACKAGE PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS (TOP VIEW)



SN54BCT979 ... WD PACKAGE SN74BCT979 ... DL PACKAGE 9-BIT REGISTERED BTL TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS (TOP VIEW)

> 48 GBA V_{CC}[AI0 2 47 LEAB 8 []00A 46 B0 Al1 🛮 4 45 GND 44 GND A01 5 GND 43 B1 6 42 ERRA AI2[7 A02 8 41 B2 40 GND Al3[] 9 AO31 10 39 GND 38 B3 Al4[] 11 GND[] 12 37 ODD/EVEN AO4 1 13 36 B4 AI5[] 14 35 SEL AO5 15 34 B5 33 GND AI6[16 AO6 17 32 T GND GND[] 18 31 B6 30 ERRB AI7 19 29 B7 AO7 20 APARI 21 28 GND

> > 27 T GND

25 GAR

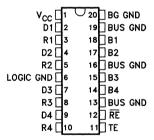
26 BPAR

APARO 22

V_{CC}[] 23

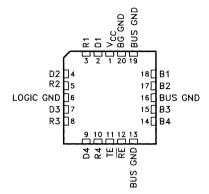
LEBA 24

SN75ALS053 ... N PACKAGE QUAD FUTUREBUS TRANSCEIVER (TOP VIEW)

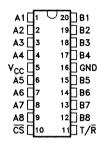


BTL TRANSCEIVERS (continued)

SN75ALS053 ... FN CHIP CARRIER PACKAGE QUAD FUTUREBUS TRANSCEIVER (TOP VIEW)



SN75ALS056 ... DW OR N PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)



SN75ALS057 ... DW OR N PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)

> U20 B1 D1∏1 R1 □ 2 19 E1 D2 🗆 3 18 B2 17 E2 16 GND D3 🗆 6 15 B3 R3 ∏7 14 E3 D4 ∏8 13 B4 R4 ∐9 12 E4

> > 11 RE

〒 **□**10

SN55ALS056 ... J OR W PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)

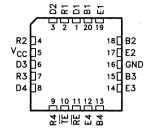
> U20∏B1 A1 ∏1 A2 ∏2 19 B2 A3 🛮 3 18 B3 17 B4 A4 ∏4 V_{CC} [5 A5 [6 16 GND 15 B5 A6 🛮 7 14 B6 A7 ∏8 13 B7 A8 ∏9 12 B8 CS T10 11 T/R

SN55ALS057 ... J OR W PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)

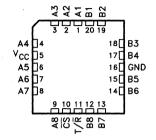
> U 20 B1 R1 ☐ 2 19 E1 18 B2 D2 🛮 3 R2 🗆 17 E2 16 GND D3 🗆 15 B3 R3 ∏7 14 E3 D4 [8 13 B4 R4 ∏9 12 E4 TE []10 11 RE

BTL TRANSCEIVERS (continued)

SN55ALS056 ... FK PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)



SN55ALS057 ... FK PACKAGE TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS (TOP VIEW)



BTA

SN74S1050 D OR N PACKAGE	SN74S1051 D OR N PACKAGE	SN74S1052 DW OR N PACKAGE					
12-BIT SCHOTTKY BARRIER DIODE	12-BIT SCHOTTKY BARRIER DIODE	16-BIT SCHOTTKY BARRIER DIODI					
BUS TERMINATION ARRAY	BUS TERMINATION ARRAYS	BUS TERMINATION ARRAY					
(TOP VIEW)	(TOP VIEW)	(TOP VIEW)					
DO1 1 1 16 D12 DO2 2 15 D11 DO3 3 14 D10 GND 4 13 GND GND 5 12 GND DO4 6 11 D09 DO5 7 10 D08 DO6 8 9 D07	V _{CC} 1 1 16 V _{CC} D01 2 15 D12 D02 3 14 D11 D03 4 13 D10 D04 5 12 D09 D05 6 11 D08 D06 7 10 D07 GND 8 9 GND	D01					
SN74S1053 DW OR N PACKAGE	SN74S1056 SC PACKAGE	SN74S1056 D PACKAGE					
16-BIT SCHOTTKY BARRIER DIODE	8-BIT SCHOTTKY BARRIER DIODE BUS	8-BIT SCHOTTKY BARRIER DIODE BU					
BUS TERMINATION ARRAYS	TERMINATION ARRAYS	TERMINATION ARRAYS					
(TOP VIEW)	(TOP VIEW)	(TOP VIEW)					

General Information	1
ACL LSI Products	2
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Bus-Termination Array Products	5
Clock Driver Products	6
ECL/TTL Translator Products	7
FIFO Products	8
Low-Impedance Line Driver Products	9
Memory Driver Products	10
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54AC11646 . . . JT PACKAGE

D2957, JULY 1987-REVISED MARCH 1990

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125 °C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\overline{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \overline{G} is active (low). In the isolation mode (control \overline{G} high), A data may be stored in one register and/or B data may be stored in the other register.

74AC11646 . . . DW OR NW PACKAGE (TOP VIEW) G∏₁ J28∏CAB А1П 27 T SAB 26∏B1 A2 ∏3 АЗ∏4 25 NB2 **A4** [24 B3 GND TI6 23 B4 GND 17 22 VCC GND ∏8 21 VCC 20 B5 GND TI9

19 B6

18 B7

17 TB8

16 CBA

15 SBA

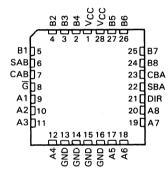
A5∏10

A6∏11

A7 □12

A8 ☐13 DIR ☐14

54AC11646 . . . FK PACKAGE (TOP VIEW)



one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC11646 is characterized for operation from -40°C to 85°C.

The 54AC11646 is characterized for operation over the full military temperature range of -55 °C to 125 °C.

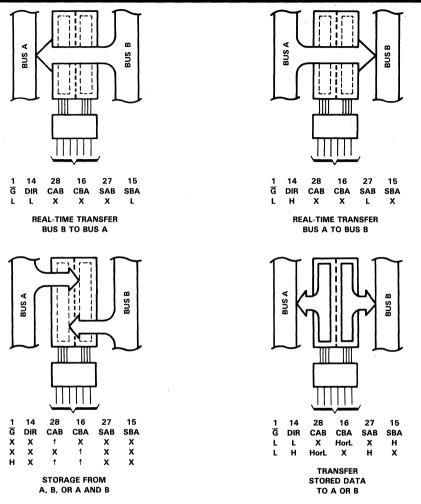
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D2957, JULY 1987-REVISED MARCH 1990



Pin numbers shown are for DW, JT, and NW packages.

FIGURE 1. BUS-MANAGEMENT FUNCTIONS



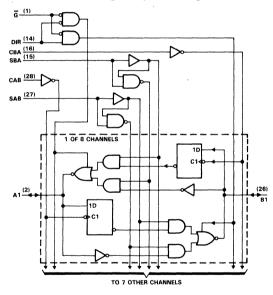
D2957, JULY 1987-REVISED MARCH 1990

FUNCTION TABLE

		INPUTS				DATA	A I/O	OPERATION OR FUNCTION		
Ğ	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION		
х	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified †		
×	X	X	†	X	X	Unspecified †	Input	Store B, A unspecified [†]		
Н	Х	1	1	X	X	1	la	Store A and B Data		
н	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage		
L	L	Х	Х	Х	L	0	lam.ut	Real-Time B Data to A Bus		
L	L	X	H or L	X	н	Output	Input	Stored B Data to A Bus		
L	Н	Х	Х	L	Х		0	Real-Time A Data to B Bus		
L	Н	H or L	X	н	X	Input	Output	Stored A Data to B Bus		

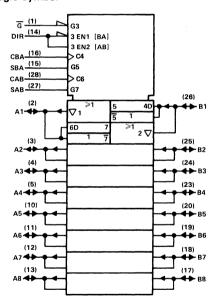
[†] The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)



Pin numbers shown are for DW, JT, and NW packages.

logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NW packages.

D2957, JULY 1987-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	-0.	5 V to	7 V
Input voltage range, V _I (see Note 1)	to V	CC+0.	5 V
Output voltage range, Vo (see Note 1)	to V	CC+0.	5 V
Input clamp current, IIK ($V_I < 0$ or $V_I > V_{CC}$)		± 20	mΑ
Output clamp current, IOK ($VO < 0$ or $VO > VCC$)		± 50	mΑ
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 50	mΑ
Continuous current through VCC or GND pins		± 200	mΑ
Storage temperature range –	65°C	to 150	o°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			5-	54AC11646			74AC11646			
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V	
		V _{CC} = 3 V	2.1			2.1				
V_{iH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V	
		V _{CC} = 5.5 V	3.85			3.85				
		V _{CC} = 3 V			0.9			0.9	V	
V_{IL}	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35		
		V _{CC} = 5.5 V		43	1.65			1.65		
VI	Input voltage		0	46.0	Vcc	0		Vcc	V	
Vο	Input voltage		0	<i>3</i> ⁴	Vcc	0		Vcc	٧	
		V _{CC} = 3 V		\$	-4			-4		
ЮН	High-level output current	V _{CC} = 4.5 V		<u>ي</u>	- 24			- 24	mA	
		V _{CC} = 5.5 V	À	7	- 24			- 24		
		V _{CC} = 3 V	*		12			12		
loL	Low-level output current	V _{CC} = 4.5 V			24			24	mA	
		V _{CC} = 5.5 V			24		-	24		
Δt/Δν	Input transition rise or fall	rate	0		10	0		10	ns/V	
TA	Operating free-air temperat	ure	- 55		125	- 40		85	°C	

D2957, JULY 1987-REVISED MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			54AC	11646	74AC	UNIT	
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Vou	IOH = -4 mA	3 V	2.58			2.4		2.48		v
∨он	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		ľ
	IOH = -24 IIIA	5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA [†]	5.5 V				3.85				
	I _{OH} = -75 mA [†]	5.5 V						3.85		
		3 V			0.1		⋑ 0.1		0.1	
	I _{OL} = 50 μA	4.5 V			0.1	Ś	0.1		0.1	
		5.5 V			0.1	Ó	0.1		0.1	
V	I _{OL} = 12 mA	3 V			0.36	್ರಿ	0.5		0.44	V
VOL	IOI = 24 mA	4.5 V			0.36	25	0.5		0.44	ľ
	IOL = 24 IIIA	5.5 V			0.36	4.	0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
IOZ A or B ports	VO = VCC or GND	5.5 V			±0.5		± 10		± 5	μΑ
I Control pins	VI = VCC or GND	5.5 V			±0.1		±1		± 1	μΑ
Icc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	5.5 V			8		160		80	μА
C _i G or DIR	V _I = V _{CC} or GND	5 V		4.5						pF
Cio A or B ports	VO = VCC or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, VCC = 3.3 V ± 0.3 V (see Note 2)

		TA -	54AC	11646	74AC	UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	0	65	0	65	0	65	MHz
tw	Pulse duration, CAB or CBA high or low	7.7		7.7		7.7		ns
t _{su}	Setup time, A before CABf or B before CBAf	6.5		6.5	S. Carlot	6.5		ns
th	Hold time, A after CAB† or B after CBA†	1		1		1		ns

timing requirements, $V_{CC} = 5 V \pm 0.5 V$ (see Note 2)

		TA = 25°C		54AC11646		74AC11646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	0	100	0	്100	0	100	MHz
t _w	Pulse duration, CAB or CBA high or low	5		.50	574	5		ns
t _{su}	Setup time, A before CABt or B before CBAt	4.5		4.5	2.	4.5		ns
th	Hold time, A after CAB† or B after CBA†	1		Y1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



D2957, JULY 1987-REVISED MARCH 1990

switching characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Note 2)

DADAMETED	FROM	то	T _A = 25°C			54AC	11646	74AC11646		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			65			65		65		MHz
^t PLH	A or B	P or A	1.5	9.1	12.1	1.5	14.9	1.5	13.8	ns
^t PHL	AOIB	B or A	1.5	10.7	13.4	1.5	15.3	1.5	14.5	115
^t PZH	G	A or B	1.5	13	16.4	1.5	20.2	1.5	18.7	ns
^t PZL	7 6	AOIB	1.5	16.1	20.4	1.5	22.2	1.5	21.8	115
tPHZ	G	A or B	1.5	7.9	9.6	1.5	10.8	1.5	10.3	ns
tPLZ]	AUID	1.5	7.2	8.9	1.5	10.1	1.5	9.6	113
^t PLH	CBA or CAB	A or B	1.5	11.8	15	1.5	्री8.4	1.5	17	ns
^t PHL	CBA OF CAB	A 01 B	1.5	13.7	16.8	1.5	19.4	1.5	18.3	""
^t PLH	SBA or SAB†	A or B	1.5	9.8	12.9	1.5	15.6	1.5	14.4	ns
tPHL	(A or B high)	AOIB	1.5	12	14.5	্বী.5	16.7	1.5	15.8	113
^t PLH	SBA or SAB†	A or B	1.5	10.7	13.8	1.5	16.6	1.5	15.4	ns
^t PHL	(A or B low)	A 01 B	1.5	12.4	15	1.5	17.3	1.5	16.4	""3
^t PZH	DIR	A or B	1.5	13.7	17.1	1.5	21	1.5	19.4	ns
tPZL	DIN	7 01 6	1.5	16.8	21	1.5	25.3	1.5	23.6	113
^t PHZ	DIR	A or B	1.5	7.9	9.7	1.5	11	1.5	10.5	ns
^t PLZ	1 DIK	7 01 6	1.5	7.3	9.1	1.5	10.4	1.5	9.9	113

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Note 2)

PARAMETER	FROM	то	T/	T _A = 25°C			54AC11646		74AC11646	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			100			100		100		MHz
^t PLH	A or B	B or A	1.5	5.5	7.9	1.5	9.5	1.5	8.8	
^t PHL	1 4016	BULA	1.5	6.3	8.9	1.5	10.3	1.5	, 9.8	ns
tPZH	G	A or B	1.5	7.8	10.7	1.5	13	1.5	12	ns
^t PZL] "	AOIB	1.5	8.5	11.9	1.5	14	1.5	13.1	l lis
^t PHZ	ਫ	A or B	1.5	5.9	8.4	1.5	9.3	1.5	8.9	ns
^t PLZ		A 01 B	1.5	5.9	7.7	1.5	8.7	1.5	8.3	118
^t PLH	CBA or CAB	A or B	1.5	7	9.7	1.5	ুরী 1.9	1.5	11	
^t PHL	CDA OF CAB	AOIB	1.5	8.2	11	1.5	13	1.5	12.2	ns
^t PLH	SBA or SAB†	A or B	1.5	5.9	8.4	1,5	10.1	1.5	9.4	
^t PHL	(A or B high)	AOIB	1.5	7.2	9.8	1.5	11.4	1.5	10.7	ns
^t PLH	SBA or SAB†	A or B	1.5	6.3	8.9	1.5	10.7	1.5	9.9	Ι
^t PHL	(A or B low)	AOIB	1.5	7.3	9.9	1.5	11.7	1.5	11	ns
^t PZH	DIR	A or B	1.5	8.4	11.2	1.5	13.6	1.5	12.6	
^t PZL] DIK	A OF B	1.5	9.1	12.3	1.5	14.6	1.5	13.7	ns
^t PHZ	DIR	A or B	1.5	6.3	8.2	1.5	9.1	1.5	8.7	
^t PLZ] DIK .	A or B	1.5	5.7	7.5	1.5	8.5	1.5	8.1	ns

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
C .	Power dissipation capacitance per transceiver	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	59	pF
Cpd		Outputs disabled	CL = 50 pr, 1 = 1 MHz	15	рг





D2957, JULY 1987-REVISED MARCH 1990

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-um Process
- 500-mA Typical Latch-Up Immunity at 125 °C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

description

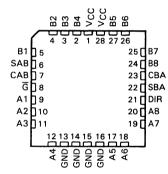
These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\overline{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \overline{G} is active (low). In the isolation mode (control \overline{G} high), A data may be stored in one register and/or B data may be stored in the other register.

54ACT11646 . . . JT PACKAGE 74ACT11646 . . . DW OR NT PACKAGE (TOP VIEW)

> G \square U28 CAB А1 П2 27 SAB 26 B1 A2 ∏3 АЗ∏4 25 | B2 A4 ∐5 24 B3 GND∏6 23 TB4 GND 🗖 7 22 \ VCC GND 18 21 VCC GND∏9 20 N B 5 A5 110 19∏B6 18 B7 A6∏11 A7 1 12 17 T B8 A8 ∏13 16 CBA DIR 114 15 SBA

54ACT11646 . . . FK PACKAGE (TOP VIEW)



When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 54ACT11646 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The 74ACT11646 is characterized for operation from $-40\,^{\circ}$ C to 85 °C.

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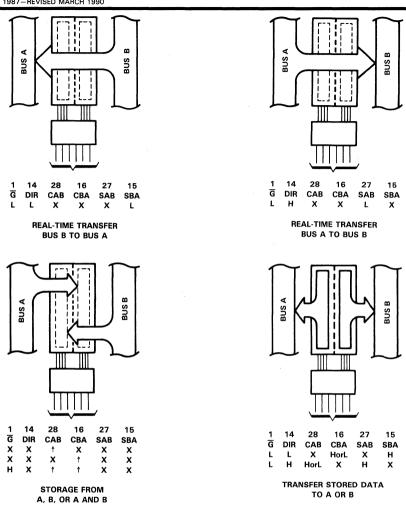


FIGURE 1. BUS-MANAGEMENT FUNCTIONS



D2957, JULY 1987-REVISED MARCH 1990

FUNCTION TABLE

INPUTS						DAT	A I/O	OPERATION OR FUNCTION		
Ğ	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION		
х	х	Ť	X	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]		
×	X	X	Ť	X	×	Unspecified [†]	Input	Store B, A unspecified [†]		
Н	Х	Ť	1	Х	X	lanut	lanut	Store A and B Data		
н	Х	H or L	H or L	х	Х	Input	Input	Isolation, hold storage		
L	L	Х	Х	Х	L	Outmut	lanut	Real-Time B Data to A Bus		
L	L	Х	H or L	X	н	Output	Input	Stored B Data to A Bus		
L	Н	Х	Х	L	х	lanut	Outros	Real-Time A Data to B Bus		
L	н	H or L	X	н	X	Input	Output	Stored A Data to B Bus		

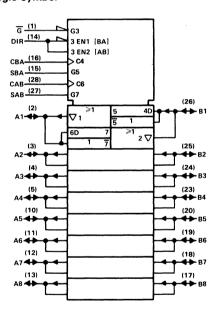
[†] The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagram (positive logic)

TO 7 OTHER CHANNELS

Pin numbers shown are for DW, JT, and NT packages.

logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

D2957, JULY 1987-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	o VCC+0.5 V
Output voltage range, Vo (see Note 1)	o VCC+0.5 V
Input clamp current, IjK ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	\dots \pm 50 mA
Continuous current through VCC or GND pins	$\dots \pm 200 \ mA$
Storage temperature range – 69	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54AC	Г11646	74AC	11646	UNIT
		MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	√Vcc	0	Vcc	٧
Vo	Output voltage	0,	[₹] VCC	0	Vcc	٧
ЮН	High-level output current		-24		- 24	mΑ
lOL	Low-level output current	್ಷನೆ	24		24	mΑ
Δt/Δν	Input transition rise or fall rate	₹ 0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	TA	= 25	°C	54AC1	11646	74AC1	11646	UNIT
PANAIVIETEN	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
	10H = - 90 ltA	5.5 V	5.4			5.4		5.4		
VoH	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		v
VOH		5.5 V	4.94			4.7		4.8		٠, ٧
	I _{OH} = -50 mA [†]	5.5 V				3.85	- L			
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					33	3.85		
	I _{OL} = 50 μA	4.5 V			0.1		Ø.1		0.1	
	10L = 90 μΑ	5.5 V			0.1		₹ 0:1		0.1	
VOL	I _{OL} = 24 mA	4.5 V			0.36		ှ 0.5		0.44	v
VOL	10L = 24 MA	5.5 V			0.36	L á	0.5		0.44	•
	$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
IOZ A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		± 5	μΑ
I _I G or DIR	$V_I = V_{CC}$ or GND	5.5 V			±0.1		± 1		± 1	μΑ
Icc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	5.5 V			8		160		80	μΑ
ΔICC§	One input at 3.4 V,	5.5 V			0.9		1		1	mA
4.00	Other inputs at GND or VCC	J.3 V			0.5		'		'	
Ci	$V_I = V_{CC}$ or GND	5 V		4.5						рF
Co	$V_O = V_{CC}$ or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, $VCC = 5 \pm 0.5 \text{ V}$ (see Note 2)

		TA =	TA = 25°C			74AC1	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	105	0	105	0	105	MHz
t _W	Pulse duration, CAB or CBA high or low	4.8		4.8	Ö. (4),	4.8		ns
t _{su}	Setup time, A before CLK1 or B before CBA1	4.5		4.5	EV.	4.5		ns
th	Hold time, A after CAB† or B after CBA†	2.5		2.5		2.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

 $^{^{\}ddagger}\text{For I/O}$ ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

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switching characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Note 2)

PARAMETER	FROM	то	T,	= 25	°C	54AC1	Г11646	74AC1	11646	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax			105			105		105		MHz
^t PLH	A or B	B or A	1.5	7.3	10.1	1.5	12.5	1.5	11.5	ns
^t PHL	. AUD	BUIA	1.5	7.2	11	1.5	12.9	1.5	12	10
tPZH	G	A or B	1.5	7.7	12.8	1.5	15.5	1.5	14.4	ns
^t PZL	·	AOIB	1.5	9.2	13.8	1.5	16.7	1.5	15.3	110
t _{PHZ}	G	A or B	1.5	8.6	10.7	1.5	12.3	1.5	11.6	ns
tPLZ	<u> </u>	X 01 B	1.5	7.8	9.7	1.5	11.2	1.5	10.6	115
^t PLH	CBA or CAB	A or B	1.5	8.8	11.9	1.5	14.7	1.5	13.5	ns
^t PHL	CBA OF CAB	A 01 B	1.5	10	13.4	1.5		1.5	14.9	10
^t PZH	DIR	A or B	1.5	10.2	13.7	1,49	16.7	1.5	15.3	ns
t _{PZL}	DIR	400	1.5	10.9	14.8	∄ .5	18	1.5	16.5	115
^t PHZ	DIR	A or B	1.5	7.9	10.5	1.5	11.8	1.5	11.3	ns
tPLZ	DIN	X 01 B	1.5	7.3	9.5	1.5	10.7	1.5	10.3	115
^t PLH	SBA or SAB	A or B	1.5	6.7	10.3	1.5	12.4	1.5	11.5	ns
t _{PHL}	(A or B high)	X 01 B	1.5	9.1	12.1	1.5	14.5	1.5	13.5	110
^t PLH	SBA or SAB	A or B	1.5	8	10.9	1.5	13.6	1.5	12.4	ns
tPHL	(A or B low)	, A 01 B	1.5	8.1	11.9	1.5	14	1.5	13.1	115

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
<u> </u>	Payer dissination consistence not transcribe.	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	63	,E
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	14	pF

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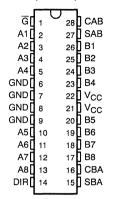
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

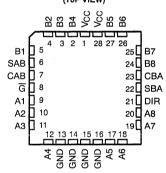
These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\overline{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-

54AC11648 . . . JT PACKAGE 74AC11648 . . . DW OR NT PACKAGE (TOP VIEW)



54AC11648 . . . FK PACKAGE (TOP VIEW)



impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \overline{G} is active (low). In the isolation mode (control \overline{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses. A or B. may be driven at a time.

The 54AC11648 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11648 is characterized for operation from -40° C to 85°C.

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D3457, MARCH 1990-REVISED MAY 1990

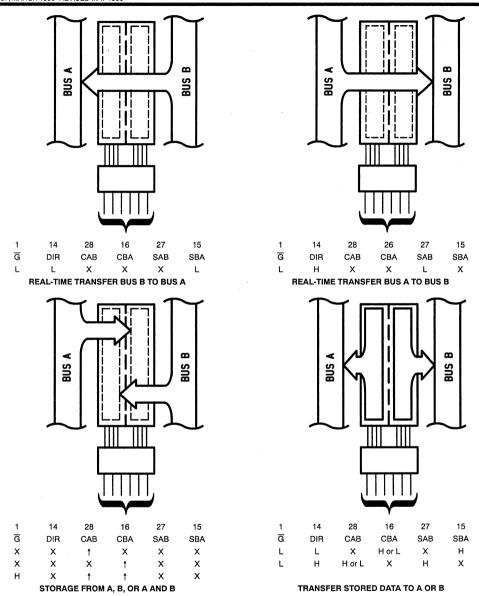


FIGURE 1. BUS-MANAGEMENT FUNCTIONS

Pin numbers shown are for DW, JD, and NW packages.



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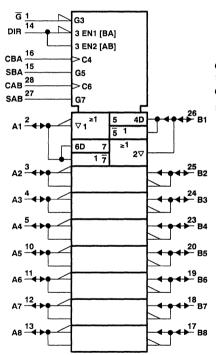
FUNCTION TABLE

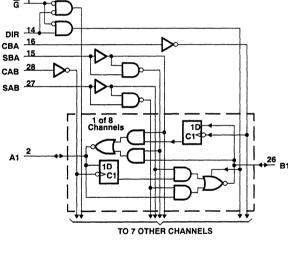
		11	NPUTS			DAT	A I/O	OREDATION OF EUROTION
Ğ	DIR	CAB	СВА	SAB	SBA	A1 THRU A8	BI THRU B8	OPERATION OR FUNCTION
X	Х	1	Х	х	х	Input	Unspecified [†]	Store A, B unspecified†
x	Х	Х	†	X	х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	†	1	X	X	Input	Input	Store A and B Data
н	X	H or L	H or L	X	х	Input	Input	Isolation, hold storage
L	L	Х	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	н	Output	Input	Stored B Data to A Bus
L	Н	X	X	L	×	Input	Output	Real-Time A Data to B Bus
L	Н	H or L	X	н	X	Input	Output	Store A Data to B Bus

[†] The data output functions may be enabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol[‡]

logic diagram (positive logic)





[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, or NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1) –	- 0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1) –	- 0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1164	18	74	AC1164	8	
			MIN NOM		MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
V _{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1,35			1.35	V
		V _{CC} = 5.5 V			4.65			1.65	
VI	Input voltage		0	6	[≫] V _{CC}	0		Vcc	V
Vo	Output voltage		0	1/4	Vcc	0		Vcc	V
		V _{CC} = 3 V	0	170	-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V	.00	,	- 24			- 24	mA
		V _{CC} = 5.5 V	4,		- 24			- 24	
		V _{CC} = 3 V			12			12	
loL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C



D3457, MARCH 1990-REVISED MAY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Γ.	PARAMETER	TEST CONDITIONS	V	Т,	Δ = 25°C		54AC	1648	74AC1	1648	UNIT
'	PANAMEIEN	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			3 V	2.9			2.9		2.9		
		I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		v
VOH		Jan. 24 m 4	4.5 V	3.94			3.7		3.8		V
		I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		
		I _{OH} = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = 75 mA [†]	5.5 V						3.85		
			3 V			0.1		<u>~</u> <0.1		0.1	
		I _{OL} = 50 μA	4.5 V			0.1		ે છે.1		0.1	
İ			5.5 V			0.1	26.26	0.1		0.1	
\v		I _{OL} = 12 mA	3 V			0.36	18/4	0.5		0.44	V
VOL		1 04 mA	4.5 V			0.36		0.5		0.44	V
1		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		I _{OL} = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	A or B ports‡	V _I = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μΑ
11	Control inputs	VI = VCC or GND	5.5 V			± 0.1		± 1		± 1	μΑ
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	Control inputs	VI = VCC or GND	5 V		4.5						pF
Со	A or B ports	V _I = V _{CC} or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (see Note 2)

		T _A =	25°C	54AC1	1648	74AC	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	0	40	. 0	(40	0	40	MHz
t _w	Pulse duration, CAB or CBA high or low	12.5		12,50		12.5		ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	6.5		⟨6.5∜	,	6.5		ns
th	Hold time, A before CAB↑ or B after CBA↑	0		80		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (see Note 2)

		T _A =	T _A = 25°C			74AC		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	90	0,	SV. 90	0	90	MHz
t _w	Pulse duration, CAB or CBA high or low	5.6		5.6	116	5.6		ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		₹4, 5 %	,	4.5		ns
th	Hold time, A before CAB↑ or B after CBA↑	0.		°O		0		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	то	Т	A = 25°0	2	54AC	11648	74AC	11648	
PARAMETER	(INPUT) (OUTPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}		,	40			40		40		MHz
^t PLH	A or B	B or A	3	8.7	12.6	3	15.6	3	14.3	ns
t _{PHL}	AGIB		3.8	9.3	14.4	3.8	17	3.8	15.9	
^t PZH	G	A or B	5	11.1	17.2	5	21	5	19.4	ns
tPZL			5.2	12.8	20.5	5.2	24.7	5.2	23	115
^t PHZ	G	A or B	4.1	7.2	9.9	4.1	11.2	4.1	10.6	ns
^t PLZ	G G	AOID	3.7	6.5	9.1	3.7	10.2	3.7	9.7	113
^t PLH	CBA or CAB	A or B	4.3	10.1	15.6	4.3	5 19.2	4.3	17.6	ns
^t PHL	OBAGIOAB	AUID	5.2	11.5	17.6	3/3//	<u>√</u> 20.5	5.2	19.4	113
t _{PLH}	SAB or SBA†	A or B	3.7	9.1	14.1	₹3, 2 °	17.2	3.7	15.8	
^t PHL	(with A or B high)	AUID	4.5	10.3	15.9	4.5	18.5	4.5	17.4	ns
t _{PLH}	SBA or SAB†	A or B	3.2	8.6	13.6	3.2	16.6	3.2	15.3	ns
t _{PHL}	(with A or B low)	Aorb	4.6	10.3	15.6	4.6	18.2	4.6	17.1	115
^t PZH	DIR	A or B	4.9	11.6	18.2	4.9	22.4	4.9	20.6	ns
^t PZL] DIR	AUIB	5.2	14.2	21.6	5.2	24.9	5.2	24.3	115
^t PHZ	DIR	A B	3.8	7.1	10.1	3.8	11.4	3.8	10.9	ns
[†] PLZ	DIR	A or B	3.5	6.5	9.3	3.5	10.6	3.5	10.1	115

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T	Δ = 25°C	•	54AC	11648	74AC	11648	UNIT
PANAMICIEN	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNI
fmax			90			90		90		MHz
tPLH .	A or B	B or A	2.6	5.6	8.3	2.6	10.3	2.6	9.5	ns
[†] PHL	1 7015		3.2	6.4	9.4	3.2	11.4	3.2	10.6	115
^t PZH	G	A or B	4.2	7.8	11.3	4.2	13.8	4.2	12.8	
^t PZL	1 " 1		4.1	8.1	12	4.1	14.7	4.1	13.6	ns
^t PHZ	G	A or B	3.8	6.3	8.6	3.8	9.6	3.8	9.2	ns
[†] PLZ] "	AOIB	3.5	5.7	7.8	3.5	8.8	3.5	8.4	113
^t PLH	CBA or CAB	A or B	3.6	6.9	10	3.6	12.4	3.6	11.4	ns
[†] PHL	T CDA OI CAB	AUID	4.3	8	11.4	4.3	13.8	4.3	12.8	113
^t PLH	SAB or SBA [†]	A D	3.1	6.2	9.2	3.1	11.3	3.1	10.4	
^t PHL	(with A or B high)	A or B	3.8	7.6	10.4	3.8	12.5	3.8	11.6	ns
^t PLH	SBA or SAB†	A au D	2.8	6.1	8.9	2.8	10.9	2.8	10.1	ns
^t PHL	(with A or B low)	A or B	3.8	7.3	10.4	3.8	12.5	3.8	11.6	113
^t PZH	DIR	A == D	4	8	11.9	4	14.5	4	13.4	ns
^t PZL	7 510	A or B	4.1	8.4	12.7	4.1	15.5	4.1	14.4	115
^t PHZ	DID		3.5	6.1	8.5	3.5	9.5	3.5	9.1	ns
^t PLZ	DIR	A or B	3.4	5.9	7.8	3.4	8.7	3.4	8.4	115

[†] These parameters are measured with the internal output state of the storagegister opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
<u> </u>	Power discination conscitance per transceivers	Outputs enabled	C _I = 50 pF, f = 1 MHz	66	ρF
Cbq	Power dissipation capacitance per transceivers	Outputs disabled	C[= 50 pr, 1 = 1 MHz	17	þΓ

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



D3458, MARCH 1990-REVISED OCTOBER 1990

- Inputs are TTL-Voltage Compatible
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable (\overline{G}) and direction (DIR) pins are provided to control the transceiver functions. In the

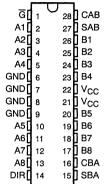
transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \overline{G} is active (low). In the isolation mode (control \overline{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

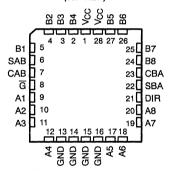
The 54ACT11648 is characterized for operation over the full military temperature range of -55° C to 125° C. The 74ACT11648 is characterized for operation from -40° C to 85° C.

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54ACT11648 ... JT PACKAGE 74ACT11648 ... DW OR NT PACKAGE (TOP VIEW)



54ACT11648 . . . FK PACKAGE (TOP VIEW)



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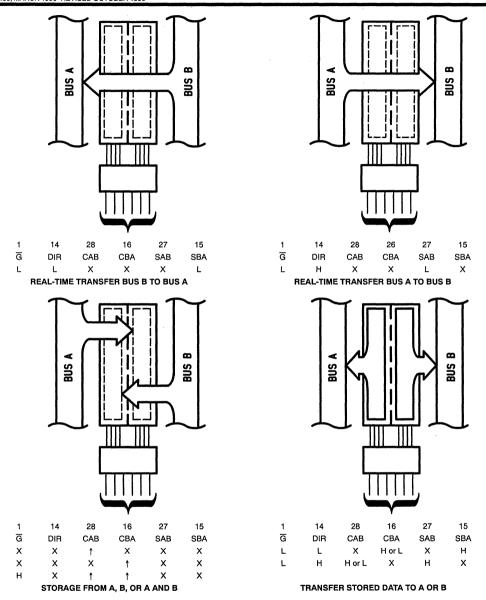


FIGURE 1. BUS-MANAGEMENT FUNCTIONS

Pin numbers shown are for DW, JT, and NT packages.



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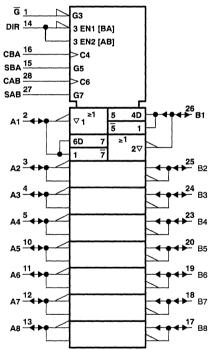
FUNCTION TABLE

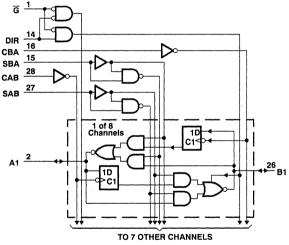
		11	NPUTS			DAT	A I/O	ODERATION OR FUNCTION
G	DIR	CAB	СВА	SAB	SBA	A1 THRU A8	BI THRU B8	OPERATION OR FUNCTION
Х	Х	1	×	×	Х	Input	Unspecified [†]	Store A, B unspecified [†]
х	Х	X	1	×	x	Unspecified [†]	Input	Store B, A unspecified [†]
н	Х	†	†	X	x	Input	Input	Store A and B Data
Н	Х	H or L	H or L	X	х	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	н	Output	Input	Stored B Data to A Bus
L	Н	Х	X	L	x	Input	Output	Real-Time A Data to B Bus
L	Н	H or L	X	н	x	Input	Output	Store A Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol‡

logic diagram (positive logic)





[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, or NT packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage température range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54	54ACT11648			74ACT11648			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2		4	2			٧	
VIL	Low-level input voltage		_	8.0			0.8	٧	
VI	Input voltage	0	- OF	*Vcc	0		Vcc	V	
Vo	Output voltage	0	X	Vcc	0		Vcc	٧	
ІОН	High-level output current	6	25	- 24			- 24	mA	
lOL	Low-level output current	SEO.		24			24	mA	
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V	
TA	Operating free-air temperature	- 55		125	- 40		85	°C	

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				T,	A = 25°C	>	54ACT	11648	74ACT	11648		
PAI	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			4.5 V	4.4			4.4		4.4			
		IOH = - 50 μA	5.5 V	5.4			5.4		5.4			
		I _{OH} = - 24 mA	4.5 V	3.94			3.7		3.8		١	
Vон		10H = - 24 IIIA	5.5 V	4.94			4.7		4.8		V	
		I _{OH} = - 50 mA [†]	5.5 V				3.85					
		I _{OH} = - 75 mA [†]	5.5 V						3.85			
			4.5 V			0.1		0.1		0.1		
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1		
			4.5 V			0.36	A.	0.5		0.44		
VOL		I _{OL} = 24 mA	5.5 V			0.36	QQ'	№ 0.5		0.44	V	
		I _{OL} = 50 mA [†]	5.5 V				6,44	1.65				
		I _{OL} = 75 mA [†]	5.5 V							1.65		
11	Control Inputs	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ	
loz	A or B ports‡	V _I = V _{CC} or GND	5.5 V	}		± 0.5		± 10		± 5	μΑ	
Icc		VI = VCC or GND, IO = 0	5.5 V			8		160		80	μΑ	
ΔICC§		One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA	
Ci	Control inputs	VI = VCC or GND	5 V		4.5						pF	
Cio	A or B ports	V _I = V _{CC} or GND	5 V		12						PΓ	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Note 2)

		T _A =	25°C	54ACT11648	74AC1	11648	UNIT
		MIN	MAX	MIN MA	K MIN	MAX	O.V.
fclock	Clock frequency	0	75	0 37	5 0	75	MHz
tw	Pulse duration, CAB or CBA high or low	6.7		6,70%	6.7		ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	5		< [₹] 5 </td <td>5</td> <td></td> <td>ns</td>	5		ns
th	Hold time, A after CAB↑ or B after CBA↑	2		₹2	2		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡] For I/O ports, the parameter IOZ includes the input leakage currrent.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM TO		Т,	Δ = 25°C	;	54ACT	11648	74ACT	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			75			75		75		MHz
tPLH	A or B	A or B B or A		6.5	9.5	2.4	11.6	2.4	10.7	ns
tPHL.	7010	50171	4.4	8.5	11.3	4.4	13.8	4.4	12.7	115
^t PZH	G	A or B	4.2	9.2	13	4.2	15.8	4.2	14.6	
tPZL		., ., .	4.3	9.8	13.9	4.3	16.9	4.3	15.6	ns
tPHZ	G	A or B	5.7	8.7	11.3	5.7	12.9	5.7	12.2	ns
tPLZ	G	7010	5.3	8.1	10.5	5.3	12.1	5.3	11.4	ns
t _{PLH}	CBA or CAB	A D	5.2	9.4	12	5.2	\$ 14.9	5.2	13.7	ns
tPHL	CDA OI CAB	A or B	6	10.5	13.5	6	16.3	6	15.2	115
^t PLH	SAB or SBA†	A D	4.7	8.6	11.3	4,7	14	4.7	12.9	
tPHL	(with A or B high)	A or B	3.8	8.6	12	3.8	14.3	3.8	13.4	ns
tPLH t	SBA or SAB†	A av B	2.6	7.1	10.2	2.6	12.5	2.6	11.5	ns
tPHL.	(with A or B low)	A or B	5.4	9.7	12.6	5.4	15.2	5.4	14.1	115
^t PZH	DIR	A as D	3.9	9.8	14.9	3.9	18.4	3.9	16.9	ns
tPZL	DIN	A or B	3.9	10.8	15.1	3.9	18.7	3.9	17.2	115
tPHZ	DIR	A D	4.5	8.2	10.6	4.5	12	4.5	11.5	ns
tPLZ	DIN	A or B	3.9	7.3	9.6	3.9	11.9	3.9	11.3	113

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CO	TYP	UNIT		
<u> </u>	Power dissipation capacitance per transceivers	Outputs enabled	C ₁ = 50 pF.	f = 1 MHz	61	pF
Cpd	rower dissipation capacitance per transceivers	Outputs disabled	OL = 50 pr,	1 = 1 1411 12	15) Pr]

54AC11651, 74AC11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

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- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

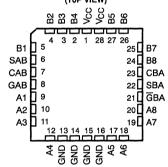
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input

54AC11651 ... JT PACKAGE 74AC11651 ... DW OR NT PACKAGE (TOP VIEW)

> **GAB** □ 28 [] CAB 27 N SAB A1∏ 2 A2[] 3 26∏ B1 25 B2 ΑЗП А4П 24 N B3 GND 23 N B4 GND 7 22 NCC GND I 8 21 VCC GND 20 B5 9 19 B6 A5 1 10 A6 11 18 N B7 A7 🛮 12 17 B8 А8П 13 16 CBA 15 SBA GΒAΠ

54AC11651 . . . FK PACKAGE (TOP VIEW)



level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 54AC11651 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11651 is characterized for operation from -40° C to 85°C.

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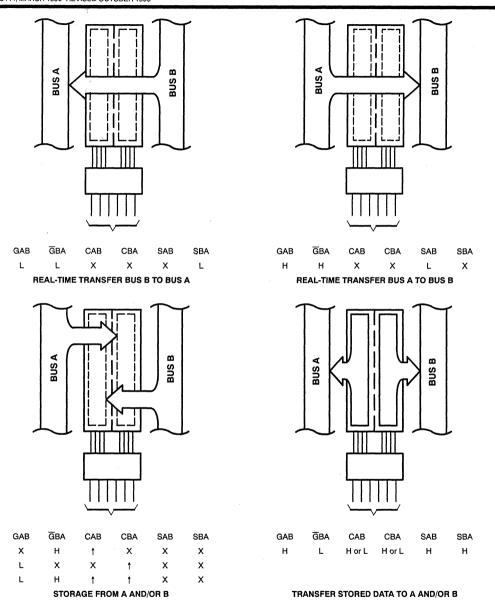


Figure 1. Bus Transfer Diagram



54AC11651, 74AC11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

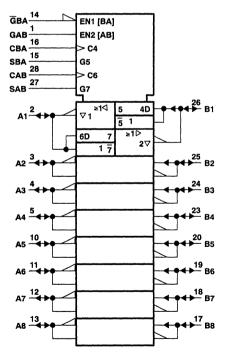
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FUNCTION TABLE

		INP	UTS			DAT	A I/O	OPERATION OR FUNCTION
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	HorL	Х	Х	Input	Input	Isolation
L	н	Ť	t	×	×	Input	Input	Store A and B Data
Х	н	1	HorL	х	×	Input	Unspecified [†]	Store A, Hold B
Н	н	t	l t	X‡	×	Input	Output	Store A in both registers
L	×	HorL	t	х	×	Unspecified [†]	Input	Hold A, Store B
L	L	1	1	Х	X‡	Output	Input	Store B in both registers
L	L	x	x	Х	L	Output	Input	Real-Time B data to A Bus
L	L	x	HorL	×	н	Output	Input	Stored B Data to A Bus
Н	н	х	×	L	×	Input	Output	Real-Time A Data to B Bus
Н	н	HorL	x	н	х	Input	Output	Stored A Data to B Bus
Н	L	HorL	HorL	н	н	Output Output		Stored A Data to B Bus and
	1					,		Stored B Data to A Bus

[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol§



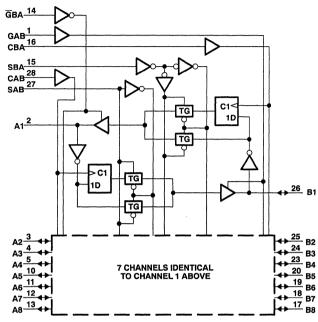
[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, or NT packages.



^{\$} Select control = L: clocks can occur simultaneously, Select control = H: clocks must be staggered in order to load both registers.

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logic diagram (positive logic)



Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11651, 74AC11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

D3444, MARCH 1990-REVISED OCTOBER 1990

recommended operating conditions

			54	AC1165	i1	74	AC1165	1	
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
\vee_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1,35			1.35	V
		V _{CC} = 5.5 V			4 7.65			1.65	
VI	Input voltage		0	DAG	Vcc	0		Vcc	٧
Vo	Output voltage		O ORODI	<u> </u>	Vcc	0		Vcc	V
		V _{CC} = 3 V	60	5	- 4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V	ORD		- 24			- 24	mA
		V _{CC} = 5.5 V	1		- 24			- 24	
		V _{CC} = 3 V			12			12	
loL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAG	DAMETER	TEST CONDITIONS		T,	A = 25°C		54AC	11651	74AC1	1651	LIMIT
PAI	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			3 V	2.9			2.9		2.9		
		IOH = - 50 μA	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
\/-··		I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		V
Vон		Jan. 24 mA	4.5 V	3.94			3.7		3.8		V
]		I _{OH} = – 24 mA	5.5 V	4.94			4.7		4.8		
		I _{OH} = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = - 75 mA [†]	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	4.5 V			0.1	"	€ 0.1		0.1	
			5.5 V			0.1	*O2	0.1		0.1	
		I _{OL} = 12 mA	3 V			0.36	41,410	0.5		0.44	v
VOL			4.5 V			0.36	4	0.5		0.44	V
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		I _{OL} = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
loz A	or B ports‡	V _I = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μΑ
I _I C	ontrol inputs	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ
lcc		VI = VCC or GND, IO = 0	5.5 V			8		160		80	μА
C _i C	ontrol inputs	VI = VCC or GND	5 V		4.5						pF
C _{io} A	or B ports	VI = VCC or GND	5 V		10						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Note 2)

		T _A =	T _A = 25°C			74AC1	11651	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	45	0	₹ 45	0	45	MHz
t _w	Pulse duration, CAB or CBA high or low	10		1,00	100	10		ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	6.5		₹ 0.5€	7,	6.5		ns
th	Hold time, A after CAB↑ or B after CBA↑	0		₹0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

		T _A =	25°C	54AC1	11651	74AC1	11651	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	0	90	0	☆ 90	0	90	MHz
t _w	Pulse duration, CAB or CBA high or low	5.5		5.5	(1)	5.5		ns
t _{su}	Setup time, A before CAB↑ or B before CBA↑	4.5		684,50	20.	4.5		ns
th	Hold time, A after CAB↑ or B after CBA↑	0.5		0.5		0.5		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T,	A = 25°C	;	54AC1	1651	74AC1	1651	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			45			45		45		MHz
^t PLH	A or B	B or A	3.2	7.7	12.1	3.2	15.4	3.2	14	
^t PHL	AOIB	BOLA	4.3	9.5	14.6	4.3	17.2	4.3	16.1	ns
^t PLH	CBA or CAB	A or B	4.6	9.8	15	4.6	15.8	4.6	17.2	
[†] PHL	CBA OF CAB	AUID	5.4	11.5	17.5	5.4	20.5	5.4	19.2	ns
tPLH	SBA or SAB†	A or B	3.8	8.6	13.3	3.8	16.9	3.8	15.3	
tphL.	with A or B high	AUID	4.8	10.2	15.5	4.8	18.2	4.8	17.1	ns
tPLH .	SBA or SAB†	A or B	3.4	8.1	12.7		्र,16	3.4	14.6	
^t PHL .	with A or B low	Aorb	5	10.3	15.5	\Q_{\(\begin{array}{c} \cdot \	18.2	5	17.1	ns
^t PZH	Ğва	А	4.6	9.8	14.9	₹4.6	18.4	4.6	16.9	ns
^t PZL	GBA	A	5.3	12.1	18.9	5.3	23.2	5.3	21.3	ns
tPHZ	Ğва	А	4.4	6.6	8.8	4.4	9.5	4.4	9.2	ns
tPLZ	GBA	^	3.8	5.8	7.8	3.8	8.3	3.8	8.1	115
^t PZH	048	6	4.9	10.2	15.5	4.9	19.2	4.9	17.6	
tPZL	GAB	В	5.5	12.2	18.8	5.5	22.9	5.5	21.2	ns
^t PHZ	GAB	В	4.4	6.7	8.9	4.4	9.6	4.4	9.3	
tPLZ	GAB	В	3.5	5.7	7.8	3.5	8.2	3.5	8	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T,	A = 25°C	;	54AC	11651	74AC1	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			90			90		90		MHz
[†] PLH	A or B	B or A	2.6	5.3	8	2.6	9.9	2.6	9.1	ns
^t PHL	AUID	D OF A	3.5	6.5	9.4	3.5	11.3	3.5	10.5	115
^t PLH	CBA or CAB	A or B	3.8	6.8	10	3.8	12.4	3.8	11.4	ns
^t PHL	CBA OI CAB	AUID	4.7	8.1	11.5	4.7	13.8	4.7	12.8	115
^t PLH	SAB or SBA†	A or B	3.2	6	8.8	3.2	₁₁	3.2	10.1	ns
^t PHL	with A or B high	AUID	3.9	7	10.1	3.9	Q 12	3.9	11.2	115
[†] PLH	SAB or SBA†	A or B	2.9	5.7	8.5		₹10.4	2.9	9.5	ns
^t PHL	with A or B low	AUID	4.1	7.2	10.3	Q 4X1	12.3	4.1	11.4	115
^t PZH	- GBA	Α	3.9	6.9	9.8	3.9	12	3.9	11.1	ns
^t PZL	GBA	^	4.2	7.6	11	4.2	13.7	4.2	12.5	115
^t PHZ	GBA	А	4.1	5.9	7.6	4.1	8.2	4.1	8	ns
^t PLZ	db/	^	3.5	5.2	6.8	3.5	7.4	3.5	7.1	113
^t PZH	GAB	В	4.2	5.9	10.4	4.2	12.9	4.2	11.8	
^t PZL	GAB	B B	4.5	8	11.4	4.5	14	4.5	12.9	ns
^t PHZ	GAB	В	4.2	6	7.8	4.2	8.4	4.2	8.2	ns
t _{PLZ}	JUAD		3.3	5.1	6.9	3.3	7.3	3.3	7.2	115

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



54AC11651, 74AC11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

D3444, MARCH 1990-REVISED OCTOBER 1990

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per transceiver	Outputs enabled	C _I = 50 pF, f = 1 MHz	64	ρF
Ора	1 over a sopalion capacitance per transceiver	Outputs disabled	OL = 50 pr, 7 = 7 Min2	14	, p.

54ACT11651, 74ACT11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

D3445, MARCH 1990-REVISED OCTOBER 1990

Inputs are TTL-Voltage Compatible

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

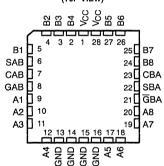
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

54ACT11651 ... JT PACKAGE 74ACT11651 ... DW OR NT PACKAGE (TOP VIEW)

GAB 1 28 CAB
A1 2 27 SAB
A2 3 26 B1
A3 4 25 B2
A4 5 24 B3
GND 6 23 B4
GND 7 22 VCC

GND I a 21 VCC GND 9 20 N B5 A5 1 10 19 B6 18 B7 А6П 11 A7Π 17 B8 12 A8 🗍 13 16 T CBA GBA 15 SBA 14

54ACT11651 . . . FK PACKAGE (TOP VIEW)



A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers. Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 54ACT11651 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11651 is characterized for operation from – 40°C to 85°C.

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D3445, MARCH 1990-REVISED OCTOBER 1990

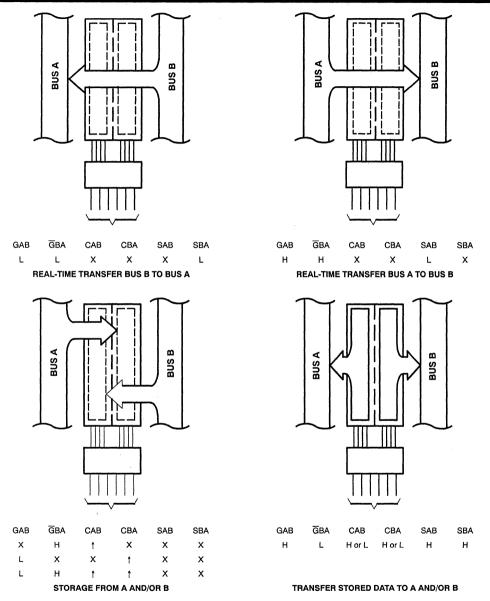


Figure 1. Bus Transfer Diagram



54ACT11651, 74ACT11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

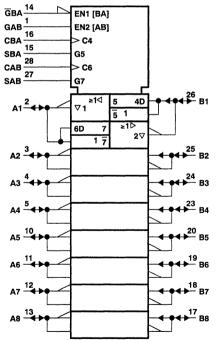
D3445, MARCH 1990-REVISED OCTOBER 1990

FUNCTION TABLE

		INP	JTS			DAT	A I/O	OPERATION OR FUNCTION
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	×	Input	Input	Isolation
L	н	î	1	×	×	Input	Input	Store A and B Data
×	Н	1	HorL	×	×	Input	Unspecified [†]	Store A, Hold B
Н	н	1	f	x‡	×	Input	Output	Store A in both registers
L	×	H or L	1	×	×	Unspecified [†]	Input	Hold A, Store B
L	L	î	1	×	X‡	Output	Input	Store B in both registers
L	L	Х	X	×	L	Output	Input	Real-Time B data to A Bus
L	L	х	HorL	×	н	Output	Input	Stored B Data to A Bus
Н	Н	Х	X	L	×	Input	Output	Real-Time A Data to B Bus
Н	н	H or L	Х	н	×	Input	Output	Stored A Data to B Bus
Н	L	H or L	HorL	н	н	Output	Output	Stored A Data to B Bus and
1				ĺ				Stored B Data to A Bus

[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol§



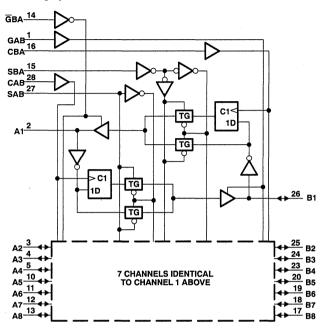
[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



[‡] Select control = L: clocks can occur simultaneously. Select control = H: clocks must be staggered in order to load both registers.

D3445, MARCH 1990-REVISED OCTOBER 1990

logic diagram (positive logic)



Pin numbers shown are for DW, JT, or NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Note 1) .	
Input clamp current, IIK (VI < 0 or VI > VC	bC) ± 20 mA
Output clamp current, IOK (VO < 0 or VO	> V _{CC}) ± 50 mA
Continuous output current, IO (VO = 0 to	v V _{CC}) ± 50 mA
Continuous current through V _{CC} or GND	pins ± 200 mA
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3445, MARCH 1990-REVISED OCTOBER 1990

recommended operating conditions

		SI	SN54ACT11651			4ACT11	651	
		MIN	NO	MAX N	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5		5 5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			6.0			0.8	٧
VI	Input voltage	(,	√ Vcc	0		Vcc	٧
Vo	Output voltage	(1	Vcc	0		Vcc	٧
ЮН	High-level output current		77°	- 24			- 24	mA
loL	Low-level output current	~c		24			24	mA
Δt/Δν	Input transition rise or fall rate	6,0		10	0		10	ns/V
TA	Operating free-air temperature	- 5	5	125	- 40		85	ŝ

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST COMPLETIONS		T,	Δ = 25°C	;	54ACT	11651	74ACT	11651	UNIT
PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			4.5 V	4.4			4.4		4.4		
		IOH = - 50 μA	5.5 V	5.4			5.4		5.4		
		I _{OH} = - 24 mA	4.5 V	3.94			3.7		3.8		v
∨он		IOH - ZTIIIA	5.5 V	4.94			4.7		4.8		· ·
		IOH = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = - 75 mA [†]	5.5 V						3.85		
		ΙΟΙ = 50 μΑ	4.5 V			0.1		0.1		0.1	
		10[= 30 μΛ	5.5 V			0.1		€ Q.1		0.1	
V		I _{OL} = 24 mA	4.5 V			0.36	70	₹0.5		0.44	V
VOL		IOL = 24 IIIA	5.5 V			0.36	\$P.X	0.5		0.44	٧
		IOL = 50 mA [†]	5.5 V				-QV	1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	A or B ports§	V _I = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μΑ
l _j	Control Inputs	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μА
Icc		VI = VCC or GND, IO = 0	5.5 V			8		160		80	μΑ
∆ICC [‡]		V _I = V _{CC} or GND	5.5 V			0.9		1		1	mA
Ci	Control inputs	VI = VCC or GND	5 V		4.5						pF
Cio	A or B ports	V _I = V _{CC} or GND	5 V		10						рF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

		T _A =	T _A = 25°C		1651	74ACT	11651	UNIT
l		MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency	0	90	0 .(3 ,90	0	90	MHz
tw	Pulse duration, CAB or CBA high or low	5.5		5,50	\$7°	5.5		ns
t _{su}	Setup time, A before CAB† or B before CBA†	4.5		Q4.50°		4.5		ns
th	Hold time, A after CAB↑ or B after CBA↑	2		₹ž		2		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

54ACT11651, 74ACT11651 OCTAL BUS TRANSCEIVERS AND REGISTERS

D3445, MARCH 1990-REVISED OCTOBER 1990

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	то	Т,	4 = 25°C	;	54ACT	11651	74ACT	11651	LIMIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax			90			90		90		MHz
t _{PLH}	A or B	B or A	2.6	5.6	8.9	2.6	10.7	2.6	9.9	ns
tPHL t	7 701 5	BOIA	4.7	7.7	10.7	4.7	12.8	4.7	11.9	113
t _{PLH}	CBA or CAB	A or B	5.5	8.4	11.2	5.5	13.8	5.5	12.7	
t _{PHL}	CBA OF CAB	7012	6.3	9.5	12.7	6.3	15.3	6.3	14.1	ns
tPLH .	SBA or SAB†	A or B	4.8	7.6	10.4	4.8	12.9	4.8	11.8	ns
t _{PHL}	with A or B high	7016	4.1	7.7	11.2	4.1	13.3	4.1	12.4	115
t _{PLH}	SBA or SAB†	A D	3	6.2	9.3	.30	[ु] ू)1.3	3	10.4	
^t PHL	with A or B low	A or B	5.6	8.7	11.7	\$.60	14.1	5.6	13	ns
^t PZH	- GBA		4	7.4	10.7	₹4	12.9	4	11.9	
†PZL	GBA	Α	4.3	8.2	11.9	4.3	14.5	4.3	13.3	ns
^t PHZ	- GBA	A	5.9	7.7	9.5	5.9	10.4	5.9	10	
^t PLZ	GBA	^	5.1	6.9	8.7	5.1	9.6	5.1	9.2	ns
^t PZH	GAB	В	5.9	9	12.1	5.9	15.1	5.9	13.7	ns
t _{PZL}	GAB	В	6.4	9.8	13.2	6.4	16.3	6.4	14.9	115
tpHZ	GAB	В	4.7	7.1	9.5	4.7	10.7	4.7	10	ns
tpLZ] JAB		3.8	6.1	8.4	3.8	9.1	3.8	8.8	115

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CON	TYP	UNIT	
C	Power dissipation capacitance per gate	Outputs enabled	C _I = 50 pF,	f = 1 MHz	61	pF
Cpd	orrer dissipation capacitance per gate	Outputs disabled	OL - 30 pr,	1 - 1 1/11/12	15	۱ ۲۰

D3107, DECEMBER 1989-REVISED OCTOBER 1990

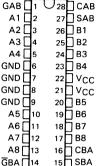
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

description

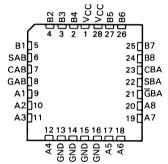
These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and reaisters.

54AC11652...JT PACKAGE 74AC11652...DW OR NT PACKAGE

(TOP VIEW)



54AC11652 . . . FK PACKAGE (TOP VIEW)



Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{GBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 54AC11652 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11652 is characterized for operation from -40° C to 85°C.

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D3107, DECEMBER 1989-REVISED OCTOBER 1990

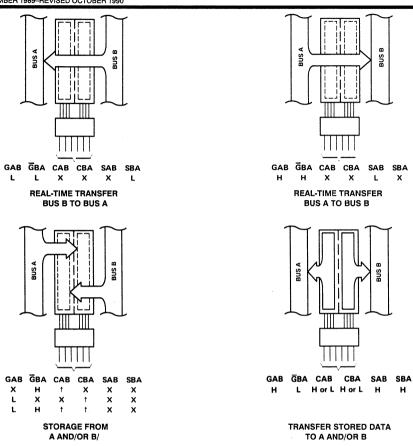


FIGURE 1. BUS TRANSFER DIAGRAM

D3107, DECEMBER 1989-REVISED OCTOBER 1990

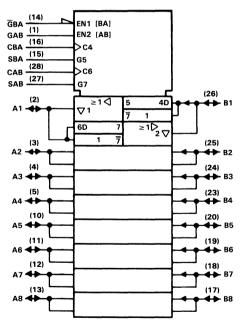
FUNCTION TABLE

		INP	UTS			DATA	A I/O†	OPERATION OR FUNCTION
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OFERATION ON FONCTION
L	Н	H or L	H or L	Х	Х	Innut	Input	Isolation
L	н	Ť	†	Х	Х	Input	mput	Store A and B Data
Х	Н	î	H or L	Х	Х	Input	Unspecified [†]	Store A, Hold B
Н	н	Ť	†	X‡	Х	Input	Output	Store A in both registers
L	Х	H or L	†	Х	Х	Unspecified [†]	Input	Hold A, Store B
L	L	1	1	Х	X‡	Output	Input	Store B in both registers
L	L	Х	Х	Х	L	Output	Input	Real-Time B Data to A Bus
L	L	Х	H or L	х	Н	Output	mput	Stored B Data to A Bus
Н	Н	Х	X	L	Χ	I	0.45.4	Real-Time A Data to B Bus
Н	н	H or L	X	Н	Х	Input	Output	Stored B Data to B Bus
Н		H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and
"	١ ١	HOL	H Of L	, n	п	Output	Culput	Stored B Data to A Bus

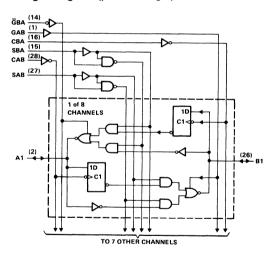
[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



[‡] Select control = L: clocks can occur simultaneously.

[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3107, DECEMBER 1989-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC		. $$ –0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5	V to VCC+0.5 V
Output voltage range, VO (see Note 1)	-0.5	V to VCC+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)		±50 mA
Continuous output current, IO (VO = 0 to VCC)		±50 mA
Continuous current through VCC or GND pins		±200 mA
Storage temperature range		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			5	4AC116	52	74	4AC1165	52	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage		3	5	5.5	3	5	5.5	V
-		V _{CC} = 3 V	2.1			2.1			
V_{IH}	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15	_		٧
		$V_{CC} = 5.5 V$	3.85			3.85			
		V _{CC} = 3 v			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	٧
		V _{CC} = 5.5 V		4.	1.65			1.65	
VI	Input voltage		0	£	Vcc	0		VCC	٧
Vo	Output voltage		0	£2	Vcc	0		VCC	٧
		V _{CC} = 3 V		24"	-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V		€) <u> </u>	-24			-24	mA
		$V_{CC} = 5.5 V$	Š	Ş	-24			-24	
		V _{CC} = 3 V	8		12			12	
IOL	Low-level output current	$V_{CC} = 4.5 \text{ V}$			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate	Control pins	0		5	0		5	ns/V
Δι/Δν	input transition rise of fail rate	Data	0		10	0		10	115/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

D3107, DECEMBER 1989-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D.A	DAMETED	TEST CONDITIONS	\\\	Т	A = 25°	°C	54AC	11652	74AC	11652	LIMIT
PA	RAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			3 V	2.9			2.9		2.9		
		$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
Vou		I _{OH} = -4 mA	3 V	2.58			2.4		2.48		v
VOH		I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8	1	v
		10H = -24 IIIA	5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
		1 _{OH} = -75 mA [†]	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		<u>></u> 0.1		Q.1	
W		I _{OL} = 12 mA	3 V			0.36		0.5		0.44	v
VOL		I _{OL} = 24 mA	4.5 V			0.36	\$2.7 \$4.7	0.5		0.44	٧
		IOL - 24 IIIA	5.5 V			0.36	ja.	0.5		0.44	
		IOL = 50 mA [†]	5.5 V				5	1.65			
		I _{OL} = 75 mA [†]	5.5 V				ŝ			1.65	
loz‡	A or B ports	V _O = V _{CC} or GND	5.5 V			±0.5	a a	±10		±5	μΑ
11	Control pins	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
Ci	Control pins	V _I = V _{CC} or GND	5 V		4.5						pF
Cio	A or B ports	VO = VCC or GND	5 V		12						рF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

	PARAMETER	TA =	25°C	54AC	11652	74AC11652		UNIT
	PANAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	65	0	.∱. 65	0	65	MHz
tw	Pulse duration, CAB or CBA high or low	7.7		7.7	22	7.7		ns
t _{su}	Setup time, A before CAB [↑] or B before CBA [↑]	6		୍ଦ 6େ	377	6		ns
th	Hold time, A after CABT or B after CBAT	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

		T _A =	T _A = 25°C		11652	74AC11652		UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	105	0	105	1	105	MHz
t _w	Pulse duration, CAB or CBA high or low	4.8		4.8		4.8		ns
t _{su}	Setup time, A before CABT or B before CBAT	4.5		4.5		4.5		ns
th	Hold time, A after CABT or B after CBAT	1		12		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

D3107, DECEMBER 1989-REVISED OCTOBER 1990

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	Т	A = 25°	C	54AC	11652	74AC	11652	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			65			65		65		MHz
^t PLH	A or B	B or A	2.9	8.5	11.1	2.9	13.9	2.9	12.9	ns
[†] PHL	X 01 B	DOIA	3.9	10.3	12.9	3.9	14.9	3.9	14.2	113
[†] PLH	CBA or CAB	A or B	4.3	11.2	14.3	4.3	17.6	4.3	16.2	ns
[†] PHL	ODA OF OAD	AOID	5.3	13.1	16.2	5.3	18.7	5.3	17.8	113
t _{PLH}	SBA or SAB†	A or B	3.4	9.4	12	3.4	14.7	3.4	13.7	ns
t _{PHL}	with A or B high	AUID	4.7	11.5	14.3	4.7	6.5	4.7	15.6	113
[†] PLH	SBA or SAB†	A or B	3.9	10.5	13.3	3.9	₹16.1	3.9	14.9	ns
t _{PHL}	with A or B low	AOID	4.8	12.1	16.3	4.8	3 18.5	4.8	17.7	113
^t PZH	ĞВА	Α	4.3	11.1	14.5	4.3	17.8	4.3	16.5	ns
tPZL	GDA	^	5.2	14.4	19.8	5.2	23.4	5.2	22	113
tPHZ	ĞВА	٨	3.7	6.4	8.1	3.7	8.7	3.7	8.5	
tPLZ	GBA	A	3.5	6	7.8	3.5	8.4	3.5	8.2	ns
^t PZH	GAB	В	4.7	11.6	15	4.7	18.3	4.7	16.9	
tPZL	GAB	В	5.6	14.8	19.9	5.6	23.4	5.6	21.9	ns
[†] PHZ		В	4	6.6	8.2	4	8.8	4	8.6	ns
t _{PLZ}	GAD		3.5	6.1	7.7	3.5	8.2	3.5	8	115

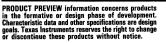
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	ТО	T	A = 25°	C	54AC	11652	74AC11652		UNIT
PANAMEIEN	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			105			105		105		MHz
[†] PLH	A or B	B or A	2.4	5.2	7.6	2.4	9.2	2.4	8.6	ns
t _{PHL}	AUID	βUA	3.1	6	8.7	3.1	10.1	3.1	9.6	115
[†] PLH	CBA or CAB	A or B	3.6	6.7	9.5	3.6	11.5	3.6	10.7	
t _{PHL}	CDA OF CAB	AUID	4.4	7.8	10.8	4.4	12.8	4.4	12	ns
t _{PLH}	SBA or SAB [†]	A or B	2.9	5.6	8.1	2.9	9.7	2.9	9.1	ns
tPHL	with A or B high	AOIB	3.8	6.9	9.6	3.8	्री1.4	3.8	10.7	115
t _{PLH}	SBA or SAB [†]	A or B	3.3	6.2	8.8	3.3	10.5	3.3	9.9	ns
tPHL	with A or B low	AUID	4	7.1	9.9	4 (11.5	4	10.9	115
tPZH	GBA	A	3.3	6.6	9.6	3.3	11.6	3.3	10.9	
tPZL	GDA	A	4.2	7.4	10.9	4.2	13	4.2	12.2	ns
tPHZ	GBA	Λ	3.6	5.5	7.2	3.6	7.8	3.6	7.6	
[†] PLZ	GBA	Α	3.3	5	6.7	3.3	7.2	3.3	7.1	ns
^t PZH	GAB	В	4.1	7.2	10.1	4.1	12.2	4.1	11.3	
[†] PZL	GAD	D	4.6	7.9	11.1	4.6	13.2	4.6	12.3	ns
tPHZ	GAB	В	3.9	5.6	7.3	3.9	7.8	3.9	7.6	
tPLZ	GAB	D	3.4	5.2	6.8	3.4	7.4	3.4	7.2	ns

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

		PARAMETER		TEST CONDITIONS	TYP	UNIT
	~ .	Power dissipation capacitance per transceiver	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	60	pF
L	-pd 	rower dissipation capacitance per transceiver	Outputs disabled	CL = 50 pr, 1 = 1 Winz	14	Pi





D3106, DECEMBER 1989

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs

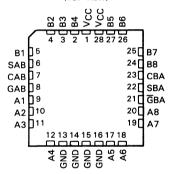
description

These devices consist of bus transceiver circuits. D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enables GAB and $\overline{G}BA$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

54ACT11652 ... JT PACKAGE 74ACT11652 ... DW OR NT PACKAGE (TOP VIEW)

GAB ☐	1 U	28	САВ
A1 📮	2	27	SAB
A2 🔲	3	26	⊒ B1
АЗ 🗌	4	25	☐ B2
A4 🗌	5	24	_] B3
GND 🗌	6	23	_] B4
	7	22	⊒∨cc
GND 🗌	8	21	∃∨cc
GND 🗌	9	20] B5
A5 🗌	10	19] B6
A6 [11	18	B7
A7 🛚	12	17] B8
A8 🛚	13	16	СВА
GBA ☐	14	15	SBA

54ACT11652 . . . FK PACKAGE



Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 54ACT11652 is characterized for operation over the full military temperature range of $-55^{\circ}C$ to $125^{\circ}C$. The 74ACT11652 is characterized for operation from $-40^{\circ}C$ to $85^{\circ}C$.

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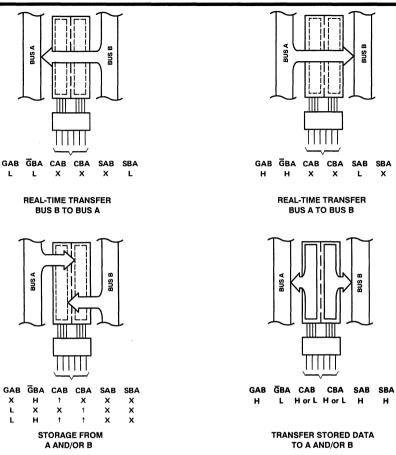


FIGURE 1. BUS TRANSFER DIAGRAM

D3106, DECEMBER 1989

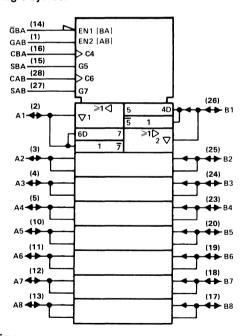
FUNCTION TABLE

		INP	UTS			DATA	A I/O†	OPERATION OR FUNCTION
GAB	GBA	CAB	СВА	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	In m A	lan	Isolation
L	н	1	1	Х	х	Input	Input	Store A and B Data
Х	Н	<u>†</u>	H or L	Х	Х	Input	Unspecified [†]	Store A, Hold B
н	н	1	1	χ‡	х	Input	Output	Store A in both registers
L	Х	H or L	Ť	X	Х	Unspecified [†]	Input	Hold A, Store B
L	L	1	1	X	χ‡	Output	Input	Store B in both registers
L	L	X	Х	Х	L	Outroit	lanut	Real-Time B Data to A Bus
L	L	X	H or L	Х	н	Output	Input	Stored B Data to A Bus
Н	Н	Х	Х	L	Х	lmm. st	0.45.4	Real-Time A Data to B Bus
Н	н	H or L	X	Н	Х	Input	Output	Stored A Data to B Bus
Н	L	H or L	H or L	Н	н	Outnut	Outnut	Stored A Data to B Bus and
"	-	HOIL	HOLL	П		Output	Output	Stored B Data to A Bus

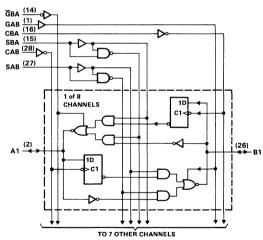
[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Select control = H: clocks must be staggered in order to load both registers.

logic symbol§



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



[‡] Select control = L: clocks can occur simultaneously.

[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3106, DECEMBER 1989

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, VCC		0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5	V to VCC+0.5 V
Output voltage range, VO (see Note 1)	-0.5	V to VCC+0.5 V
Input clamp current, IK (Al < 0 or Al > ACC)		±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)		±50 mA
Continuous output current, IO (VO = 0 to VCC)		±50 mA
Continuous current through VCC or GND pins		±200 mA
Storage temperature range		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54AC	T11652	74ACT	11652	UNIT
		MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage	4.5	5.5	4.5	5.5	٧
VilH	High-level input voltage	2	,3	2		٧
VIL	Low-level input voltage		\$0.8		0.8	٧
VĮ	Input voltage	0	₹Vcc	0	Vcc	٧
Vo	Output voltage	Q (VCC	0	Vcc	٧
ЮН	High-level output current	ें	-24		-24	mA
lOL	Low-level output current	, gi	24		24	mA
Δt/Δν	Input transition rise or fall rate	~ 0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C



NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

D3106, DECEMBER 1989

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	RAMETER	TEST CONDITIONS	V	T	A = 25	°C	54AC	Γ11652	74AC1	11652	UNIT
FA	MANIETEN	1E31 CONDITIONS	v _C C	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
		l _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
		10H = -30 μA	5.5 V	5.4			5.4		5.4		
V		IOH = -24 mA	4.5 V	3.94			3.7		3.8		v
VOH		10H = -24 IIIA	5.5 V	4.94			4.7		4.8		
		I _{OH} = -50 mA [†]	5.5 V				3.85				
		I _{OH} = -75 mA [†]	5.5 V						3.85		
		Ι _{ΟL} = 50 μΑ	4.5 V			0.1		₷ 0.1		0.1	
		ΙΟΓ = 20 μΑ	5.5 V			0.1		0.1		0.1	
V		IOL = 24 mA	4.5 V			0.36	á	0.5		0.44	٧
VOL		IOL = 24 IIIA	5.5 V			0.36	Ô	0.5		0.44	V
		I _{OL} = 50 mA [†]	5.5 V				ें ਹ	1.65			
		I _{OL} = 75 mA [†]	5.5 V				, S			1.65	
loz	A or B ports‡	V _O = V _{CC} or GND	5.5 V			±0.5	- 40	±10		±5	μΑ
l _l	GAB or GBA	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μА
ΔICC§		One input at 3.4 V, Other inputs at GND or VCC	5.5 V			0.9		1		1	mA
Ci	GAB or GBA	V _I = V _{CC} or GND	5 V		4.5						pF
Co	A or B ports	V _O = V _{CC} or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Note 2)

	PARAMETER	T _A =	25°C	54AC	Γ11652	74ACT	Г11652	UNIT
	PANAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency	0	105	0	105	0	105	MHz
tw	Pulse duration, CAB or CBA high or low	4.8		4.8	16.70	4.8		ns
t _{su}	Setup time, A before CLK† or B before CBA†	4		₹ 4	,	4		ns
th	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		2.5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

D3106, DECEMBER 1989

switching characteristics (see Note 2)

PARAMETER	FROM	TO	T	A = 25°	Č	54ACT	11652	74AC1	Γ11652	UNIT
PANAMEIEN	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			105			105		105		MHz
^t PLH	A or B	B or A	3.8	7	9.9	3.8	11.9	3.8	11.1	ns
tPHL	AOID	BULA	3.4	6.7	10.7	3.4	12.2	3.4	11.6	115
[†] PLH	CBA or CAB	A or B	5.4	8.4	11.8	5.4	14.1	5.4	13.1	ns
^t PHL	CDA OI CAD	AOIB	6.1	9.4	13.1	6.1	15.3	6.1	14.4	115
^t PLH	SBA or SAB†	A or B	2.8	6.2	10.1	2.8	11.8	2.8	11	ns
^t PHL	with A or B high		5.5	8.7	12.1	5.5	14.1	5.5	13.3	115
^t PLH	SBA or SAB†	A or B	4.9	7.8	11	4.9	3.2	4.9	12.2	ns
^t PHL	with A or B low	AOIB	3.9	7.5	11.6	3.9	13.3	3.9	12.6	113
^t PZH	GBA	A	3.3	7.2	11.4	3.3	13.5	3.3	12.6	
t _{PZL}	GDA	^	4.1	7.8	12.6	4,1	14.7	4.1	13.8	ns
t _{PHZ}	GBA		5.2	7.2	9.3	5.2	10.4	5.2	9.9	
t _{PLZ}	GDA	A	4.8	6.7	8.6	4.8	9.7	4.8	9.3	ns
tpzH	CAR	В	5.1	9.1	13.4	5.1	16.7	5.1	15.2	
tPZL	GAB	В	5.8	9.7	14.2	5.8	17.6	5.8	16.1	ns
tPHZ	GAB	В	3.4	6.8	9.7	3.4	10.8	3.4	10.3	
t _{PLZ}	GAD	D D	3.1	6	8.8	3.1	9.7	3.1	9.3	ns

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, VCC = 5 V, TA = 25°C

	PARAMETER		TEST CONDITIONS	TYP	UNIT
C .	Power dissipation capacitance per transceiver	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	59	pF
Cpd	rower dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pH}, T = 1 \text{ MHz}$	14	PΓ

- High-Speed Bus Transceivers With Parity Generator/Checker
- Parity-Error-Flag Open-Drain Output
- Register for Storage of the Parity-Error Flag
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

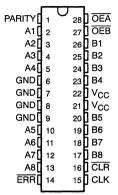
description

The 'AC11833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the \overline{ERR} output will indicate whether or not an error in the B data has occurred. The output enable inputs \overline{OEA} and \overline{OEB} can be used to disable the device so that the buses are effectively isolated.

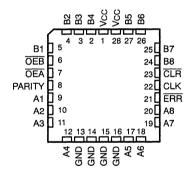
A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity error flag (ERR). ERR is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the CLR input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54AC11833 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11833 is characterized for operation from – 40°C to 85°C.

54AC11833 . . . JT PACKAGE 74AC11833 . . . DW OR NT PACKAGE (TOP VIEW)



54AC11833 . . . FK PACKAGE (TOP VIEW)



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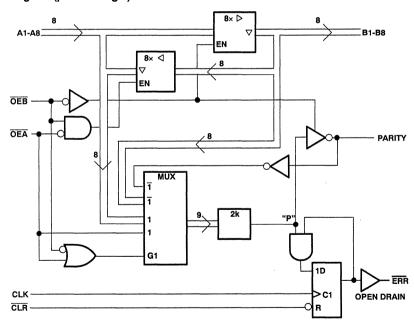
PRODUCT PREVIEW

Function Table

			INPUT	S			OUTF	PUT AND I/O)	
OEB	OEA	CLR	CLK	Ai Σ of H's	Bi [†] Σ of H's	A	В	PARITY	ERR	FUNCTION
L	Н	Х	х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and Generate Parity
Н	L	н	1	NA	Odd Even	В	NA	NA	ΓI	B Data to A Bus and Check Parity
Х	Х	L	Х	Х	Х	Х	NA	NA	Н	Clear Error Flag Register
Н	н	H L H	No† No† †	X X Odd Even	×	z	z	z	riiS	Ișolation‡
L	L	х	х	Odd Even	NA	NA	Α	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

logic diagram (positive logic)





[†] Summation of high-level inputs includes PARITY along with Bi inputs.

[‡] In this mode, the ERR output, when clocked, shows inverted parity of the A bus.

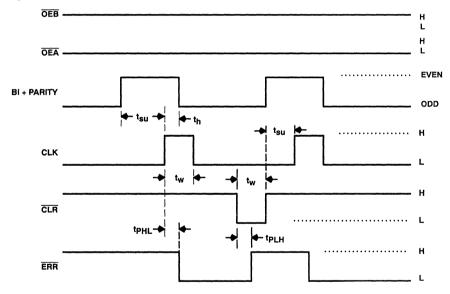
PRODUCT PREVIEW

Error-Flag Function Table

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	ОИТРИТ	FUNCTION
CLR	CLK	POINT "P"	ERR n-1	ERR	
н	1	н	н	н	
н	1	x	L	L	Sample
н	1	L	X	L	
L X		х	X	н	Clear

ERR n-1 represents the state of the ERR output before any changes at CLR, CLK, or point "P".

error-flag waveforms





54AC11833, 74AC11833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3448, MARCH 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	– 0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±225 mA
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1183	3	74	AC1183	3	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		3	5	5.5	3	5	5.5	٧
		V _{CC} = 3 V	2.1			2.1			
VIH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	٧
		V _{CC} = 5.5 V			1.65			1.65	
٧ı	Input voltage		0		Vcc	0		Vcc	٧
Vo	Output voltage		0		Vcc	0		Vcc	٧
		V _{CC} = 3 V			-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V			- 24			- 24	mΑ
		V _{CC} = 5.5 V			- 24			- 24	
		V _{CC} = 3 V			12			12	
loL	Low-level output current	V _{CC} = 4.5 V			24			24	mΑ
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	Vcc	T,	A = 25°C		54AC	11833	74AC1	1833	UNIT
	FARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
ЮН	ERR	VO = VCC	5.5 V			0.5		10		5	μΑ
			3 V	2.9			2.9		2.9		
		IOH = - 50 μA	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
Va.,	All outputs except	IOH = - 4 mA	3 V	2.58			2.4		2.48		V
VOH	ERR	I _{OH} = ~ 24 mA	4.5 V	3.94			3.7		3.8		V
		1	5.5 V	4.94			4.7		4.8		
		I _{OH} = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = ~ 75 mA [†]	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		IOL = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
\/		I _{OL} = 12 mA	3 V			0.36		0.5		0.44	٧
VOL		Ja. 04 mA	4.5 V			0.36		0.5		0.44	V
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		I _{OL} = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	A or B ports, PARITY	VO = VCC or GND	5.5 V			± 0.5		± 10		± 5	μΑ
IJ	OEA, OEB, CLK, and CLR	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ
lcc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	OEA, OEB, CLK, and CLR	V _I = V _{CC} or GND	5 V		4.5						pF
C _{io}	A or B ports, PARITY	VO = VCC or GND	5 V		12						pF

The Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

			T _A = :	T _A = 25°C		54AC11833		74AC11833	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		CLK high	5		5		5		
t _W	Pulse duration	CLK low	5	5	5		5		ns
	Pulse duration	CLR low	5		5		5		
	Saturations hafara CLVA	Bi and PARITY	14		14		14		
tsu	Setup time before CLK↑	CLR inactive	2		2		2		ns
th	Hold time after CLK ↑, Bi and	PARITY	0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



54AC11833, 74AC11833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3448, MARCH 1990-REVISED OCTOBER 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

			T _A =	T _A = 25°C		11833	74AC11833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		CLK high	5		5		5		
tw	Pulse duration	CLK low	5		5		5		ns
1		CLR low	. 5		5		5		
	Setup time before CLIVA	Bi and PARITY	14		14		14		
tsu	Setup time before CLK↑	CLR inactive	2		2		2		ns
th	Hold time after CLK ↑, Bi and	PARITY	0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

	PARAMETER	TEST CO	TYP	UNIT			
		0.44	A to B	0 50-5	4 4 1411-	87	
١, .	Power dissipation capacitance per transceiver	Outputs enabled B to A C _L = 50 pF, f = 1 MH		f = 1 MHz	60	pF	
C _{pd}	rower dissipation capacitatice per transceiver	Outputs disabled	A to B	C. = 50.55	f = 1 MHz	28	pF
		Outputs disabled	B to A	C _L = 50 pF,	1 = 1 WITZ	8	pΓ



54ACT11833, 74ACT11833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3449, MARCH 1990-REVISED OCTOBER 1990

- Inputs are TTL-Voltage Compatible
- High-Speed Bus Transceivers With Parity Generator/Checker
- Parity-Error-Flag Open-Drain Output
- Register for Storage of the Parity-Error Flag
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

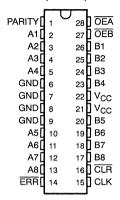
The 'ACT11833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the ERR output will indicate whether or not an error in the B data has occurred. The output enable inputs OEA and OEB can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity

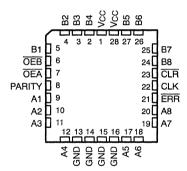
error flag (ERR). ERR is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the CLR input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54ACT11833 is characterized for operation over the full military temperature range of $-55^{\circ}C$ to $125^{\circ}C$. The 74ACT11833 is characterized for operation from $-40^{\circ}C$ to $85^{\circ}C$.

54ACT11833 ... JT PACKAGE 74ACT11833 ... DW OR NT PACKAGE (TOP VIEW)



54ACT11833 . . . FK PACKAGE (TOP VIEW)



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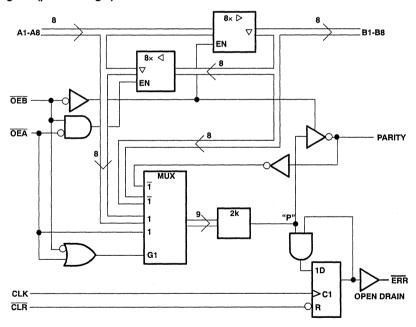


Function Table

			INPUT	S			OUTF	PUT AND I/O)	
OEB	OEA	CLR	CLK	Ai Σ of H's	Bi [†] Σ of H's	А	В	PARITY	ERR	FUNCTION
L	Н	Х	Х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and Generate Parity
Н	L	Н	1	NA	Odd Even	В	NA	NA	ΓI	B Data to A Bus and Check Parity
X	X	L	Х	Х	Χ	Х	NA	NA	Н	Clear Error Flag Register
н	Н	H L H	No† No† †	X X Odd Even	×	z	z	Z	r I I S	Isolation [‡]
L	L	х	Х	Odd Even	NA	NA	Α	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

logic diagram (positive logic)





[†] Summation of high-level inputs includes PARITY along with Bi inputs.

[‡] In this mode, the ERR output, when clocked, shows inverted parity of the A bus.

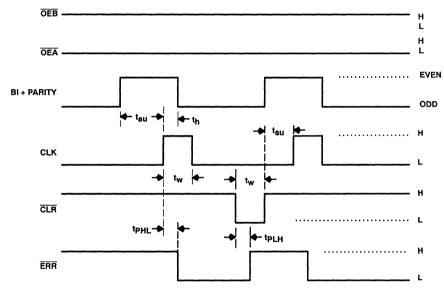
BODIICT PREVIEW

Error-Flag Function Table

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	ОИТРИТ	FUNCTION
CLR	CLK	POINT "P"	ERR n-1	ERR	
Н	1	н	н	Н	
Н	1	x	L	L	Sample
Н	†	L	x	L	
L	Х	X	x	Н	Clear

ERR n-1 represents the state of the ERR output before any changes at CLR, CLK, or point "P".

error-flag waveforms



54ACT11833, 74ACT11833 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3449, MARCH 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND pins	±225 mA
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54	54ACT11833			ACT118	33	
	,	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIН	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
٧ı	Input voltage	0		Vcc	0		Vcc	٧
٧o	Output voltage	0		Vcc	0		Vcc	٧
ЮН	High-level output current			- 24			- 24	mA
lOL	Low-level output current			24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	- 55		125	40		85	°C



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

JCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST COMPLETIONS	.,	T,	Δ = 25°C	;	54ACT	11833	74ACT	11833	
	PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			4.5 V	4.4			4.4		4.4		
		ΙΟΗ = - 50 μΑ	5.5 V	5.4			5.4		5.4		
	All outputs except		4.5 V	3.94			3.7		3.8		
∨он	ERR	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		V
		IOH = - 50 mA†	5.5 V				3.85				
	1	1 _{OH} = - 75 mA [†]	5.5 V						3.85		
		L 50 A	4.5 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	
1/			4.5 V			0.36		0.5		0.44	V
VOL		IOL = 24 mA	5.5 V			0.36		0.5		0.44	V
		I _{OL} = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
łį	OEA, OEB, CLK, and CLR	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ
loz	A or B ports, PARITY [‡]	VO = VCC or GND	5.5 V			± 0.5		± 10		± 5	μΑ
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μА
ΔlCC§	Ÿ	One input at 3.4 V, Other inputs at GND or VCC	5.5 V			0.9		1		1	mA
Ci	OEA, OEB, CLK, and CLR	V _I = V _{CC} or GND	5 V		4.5						
C _{io}	A or B ports, PARITY	VO = VCC or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

			T _A =	T _A = 25°C		54ACT11833		74ACT11833	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		CLK high	5		5		5		
tw	Pulse duration	CLK low	5		5		5		ns
		CLR low		5		5			
	0	Bi and PARITY	14		14		14		
t _{su}	Setup time before CLK↑	CLR inactive	2		2		2		ns
th	Hold time after CLK ↑, Bi and	PARITY	0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST COI	TYP	UNIT			
			A to B	0 50 5		87	
	Danier diseisation conseitance and transcripes	Outputs enabled B to A C _L = 50 pF, f = 1 MHz			60	pF	
C _{pd}	Power dissipation capacitance per transceiver	Outside disabled	A to B	C. F0.=F	4 1 MH=	28	
		Outputs disabled	B to A	C _L = 50 pF,	f = 1 MHz	8	рF



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

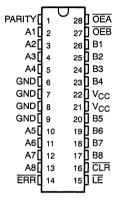
- High-Speed Bus Transceivers With Parity Generator/Checker
- Parity-Error-Flag Open-Drain Output
- Register for Storage of the Parity-Error Flag
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'AC11853 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the ERR output will indicate whether or not an error in the B data has occurred. The output-enable inputs OEA and OEB can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity-

54AC11853 . . . JT PACKAGE 74AC11853 . . . DW OR NT PACKAGE (TOP VIEW)



54AC11853 . . . FK PACKAGE (TOP VIEW)

B₁ 25 B7 OEB **B8** 24 OEA T 23 CLR PARITY LE 22 Α1 П 9 21 TERR A2 10 20 A8 19 A7 АЗ

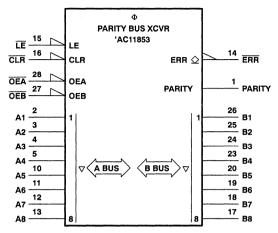
error flag (ERR). ERR can be either passed, sampled, stored, or cleared from the latch using the LE and CLR control inputs. The error flag register is cleared with a low pulse on the CLR input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54AC11853 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11853 is characterized for operation from -40° C to 85°C.

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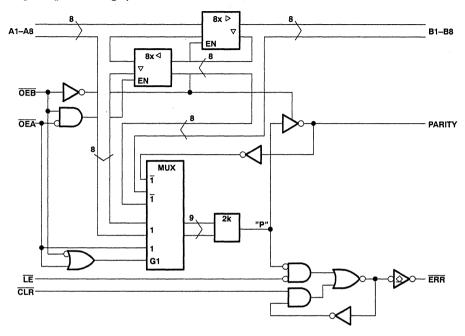
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984. Pin numbers shown are for DW, JT, and NT packages.

D3473, MARCH 1990

logic diagram (positive logic)



FUNCTION TABLE

			INPUT	S			OUT	PUT AND I/	0	
OEB	OEA	CLR	LE	Ai Σ of H's	Bi [†] Σ of H's	А	В	PARITY	ERR‡	FUNCTION
L	н	х	х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and Generate Parity
Н	L	х	L	NA	Odd Even	В	NA	NA	H L	B Data to A Bus and Check Parity
Н	L	Н	Н	NA	X	Х	NA	NA	NC	Store Error Flag
×	Х	L	Н	X	Х	Х	NA	NA	Н	Clear Error Flag Register
Н	Н	H L X	H H L L	X X L Odd H Even	x	z	z	z	NC H H L	Isolation [§] (Parity check)
L	L	х	х	Odd Even	NA	NA	Α	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

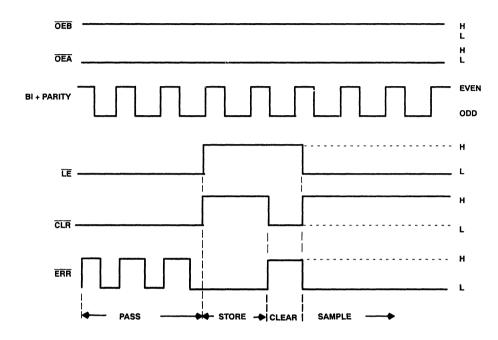
† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume the ERR output was previously high.

§ In this mode, the ERR output, when enabled, shows inverted parity of the A bus.



error-flag waveforms



ERROR FLAG FUNCTION TABLE

ERROR FEAG TOROTTON TABLE												
	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	ОИТРИТ	FUNCTION							
LE CLR		POINT "P"	ERR _{n-1} †	ERR								
L	L	L H	х	H	PASS							
L	н	L X H	X L H	H	SAMPLE							
Н	L	Х	X	Н	CLEAR							
н	н	x	L H	L H	STORE							

[†] ERRn-1 represents the state of the ERR output before any changes at CLR, LE, or point P.

54AC11853, 74AC11853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3473, MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Note 1)	. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54	AC1185	3	74AC11853			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
V_{IL}	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
VI	Input voltage		0		Vcc	0		Vcc	V
Vo	Output voltage		0		Vcc	0		Vcc	V
		V _{CC} = 3 V			-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V			- 24			- 24	mΑ
		V _{CC} = 5.5 V			- 24			- 24	
		V _{CC} = 3 V			12			12	
IOL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V	T,	Δ = 25°C		54AC	11853	74AC1	1853	UNIT
	FANAMETEN	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
IОН	ERR	VO = VCC	5.5 V			0.5		10		5	μΑ
			3 V	2.9			2.9		2.9		
		ΙΟΗ = – 50 μΑ	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
V	All outputs	IOH = - 4 mA	3 V	2.58			2.4		2.48		٧
∨он	except ERR	I _{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		V
		IOH = - 24 IIIA	5.5 V	4.94			4.7		4.8		
	1	I _{OH} = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = - 75 mA [†]	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		IOL = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
.,		I _{OL} = 12 mA	3 V			0.36		0.5		0.44	V
VOL			4.5 V			0.36		0.5		0.44	V
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA [†]	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	A or B ports, PARITY	V _O = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μΑ
lį	OEA, OEB, LE, and CLR	VI = VCC or GND	5.5 V			± 0.1		± 1		± 1	μΑ
^I CC		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μА
Ci	OEA, OEB, LE, and CLR	VI = V _{CC} or GND	5 V		4.5						pF
C _{iO}	A or B ports, PARITY	VO = VCC or GND	5 V	•	12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Note 2)

			T _A = 2	T _A = 25°C		1853	74AC11853		
			MIN		MAX	MIN	MAX	UNIT	
		LE high	5		5		5		
t _w	Pulse duration	LE low	5		5		5		ns
		CLR low	5		5		5		
	Cotum time hefere IEA	Bi and PARITY	14		14		14		
t _{su}	Setup time before LE↑	CLR inactive	2		2		2		ns
th	Hold time, Bi and PARITY af	ter LE↑	0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

54AC11853, 74AC11853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3473, MARCH 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

			TA = 25	5°C	54AC11853		74AC11853		UNIT
			MIN	MAX	MIN ,	MAX	MIN	MAX	UNII
		LE high	5		5		5		
tw	Pulse duration	LE low	5		5		5		ns
	i e	CLR low	5		5		5		
	Cotum time hafara IFI	Bi and PARITY	14		14		14		
tsu	Setup time, before LE↓	CLR inactive	2		2		2		ns
th	Hold time, Bi and PARITY after LE↓		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CO	NDITIONS	TYP	UNIT
		0.4.4.4.	A to B		87	
	Power dissipation capacitance per transceiver	Outputs enabled B to A	C EO nE 4 1 MH-	60	pF	
C _{pd}	rower dissipation capacitance per transceiver	Outputs disabled	A to B	C _L = 50 pF, f = 1 MHz	28	pr
		Outputs disabled	B to A	1	8	



54ACT11853, 74ACT11853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3474, MARCH 1990-REVISED OCTOBER 1990

- High-Speed Bus Transceivers With Parity Generator/Checker
- Parity-Error-Flag Open-Drain Output
- Register for Storage of the Parity-Error Flag
- Inputs are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

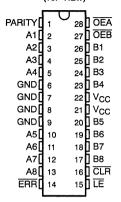
The 'ACT11853 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the \overline{ERR} output will indicate whether or not an error in the B data has occurred. The output-enable inputs \overline{OEA} and \overline{OEB} can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the

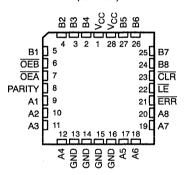
parity of the I/O ports with an open-drain parity-error flag (\overline{ERR}). \overline{ERR} can be either passed, sampled, stored, or cleared from the latch using the \overline{LE} and \overline{CLR} control inputs. The error flag register is cleared with a low pulse on the \overline{CLR} input. When both \overline{OEA} and \overline{OEB} are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54ACT11853 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74ACT11853 is characterized for operation from -40° C to 85°C.

54ACT11853...JT PACKAGE 74ACT11853...DW OR NT PACKAGE (TOP VIEW)



54ACT11853 . . . FK PACKAGE (TOP VIEW)



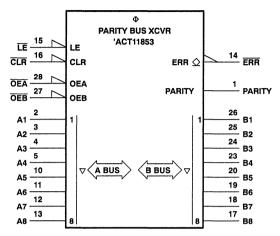
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54ACT11853, 74ACT11853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3474, MARCH 1990-REVISED OCTOBER 1990

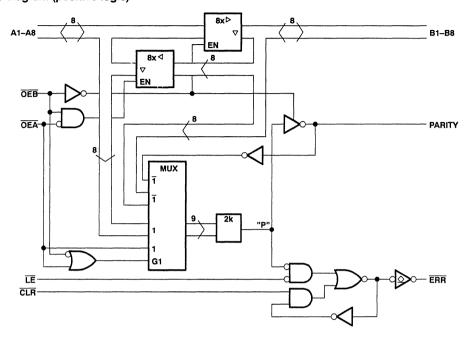
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984. Pin numbers shown are for DW, JT, and NT packages.

PRODUCT PREVIEW

logic diagram (positive logic)



FUNCTION TABLE

						CHON	1700	-		
			INPUT	S		i	OUT	PUT AND I/	0	
ŌĒB	OEA	CLR	ΪĒ	Al Σ of H's	Bi [†] Σ of H's	А	В	PARITY	ERR‡	FUNCTION
L	Н	х	х	Odd Even	NA	NA	Α	L H	NA	A data to B bus and Generate Parity
Н	L	х	L	NA	Odd Even	В	NA	NA	Г	B Data to A Bus and Check Parity
Н	L	Н	Н	NA	×	Х	NA	NA	NC	Store Error Flag
X	X	L	Н	X	×	Х	NA	NA	Н	Clear Error Flag Register
н	н	H L X	H H L	X X L Odd H Even	х	z	z	z	r i i S	Isolation [§] (Parity check)
L	L	х	×	Odd Even	NA	NA	Α	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

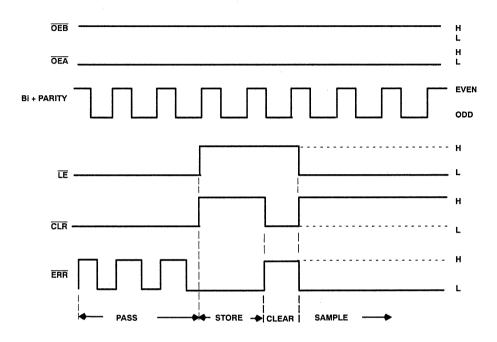
[†] Summation of high-level inputs includes PARITY along with Bi inputs.

[‡] Output states shown assume the ERR output was previously high.

[§] In this mode, the ERR output, when enabled, shows inverted parity of the A bus.

D3474, MARCH 1990-REVISED OCTOBER 1990

error-flag waveforms



ERROR FLAG FUNCTION TABLE

INP	INTERNAL OUTPUT		PRE-STATE	OUTPUT ERR	FUNCTION
		L	L		D. 00
<u> </u>	L	H	X	H	PASS
L	Н	X H	L H	L H	SAMPLE
Н	Ĺ	Х	X	Н	CLEAR
н	Н	х	L H	L H	STORE

[†] ERRn-1 represents the state of the ERR output before any changes at CLR, LE, or point P.

PRODUCT PREVIEW

absolute maximum	ratings over o	perating free-air	temperature ran	ige (unless	otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND pins	
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54.	ACT118	53	74.	ACT1185	53	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	٧
VI	Input voltage	0		Vcc	0		Vcc	V
Vo	Output voltage	0		Vcc	0		Vcc	V
ЮН	High-level output current			- 24			- 24	mA
lOL	Low-level output current			24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	- 55		125	- 40		85	°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEGT COMPLETIONS		T,	_A = 25°C	;	54ACT	11853	74ACT11853		
	PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			4.5 V	4.4			4.4		4.4		
		ΙΟΗ = – 50 μΑ	5.5 V	5.4			5.4		5.4		
11	All outputs except		4.5 V	3.94			3.7		3.8		
VOH	ERR	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		٧
		I _{OH} = - 50 mA [†]	5.5 V				3.85				
		I _{OH} = - 75 mA [†]	5.5 V						3.85		
			4.5 V		,	0.1		0.1		0.1	
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	
.,			4.5 V			0.36		0.5		0.44	
VOL		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	V
		IOL = 50 mA†	5.5 V					1.65			
		I _{OL} = 75 mA [†]	5.5 V							1.65	
ij	OEA, OEB, LE, and CLR	VI = VCC or GND	5.5 V			± 0.1		± 1		± 1	μΑ
loz	A or B ports, PARITY [‡]	V _O = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μА
lcc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
ΔICC§	,	One input at 3.4 V, Other inputs at GND or VCC	5.5 V			0.9		1		1	mA
Ci	OEA, OEB, LE, and CLR	VI = V _{CC} or GND	5 V		4.5						_
C _{io}	A or B ports, PARITY	V _O = V _{CC} or GND	5 V		12						рF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

			T _A = 25°C		54ACT11853		74ACT11853		UNIT
			MIN MAX	MIN	MAX	MIN	MAX	0	
		LE high	5		5		5	.,	
$t_{\mathbf{W}}$	Pulse duration	LE low	5		5		5		ns
		CLR low	5		5		5		
	Setup time, before LE↓	Bi and PARITY	14		14		14		
^t su	Setup time, before LE.	CLR inactive	2		2		2		ns
th	Hold time, Bi and PARITY after LE↓		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS				
C _{pd} Power dissipation capacitance pe			A to B		87		
	Power dissipation capacitance per transceiver	Outputs enabled	B to A		60	_	
		0.1111	A to B	C _L = 50 pF, f = 1 MHz	28	pF	
		Outputs disabled	B to A		8		



 $[\]ensuremath{^{\ddagger}}$ For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

D3398, JANUARY 1990

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{\text{CLR}}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{\text{OC}}$ (output control) is at a high logic level.

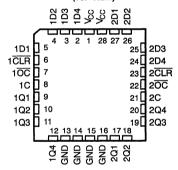
The 54AC11873 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11873 is characterized for operation from -40° C to 85°C.

54AC11873 ... JT PACKAGE 74AC11873 ... DW OR NT PACKAGE

(TOP VIEW)

		_	
1C[₁ U	28	1 <u>0C</u>
1Q1[2	27	1CLR
1Q2[3	26] 1D1
1Q3[4	25	1D2
1Q4[5	24] 1D3
GND[6	23] 1D4
GND[7	22] v _{cc}
GND[8	21] v _{cc}
GND[9	20	2D1
2Q1[10	19	2D2
2Q2[11	18	2D3
2Q3[12	17	2D4
2Q4[13	16	2CLR
2C[14	15	2 <u>0C</u>

54AC11873 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE

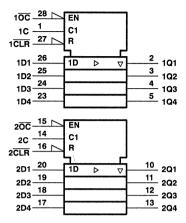
	IN	PUTS		OUTPIJT
OC	CLR	С	D	Q
L	L	X	Х	L
L	н	Н	Н	н
L	н	Н	L	L
L	Н	L	X	Q _o
Н	×	Х	X	z

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D3398, JANUARY 1990

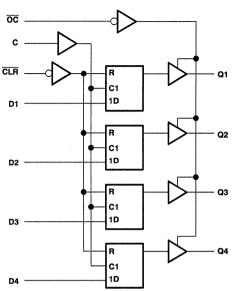
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, or NT packages.

logic diagram, each quad latch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$-0.5 \mathrm{V}$ to $\mathrm{V}_{\mathrm{CC}} + 0.5 \mathrm{V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage temperature range	– 65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3398, JANUARY 1990

recommended operating conditions

			54	AC1187	'3	74	AC1187	3	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1,35			1.35	V
		V _{CC} = 5.5 V			(d).65			1.65	
Vı	Input voltage		O O	~	* Vcc	0		Vcc	V
Vο	Output voltage		0	76	Vcc	0		Vcc	V
		V _{CC} = 3 V		20	- 4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V	20		- 24			- 24	mA
		V _{CC} = 5.5 V	4.		- 24			- 24	
		V _{CC} = 3 V			12			12	
lOL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETONS		T,	4 = 25°C	;	54AC1	1873	74AC1	1873	
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		
Voн	1 01	4.5 V	3.94			3.7		3.8		V
	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	IOH = - 75 mA [†]	5.5 V						3.85		
		3 V			0.1		G 0.1		0.1	
	Ι _{ΟL} = 50 μΑ	4.5 V			0.1	~Q	₹20.1		0.1	
		5.5 V			0.1	6646 600	0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36	15/	0.5		0.44	
VOL		4.5 V			0.36		0.5		0.44	٧
	I _{OH} = 24 mA	5.5 V			0.36		0.5		0.44	
	IOL = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	V _O = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μА
. 1	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μА
¹ CC	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	V _I = V _{CC} or GND	5 V		13.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



54AC11873, 74AC11873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3398, JANUARY 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

	DA DA NA		T _A = 25°C	54AC11873	74AC11873	
	PARAM	EIEH	MIN MAX	MIN MAX	MIN MAX	UNIT
		CLR low	5	5	5	
tw	Pulse duration	C high	5	5 🔨	5	ns
	Catura times data bafasa Ci	Data high	3	3/1/2/1	3	
tsu	Setup time, data before C↓	Data low	4	C 4.71	4	ns
	Hold time, data after C↓	Data high	1	1.5A	1	
th	noid time, data after O‡	Data low	1	1	1	ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

	2020	T _A = 25	T _A = 25°C		1873	74AC11873			
	PARAM	EIEK	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	D. Landau Cara	CLR low	5		5		5		
tw	Pulse duration	C high	5		5	6	5		ns
	Octor time data before Ol	Data high	2		.33	500	2		
t _{su}	Setup time, data before C↓	Data low	3		_(₹3 €)	24.	3		ns
4.	Hold time, data after C↓	Data high	1		ং		1		
th	Hold time, data after O	Data low	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	то	T,	4 = 25°C	;	54AC	11873	74AC1	11873	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	_	_	2.8	8.8	11.2	2.8	14.1	2.8	13	
t _{PHL}	D	Q	2.8	9	11.2	2.8	13.6	2.8	12.7	ns
tPLH		Q	3	9.4	11.8	3	14.9	3	13.6	
t _{PHL}	С	u .	2.9	9.4	11.7	2.9	A 4.2	2.9	13.2	ns
t _{PHL}	CLR	Q	2.3	8.2	10.3	2.3	12.2	2.3	11.5	ns
^t PZH		_	1.8	6.4	8.4	1.8	10.5	1.8	9.7	
tpzL	ŌĊ	Q	2.7	9.9	12.5	27	15.7	2.7	14.4	ns
tPHZ			3.8	6.8	8.4	3.8	9.4	3.8	9	
t _{PLZ}	<u>oc</u>	Q	3.5	6.8	8.5	3.5	9.5	3.5	9.1	1 ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

	FROM	то	T T	Δ = 25°C		54ACT	11973	74ACT	11873	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	_	_	2.2	5.5	7.3	2.2	9.2	2.2	8.4	
t _{PHL}	D	Q	2.1	5.5	7.2	2.1	8.9	2.1	8.2	ns
tPLH			2.4	5.9	7.8	2.4	9.7	2.4	8.9	
tPHL	C	Q	2.2	5.8	7.6	2.2	Q9.4	2.2	8.7	ns
t _{PHL}	CLR	Q	1.7	5.1	6.8	1,50		1.7	7.6	ns
^t PZH		_	1.2	4.1	5.6	Q1.2 %	7	1.2	6.4	
^t PZL	oc	Q	1.9	5.5	7.3	1.9	9.2	1.9	8.5	ns
^t PHZ	oc		3.5	5.9	7.4	3.5	8.2	3.5	7.9	
t _{PLZ}	1 00	Q	3.3	5.5	7	3.3	7.9	3.3	7.6	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

Texas Instruments

54AC11873, 74AC11873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS D3398, JANUARY 1990

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
C _{pd}	Down dissination associations are lately	Outputs enabled	C: 50 = 5 4 4 MU-	43	
	Power dissipation capacitance per latch	Outputs disabled	C _L = 50 pF, f = 1 MHz	9	pF

54ACT11873, 74ACT11873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3399, FEBRUARY 1990

- Inputs are TTL-Voltage Compatible
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{\text{OLR}}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{\text{OC}}$ (output control) is at a high logic level.

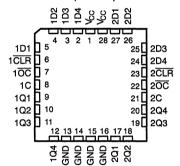
The 54ACT11873 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11873 is characterized for operation from – 40°C to 85°C.

54ACT11873...JT PACKAGE 74ACT11873...DW OR NT PACKAGE

(TOP VIEW)

10	, 0	28	10C
1Q1	2	27	1CLR
1Q2[3	26] 1D1
1Q3[4	25] 1D2
1Q4[5	24] 1D3
GND[6	23] 1D4
GND[7] v _{cc}
GND[8	21] Vcc
GND[9	20] 2D1
2Q1[10	19] 2D2
2Q2[11	18] 2D3
2Q3[12	17] 2D4
2Q4[13	16] 2CLR
2C[14	15] 2 <u>00</u>

54ACT11873 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE

	INF	OUTPUT		
OC	CLR	С	D	Q
L	L	Х	X	L
L	н	н	Н	н
L	н	Н	L	L
L	н	L	Х	Q _o
Н	×	Х	Х	z

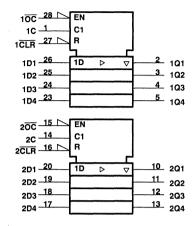
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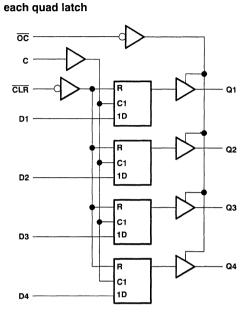
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through V _{CC} or GND pins	± 200 mA
Storage temperature range	– 65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11873, 74ACT11873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

D3399, FEBRUARY 1990

recommended operating conditions

		54AC1	Γ11873	74ACT	11873	
	1	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	40	2		٧
VIL	Low-level input voltage		8.0 Vis		0.8	V
VI	Input voltage	0	oo™ vcc	0	Vcc	V
Vo	Output voltage	0 4	Vcc	0	Vcc	V
ЮН	High-level output current	TIO ₂	- 24		- 24	mA
lOL	Low-level output current	OPE	24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			T,	4 = 25°C	;	54ACT	11873	74ACT	11873	
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		4.5 V	4.4			4.4		4.4		
	IOH = - 50 μA	5.5 V	5.4			5.4		5.4		
		4.5 V	3.94			3.7		3.8		
∨он	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		V
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	I _{OH} = - 75 mA [†]	5.5 V						3.85		
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	5.5 V			0.1	. •	<u>د 0.1</u>		0.1	
		4.5 V			0.36	70	0.5		0.44	
VOL	I _{OL} = 24 mA	5.5 V			0.36	\$6.90	0.5		0.44	٧
	IOL = 50 mA†	5.5 V				6.	1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	Vo = Vcc or GND	5.5 V			± 0.5		± 10		± 5	μΑ
IĮ.	VI = VCC or GND	5.5 V			± 0.1		± 1		± 1	μΑ
lcc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
	One input at 3.4 V,									
∆lcc [‡]	Other inputs at GND or VCC	5.5 V	İ		0.9		1		1	mA
Ci	VI = VCC or GND	5 V		4.5						рF
Co	V _O = V _{CC} or GND	5 V		13.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

D3399, FEBRUARY 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

			T _A = 25°C	54ACT11873	74ACT11873	
	PARAM	ETER	MIN MAX	MIN MAX	MIN MAX	UNIT
		CLR low	5	5	5	
t _w	Pulse duration	Enable C high	5	5 🔨	5	ns
		Data high	6	6754	6	
t _{su}	Setup time, data before C↓	Data low	3	\$63°71.	3	ns
	Held him a data after Ol	Data high	0	456	0	
th	Hold time, data after C↓	Data low	0	0	0	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	то	T,	4 = 25°C	;	54ACT	11873	74ACT	11873	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}			4.4	7.2	8.8	4.4	10.9	4.4	10	
^t PHL	D	Q	3	6.6	9.1	3	10.9	3	10.2	ns
t _{PLH}		0	4.7	8.1	10	4.7	12.3	4.7	11.3	
^t PHL	С	Q	5.2	8.9	10.9	5.2	C)3.3	5.2	12.3	ns
^t PHL	CLR	Q	2.9	6.5	9		10.7	2.9	10	ns
^t PZH			1.9	4.9	7.1	ক পুঞ্	8.5	1.9	8	
^t PZL	<u>oc</u>	Q	2.7	6.4	9.1	Ž.7	11.1	2.7	10.3	ns
^t PHZ			5.7	8	9.5	5.7	10.6	5.7	10.2	
tPLZ	ŌĊ	Q	5.2	7.8	9.1	5.2	10.2	5.2	9.8	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

		PARAMETER		TEST CONDITIONS	TYP	UNIT
	<u> </u>	Power dissipation capacitance per latch	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	40	pF
ı	Cbq	rower dissipation capacitance per laten	Outputs disabled	C[=50 pr, 1=1 MH2	7) PF

D3446, MARCH 1990-REVISED OCTOBER 1990

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Asynchronous Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

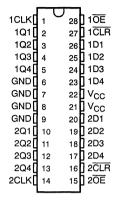
description

The 54AC11874 and 74AC11874 contain dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, and working registers.

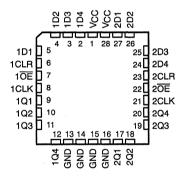
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'AC11874 has $\overline{\text{CLR}}$ inputs and noninverting outputs. Taking this input ($\overline{\text{CLR}}$) low causes the four Q outputs to go low independently of the clock.

The 54AC11874 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC11874 is characterized for operation from –40°C to 85°C.

54AC11874 . . . JT PACKAGE 74AC11874 . . . DW OR NT PACKAGE (TOP VIEW)



54AC11874 . . . FK PACKAGE (TOP VIEW)

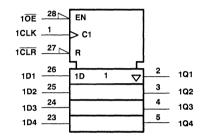


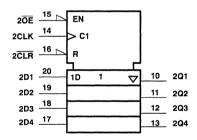
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FUNCTION TABLE (each flip-flop)

	INPU	TS		OUTPUT
ŌĒ	CLR	CLK	D	Q
L	L	Х	Χ	L
L	Н	1	Н	н
L	Н	1	L	L
L	Н	L	X	QO
Н	Х	Х	х	z

logic symbol†

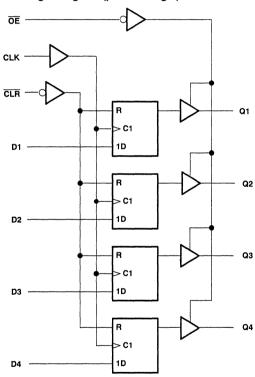




[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



D3446, MARCH 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND pins	± 200mA
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54	AC1187	4	74	AC1187	4	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
۷ _{IL}	Low-level input voltage	V _{CC} = 4.5 V			1,35			1.35	V
		V _{CC} = 5.5 V			65			1.65	
٧ı	Input voltage		0	, QQ	VCC	0		Vcc	V
Vo	Output voltage		0	100	Vcc	0		Vcc	V
		V _{CC} = 3 V	O PROD	\$0	-4	,		4	
ЮН	High-level output current	V _{CC} = 4.5 V	700		- 24			- 24	mA
		V _{CC} = 5.5 V	Q.		~ 24			24	
		V _{CC} = 3 V			12			12	
IOL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3446, MARCH 1990-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T,	A = 25°C		54AC1	1874	74AC1	1874	UNIT
PANAMETER	TEST CONDITIONS	Vcc	MIN	TYP N	MAX	MIN	MAX	MIN	MAX	UNII
		3 V	2.9			2.9		2.9		
	I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
V	I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		v
Voн	In. Odma	4.5 V	3.94			3.7		3.8		· •
	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	IOH = - 75 mA [†]	5.5 V						3.85		
		3 V			0.1		∠ 0.1		0.1	
	I _{OL} = 50 μA	4.5 V			0.1	نہ	× 0.1		0.1	
		5.5 V			0.1	°0%	₩ 0.1		0.1	
Va	I _{OL} = 12 mA	3 V		(0.36	5760	0.5		0.44	v
VOL	In 24 mA	4.5 V			0.36		0.5		0.44	v
	I _{OL} = 24 mA	5.5 V		(0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	VO = VCC or GND	5.5 V		:	± 0.5		± 10		± 5	μΑ
l _l	V _I = V _{CC} or GND	5.5 V		-	± 0.1		± 1		± 1	μА
lcc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	V _I = V _{CC} or GND	5 V		4.5						рF
Co	VO = VCC or GND	5 V		13.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $_\pm$ 0.3 V (unless otherwise noted) (see Note 2)

	PARAN	IETED	T _A =	25°C	54AC	1874	74AC1	1874	UNIT
	FARAN	METER	MIN	MAX	MIN	MAX	MIN	MAX	ONII
fclock	Clock frequency		0	60	0	60	0	60	MHz
	5	CLR low	4		4	.Ó.	4		
™	Pulse duration	CLK high or low	8.3		8,3)	£100	8.3		ns
	Setup time before CLK↑	Data	3		06.35	2,	3		
tsu	Setup time before CLK	CLR inactive	1.5		K 5		1.5		ns
th	Hold time after CLK†	Data	1		1		1		ns

D3446 MARCH 1990-REVISED OCTOBER 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

	PARAM	IETED	T _A =	25°C	54AC1	1874	74AC	11874	UNIT
	FARAII	EIER	MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency		0	125	0	125	0	125	MHz
		CLR low	4		4	<u></u>	4		
t _w	Pulse duration	CLK high or low	4		40	15/4	4		ns
	Setup time before CLK↑	Data	2		ु०१		2		
^t su	Setup time before CEN	CLR inactive	1.5		15		1.5		ns
th	Hold time after CLK†	Data	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	то	T,	4 = 25°C	;	54AC	11874	74AC	11874	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f _{max}			60			60		60		MHz
^t PLH	CLK	A O	2.9	7.3	11	2.9	13.5	2.9	12.5	
^t PHL		Any Q	3.7	8.8	13.1	3.7	5.6	3.7	14.6	ns
[†] PHL	CLR	Any Q	3.9	9.3	14	3.90	76.8	3.9	15.7	ns
^t PZH	ŌĒ	4	2.1	5.6	8.7	2	10.7	2.1	9.8	
^t PZL	UE.	Any Q	3.1	8.4	13.1	38.1	16	3.1	14.9	ns
^t PHZ	ŌĒ	Any Q	4	6.2	8.2	4	8.9	4	8.7	
tPLZ	OE .	Ally Q	3.9	6.3	8.5	3.9	9.3	3.9	9	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	Т,	4 = 25°C	;	54AC1	1874	74AC1	1874	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fmax			125			125		125		MHz
t _{PLH}	CLK	Any Q	2.3	5.2	7.4	2.3	9	2.3	8.3	ns
t _{PHL}	OLK	Ally Q	2.9	6.1	8.6	2.9	(70.3	2.9	9.6	115
t _{PHL}	CLR	Any Q	2.9	6.3	8.9			2.9	10	ns
tPZH	ŌĒ	Any Q	1.5	4	5.9	₹ .5∢	7.1	1.5	6.6	ns
tPZL	OE.	Any Q	2.3	5.4	7.8	2.3	9.5	2.3	8.8	115
tPHZ	ŌĒ	Any Q	3.8	5.7	7.3	3.8	8	3.8	7.7	ns
tPLZ	ŲL.	rany Q	3.7	5.5	7.1	3.7	7.8	3.7	7.5	113

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

		PARAMETER	TEST CON	TYP	UNIT		
Γ	<u> </u>	Davies dissination consistence	Outputs enabled	0. 50.55	f = 1 MHz	31	pF
L	∪pd	Power dissipation capacitance	Outputs disabled	C _L = 50 pF,	1 = 1 WITZ	13	рг

D3447, MARCH 1990-REVISED OCTOBER 1990

- Inputs are TTL-Voltage Compatible
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Asynchronous Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

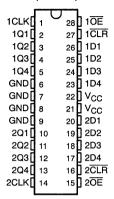
description

The 54ACT11874 and 74ACT11874 contain dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, and working registers.

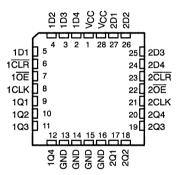
The edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 'ACT11874 has $\overline{\text{CLR}}$ inputs and noninverting outputs. Taking $\overline{\text{CLR}}$ low causes the four Q outputs to go low independently of the clock.

The 54ACT11874 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11874 is characterized for operation from – 40°C to 85°C.

54ACT11874 . . . JT PACKAGE 74ACT11874 . . . DW OR NT PACKAGE (TOP VIEW)



54ACT11874 . . . FK PACKAGE (TOP VIEW)



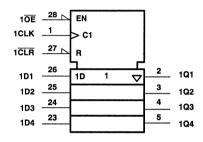
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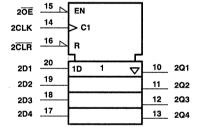
D3447, MARCH 1990-REVISED OCTOBER 1990

FUNCTION TABLE (each flip-flop)

	INPU	OUTPUT		
ŌĒ	CLR	CLK	D	Q
L	L	Х	Х	L
L	Н	1	Н	н
L	Н	↑	L	L
L	Н	L	Х	Q ₀
Н	Х	X	Х	z

logic symbol†

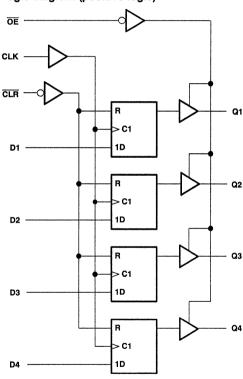




[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



D3447, MARCH 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V _I (see Note 1) – 0.8	5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20mA
Output clamp current, IOK (VO < 0 or VO > VCC)	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 200mA
Storage temperature range	. -55°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54ACT	11874	74ACT	11874	
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
VIL	Low-level input voltage		× 0.8		0.8	٧
VI	Input voltage	0,	.Vcc	0	Vcc	٧
Vo	Output voltage	200%	₩VCC	0	Vcc	V
ЮН	High-level output current	5,50	- 24		- 24	mA
loL	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		T	T,	λ = 25°C	T	54ACT	11874	74ACT	11874	
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP M	¥Χ	MIN	MAX	MIN	MAX	UNIT
	ΙΟΗ = - 50 μΑ	4.5 V	4.4			4.4		4.4		
	011	5.5 V	5.4			5.4		5.4		
Voн	I _{OH} = – 24 mA	4.5 V	3.94		\neg	3.7		3.8		V
-011	1011	5.5 V	4.94			4.7		4.8		
	I _{OH} = - 50 mA [‡]	5.5 V				3.85			i	
	I _{OH} = - 75 mA [‡]	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V		().1		0.1		0.1	
	I OL STATE	5.5 V		().1		~ 0.1		0.1	
VOL	IOI = 24 mA	4.5 V		0.	36		0.5		0.44	V
OL.	100	5.5 V		0.	36	36,50	0.5		0.44	
	IOL = 50 mA [‡]	5.5 V				164	1.65			
	I _{OL} = 75 mA [‡]	5.5 V							1.65	
loz	VO = VCC or GND	5.5 V		±	0.5		± 10		± 5	μΑ
l ₁	V _I = V _{CC} or GND	5.5 V		±	0.1		± 1		± 1	μΑ
lcc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Aloo§	One input at 3.4 V, Other inputs at GND or VCC				0.9		1		1	mA
7.00			ļ		ا ق.ر		'		'	шА
Ci	V _I = V _{CC} or GND	5 V		4.5	T					pF
Co	VO = VCC or GND	5 V		13.5						pF

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3447, MARCH 1990-REVISED OCTOBER 1990

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

	PARAM	METER	T _A =	25°C	54ACT	11874	74ACT	UNIT	
	· Allan	MIN	MAX	MIN	MAX	MIN	MAX	0	
fclock	Clock frequency		0	125	0	125	0	125	MHz
		CLR low	4		4	.ć\.	4		
tw	Pulse duration	CLK high or low	4		43	S. Car	4		ns
	Cabra time before OLICA	Data	5		S\$35	7	5		
t _{su}	Setup time before CLK†	CLR low	2		'\$2		2		ns
th	Hold time after CLK↑	Data	1		1		1		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $_{\pm}$ 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T,	4 = 25°C	;	54ACT	11874	74ACT	11874	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONII
f _{max}			125			125		125		MHz
[‡] PLH	CLK	Any Q	3.7	6.6	8.4	3.7	10.2	3.7	9.4	ns
t _{PHL}		Any Q	4.1	7.6	9.5	4.1	A1.3	4.1	10.6	115
t _{PHL}	CLR	Any Q	3.5	7.8	10.5	3.5	2.7	3.5	11.8	ns
^t PZH	ŌĒ	Any Q	1.6	4.6	6.7	.4.6∢	7.9	1.6	7.4	ns
^t PZL	05	Ally Q	2.4	6	8.6	224	10.2	2.4	9.5	115
t _{PHZ}	ŌĒ	Any Q	5.4	7.4	8.9	5.4	9.7	5.4	9.4	ns
tPLZ	OL .	Ally G	4.9	7.1	8.5	4.9	9.5	4.9	9.1	113

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

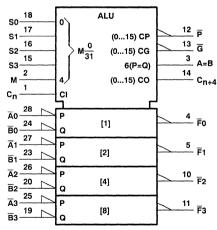
operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CON	TYP	UNIT		
C-4	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF,	f = 1 MHz	35	ρF
Cpd	1 Ower dissipation capacitance	Outputs disabled	оц - 50 рг,	1 - 1 1411 12	17	P,

D3479, MARCH 1990

- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes: Addition, Subtraction, Shift Operand A One Position, Magnitude Comparison, Plus Twelve Other Arithmetic Operations
- Logic Function Modes Exclusive-OR, Comparator, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Provides Status Register Checks
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

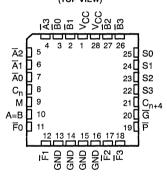
Pin numbers shown are for DW, JT, and NT packages.

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54AC11881 . . . JT PACKAGE 74AC11881 . . . DW OR NT PACKAGE (TOP VIEW)

		_	
C _n [₁ U	28] Ā0
М[2	27] Ā1
A=B[3	26] Ā2
Fo[4	25] Ā3
F1[5	24] Bo
GND[6	23] B̄1
GND[7	22] V _{CC}
GND[8	21] V _{CC}
GND[9	20	B2
F2[10	19] B 3
F3[11	18] S0
P[12	17] S1
G[13	16	S2
C _{n+4} [14	15] S3

54AC11881 . . . FK PACKAGE (TOP VIEW)



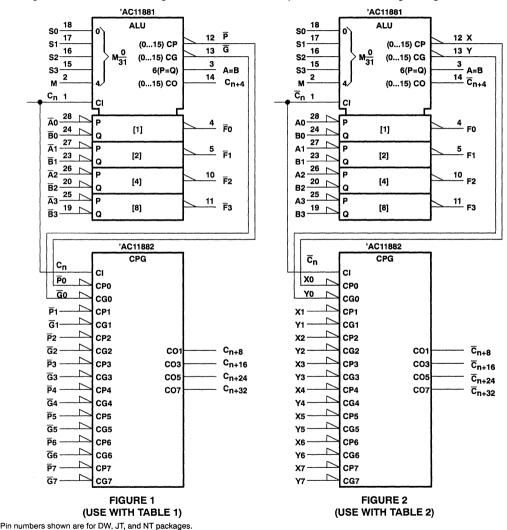
RODUCT PREVIEW



PRODUCT PREVIEW

signal designations

In both Figures 1 and 2, the polarity indicators () indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.



The 'AC11881 arithmetic logic units (ALU)/function generators have a complexity of 77 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, \overline{G} and \overline{P} , for the four bits in the package. When used in conjunction with the 54AC11882 or 74AC11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AC11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without enternal circuitry.

The 'AC11881 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-low data (Table 1)	Ã0	B0	Ā1	B1	Ã2	B2	Ā3	B3	F0	F1	F2	F3	Cn	C _{n+4}	P	G
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	A3	В3	F0	F1	F2	F3	\overline{C}_n	Cn+4	Х	Y

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'AC11881 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2,F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n =H when performing this comparison. The A=B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

	INPUT Cn	OUTPUT Cn+4	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
Ī	Н	н	A≥B	A≤B
	Н	L	A < B	A > B
	L	Н	A > B	A < B
ſ	L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

The 'AC11881 has the same pinout and same functionality as the 'AC11181 except for the \overline{P} , \overline{G} , and C_{n+4} outputs when the device is in the logic mode (M = H).



description (continued)

In the logic mode, the 'ACT11881 provides the user with a status check on the input words A and B and the output word F. While in the logic mode, the \overline{P} , \overline{G} , and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = F0 + F1 + F2 + F3$$

 $\overline{G} = H$
 $C_{n+4} = PC_n$

Function Tables for Input Bits Equal/Not Equal

S0 = S3 = H, S1 = S2 = L, AND M = H

_		DATA		OUTPUTS			
Cn		DAIA	INPUTS		Ğ	P	Cn+4
Н	$\overline{A}0 = \overline{B}0$	Ā1 = B1	Ã2 = B2	A3 = B3	Н	L	Н
L	$\overline{A}0 = \overline{B}0$	A1 = B1	Ã2 = B2	A3 = B3	Н	L	L
X	Ã0 ≠ B0	Х	×	×	Н	Н	L
X	×	Ā1 ≠ B1	X	×	Н	Н	L
X	×	X	Ã2 ≠ B2	×	Н	Н	L
Х	X	X	X	Ā3 ≠ B 3	Н	Н	L

S0 = S1 = S3 = L, S2 = H, AND M = H

_				OUTPUTS			
c _n		DAIA	INPUTS		G	P	Cn+4
Н	A0 or B0 = L	A1 or B1 = L	A2 or B2 ≈ L	A3 or B3 = L	Н	L	Н
L	A0 or B0 = L	A1 or B1 = L	A2 or B2 ≈ L	A3 or B3 = L	Н	L	L
×	A0 = B0 = H	×	×	×	Н	Н	L
×	X	Ā1 = B1 = H	×	×	Н	Н	L
Х	×	X	Ā2 = B2 = H	×	Н	Н	L
×	X	X	X	A3 = B3 = H	Н	Н	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits $\overline{F}i$. By monitoring the \overline{P} and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'ACT11881 has the unique feature of providing an A = B status while the exclusive-OR (\oplus) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs $(\overline{A}i, \overline{B}i)$ are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem-pole \overline{P} output, is particularly useful when cascading 'ACT11881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode (\overline{P}) and (\overline{G}) . Thus, the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-drain output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs $(\overline{A}i, \overline{B}i)$ being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	М	P = F0 + F1 + F2 + F3
L	Н	L	L	Н	A0B0 + A1B1 + A2B2 + A3B3
H	L	L	Н	Н	(A0 ⊕ B0) + (A1 ⊕ B1) + (A2 ⊕ B2) + (A3 ⊕ B3)



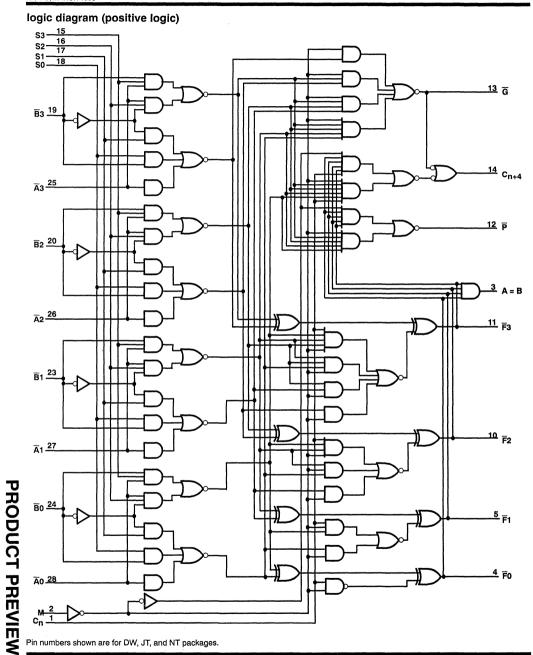
Table 1. Logic Functions and Arithmetic Operations (Active-Low)

	SELEC	CTION			ACTIVE-LOW DATA	
CO	S2		-	M = H	M = L; ARITHME	TIC OPERATIONS
S3	52	S1	SO	LOGIC FUNCTIONS	C _n = L (no carry)	C _n = H (with carry)
L	L	L	L	F = Ā	F = A MINUS 1	F = A
L	L	L	н	F = AB	F = AB MINUS 1	F = AB
L	L	Н	L	F = A + B	F = AB MINUS 1	F = AB
L	L	Н	н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	Н	L	L	$F = \overline{A + B}$	$F = A PLUS (A + \overline{B})$	F = A PLUS (A + B) PLUS 1
L	Н	L	н	F=B	$F = AB PLUS (A + \overline{B})$	$F = AB PLUS (A + \overline{B}) PLUS 1$
L	Н	Н	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	н	н	$F = A + \overline{B}$	F = A + B	F = (A + B) PLUS 1
н	L	L	L	F = $\overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
н	L	L	н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F = B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
Н	L	н	н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
н	н	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
н	н	L	н	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
н	Н	н	L.	F = AB	F ≈ AB PLUS A	F = AB PLUS A PLUS 1
н	Н	Н	н	F=A	F = A	F = A PLUS 1

Table 2. Logic Functions and Arithmetic Operations (Active-High)

	SELEC	CTION			ACTIVE-HIGH DATA	
-				M = H	M = L; ARITHME	TIC OPERATIONS
S3	S2	S1	SO	LOGIC FUNCTIONS	Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	F=Ā	F = A	F = A PLUS 1
L	L	L	н	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	Н	L	F = ĀB	F = A + B	$F = (A + \overline{B}) PLUS 1$
L	L	Н	н	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	н	L	L	F = ĀB	F = A PLUS AB	F = A PLUS AB PLUS 1
L	Н	L	Н	F≖B	$F = (A + B) PLUS A\overline{B}$	F = A PLUS AB PLUS 1
L	Н	н	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	н	н	F = AB	F ≃ AB MINUS 1	F = AB
н	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
Н	L	L	н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
Н	L	Н	L	F=B	$F = (A + \overline{B}) PLUS AB$	F = (A + B) PLUS AB PLUS 1
Н	L	Н	Н	F = AB	F = AB MINUS 1	F = AB
Н	н	L	L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1
н	н	L	н	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
Н	н	н	L	F = A + B	$F = (A + \overline{B}) PLUS A$	F = (A + B) PLUS A PLUS 1
Н	Н	н	н	F = A	F = A MINUS 1	F = A

[†] Each bit is shifted to the next more significant position.



Texas Instruments

D3479, MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	– 0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND pins	± 200mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54	AC1188	1	74	AC1188	1		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		3	5	5.5	3	5	5.5	٧	
		V _{CC} = 3 V	2.1			2.1				
٧ıH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V	
		V _{CC} = 5.5 V	3.85			3.85				
		V _{CC} = 3 V			0.9			0.9		
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V	
		V _{CC} = 5.5 V			1.65	-		1.65		
VI	Input voltage		0		Vcc	0		Vcc	V	
٧o	Output voltage		0		Vcc	0		Vcc	V	
		V _{CC} = 3 V			- 4			- 4		
ЮН	High-level output current, All outputs except A=B	V _{CC} = 4.5 V			- 24			- 24	mA	
		V _{CC} = 5.5 V			- 24			- 24		
		V _{CC} = 3 V			12			12		
lol	Low-level output current	V _{CC} = 4.5 V			24			24	mA	
		V _{CC} = 5.5 V			24			24		
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V	
TA	Operating free-air temperature		- 55		125	- 40		85	ô	

PRODUCT PREVIEW



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA44	ETED	TEST CONDITIONS	T .,.	T,	A = 25°C	;	54AC	11881	74AC11881			
PARAM	EIEH	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
ЮН	A = B	VO = VCC	5.5 V			0.5		10		5	μΑ	
			3 V	2.9	_		2.9		2.9			
		I _{OH} = 50 μA	4.5 V	4.4			4.4		4.4			
			5.5 V	5.4			5.4		5.4			
		I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		٧	
∨он			4.5 V	3.94			3.7		3.8		v	
		I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8			
		I _{OH} = - 50 mA [†]	5.5 V				3.85					
		I _{OH} = - 75 mA [†]	5.5 V						3.85			
			3 V			0.1		0.1		0.1		
		I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1		
			5.5 V			0.1		0.1		0.1		
.,		I _{OL} = 12 mA	3 V			0.36		0.5		0.44		
VOL			4.5 V			0.36		0.5		0.44	٧	
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44		
		IOL = 50 mA†	5.5 V					1.65				
		I _{OL} = 75 mA [†]	5.5 V							1.65		
lį		V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		±1	μА	
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μА	
Ci		V _I = V _{CC} or GND	5 V		4.5						pF	
Co	A = B	V _O = V _{CC} or GND	5 V		11						рF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER	TEST CO	NDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF,	f = 1 MHz	161	pF

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

	INPUT	OTHER INP	JT SAME BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
^t PLH	Āi	Bi	None	Remaining A and B	Cn	Fi	In-Phase
^t PHL	Āi	Bi	None	Remaining $\overline{\overline{A}}$ and $\overline{\overline{B}}$	Cn	Fi	In-Phase
^t PLH	Bi	Āi	None	Remaining A and B	- C _n	Fi	In-Phase
^t PHL	Bi	Āi	None	Remaining A and B	C _n	Fi	In-Phase
^t PLH	Āi	Bi	None	None	Remaining A and B, Cn	P	In-Phase
^t PHL	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
^t PLH	Bi	Āi	None	None	Remaining A and B, C _n	Ē	In-Phase
^t PHL	Bi	Āi	None	None	Remaining A and B, C _n	P	In-Phase
^t PLH	Āi	None	Bi	Remaining B	Remaining A, C _n	G	In-Phase
^t PHL	Āi	None	Bi	Remaining B	Remaining A, C _n	G	In-Phase
^t PLH	Bi	None	Āi	Remaining B	Remaining A, C _n	G	In-Phase
^t PHL	Bi	None	Āi	Remaining B	Remaining A, C _n	G	In-Phase
^t PLH	· C _n	None	None	All Ā	All B	Any F or C _{n+4} Any F	In-Phase
^t PHL	Cn	None	None	All Ā	All B	Any F or C _{n+4}	In-Phase
^t PLH	Āi	None	Bi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PHL	Āi	None	Bi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PLH	Bi	None	Āi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PHL	Bi	None	Āi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase



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PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

	INPUT	OTHER INP	JT SAME BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
^t PLH	Āi	None	Bi	Remaining A	Remaining B, C _n	Fi	In-Phase
[†] PHL	Āi	None	Bi	Remaining A	Remaining B, C _n	Fi	In-Phase
^t PLH	Bi	Āi	None	Remaining A	Remaining B, C _n	Fi	Out-of-Phase
[†] PHL	Bi	Āi	None	Remaining A	Remaining B, C _n	Fi	Out-of-Phase
^t PLH	Āi	None	Bi	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
[†] PHL	Āi	None	Bi	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
^t PLH	Bi	Āi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	Out-of-Phase
^t PHL	Bi	Āi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	Out-of-Phase
^t PLH	, Ā i	Bi	None	None	Remaining A and B, C _n	G	In-Phase
^t PHL	Āi	Bi	None	None	Remaining A and B, Cn	G	In-Phase
^t PLH	Bi	None	Āi	None	Remaining A and B, C _n	G	Out-of-Phase
^t PHL	Bi	None	Āi	None	Remaining \overline{A} and \overline{B} , C_n	G	Out-of-Phase
^t PLH	Āi	None	Bi	Remaining A	Remaining B, C _n	A = B	In-Phase
^t PHL	Āi	None	Bi	Remaining A	Remaining B, C _n	A = B	In-Phase
^t PLH	Bi	Āi	None	Remaining A	Remaining B, C _n	A = B	Out-of-Phase
^t PHL	Bi	Āi	None	Remaining A	Remaining B, C _n	A = B	Out-of-Phase

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PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table (Continued)

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

	INPUT	OTHER INPL	JT SAME BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
t _{PLH}	Cn	None	None	All A and B	None	Cn+4 or Any F	In-Phase
tPHL	Cn	None	None	All A and B	None	C _{n+4} or Any F	In-Phase
^t PLH	Āi	Bi	None	None	Remaining A, B, C _n	C _{n+4}	Out-of-Phase
[†] PHL	Āi	Bi	None	None	Remaining A, B, C _n	C _{n+4}	Out-of-Phase
^t PLH	Bi	None	Āi	None	Remaining A, B, C _n	C _{n+4}	In-Phase
^t PHL	Bi	None	Āi	None	Remaining A, B, C _n	C _{n+4}	In-Phase

Logic Mode Test Table

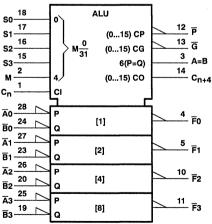
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

	INPUT	OTHER INPU	JT SAME BIT	OTHER D	ATA INPUTS	OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
tPLH	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	Fi	Out-of-Phase
tpHL	Āi	Bi	None	None	Remaining A, and B, C _n	Fi	Out-of-Phase
^t PLH	Bi	Āi	None	None	Remaining \overline{A} , and \overline{B} , C_n	Fi	Out-of-Phase
^t PHL	Bi	Āi	None	None	Remaining \overline{A} , and \overline{B} , C_n	Fi	Out-of-Phase

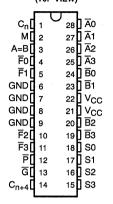
2-106

- Inputs are TTL-Voltage Compatible
- Full Look-Ahead for High-Speed **Operations on Long Words**
- Arithmetic Operating Modes: Addition. Subtraction, Shift Operand A One Position, Magnitude Comparison, Plus Twelve Other Arithmetic Operations
- Logic Function Modes Exclusive-OR, Comparator, AND, NAND, OR, NOR, Plus **Ten Other Logic Operations**
- **Provides Status Register Checks**
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**

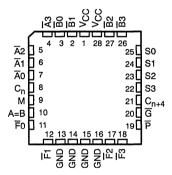
logic symbol†



54ACT11881 . . . JT OR JW PACKAGE 74ACT11881 . . . DW OR NT PACKAGE (TOP VIEW)



54ACT11881 . . . FK PACKAGE (TOP VIEW)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

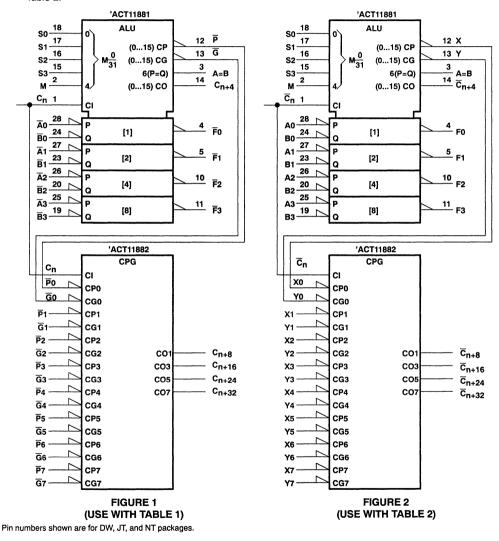
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PRODUCT PREVIEW

signal designations

In both Figures 1 and 2, the polarity indicators () indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.



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description

The 'ACT11881 arithmetic logic units (ALU)/function generators have a complexity of 77 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs, \overline{G} and \overline{P} , for the four bits in the package. When used in conjunction with the 54ACT11882 or 74ACT11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'ACT11882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without enternal circuitry.

The 'ACT11881 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-low data (Table 1)	Ā0	B0	Ā1	B1	Ã2	B2	Ā3	B3	F0	F1	F2	F3	Cn	Cn+4	P	G
Active-high data (Table 2)	A0	B0	A1	B1	A2	B2	АЗ	ВЗ	F0	F1	F2	F3	Cn	Cn+4	Х	Υ

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'ACT11881 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2,F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU must be in the subtract mode with C_n =H when performing this comparison. The A=B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C _n	OUTPUT C _{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
Н	Н	A≥B	A≤B
Н	L	A < B	A > B
L	н	A > B	A < B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

The 'ACT11881 has the same pinout and same functionality as the 'ACT11181 except for the \overline{P} , \overline{G} , and C_{n+4} outputs when the device is in the logic mode (M = H).



description (continued)

In the logic mode, the 'ACT11881 provides the user with a status check on the input words A and B and the output word F. While in the logic mode, the \overline{P} , \overline{G} , and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{G}$$
 = F0 + F1 + F2 + F3
 \overline{G} = H
 C_{n+4} = PC_n.

Function Tables for Input Bits Equal/Not Equal

S0 = S3 = H, S1 = S2 = L, AND M = H

		DATA	OUTPUTS					
Cn		DATA	Ğ	P	Cn+4			
Н	$\overline{A}0 = \overline{B}0$	Ā1 = B1	A2 = B2	$\overline{A}3 = \overline{B}3$	Н	L	Н	
L	$\overline{A}0 = \overline{B}0$	Ā1 = B1	$\overline{A}2 = \overline{B}2$	A3 = B3	Н	L	L	
X	Ã0 ≠ B0	X	X	X	Н	Н	L	
X	X	Ā1 ≠ B1	X	X	Н	Н	L	
X	×	X	Ā2 ≠ B2	X	Н	Н	L	
X	X	X	Х	Ã3 ≠ B3	Н	Н	L	

		DATA	INPUTS			OUTPUT	5
Cn		Ğ	P	Cn+4			
Н	A0 or B0 = L	$\overline{A}1 \text{ or } \overline{B}1 = L$	$\overline{A}2$ or $\overline{B}2 = L$	A3 or B3 = L	Н	L	I
L	A0 or B0 = L	A1 or B1 = L	$\overline{A}2$ or $\overline{B}2 = L$	A3 or B3 = L	Н	L	٦
X	A0 = B0 = H	×	×	Х	Н	Н	L
X	X	Ā1 = B1 = H	×	Х	Н	Н	L
X	X	×	Ā2 = B2 = H	х	Н	Н	L
Х	Х	X	X	$\overline{A}3 = \overline{B}3 = H$	Н	Н	L

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits $\overline{F}i$. By monitoring the \overline{P} and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'ACT11881 has the unique feature of providing an A = B status while the exclusive-OR (\oplus) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs ($\overline{A}i$, $\overline{B}i$) are equal in the following manner: $\overline{P} = (A0 \oplus B0) + (A1 \oplus B1) + (A2 \oplus B2) + (A3 \oplus B3)$. This unique bit-by-bit comparison of the data words, which is available on the totem-pole \overline{P} output, is particularly useful when cascading 'ACT11881s. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode (\overline{P} and \overline{G}). Thus, the A = B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A = B open-drain output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs $(\overline{A}i, \overline{B}i)$ being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	М	P = F0 + F1 + F2 + F3
L	Н	L	L	Н	A0B0 + A1B1 + A2B2 + A3B3
Н	L	L	Н	Н	(A0 ⊕ B0) + (A1 ⊕ B1) + (A2 ⊕ B2) + (A3 ⊕ B3)



Table 1

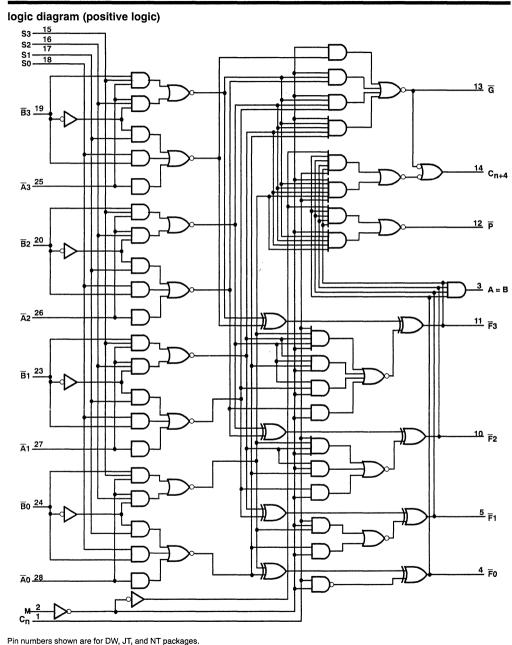
	SELEC	TION			ACTIVE-LOW DATA	
-		~_		M = H	M = L; ARITHME	TIC OPERATIONS
S3	S2	S1	S0	LOGIC FUNCTIONS	C _n = L (no carry)	C _n = H (with carry)
L	L	L	L	F = Ā	F = A MINUS 1	F = A
L	L	L	Н	F = AB	F = AB MINUS 1	F = AB
L	L	н	L	F = A + B	F = AB MINUS 1	F = AB
L	L	н	н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	Н	L	L	$F = \overline{A + B}$	$F = A PLUS (A + \overline{B})$	F = A PLUS (A + B) PLUS 1
L	Н	L	Н	F = B	$F = AB PLUS (A + \overline{B})$	F = AB PLUS (A + B) PLUS 1
L	Н	Н	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	Н	н	F = A + B	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$
Н	L	L	L	F≖ĀB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
Н	L	L	Н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
Н	L	Н	L	F=B	$F = A\overline{B} PLUS (A + B)$	F = AB PLUS (A + B) PLUS 1
Н	L	Н	Н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
н	Н	L	L	F = 0	F = A PLUS A [†]	F = A PLUS A PLUS 1
Н	Н	L	Н	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	Н	н	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	Н	Н	Н	F=A	F=A	F = A PLUS 1

Table 2

	SELEC	CTION			ACTIVE-HIGH DATA	
				M = H	M = L; ARITHME	TIC OPERATIONS
S3	S2	S1	S0	LOGIC FUNCTIONS	Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	F=Ā	F≡A	F = A PLUS 1
L	L	L	Н	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	Н	L	F = ĀB	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$
L	L	Н	Н	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	н	L	L	F ≈ AB	F = A PLUS AB	F = A PLUS AB PLUS 1
L	Н	L	Н	F=B	$F = (A + B) PLUS A\overline{B}$	F = A PLUS AB PLUS 1
L	Н	Н	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	Н	Н	н	$F = A\overline{B}$	F = AB MINUS 1	$F = A\overline{B}$
н	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
н	L	L	н	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
Н	L	Н	L	F = B	$F = (A + \overline{B}) PLUS AB$	$F = (A + \overline{B})$ PLUS AB PLUS 1
н	L	Н	Н	F≃AB	F = AB MINUS 1	F = AB
н	Н	L	L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1
Н	Н	L	Н	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
н	Н	Н	L	F = A + B	$F = (A + \overline{B}) PLUS A$	$F = (A + \overline{B})$ PLUS A PLUS 1
н	Н	Н	н	F = A	F = A MINUS 1	F = A

 $^{^{\}dagger}$ Each bit is shifted to the next more significant position.





Texas 🐶

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through V _{CC} or GND pins	
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT	11881	74ACT1	1881	UNIT
		MIN	MAX	MIN	MAX	0
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	Vcc	0	Vcc	V
Vο	Output voltage	0	Vcc	0	Vcc	V
ЮН	High-level output current		- 24		- 24	mA
lOL	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

20000		TEST SOURITIONS	T	T,	4 = 25°C		54ACT	11881	74ACT	11881		
PARAM	EIER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
ЮН	A = B	VO = VCC	5.5 V			0.5		10		5	μА	
		I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4			
Ì		10H = - 30 μA	5.5 V	5.4			5.4		5.4			
.,			4.5 V	3.94			3.7		3.8			
∨он		I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		٧	
l		I _{OH} = - 50 mA [†]	5.5 V				3.85					
		I _{OH} = - 75 mA [†]	5.5 V						3.85			
			4.5 V			0.1		0.1		0.1		
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1		
			4.5 V			0.36		0.5		0.44		
VOL		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	V	
		I _{OL} = 50 mA†	5.5 V					1.65				
		I _{OL} = 75 mA [†]	5.5 V	<u> </u>						1.65		
l ₁		V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		±1	μА	
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	μΑ	
ΔICC [‡]		V _I = V _{CC} or GND	5.5 V			0.9		1		1	mA	
Ci		V _I = V _{CC} or GND	5 V		4.5						pF	
Co	A = B	VO = VCC or GND	5 V		11						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

ſ	PARAMETER		TEST CO	NDITIONS	TYP	UNIT
	C _{pd} Power dissipation capacitance	CL	= 50 pF,	f = 1 MHz	170	pF

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

PARAMETER MEASUREMENT INFORMATION

SUM Mode Test Table

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

	INPUT	OTHER INPL	JT SAME BIT	OTHER DA	TA INPUTS	OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
tPLH	Āi	Bi	None	Remaining \overline{A} and \overline{B}	Cn	Fi	In-Phase
^t PHL	Āi	Bi	None	Remaining A and B	C _n	Fi	In-Phase
^t PLH	Bi	Āi	None	Remaining A and B	Cn	Fi	In-Phase
t _{PHL}	Bi	Āì	None	Remaining \overline{A} and \overline{B}	C _n	Fi	In-Phase
^t PLH	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
tPHL	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_{n}	P	In-Phase
^t PLH	Bi	Āi	None	None	Remaining \overline{A} and \overline{B} , C_{n}	P	In-Phase
^t PHL	Bi	Āi	None	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
^t PLH	Āi	None	Bi	Remaining B	Remaining Ā, C _n	G	In-Phase
^t PHL	Āi	None	Bi	Remaining B	Remaining A, C _n	G	In-Phase
^t PLH	Bi	None	Āi	Remaining B	Remaining A, C _n	G	In-Phase
^t PHL	Bi	None	Āi	Remaining B	Remaining A, C _n	G	In-Phase
^t PLH	Cn	None	None	All Ā	All B	Any F or C _{n+4} Any F	In-Phase
t _{PHL}	Cn	None	None	All Ā	All B	Any ₹ or C _{n+4}	In-Phase
^t PLH	Āi	None	Bi	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PHL	Āi	None	Bi	Remaining B	Remaining \overline{A} , C_n Remaining \overline{A} ,	C _{n+4}	Out-of-Phase
^t PLH	Bi	None	Āi	Remaining B	Cn	C _{n+4}	Out-of-Phase
tPHL	Bi	None	Āi	Remaining B	Remaining A,	C _{n+4}	Out-of-Phase



PRODUCT PREVIE

PARAMETER MEASUREMENT INFORMATION

DIFF Mode Test Table

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

	INPUT OTHER INPUT SAME BIT OTHER DATA INPUTS		TA INPUTS	OUTPUT	OUTPUT		
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
^t PLH	Āi	None	Bi	Remaining A	Remaining B, C _n	Fi	In-Phase
^t PHL	Āi	None	Bi	Remaining A	Remaining B, C _n	Fi	In-Phase
[†] PLH	Bi	Āi	None	Remaining A	Remaining B, C _n Remaining B,	Fi	Out-of-Phase
^t PHL	Bi	Āi	None	Remaining A	Remaining B, C _n Remaining A	Fi	Out-of-Phase
^t PLH	Āi	None	Bi	None	and \overline{B} , C_n	P	In-Phase
^t PHL	Āi	None	Bi	None	Remaining \overline{A} and \overline{B} , C_n	P	In-Phase
^t PLH	Bi	Āi	None	None	Remaining A and B, C _n	P	Out-of-Phase
^t PHL	Bi	Āi	None	None	Remaining A and B, C _n	P	Out-of-Phase
^t PLH	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	Ğ	In-Phase
^t PHL	Āi	Bi	None	None	Remaining \overline{A} and \overline{B} , C_n	G	In-Phase
[†] PLH	Bi	None	Āi	None	Remaining \overline{A} and \overline{B} , C_n	G	Out-of-Phase
^t PHL	Bi	None	Āi	None	Remaining A and B, C _n	Ğ	Out-of-Phase
^t PLH	Āi	None	Bi	Remaining A	Remaining B, C _n	A = B	In-Phase
tPHL	Āi	None	Bi	Remaining A	Remaining B, C _n Remaining B,	A = B	In-Phase
^t PLH	Bi	Āi	None	Remaining A	Remaining B, C _n Remaining B,	A = B	Out-of-Phase
[†] PHL	Bi	Āi	None	Remaining A	Remaining B, C _n	A = B	Out-of-Phase
^t PLH	Cn	None	None	All \overline{A} and \overline{B}	None	C _{n+4} or Any F	In-Phase
^t PHL	C _n	None	None	All \overline{A} and \overline{B}	None	C _{n+4} or Any F	In-Phase
^t PLH	Āi	Bi	None	None	Remaining Ā, B, C _n	C _{n+4}	Out-of-Phase
^t PHL	Āi	Bi	None	None	Remaining Ā, B, C _n	C _{n+4}	Out-of-Phase
^t PLH	Bi	None	Āi	None	Remaining Ā, B, C _n	C _{n+4}	In-Phase
^t PHL	Bi	None	Āi	None	Remaining A, B, C _n	C _{n+4}	In-Phase



PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

Logic Mode Test Table

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = M = 0 V

	INPUT	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT	OUTPUT
PARAMETER	UNDER	APPLY	APPLY	APPLY	APPLY	UNDER	WAVEFORM
	TEST	4.5 V	GND	4.5 V	GND	TEST	(SEE NOTE 2)
^t PLH	Āi	Bi	None	None	Remaining A and B, Cn	Fi	Out-of-Phase
[†] PHL	Āi	Bi	None	None	Remaining \overline{A} , and \overline{B} , C_n	Fi	Out-of-Phase
tpLH	Bi	Āi	None	None	Remaining \overline{A} , and \overline{B} , C_n	Fi	Out-of-Phase
[†] PHL	Bi	Āi	None	None	Remaining A, and B, C _n	Fi	Out-of-Phase

General Information	
ACL LSI Products	2
ACL Widebus™ Products	3
BTL Transceiver Products	1
Bus-Termination Array Products	5
Clock Driver Products	6
ECL/TTL Translator Products	
FIFO Products	3
Low-Impedance Line Driver Products)
Memory Driver Products	0
SCOPE™ Testability Products	1
64BCT Series Products	2
Mechanical Data	3

54AC16240, 74AC16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

TI0281-D3605, JULY 1990-REVISED NOVEMBER 1990

Members of the Texas Instruments Widebus™ Family	54AC16240 WD PACKAGE 74AC16240 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1G
 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers 	GND
 Flow-Through Architecture Optimizes PCB Layout 	1Y4
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	2Y2
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process 	2Y3
• 500-mA Typical Latch-Up Immunity at 125°C	3Y2
description	3Y3 16 33 3A3
The 'AC16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	3Y4
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical G (active-low output enable) inputs. The 'AC16240 is packaged in TI's	4Y3

shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54AC16240 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC16240 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

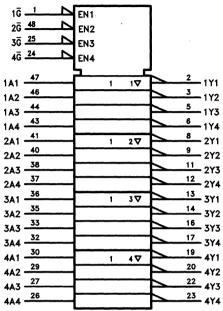
INP	UTS	OUTPUT
G	Α	Y
L	Н	L
L	L	н
Н	Х	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



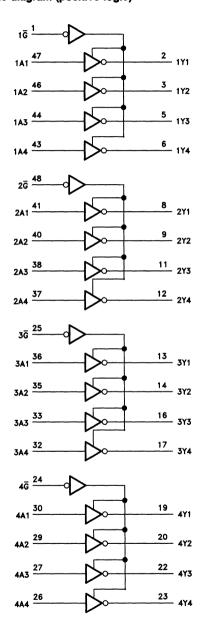
D3605, JULY 1990-REVISED NOVEMBER 1990-Ti0281

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



54AC16240, 74AC16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

TI0281-D3605, JULY 1990-REVISED NOVEMBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, VCC0.5 \	√ to 7 V
Input voltage range, V _I (see Note 1)	+ 0.5 V
Output voltage range, V _O (see Note 1)	+ 0.5 V
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	± 50 mA
Continuous current through V _{CC} or GND pins ±	400 mA
Storage temperature range65°C to	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1624	10	74	AC1624	0	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
VιΗ	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		$V_{CC} = 5.5 V$	3.85			3.85			
		V _{CC} = 3 V		3	0.9			0.9	
V _{IL} Low-level inp	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V
		$V_{CC} = 5.5 V$		EL)	1.65			1.65	
VI	Input voltage		0	SC.	VCC	0		Vcc	V
Vo	Output voltage		0	Į	VCC	0		Vcc	V
		V _{CC} = 3 V		3	-4			-4	
ЮН	High-level output current	$V_{CC} = 4.5 V$		9	-24			-24	mΑ
		$V_{CC} = 5.5 V$	4	2	-24			24	
		V _{CC} = 3V	4		12			12	
IOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mΑ
		$V_{CC} = 5.5 V$			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

D3605, JULY 1990-REVISED NOVEMBER 1990-TI0281

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	4 = 25°	С	54AC	16240	74AC16240			
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
		3 V	2.9			2.9		2.9			
	$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4			
		5.5 V	5.4			5.4		5.4			
V	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.4		2.48		v	
VOH		4.5 V	3.94			3.7		3.8		٧	
	$I_{OH} = -24 \text{mA}$	5.5 V	4.94			4.7		4.8			
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
	$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85			
		3 V			0.1		0.1		0.1		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1		
		5.5 V			0.1		0.1		0.1		
V	IOL = 12 mA	3 V			0.36	_	0.5		0.44	.,	
VOL	Jan - 04 - 4	4.5 V			0.36		√0.5		0.44	٧	
	IOL = 24 mA	5.5 V			0.36	<_\\\\	0.5		0.44		
	IOL = 50 mA†	5.5 V				4	1.65				
	IOL = 75 mA†	5.5 V							1.65		
lį	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
loz	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ	
Icc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ	
Ci	V _I = V _{CC} or GND	5 V		4.5						pF	
Co	VO = VCC or GND	5 V		12						pF	

The Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm0.3~V$ (see Note 3)

FROM	то	T,	1 = 25°	С	54AC	16240	74AC	16240	UNIT
(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
A	V	1.8	5.4	7.5	1.8	8.9	1.8	8.3	
	A Y	2.5	7	9.3	2.5	5 10.8	2.5	10.2	ns
G	V	2.1	6.1	8.5	20	10.2	2.1	9.5	
	Y	2.9	8.4	11.3	2.9	13.5	2.9	12.6	ns
G	V	4.3	6.2	8.3	4.3	9	4.3	8.7	
	r	3.6	6	7.8	3.6	8.5	3.6	8.4	ns
	(INPUT) A G	(INPUT) (OUTPUT) A Y G Y	(INPUT) (OUTPUT) MIN A Y 1.8 2.5 G Y 2.1 2.9 G Y 4.3	(INPUT) (OUTPUT) MIN TYP A Y 1.8 5.4 2.5 7 G Y 2.1 6.1 2.9 8.4 G Y 4.3 6.2	(INPUT) (OUTPUT) MIN TYP MAX A Y 1.8 5.4 7.5 2.5 7 9.3 G Y 2.1 6.1 8.5 2.9 8.4 11.3 G Y 4.3 6.2 8.3	(INPUT) (OUTPUT) MIN TYP MAX MIN A Y 1.8 5.4 7.5 1.8 2.5 7 9.3 2.5 G Y 2.1 6.1 8.5 2.1 G Y 4.3 6.2 8.3 4.3	(INPUT) (OUTPUT) MIN TYP MAX MIN MAX 1.8 5.4 7.5 1.8 8.9 2.5 7 9.3 2.5 10.8 G Y 2.1 6.1 8.5 2.1 10.2 2.9 8.4 11.3 2.9 13.5 G Y 4.3 6.2 8.3 4.3 9	(INPUT) (OUTPUT) MIN TYP MAX MIN MAX MIN A Y 1.8 5.4 7.5 1.8 8.9 1.8 2.5 7 9.3 2.5 10.8 2.5 G Y 2.1 6.1 8.5 2.1 10.2 2.1 2.9 8.4 11.3 2.9 13.5 2.9 4.3 6.2 8.3 4.3 9 4.3	(INPUT) (OUTPUT) MIN TYP MAX MIN MAX MIN MAX A Y 1.8 5.4 7.5 1.8 8.9 1.8 8.3 2.5 7 9.3 2.5 10.8 2.5 10.2 G Y 2.1 6.1 8.5 2.1 10.2 2.1 9.5 2.9 8.4 11.3 2.8 13.5 2.9 12.6 4.3 6.2 8.3 4.3 9 4.3 8.7

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

54AC16240, 74AC16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

TI0281---D3605, JULY 1990---REVISED NOVEMBER 1990

switching characteristics over recommended operating free-air temperature range, VCC = 5 V ± 0.5 V (see Note 4)

PARAMETER	FROM TO	T	T _A = 25°C			16240	74AC			
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .	A	V	1.3	3.3	5.3	1.3	6.2	1.3	5.8	
tPHL		Υ	1.9	4.3	6.5	1.9	7.6	1.9	7.1	ns
tPZH	~	G Y	1.6	3.8	5.9	1,6	7	1.6	6.6	
tPZL	G		3.2	4.7	7.2	€ 2.2	8.7	2.2	8.1	ns
tPHZ	G	5	4.2	6	7.7	4.2	8.4	4.2	8.1	
tPLZ	G	Y	3.4	5.1	6.9	3.4	7.5	3.4	7.3	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
Г	C . Bower dissipation conscitance per letch	Outputs enabled	C: = 50 = 5 4 = 4 MH=	42	ρF
L	Cpd Power dissipation capacitance per latch	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	6	ρr

54ACT16240, 74ACT16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

TI0282-D3606, JULY 1990

 Members of the Texas Instruments Widebus™ Family 	54ACT16240 WD PACKAGE 74ACT16240 DL PACKAGE
•	(TOP VIEW)
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch 	16
Ceramic Flat Packages Using 25-mil	1Y1 🛛 2 47 🔲 1A1
Center-to-Center Pin Spacings	1Y2 🗍 3 46 🗍 1A2
Inputs Are TTL-Voltage Compatible	GND 4 45 GND
3-State Outputs Drive Bus Lines or Buffer	1Y3
Memory Address Registers	1Y4 🛮 6 43 🗎 1A4
•	V _{CC} □7 42 □ V _{CC}
 Flow-Through Architecture Optimizes PCB 	2Y1 🛮 8 41 🗎 2A1
Layout	2Y2
 Distributed V_{CC} and GND Pin Configuration 	GND 10 39 GND
Minimizes High-Speed Switching Noise	2Y3
a EDIOTI /Enhanced Devicements Implement	2Y4 🛘 12 37 🕽 2A4
EPIC™ (Enhanced-Performance Implanted CMOS) 1	3Y1 13 36 3A1
CMOS) 1-μm Process	3Y2
 500-mA Typical Latch-Up Immunity at 125°C 	GND 15 34 GND
	3Y3
description	3Y4 🔲 17 32 🔲 3A4
The 'ACT16240 is a 16-bit buffer and line driver	V _{CC} ☐18 31 ☐ V _{CC}
designed specifically to improve both the	4Y1 19 30 4A1
performance and density of 3-state memory	4Y2
address drivers, clock drivers, and bus-oriented	GND 21 28 GND
receivers and transmitters.	4Y3 🛮 22 27 🖸 4A3
The device can be used as four 4 his huffers	4Y4 23 26 4A4
The device can be used as four 4-bit buffers,	4Ġ

device provides inverting outputs and symmetrical \overline{G} (active-low output enable) inputs. The 'ACT16240 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54ACT16240 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74ACT16240 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

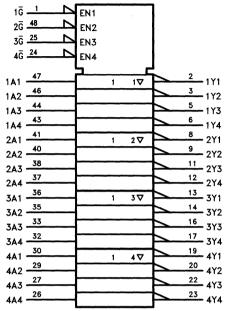
INP	UTS	OUTPUT
G	Α	Y
L	Н	L
L	L	н
н	x	Z

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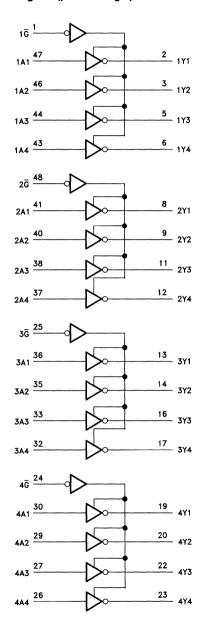
TI0282-D3606, JULY 1990

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



54ACT16240, 74ACT16240 16-BIT BUS DRIVERS WITH 3-STATE OUTPUTS

D3606, JULY 1990-TI0282

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0 \text{ or } V_{ } > V_{CC})$	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT	16240	74ACT	16240	
		MIN MAX		MIN MAX		UNIT
VCC	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	٧
ViH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧
٧ı	Input voltage	0	N €C	0	Vcc	٧
Vo	Output voltage	.0	VCC	0	Vcc	٧
ЮН	High-level output current	8,00	-24		-24	mA
lOL	Low-level output current	6,	24		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater.

3. All V_{CC} and GND pins must be connected to the proper voltage power supply.

TI0282-D3606, JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COMPLTIONS	V	TA	= 25°	С	54ACT	16240	74ACT16240		LINUT
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	Jan 50 . A	4.5 V	4.4			4.4		4.4		
	$IOH = -50 \mu A$	5.5 V	5.4			5.4		5.4		
V	I _{OH} = -24 mA	4.5 V	3.94			3.94		3.8		v
Voн	10H = -24 MA	5.5 V	4.94			4.94		4.8		٧
	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	v
Voi	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
VOL		5.5 V			0.36		0.5		0.44	•
	IOL = 50 mA†	5.5 V				A				
	IOL = 75 mA†	5.5 V				9.3	,		1.65	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1	(2)	±1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			± 0.5	- AZ	±10		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8	42	160		80	μΑ
Mest	Other inputs at	5.5 V			0.9		-		1	mA
ΔlCC‡	One input at 3.4 V, GND or V _{CC}	5.5 V	1		0.9		1		'	IIIA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	$V_O = V_{CC}$ or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \ V \pm 0.5 \ V$ (see Note 4)

DADAMETED	FROM TO		TA	T _A = 25°C			16240	74ACT	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
tPLH	Δ	V	2.3	5	7.7	2.3	9	2.3	8.5		
tPHL	A	·) · · · ·	4.1	6.7	9.2	4.1	1/1.1	4.1	10.2	ns	
^t PZH	5	G Y	2.6	5.6	8.5	2.6	10,1	2.6	9.4		
tPZL	G		3.3	6.7	10.2	3,3	12.2	3.3	11.4	ns	
^t PHZ	PHZ G Y	V	5.9	8.3	11	5.9	12.7	5.9	12		
tPLZ	G	ľ	5.1	7.4	9.9	5.1	11.3	5.1	10.7	ns	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

ſ		PARAMETER	TEST CONDITIONS	TYP	UNIT	
	C _{pd}	Power dissipation capacitance per latch	Outputs enabled Outputs disabled	C _L = 50 pF, f = 1 MHz	38 9	pF

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54AC16244, 74AC16244 16-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

TI0180--- D3465, MARCH 1990

	110180
 Member of the Texas Instruments Widebus™ Family 	54AC16244 WD PACKAGE 74AC16244 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1G (1 48) 2G 1Y1 (2 47) 1A1 1Y2 (3 46) 1A2
 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers 	GND [] 4 45 [] GND 1Y3 [] 5 44 [] 1A3
 Flow-Through Architecture to Optimize PCB Layout 	1Y4 [] 6 43 [] 1A4 V _{CC} [] 7 42 [] V _{CC} 2Y1 [] 8 41 [] 2A1
 Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise 	2Y2 [9 40] 2A2 GND [10 39] GND
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	2Y3
● 500-mA Typical Latch-Up Immunity at 125°C	3Y1 [13 36] 3A1 3Y2
description	3Y3 1 16 33 1 3A3
The 'AC16244 is a 16-bit buffer and line driver designed specifically to improve both the	3Y4 [] 17 32 [] 3A4 V _{CC} [] 18 31 [] V _{CC}
performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be	4Y1 [] 19 30 [] 4A1 4Y2 [] 20 29 [] 4A2 GND [] 21 28 [] GND
used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true	4Y3
outputs and symmetrical $\overline{\mathbf{G}}$ (active-low) outputenable inputs.	4G (24 25) 3G

The 74AC16244 is packaged in the Ti's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16244 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC16244 is characterized for operation from -40° C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



FUNCTION TABLE (each driver)

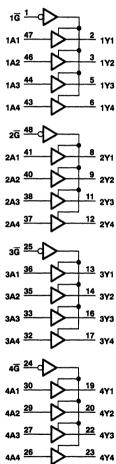
INP	UTS	OUTPUT
Ğ	A	Y
L	Н	Н
L	L	L
Н	Х	z

logic symbol†

•				
1\overline{G} \frac{1}{48} \rightarrow \frac{2\overline{G}}{3\overline{G}} \frac{25}{4\overline{G}} \rightarrow \frac{4}{3\overline{G}} \frac{24}{3\overline{G}} \rightarrow \frac{4}{3\overline{G}} \frac{24}{3\overline{G}} \rightarrow \frac{4}{3\overline{G}} \frac{2}{3\overline{G}} \frac{2}{3\o	EN1 EN2 EN3 EN4			
1A1 47 46		1	1▽	2 3 1Y1
1A2 44				
1A3 43				1Y3
1A4 41				8 1Y4
2A1 40		1	2 ▽	9 2Y1
2A2 38				11 2Y2
2A3				12 2Y3
2A4				13 2Y4
3A1			3 ▽	14 3Y1
3A2				16 3Y2
3A3 32				17 3Y3
3A4		1		19 3Y4
4A1			4 ▽	20 4Y1
4A2 27				22 4Y2
4A3 26				23 4Y3
4A4	L			4Y4

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



54AC16244, 74AC16244 16-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3465, MARCH 1990-TI0180

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC			-0.	5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5	V t	o Vcc	+ 0.5 V
Output voltage range, VO (see Note 1)	0.5	V t	o VCC	+ 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})				±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)				±50 mA
Continuous output current, IO (VO = 0 to VCC)				\pm 50 mA
Continuous current through VCC or GND pins				±400 mA
Storage temperature range		_	-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	54AC16244		74AC16244			LINIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
		V _{CC} = 3 V	2.1			2.1			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		V _{CC} = 5.5 V	3.85			3.85			
		VCC = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	٧
		V _{CC} = 5.5 V			1.65			1.65	1
VI	Input voltage		0		Vcc	0		Vcc	٧
Vo	Output voltage		0		VCC	0		Vcc	٧
		VCC = 3 V			-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V			-24			-24	mA
		V _{CC} = 5.5 V		***************************************	-24			-24	
		V _{CC} = 3 V			12			12	
IOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
		$V_{CC} = 5.5 V$			24			24	
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: All VCC and GND pins must be connected to the proper voltage supply.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST CONDITIONS		T _A = 25°C			54AC	16244	74AC16244		UNIT
PARAMETER		Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	IOH = -50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Vari	IOH = -4 mA	3 V	2.58			2.4		2.48		v
Voн	Jan 24 - 4	4.5 V	3.94			3.7		3.8		٧
	IOH = -24 mA	5.5 V	4.94			4.7		4.8		
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
		3 V			0.1		0.1		0.1	
	IOL = 50 μA	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
V	IOL = 12 mA	3 V			0.36		0.5		0.44	v
VOL	la: = 24 = 4	4.5 V			0.36		0.5		0.44	•
	IOL = 24 mA	5.5 V			0.36		0.5		0.44	
	IOL = 50 mA†	5.5 V					1.65			
	IOL = 75 mA [†]	5.5 V							1.65	
Ŋ	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
loz	V _I = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ
Icc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	V _I = V _{CC} or GND	5 V		12						PΕ

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

54ACT16244, 74ACT16244 16-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

TI0181--D3465, MARCH 1990--REVISED JULY 1990

Members of the Texas Instruments Widebus™ Family	54ACT16244 WD PACKAGE 74ACT16244 DL PACKAGE
Packaged in Shrink Small Outline 300-mil	(TOP VIEW)
	-
Packages (SSOP) and 380-mil Fine-Pitch	1Ġ[] 1
Ceramic Flat Packages Using 25-mil	1Y1[] 2 47[] 1A1
Center-To-Center Pin Spacings	1Y2[]3 46[]1A2
Inputs are TTL-Voltage Compatible	GND[] 4 45[] GND
a Cotata Custanuta Bulua Dua Linaa ay Buffay	1Y3[] 5 44[] 1A3
3-State Outputs Drive Bus Lines or Buffer	1Y4[] 6 43[] 1A4
Memory Address Registers	V _{CC} [] 7 42]] V _{CC}
Flow-Through Architecture Optimizes PCB	2Y1 8 41 2A1
Layout	2Y2[] 9 40[] 2A2
Distributed Voc and CND Din Configuration	GND[] 10 39[] GND
Distributed V _{CC} and GND Pin Configuration Minimize High Speed Switching Major	2Y3[] 11 38[] 2A3
to Minimize High-Speed Switching Noise	2Y41 12 37 2A4
 EPIC™ (Enhanced-Performance Implanted 	3Y1 13 36 3A1
CMOS) 1-μm Process	3Y2[] 14 35[] 3A2
● 500-mA Typical Latch-Up Immunity at 125°C	GND 15 34 GND
• 500-IIIA Typical Latell-Op Illilliumity at 125 C	3Y3 1 16 33 1 3A3
description	3Y41 17 321 3A4
uescription	V _{CC} [] 18 31 V _{CC}
The 'ACT16244 is a 16-bit buffer and line driver	4Y1 19 30 4A1
designed specifically to improve both the	4Y21 20 291 4A2
performance and density of 3-state memory	GND 21 28 GND
address drivers, clock drivers, and bus-oriented	
receivers and transmitters. The device can be	
used as four 4-bit buffers, two 8-bit buffers, or	4Y4[] 23 26] 4A4
one 16-bit buffer. This device provides true	4G[24 25 3G
outputs and symmetrical G (active-low) output-	the same of the sa

The 74ACT16244 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16244 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74ACT16244 is characterized for operation from -40° C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

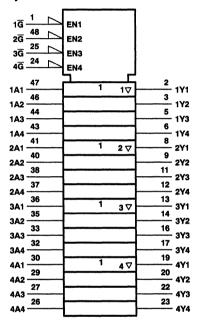


enable inputs.

FUNCTION TABLE (each driver)

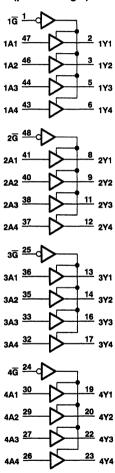
ſ	INP	UTS	OUTPUT
Ī	Ğ	A	Y
	L	Н	Н
	L	L	L
	н	Χ	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



54ACT16244, 74ACT16244 16-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3465, MARCH 1990-REVISED JULY 1990-TI0181

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	0.5 V to 7 V
Input voltage range, VI (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54ACT16244		74ACT	16244	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0,	2,4ec	0	VCC	٧
Vo	Output voltage	, (9)	*/ACC	0	VCC	٧
ЮН	High-level output current	64,04	-24		-24	· mA
lOL	Low-level output current	۷,	24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{3.} All V_{CC} and GND pins must be connected to the proper voltage supply.

TI0181-D3465, MARCH 1990-REVISED JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		T	= 25°	С	54ACT	16244	74ACT16244		LIMIT
PARAMETER		VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	Jan - 50 - A	4.5 V	4.4			4.4		4.4		
	IOH = -50 μA	5.5 V	5.4			5.4		5.4		
Vou	I _{OH} = −24 mA	4.5 V	3.94			3.7		3.8		٧
VOH	10H = −24 mA	5.5 V	4.94			4.7		4.8		٧
	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
	IOL = 50 μA	4.5 V			0.1		0.1		0.1	
	10L - 50 µA	5.5 V			0.1		0.1		0.1	
Va.	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	٧
VOL		5.5 V			0.36	20.	0.5		0.44	V
	IOL = 50 mA†	5.5 V				(o.	1.65			1
	IOL = 75 mA†	5.5 V				ά,			1.65	
1	V _I = V _{CC} or GND	5.5 V			±0.1		± 1		±1	μΑ
loz	V _I = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ
lcc	$V_{\parallel} = V_{CC}$ or GND, $I_{O} = 0$	5.5 V			8		160		80	μΑ
Alaat	One input at 3.4 V,	5.5 V			0.9				1	4
∆lcc‡	Other inputs at GND or VCC	5.5 V			0.9		'		'	mA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
C _o	V _I = V _{CC} or GND	5 V		13.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (unless otherwise noted) (see Note 4)

PARAMETER	FROM	то	T/	T _A = 25°C		54ACT16244		74ACT16244		LINUT
	(INPUT) (OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
tPLH .		Y	4	6.5	8.5	4	10.3	4	9.4	ns
tPHL	1 ^		3.4	6.3	8.7	3.4	5/10/1	3.4	9.5	
^t PZH	G		3	5.8	8.1	્ર	√9.5	3	8.9	ns
tPZL] 4	Ť	3.7	6.7	9.3	₹3,7	· 11	3.7	10.3	
tpHZ	G	.,	5.4	8.1	10.3	5.4	12	5.4	11.3	
tPHL	1 4	Y	5	7.5	9.5	5	10.9	5	10.3	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
	Device discipation consists of the least	Outputs enabled	C	39	
Cpd Power dissipation capacitance per latch		Outputs disabled	C _L = 50 pF, f = 1 MHz	11	pF

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54AC16245, 74AC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0173--- D3451, MARCH 1990

•	Members	of	the	Texas	Instruments
	Widebus [™]	' Fa	amil	v	

- Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control inputs (DIR). The enable inputs (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

54AC16245 ... WD PACKAGE 74AC16245 ... DL PACKAGE (TOP VIEW)

1DIR	, 0	40	1G
1B1			1A1
1B2	-		1A2
GND [4		GND
1B3 []	5		1A3
1B4 [6		1A4
Vcc [7	42	V _{CC}
1B5 [8	41	1A5
1B6 🛚	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8			1A8
2B1 [2A1
2B2			2A2
GND [GND
			2A3
2B3 [
2B4 [17	32	2A4
V _{CC} [Vcc
2B5 [19		2A5
2B6 [20	29	2A6
GND [21	28	GND
2B7 [22	27	2A7
2B8			2A8
2DIR			2G
20111	<u> </u>	لّــــ	,

The 74AC16245 is packaged in Tl's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

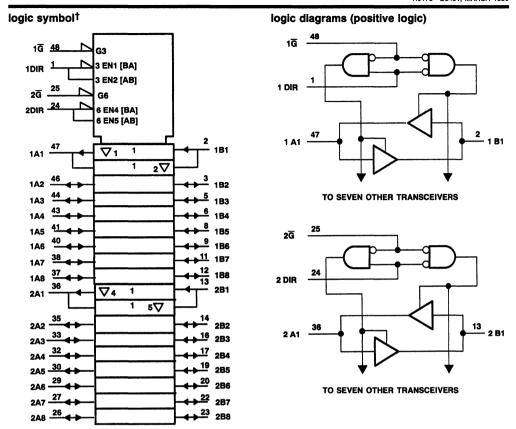
The 54AC16245 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16245 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE

	TROL PUTS	OPERATION
G	DIR	
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

EPIC and Widebus are trademarks of Texas Instruments Incorporated.





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3451, MARCH 1990-TI0173

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16245			74	AC1624	5		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧	
		VCC = 3 V	2.1			2.1				
VIH	VIH High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧	
		$V_{CC} = 5.5 V$	3.85			3.85				
V _{IL} Lo		VCC = 3 V			0.9			0.9		
	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	v	
		$V_{CC} = 5.5 V$			1.65			1.65		
Vį	Input voltage	,	0	08	VCC	0		VCC	٧	
Vo	Output voltage		0	4	VCC	0		VCC	٧	
		VCC = 3 V		200	-4			-4		
ЮН	High-level output current	$V_{CC} = 4.5 V$	00		-24			-24	mA	
		$V_{CC} = 5.5 V$	4		-24			-24		
		V _{CC} = 3 V			12			12		
IOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA	
		$V_{CC} = 5.5 V$			24			24		
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V	
TA	Operating free-air temperature		-55		125	-40		85	°C	

NOTE 2: All VCC and GND pins must be connected to the proper voltage supply.

TI0173-D3451, MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA	= 25°	С	54AC16245		74AC16245		UNIT
PA	HAMEIER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			3 V	2.9			2.9		2.9		
		$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
V		IOH = -4 mA	3 V	2.58			2.4		2.48		٧
VOH		IOH = -24 mA	4.5 V	3.94			3.7		3.8		٧
j		10H = -24 MA	5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V					Á	3.85		
			3 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	4.5 V			0.1	"O _L	0.1		0.1	
			5.5 V			0.1	4°34	0.1		0.1	
\ _{V-} .		IOL = 12 mA	3 V			0.36	~	0.5		0.44	v
VOL		1 044	4.5 V		-	0.36		0.5		0.44	٧
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA [†]	5.5 V					1.65			
		IOL = 75 mA [†]	5.5 V							1.65	
lį	Control inputs	VI = VCC or GND	5.5 V			±0.1		±1		±1	μΑ
loz	A or B ports‡	V _I = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	Control inputs	VI = VCC or GND	5 V		4.5						pF
Cio	A or B ports	V _I = V _{CC} or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm~0.3~V$ (see Figure 1)

DADAMETED	FROM	то	T/	T _A = 25°C		54AC16245		74AC16245		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .	A D	D A	2.5	7.6	10.4	2.5	12.8	2.5	11.9	ns
tPHL	A or B	B or A	3.1	9	12.3	3.1	14.3	3.1	13.5	
^t PZH	G	A D	2.8	8.6	11.8	2,8	44.4	2.8	13.2	
tPZL	7 G	A or B	3.9	12	16.2	₹3.9	19.3	3.9	18	ns
t _{PHZ}	G	A or B	5.3	8.4	10.4	5.3	11.6	5.3	11.2	
tPLZ	7 "		4.4	7.7	9.7	4.4	10.6	4.4	10.3	ns

switching characteristics over recommended operating free-air temperature range, VCC = 5 V \pm 0.5 V (see Figure 1)

PARAMETER	FROM	то	T,	= 25°	С	54AC	16245	74AC	6245	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
tPLH	A or D	B or A	2	4.6	6.9	2	8.5	2	7.9	ns
tPHL	A or B		2.5	5.2	7.9	2.5	9,5	2.5	8.9	
tPZH	G	A D	2.3	4.9	7.5	2.9	√9.3	2.3	8.6	
tPZL	G	A or B	3	6.2	9.5	₹ 3<	11.6	3	10.7	ns
t _{PHZ}	G	A or B	5	7.2	9.1	₹5	10.2	5	9.8	
tPLZ	G		4.2	6.2	8.1	4.2	9	4.2	8.7	ns

[‡] For I/O ports, the parameter IO7 includes the input leakage current.

54AC16245, 74AC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3451, MARCH 1990-TI0173

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
<u> </u>	Down discination consistence	Outputs enabled	C: - 50 - 5 4 - 4 MI-	43	nΕ
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	8	PF

54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0182-D3402, DECEMBER 1989-REVISED MARCH 1990

- Members of the Texas Instruments Widebus™ Family
- Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ACT16245 is a 16-bit bus transceiver organized as a dual-octal noninverting 3-state transceiver and is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input $(\overline{\mathbf{G}})$ can be used to disable the device so that the buses are effectively isolated.

The 74ACT16245 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16245 is characterized over the full military temperature range of -55° C to 125°C. The 74ACT16245 is characterized for operation from -40° C to 85° C.

54ACT16245 ... WD PACKAGE 74ACT16245 ... DL PACKAGE (TOP VIEW)

		-	
1DIR[1 U	48	1G
1B1[2	47	1A1
1B2	3	46	1A2
GND[4	45	GND
1B3[5	44	1A3
1B4[6	43	1A4
V _{CC} [7	42	Vcc
1B5[8	41	1A5
1B6[9	40	1A6
GND[10	39	GND
1B7[11	38	1A7
1B8[12	37	1A8
2B1 [13	36	2A1
2B2[14	35	2A2
GND[15	34	GND
2B3[16	33	2A3
2B4[17		2A4
V _{CC} [18	31	V _{CC}
2B5[19	30	2A5
2B6[20	29	2A6
GND[21	28	GND
2B7[22	27	2A7
2B8[23		2A8
2DIR[24	25	2Ğ
į			

FUNCTION TABLE

	FUNCT	ON IABLE
	ITROL PUTS	OPERATION
Ğ	DIR	
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

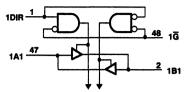
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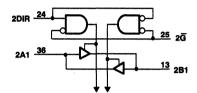
logic symbol† 1Ğ G3 3 EN1 [BA] 1DIR 3 EN2 [AB] 25 2G G6 6 EN4 [BA] 2DIR 6 EN5 [AB] ∇1 1B1 1A1 2▽ 1A2 5 1B3 1A3 6 1B4 1A4 8 1B5 1A5 9 1B6 1A6 11 1B7 1A7 12 1B8 1A8 13 2B1 2A1 5▽ 14 2B2 2A2 16 2B3 2A3 17 2B4 19 2B5 2A5

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



TO SEVEN OTHER TRANSCEIVERS



TO SEVEN OTHER TRANSCEIVERS

54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0182-D3402, DECEMBER 1989-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }$ ($V_1 < 0$ or $V_1 > V_{CC}$)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54ACT	54ACT16245		16245	
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	124	2		٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	√Ç [©] VCC	0	VCC	٧
Vo	Output voltage	0 🔨	VCC	0	Vcc	٧
ЮН	High-level output current	The state of the s	-24		-24	mA
IOL	Low-level output current	45	24		24	mA
Δt/Δν	Input transition rise or fall rate	€ 0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	ô

NOTES: 2. Unused or floating inputs should be tied to VCC through a pullup resistor of approximately 5 k Ω or greater.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{3.} All V_{CC} and GND pins must be connected to the proper voltage supply.

D3402, DECEMBER 1989—REVISED MARCH 1990—TI0182

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				TA	= 25°	С	54ACT	16245	74ACT16245			
VOL Control inputs	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT		
		I 50 A	4.5 V	4.4			4.4		4.4			
		$IOH = -50 \mu A$	5.5 V	5.4			5.4		5.4			
		Jan. — 04 4	4.5 V	3.94			3.94		3.8		v	
VOH		IOH = -24 mA	5.5 V	4.94			4.94		4.8		٧	
		$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V						3.85			
,		In 50 A	4.5 V			0.1		0.1		0.1		
VoL	IOL = 50 μA	5.5 V			0.1		0.1		0.1			
	L 04 - 4	4.5 V			0.36	_	0.5		0.44	0.44 V		
VOL		IOL = 24 mA	5.5 V			0.36	-05	0.5		0.44	٧	
		IOL = 50 mA†	5.5 V				64,04	1.65				
		IOL = 75 mA†	5.5 V				4,			1.65		
lį.	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ	
416		One input at 3.4 V,	F 5 1/									
ΔICC [§]		Other inputs at GND or VCC	5.5 V			0.9		'		1	mA	
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF	
Cio	A or B ports	V _O = V _{CC} or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Figure 1)

PARAMETER	FROM	ТО	T	T _A = 25°C			54ACT16245		74ACT16245	
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .	A D	B or A	3.2	6.9	9.3	3.2	11.5	3.2	10.5	ns
tpHL.	A or B		2.6	6.4	9.2	2.6	24121	2.6	10.2	
^t PZH	G	B or A	2.7	6.4	9.1	2.7	10.9	2.7	10	
tPZL.	G		3.4	7.4	10.5	3.4	12.6	3.4	11.6	ns
tPHZ	<u> </u>	D A	5.8	9.2	11.6	5.8	13.4	5.8	12.6	
^t PLZ	G	B or A	5.5	8.5	10.8	5.5	12.7	5.5	11.8	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Down dissination consistence nor transactives	Outputs enabled	C _I = 50 pF, f = 1 MHz	52	pF
C _{pd}	Power dissipation capacitance per transceiver	Outputs disabled	CL = 50 pr, 1 = 1 MHz	10	p⊢

[‡] For I/O ports, the parameter IOZ includes the input leakage current I_I.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

TI0154-D3467, MARCH 1990

•	Member	of the	Texas	Instruments	Widebus™
	Family				

- Packaged in Shrink Small Outline 300-mll Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Flow-Through Architecture to Optimize PCB Lavout
- Distributed Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16373 is a 16-bit D-type transparent latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches will follow the D inputs if enable C is taken high. When C is taken low, the Q outputs will be latched at the levels set up at the D inputs.

54AC16373 ... WD PACKAGE 74AC16373 ... DL PACKAGE (TOP VIEW)

10E[1	48	1C
1Q1[2	47	1D1
1Q2[3	46] 1D2
GND[4	45] GND
1Q3[5	44] 1D3
1Q4[6	43] 1D4
Vcc[7] v _{cc}
1Q5[8] 1D5
1Q6[9] 1D6
GND[] GND
1Q7[] 1D7
1Q8[]	1		1D8
2Q1[2D1
2Q2[]			2D2
GND[15] GND
2Q3[16		2D3
2Q4	17		2D4
Vcc	18] v _{cc}
2Q5[19		2D5
2Q6[20		2D6
GND[21] GND
2Q7[22		2D7
2Q8	23		2D8
2OE[24	25	2C
			l

A buffered output-enable input \overline{OE} can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control \overline{OE} does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16373 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16373 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16373 is characterized for operation from -40° C to 85°C.

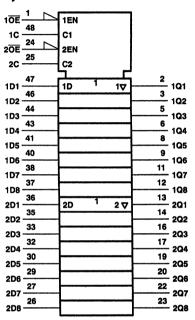
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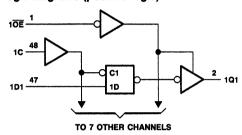
FUNCTION TABLE

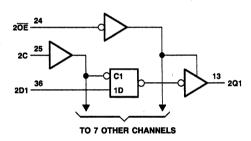
1	NPUTS		OUTPUT
ŌĒ	С	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
н	×	Х	z

logic symbol†



logic diagrams (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TI0154--- D3467, MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	± 50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

			54	4AC1637	'3	74	IAC1637	3	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 3)		3	5	5.5	3	5	5.5	V
		V _{CC} = 3 V	2.1			2.1			
VIH	High-level input voltage	VCC = 4.5 V	3.15			3.15			٧
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
Vi	Input voltage		0		Vcc	0		Vcc	٧
Vo	Output voltage		0		Vcc	0		Vcc	V
		V _{CC} = 3 V			-4			-4	mA
ЮН	High-level output current	V _{CC} = 4.5 V			-24			-24	
		V _{CC} = 5.5 V			-24			-24	
		V _{CC} = 3 V			12			12	
I OL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater.

3. All VCC and GND pins must be connected to the proper voltage supply.

D3467, MARCH 1990-TI0154

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		Γ.,	T	= 25°	С	54AC	16373	74AC1	16373	
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Ma	IOH = -4 mA	3 V	2.58			2.4		2.48		٧
VOH	Jan. — 04 m4	4.5 V	3.94			3.7		3.8		٧
	IOH = -24 mA	5.5 V	4.94			4.7		4.8		
	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
		3 V			0.1		0.1		0.1	ط ا
	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
14	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	.,
VOL		4.5 V			0.36		0.5		0.44	V
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
	IOL = 50 mA†	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
l _l	V _I = V _{CC} or GND	5.5 V			±0.1	,	±1		±1	μΑ
loz	V _I = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	V _I = V _{CC} or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



TI0150-D3468, MARCH 1990-REVISED JUNE 1990

Members of the Texas Instruments	54ACT16373 WD PACKAGE 74ACT16373 DL PACKAGE
Widebus™ Family	(TOP VIEW)
Packaged in Shrink Small Outline 300-mil	(IOF VIEW)
Packages (SSOP) and 380-mil Fine-Pitch	10E 1 48 1C
Ceramic Flat Packages Using 25-mil Center-	1Q1 2 47 1D1
to-Center Pin Spacings	1Q2[] 3 46[] 1D2
	GND[] 4 45 GND
Inputs are TTL-Voltage Compatible	1Q3 5 44 1 1D3
3-State Bus-Driving True Outputs	1Q4 6 43 11D4
o Full Devellat Assess for Londing	V _{CC} 7 42 V _{CC}
Full Parallel Access for Loading	1Q5[] 8 41] 1D5
Buffered Control Inputs	1Q6[] 9 40]] 1D6
a Flow Through Architecture Ontimines DCB	GND[] 10 39[] GND
Flow-Through Architecture Optimizes PCB	1Q7[] 11 38[] 1D7
Layout	1Q8[] 12 37 [] 1D8
 Distributed Center-Pin V_{CC} and GND 	2Q1 13 36 2D1
Configurations to Minimize High-Speed	2Q2 14 35 2D2
Switching Noise	GND[] 15 34
a FDIOTI (Enhanced Devicements Implement	2Q4[17 32] 2D4
EPIC™ (Enhanced-Performance Implanted CMOS) 1 um Process	V _{CC} 18 31 V _{CC}
CMOS) 1-μm Process	2Q5[19 30] 2D5
 500-mA Typical Latch-Up Immunity at 125°C 	2Q6 20 29 2D6
	GND[21 28 GND
description	2Q7[] 22 27[] 2D7
The ACT16070 is a 16 bit D time transparent	2Q8[] 23 26[] 2D8
The 'ACT16373 is a 16-bit D-type transparent	2 0E [] 24 25] 2C
latch with 3-state outputs designed specifically	

It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches will follow the D inputs if enable C is taken high. When C is taken low, the Q outputs will be latched at the levels set up at the D inputs.

A buffered output-enable input OE can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output enable OE does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16373 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16373 is characterized over the full military temperature range of -55°C to 125°C. The 74ACT16373 is characterized for operation from -40° C to 85°C.

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for driving highly capacitive or relatively low-

impedance loads.

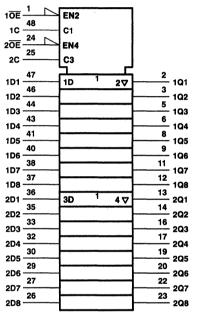


D3468, MARCH 1990-REVISED JUNE 1990-TI0150

FUNCTION TABLE (each section)

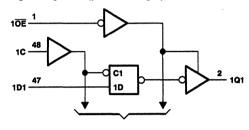
ı	NPUTS	OUTPUT	
OE	С	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
н	X	X	z

logic symbol†

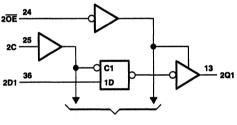


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



TO 7 OTHER CHANNELS



TI0150--- D3468, MARCH 1990--- REVISED JUNE 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	±400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16373		74ACT16373		UNIT	
		MIN MAX		MIN MAX			
Vcc	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage	2		2		V	
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage	0.	VACC	0	VCC	٧	
Vo	Output voltage	(0)	VCC	0	Vcc	٧	
ЮН	High-level output current	24,24	- 24		-24	mA	
IOL	Low-level output current	8	24		24	mA	
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V	
TA	Operating free-air temperature	-55	125	- 40	85	°C	

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater.

3. All VCC and GND pins must be connected to the proper voltage supply.

D3468, MARCH 1990-REVISED JUNE 1990-Ti0150

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445772	METER TEST CONDITIONS VCC TA = 25°C		54ACT	16373	74ACT	16373				
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4		
	1.04 35 ///	5.5 V	5.4			5.4		5.4		
Voн	I _{OH} = -24 mA	4.5 V	3.94			3.7		3.8		v
VOH	10H 24111X	5.5 V	4.94			4.7		4.8		•
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
VOL	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	v
·OL		5.5 V			0.36	_,	0.5		0.44	•
	I _{OL} = 50 mA [†]	5.5 V				-05	1.65			
	IOL = 75 mA†	5.5 V				880	/		1.65	
l _l	VI = VCC or GND	5.5 V			±0.1	6.	±1		±1	μΑ
loz	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
Icc	VI = VCC or GND, IO = 0	5.5 V			8		160		80	μΑ
ΔlCC‡	One input at 3.4 V,	5.5 V		1.1000	0.9		1		1	mA
	Other inputs at GND or VCC	0.5 1			5.5		'		'	""
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	VO = VCC or GND	5 V		12						pF

T Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (see Figure 1)

		T _A = 25°C	54ACT16373	74ACT16373	
l		MIN MAX	MIN MAX	MIN MAX	UNIT
tw	Pulse duration, C high	4	4	4	ns
tsu	Setup time, data before C↓	1	\$\sqrt{3\sqrt{\circ}}	1	ns
th	Hold time, data after C↓	5	₹5	5	ns

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T/	= 25°	С	54ACT	16373	74ACT	16373	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .			3.8	7.9	9.4	3.8	11.8	3.8	11.1	
tPHL	D	Q	3.1	8.2	9.7	3.1	13	3.1	12.3	ns
tPLH .	С		4.6	9.3	10.8	4.6	3.7	4.6	12.8	
tPHL		Q	4.5	9.1	10.5	4.5	ô13	4.5	12.2	ns
tPZH	ŌĒ	0	3.1	8	9.5	₹3,1	13	3.1	12.1	
tPZL.	OE	Q	3.8	9.4	11.1	3.8	15.1	3.8	14.2	ns
tPHZ	ŌĒ		5.3	8.6	9.9	5.3	11	5.3	10.7	
tPLZ	OE	Q	4.3	7.4	8.7	4.3	9.8	4.3	9.4	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
C _{pd}	Power discipation annuitance and lateb	Outputs enabled	C: - 50 - 5 4 - 4 M I-	43	
	Power dissipation capacitance per latch	Outputs disabled	C _L = 50 pF, f = 1 MHz	4.5	pF

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54AC16374, 74AC16374 16-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0193-D3470, MARCH 1990

 Member of the Texas Instruments Widebus™ Family 	54AC16374 WD PACKAGE 74AC16374 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	10E[1 48] 1CLK 1Q1[2 47] 1D1 1Q2[3 46] 1D2
3-State Bus-Driving True Outputs	GND[] 4 45 [] GND 1Q3 [] 5 44 [] 1D3
Full Parallel Access for Loading	1Q4[] 6 43[] 1D4
 Flow-Through Architecture to Optimize PCB Layout 	V _{CC} [] 7
 Distributed Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise 	GND 10 39 GND 1Q7 11 38 1D7 1Q8 12 37 1D8
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	2Q1[] 13 36 [] 2D1 2Q2[] 14 35 [] 2D2 GND[] 15 34 [] GND
● 500-mA Typical Latch-Up Immunity at 125°C	2Q3[] 16 33] 2D3 2Q4[] 17 32] 2D4
description	V _{CC} 18 31 V _{CC}
The 'AC16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.	2Q5 19 30 2D5 2Q6 20 29 2D6 GND 21 28 GND 2Q7 22 27 2D7 2Q8 23 26 2D8 2OE 24 25 2CLK

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of CLK, the Q outputs of the flip-flop are set to the logic levels set up at the D inputs.

An output enable input \overline{OE} can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output enable \overline{OE} does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16374 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16374 is characterized for operation from -40° C to 85°C.

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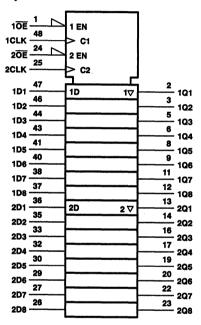


D3470, MARCH 1990-TI0193

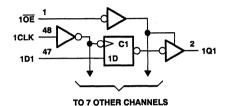
FUNCTION TABLE

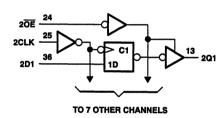
I	NPUTS		OUTPUT
ŌĒ	С	D	Q
L	<u> </u>	Н	Н
L	1	L	L
L	Х	X	QO
L	1	Х	Q _O Q _O
н	Х	Х	z

logic symbol†



logic diagrams (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TI0193--- D3470, MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC			-0.5	V to	7 V
Input voltage range, V _I (see Note 1)	0.5	V to	V _C C	+ 0	.5 V
Output voltage range, Vo (see Note 1)	0.5	V to	V _C C	+ 0).5 V
Input clamp current, $I_{ K }(V_{ } < 0 \text{ or } V_{ } > V_{CC})$				±20	mA
Output clamp current, IOK (VO < 0 or VO > VCC)				±50	mA (
Continuous output current, IO (VO = 0 to VCC)				±50	mA
Continuous current through VCC or GND pins			:	± 400	mA (
Storage temperature range			65°C	to 15	50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1637	4	74AC16374			LIMIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
		V _{CC} = 3 V	2.1			2.1			
٧н	H High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		V _{CC} = 5.5 V	3.85			3.85			
		VCC = 3 V			0.9			0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
VI	Input voltage		0		VCC	0		VCC	٧
Vo	Output voltage		0		VCC	0		VCC	٧
		VCC = 3 V			-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V			-24			-24	mA
		V _{CC} = 5.5 V			-24			-24	
		V _{CC} = 3 V			12			12	
IOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
	·	V _{CC} = 5.5 V			24			24	
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

D3470, MARCH 1990-TI0193

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST SOMBITIONS		TA	= 25°C	54AC	16374	74AC1	6374	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP MA	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9		2.9		2.9		
	IOH = - 50 μA	4.5 V	4.4		4.4		4.4		
		5.5 V	5.4		5.4		5.4		
V	IOH = -4 mA	3 V	2.58		2.4		2.48		V
VOH	lou = -24 mA	4.5 V	3.94		3.7		3.8		V
	IOH = -24 mA	5.5 V	4.94		4.7		4.8		
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				
	$IOH = -75 \text{mA}^{\dagger}$	5.5 V					3.85		
		3 V		0.	1	0.1		0.1	
	IOL = 50 μA	4.5 V		0.	1	0.1		0.1	
		5.5 V		0.	1	0.1		0.1	
. Va.	I _{OL} = 12 mA	3 V		0.3	6	0.5		0.44	V
VOL	Jan - 04 - 4	4.5 V		0.3	6	0.5		0.44	v
	IOL = 24 mA	5.5 V		0.3	6	0.5		0.44	
	IOL = 50 mA†	5.5 V				1.65			
	IOL = 75 mA [†]	5.5 V						1.65	
ll li	VI = VCC or GND	5.5 V		±0.	1	± 1		±1	μΑ
loz	VO = VCC or GND	5.5 V		±0.	5	±10		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8	160		80	μΑ
Ci	VI = VCC or GND	5 V		4.5					рF
Co	V _O = V _{CC} or GND	5 V		12					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm~0.3~V$ (unless otherwise noted) (see Note 3)

			T _A = 25°C		TA = 25°C 54AC16374		74AC16374		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency								MHz
	D.J. J. W.	CLK low							
tW	Pulse duration	CLK high							ns
tsu	Setup time, data before C ↑								ns
th	Hold time, data after C↑								ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TI0193-D3470, MARCH 1990

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Note 3)

			T _A =	25°C	54AC	16374	74AC	16374	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency								MHz
	D. J	CLK low							
tW	Pulse duration	CLK high							ns
tsu	Setup time, data before C↑								ns
th	Hold time, data after C↑								ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Note 3)

DADAMETED	FROM	TO	TO T _A = 25°C		54AC16374		74AC16374		LINUT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax										MHz
tPLH .	CLK	Q								ns
t _{PHL}	OLK	<u> </u>								115
^t PZH	ŌĒ	Q								
tPZL)	ų ,								ns
^t PHZ	ŌĒ	Q								200
tPLZ) OE	ď								ns

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm~0.5~V$ (unless otherwise noted) (see Note 3)

DADAMETED	FROM	TO	T,	$T_A = 25^{\circ}C$		54AC16374		74AC16374		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax										MHz
tPLH	CLK	Q								
[†] PHL] OLK	Ų.								ns
^t PZH	ŌĒ									
^t PZL] OE	Q								ns
tPHZ	ŌĒ	_								
tPLZ] 05	Q								ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT	
^ .	Device discipation associations	Outputs enabled	O: - 50 - 5 4 - 4 MU-		ρF	
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$		рг	1

PRODUCT PREVIEW

TI0195-D3469, MARCH 1990-REVISED JUNE 1990

 Members of the Texas Instruments Widebus™ Family 		WD PACKAGE DL PACKAGE
•	(TOP	VIEW)
Packaged in Shrink Small Outline 300-mil Packaged (CSOR) and 300 mil Fine Bitch		J
Packages (SSOP) and 380-mil Fine-Pitch	10E[] 1	48 1 1CLK
Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings	1Q1 [] 2	47 1D1
Center-to-Center Fin Spacings	1Q2[] 3	46 1D2
 Inputs are TTL-Voltage Compatible 	GND 4	45 GND
3-State Bus-Driving True Outputs	1Q3[] 5	44 1D3
•	1Q4 [] 6	43 1D4
Flow-Through Architecture Optimizes PCB	V _{CC} [] 7	42 V _{CC}
Layout	1Q5[] 8	41 1D5
Distributed Center-Pin V _{CC} and GND Pin	1Q6[] 9	· · ·
Configurations to Minimize High-Speed	GND 10	
Switching Noise	107 11	
● EDIC™ (Enhanced Performance Implented	1Q8[] 12	37 D 1D8
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	2Q1 13	
CMOS) 1-µIII Flocess	2Q2 14	35 2D2
● 500-mA Typical Latch-Up Immunity at 125°C	GND 15	34 [] GND
	2Q3 16	33 2D3
description	204 17	32 2D4
The 'ACT16374 is a 16-bit edge-triggered	V _{CC} 18	31 [] V _{CC}
D-type flip-flop with 3-state outputs designed	2Q5[] 19	30 2D5
specifically for driving highly capacitive or	2Q6[] 20	29 2D6
relatively low-impedance loads. It is particularly	GND 21	28 [] GND
suitable for implementing buffer registers, I/O	2Q7[] 22	27 2D7
ports, bidirectional bus drivers, and working	2Q8[] 23	26 2D8
registers.	2 0E [] 24	25 2CLK

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of CLK, the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

An output-enable input \overline{OE} can be used to place the outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output-enable \overline{OE} does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16374 is characterized over the full military temperature range of -55° C to 125°C. The 74ACT16374 is characterized for operation from -40° C to 85°C.

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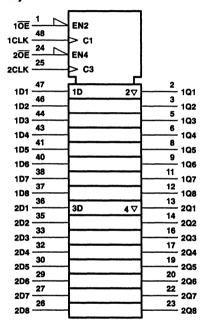


TI0195-D3469, MARCH 1990-REVISED JUNE 1990

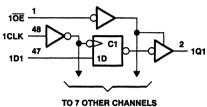
FUNCTION TABLE (each section)

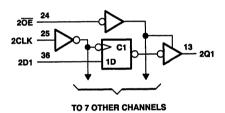
	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	QO
н	X	Х	z

logic symbol†



logic diagrams (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3469, MARCH 1990—REVISED JUNE 1990—TI0195

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}			-0.5	V to 7 V
Input voltage range, V _I (see Note 1)	-0.5	V to	Vcc	+ 0.5 V
Output voltage range, VO (see Note 1)	-0.5	V to	VCC	+ 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})				$\pm 20 \ mA$
Output clamp current, IOK (VO < 0 or VO > VCC)				$\pm 50~\text{mA}$
Continuous output current, IO (VO = 0 to VCC)				$\pm 50~\text{mA}$
Continuous current through VCC or GND pins			±	± 400 mA
Storage temperature range		_	65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54	ACT163	74	74	ACT163	74	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	٧
٧н	High-level input voltage	2		542	2			٧
VIL	Low-level input voltage			0.8			0.8	٧
۷į	Input voltage	0	00	VCC	0		VCC	٧
Vo	Output voltage	0	6	Vcc	0		VCC	٧
ЮН	High-level output current		2,	-24			-24	mA
lOL	Low-level output current	60		24			24	mA
Δt/Δν	Input transition rise or fall rate	₹ 0		10	0		10	ns/V
TA	Operating free-air temperature	-55		125	-40		85	ů

NOTE 2: All VCC and GND pins must be connected to the proper voltage supply.

TI0195-D3469, MARCH 1990-REVISED JUNE 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COMPLETIONS		TA	= 25°	С	54ACT	16374	74ACT	16374	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	10 50	4.5 V	4.4			4.4		4.4		
	$IOH = -50 \mu A$	5.5 V	5.4			5.4		5.4		
V	IOH = -24 mA	4.5 V	3.94			3.94		3.8		v
VOH	IOH = -24 MA	5.5 V	4.94			4.94		4.8		v
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
	$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
	lo: = 504	4.5 V			0.1		0.1		0.1	
	IOL = 50 μA	5.5 V			0.1		0,1		0.1	
V	10 044	4.5 V			0.36	-0	√√0.5		0.44	v
VOL	IOL = 24 mA	5.5 V			0.36	9505	0.5		0.44	v
	$IOL = 50 \text{ mA}^{\dagger}$	5.5 V				4,	1.65			
	$IOL = 75 \text{ mA}^{\dagger}$	5.5 V							1.65	
li .	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
loz	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
ΔlCC‡	One input at 3.4 V,	5.5 V			0.9				1	m A
□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	Other inputs at GND or VCC	5.5 V			0.9				,	mA
Ci	V _I = V _{CC} or GND	5 V		4.5						pF
Co	VO = VCC or GND	5 V		12						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, VCC = 5 V ± 0.5 V

			TA =	T _A = 25°C		54ACT16374		74ACT16374	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency		0	65	0	₄ 65	0	65	MHz
	D.L. J. P.	CLK low	7.5		7.5	50.00	7.5		
τ _W	Pulse duration	CLK high	4.5		4,5	.<:	4.5		ns
t _{su}	Setup time, data before C↑		6.5		€.5	~	6.5		ns
th	Hold time, data before C↑		1	-	₹1		1		ns

switching characteristics over recommended operating free-air temperature range, VCC = 5 V ± 0.5 V

DADAUETED	FROM	FROM TO		T _A = 25°C		54ACT16374		74ACT16374		
PARAMETER	(INPUT) (OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
fmax			65			65		65		MHz
tPLH .	OLK.	_	5.1	8.8	10.9	5.1	13.2	5.1	12.4	
tPHL	CLK	Q	5.3	8.8	10.9	5.3	S-13,1	5.3	12.2	ns
tPZH	ŌĒ	0	3.7	8.4	10.5	3.7	12.7	3.7	11.9	
tPZL	OE	Q	4.4	9.7	11.9	4,4	14.3	4.4	13.4	ns
tPHZ	ŌĒ	_	5.4	7.9	9.8	5.4	10.9	5.4	10.4	
tPLZ	OE	Q	4.9	7.2	9.1	4.9	10.2	4.9	9.8	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
	0	Outputs enabled	C: - F0 oF 4 - 1 MH-	52	pF
1	Cpd Power dissipation capacitance per flip-flop	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	38	рг

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[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

54AC16470, 54ACT16470 74AC16470, 74ACT16470

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS T10246—D3569, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16470 and 'ACT16470 are noninverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (10EAB or 20EAB), direction enable (1DEAB or 2DEAB), and clock (1CLKAB or 2CLKAB) inputs.

54AC16470, 54ACT16470 ... WD PACKAGE 74AC16470, 74ACT16470 ... DL PACKAGE (TOP VIEW)

10EAB	ı U	56	10EBA
1CLKAB	2	55	1CLKBA
1 DEAB	3	54	1 DEBA
GND [4	53	GND
1A1	5	52]1B1
1A2 [6	51	1B2
V _{CC} [7	50]∨ _{cc}
1A3 [8	49	1B3
1A4	9	48]1B4
1A5 [10	47	1B5
GND [11	46	GND
1A6	12	45]1B6
1A7 [13	44] 1B7
1A8 [14	43] 1B8
2A1[15	42	2B1
2A2 [16	41	2B2
2A3 [17	40	2B3
GND [18	39	GND
2A4 [19	38	_ 2B4
2A5 [20	37	2B5
2A6 [21	36	2B6
V _{cc} [22	35]∨ _{cc}
2A7 [23	34	2B7
2A8 [24	33] 2B8
GND [25	32	GND
2DEAB	26	31	2DEBA
2CLKAB	27	30] 2CLKBA
20EAB	28	29	20EBA

When 1DEAB (or 2DEAB) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1DEAB (or 2DEAB) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1OEAB (or 2OEAB). A low level on 1CLKAB (or 2CLKAB) inhibits register loading; a low-to-high transition on 1CLKAB (or 2CLKAB) causes loading of the corresponding registers with the current A-bus data. If 1OEAB (or 2OEAB) is low, the corresponding B outputs reflect the contents of the registers. A high level on 1OEAB (or 2OEAB) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION†

	INPUTS		LATOURATA	D OUTDUTO	
DEAB	CLKAB	OEAB	LATCH DATA	B OUTPUTS	
Н	Х	Х	Previous A Data	Z	
L	L	Н	Previous A Data	Z	
L	L	L	Previous A Data	Previous A Data	
L	1	Н	Current A Data	Z	
L	1	L	Current A Data	Current A Data	

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by DEBA, CLKBA, and OEBA.

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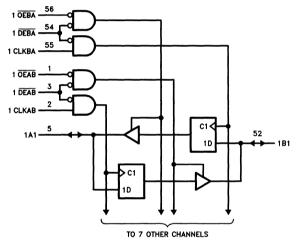
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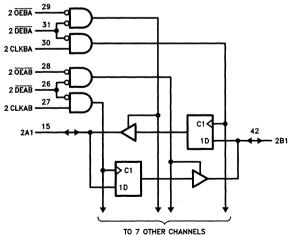
Data flow from B to A is similar, but uses 1OEBA and/or 2OEBA
The 74AC16470 and 74ACT16470 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16470 has CMOS-compatible input thresholds. The 'ACT16470 has TTL-compatible input thresholds.

The 54AC16470 and 54ACT16470 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16470 and 74ACT16470 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





54AC16471, 54ACT16471 74AC16471, 74ACT16471

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0247--- D3570, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16471 and 'ACT16471 are inverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (10EAB or 20EAB), direction-enable (1DEAB or 2DEAB), and clock (1CLKAB or 2CLKAB) inputs.

54AC16471, 54ACT16471 ... WD PACKAGE 74AC16471, 74ACT16471 ... DL PACKAGE (TOP VIEW)

1 OEAB	1	J 56	1 OEBA
1CLKAB	2	55]1CLKBA
1 DEAB	3	54	1 DEBA
GND [4	53	GND
1A1 🗌	5	52]1B1
1A2 🗌	6	51]1B2
V _{cc} □	7	50	∃v _{cc}
1A3 [8	49]1B3
1A4	9	48]1B4
1A5 [10	47] 1B5
GND [11	46	GND
1A6 [12	45]1B6
1A7 🗌	13	44] 187
1A8 [14	43] 1B8
2A1 🗌	15	42	2B1
2A2 🗌	16	41	2B2
2A3 🗌	17	40	□ 2B3
GND [18	39	GND
2A4 🗌	19	38	2B4
2A5 [20	37	2B5
2A6 🗌	21	36] 2B6
V _{cc} □	22	35	□ v _{cc}
2A7	23	34	2B7
2A8 [24	33	2B8
GND [25	32	GND
2DEAB	26	31	2DEBA
2CLKAB	27	30] 2CLKBA
20EAB	28	29	20EBA

When 1DEAB (or 2DEAB) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1DEAB (or 2DEAB) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1DEAB (or 2DEAB). A low level on 1CLKAB (or 2CLKAB) inhibits loading of the registers with the current A-bus data; a low-to-high transition on 1CLKAB (or 2CLKAB) causes the corresponding registers to be loaded with the current A-bus data. If 1DEAB (or 2DEAB) is low, the corresponding B outputs reflect the inverse of the register contents. A high level on 1DEAB (or 2DEAB) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION[†]

INPUTS			D OUTDUTS	
DEAB	CLKAB	OEAB	LATCH DATA	B OUTPUTS
Н	X	X	Previous A Data	Z
L	L	Н	Previous A Data	Z
L	L	L	Previous A Data	Inverse of Previous A Data
L	1	Н	Current A Data	Z
L	<u> </u>	L	Current A Data	Inverse of Current A Data

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by DEBA, CLKBA, and OEBA.

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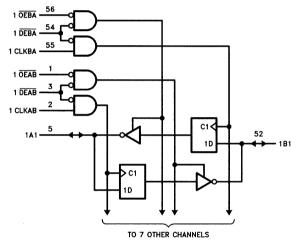
Data flow from B to A is similar, but uses 1OEBA and/or 2OEBA, 1DEBA and/or 2DEBA, and 1CLKBA and/or 2CLKBA.

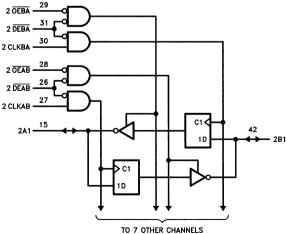
The 74AC16471 and 74ACT16471 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16471 has CMOS-compatible input thresholds. The 'ACT16471 has TTL-compatible input thresholds.

The 54AC16471 and 54ACT16471 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16471 and 74ACT16471 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





54AC16472, 54ACT16472 74AC16472, 74ACT16472 18-BIT LATCHED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0248-D3571, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Package (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16472 and 'ACT16472 are noninverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (10EAB or 20EAB) and latch enable (1LEAB or 2LEAB) inputs. When 10EAB (or 20EAB) is low, the corresponding B outputs are active (high or low logic levels). When 10EAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when 1LEAB (or 2LEAB) is high and reflect the states of the corresponding A inputs when 1LEAB (or 2LEAB) is low.

FUNCTION TABLE, EACH SECTION[†]

INPUTS			
LEAB	OEAB	LATCH DATA	B OUTPUTS
L	L	Current A Data	Current A Data
Н	L	Previous A Data	Previous A Data
L	Н	Current A Data	Z
Н	Н	Previous A Data	Z

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by OEBA and LEBA.

54AC16472, 54ACT16472 ... WD PACKAGE 74AC16472, 74ACT16472 ... DL PACKAGE (TOP VIEW)

		_	L
10EAB	l1 \(\)	56	10EBA
1 LEAB	2	55	1 LEBA
1A1	3	54	□1B1
GND [4	53	GND
1A2	5	52	□1B2
1A3	6	51	1B3
V _{CC}	7	50	Бν _{сс}
1A4 [8	49	1B4
1A5	9	48	T1B5
1A6	10	47	П _{1В6}
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	11B8
1A9 [14	43	1B9
2A1	15	42	F _{2B1}
2A2	16	41	52B2
2A3	17	40	
GND	18	39	E
2A4 [19	38	E
2A5	20	37	E ·
2A6	21	36	Б _{2В6}
V _{CC}	22	35	5vcc
2A7 [23	34	
2A8 [24	33	E
GND [25	32	E
2A9 [26	31	E
	27		=
2LEAB	i	30	
20EAB	28	29	20EBA

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TI0248-D3571, JUNE 1990

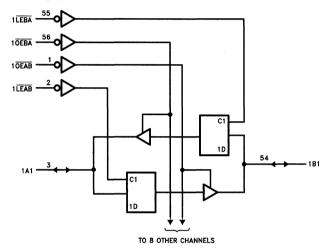
Data flow from B to A is similar, but uses 1OEBA and/or 2OEBA and 1LEBA and/or 2LEBA.

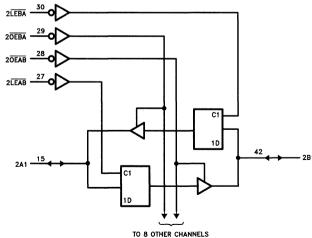
The 74AC16472 and 74ACT16472 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16472 has CMOS-compatible input thresholds. The 'ACT16472 has TTL-compatible input thresholds.

The 54AC16472 and 54ACT16472 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16472 and 74ACT16472 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)







- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil **Center-to-Center Pin Spacings**
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16473 and 'ACT16473 are inverting 18-bit latched bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (1OEAB or 2OEAB) and latch enable (1LEAB or 2LEAB) inputs. When 1OEAB (or 2OEAB) is low, the corresponding B outputs are active (high or low logic levels). When 1OEAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. The latches retain their prior states when 1LEAB (or 2LEAB) is high and reflect the states of the corresponding A inputs when 1LEAB (or 2LEAB) is low.

FUNCTION TABLE, EACH SECTION[†]

IN	INPUTS LATCH DATA		B OUTPUTS
LEAB	OEAB	LAICHDAIA	BOUIPUIS
L	L	Current A Data	Inverse of Current A Data
Н	L	Previous A Data	Inverse of Previous A Data
L	Н	Current A Data	Z
Н	Н	Previous A Data	Z

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by OEBA and LEBA.

54AC16473, 54ACT16473 ... WD PACKAGE 74AC16473, 74ACT16473 ... DL PACKAGE (TOP VIEW)

1 OEAB	ıυ	56	10EBA
1 LEAB	2	55	1 LEBA
1A1	3	54]1B1
GND [4	53	GND
1A2	5	52]1B2
1A3 [6	51] 1B3
V _{CC} [7	50	$\exists v_{cc}$
1A4	8	49] 1B4
1A5 [9	48] 1B5
1A6 [10	47]1B6
GND [11	46	GND
1A7 [12	45] 1B7
1A8 [13	44]1B8
1A9 [14	43] 1B9
2A1	15	42] 2B1
2A2	16	41] 2B2
2A3 [17	40	_ 2B3
GND [18	39	GND
2A4 [19	38	☐ 2B4
2A5 [20	37	_ 2B5
2A6 [21	36] 2B6
V _{cc} [22	35	□ V _{CC}
2A7 [23	34	_ 2B7
2A8 [24	33	2B8
GND [25	32	GND
2A9 [26	31] 2B9
2LEAB	27	30	2LEBA
20EAB	28	29	20EBA

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PRODUCT PREVIEW

TI0249--- D3572, JUNE 1990

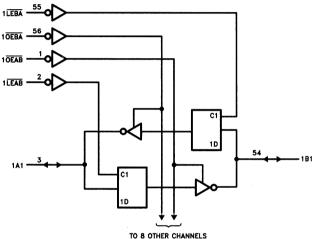
Data flow from B to A is similar, but uses 10EBA and/or 20EBA and 1LEBA and/or 2LEBA.

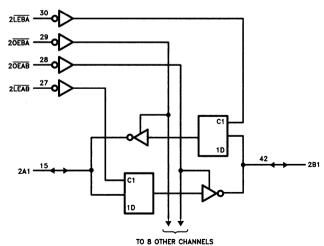
The 74AC16473 and 74ACT16473 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16473 has CMOS-compatible input thresholds. The 'ACT16473 has TTL-compatible input thresholds.

The 54AC16473 and 54ACT16473 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16473 and 74ACT16473 are characterized for operation from -40°C to 85°C.

logic diagram (positive logic)







PRODUCT PREVIEW

3-54

54AC16474, 54ACT16474 74AC16474, 74ACT16474

18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0250--- D3573, JUNE 1990

•	Members	of	Texas	Instruments	Widebus™
	Family				

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration
 Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16474 and 'ACT16474 are noninverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (1ŌEAB or 2ŌEAB) and clock (1CLKAB or 2CLKAB) inputs. When 1ŌEAB (or 2ŌEAB) is low, the corresponding B outputs are active (high or low logic levels) and take on either the current A-bus data on a low-to-high transition of 1CLKAB (or 2CLKAB) or the previously stored A-bus data if 1CLKAB (or 2CLKAB) is low.

54AC16474, 54ACT16474 ... WD PACKAGE 74AC16474, 74ACT16474 ... DL PACKAGE (TOP VIEW)

10EAB	1	U	56		10EBA
CLKAB [2		55	П	1CLKBA
1A1	3		54		1B1
GND [4		53		GND
1A2 [5		52		1B2
1A3 [6		51		1B3
V _{CC}	7		50		v _{cc}
1A4 [8		49	₽	1B4
1A5 [9		48		1B5
1A6 [10		47		1B6
GND [11		46		GND
1A7 [12		45		187
1A8 [13		44		1B8
1A9 [14		43		1B9
2A1	15		42		2B1
2A2 🗌	16		41		2B2
2A3 🗌]17		40		2B3
GND [18		39	П	GND
2A4 [19		38	р	2B4
2A5 [20		37	р	2B5
2A6 [21		36	П	2B6
V _{CC}]22		35		V _{CC}
2A7 [23		34	р	2B7
2A8 [24		33	П	2B8
GND [25		32	П	GND
2A9 [26		31	ш	2B9
2CLKAB	27		30	Ц	2CLKBA
20EAB	28		29	μ	20EBA

When 1OEAB (or 2OEAB) is high, the corresponding B outputs are in the high-impedance state. 1OEAB (or 2OEAB) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses 10EBA and/or 20EBA and 1CLKBA and/or 2CLKBA.

FUNCTION TABLE, EACH SECTION[†]

INPUTS CLKAB OEAB		PUTS		
		LATCH DATA	B OUTPUTS	
L	L	Previous A Data	Previous A Data	
L	Н	Previous A Data	Z	
1	L	Current A Data	Current A Data	
1	Н	Current A Data	Z	

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by CLKBA and OEBA.

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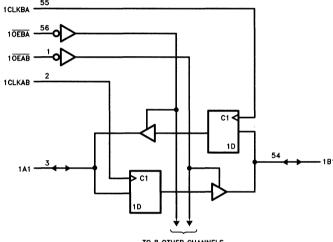
TI0250-D3573, JUNE 1990

The 74AC16474 and 74ACT16474 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

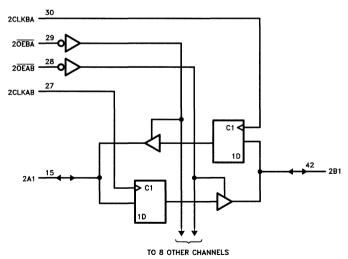
The 'AC16474 has CMOS-compatible input thresholds. The 'ACT16474 has TTL-compatible input thresholds.

The 54AC16474 and 54ACT16474 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16474 and 74ACT16474 are characterized for operation from -40°C to 85°C.

logic diagram (positive logic)



TO 8 OTHER CHANNELS



54AC16475, 54ACT16475 74AC16475, 74ACT16475

18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS T10251—D3674, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16475 and 'ACT16475 are inverting 18-bit registered bus transceivers composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable (10EAB or 20EAB) and clock (1CLKAB or 2CLKAB) inputs. When 10EAB (or 20EAB) is low, the corresponding B outputs are active (high or low logic levels) and take on either the inverse of the current A-bus data on a low-to-high transition of 1CLKAB (or 2CLKAB) or the inverse of the previously stored A-bus data if 1CLKAB (or 2CLKAB) is low.

54AC16475, 54ACT16475 ... WD PACKAGE 74AC16475, 74ACT16475 ... DL PACKAGE (TOP VIEW)

1 OEAB	10	56 10EBA
1 CLKAB	2	55 1CLKBA
1A1	3	54 🗌 1B1
GND [4	53 GND
1A2 [5	52 1B2
1A3 [6	51 1 B3
v _{cc} [7	50 □ V _{CC}
1A4 [8	49 🗌 1 B.4
1A5 🗌	9	48 🗌 1 B5
1A6 [10	47 🗌 1B6
GND [11	46 🗌 GND
1A7 [12	45 🗌 1 B 7
1A8 [13	44 🗌 1B8
1A9 [14	43 🗌 1B9
2A1[15	42 2B1
2A2	16	41 🗌 2B2
2A3	17	40 🗌 2B3
GND [18	39 GND
2A4 [19	38 🗌 2B4
2A5 🗌	20	37 🗌 2B5
2A6	21	36 🗌 2B6
V _{CC}	22	35 V _{CC}
2A7 [23	34 🗌 2B7
2A8 [24	33 2B8
GND [25	32 GND
2A9 [26	31 2B9
2CLKAB	27	30 2CLKBA
20EAB	28	29 20EBA

When 1OEAB (or 2OEAB) is high, the corresponding B outputs are in the high-impedance state. 1OEAB (or 2OEAB) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION[†]

INPL	INPUTS LATOURATA		D OUTDUTS
CLKAB	OEAB	LATCH DATA	B OUTPUTS
L	L	Previous A Data	Inverse of Previous A Data
L	Н	Previous A Data	Z
1	L	Current A Data	Inverse of Current A Data
1	Н	Current A Data	Z

[†] A-to-B data flow is shown. B-to-A data flow is controlled analogously by CLKBA and OEBA.

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18-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0251-D3574, JUNE 1990

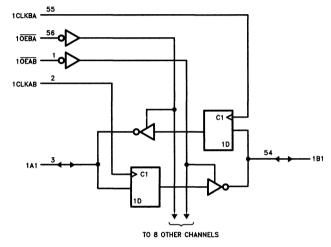
Data flow from B to A is similar, but uses 10EBA and/or 20EBA and 1CLKBA and/or 2CLKBA.

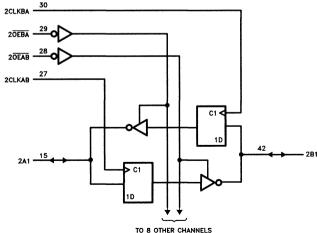
The 74AC16475 and 74ACT16475 are packaged in Tl's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16475 has CMOS-compatible input thresholds. The 'ACT16475 has TTL-compatible input thresholds.

The 54AC16475 and 54ACT16475 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16475 and 74ACT16475 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





54AC16543, 74AC16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0196-D3475, MARCH 1990

 Members of the Texas Instruments Widebus™ Family 	54AC16543 WD PACKAGE 74AC16543 DL PACKAGE
Packaged in Shrink Small Outline 300-mil	(TOP VIEW)
Packages (SSOP) and 380-mil Fine-Pitch	1GAB 1 1 56 1 1GBA
Ceramic Flat Packages Using 25-mil	1LEAB 2 55 1LEBA
Center-to-Center Pin Spacings	1CEAB 3 54 1CEBA
3-State True Outputs	GND 4 53 GND
Flow-Through Architecture to Optimize PCB	1A1 0 5 52 0 1B1
Layout	1A2 6 51 1B2
Distributed Vocand CND Dis Configuration	V _{CC} 7 50 V _{CC}
 Distributed VCC and GND Pin Configuration to Minimize High-Speed Switching Noise 	1A4 9 48 11B4
	1A5 10 47 1B5
■ EPIC™ (Enhanced-Performance Implanted ■ CMOS) 4	GND 11 46 GND
CMOS) 1-μm Process	1A6 12 45 1B6
● 500-mA Typical Latch-Up Immunity at 125°C	1A7 🚺 13 44 🗓 1B7
	1A8 🚺 14 43 🗍 1B8
description	2A1 🛛 15 42 🗍 2B1
The 'AC16543 is a 16-bit registered transceiver	2A2 🛛 16 41 🖺 2B2
and contains two sets of D-type latches for	2A3 🛛 17 40 🖟 2B3
temporary storage of data flowing in either	GND 18 39 GND
direction. The 'AC16543 can be used as two	2A4] 19 38] 2B4
8-bit transceivers or one 16-bit transceiver.	2A5 20 37 2B5
Separate Latch Enable (LEAB or LEBA) and Output Enable (GAB or GBA) inputs are	2A6
provided for each register to permit	V _{CC}
independent control in either direction of data	2A8 24 33 2B8
flow.	GND 1 25 32 1 GND
The A-to-B Enable (CEAB) input must be low in	2CEAB 26 31 2CEBA
order to enter data from A or to output data to	2LEAB 27 30 2LEBA
B. Having (CEAB) low and (LEAB) low makes	2GAB [] 28 29 [] 2GBA
the A-to-B latches transparent; a subsequent	

low-to-high transition (LEAB) puts the A latches in the storage mode. Data flow from B-to-A is similar, but requires using the (CEBA), (LEBA), and (GBA) inputs.

The 74AC16543 is packaged in Tl's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16543 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16543 is characterized for operation from -40° C to 85°C.

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FUNCTION TABLE (each octal register)

	INPUTS		LATCH STATUS	OUTPUT BUFFERS
CEAB	LEAB	GAB	A TO B†	B1 THRU B8
Н	Х	Х	Storing	High Z
x	Н		Storing	
X		Н	ł	High Z
L	L	L	Transparent	Current A Data
L	Н	L	Storing	Previous‡ A Data

[†] A-to-B data flow is shown: B-to-A flow control is the same except uses CEBA, LEBA, and GBA.

logic diagram (positive logic)

logic symbol§

1GBA 56 1GBA 1 EN3 1CEBA 1CEBA G1 55 1LEBA 1 C5 1LEBA 55 1GAB 2 EN4 1CEAB 3 G2 1GAB-1LEAB 2 C6 2GBA 7 EN9 31 2CEBA G7 30 1LEAB 2LEBA C1 7 C11 1A1 28 1D 2GAB 8 EN10 26 2CEAB G8 27 2LEAB 8 C12 **⊽3** 5D 181 6D 4▽ TO 7 OTHER CHANNELS 51 1**B**2 1A2 49 1**B**3 43 9 1**B**4 2GBA 29 10 47 185 12 2CEBA 31 186 44 13 1B7 1A7 2LEBA 30 43 14 1A8 1B8 42 15 2GAB 28 2B1 11D PRODUCT PREVIEW

2CEAB 26

2LEAB 27

2A1

15

2B2

2B3

2B4

2B5

2B6

2B7 33 2B8

40

38

37

§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

12D

2A2

2A3-

17

19

23

10 ▽



C1

1D

TO 7 OTHER CHANNELS

[‡] Data present before low-to-high transition of LEAB

54AC16543, 74AC16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3475, MARCH 1990-TI0196

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _K (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	54AC16543			74AC16543		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
	-	V _{CC} = 3 V	2.1			2.1			
ViΗ	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		$V_{CC} = 5.5 V$	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
٧ı	Input voltage		0		VCC	0		VCC	٧
Vo	Output voltage		0		Vcc	0		Vcc	٧
		VCC = 3 V			-4			-4	mA
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			-24	
	•	$V_{CC} = 5.5 V$			-24			-24	
		V _{CC} = 3 V			12			12	
lOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
		$V_{CC} = 5.5 V$			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	. 0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEGT CONDITIONS		TA	= 25°0	C	54AC16543		74AC16543		UNIT
		TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			3 V	2.9			2.9		2.9		
		$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4		1
		5.5 V	5.4			5.4		5.4			
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		IOH = -4 mA	3 V	2.58			2.4		2.48		v
VOH		1 04 mA	4.5 V	3.94			3.7		3.8		٧
	IOH = -24 mA	5.5 V	4.94			4.7		4.8			
		IOH = -50 mA†	5.5 V				3.85				ĺ
		$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
		I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
\		IOL = 12 mA	3 V			0.36		0.5		0.44	v
VOL			4.5 V			0.36		0.5		0.44	, v
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA†	5.5 V					1.65			
1		IOL = 75 mA†	5.5 V							1.65	
l ₁	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
Ci	Control inputs	VI = VCC or GND	5 V		4.5						pF
Cio	A or B ports	V _O = V _{CC} or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

54ACT16543, 74ACT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0194-D3476, MARCH 1990

Members of the Texas Instruments Widebus™ Family	54ACT16543 WD PACKA 74ACT16543 DL PACKA	
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	(TOP VIEW) 1GAB [1 56] 1GB. 1LEAB [2 55] 1LE	BA
Inputs are TTL-Voltage Compatible	1CEAB [] 3 54] 1CE GND [] 4 53] GND	
3-State True Outputs	1A1 0 5 52 1B1 1A2 0 6 51 1B2	
Flow-Through Architecture to Optimize PCB Layout	V _{CC} 7 50 V _{CC} 1A3 8 49 183	
Distributed V _{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise	1A4 [] 9 48 [] 1B4 1A5 [] 10 47 [] 1B5 GND [] 11 46 [] GND	
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	1A6 12 45 1B6 1A7 13 44 1B7	
500-mA Typical Latch-Up Immunity at 125°C	1A8 0 14 43 0 1B8 2A1 0 15 42 0 2B1	
description	2A2 [] 16 41 [] 2B2 2A3 [] 17 40 [] 2B3	
The 'ACT16543 is a 16-bit registered	GND 18 39 GND 2A4 19 38 2B4	
transceiver and contains two sets of D-type latches for temporary storage of data flowing in	2A5 🗍 20 37 🗓 2B5	
either direction. The 'ACT16543 can be used as two 8-bit transceivers or one 16-bit	2A6 [] 21 36 [] 2B6 V _{CC} [] 22 35 [] V _{CC}	
transceiver. Separate latch enable (LEAB or	2A7 [] 23 34 [] 2B7	
LEBA) and output enable (GAB or GBA) inputs are provided for each register to permit	2A8 [] 24 33 [] 2B8 GND [] 25 32 [] GND	
independent control in either direction of data	2CEAB 26 31 2CE 2LEAB 27 30 2LE	BA
flow.	2GAB 27 30 2LEI 2GAB 28 29 2GB	

The A-to-B Enable (CEAB) input must be low in order to enter data from A or to output data

to B. Having CEAB low and LEAB low makes the A-to-B latches transparent; a subsequent low-to-high transition (LEAB) puts the A latches in the storage mode. Data flow from B-to-A is similar, but requires using the CEBA, LEBA, and GBA inputs.

The 74ACT16543 is packaged in Tl's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54ACT16543 is characterized over the full military temperature range of -55° C to 125°C. The 74ACT16543 is characterized for operation from -40° C to 85°C.

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TI0194-D3476, MARCH 1990

Function Table (each octal register)

	INPUTS		LATCH STATUȘ	OUTPUT BUFFERS B1 THRU B8
CEAB	LEAB	GAB	A TO B†	D1111110 D0
Н	Х	Х	Storing	Z
Х	Н	Х	Storing	
Х	Х	Н		Z
L	L	L	Transparent	Current A Data
L	Н	L	Storing	Previous‡ A Data

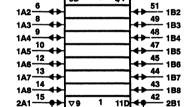
[†] A-to-B data flow is shown: B-to-A flow control is the same except it uses CEBA, LEBA, and GBA.

logic symbol§

1GBA

1CEBA G1 55 1LEBA-1 C5 1GAB 2 EN4 1CEAB 3 G2 ILEAB 2 C6 29 2GBA 7 EN9 31 2CEBA **G7** 2LEBA 7 C11 28 2GAB 8 EN10 26 2CEAB G8 2LEAB 8 C12

1 EN3



12D

16

17

19

20

21

23

52

41 2B2

37 2B5

34 2B7

2B3

2B4

2B6

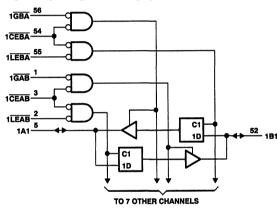
1B1

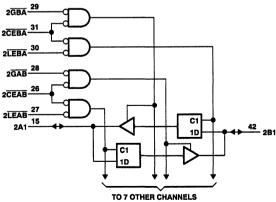
5D

This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

10 ▽

logic diagram (positive logic)







[‡] Data present before low-to-high transition of LEAB occurring while CEAB is low.

54ACT16543, 74ACT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3476, MARCH 1990-TI0194

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	±400 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54ACT16543			74ACT16543			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2		1.69	2			٧
VIL	Low-level input voltage			0.8			0.8	٧
VI	Input voltage	0	o?	VCC	0		Vcc	V
Vo	Output voltage	0	7	Vcc	0		Vcc	V
ЮН	High-level output current	-	2,0	-24			-24	mA
lOL	Low-level output current	20"		24			24	mA
Δt/Δν	Input transition rise or fall rate	₹ 0		10	0		10	ns/V
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

TI0194-D3476, MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				T _A	= 25°	С	54AC1	16543	74ACT16543		UNIT	
"	ARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
		I 50 A	4.5 V	4.4			4.4		4.4			
		$IOH = -50 \mu A$	5.5 V	5.4			5.4		5.4			
		24 4	4.5 V	3.94			3.7		3.8			
VOH		IOH = -24 mA	5.5 V	4.94			4.7		4.8		٧	
		$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85	100				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V					161	3.85			
		I 50 A	4.5 V			0.1		0.1		0.1		
		IOL = 50 μA	5.5 V			0.1		0.1		0.1	v	
١.,		I _{OL} = 24 mA	4.5 V			0.36	ź	0.5		0.44		
VOL			5.5 V			0.36		0.5		0.44		
		IOL = 50 mA†	5.5 V				_0	1.65				
		IOL = 75 mA†	5.5 V				250			1.65		
11	Control Inputs	V _I = V _{CC} or GND	5.5 V			±0.1	4	± 1		±1	μΑ	
loz	A or B Ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ	
ΔICC [§]		One input at 3.4 V,	5.5 V			0.9		1		1	mΑ	
2.00		Other inputs at GND or VCC	0.5 V			0.5		•				
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5							
Cio	A or B ports	V _I = V _{CC} or GND	5 V		12						pF	

[†] Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (unless otherwise noted) (see Note 3)

		T _A =	25°C	54ACT16543	74ACT16543		UNIT
		MIN	MAX	MIN MAX	MIN	MAX	UNII
tw	Pulse duration, LEAB or LEBA low	7.5		7,5	7.5		ns
tsu	Setup time, data before LEAB or LEBA ↑	2.5		2.5	2.5		ns
th	Hold time, data after LEAB or LEBA ↑	4		4	4		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54ACT16543, 74ACT16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

D3476, MARCH 1990-TI0194

switching characteristics over recommended operating free-air temperature range, VCC = 5 V ± 0.5 V (see Note 4)

DADAMETED	FROM	то	T/	T _A = 25°C			16543	74ACT		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .	A D	or B A or B	3.5	6.9	9.5	3.5	11.3	3.5	10.5	ns
tPHL	AOFB		3.1	7.3	10.7	3.1	13.1	3.1	11.6	
^t PLH	LEAB or LEBA	4 5	3.9	8.6	12.3	3.9	15.1	3.9	13.8	
tPHL	LEAB OF LEBA	A or B	3.9	8.7	12.2	3.9	14.6	3.9	13.5	ns
^t PZH	GAB or GBA	A or B	2.6	7.1	10.3	2.6	12.6	2.6	11.4	ns
tPZL	GAB OF GBA		3.5	8.3	11.9	3,5	14.4	3.5	13.2	
tPHZ	GAB or GBA		4.1	8.2	10.5	₹4,1 <	11.3	4.1	11.1	T
tPLZ	GAB OF GBA	A or B	5	7.3	9.3	₹5	10.4	5	9.6	ns
tPZH	OFFI OFFI	4 5	3.1	7.3	10.7	3.1	12.9	3.1	11.7	
tPZL	CEAB or CEBA	A or B	3.9	8.5	12.2	3.9	14.8	3.9	13.5	ns
tPHZ	OEAD OEDA	A D	4.6	8.5	11	4.6	11.9	4.6	11.6	
tPLZ	CEAB OF CEBA	CEAB or CEBA A or B	5.2	7.4	9.7	5.2	10.8	5.2	10.5	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd} F	Down discination consistence not transcribe.	Outputs enabled	C: - 50 - 5 4 - 1 MH-	45	ρF
	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	12	pr-

54AC16620, 74AC16620 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0289-D3600, JULY 1990-REVISE OCTOBER 1990

Members of the Texas Instruments Widebus™ Family	54AC16620 WD PACKAGE 74AC16620 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1GAB 1 48 1 GBA 1B1 2 47 1A1 1B2 3 46 1A2
3-State Outputs Drive Bus Lines Directly	GND
• Flow-Through Architecture Optimizes PCB Layout	1B4
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1B5
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	1B7
● 500-mA Typical Latch-Up Immunity at 125°C	2B1
escription	GND 15 34 GND
The 'AC16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.	2B3
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the complementary enable inputs (1\overline{G}BA, 1\overline{G}AB, 2\overline{G}BA, and 2\overline{G}AB). The enable inputs can be used to	2B7

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of 1GBA and 1GAB (and/or 2GBA and 2GAB). Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74AC16620 is packaged in TI's shrink small-outline packages (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16620 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16620 is characterized for operation from -40° C to 85°C.

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disable the device so that the buses are



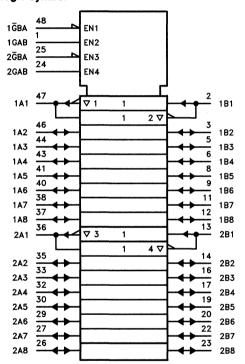
effectively isolated.

D3600, JULY 1990-REVISE OCTOBER 1990-TI0289

FUNCTION TABLE, EACH SECTION

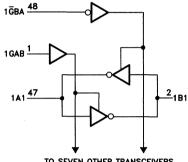
	BLE UTS	OPERATION
GBA	GAB	}
L	L	B data to A bus
н	н	Ā data to B bus
н	L	Isolation
		B data to A bus,
L	н	Ā data to B bus

logic symbol†

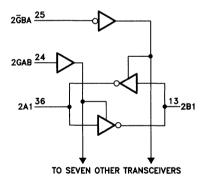


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS



54AC16620, 74AC16620 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0289-D3600, JULY 1990-REVISE OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage range, V _I (see Note 1) – 0.5 V	to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1) 0.5 V	to VCC + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	- 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1662	90	74	AC1662	0	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
		$\Lambda^{CC} = 3 \Lambda$	2.1			2.1			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V
		$V_{CC} = 5.5 V$	3.85			3.85			
		VCC = 3 V			0.9			0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	٧
		$V_{CC} = 5.5 V$			1.65			1.65	
VI	Input voltage		0	(A	VCC	0		VCC	V
VO	Output voltage		0	1	VCC	0		VCC	٧
		$V_{CC} = 3 V$		13	- 4			- 4	
ЮН	High-level output current	$V_{CC} = 4.5 V$	1 0°C.		-24			-24	mΑ
		$V_{CC} = 5.5 V$	₹.		-24			-24	
		VCC = 3 V			12			12	
lOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
		$V_{CC} = 5.5 V$			24			24	
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

D3600, JULY 1990-REVISE OCTOBER 1990-TI0289

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLETIONS		TA	= 25°C		54AC	16620	74AC16620			
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP M	AX	MIN	MAX	MIN	MAX	UNIT	
		3 V	2.9			2.9		2.9			
ĺ	$IOH = -50 \mu A$	4.5 V	4.4			4.4		4.4			
		5.5 V	5.4			5.4		5.4			
Va	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.4		2.48		v	
VOH	Jan 24 - 4	4.5 V	3.94			3.7		3.8		٧	
ł	IOH = -24 mA	5.5 V	4.94			4.7		4.8			
	$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
	$IOH = -75 \text{ mA}^{\dagger}$	5.5 V					4	3.85			
		3 V			0.1		√ 0.1		0.1		
Į.	IOL = 50 μA	4.5 V		-	0.1	-05	√0.1		0.1		
1		5.5 V			0.1	850K	0.1		0.1		
\ \v	IOL = 12 mA	3 V		C	.36	6.4	0.5		0.44	v	
VOL	Jan - 04 mA	4.5 V		C	0.36		0.5		0.44	\ \ \	
	IOL = 24 mA	5.5 V		C	0.36		0.5		0.44		
	IOL = 50 mA [†]	5.5 V					1.65				
	IOL = 75 mA†	5.5 V							1.65		
I Control inp	uts V _I = V _{CC} or GND	5.5 V		±	0.1		±1		±1	μΑ	
IOZ A or B port	s‡ V _I = V _{CC} or GND	5.5 V		±	0.5		±10		±5	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ	
C _i Control inp	uts V _I = V _{CC} or GND	5 V		4.5						pF	
Cio A or B port	s V _I = V _{CC} or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, VCC = 3.3 V \pm 0.3 V (see Note 3)

PARAMETER	FROM	то	T _A = 25°C			54AC	16620	74AC16620		11117
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH	A or B	B or A	2.7	6.1	8.7	2.7	10.3	2.7	9.7	
tPHL	AOrb		3.9	7.9	10.6	3.9	12.3	3.9	11.7	ns
tPZH	ĞВА	A	3.2	7.1	10	3.2	11.8	3.2	11.2	
tPZL	GDA		4.5	11.1	13.5	4.5	15.8	4.5	15	ns
tPHZ	ĞВА	A	5.3	7.4	9.5	5.3	10.6	5.3	10.2	ns
tPLZ	GDA		4.6	7	9.2	4.6	10.1	4.6	9.8	
tPZH	GAB	В	3.1	6.7	9.5	3.1	11.3	3.1	10.7	
tPZL	GAB	В	4.4	9.6	13	4.4	15.2	4.4	14.5	ns
tPHZ	GAB	В	5	7.1	9.3	5	10.1	5	9.8	no
tPLZ	GAB		4.4	6.8	8.9	4.4	9.7	4.4	9.4	9.4 ns

NOTE 3: For load circuit and voltage waveforms, see Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

54AC16620, 74AC16620 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Ti0289-D3600, JULY 1990-REVISE OCTOBER 1990

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (see Note 3)

DADAMETED	FROM	TO	TA	T _A = 25°C			16620	74AC16620		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
[‡] PLH	A D	54	2.1	3.9	6.1	2.1	7.2	2.1	6.8	ns
tPHL	A or B	B or A	3.1	4.9	7.3	3.1	8.7	3.1	8.2	
^t PZH	- GBA		2.2	4.3	6.8	2.2	8	2.2	7.6	
tPZL	1 GBA	A	3.3	5.5	8.4	3.3	9.9	3.3	9.4	ns
tPHZ	GBA		4.9	6.6	8.6	4.9	9.5	4.9	9.2	ne l
tPLZ	GDA	A	4.1	5.8	7.8	4.1	€8.6	4.1	8.3	
tPZH	CAR		2.2	4.2	6.5	2.2	7.7	2.2	7.3	
^t PZL	GAB	В	3.4	5.4	8.1	3.4	9.6	3.4	9.1	ns
t _{PHZ}	CAR	ь.	4.6	6.4	8.5	4.6	9.4	4.6	9	
†PLZ	GAB	В	4.1	5.6	7.6	4.1	8.3	4.1	8	ns

NOTE 3: For load circuit and voltage waveforms, see Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS					
	Daniel discipation and situation and transfer	Outputs enabled	O: - 50 - 5 4 - 4 MII-	49	ρF			
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	6	pr-			

PRODUCT PREVIEW

•	Members of Texas Instruments Widebus™ Family
•	Packaged in Shrink Small-Outline 300-mil
	Packages (SSOP) and 380-mil Fine-Pitch
	Ceramic Flat Packages Using 25-mil Cente
	to-Center Pin Spacings

- Inputs are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ACT16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the complementary enable inputs (1\overline{G}BA, 1GAB, 2\overline{G}BA, and 2GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

54ACT16620 ... WD PACKAGE 74ACT16620 ... DL PACKAGE (TOP VIEW)

1GAB [1	U 48	1 GBA
	‡′.		=
1B1	2	47	1A1
1B2	3	46	□1A2
GND [4	45	GND
1B3 [5	44]1A3
1B4 []6	43	□1A4
V _{cc} []7	42	□vcc
1B5	8	41] 1 A 5
1B6 [9	40	□1A6
GND [10	39	GND
1B7 []11	38	□1A7
1B8 [12	37	1A8
2B1[13	36	2A1
2B2 []14	35	2A2
GND [15	34	GND
2B3 [16	33	2A3
2B4 []17	32	2A4
V _{cc} []18	31	□ v _{cc}
2B5 []19	30	2A5
2B6 []20	29	2A6
GND [121	28	GND
2B7 []22	27	2A7
2B8 [23	26	☐ 2A8
2GAB [24	25	☐ 2GBA

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of 1GBA (or 2GBA) and 1GAB (or 2GAB). Each output reinforces its input in this transceiver configuration. Thus, when both output-enable inputs are active and all other sources to the two sets of bus lines are high impedance, the bus lines remain at their last states.

The 'ACT16620 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54ACT16620 is characterized over the full military temperature range of -55° C to 125°C. The 74ACT16620 is characterized for operation from -40° C to 85°C.

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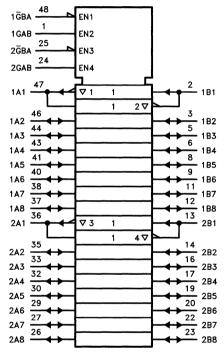
PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas instruments reserves the right to change or discontinue these products without notice.



FUNCTION TABLE,

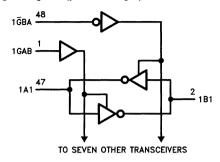
	BLE UTS	OPERATION
GBA	GAB	
L	L	B data to A bus
Н	Н	A data to B bus
Н	L	Bus Isolation
	н	B data to A bus,
-	п	A data to B bus

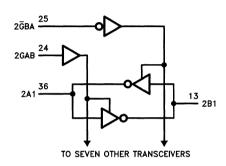
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





PRODUCT PREVIEW

D3584, JUNE 1990-TI0243

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	$-0.5\ V$ to 7 V
Input voltage range, V _I (see Note 1)	VCC + 0.5 V
Output voltage range, VO (see Note 1)0.5 V to	VCC + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pins	± 400 mA
Storage temperature range	·65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54ACT16620		74ACT16620		UNIT
l		MIN	MAX	MIN	MAX	ONH
VCC	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	VCC	0	VCC	٧
Vo	Output voltage	0	VCC	0	VCC	٧
ЮН	High-level output current		-24		-24	mA
lOL	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{3.} All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V	T _A = 25°C			54ACT	16620	74ACT16620		UNIT
			vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
	50. 4	I 50 A	4.5 V	4.4			4.4		4.4		
		IOH = -50 μA	5.5 V	5.4			5.4		5.4	4	
\		IOH = -24 mA	4.5 V	3.94			3.94		3.8		٧
VOH		10H = -24 MA	5.5 V	4.94			4.94		4.8		٧
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
		lo 50 A	4.5 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	v
\		1	4.5 V			0.36		0.5		0.44	
VOL		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA [†]	5.5 V					1.65			
		IOH = 75 mA†	5.5 V							1.65	
1	Control inputs	V _I = V _{CC} or GND	5.5 V			± 0.1		±1		±1	μΑ
loz	A or B ports‡	VO = VCC or GND	5.5 V			± 0.5		±10		±5	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
A1008		One input at 3.4 V,	5.514			0.9				1	m A
ΔICC ₈		Other inputs at GND or VCC	5.5 V			0.9		1		'	mA
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF
Cio	A or B Ports	V _O = V _{CC} or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm~0.5~V$ (unless otherwise noted) (see Note 4)

DADAMETED	FROM	то	T _A = 25°C			54ACT16620		74ACT16620		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	A ou D	B or A								
^t PHL	A or B									ns
tPZH	GBA	Α								
tPZL		^								ns
tPHZ	GBA	A								
t _{PLZ}										ns
^t PZH	GAB	GAB B								ns
^t PZL										115
tPHZ	GAB	В								ns
tPLZ										l lis

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

54ACT16620, 74ACT16620 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3584, JUNE 1990-TI0243

operating characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
	Davies dissination considers and transmission	Outputs enabled	C: - 50 - 5 4 - 4 M l-		
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF, f = 1 MHz		pF

54AC16640, 74AC16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Ti0284-D3607, JULY 1990-REVISED OCTOBER 1990

 Members of the Texas Instruments Widebus™ Family 	54AC16640 WD PACKAGE 74AC16640 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1 DIR 1 48 1 G 1 B1 2 47 1 A1 1 B2 3 46 1 A2
 Flow-Through Architecture Optimize PCB Layout 	GND
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	V _{CC}
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	GND
500-mA Typical Latch-Up Immunity at 125°C	1B8
description	GND ☐ 15 34 ☐ GND
The 'AC16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.	2B3
This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the direction control inputs (1DIR and 2DIR).	2B6

The enable inputs $(1\overline{G} \text{ and } 2\overline{G})$ can be used to disable the device so that the buses are effectively isolated. The 'AC16640 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 54AC16640 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16640 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

	ITROL PUTS	OPERATION
G	DIR	1
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	X	Bus Isolation

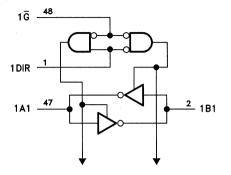
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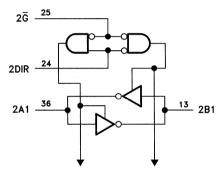
logic symbol† 1G 48 G3 3 EN1 [BA] 3 EN2 [AB] 2G 25 G6 2DIR 24 6 EN4 [BA] 6 EN5 [AB] 2 1B1 ∇1 2 ▽ 3 1B2 1A2 -5 1B3 6 1B4 8_ 1B5 1A5 1A6 40 9 1B6 11 1B7 38 1A7 -37 12__ 1B8 1A8 -13 2B1 ∇4 5 ▽ 35 14 2B2 2A2 -16 2B3 33 2A3 -32 17 2B4 244 -30__ 19 2B5 2A5 -29 20 2A6 2B6 27 22 2B7

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS



TO SEVEN OTHER TRANSCEIVERS

2B8

54AC16640, 74AC16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0284---D3607, JULY 1990---REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}			-0.5	V to 7 V
Input voltage range, V _I (see Note 1)	-0.5	V to	Vcc	+ 0.5 V
Output voltage range, VO (see Note 1)	-0.5	V to	VCC	+ 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)				$\pm20~\text{mA}$
Output clamp current, IOK (VO < 0 or VO > VCC)				$\pm50~\text{mA}$
Continuous output current, IO (VO = 0 to VCC)				$\pm50~\text{mA}$
Continuous current through VCC or GND pins			±	400 mA
Storage temperature range		(65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1664	10	74	AC1664	0	114117
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
		ACC = 3 A	2.1			2.1			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		V _{CC} = 5.5 V	3.85			3.85			
		ACC = 3 A			0.9			0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
VI	Input voltage		0		VCC	0		VCC	٧
Vo	Output voltage	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	0	Case -	VCC	0		VCC	٧
		VCC = 3 V			-4			-4	
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			- 24	mA
		V _{CC} = 5.5 V			-24			-24	
		VCC = 3 V			12			12	
lOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

D3607, JULY 1990-REVISED OCTOBER 1990-TI0284

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COMPLETIONS		TA	= 25°C	2	54AC	16640	74AC	16640	
PAF	HAMEIEH	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	V
			3 V	2.9			2.9		2.9		
		IOH = - 50 μA	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		IOH = -4 mA	3 V	2.58			2.4		2.48		V
VOH		I 044	4.5 V	3.94			3.7		3.8		
		I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		IOH = -50 mA†	5.5 V				3.85				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
			3 V			0.1		0.1		0.1 0.1	
		I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		S 0.1		0.1	
Va.		IOL = 12 mA	3 V			0.36	-0,	₹0.5		0.44	.,
VOL		la: 04 mA	4.5 V			0.36	(C	0.5		0.44	
		I _{OL} = 24 mA	5.5 V			0.36	6,	0.5		0.44	
		IOL = 50 mA [†]	5.5 V					1.65			
		$IOL = 75 \text{ mA}^{\dagger}$	5.5 V							1.65	
-lj	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF
C _{io}	A or B ports	VO = VCC or GND	5 V		16						pF

[†] Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm~0.3~V$ (see Note 3)

PARAMETER	FROM	то	T/	= 25°	С	54AC	16640	74AC1	6640	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
tPLH	A D	D A	2.2	6.9	9.1	2.2	10.7	2.2	10	
tPHL	A or B	B or A	3	8.5	11	3 ,	12.6	3	11.9	ns
tPZH	G	A D	3	8.2	11	(3)	√13.2	3	12.3	
tPZL.	G	A or B	3.9	10.9	14	3.9	16.8	3.9	15.5	ns
tPHZ	G	A or B	5.1	8.3	10.6	5.1	11.7	5.1	11.2	
tPLZ			4.3	7.8	10.1	4.3	11	4.3	10.6	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

54AC16640, 74AC16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0284---D3607, JULY 1990---REVISED OCTOBER 1990

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (see Note 3)

	FROM	то	T/	√ = 25°C		54AC16640 74AC16640		6640		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP M	IAX	MIN	MAX	MIN	MAX	ns ns
tPLH	A D	D A	1.8	4.7		1.8	, î, 8	1.8	7.3	- ns ∣
tPHL	A or B	B or A	2.6	5.7		2.6	9.2	2.6	8.6	
tPZH	G	45	2.4	5.6		2.4	8.5	2.4	8	
tPZL	G	A or B	3	6.6		« 3	10.7	3	9.9	ns
tPHZ		A D	5	7.5		₹5	10.4	5	9.9	
tPLZ	G	A or B	4.1	6.5		4.1	9.3	4.1	9	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
<u> </u>	Device discipation consistence and transcript	Outputs enabled	C: - 50 - 5 f - 1 MH-	55	, .
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	8	pF

54ACT16640, 74ACT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0244-D3585, JUNE 1990

 Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ACT16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the direction control inputs (1DIR and 2DIR). The enable inputs ($1\overline{G}$ and $2\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The 'ACT16640 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

54ACT16640 ... WD PACKAGE 74ACT16640 ... DL PACKAGE (TOP VIEW)

- -

1B1 2 47 1A1 1B2 3 46 1A2 GND 4 45 GND 1B3 5 44 1A3 1B4 6 43 1A4 VCC 7 42 VCC 1B5 8 41 1A5 1B6 9 40 1A6 GND 10 39 GND 1B7 11 38 1A7 1B8 12 37 1A8 2B1 13 36 2A1 2B2 14 35 2A2 GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 VCC 18 31 VCC 2B5 19 30 2A5 CRES 19 30 2A5 CRES 20 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8 2DIR 24 25 2G	1 DIR	1	U	48	∏1Ğ
GND	1B1]2		47]1A1
1B3 5 44 1A3 1B4 6 43 1A4 V _{CC} 7 42 V _{CC} 1B5 8 41 1A5 1B6 9 40 1A6 GND 10 39 GND 1B7 11 38 1A7 1B8 12 37 1A8 2B1 13 36 2A1 2B2 14 35 2A2 GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	1B2 []3		46	1A2
1B4	GND []4		45	GND
V _{CC} 7 42 V _{CC} 185 8 41 1.55 186 9 40 1.66 GND 10 39 GND 187 111 38 1.47 1.88 122 37 1.48 281 13 36 2.41 282 14 35 2.42 GND 15 34 GND 283 16 33 2.44 2.45 17 32 2.44 2.45 19 30 2.45 2.66 20 29 2.46 GND 21 28 GND 21 28 GND 21 28 GND 22 27 2.47 2.47 2.48 2.55 2.55 2.55 2.55 2.55 2.55 2.55 2.5	1B3 [[5		44	□1A3
185 8 41 1A5 186 9 40 1A6 GND 10 39 GND 187 11 38 1A7 188 12 37 1A8 281 13 36 2A1 282 14 35 2A2 GND 15 34 GND 283 16 33 2A3 284 17 32 2A4 VCC 18 31 VCC 285 19 30 2A5 286 20 29 2A6 GND 21 28 GND 287 22 27 2A7 288 23 26 2A8	1B4 []6		43]1A4
1B5	V _{CC}]7		42	□v _{cc}
GND 10 39 GND 187 11 38 1A7 188 12 37 1A8 2B1 13 36 2A1 2B2 14 35 2A2 GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 VCC 18 31 VCC 18 31 VCC 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 21 28 GND 21 28 GND 22 27 2A7 2B8 23 26 2A8		8		41]1A5
1B7 11 38 1A7 1B8 12 37 1A8 2B1 13 36 2A1 2B2 14 35 2A2 GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 VCC 18 31 VCC 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	1B6 [9		40]1A6
1BB 12 37 1AB 2B1 13 36 2A1 2B2 14 35 2A2 37 36 2A1 2B3 16 33 2A3 2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 3A 2B7 22 27 2A7 2B8 23 26 2A8 2	GND [10		39	GND
281 13 36 2A1 282 14 35 2A2 GND 15 34 GND 283 16 33 2A3 284 17 32 2A4 V _{CC} 18 31 V _{CC} 285 19 30 2A5 286 20 29 2A6 GND 21 28 GND 287 22 27 2A7 288 23 26 2A8	1B7 [11		38] 1A7
2B2 14 35 2A2 GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	1B8 [12		37	□1A8
GND 15 34 GND 2B3 16 33 2A3 2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	2B1[13		36] 2A1
2B3 16 33 2A3 2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	2B2	14		35	2A2
2B4 17 32 2A4 V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	GND [15		34	GND
V _{CC} 18 31 V _{CC} 2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	2B3 [16		33	2A3
2B5 19 30 2A5 2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	2B4 [17		32	□ 2A4
2B6 20 29 2A6 GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	V _{CC} [18		31	□Vcc
GND 21 28 GND 2B7 22 27 2A7 2B8 23 26 2A8	2B5 [19		30	2A5
2B7 22 27 2A7 2B8 23 26 2A8	2B6 [20		29	□ 2A6
2B8 23 26 2A8	GND [21		28	GND
	2B7 [22		27	_
2DIR 24 25 2 2 G	2B8 []23		26	
	2DIR [24		25	∏ 2Ğ

The 54ACT16640 is characterized over the full military temperture range of -55° C to 125°C. The 74ACT16640 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

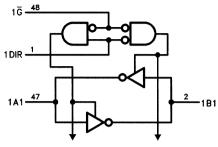
	TROL UTS	OPERATION
G	DIR	1
L	L	B data to A bus
L	Н	Ā data to B bus
Н	Х	Bus Isolation

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

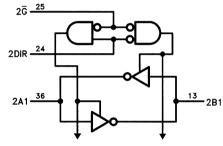
logic symbol† 1G 48 G3 1DIR -3 EN1 [BA] 3 EN2 [AB] 2<u>ē</u> 25 G6 2DIR 24 6 EN4 [BA] 6 EN5 [AB] **V** 1 1 2∇ - 1B3 **-**184 8___1B5 - 1B6 11__1B7 12__1B8 1A8 37 13 2B1 $\nabla 4$ 1 5 ▽ 14 2B2 2A2 35 16 2B3 2A3 33 17_2B4 19 2B5 20 2B6 22 2B7 23 2B8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS



TO SEVEN OTHER TRANSCEIVERS

54ACT16640, 74ACT16640 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3585, JUNE 1990-TI0244

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}			-0.5	V to 7 V
Inut voltage range, V _I (see Note 1)	- 0.5	V to	VCC	+ 0.5 V
Output voltage range, VO (see Note 1)	- 0.5	V to	VCC	+ 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})				\pm 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)				$\pm50~\text{mA}$
Continuous output current, IO (VO = 0 to VCC)				$\pm50~mA$
Continuous current through VCC or GND pins			±	± 400 mA
Storage temperature range		_	65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54ACT	16640	74ACT	16640	UNIT	
		MIN	MAX	MIN	MAX	UNII	
VCC	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	٧	
VIH	High-level input voltage	2	4	2		٧	
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage	0	VCC	0	Vcc	٧	
Vo	Output voltage	્ર′ 0<	VCC	0	Vcc	٧	
ЮН	High-level output current	3	-24		-24	mA	
lOL	Low-level output current		24		24	mA	
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V	
TA	Operating free-air temperature	-55	125	-40	85	°C	

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 k Ω or greater.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{3.} All VCC and GND pins must be connected to the proper voltage power supply.

TI0244-D3585, JUNE 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEST SOURITIONS		TA	= 25°	С	54ACT	16640	74ACT	16640		
Ρ,	ARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
		lavi – FO · A	4.5 V	4.4			4.4		4.4			
		$IOH = -50 \mu A$	5.5 V	5.4			5.4		5.4			
V		Jan. — 24 mA	4.5 V	3.94			3.94		3.8		v	
VOH		$I_{OH} = -24 \text{ mA}$	5.5 V	4.94			4.94		4.8		V	
		$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85			
		I	4.5 V			0.1		0.1		0.1		
		IOL = 50 μA	5.5 V			0.1		0.1		0.1	v	
		1	4.5 V			0.36		0,5		0.44		
VOL		IOL = 24 mA	5.5 V			0.36	.0	0.5		0.44	, v	
		IOL = 50 mA†	5.5 V				\$ C.	1.65				
		IOL = 75 mA†	5.5 V				9.			1.65		
Ιį	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ	
416		One input at 3.4 V, Other inputs	5.5 V			0.9				1	4	
∇ICC [§]		at GND or VCC	5.5 V			0.9		1		1	mA	
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF	
Cio	A or B Ports	VO = VCC or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (see Figure 1)

DADAMETER	FROM	то	T,	T _A = 25°C			54ACT16640		74ACT16640	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH .	A or D	D or A	2.2	6	8.3	2.2	9.6	2.2	9.1	
tPHL	A or B	B or A	4.1	7.6	9.3	4.1	11.3	4.1	10.5	ns
tPZH	G	A D	2.7	6.9	8.9	2,7	10.4	2.7	9.8	
tPZL.	٩	A or B	3.5	8.2	10.4	₹3,5	12.1	3.5	11.5	ns
tPHZ	G	A == D	6.1	9.4	11.4	6.1	13.1	6.1	12.5	
tPLZ	G	A or B	5.5	8.7	10.3	5.5	11.5	5.5	11	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
	D	Outputs enabled	0: - 50 - 5 4 - 4 1 1 1 -	52	
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF, f = 1 MHz	9	pF

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

3-86

the

four

fundamental

bus transceivers and registers.

functions that can be performed with the octal

54AC16646, 74AC16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

TI0189-D3477, MARCH 1990

 Member of the Texas Instruments Widebus™ Family 	54AC16646 74AC16646 (TOP V	DL PACKAGE
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1DIR[1 1CAB[2 1SAB[3	56] 1G 55] 1CBA 54] 1SBA
Independent Registers for A and B Buses	GND[] 4	53 GND
Multiplexed Real-Time and Stored Data	1A1 5	52 1B1
·	1A2 [] 6	51]] 1B2
Flow-Through Architecture to Optimize PCB	V _{CC} [] 7	50 V _{CC}
Layout	1A3[] 8	49 🛛 1B3
 Distributed V_{CC} and GND Pin Configuration 	1A4 [] 9	48 🛭 1B4
to Minimize High-Speed Switching Noise	1A5[] 10	47 1B5
 EPIC™ (Enhanced-Performance Implanted 	GND∏ 11	46 GND
CMOS) 1-μm Process	1A6[] 12	45 1B6
● 500-mA Typical Latch-Up Immunity at 125°C	1A7[] 13	44 1 1B7
• 300-ma Typical Laten-op inilitating at 125 C	1A8[] 14 2A1[] 15	43 🛮 1B8 42 🖟 2B1
description	2A1U 15 2A2U 16	42 J 2B1 41 J 2B2
•	2A2U 16 2A3[] 17	40 1 2B3
The 'AC16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control	GNDI 18	39 I GND
circuitry with 3-state outputs arranged for	2A4 19	38 1 2B4
multiplexed transmission of data directly from	2A5[20	37 1 2B5
the data bus or from the internal storage	2A6[21	36 2B6
registers. The device can be used as two 8-bit	V _{CC} [] 22	35 V _{CC}
transceivers or one 16-bit transceiver. Data on	2A7 23	34 🛮 2B7
the A or B bus is clocked into the registers on	2A8[] 24	33 🛚 2B8
the low-to-high transition of the appropriate	GND[] 25	32 🗓 GND
clock input (CAB or CBA). Figure 1 illustrates	2SAB[26	31 2SBA

bus-management

Enable $\overline{\mathbb{G}}$ and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receives data when $\overline{\mathbb{G}}$ is active (low). In the isolation mode $\overline{\mathbb{G}}$ high), A data may be stored in one register and/or B data may be stored in the other register.

2CAB[27

2DIR[

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC16646 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

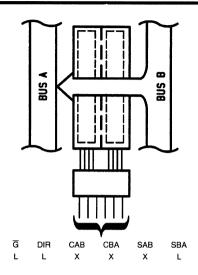
The 54AC16646 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC16646 is characterized for operation from -40° C to 85°C.

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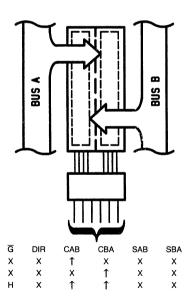


30 11 2CBA

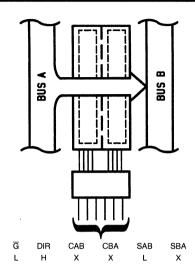
29 1 2G



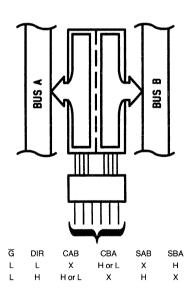
REAL-TIME TRANSFER BUS B TO BUS A



STORAGE FROM A, B OR A AND B



REAL-TIME TRANSFER BUS A TO BUS B



TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS TRANSFER DIAGRAM



D3477, MARCH 1990-TI0189

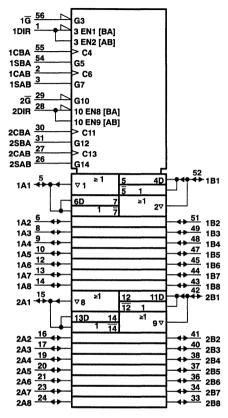
FUNCTION TABLE

INPUTS						DATA	\ I/O [†]	OPERATION OR FUNCTION
G	DIR	CAB	СВА	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	<u> </u>	Х	X	Х	Input	Unspecified	Store A, B unspecified†
Х	X	Χ	↑	Х	Х	Unspecified	Input	Store B, A unspecified†
Н	Х	↑	<u> </u>	Х	Х	Input	Input	Store A and B Data
Н	Х	H or L	H or L	Х	Х	Input	Input	Isolation, hold storage
L	L	X	Х	Х	L	Output	Input	Real-Time B Data to A Bus
L	L	Х	H or L	X	Н	Output	Input	Stored B Data to A Bus
L	Н	Х	Х	L	Х	Input	Output	Real-Time A Data to B Bus
L	н	H or L	X	н	Х	Input	Output	Stored A Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the G or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

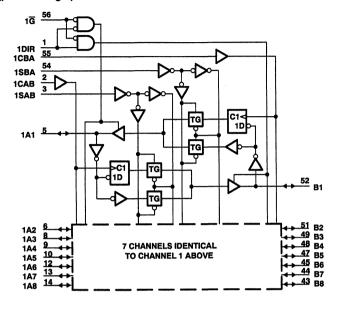


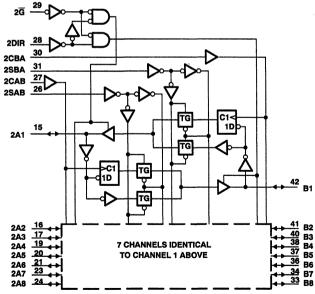
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)







Supply voltage range, V _{CC}			-0.5	V to 7 V
Input voltage range, V _I (see Note 1)	-0.5	V to	Vcc	+ 0.5 V
Output voltage range, VO (see Note 1)	-0.5	V to	Vcc	+ 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)				±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)				±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})				±50 mA
Continuous current through V _{CC} or GND pins			. ±	400 mA
Storage temperature range		6	35°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1664	16	74	AC1664	6	UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNII	
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧	
		VCC = 3 V	2.1			2.1				
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧	
		$V_{CC} = 5.5 V$	3.85			3.85				
		VCC = 3 V			0.9			0.9		
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V	
		$V_{CC} = 5.5 V$			1.65			1.65		
VI	Input voltage		0		Vcc	0		Vcc	٧	
Vo	Output voltage		0		Vcc	0		Vcc	٧	
		VCC = 3 V			-4			-4		
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			-24	mA	
		$V_{CC} = 5.5 V$			-24			-24		
		V _{CC} = 3 V			12			12		
IOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA	
		$V_{CC} = 5.5 V$			24			24		
Δt/Δν	Input transition rise or fall rate	***************************************	0		10	0		10	ns/V	
TA	Operating free-air temperature		-55		125	-40		85	°C	

NOTE 2: All VCC and GND pins must be connected to the proper voltage supply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEGT COMPUTIONS		TA	= 25°	С	54AC	16646	74AC16646		UNIT
"	ARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			3 V	2.9			2.9		2.9		
		$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4		
1			5.5 V	5.4			5.4		5.4		i
\		I _{OH} = -4 mA	3 V	2.58			2.4		2.48		٧
VOH		Jan. — 24 mA	4.5 V	3.94			3.7		3.8		v
		I _{OH} = -24 mA	5.5 V	4.94			4.7		4.8		
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
		$I_{OH} = -75 \text{mA}^{\dagger}$	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
\		IOL = 12 mA	3 V			0.36		0.5		0.44	v
VOL		1	4.5 V			0.36		0.5		0.44	, v
		IOL = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA†	5.5 V					1.65			
		IOL = 75 mA [†]	5.5 V							1.65	
l _l	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
ICC		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF
Cio	A or B ports	VO = VCC or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

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- Member of the Texas Instruments Widebus™
 Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL-Voltage Compatible
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Flow-Through Architecture to Optimize PCB Layout
- Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ACT16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

54ACT16646 ... WD PACKAGE 74ACT16646 ... DL PACKAGE (TOP VIEW)

1DIR[1	56] 1G
1CAB[2	55	1CBA
1SAB[3	54] 1SBA
GND[4	53	GND
1A1[5	52] 1B1
1A2[6	51	1B2
V _{CC} [7	50	Vcc
1A3[8	49	1B3
1A4[9	48	1B4
1A5[10	47	1B5
GND[11	46	GND
1A6[12	45	1B6
1A7[13	44	1B7
1A8[14	43	1B8
2A1[15	42	2B1
2A2[16	41	2B2
2A3[17	40] 2B3
GND[18	39	GND
2A4[19	38	2B4
2A5[20	37] 2B5
2A6[21	36] 2B6
V _{CC} [22	35] v _{cc}
2A7[23	34] 2B7
2A8[24	33] 2B8
GND[25	32] GND
2SAB[26	31] 2SBA
2CAB[27	30	2CBA
2DIR[28	29] 2 <u>G</u>
			•

Enable (\overline{G}) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receivers data when \overline{G} is low. In the isolation mode $(\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT16646 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54ACT16646 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74ACT11646 is characterized for operation from -40° C to 85°C.

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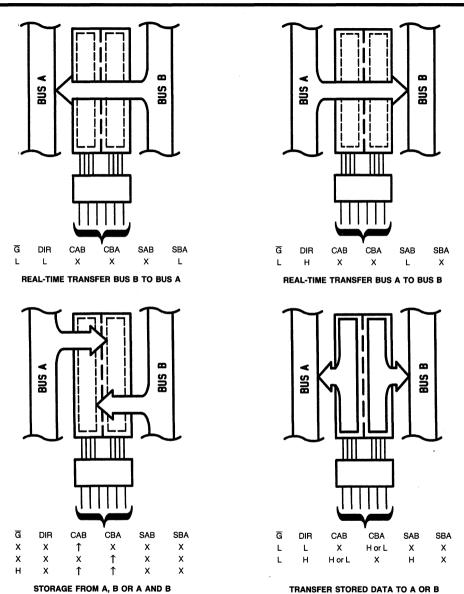


FIGURE 1. BUS TRANSFER DIAGRAM



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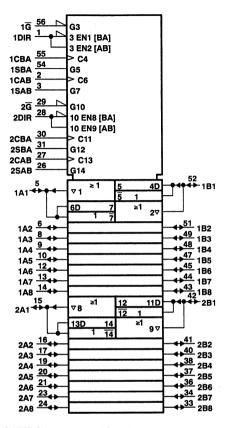
FUNCTION TABLE

		IN	PUTS			DAT	A I/O	OPERATION OF FUNCTION
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
Х	Х	1	Х	Х	X	Input	Unspecified†	Store A, B unspecified†
Χ	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
Н	Х	1	1	X	Х	Input	Input	Store A and B Data
Н	X	H or L	H or L	X	Х	Input	Input	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-Time B Data to A Bus
L	L	Χ	H or L	Х	Н	Output	Input	Stored B Data to A Bus
L	Н	X	Х	L	Х	Input	Output	Real-Time A Data to B Bus
L	Н	H or L	Χ	н	Х	Input	Output	Stored A Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

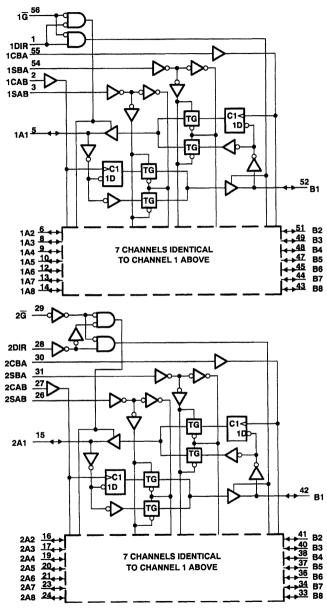
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



D3478, MARCH 1990-TI0169

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.	5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5°	V to VCC	+ 0.5 V
Output voltage range, VO (see Note 1)	-0.5°	V to VCC	+ 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0 \text{ or } V_{ } > V_{CC})$			±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)			\pm 50 mA
Continuous output current, IO (VO = 0 to VCC)			\pm 50 mA
Continuous current through VCC or GND pins			$\pm400~\text{mA}$
Storage temperature range		65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54ACT	16646	74ACT	16646	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2		2		٧
VIL	Low-level input voltage		0.8		0.8	V
Vį	Input voltage	0 .	2 vcc	0	Vcc	V
Vo	Output voltage	0	VCC	0	Vcc	٧
ЮН	High-level output current	47°K	24		-24	mA
lOL	Low-level output current	₹,	24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 2. All V_{CC} and GND pins must be connected to the proper voltage supply.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{3.} Unused or floating inputs should be tied to VCC through a pullup resistor of 5 k Ω or greater.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-	ADAMETED	TEST CONDITIONS		TA	= 25°	С	54AC	16646	74AC	16646	11507
Ρ,	ARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		Jan 50 A	4.5 V	4.4			4.4		4.4		
		$I_{OH} = -50 \mu\text{A}$	5.5 V	5.4			5.4		5.4		
V		1 04 mA	4.5 V	3.94			3.94		3.8		٧
VOH		IOH = -24 mA	5.5 V	4.94			4.94		4.8		V
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V				3.85				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
		I 50 A	4.5 V			0.1		0.1		0.1	
		I _{OL} = 50 μA	5.5 V			0.1		0.1		0.1	
		l 04 - A	4.5 V			0.36		0.5		0.44	٧
VOL		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	٧
		IOL = 50 mA†	5.5 V				\$ 25°	1.65			
		IOL = 75 mA [†]	5.5 V				7.5			1.65	
4	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		± 1	μΑ
loz	A or B ports‡	V _O = V _{CC} or GND	5.5 V			±0.5		±10		±5	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
416		One input at 3.4 V,	F. F. V								4
ΔICC®		Other inputs at GND or VCC	5.5 V	1		0.9		1	Ì	1	mA
Ci	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
Cio	A or B ports	V _O = V _{CC} or GND	5 V		16						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (unless otherwise noted) (see Note 3)

			T _A =	T _A = 25°C		16646	74ACT16646		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency		0	90	0	.₹90	0	90	MHz
tw	Pulse duration, CAB or CBA high or low		5.5		5.5	N 244	5.5		ns
t _{su}	Setup time, A before CAB ↑ or B before CBA ↑	Data high	4		4		4		ns
'Su	Cottap little, // Belove O/LB O/ B Belove OB//	Data low	6		6		6		1,0
th	Hold time, A after CAB ↑ or B after CBA ↑		1.5		1.5		1.5		ns

NOTE: 3. Load circuits and voltage waveforms are shown in Section 1 of Advanced CMOS Logic Data Book, 1990.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

D3478, MARCH 1990—TI0169

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm0.5~V$ (unless otherwise noted) (see Note 3)

DARAMETER	FROM	то	TA	4 = 25°	С	54ACT	16646	74ACT	16646	LINIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
fmax			90			90		90		MHz
tPLH	A or B	B or A	3.9	7.5	9.4	3.9	11.5	3.9	10.6	ns
tPHL			3.4	7.6	10.8	3.4	12.2	3.4	11.4	
^t PZH	G	A or B	3.2	7.7	10.8	3.2	12.9	3.2	11.9	ns
tPZL			4.2	9.0	12.2	4.2	14.6	4.2	13.5	
tPHZ	G	A or B	5.3	7.7	9.6	5.3	10.4	5.3	10.2	ns
^t PLZL			4.9	7.3	9.2	4.9	10.3	4.9	9.9	
t _{PLH}	CBA or CAB	A or B	4.9	8.9	11.1	4.9	13.1	4.9	12.2	ns
t _{PHL}			5.1	9.0	11.0	5.1	13.1	5.1	12.3	
tPLH .	SAB or SBA†	A or B	5.2	10.3	13.8	5.2	17.2	5.2	15.6	ns
t _{PHL}	(with A or B high)		4.9	8.2	10.6	4.9	12.5	4.9	11.7	
t _{PLH}	SBA or SAB†	A or B	4.3	7.8	9.9	4.3	12.1	4.3	11.1	ns
tPHL	(with A or B low)		5.9	11.2	14.9	5.9	18.2	5.9	16.7	
tPZH	DIR	A or B	4.5	9.5	13.8	4.5	18.2	4.5	15.2	ns
tPZL]		4.3	9.2	11.8	4.3	14.2	4.3	13.1	
t _{PHZ}	· DIR	A or B	4.5	7.9	10.2	4.5	11.2	4.5	10.8	ns
tPLZ		- · · · · · · · · · · · · · · · · · · ·	4.4	7.5	9.8	4.4	10.8	4.4	10.4	

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE: 3. Load circuits and voltage waveforms are shown in Section 1 of Advanced CMOS Logic Data Book, 1990.

operating characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Down dissination considers and transmission	Outputs enabled	C: - 50 - 5 4 - 4 MI -	58	pF
Cpd	Power dissipation capacitance per tranceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$	13	pr

TI0190-D3463, MARCH 1990

•	Member of the Texas Instruments Widebus™ Family	74AC166	552	DL F	PACKAGE PACKAGE
	Packaged in Shrink Small Outline 300-mil		(TOP V	IEW,	,
'					
	Packages (SSOP) and 380-mil Fine-Pitch	1GAB	•] 1GBA
	Ceramic Flat Packages Using 25-mil	1CAB	-] 1CBA
	Center-to-Center Pin Spacings	1SAB [4 ~] 1SBA
•	Bus Transceivers/Registers	GND [3 '] GND
_	Independent Registers and Enables for A	1A1 [1 -] 1B1
•	and B Buses	1A2[1] 1B2
		Vcc [V _{CC}
•	Multiplexed Real-Time and Stored Data	1A3 [9 -		1B3
	Flow-Through Architecture to Optimize PCB	1A4 [1 -		1B4
	Layout	1A5[1B5
	•	GND [,		GND
•	Distributed V _{CC} and GND Pin Configuration	1A6 [1B6
	to Minimize High-Speed Switching Noise	1A7 [3		1B7
•	EPIC™ (Enhanced-Performance Implanted	1A8[1 '] 1B8
	CMOS) 1-µm Process	2A1 [5] 2B1
	• •	2A2[•		2B2
•	500-mA Typical Latch-Up Immunity at 125°C	2A3[1] 2B3
		GND [3		GND
aes	scription	2A4 [2A5 [3] 2B4] 2B5
	The 'AC16652 is a 16-bit bus transceiver which	2A5 [2A6 [3		₽,
	consists of D-type flip-flops and control circuitry		1] 2B6
	arranged for multiplexed transmission of data	V _{CC} [2A7[] V _{CC}] 2B7
	directly from the data bus or from the internal	2A7 [2A8 [1] 2B/] 2B8
	storage registers. The device can be used as	GND [3		I 288 I GND
	two 8-bit transceivers or one 16-bit transceiver.	2SAB	1] GND] 2SBA
	Enable GAB and GBA are provided to control	2SAB [2CAB [1		2SBA 2CBA
	the transceiver functions, SAB and SBA control	2GAB [3		1 2GBA 1 2GBA
	pins are provided to select whether real-time or	ZGAB	<u></u>	29] ZUDA

stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental busmanagement functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 74AC16652 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16652 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC16652 is characterized for operation from -40°C to 85°C.

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D3463, MARCH 1990-TI0190

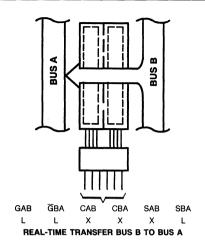
FUNCTION TABLE

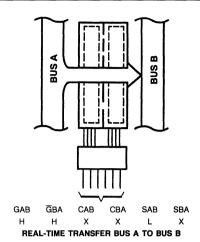
		INP	INPUTS DATA I/O†					
GAB	GBA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	X	Input	Input	Isolation
L	Н	1	1	х	X	Input	Input	Store A and B Data
Х	Н	1	HorL	Х	Х	input	Unspecified	Store A, Hold B
Н	Н	1	1	X	X	Input	Output	Store A in both registers
L	Х	H or L	<u> </u>	X	X	Unspecified	Input	Hold A, Store B
L	L	1	↑	X	X	Output	Input	Store B in both registers
L	L	Х	Х	Х	L	Output	input	Real-Time B Data to A Bus
L	L	Х	H or L	х	Н	Output	Input	Stored B Data to A Bus
Н	Н	Х	Х	L	Х	Input	Output	Real-Time A Data to B Bus
Н	Н	H or L	Х	н	X	Input	Output	Stored A Data to B Bus
Н	ı	H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and
• • •	L	1,01	11 OI L		П	Sulput	Calput	Stored B Data to A Bus

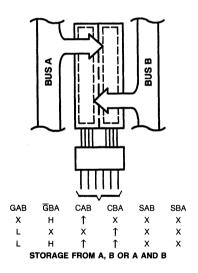
[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.











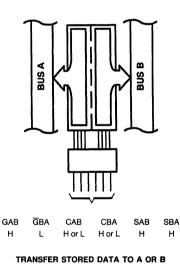
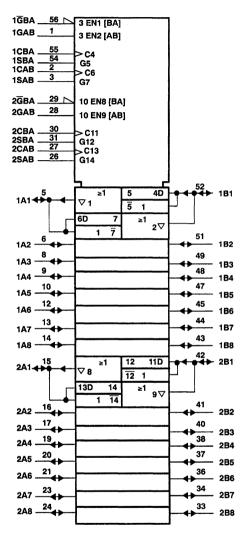


FIGURE 1. BUS TRANSFER DIAGRAM

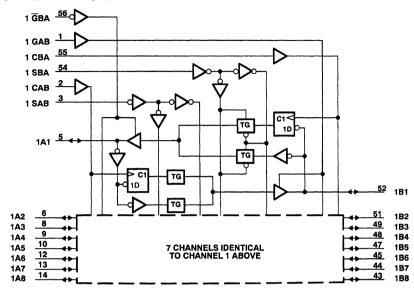
D3463, MARCH 1990-TI0190

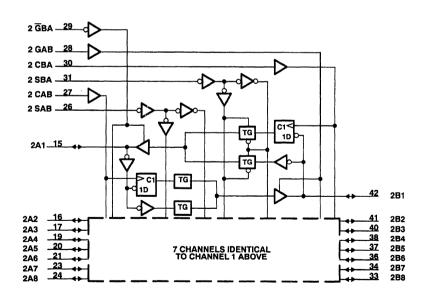
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





D3463, MARCH 1990-TI0190

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage	e range, V _{CC}		0.5	5 V to 7 V
Input voltage	range, V _I (see Note 1)	-0.5 V	√ to V _C C	+ 0.5 V
Output voltag	e range, VO (see Note 1)	−0.5 \	√ to VCC	+ 0.5 V
Input clamp	urrent, I_{IK} (V_{I} < 0 or V_{I} > V_{CC})			±20 mA
Output clamp	current, I _{OK} (V _O < 0 or V _O > V _{CC})			\pm 50 mA
Continuous of	utput current, IO (VO = 0 to VCC)			±50 mA
Continuous c	urrent through VCC or GND pins			±400 mA
Storage temp	erature range		−65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54	AC1665	2	74	AC1665	2	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧
		VCC = 3 V	2.1			2.1			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧
		$V_{CC} = 5.5 V$	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	٧
		$V_{CC} = 5.5 V$			1.65			1.65	
٧ı	Input voltage	-	0		VCC	0		Vcc	V
VO	Output voltage		0		VCC	0		Vcc	٧
		VCC = 3 V			-4			-4	
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			-24	mΑ
		$V_{CC} = 5.5 V$			-24			-24	
		VCC = 3 V			12			12	
lOL	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	-40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAME	TED	TEST CONDITIONS	V	T/	= 25°	С	54AC	16652	74AC1	6652	LIMIT
PARAMET	IEN	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			3 V	2.9			2.9		2.9		
		IOH = -50 μA	4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
V~		IOH = -4 mA	3 V	2.58			2.4		2.48		v
VOH		la = 24 m4	4.5 V	3.94			3.7		3.8		٧
		IOH = -24 mA	5.5 V	4.94			4.7		4.8		
		IOH = -50 mA†	5.5 V				3.85				
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85		
			3 V			0.1		0.1		0.1	
		IOL = 50 μA	4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
V		IOL = 12 mA	3 V			0.36		0.5		0.44	v
VOL		In 04 m4	4.5 V			0.36		0.5		0.44	٧
1		IOL = 24 mA	5.5 V			0.36		0.5		0.44	
		IOL = 50 mA†	5.5 V					1.65			i
		I _{OL} = 75 mA [†]	5.5 V							1.65	
II Contro	ol inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ
IOZ A or B	ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ
Icc		$V_1 = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ
C _i Contro	ol inputs	V _I = V _{CC} or GND	5 V		4.5						pF
Cio A or B	ports	VO = VCC or GND	5 V		16						рF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

TI0191-D3464, MARCH 1990

 Member of the Texas Instruments Widebus™ Family 		652	DL P	ACKAGE
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	1GAB [1CAB [1SAB [2	56 55	1GBA 1CBA 1SBA
Inputs are TTL-Voltage Compatible	GND [GND
Bus Transceivers/Registers	1A1 [1B1
 Independent Registers and Enables for A and B Buses 	1A2 [V _{CC} [1A3 [7	50	1B2 V _{CC} 1B3
Multiplexed Real-Time and Stored Data	1A4 [1 -		1B4
Flow-Through Architecture to Optimize PCB Layout	1A5 [GND [1A6 [11	46	1B5 GND 1B6
 Distributed V_{CC} and GND Pin Configuration to Minimize High-Speed Switching Noise 	1A7 [1A8 [14	43	1B7 1B8
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process 	2A1 [2A2 [2A3 [16	41	2B1 2B2 2B3
● 500-mA Typical Latch-Up Immunity at 125°C	GND [1		GND
description	2A4 [2A5 [2A6 [20	37] 2B4] 2B5] 2B6
The 'ACT16652 is a 16-bit bus transceiver which consists of D-type flip-flops and control	V _{CC} [2A7 [22	35	266 V _{CC} 287
circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be	2A8 [GND [25	33 32] 2B8] GND
used as two 8-bit transceivers or one 16-bit transceiver.	2SAB [2CAB [2GAB [27	30] 2SBA] 2CBA] 2GBA

Enable GAB and GBA are provided to control the transceiver functions, SAB and SBA control pins are provided to select whether real-time or

stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data. Figure 1 illustrates the four fundamental busmanagement functions that can be performed with the octal bus transceivers and registers.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flipflops by simultaneously enabling GAB and GBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The 74ACT16652 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54ACT16652 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74ACT16652 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

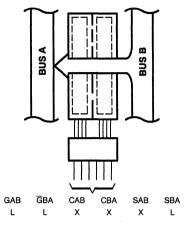


TI0191-D3464, MARCH 1990

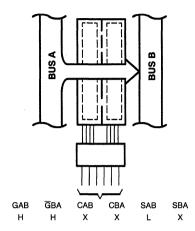
FUNCTION TABLE

		INP	UTS			DATA	A I/O†	ODERATION OF FUNCTION
GAB	GBA	CAB	СВА	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	Н	1	↑	×	Х	Input	Input	Store A and B Data
Х	Н	1	H or L	X	Х	Input	Unspecified	Store A, Hold B
н	н	1	1	X	Х	Input	Output	Store A in both registers
L	Х	H or L	1	Х	Х	Unspecified	Input	Hold A, Store B
L	L	↑	↑	Х	Х	Output	Input	Store B in both registers
L	L	Х	Х	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	Н	Output	Input	Stored B Data to A Bus
н	1	H or L	H or L	Н	Н	Output	Output	Stored A Data to B Bus and
''	-	11012	1101 L	''		Cutput	Output	Stored B Data to A Bus

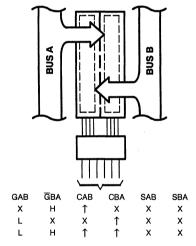
[†] The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.



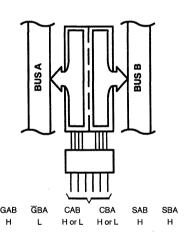
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A, B OR A AND B

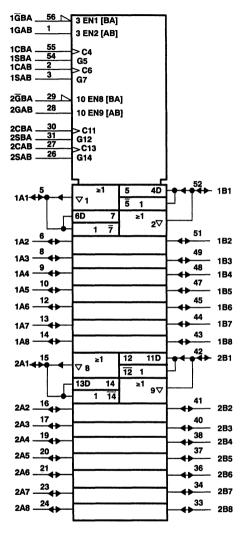


TRANSFER STORED DATA TO A OR B

FIGURE 1. BUS TRANSFER DIAGRAM

PRODUCT PREVIEW

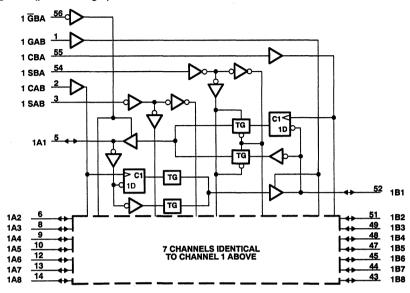
logic symbol†

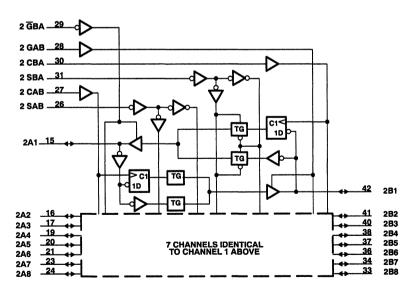


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagrams (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	- 0.5	V to 7 V
Input voltage range, V _I (see Note 1)	to VCC	+ 0.5 V
Output voltage range, VO (see Note 1)0.5 V	to VCC	+ 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})		± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)		\pm 50 mA
Continuous output current, IO (VO = 0 to VCC)		±50 mA
Continuous current through V _{CC} or GND pins	=	± 400 mA
Storage temperature range	-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54ACT16652			74ACT16652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
VI	Input voltage	0		VCC	0		Vcc	٧
VO	Output voltage	0		VCC	0		VCC	٧
ЮН	High-level output current			-24			-24	mA
lOL	Low-level output current			24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	- 55		125	-40		85	°C

NOTE 2: All VCC and GND pins must be connected to the proper voltage supply.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT16652, 74ACT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

D3464, MARCH 1990-TI0191

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEGT COURTIONS		TA	= 25°0	C	54ACT	16652	74ACT	16652		
Ρ/	ARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
		1 50 4	4.5 V	4.4			4.4		4.4			
		$I_{OH} = -50 \mu A$	5.5 V	5.4			5.4		5.4			
		1	4.5 V	3.94			3.94		3.8		.,	
VOH		$I_{OH} = -24 \text{ mA}$	5.5 V	4.94			4.94		4.8		٧	
		$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85			
			4.5 V			0.1		0.1		0.1		
		$IOL = 50 \mu A$	5.5 V			0.1		0.1		0.1		
			4.5 V			0.36		0.5		0.44	v	
VOL		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44		
		IOL = 50 mA†	5.5 V					1.65	5			
		IOL = 75 mA†	5.5 V							1.65		
l _l	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μА	
loz	A or B ports‡	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
ICC		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ	
Aloos		One input at 3.4 V,	E E V			0.0		-		4	1	
ΔICC ₈		Other inputs at GND or VCC	5.5 V	0.9		1		1		mA		
Ci	Control inputs V _I = V _{CC} or GND		5 V		4.5						pF	
Cio	A or B ports	VO = VCC or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

For I/O ports, the parameter IO7 includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to VCC.

RODUCT PREVIEW

54AC16657, 74AC16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0245-D3586, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive input (1T/ \overline{R} or $2T/\overline{R}$) determines the direction of data flow. When $1T/\overline{R}$ (or $2T/\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when $1T/\overline{R}$ (or $2T/\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable input $1\overline{OE}$ (or $2\overline{OE}$) is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/EVEN (or 2ODD/EVEN) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

54AC16657 ... WD PACKAGE 74AC16657 ... DL PACKAGE (TOP VIEW)

10E	1 🔾	56	∏1T/Ř
NC [2	55	10DD/EVEN
I ERROR	3	54] 1 PARITY
GND [4	53	GND
1A0 [5	52	□1B 0
1A1 [6	51	□1B1
V _{CC} □	7	50	□v _{cc}
1A2 [8	49]1B2
1A3 [9	48]1B3
1A4 [10	47]1B4
GND [11	46	GND
1A5 🗌	12	45]1 B5
1A6 🗌	13	44]1B6
1A7 [14	43	□1B7
2A0 🗌	15	42	☐ 2B0
2A1	16	41	☐ 2B1
2A2 🗌	17	40	☐ 2B2
GND [18	39	GND
2A3 🗌	19	38	☐ 2B3
2A4 [20	37	☐ 2B4
2A5 [21	36	☐ 2B5
V _{CC}	22	35	□ v _{cc}
2A6 🗌	23	34	☐ 2B6
2A7 [24	33	☐ 2B7
GND [25	32	GND
2ERROR	26	31	2PARITY
NC [27	30	20DD/EVEN
20E [28	29	□ 2T/Ř

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/EVEN (or 2ODD/EVEN) input. For example, if 1ODD/EVEN is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1ERROR (or 2ERROR) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/EVEN is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1ERROR is low, indicating a parity error.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



54AC16657, 74AC16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

D3586, JUNE 1990-TI0245

The 'AC16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board.

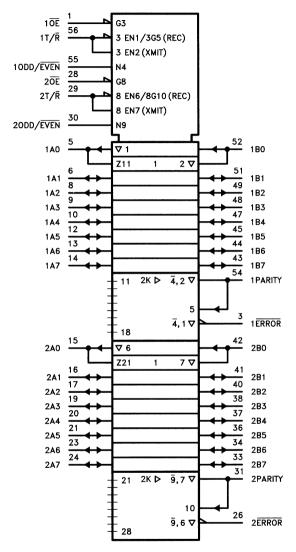
The 54AC16657 is characterized over the full military temperature range of -55° C to 125°C. The 74AC16657 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

NUMBER OF A OR B		IN	PUTS	INPUT/OUTPUT	(DUTPUTS
INPUTS THAT ARE HIGH	ŌĒ	T/R	ODD/EVEN	PARITY	ERROR	OUTPUT MODE
0, 2, 4, 6, 8	L	Н	Н	Н	Z	Transmit
	L	Н	L	L	Z	Transmit
	L	L	Н	Н	Н	Receive
	L	L	Н	L	L	Receive
	L	L	L	Н	L	Receive
	L	L	L	L	Н	Receive
1, 3, 5, 7	L	Н	Н	L	Z	Transmit
	L	Н	L	Н	Z	Transmit
	L	L	Н	Н	L	Receive
	L	L	Н	L	Н	Receive
	L	L	L	Н	Н	Receive
	L	L	L	L	L	Receive
DON'T CARE	Н	Х	X	Z	Z	Z



logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

54AC16657, 74AC16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS D3586, JUNE 1990—T10245

logic diagram, each transceiver (positive logic) ŌĒ ΑO - B0 Α1 A2 -Α3 **B3** Α4 В4 Α5 **B**5 Α6 - B6 Α7 - B7 PRODUCT PREVIEW **PARITY** ODD/EVEN . ERROR

54AC16657, 74AC16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0245-D3586, JUNE 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC			-0.5	V to	7 V
Input voltage range, V _I (see Note 1)	-0.5	V to	VCC	+ 0.	.5 V
Output voltage range, VO (see Note 1)	-0.5	V to	VCC	+ 0.	.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})				±20	mΑ
Output clamp current, IOK (VO < 0 or VO > VCC)				± 50	mΑ
Continuous output current, IO (VO = 0 to VCC)				±50	mΑ
Continuous current through VCC or GND pins			±	± 500	mΑ
Storage temperature range			65°C	to 15	0°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54	AC1665	7	74	AC1665	7	HAUT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V	
		VCC = 3 V	2.1			2.1				
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			٧	
		$V_{CC} = 5.5 V$	3.85			3.85				
		V _{CC} = 3 V			0.9			0.9		
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	V	
		$V_{CC} = 5.5 V$			1.65			1.65		
VI	Input voltage		0		Vcc	0		VCC	٧	
Vo	Output voltage		0		Vcc	0		Vcc	٧	
		V _{CC} = 3 V			-4			-4		
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			-24	mΑ	
		$V_{CC} = 5.5 V$			-24			-24		
		VCC = 3 V			12			12		
lol	Low-level output current	$V_{CC} = 4.5 V$			24			24	mΑ	
		$V_{CC} = 5.5 V$			24			24		
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V	
TA	Operating free-air temperature		-55		125	-40		85	°C	

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

D3586, JUNE 1990-TI0245

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				TA	= 25°	С	54AC	16657	74AC1	16657		
PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			3 V	2.9			2.9		2.9			
		$I_{OH} = -50 \mu A$	4.5 V	4.4			4.4		4.4			
			5.5 V	5.4			5.4		5.4			
\/-··		IOH = -4 mA	3 V	2.58			2.4		2.48		V	
VOH		1 04-mA	4.5 V	3.94			3.7		3.8		V	
		1OH = −24 mA	5.5 V	4.94			4.7		4.8			
		$IOH = -50 \text{ mA}^{\dagger}$	5.5 V				3.85					
		$IOH = -75 \text{ mA}^{\dagger}$	5.5 V						3.85			
			3 V			0.1		0.1		0.1		
		IOL = 50 μA	4.5 V			0.1		0.1		0.1		
			5.5 V			0.1		0.1		0.1		
		I _{OL} = 12 mA	3 V			0.36		0.5		0.44	٧	
VOL			4.5 V			0.36		0.5		0.44	V	
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44		
		I _{OL} = 50 mA [†]	5.5 V					1.65				
		IOL = 75 mA [†]	5.5 V							1.65		
lj .	Control inputs	VI = VCC or GND	5.5 V			±0.1		± 1		± 1	μΑ	
loz	A or B ports§	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μΑ	
Ci	Ci Control inputs V _I = V _{CC} or GND		5 V		4.5						pF	
Cio	A or B ports	V _O = V _{CC} or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm~0.3~V$ (unless otherwise noted) (see Note 3)

DADAMETED	FROM	ROM TO		$T_A = 25^{\circ}C$		54AC	16657	74AC1	16657		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
tPLH	A or B	B or A								ns	
tPHL	AUID	BUIA								115	
tPLH	^	PARITY								ns	
tPHL	An	FADILI								115	
tPLH	ODD/EVEN	PARITY, ERROR								ns	
^t PHL	ODD/EVEN	FANIT,ENNON								115	
tPLH	Bn	ERROR								ns	
tPHL_	on on	ENHON								115	
tPLH	PARITY	ERROR								ns	
tPHL	FABILI	LAHOH								113	
^t PZH	ŌĒ	An, Bn, PARITY or ERROR								ns	
^t PZL	OL	Λη, ση, FARITI OI ERROR								113	
t _{PHZ}	ŌĒ	A _n , B _n , PARITY or ERROR								ns	
^t PLZ	JE	An, Dn, FAITH TO ENHON								113	

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

54AC16657, 74AC16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0245--- D3586, JUNE 1990

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm~0.5~V$ (unless otherwise noted) (see Note 3)

DADAMETED	FROM	то	T _A =	= 25°	С	54AC	16657	74AC1	6657	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH	A or B	B or A								ns
^t PHL	AOIB	BUIA								115
^t PLH		PARITY								ns
^t PHL	An	FARITI								115
^t PLH	ODD/EVEN	PARITY, ERROR								ns
[†] PHL	ODD/EVEN	FARITT,ERROR								
^t PLH	В	ERROR								ns
^t PHL	B _n	ENNON								ris
tPLH .	PARITY	ERROR								ns
†PHL	PANIT	ENNON								118
^t PZH	- ŌĒ	An, Bn, PARITY or ERROR								
tPZL]	An, on, FARILY OF ERROR								ns
^t PHZ	- ŌĒ	An, Bn, PARITY or ERROR								
tPLZ]	An, Dn, FARITY OF ERROR								ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Daniel dia dia dia dia dia dia dia dia dia dia	Outputs enabled	O		
Opd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$		p-

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54ACT16657, 74ACT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0292-D3586, AUGUST 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- 3-State Outputs Drive Bus Lines Directly
- Inputs are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'ACT16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive input (1T/ \overline{R} or $2T/\overline{R}$) determines the direction of data flow. When $1T/\overline{R}$ (or $2T/\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when $1T/\overline{R}$ (or $2T/\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable input $1\overline{OE}$ (or $2\overline{OE}$) is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/EVEN (or 2ODD/EVEN) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

54ACT16657 ... WD PACKAGE 74ACT16657 ... DL PACKAGE (TOP VIEW)

10E	1 U	56	∏1T/Ř
NC [2	55	10DD/EVEN
1 ERROR	3	54	1PARITY
GND [4	53	GND
1A0 [5	52]1B0
1A1	6	51]1B1
V _{CC} □	7	50	□ v _{cc}
1A2	8	49]1B2
1A3 [9	48]1B3
1A4 [10	47	□1 B4
GND [11	46	☐GND
1A5 [12	45] 1B5
1A6 🗌	13	44]1B6
1A7 🗌	14	43]1B7
2A0 [15	42	☐ 2B0
2A1	16	41	☐ 2B1
2A2 🗌	17	40	☐ 2B2
GND [18	39	GND
2A3 🗌	19	38	☐ 2B3
2A4 [20	37	☐ 2B4
2A5 🗌	21	36	☐ 2B5
V _{CC} □	22	35	□ v _{cc}
2A6	23	34	☐ 2B6
2A7 🗌	24	33	☐ 2B7
GND [25	32	GND
2ERROR [26	31	2PARITY
NC [27	30	20DD/EVEN
20E	28	29	□ 2T/R
			-

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/EVEN (or 2ODD/EVEN) input. For example, if 1ODD/EVEN is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1ERROR (or 2ERROR) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 10DD/EVEN is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1ERROR is low, indicating a parity error.

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Texas Instruments

PRODUCT PREVIEW

54ACT16657, 74ACT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0292-D3586, AUGUST 1990

description (continued)

The 'ACT16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board.

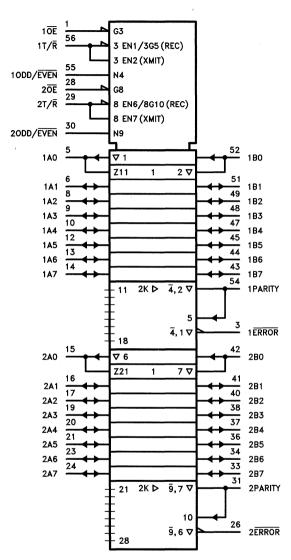
The 54ACT16657 is characterized over the full military temperature range of -55° C to 125°C. The 74ACT16657 is characterized for operation from -40° C to 85°C.

FUNCTION TABLE, EACH SECTION

NUMBER OF A OR B		IN	PUTS	INPUT/OUTPUT	(DUTPUTS
INPUTS THAT ARE HIGH	ŌĒ	T/R	ODD/EVEN	PARITY	ERROR	OUTPUT MODE
0, 2, 4, 6, 8	L	Н	Н	Н	Z	Transmit
	L	Н	L	L	Z	Transmit
	L	L	Н	Н	Н	Receive
	L	L	Н	L	L	Receive
	L	L	L	Н	L	Receive
	L	L	L	L	Н	Receive
1, 3, 5, 7	L	Н	Н	L	Z	Transmit
	L	Н	L	Н	Z	Transmit
	L	L	Н	Н	L	Receive
	L	L	Н	L	Н	Receive
	L	L	L	Н	Н	Receive
	L	L	L	L	L	Receive
DON'T CARE	Н	Х	Х	Z	Z	Z

D3586, AUGUST 1990-TI0292

logic symbol†

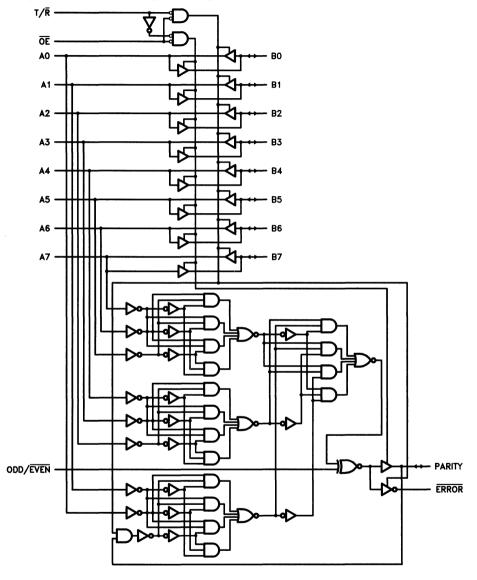


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



TI0292-D3586, AUGUST 1990

logic diagram, each transceiver (positive logic)





PRODUCT PREVIEW

54ACT16657, 74ACT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

D3586, AUGUST 1990-TI0292

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	± 50 mA
Continuous output current, IO (VO = 0 to VCC)	± 50 mA
Continuous current through VCC or GND pins	± 500 mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54	ACT166	57	74.	ACT166	57		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	٧	
		VCC = 3 V	2.1			2.1				
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V .	
		$V_{CC} = 5.5 V$	3.85			3.85				
		VCC = 3 V			0.9			0.9		
VIL	Low-level input voltage	$V_{CC} = 4.5 V$			1.35			1.35	٧	
		$V_{CC} = 5.5 V$			1.65			1.65		
٧ı	Input voltage		0		VCC	0		Vcc	٧	
Vo	Output voltage		0		Vcc	0		Vcc	٧	
		V _{CC} = 3 V			-4			-4		
ЮН	High-level output current	$V_{CC} = 4.5 V$			-24			-24	mA	
		$V_{CC} = 5.5 V$			-24			-24		
		VCC = 3 V			12			12		
lOL .	Low-level output current	$V_{CC} = 4.5 V$			24			24	mA	
		$V_{CC} = 5.5 V$			24			24		
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V	
TA	Operating free-air temperature		-55		125	-40		85	°C	

NOTE 2: All VCC and GND pins must be connected to the proper voltage power supply.



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT16657, 74ACT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

TI0292--- D3586, AUGUST 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETER	TEST CONDITIONS		TA	= 25°C	;	54ACT	16657	74ACT	16657	LIMIT	
Ρ,	ARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			3 V	2.9			2.9		2.9			
		I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4			
1			5.5 V	5.4			5.4		5.4			
		IOH = -4 mA	3 V	2.58			2.4		2.48		V	
VOH		Jan. — 04 m4	4.5 V	3.94			3.7		3.8		· •	
		IOH = -24 mA	5.5 V	4.94			4.7		4.8			
		IOH = -50 mA†	5.5 V				3.85					
		IOH = -75 mA†	5.5 V						3.85		1	
			3 V			0.1		0.1		0.1		
		IOL = 50 μA	4.5 V			0.1		0.1		0.1		
			5.5 V			0.1		0.1		0.1		
\		IOL = 12 mA	3 V			0.36		0.5		0.44	\ v	
VOL		1	4.5 V			0.36		0.5		0.44		
		I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44		
		IOL = 50 mA†	5.5 V					1.65				
		I _{OL} = 75 mA [†]	5.5 V							1.65		
II.	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	μΑ	
loz	A or B ports§	VO = VCC or GND	5.5 V			±0.5		±10		±5	μΑ	
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF	
Cio	A or B ports	VO = VCC or GND	5 V		16						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V~\pm~0.3~V$ (unless otherwise noted) (see Note 3)

	FROM	ТО	T	TA = 25°C		54AC1	16657	74ACT	16657	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
tPLH .	A or B	B or A									
tPHL	AUID	BOLA								ns	
^t PLH	Δ	PARITY									
tPHL_	An	PARILI								ns	
tPLH	ODD/EVEN	PARITY, ERROR								ns	
^t PHL	ODD/EVEN	PARITY,ERROR									
tPLH .	ь	ERROR									
^t PHL	- B _n	ERHOR								ns	
tPLH	PARITY	ERROR								ns	
^t PHL	PANIII	ENNON									
^t PZH	ŌĒ	A D DADITY or FROND									
^t PZL	7 05	A _n , B _n , PARITY or ERROR								ns	
tPHZ	- ŌĒ	A D DADITY or FREED									
tPLZ]	A _n , B _n , PARITY or ERROR								ns	

switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V~\pm~0.5~V$ (unless otherwise noted) (see Note 3)

	FROM	то	T	= 25°	C	54ACT	16657	74ACT	16657		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
tPLH .	A or B	B or A								ns	
tPHL	AUID	BOTA								115	
^t PLH		PARITY								ns	
^t PHL	An	PARIT								118	
^t PLH	ODD/EVEN	PARITY, ERROR									
^t PHL	ODD/EVEN	FANIIT,ENNON								ns	
tPLH		ERROR									
tPHL	B _n	ENNON								ns	
tPLH .	PARITY	ERROR									
^t PHL	PARILI	ENNON								ns	
^t PZH	ŌĒ	An, Bn, PARITY or ERROR									
^t PZL] VE	An, Dn, PARITY OF ERROR								ns	
tPHZ	- ŌĒ	A P PARITY OF ERROR									
tPLZ] OE	A _n , B _n , PARITY or ERROR								ns	

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

\mathbf{J} operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
C .	Davies dissination considers a sector as	Outputs enabled	C: = 50 = 5 4 = 4 MH=		
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF, f} = 1 \text{ MHz}$		pF

20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0252-D3575, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration
 Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16821 and 'ACT16821 are noninverting 20-bit D-type flip-flops composed of two 10-bit sections with separate control signals. For either 10-bit flip-flop section, the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of the clock input (1CLK or 2CLK) and appears on the appropriate Q outputs if the output enable $1\overline{\text{OE}}$ (or $2\overline{\text{OE}}$) is low. If $1\overline{\text{OE}}$ (or $2\overline{\text{OE}}$) is high, the outputs are in the high-impedance state. $1\overline{\text{OE}}$ (or $2\overline{\text{OE}}$) does not affect the operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPL	JTS	FI ID FI OD DATA	O OLITPLITO			
CLK	ŌĒ	FLIP-FLOP DATA	Q OUTPUTS			
1	Н	Current D Data	Z			
L	Н	Previous D Data	Z			
1	L	Current D Data	Current D Data			
L	L	Previous D Data	Previous D Data			

54AC16821, 54ACT16821 ... WD PACKAGE 74AC16821, 74ACT16821 ... DL PACKAGE (TOP VIEW)

10E	Ц	1	U	56	Ь	10	CL	K
1Q1	₫	2		55		11	D1	
1Q2	П	3		54	Б	11	D2	
GND	П	4		53	D	G	NE)
1Q3	Ц	5		52		11	D3	
1Q4	D	6		51		11	D4	
Vcc	Ц	7		50		٧	cc	
1Q5	П	8		49		11	D5	
1Q6	П	9		48		11	D6	
1Q7	D	10		47		11	D7	
GND		11		46		G	NE)
1Q8	Ц	12		45		1 (D8	
1Q9		13		44		11	D9	
1Q10		14		43		11	D1	0
2Q1		15		42		2	D1	
2Q2		16		41		2	D2	:
2Q3		17		40		2	D3	;
GND		18		39		G	NE)
2Q4		19		38		2	D4	ļ
2Q5		20		37		2	D5	,
2Q6		21		36		2	D6	;
Vcc		22		35		٧	cc	
2Q7		23		34		2	D7	,
2Q8		24		33		2	D8	1
GND		25		32	Р	G	NE)
2Q9		26		31	П	2	D9	1
2Q10		27		30	П	2	D1	0
20E		28		29	Р	2	CL	K

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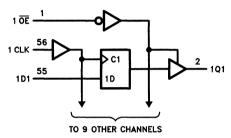
PRODUCT PREVIEW

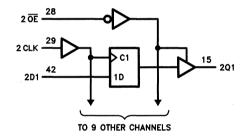
The 74AC16821 and 74ACT16821 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16821 has CMOS-compatible input thresholds. The 'ACT16821 has TTL-compatible input thresholds.

The 54AC16821 and 54ACT16821 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16821 and 74ACT16821 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





TI0253-D3576, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16822 and 'ACT16822 are inverting 20-bit D-type flip-flops composed of two 10-bit sections with separate control signals. For either 10-bit flip-flop section, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of the clock input (1CLK or 2CLK) and appears on the appropriate Q outputs if the output enable 10E (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the outputs are in the high-impedance state. 10E (or 20E) does not affect the operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPL	JTS	FI ID FI OD DATA	O CUITDUITO
CLK	ŌE	FLIP-FLOP DATA	Q OUTPUTS
1	Н	Current D Data	Z
L	Н	Previous D Data	Z
1	L	Current D Data	Inverse of Current D Data
L	L	Previous D Data	Inverse of Previous D Data

54AC16822, 54ACT16822 ... WD PACKAGE 74AC16822, 74ACT16822 ... DL PACKAGE

(TOP VIEW)

10E] ₁ ∪	56 1 1 CLK	
1Q1[2	55] 1 D 1	
1Q2 [3	54	
GND []4	53 GND	
1Q3 [5	52 1 D̄3	
1Q4 []6	51 1 D 4	
V _{CC}	7	50 V _{CC}	
1Q5 [8	49 🗌 1 🗖 5	
1Q6 [9	48 🛮 1 Ū6	
1Q7 [10	47 🛮 1 🗖 7	
GND [111	46 GND	
1Q8 [12	45 ☐ 1 D̄8	
1Q9 [13	44 🗌 1 🗖 9	
1Q10[14	43 🛮 1 🗖 1 0	
2Q1[15	42 2 D 1	
2Q2 [16	41 2D2	
2Q3 [17	40 🗌 2D̄3	
GND [18	39 🗌 GND	
2Q4 [19	38 2D4	
2Q5 [20	37 🗌 2D̄5	
2Q6 [21	36∏ 2Ū6	
v _{cc} [22	35 V _{CC}	
2Q7 [23	34 2 D7	
2Q8 [24	33 🗌 2 🗖 8	
GND [25	32 GND	
2Q9 [26	31 2D9	
2Q10[27	30 ☐ 2D̄10	
20E [28	29 2CLK	

RODUCT PREVIEW

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20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

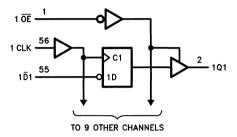
D3576, JUNE 1990-TI0253

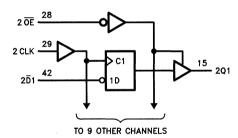
The 74AC16822 and 74ACT16822 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16822 has CMOS-compatible input thresholds. The 'ACT16822 has TTL-compatible input thresholds.

The 54AC16822 and 54ACT16822 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16822 and 74ACT16822 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





54AC16823, 54ACT16823 74AC16823, 74ACT16823 18-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

Ti0254-D3577, JUNE 1990

 Members of Texas Instruments Widebus™ Family 	54AC16823, 54ACT16823 WD PACKAGE 74AC16823, 74ACT16823 DL PACKAGE (TOP VIEW)
 Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center- to-Center Pin Spacings 	1 CLR 1
 Inputs are TTL- or CMOS-Voltage Compatible 	GND
3-State Outputs Drive Bus Lines Directly	1 Q3
 Flow-Through Architecture Optimizes PCB Layout 	1Q4
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1Q6
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process 	1Q7 12
● 500-mA Typical Latch-Up Immunity at 125°C	2Q1
description	2Q3 🛮 17 40 🗒 2D3
The 'AC16823 and 'ACT16823 are noninverting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For either 9-bit flip-flop section, if the clock enable (1CLKEN or 2CLKEN) is low, the data present at the corresponding D inputs is stored in the	GND

When the output enable (10E or 20E) is low, the corresponding Q outputs are active (high or low logic levels). When $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state. $1\overline{OE}$ (or 20E) does not affect the internal operation of the flip-flops; previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE. EACH SECTION

INPUTS				FLIP-FLOP DATA	O OUTPUTO
CLR	CLKEN	CLK	ŌĒ	FLIP-FLOP DATA	Q OUTPUTS
L	Х	Х	L	L	L
Н	Н	Х	L	Previous D Data	Previous D Data
Н	Х	L	L	Previous D Data	Previous D Data
Н	L	1	L	Current D Data	Current D Data
Н	Н	X	Н	Previous D Data	Z
Н	X	L	Н	Previous D Data	Z
Н	L	1	Н	Current D Data	Z

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flip-flops on the rising edge of 1CLK (or 2CLK).

When 1CLKEN (or 2CLKEN) is high, the flip-

flops retain their previously stored values.

Taking 1CLR (or 2CLR) low asynchronously

clears the corresponding flip-flops.



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33 2D8

32 GND

31 2D9

29 2CLK

30 2CLKEN

2Q8 T24

GND □25

2Q9 T26

20E | 27

2CLR 128

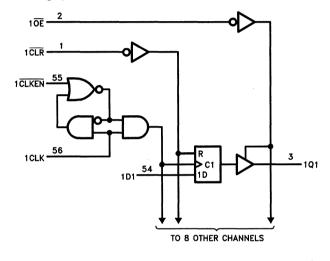
D3577, JUNE 1990-TI0254

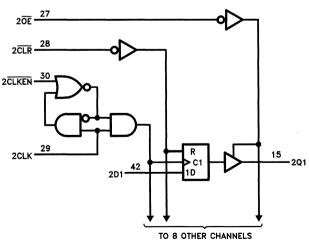
The 74AC16823 and 74ACT16823 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16823 has CMOS-compatible input thresholds. The 'ACT16823 has TTL-compatible input thresholds.

The 54AC16823 and 54ACT16823 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16823 and 74ACT16823 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)





RODUCT PREVIEW

•	Members	of	Texas	Instruments	Widebus™
	Family				

- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16824 and 'ACT16824 are inverting 18-bit D-type flip-flops composed of two 9-bit sections with separate control signals. For either 9-bit flip-flop section, if the clock enable (1CLKEN or 2CLKEN) is low, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of 1CLK (or 2CLK). When 1CLKEN (or 2CLKEN) is high, the flip-flops retain their previously stored values. Taking 1CLR (or 2CLR) low asynchronously clears the corresponding flip-flops.

54AC16824, 54ACT16824 ... WD PACKAGE 74AC16824, 74ACT16824 ... DL PACKAGE (TOP VIEW)

1 CLR	ı O	56	1CLK
10E	2	55	1 CLKEN
1Q1	3	54	1D1
GND [4	53	GND
1Q2 [5	52] 1 D̄2
1Q3 [6	51	□1D3
V _{CC} [7	50	□ v _{cc}
1Q4 [8	49] 1 D̄4
1Q5 [9	48]1D̄5
1Q6 [10	47] 1 D̄ 6
GND [11	46	GND
1Q7 [12	45	_ 1 D̄7
1Q8 [13	44	_1 D̄8
1Q9 [14	43]1Ū9
2Q1[15	42	_ 2D̄1
2Q2 [16	41	_ 2D̄2
2Q3 [17	40] 2D3
GND [18	39	GND
2Q4 [19	38	_] 2Ū4
2Q5 [20	37] 2Ď5
2Q6 [21	36] 2Ū6
V _{CC} [22	35	□ v _{cc}
2Q7 [23	34	□ 2D7
2Q8 [24	33	□ 2D8
GND [25	32	GND
2Q9 [26	31	2D9
20E	27	30	2CLKEN
2CLR	28	29	☐ 2CLK

When the output enable $(1\overline{OE} \text{ or } 2\overline{OE})$ is low, the corresponding Q outputs are active (high or low logic levels). When $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state. $1\overline{OE}$ (or $2\overline{OE}$) does not affect the internal operation of the flip-flops: previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE, EACH SECTION

INPUTS				FLIP-FLOP DATA	Q OUTPUTS	
CLR	CLKEN	CLK	ŌĒ	FLIP-FLOP DATA	QOUIPUIS	
L	X	X	L	L	L	
Н	Н	X	L	Previous D Data	Inverse of Previous D Data	
Н	X	L	L	Previous D Data	Inverse of Previous D Data	
Н	L	1	L	Current D Data	Inverse of Current D Data	
Н	Н	X	Н	Previous D Data	Z	
Н	X	L	Н	Previous D Data	Z	
Н	L	1	Н	Current D Data	Z	

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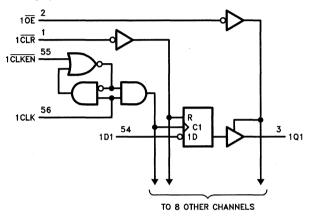


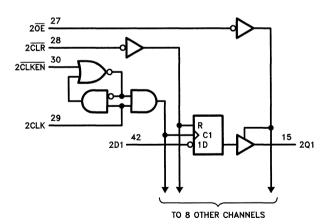
The 74AC16824 and 74ACT16824 are packaged in Ti's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16824 has CMOS-compatible input thresholds. The 'ACT16824 has TTL-compatible input thresholds.

The 54AC16824 and 54ACT16824 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16824 and 74ACT16824 are characterized for operation from -40° C to 85°C.

logic diagram (positive logic)







74AC16827, 74ACT16827 20-BIT BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

TI0268-D3544, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16827 and 'ACT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output enable inputs ($1\overline{G}1$ and $1\overline{G}2$ or $2\overline{G}1$ and $2\overline{G}2$) must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74AC16827 and 74ACT16827 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

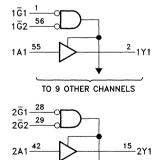
The 'AC16827 has CMOS-compatible input thresholds. The 'ACT16827 has TTL-compatible input thresholds.

The 54AC16827 and 54ACT16827 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16827 and 74ACT16827 are characterized for operation from -40°C to 85°C.

54AC16827, 54ACT16827 ... WD PACKAGE 74AC16827, 74ACT16827 ... DL PACKAGE (TOP VIEW)

1 Ē 1□	1	U 56	Ь	1 G 2	2
1Y1	2	55	Б	1 A 1	
1Y2	3	54	Б	1A2	2
GND 🗌	4	53	Б	GNI)
1Y3 🗌	5	52	Б	1 A 3	5
1Y4 🗌	6	51	Ь	1 A 4	Ļ
V _{cc} □	7	50		٧cc	2
1Y5 🗌	8	49		1A5	5
1Y6 🗌	9	48		146	5
1Y7 [10	47		1 A 7	7
GND [11	46		GNI	0
1Y8 🗌	12	45		1 A 8	3
1 Y 9 🗌	13	44		1 A S	•
1Y10 🗌	14	43		1 A 1	0
2Y1 🗌	15	42		2A	1
2Y2 🗌	16	41		2A2	2
2Y3 🗌	17	40		2A3	3
GND [18	39		GNI	D
2Y4 🗌	19	38		2A4	4
2Y5 🗌	20	37		2A5	5
2Y6 🗌	21	36		2A(6
V _{cc} □	22	35		Vcc)
2Y7 🗌	23	34		2A	7
2Y8 🗌	24	33		2A8	3
GND [25	32		GNI	D
2Y9 🗌	26	31		2A9	€
2Y10 🗌	27	30	_	2A	
2Ğ1 🗌	28	29		2Ğ:	2

logic diagram (positive logic)



TO 9 OTHER CHANNELS

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TI0269--- D3545, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

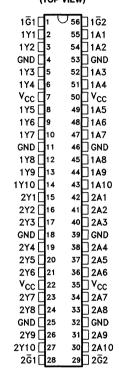
The 'AC16828 and 'ACT16828 are inverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output enable inputs ($1\overline{G}1$ and $1\overline{G}2$ or $2\overline{G}1$ and $2\overline{G}2$) must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are placed into the high-impedance state.

The 74AC16828 and 74ACT16828 are packaged in Tl's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

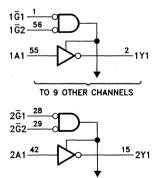
The 'AC16828 has CMOS-compatible input thresholds. The 'ACT16828 has TTL-compatible input thresholds.

The 54AC16828 and 54ACT16828 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16828 and 74ACT16828 are characterized for operation from -40° C to 85°C.

54AC16828, 54ACT16828 ... WD PACKAGE 74AC16828, 74ACT16828 ... DL PACKAGE (TOP VIEW)



logic diagram (positive logic)



TO 9 OTHER CHANNELS

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PRODUCT PREVIEW

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

TI0270-D3546, JUNE 1990

Members of Texas Instruments Widebus™ **Family**

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- EPIC™ (Enhanced-Performance Implanted) CMOS) 1-µm Process
- 500-mA Typical Latch-up Immunity at 125°C

description

The 'AC16833 and 'ACT16833 contain two noninverting 8-bit to 9-bit parity transceivers. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

54AC16833, 54ACT16833 ... WD PACKAGE 74AC16833, 74ACT16833 ... DL PACKAGE (TOP VIEW)

10EB	1	56 10EA
1 CLK	2	55 1 CLR
1 ERR	3	54 1 PARITY
GND [4	53 GND
1A1[5	52 1B1
1A2	6	51 1B2
V _{CC} □	7	50 □ V _{CC}
1A3 🗌	8	49 🗌 1 B 3
1A4 🗌	9	48 🗌 1 B 4
1A5 [10	47 🗌 1 B5
GND [11	46 GND
1A6 [12	45 🗌 1 B6
1A7 🗌	13	44 🗌 1 B7
1 A 8 🗌	14	43 1B8
2A1	15	42 2B1
2A2 [16	41 2B2
2A3 🗌	17	40 2B3
GND [18	39 🗌 GND
2A4 🗌	19	38 🗌 2B4
2A5 🗌	20	37 2B5
2A6 🗌	21	36 🗌 2B6
V _{cc} □	22	35 V _{CC}
2A7 🗌	23	34 🗌 2B7
2A8 🗌	24	33 🗌 2B8
GND [25	32 GND
2ERR	26	31 2PARITY
2CLK	27	30 2CLR
20EB	28	29 20EA

The error output (1ERR or 2ERR) is configured as an open-collector output. The B-to-A parity error flag is clocked into 1ERR (or 2ERR) on the low-to-high transition of 1CLK (or 2CLK). 1ERR (or 2ERR) is cleared (set high) by taking the clear input 1CLR (or 2CLR) low.

The 74AC16833 and 74ACT16833 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16833 has CMOS-compatible input thresholds. The 'ACT16833 has TTL-compatible input thresholds.

The 54AC16833 and 54ACT16833 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16833 and 74ACT16833 are characterized for operation from -40°C to 85°C.

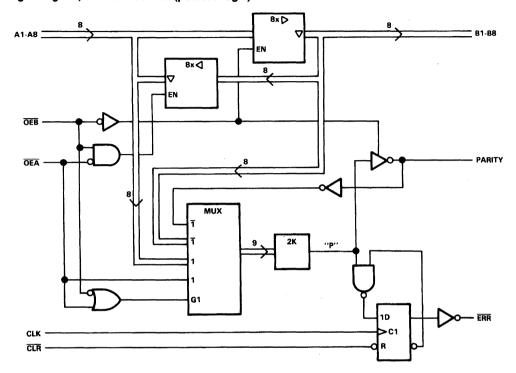
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INSTRUMENTS

D3546, JUNE 1990-TI0270

logic diagram, each transceiver (positive logic)



54AC16834, 54ACT16834 74AC16834, 74ACT16834 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

TI0271-D3547, JUNE 1990

 Members of Texas Instruments Widebus™ Family 	54AC16834, 54ACT16834 WD PACKAGE 74AC16834, 74ACT16834 DL PACKAGE
 Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings 	(TOP VIEW) 1 OEB
 Inputs are TTL- or CMOS-Voltage Compatible 	GND 4 53 GND 1A1 5 52 1B1
3-State Outputs Drive Bus Lines Directly	1A2
 Flow-Through Architecture Optimizes PCB Layout 	1A3 🛮 8 49 🗎 1B3 1A4 🗓 9 48 🔲 1B4
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	1A5
 EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process 	1A7
• 500-mA Typical Latch-Up Immunity at 125°C	2A1 ☐ 15 42 ☐ 2B1 2A2 ☐ 16 41 ☐ 2B2
description	2A3 🛮 17 40 🗒 2B3
The 'AC16834 and 'ACT16834 contain two inverting 8-bit to 9-bit parity bus transceivers. For each transceiver, when data is transmitted	GND □18 39 □ GND 2A4 □19 38 □ 2B4 2A5 □20 37 □ 2B5 2A6 □21 36 □2B6

2A6 □21 from the A bus to the B bus, an odd-parity bit is 35 V_{CC} generated and output on the parity I/O pin 34 🗆 2B7 2A7 🛮 23 (1PARITY or 2PARITY). When data is 2A8 | 24 33 2B8 transmitted from the B bus to the A bus, GND 25 32 GND 1PARITY (or 2PARITY) is configured as an 2ERR | 26 31 2PARITY input and combined with the B input data to 2CLK 27 30 2CLR generate an active-low error flag if odd parity is 20EB 28 29 20EA not detected.

The error output (1ERR or 2ERR) is configured as an open-collector output. The B-to-A parity error flag is clocked into 1ERR (or 2ERR) on the low-to-high transition of 1CLK (or 2CLK). 1ERR (or 2ERR) is cleared (set high) by taking the clear input 1CLR (or 2CLR) low.

The 74AC16834 and 74ACT16834 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16834 has CMOS-compatible input thresholds. The 'ACT16834 has TTL-compatible input thresholds.

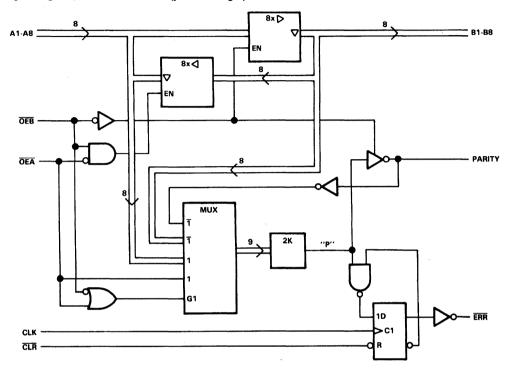
The 54AC16834 and 54ACT16834 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16834 and 74ACT16834 are characterized for operation from -40° C to 85°C.

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D3547, JUNE 1990-TI0271

logic diagram, each transceiver (positive logic)



PRODIICT PREVIEW

Members of Texas Instruments Widebus™ Family Packaged In Shrink Small-Outline 300-mil

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 54AC/ACT16841 and 74AC/ACT16841 are noninverting 20-bit D-type latches composed of two 10-bit sections. Separate control signals are provided for each 10-bit section.

For each 10-bit section, when the enable input (1C or 2C) is low, the latches are placed into the storage mode. In contrast, when (1C or 2C) is high, the latches are transparent. In this mode, the data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

74AC/ACT16841 ... DL PACKAGE 54AC/ACT16841 ... WD PACKAGE

(TOP VIEW)

1 OE	₫ī	\cup_{5}	6]]	1C
1Q1	2	5	5[]	1D1
1Q2	[]₃	5	4	1D2
GND	[]4	5	3 🛚	GND
1Q3	[]5	5	2	1D3
1Q4	6	5	巾	1 D4
v_{cc}	□ 7	5	巾	v_{cc}
1Q5	[]8	4	9[]	1D5
1Q6	9	4	8	1D6
1Q7	[]10	4	巾	1D7
GND	[]11	4	6	GND
1Q8	12	4	5	1 D8
1Q9	13	4	4[]	1 D9
1Q10	[]14	4.	3	1D10
2Q1	15	4.	2	2D1
2Q2	[]16	4	巾	2D2
2Q3	[]17	4	미	2D3
GND	18	3	9[]	GND
2Q4	[]19	3	8[]	2D4
2Q5	20	3	7	2D5
2Q6	2	1 3	6[]	2D6
v_{cc}	□ 22	2 3	5]]	v_{cc}
2Q7	23	3	4	2D7
2Q8	24	1 3	3[]	2D8
GND	25	5 3.	2	GND
2Q9	26	3	1	2D9
2Q10	27	7 3	巾	2D10
20E	28	3 2	9	2C

The 74AC16841 and 74ACT16841 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

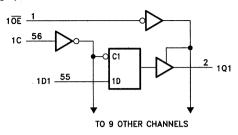
The 'AC16841 has CMOS-compatible input thresholds. The 'ACT16841 has TTL-compatible input thresholds.

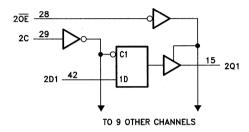
The 54AC/ACT16841 is characterized over the full military temperature range of -55° C to 125°C. The 74AC/ACT16841 is characterized for operation from -40° C to 85°C.

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Texas VI

logic diagram (positive logic)





54AC16842, 54ACT16842 74AC16842, 74ACT16842 20-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

 Members of Texas Instruments Widebus™ Family 	54AC16842, 54ACT16842 WD PACKAGE 74AC16842, 74ACT16842 DL PACKAGE
Packaged In Shrink Small-Outline 300-mil	(TOP VIEW)
Packages (SSOP) and 380-mil Fine-Pitch	10E
Ceramic Flat Packages Using 25-mil Center-	
to-Center Pin Spacings	1Q1 2 55 1D1
, •	1Q2 ☐3 54 ☐ 1D2 GND ☐4 53 ☐ GND
Inputs are TTL- or CMOS-Voltage	GND
Compatible	1Q3 [] 52 [] 1D3 1Q4 [] 6 51 [] 1D4
3-State Outputs Drive Bus Lines Directly	
Elow Through Architecture Ontimizes BOB	V _{CC}
 Flow-Through Architecture Optimizes PCB Layout 	1Q5 0 49 1D5 1Q6 19 48 1D6
Layout	1Q7 10 47 1D7
 Distributed V_{CC} and GND Pin Configuration 	GND TITE 46 GND
Minimizes High-Speed Switching Noise	1Q8 12 45 1D8
 EPIC™ (Enhanced-Performance Implanted 	109 13 44 1 1 1 1 1 1 1 1
CMOS) 1-µm Process	1010 14 43 1 D10
, ,	2Q1 \[15 \] 42 \[2\bar{D}1
 500-mA Typical Latch-Up Immunity at 125°C 	202 16 41 2D2
description	208 17 40 2D3
•	GND 18 39 GND
The 'AC16842 and 'ACT16842 are inverting	204 119 38 2 D 4
20-bit D-type latches composed of two 10-bit	205 20 37 205
sections with separate control signals. For each	206 21 36 2 0 6
10-bit section, when the enable input 1C (or	V _{CC}
2C) is low, the latches are in the storage mode.	207 23 34 207
In contrast, when 1C (or 2C) is high, the	2Q8 24 33 2D8
latches are transparent. In this mode, the	GND 25 32 GND
inverse of the data present at the 1D (or 2D)	2Q9 26 31 2D9
inputs is transmitted to the 1Q (or 2Q) outputs if 1OE (or 2OE) is low. If 1OE (or 2OE) is high,	2Q10 27 30 2D10
the corresponding outputs are in the high-	20E 28 29 2C
impedance state.	201 (120 23) 20

The 74AC16842 and 74ACT16842 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16842 has CMOS-compatible input thresholds. The 'ACT16842 has TTL-compatible input thresholds.

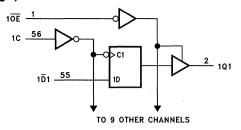
The 54AC16842 and 54ACT16842 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16842 and 74ACT16842 are characterized for operation from -40° C to 85°C.

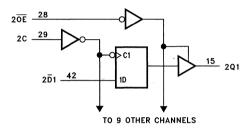
PRODUCT PREVIEW

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logic diagram (positive logic)





TI0274—D3550, JUNE 1990

 Members of Texas Instruments Widebus™ 54AC16843, 54ACT16843 ... WD PACKAGE 74AC16843, 74ACT16843 ... DL PACKAGE Family (TOP VIEW) Packaged In Shrink Small-Outline 300-mil ∪56∏1C Packages (SSOP) and 380-mil Fine-Pitch 1CLR T Ceramic Flat Packages Using 25-mil Center-10E [2 55 1PRE to-Center Pin Spacings 54 1D1 101∏3 GND ∏4 53 GND Inputs are TTL- or CMOS-Voltage 102 ∏5 52 1D2 Compatible 103 □6 51 D 1 D 3 3-State Outputs Drive Bus Lines Directly V_{CC} □ 7 50 7 VCC 1Q4 🗍 8 49 1D4 Flow-Through Architecture Optimizes PCB 105 ∏9 48 1D5 Lavout 47 1D6 106 110 Distributed Vcc and GND Pin Configuration GND T11 46 GND **Minimizes High-Speed Switching Noise** 45 1D7 107 🗆 12 EPIC™ (Enhanced-Performance Implanted) 1Q8 🗍 13 44 🗍 1 D8 43 1 D9 CMOS) 1-µm Process 109 114 2Q1[15 42 7 2D1 500-mA Typical Latch-Up Immunity at 125°C 41 2D2 2Q2 🗍 16 203 17 40 2D3 description 39 GND GND ∏18 The 'AC16843 and 'ACT16843 are noninverting 204 ∏19 38 72D4 18-bit D-type latches composed of two 9-bit 2Q5 T 20 37 D 2D5 sections with separate control signals. For each 206 721 36 2D6 9-bit section, when the enable input 1C (or 2C) 35 VCC is low, the latches are in the storage mode, In 207 23 34 2D7 contrast, when 1C (or 2C) is high, the latches 2Q8 🛮 24 33 2D8 are transparent. In this mode, data present at GND 125 32 GND the 1D (or 2D) inputs is transmitted to the 1Q 209 1 26 31 7 2D9 (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ 20E [27 30 2PRE (or 20E) is high, the corresponding outputs are 2CLR 28 29 2C in the high-impedance state.

Preset (1PRE and 2PRE) and clear (1CLR and 2CLR) inputs are provided to set the corresponding Q outputs asynchronously to a high or low logic level. Taking 1PRE (or 2PRE) low sets the corresponding outputs high. If 1PRE (or 2PRE) is high, taking 1CLR (or 2CLR) low sets the corresponding outputs low.

The 74AC16843 and 74ACT16843 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

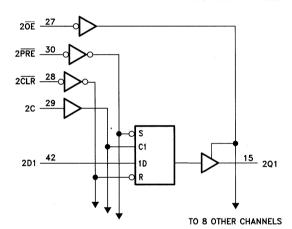
The 'AC16843 has CMOS-compatible input thresholds. The 'ACT16843 has TTL-compatible input thresholds.

The 54AC16843 and 54ACT16843 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16843 and 74ACT16843 are characterized for operation from -40° C to 85°C.

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TI0275-D3551, JUNE 1990

 Members of Texas Instruments Widebus™ Family

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 54AC/ACT16844 and 74AC/ACT16844 are inverting 18-bit D-type latches composed of two 9-bit sections. Separate control signals are provided for each 9-bit section.

For each 9-bit section, when the enable input 1C (or 2C) is low, the latches are placed into the storage mode. In contrast, when 1C (or 2C) is high, the latches are transparent. In this mode, the inverse of the data present at the 1D (or 2D) inputs is transmitted to the 1Q (or 2Q) outputs if $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the corresponding outputs are in the high-impedance state.

SN54AC/ACT16844 ... WD PACKAGE SN74AC/ACT16844 ... DL PACKAGE (TOP VIEW)

1 CLR	1	U	56		1C
10E [2		55	Ō	1PRE
1Q1 [3		54	D	1D1
GND [4		53	D	GND
1Q2	5		52	D	1D2
1Q3 [6		51	b	1 D̄ 3
V _{cc} [7		50		v_{cc}
1Q4 [8		49		1 D̄4
1Q5 [9		48		1 D̄ 5
1Q6 [10		47		1D̄6
GND [111		46		GND
1Q7 [12		45		1 D̄ 7
1Q8 [13		44		1 D̄8
1Q9 [14		43		1 D̄ 9
2Q1 [15		42	Д	2D1
2Q2 [16		41		2D2
2Q3 [17		40		2D3
GND [18		39		GND
2Q4 🗌	19		38	П	2D4
2Q5 [20		37	Р	2D5
2Q6 [21		36	р	2D6
V _{cc} [22		35	Р	v _{cc}
2Q7 [23		34	Р	2 <u>D</u> 7
2Q8 [24		33		2D8
GND [25		32		GND
2Q9 [26		31	Ц	2D9
20E	27		30	Ц	2PRE
2CLR	28		29	μ	2C

Preset (1PRE and 2PRE) and clear (1CLR and 2CLR) inputs are provided to set the corresponding Q outputs asynchronously to a high or low logic level. Taking 1PRE (or 2PRE) low sets the corresponding outputs high. If 1PRE (or 2PRE) is high, taking 1CLR (or 2CLR) low sets the corresponding outputs low.

The 74AC16844 and 74ACT16844 are packaged in Ti's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

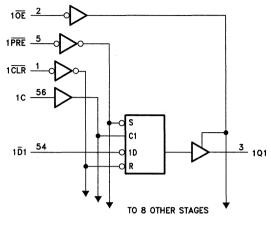
The 'AC16844 has CMOS-compatible input thresholds. The 'ACT16844 has TTL-compatible input thresholds.

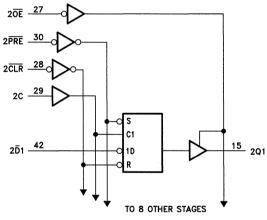
The 54AC/ACT16844 is characterized over the full military temperature range of -55°C to 125°C. The 74AC/ACT16844 is characterized for operation from -40° C to 85°C.

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TI0276--- D3552, JUNE 1990

Members of Texas Instruments Widebus™ Family

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted) CMOS) 1-um Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16853 and 'ACT16853 contain two noninvertina 8-bit to 9-bit parity transceivers. For either transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY), When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1ERR or 2ERR) is an opencollector output. 1ERR (or 2ERR) can be passed, sampled, stored, and cleared from the latch using the latch enable (1EN and 2EN) and clear (1CLR and 2CLR) inputs.

54AC16853, 54ACT16853 ... WD PACKAGE 74AC16853, 74ACT16853 ... DL PACKAGE (TOP VIEW)

10EB	1	56	10EA
1EN	2	55	1 CLR
1 ERR	3	54	1 PARITY
GND [4	53	GND
1A1 [5	52	☐1B1
1A2	6	51] 1B2
V _{cc} [7	50	□ v _{cc}
1A3 🗌	8	49] 1B3
1A4	9	48] 1B4
1A5 🗌	10	47] 1B5
GND [11	46	GND
1A6	12	45]1B6
1A7 [13	44] 1B7
1A8 [14	43]1B8
2A1 [15	42	☐ 2B1
2A2 [16	41	2B2
2A3 [17	40	☐ 2B3
GND [18	39	GND
2A4 [19	38	☐ 2B4
2A5 [20	37	☐ 2B5
2A6 [21	36	2B6
V _{CC} [22	35	$\Box v_{cc}$
2A7 [23	34	2B7
2A8 🗌	24	33	2B8
GND [25	32	GND
2ERR	26	31	2PARITY
2EN [27	30	2CLR
20EB	28	29	20EA

The 74AC16853 and 74ACT16853 are packaged in Ti's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

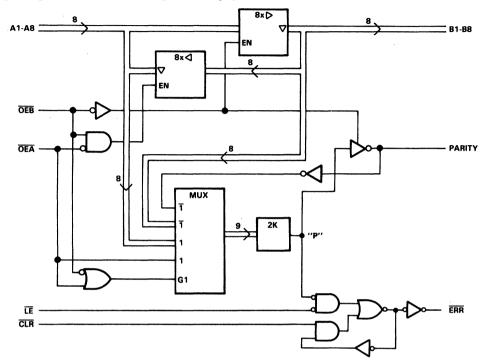
The 'AC16853 has CMOS-compatible input thresholds. The 'ACT16853 has TTL-compatible input thresholds.

The 54AC16853 and 54ACT16853 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16853 and 74ACT16853 are characterized for operation from -40°C to 85°C.

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logic diagram, each transceiver (positive logic)



TI0277-D3553, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted) CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16854 and 'ACT16854 contain two inverting 8-bit to 9-bit parity bus transceivers. For either transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1ERR or 2ERR) is an opencollector output, 1ERR (or 2ERR) can be passed, sampled, stored, and cleared from the latch using the latch enable (1EN and 2EN) and clear (1CLR and 2CLR) inputs.

54AC16854, 54ACT16854 ... WD PACKAGE 74AC16854, 74ACT16854 ... DL PACKAGE (TOP VIEW)

OEB [1 U	56	1 OEA
1EN [2	55	1 CLR
1 ERR	3	54] 1 PARITY
GND [4	53	GND
1A1 🗌	5	52]1B1
1A2 🗌	6	51]1B2
V _{CC}	7	50	□ v _{cc}
1A3 🗌	8	49	□1B3
1A4 🗌	9	48]1B4
1 A 5 🗌	10	47	∏1B5
GND [11	46	GND
1 A 6 🗌	12	45	□1B6
1 A 7 🗌	13	44	□1B7
1 A 8 🗌	14	43	☐1B8
2A1 🗌	15	42	☐ 2B1
2A2 🗌	16	41	☐ 2B2
2A3 🗌	17	40	☐ 2B3
GND [18	39	GND
2A4 🗌	19	38	☐ 2B4
2A5 🗌	20	37	☐ 2B5
2A6 🗌	21	36	☐ 2B6
V _{CC} □	22	35	□ ^v cc
2A7 🗌	23	34	☐ 2B7
2A8 🗌	24	33	☐ 2B8
GND [25	32	GND
2ERR	26	31	2PARITY
2EN	27	30	2CLR
20EB	28	29	20EA

The 74AC16854 and 74ACT16854 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

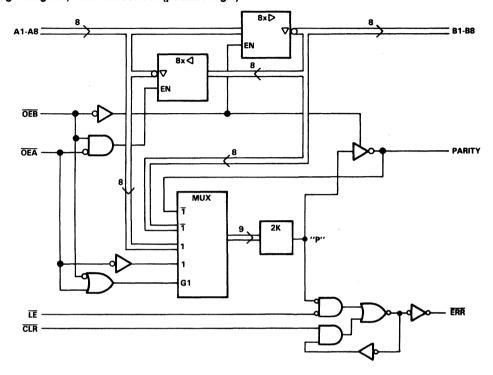
The 'AC16854 has CMOS-compatible input thresholds. The 'ACT16854 has TTL-compatible input thresholds.

The 54AC16854 and 54ACT16854 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16854 and 74ACT16854 are characterized for operation from -40°C to 85°C.

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logic diagram, each transceiver (positive logic)





54AC16861, 54ACT16861 74AC16861, 74ACT16861 20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0234-D3556, JUNE 1990

 Members of Texas Instruments Widebus™ Family 	54AC16861, 54ACT16861 WD PACKAGE 74AC16861, 74ACT16861 DL PACKAGE (TOP VIEW)
Packaged In Shrink Small-Outline 300-mil	(IOP VIEW)
•	1ĞAB∏1 ∪56∏1ĞBA
Packages (SSOP) and 380-mil Fine-Pitch	
Ceramic Flat Packages Using 25-mil Center-	1B1 []2 55 []1A1
to-Center Pin Spacings	1B2 □ 3 54 □ 1A2
a landa and TTI an ONOO Valtage	GND□4 53□GND
Inputs are TTL- or CMOS-Voltage	1B3∐5 52∐1A3
Compatible	1B4∏6 51∏1A4
3-State Outputs Drive Bus Lines Directly	ν _{cc}
• 3-3tate Outputs Drive bus Lines Directly	185 8 49 1A5
 Flow-Through Architecture Optimizes PCB 	186
Layout	1B7 10 47 11A7
·	GNDH11 46HGND
 Distributed V_{CC} and GND Pin Configuration 	1B8 12 45 1A8
Minimizes High-Speed Switching Noise	
• • •	189 13 44 1A9
 EPIC™ (Enhanced-Performance Implanted 	1B10 14 43 1A10
CMOS) 1-μm Process	2B1🖸15 42🗘 2A1
a 500 m A Tomical Latab Un Immunity at 40500	2B2□16 41□2A2
 500-mA Typical Latch-Up Immunity at 125°C 	2B3∐17 40 <u></u> 2A3
	GND ☐ 18 39
description	2B4 19 38 2A4
The !AC16061 and !ACT16061 are manipulating	2B5 20 37 2A5
The 'AC16861 and 'ACT16861 are noninverting	2B6 721 36 72A6
20-bit bus transceivers composed of two 10-bit	V _{CC} 22 35 V _{CC}
transceiver sections with separate control	2B7 23 34 2A7
signals. These devices allow data transmission	
from the A bus to the B bus or from the B bus	
to the A bus, depending upon the levels	GND
present at the output-enable inputs (1GAB,	2B9[]26 31[]2A9
	2 <u>B</u> 10□27 30□2 <u>A</u> 10
2GAB, 1GBA, and 2GBA). The control logic	2ĞAB∐28 29∏2ĞBA
also allows for isolation and latching.	

The 74AC16861 and 74ACT16861 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16861 has CMOS-compatible input thresholds. The 'ACT16861 has TTL-compatible input thresholds.

The 54AC16861 and 54ACT16861 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16861 and 74ACT16861 are characterized for operation from -40° C to 85°C.

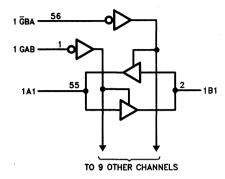
FUNCTION TABLE, EACH SECTION

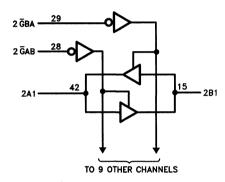
INP	UTS	OPERATION
GAB	GBA	OPERATION
L	Н	A to B
Н	L	B to A
Н	Н	Isolation
		Latch A and B
L .	-	(A = B)

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Ti0235-D3557, JUNE 1990

•	Members	of	Texas	Instruments	Widebus™
	Family				

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16862 and 'ACT16862 are inverting 20-bit bus transceivers composed of two 10-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs (1GAB, 2GAB, 1GBA, and 2GBA). The control logic also allows for isolation and latching.

54AC16862, 54ACT16862 ... WD PACKAGE 74AC16862, 74ACT16862 ... DL PACKAGE (TOP VIEW)

1ĞAB[1	U	56	р	1 GB/	١
1 B1	2		55	b	1A1	
1B2[3		54	Б	1A2	
GND	4		53	b	GND	
1B3[5		52	Б	1 A 3	
1B4[6		51	Ō	1A4	
V _{CC} [7		50	D	V _{CC}	
185[8		49	Ď	1Ã5	
1B6[9		48		1A6	
1B7[10		47	b	1 A 7	
GND[11		46		GND	
1B8[12		45	D	1 A 8	
1B9[13		44		1A9	
1B10[14		43		1A10)
2B1[15		42		2A1	
2B2[16		41		2A2	
2B3[17		40		2A3	
GND[18		39		GND	
2B4[19		38		2A4	
2B5[20)	37		2A5	
2B6[21		36	Þ	2A6	
V _{CC} [22	!	35	D	v _{cc}	
2B7[23		34		2A7	
2B8[24		33		2A8	
GND[25		32	Р	GND	
2B9[26		31	Р	2A9	
2B10[27		30	Р	2 <u>A</u> 1	
2GAB[28	_	29	П	2GB	4

The 74AC16862 and 74ACT16862 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16862 has CMOS-compatible input thresholds. The 'ACT16862 has TTL-compatible input thresholds.

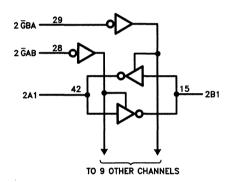
The 54AC16862 and 54ACT16862 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16862 and 74ACT16862 are characterized for operation from -40°C to 85°C.

FUNCTION TABLE, EACH SECTION

	UTS	OPERATION
GAB	GBA	OPERATION
L	Н	Ā to B
Н	L	B to A
Н	Н	Isolation
		Latch A and B
-	-	$(A = \overline{B})$

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1 GBA 56 1 GAB 1 1A1 55 TO 9 OTHER CHANNELS



PRODUCT PREVIEW

Members of Texas Instruments Widebus™ Family

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16863 and 'ACT16863 are noninverting 18-bit bus transceivers composed of two 9-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs (1GAB, 2GAB, 1GBA, and 2GBA). The control logic also allows for isolation and latching.

54AC16863, 54ACT16863 ... WD PACKAGE 74AC16863, 74ACT16863 ... DL PACKAGE (TOP VIEW)

1GAB[1	56]1ĞBA
1B1[2	55	1A1
1B2	3	54	1A2
GND	4	53	GND
1B3	5	52	1A3
1B4	6	51	1 1A4
V _{cc}	7	50	5vcc
1B5	8	49	1A5
1B6	9	48	T1A6
187	10	47	1A7
GND	11	46	GND
1B8	12	45	T1A8
1B9	13	44	11A9
GND	14	43	GND
GND	15	42	GND
2B1	16	41	72A1
2B2	17	40	12A2
GND	18	39	GND
2B3	19	38	12A3
2B4	20	37	12A4
2B5	21	36	2A5
Vcc	22	35	Hvac
2B6	23	34	2A6
~30[1	~~	

33 2A7

32 GND

31 2A8

30 T 2A9

29 2 GBA

287 24

GND 25

288 726

2B9 727

2ĞAB∏28

The 74AC16863 and 74ACT16863 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16863 has CMOS-compatible input thresholds. The 'ACT16863 has TTL-compatible input thresholds.

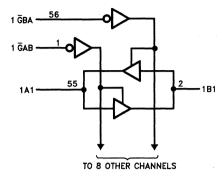
The 54AC16863 and 54ACT16863 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16863 and 74ACT16863 are characterized for operation from -40° C to 85°C.

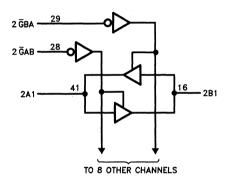
FUNCTION TABLE, EACH SECTION

INP	UTS	ODEDATION
GAB	GBA	OPERATION
L	Н	A to B
Н	L	B to A
Н	Н	Isolation
		Latch A and B
_	L	(A = B)

EPIC and Widebus are trademarks of Texas Instruments Incorporated.







Members of Texas Instruments Widebus™ Family

- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16864 and 'ACT16864 are inverting 18-bit bus transceivers composed of two 9-bit transceiver sections with separate control signals. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels present at the output-enable inputs (1GAB, 2GAB, 1GBA, and 2GBA). The control logic also allows for isolation and latching.

54AC16864, 54ACT16864 ... WD PACKAGE 74AC16864, 74ACT16864 ... DL PACKAGE (TOP VIEW)

1GAB	1	56]1GBA
1 B1	2	55]1A1
1B2[3	54]1A2
GND[4	53	GND
1B3[5	52]1A3
1B4[6	51]1A4
v _{cc} [7	50	□vcc
1B5	8	49]1A5
1B6[9	48]1A6
1B7[10	47]1A7
GND	11	46	GND
1B8[12	45]1A8
1B9[13	44]1A9
GND[14	43	GND
GND	15	42	GND
2B1[16	41]2A1
2B2[17	40]2A2
GND	18	39	GND
2B3[19	38	2A3
2B4[20	37]2A4
2B5[21	36]2A5
V _{CC} [22	35	□vcc
2B6	23	34]2 A6
2B7[24	33]2A7
GND[25	32	GND
2B8[26	31]2A8
2B9[27	30]2A9
2GAB	28	29	□2ĞBA
			•

The 74AC16864 and 74ACT16864 are packaged in Tl's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16864 has CMOS-compatible input thresholds. The 'ACT16864 has TTL-compatible input thresholds.

The 54AC16864 and 54ACT16864 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16864 and 74ACT16864 are characterized for operation from -40° C to 85°C.

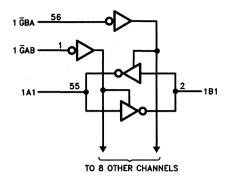
FUNCTION TABLE, EACH SECTION

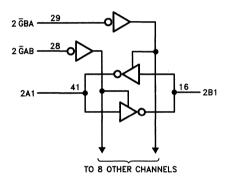
INP	UTS	OPERATION		
GAB	GBA	OPERATION		
L	Н	Ā to B		
Н	L	B to A		
Н	Н	Isolation		
		Latch A and B		
L	L	$(A = \overline{B})$		

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RODUCT PREVIEW







54AC16952, 54ACT16952 74AC16952, 74ACT16952

TI0238-D3560, JUNE 1990

16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Members of Texas Instruments Widebus™ Family
- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Lavout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16952 and 'ACT16952 are noninverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1OEAB and 2OEAB), clockenable (1CEAB and 2CEAB), and clock (1CLKAB and 2CLKAB) inputs. When 1CEAB (or 2CEAB) is high, data storage is inhibited and the registers retain their previous states. When 1CEAB (or 2CEAB) is low, the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB). If 1OEAB (or 2OEAB) is also low, this stored data appears on the corresponding B outputs; if 10EAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. 1OEAB (or 2OEAB) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is controlled by 10EBA and 20EBA, 1CEBA and 2CEBA, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

54AC16952, 54ACT16952 ... WD PACKAGE 74AC16952, 74ACT16952 ... DL PACKAGE (TOP VIEW)

10EAB	1	56	10EBA
1 CLKAB	2	55]1CLKBA
1 CEAB	3	54	1 CEBA
GND [4	53	GND
1A1 🗌	5	52]1B1
1A2 🗌	6	51]1B2
V _{CC}	7	50	□ v _{cc}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND 🗌	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8 🗌	14	43	1B8
2A1	15	42	2B1
2A2 🗀	16	41] 2B2
2A3 [17	40] 2B3
GND [18	39	GND
2A4 🗌	19	38] 2B4
2A5 [20	37	2B5
2A6 [21	36	☐ 2B6
V _{CC} □	22	35	□ v _{cc}
2A7 [23	34] 2B7
2A8 🗌	24	33] 2B8
GND [25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA

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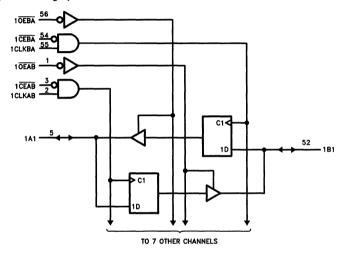


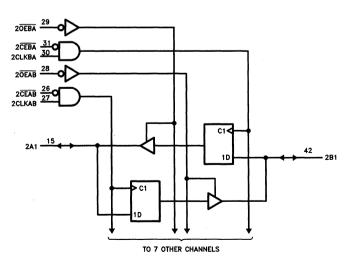
PRODUCT PREVIEW

The 74AC16952 and 74ACT16952 are packaged in Ti's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16952 has CMOS-compatible input thresholds. The 'ACT16952 has TTL-compatible input thresholds.

The 54AC16952 and 54ACT16952 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16952 and 74ACT16952 are characterized for operation from -40° C to 85°C.







16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0239-D3561, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged In Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16953 and 'ACT16953 are inverting 16-bit registered bus transceivers composed of two 8-bit transceiver sections with separate control signals.

Data flow in the A-to-B mode is controlled by output-enable (1OEAB and 2OEAB), clockenable (1CEAB and 2CEAB), and clock (1CLKAB and 2CLKAB) inputs. When 1CEAB (or 2CEAB) is high, data storage is inhibited and the registers retain their previous states. When 1CEAB (or 2CEAB) is low, the inverse of the data present at the corresponding A inputs is stored in the device on a low-to-high transition of 1CLKAB (or 2CLKAB), If 1OEAB (or 2OEAB) is also low, this stored data appears on the corresponding B outputs; if 10EAB (or 20EAB) is high, the corresponding B outputs are in the high-impedance state. 1OEAB (or 2OEAB) does not affect the operation of the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the highimpedance state.

Data flow from B to A is controlled by 10EBA and 20EBA, 1CEBA and 2CEBA, and 1CLKBA and 2CLKBA in a manner analogous to that described above for A-to-B data flow.

54AC16953, 54ACT16953 ... WD PACKAGE 74AC16953, 74ACT16953 ... DL PACKAGE (TOP VIEW)

1 OEAB	1	56	1 OEBA
1CLKAB	2	55	1CLKBA
1 CEAB	3	54	1 CEBA
GND [4	53	GND
1A1 🗌	5	52]1B1
1A2 🗌	6	51] 1 B 2
v _{cc} □	7	50	□v _{cc}
1A3 [8	49]1B3
1A4 [9	48]1B4
1A5 🗌	10	47]1B5
GND [11	46	GND
1A6 [12	45]1B6
1A7 🖺	13	44] 1B7
1A8 [14	43]1B8
2A1 [15	42] 2B1
2A2 [16	41] 2B2
2A3 🗌	17	40] 2B3
GND [18	39	GND
2A4 🗌	19	38	☐ 2B4
2A5 [20	37] 2B5
2A6 🗌	21	36	☐ 2B6
v _{cc} □	22	35	□ v _{cc}
2A7 🗌	23	34] 2B7
2A8 🗌	24	33] 2B8
GND [25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	20EBA
			•

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Texas Instruments

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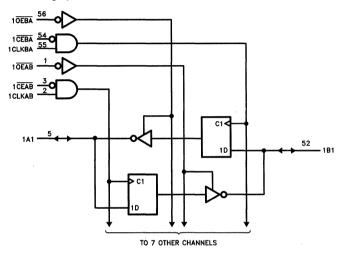
RODUCT PREVIE

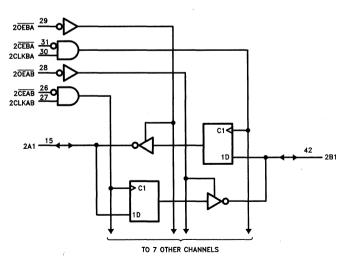
D3561, JUNE 1990-TI0239

The 74AC16953 and 74ACT16953 are packaged in Tl's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16953 has CMOS-compatible input thresholds. The 'ACT16953 has TTL-compatible input thresholds.

The 54AC16953 and 54ACT16953 are characterized over the full military temperature range of -55° C to 125°C. The 74AC16953 and 74ACT16953 are characterized for operation from -40° C to 85°C.





General Information	1
ACL LSI Products	2
ACL Widebus™ Products	3
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Clock Driver Products	6
ECL/TTL Translator Products	7
FIFO Products	8
Low-Impedance Line Driver Products	9
Memory Driver Products	10
SCOPE™ Testability Products	11
64BCT Series Products	12
Mechanical Data	13

High Speed Quad Transceiver

 Fully Compatible with IEEE Standard 896.1-1987 Futurebus Requirements

- Drives Load Impedances as Low as 10 Ω
- **High-Speed Advanced Low-Power Schottky** Circuits
- Low Power Dissipation . . . 81 mW Max per Channel
- High-Impedance P-N-P Inputs
- BTL™ Logic Level 1-V Bus Swing Reduces **Power Consumption**
- Low Bus-Port Capacitance
- Power-Up/Power-Down Protection (Glitch-Free)
- Open-Collector Driver Outputs Allows Wired-OR Connections
- Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference
- Designed to Be a Faster. Lower Power Functional Equivalent of National DS3893

description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This

transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

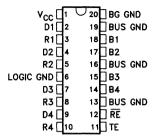
These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω .

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over VCC and temperature variations.

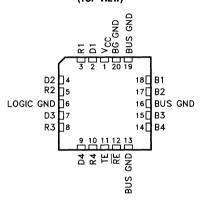
These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0°C to 70°C.

N PACKAGE (TOP VIEW)



FN CHIP CARRIER PACKAGE (TOP VIEW)



BTL is a trademark of National Semiconductor Corporation.



SN75ALS053 QUAD FUTUREBUS TRANSCEIVER

D3077, JANUARY 1988-REVISED SEPTEMBER 1989-TI0267

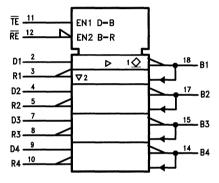
FUNCTION TABLE TRANSMIT/RECEIVE

CONT	ROLS	CHANNELS			
TE	RE	$D \rightarrow B$	$B \rightarrow R$		
L	L	D	R		
L	Н	D	D		
Н	L	Т	R		
Н	Н	Т	D		

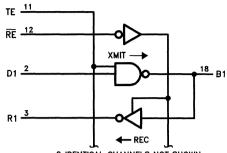
H = high level, L = low level, R = receive, T = transmit, D = disable

Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

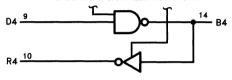
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

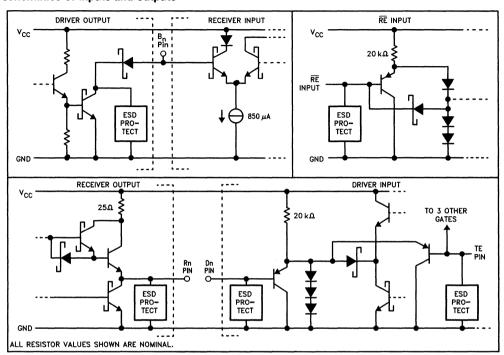


2 IDENTICAL CHANNELS NOT SHOWN



TI0267-D3077, JANUARY 1988-REVISED SEPTEMBER 1989

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, VCC (see Note 1)	6 V
Control input voltage	
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C
Case temperature for 10 seconds: FN package	260°C
Lead temperature 1,6mm (1/16 in.) from case for 10 seconds: N package	

NOTE 1: Voltage values are with respect to network ground terminal.

D3077, JANUARY 1988-REVISED SEPTEMBER 1989-TI0267

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	٧
VIH	High-level driver and control input voltage	2			٧
VIL	Low-level driver and control input voltage			0.8	V
	Bus termination voltage	1.9		2.1	٧
TA	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER		TES	ST CONDITIONS	MIN	TYP MAX	UNIT
VIK	Input clamp voltage at Dn, DE, or RE		I _I = -18 mA			- 1.5	V
٧ _T	Receiver input threshold at Bn				1.426	1.674	V
Vон	High-level output voltage at Rn		Bn at 1.2 V, IOH = -1 mA	RE at 0.8 V,	2.5		V
		Rn	Bn at 2 V, IOL = 20 mA	RE at 0.8 V,		0.5	
VOL	Low-level output voltage	Bn	Dn at 2.4 V, V _L = 2 V, See Figure 1	TE at 2.4 V, $R_L = 10 \Omega$,	0.75	1.2	\ \
		Dn, TE or RE	VI = VCC			40	
ΙΗ	High-level input current	Bn	V _I = 2 V, Dn at 0.8 V,	V _{CC} = 0 or 5.25 V, TE at 0.8 V,		100	μΑ
ΙĮL	Low-level input current at Dn, TE or RE		V _I = 0.4 V			- 400	μΑ
los	Short-circuit output current at Rn		Rn at 0 V, RE at 0.8 V	Bn at 1.2 V,	-70	- 200	mA
Icc	Supply curent					65	mA
Co(B)	Driver output capacitance		VCC = 5 V, TA	= 25°C		6.5	pF

TI0267--- D3077, JANUARY 1988--- REVISED SEPTEMBER 1989

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST	CONDITIONS	MIN	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	Dn	D-	TE at 3 V,	V _L = 2 V,	2	7	
tPHL	Propagation delay time high-to-low-level output	Dn	Bn	See Figure 2		2	7	ns
tPLH	Propagation delay time, low-to-high-level output	D-	D-	Dn at 3 V,	V _L = 2 V,	2	7	ns
tPHL	Propagation delay time high-to-low-level output	Dn	Bn	See Figure 2		2	7	113
tTLH	Transition time, low-to-high-level output	D-	Bn	TE at 3 V,	V _L = 2 V,	0.5	5	
tTHL	Transition time, high-to-low-level output	Dn	DΠ	See Figure 2		0.5	5	ns
	Skew between driver channels†	Dn	Bn	TE at 3 V,	V _L = 2 V		1	ns

receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output			DE HOOV TE HOOV ON E	2	8	
tPHL	Propagation delay time high-to-low-level output	Bn	Rn	RE at 0.3 V, TE at 0.3 V, See Figure 3	2	8	ns
tPLZ	Output disable time from low level	RE	Rn	Bn at 2 V, TE at 0.3 V, $V_L = 5$ V, $C_L = 5$ pF, $R_{L1} = 500 \Omega$, See Figure 4		6	ns
tPZL	Output enable time to low level	RE	Rn	Bn at 2 V, TE at 0.3 V, $V_L = 5$ V, $C_L = 5$ pF, $R_{L1} = 500 \Omega$, See Figure 4		12	ns
^t PHZ	Output disable time from high level	RE	Rn	Bn at 1 V, TE at 0.3 V, $V_L=0$, $C_L=5$ pF, $R_{L1}=500$ Ω , See Figure 4		6	ns
^t PZH	Output enable time to high level	RE	Rn	Bn at 1 V, TE at 0.3 V, $V_L=0$, $C_L=5$ pF, $R_{L1}=500$ Ω , See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	RE at 0.3 V, TE at 0.3 V		1	ns

[†] Skew is the difference between the propagation delay time (tpLH or tpHL) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both tpLH and tpHL.

PARAMETER MEASUREMENT INFORMATION

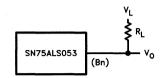
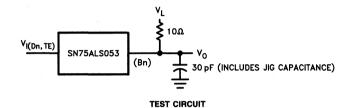
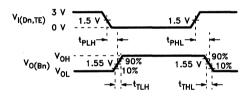


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



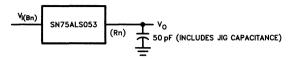


VOLTAGE WAVEFORMS

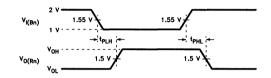
NOTE: $t_r = t_f \le 5$ ns from 10% to 90%

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



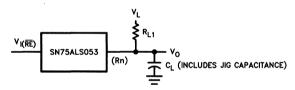
TEST CIRCUIT



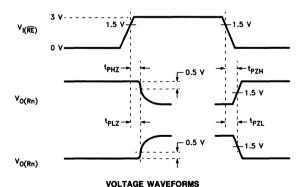
VOLTAGE WAVEFORMS

NOTE: $t_f = t_f \le 10$ ns from 10% to 90%

FIGURE 3. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT



NOTE: $t_r = t_f \le 5$ ns from 10% to 90%

FIGURE 4. PROPAGATION DELAY FROM RE TO Rn



SDAS171--TI0265---D3275, APRIL 1989

- Suitable for IEEE Standard 896 Applications[†]
- SN55ALS056 is an Octal Transceiver
- SN55ALS057 is a Quad Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 60 mW/Channel
 Max
- High-Impedance P-N-P Inputs
- BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption
- Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines
- Power-Up/Down Protection (Glitch-Free)
- Open-Collector Driver Outputs Allow Wired-OR Connections

description

The SN55ALS056 is an 8-channel, monolithic, high-speed, Advanced Low-Power Schottky device designed for 2-way data communication in a densely populated backplane. The SN55ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En). Both are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω . The receivers have internal low-pass filters to further improve noise immunity.

The SN55ALS056 and SN55ALS057 are characterized for operation from -55°C to 125°C.

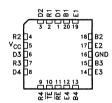
SN55ALS056 ... J OR W PACKAGE (TOP VIEW)

A1 [1	∪20]B1
A2 2	19 B2
A3 🛚 3	18 B3
A4	17 B4
V _{CC}	16 GNI
A5 ∏6	15 B5
A6 🔲 7	14∏B6
A7 []8	13 B7
A8 🔲 9	12 B8
CS 🗆 10	11 T/F

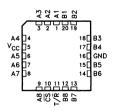
SN55ALS057 ... J OR W PACKAGE (TOP VIEW)

D1 🛮	1 0	20	B1
R1 [2	19]E1
D2 [3	18	B2
R2 🗌	4	17	E2
Vcc ☐	5	16] GND
D3 [6	15	B3
R3 🗌	7	14]E3
D4 🗌	8	13	B4
R4 🗌	9	12]E4
TE 🗆	10	11	RE

SN55ALS056 ... FK PACKAGE (TOP VIEW)



SN55ALS057 ... FK PACKAGE (TOP VIEW)

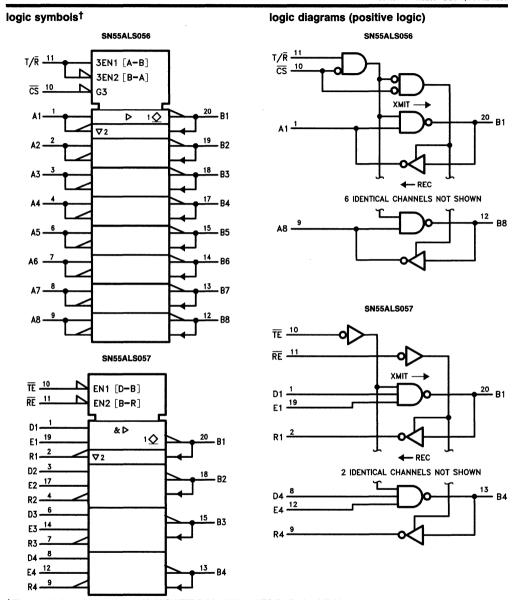


[†] The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range. BTL is a trademark of National Semiconductor Corporation.



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SDAS171-TI0265-D3275, APRIL 1989



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D3275, APRIL 1989-TI0265-SDAS171

SN55ALS056 FUNCTION TABLE TRANSMIT/RECEIVE

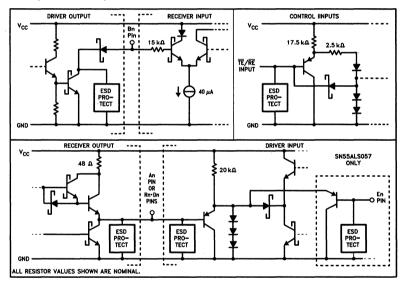
CONT	ROLS	CHANNELS
CS	T/R	A←→B
L	Н	$T(A \rightarrow B)$
L	L	$R(B \rightarrow A)$
н	X	D

SN55ALS057 FUNCTION TABLE TRANSMIT/RECEIVE

CC	NTRO	LS	CHAN	INELS
TE	RE	En	$D \rightarrow B$	$B \rightarrow R$
L	L	L	D	R
L	L	Н	Т	R
L	Н	L	D	D
L	н	Н	Т	D
Н	L	Х	D	R
Н	Н	Х	D	D
Н	H	X	T D	D R

H = high level, L = low-level, R = receive, T = transmit, D = disable, X = irrelevant Direction of data transmission is from An to Bn for the SN55ALS056 and from Dn to Bn for the SN55ALS057. Direction of data reception is from Bn to An for the SN55ALS056 and from Bn to Rn for the SN55ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



[†] Additional ESD protection is on the SN55ALS057, which has separate receiver output and driver input pins.



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	6 V
Control input voltage	5.5 V
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) 1375	mW c
Operating free-air temperature range -55°C to 1	25°C
Storage temperature range65°C to 1	50°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	100°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level driver and control input voltage	2			٧
VIL	Low-level driver and control input voltage			0.8	٧
	Bus termination voltage	1.9		2.1	٧
TA	Operating free-air temperature	-55		125	°C

^{2.} For operation above 25°C free-air temperature, derate to 275 mW at 125°C at the rate of 11.0 mW/°C.

D3275, APRIL 1989-TI0265-SDAS171

SN55ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER		TES	T CONDITIONS	MIN	TYP†	MAX	UNIT
VIK	Input clamp voltage at An	, T/R, or CS	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5	٧
\/	Desciver input threehold	-4 D	V _C C = 5 V,	T _A = 25°C	1.45		1.65	V
٧T	Receiver input threshold a	at bn	V _{CC} = 5 V,	$T_A = -55^{\circ}C \text{ to } 125^{\circ}C$	1.4		1.7	, ν
			$V_{CC} = 4.5 V$	Bn at 1.2 V,				
VOH	High-level output voltage	at An	CS at 0.8 V,	T/R at 0.8 V,	2.4			٧
			$IOH = -400 \mu A$					
			V _{CC} = 4.5 V,	Bn at 2V,				
		An	CS at 0.8 V,	T/\overline{R} at 0.8 V,			0.5	
	Lauretanal andre Arrabana		T/R at 0.8 V,	$I_{OL} = 16 mA$.,
VOL	Low-level output voltage	Bn	$V_{CC} = 4.5 V,$	An at 2 V,				V
			CS at 0.8 V,	T/\overline{R} at 2 V,	0.75		1.2	
			See Figure 1					
		An, T/R, or CS	$V_{I} = V_{CC} = 5.5 V$				40	
ЧН	High-level input current	D-	V _{CC} = 5.5 V,	V _I = 2 V,			100	μΑ
		Bn	An at 0.8 V,	T/R at 0.8 V			100	
IIL	Low-level input current at	An, T/R, or CS	$V_{CC} = 5.5 V$,	V _I = 0.4 V			-400	μΑ
			$V_{CC} = 5.5 V$,	An at 0 V,				
los	Short-circuit output current at An		Bn at 1.2 V,	CS at 0.8 V,	-35		-125	μΑ
			T/R at 0.8 V					
ICC	Supply current		V _{CC} = 5.5 V				85	mA
C _{o(B)}	Driver output capacitance)				4.5		pF

SN55ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER		TEST	CONDITIONS	MIN	TYP†	MAX	UNIT
VIK	input clamp voltage at Dn	, En, TE, or RE	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5	٧
\ <u></u>	D	D	$V_{CC} = 5 V$,	T _A = 25°C	1.45		1.65	V
٧T	Receiver input threshold a	at Bn	$V_{CC} = 5 V$,	T _A = -55°C to 125°C	1.4		1.7	٧
		-4 D-	$V_{CC} = 4.5 V$,	Bn at 1.2 V,	0.4			
VOH	High-level output voltage	at ri n	RE at 0.8 V,	$I_{OH} = -400 \mu A$	2.4			٧
	Low-level output voltage	D-	$V_{CC} = 4.5 V,$	Bn at 2 V,			0.5	
		Rn	RE at 0.8 V,	$I_{OL} = 16 mA$			0.5	
VOL			$V_{CC} = 4.5 V,$	Dn at 2 V,				٧
		Bn	En at 2 V,	TE at 0.8 V	0.75		1.2	
			See Figure 1		1			
		Dn, En, TE, or RE	$V_I = V_{CC} = 5.5 V$				40	
	High Investigated account		$V_{CC} = 5.5 V,$	V _I = 2 V,				
lН	High-level input current	Bn	Dn at 0.8 V,	En at 0.8 V,			100	μΑ
			TE at 0.8 V		1			
ll.	Low-level input current at	Dn, En, TE, or RE	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-400	μΑ
	Short-circuit output current at Rn		$V_{CC} = 5.5 V,$	Rn at 0 V,	-35		-125	
los			Bn at 1.2 V,	RE at 0.8 V				μΑ
ICC	Supply current		V _{CC} = 5.5 V				85	mA
C _{o(B)}	Driver output capacitance					4.5		pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND	ITIONS	TA [†]	MIN	TYP	MAX	UNIT		
tPLH	Propagation delay time, low- to high-level output			CS at 0.8 V,	T/R at 0.8 V,	25°C Full range			20 22			
tou	Propagation delay time,	Bn	An	V _L = 5 V, See Figure 4	S1 closed,	25°C			18	ns		
tPHL	high- to low-level output			Gee rigule 4		Full range			20			
^t PLZ	Output disable time from low level	CS		Bn at 2 V,	T/R at 0.8 V, S1 closed.	25°C Full range			20 22			
tPZL	Output enable time to low level	l CS	An	V _L = 5 V, See Figure 5	ST Closed,	25°C Full range			13	ns		
tPHZ	Output disable time from high level			Bn at 0.8 V, V _L = 0, S1 closed,	T/R at 0.8 V, See Figure 5				12 13			
tPZH	Output enable time to high-level	CS	An	All	Bn at 0.8 V, S1 open,	T/R at 0.8 V, See Figure 5	25°C Full range			14 22	ns	
tPLZ	Output disable time from low level	T/R		<u>CS</u> at 0.8V,	VC at 2 V,	25°C Full range			17 20			
tPZL	Output enable time to low level	178	An	An	ΑΠ	V _L = 5 V, See Figure 5	S1 closed,	25°C Full range			25 40	ns
tPHZ	Output disable time from high level	T/R		CS at 0.8 V, S1 closed,	V _L = 0 See Figure 5	25° Full range			12 13			
tPZH	Output enable time to high level	1/5	An	CS at 0.8 V, See Figure 5	S1 open,	25°C Full range			15 22	ns		
tw(NR)	Receiver noise rejection pulse duration	Bn	An or Rn	V _L = 5 V, See Figure 6	S1 closed,	25°C Full range	4 2			ns		

driver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND	ITIONS	TA [†]	MIN	TYP‡	MAX	UNIT			
4	Propagation delay time,					25°C			10				
tPLH	low- to high-level output			CS at 0.8 V,	T/R at 2 V,	Full range			40				
A	Propagation delay time,	An	Bn	V _L = 2 V,	See Figure 2	25°C			12	ns			
tPHL	high- to low-level output					Full range			15				
	Propagation delay time,					25°C			18				
tPLH	low- to high-level output	cs	~~	<u> </u>		_	An and T/R at 2 V,	$V_L = 2 V$,	Full range			30	
	Propagation delay time,	CS	Bn	See Figure 2		25°C			20	ns			
tPHL	high- to low-level output					Full range			22				
	Propagation delay time,					25°C			18				
tPLH	low- to high-level output	- /E	_	CS at 0.8 V,	$V_L = 2 V$,	Full range			37				
	Propagation delay time,	T/R	Bn	See Figure 3	_	25°C			18	ns			
tPHL	high- to low-level output			J		Full range			21				
	Transition time,					25°C	1	3	8	************			
†TLH	low- to high-level output		_	CS at 0.8 V,	T/R at 2 V,	Full range	1		33				
	Transition time,	An	Bn	V _L = 2 V,	See Figure 2	25°C	1	3	10	ns			
tTHL	high- to low-level output				-	Full range	1		13				

[†] Full range is -55°C to 125°C.



[‡] Typical values are at $V_{CC} = 5 \text{ V}$.

D3275, APRIL 1989-TI0265-SDAS171

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	ONDITIONS	T _A †	MIN	MAX	UNIT	
	Propagation delay time,			RE at 0.8 V,	TE at 2 V.	25°C		20		
tPLH	low- to high-level output	n	D-		•	Full range		22		
	Propagation delay time,	Bn		V _L = 5 V,	S1 closed,	25°C		18	ns	
tPHL	high- to low-level output			See Figure 4	4	Full range		20		
	Output disable time		RE Rn V	D101/	TE -+ 0.14	25°C		15		
tPLZ	from low level	55			Bn at 2 V,	TE at 2 V,	Full range		17	
	Output enable time	HE		V _L = 5 V, See Figure 5	S1 closed,	25°C		13	ns	
tPZL	to low level					Full range		14		
	Output disable time			Bn at 0.8 V, TE	at 2 V, V _L = 0,	25°C		12		
tPHZ	from high level		_	S1 closed,	See Figure 5	Full range		13		
	Output enable time	t enable time	Rn	Bn at 0.8 V,	TE at 2 V,	25°C		14	ns	
^t PZH	to high-level			S1 closed,	See Figure 5	Full range		15		
	Receiver noise rejection	_	_	V _L = 5 V,	S1 closed,	25°C	4			
tw(NR)	pulse duration	Bn	Rn	See Figure 6		Full range	2		ns	

driver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND	OITIONS	T _A †	MIN	TYP‡	MAX	UNIT
	Propagation delay time,					25°C			10	
tPLH	low- to high-level output	Dn	Bn	TE at 0.8 V,	RE at 2 V,	Full range			27	
	Propagation delay time,	or En	БП	$V_L = 2 V$	See Figure 2	25°C			12	ns
tPHL.	high- to low-level output					Full range			15	
•	Propagation delay time,					25°C			10	
tPLH	low- to high-level output		_	Dn, En, RE at 2 V,	$V_L = 2 V$,	Full range			27	
	Propagation delay time,	TE	Bn	See Figure 2		25°C			17	ns
tPHL	high- to low-level output					Full range			19	
	Transition time,					25°C	1	3	8	
tTLH	low- to high-level output	Dn		RE at 2 V,	$V_L = 2 V$,	Full range	1		33	
	Transition time,	or En	Bn See F	See Figure 2		25°C	1	3	10	ns
THL	high- to low-level output					Full range	1		13	

[‡] Typical values are at V_{CC} = 5 V.

driver plus receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDIT	TIONS	TA [†]	MIN	MAX	UNIT
	Propagation delay time,			RE at 0.8 V.	TE at 0.8 V.	25°C		25	
tPLH	low- to high-level output	D	n.			Full range		35	
	Propagation delay time,	Dn	Rn	V _L = 2 V,	See Figure 7	25°C		25	ns
tPHL.	high- to low-level output			(Both loads are used)		Full range		35	

[‡] Full range is -55°C to 125°C.



PARAMETER MEASUREMENT INFORMATION

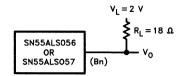
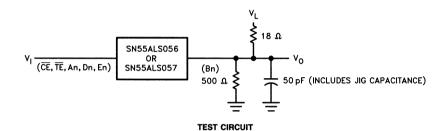
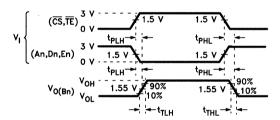


FIGURE 1. TEST CIRCUIT FOR DRIVER LOW-LEVEL OUTPUT VOLTAGE



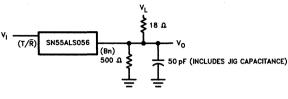


VOLTAGE WAVEFORMS

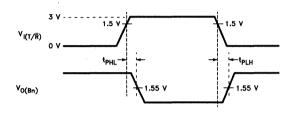
NOTE: $t_{f} = t_{f} \le 5$ ns from 10% to 90%.

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



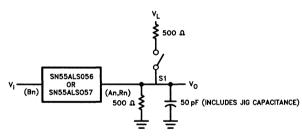
TEST CIRCUIT



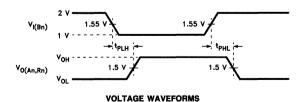
VOLTAGE WAVEFORMS

NOTE: $t_f = t_f \le 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/R TO Bn



TEST CIRCUIT

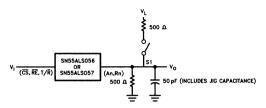


NOTE: $t_r = t_f \le 10 \text{ ns from } 10\% \text{ to } 90\%.$

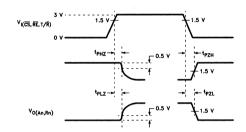
FIGURE 4. RECEIVER PROPAGATION DELAY TIMES



PARAMETER MEASUREMENT INFORMATION



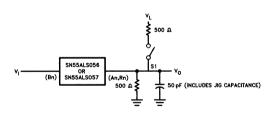
TEST CIRCUIT



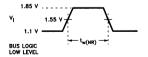
VOLTAGE WAVEFORMS

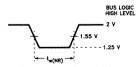
NOTE: $t_r = t_f \le 5$ ns from 10% to 90%.

FIGURE 5. PROPAGATION DELAY FROM CS OR T/R TO An OR FROM RE TO Rn



TEST CIRCUIT





t_W is increased until the output voltage fall just reaches 2.0 V. t_W is increased until the output voltage rise just reaches 0.8 V. **VOLTAGE WAVEFORMS**

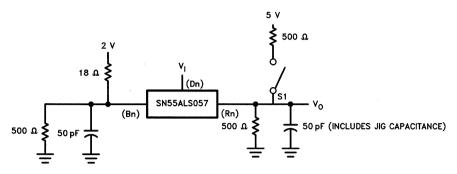
NOTE: $t_r = t_f \le 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY

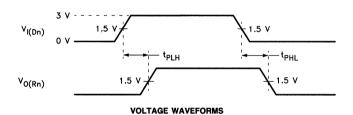


D3275, APRIL 1989-TI0265-SDAS171

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



NOTE: $t_f = t_f \le 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

TI0266--- D3025, AUGUST 1987--- REVISED JUNE 1990

SN75ALS056 is an Octal Transceiver	SN75ALS056
SN75ALS057 is a Quad Transceiver	DW OR N PACKAGE (TOP VIEW)
 High-Speed Advanced Low-Power Schottky Circuitry 	A1 1 20 B1 A2 2 19 B2
 Low Power Dissipation 52.5 mW/Channel Max 	A2 2 19 182 A3 3 18 183 A4 4 17 184
High-Impedance P-N-P Inputs	V _{CC}
 Logic Level 1-V Bus Swing Reduces Power Consumption 	A5
 Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines 	A8 9 12 B8 CS 10 11 T/R
 Power-Up/Down Protection (Glitch Free) 	
 Open-Collector Driver Outputs Allow Wired-OR Connections 	SN75ALS057 DW OR N PACKAGE (TOP VIEW)
 Designed to Be a Faster, Lower Power Functional Equivalent of National DS3896, DS3897 	D1 1 20 B1 R1 2 19 E1 D2 3 18 B2
description	R2 ☐4 17 ☐ E2
The SN75ALS056 is an 8-channel, monolithic, high-speed, advanced low-power Schottky device designed for 2-way data communication in a densely populated backplane. The SN75ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable	V _{CC}

These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω .

The receivers have internal low-pass filters to further improve noise immunity.

The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

for each driver (En).

D3025, AUGUST 1987-REVISED JUNE 1990-TI0266

logic symbols† logic diagrams (positive logic) SN75ALS056 **SN75ALS056** $T/\bar{R} \frac{11}{\bar{R}}$ 3 EN1 [A-B] CS 10 3 EN2 [B-A] XMIT -20 B1 10 Þ **∇**2 - B3 - REC 17_B4 6 IDENTICAL CHANNELS NOT SHOWN A8 _9 - B5 - B6 SN75ALS057 SN75ALS057 TE 10 TE 10 EN1 [D-B] EN2 [B-R] XMIT -& D E1-19 20 B1 10 E1 19 **▽**2 R1 -2 **←** REC 2 IDENTICAL CHANNELS NOT SHOWN E3 14 E4 12 - B4 R4 _ 9

[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



TI0266--D3025, AUGUST 1987--REVISED JUNE 1990

SN75ALS056 FUNCTION TABLE TRANSMIT/RECEIVE

CONT	ROLS	CHANNELS
CS	T/R	A←→B
L	Н	$T(A \rightarrow B)$
L	L	$R (B \rightarrow A)$
н	X	ם

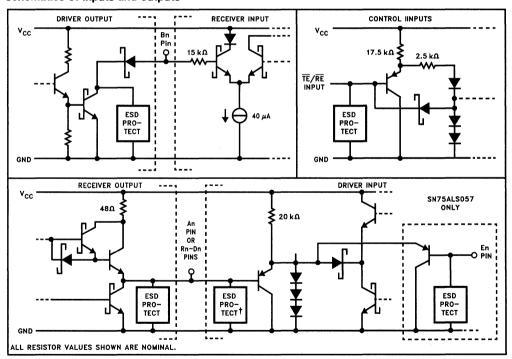
SN75ALS057 FUNCTION TABLE TRANSMIT/RECEIVE

CC	NTRO	LS	CHAN	INELS
TE	RE	En	$D \rightarrow B$	$B \rightarrow R$
L	L	L	D	R
L	L	Н	Т	R
L	Н	L	D	D
L	Н	Н	T	D
Н	L	Х	D	R
н	Н	Х	D	D

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



[†] Additional ESD protection is on the SN75ALS057 only, which has separate receiver output and driver input pins.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	6 V
Control input voltage	
Driver input voltage	5.5 V
Driver output voltage	2.5 V
Receiver input voltage	2.5 V
Receiver output voltage	5.5 V
Continuous total power dissipation	. See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C
Lead temperature 1.6 mm (1/4 inch) from case for 10 seconds	

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.5	٧
VIH	High-level driver and control input voltage	2			٧
VIL	Low-level driver and control input voltage			0.8	٧
	Bus termination voltage	1.9		2.1	٧
TA	Operating free-air temperature	0		70	င့

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SN75ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER			TEST CONDITIONS	MIN	TYP† MAX	UNIT
VIK	Input clamp voltage at An,	T/R, or CS	$I_{I} = -18 \text{ mA}$			-1.5	V
٧ _T	Receiver input threshold a	t Bn			1.426	1.674	mV
VOH	High-level output voltage a	ıt An	Bn at 1.2 V,	CS at 0.8 V,	2.4		v
VOH	nigh-level output voltage a	II AII	T/R at 0.8 V,	$IOH = -400 \mu A$	2.4		'
			Bn at 2 V,	CS at 0.8 V,		0.5	
		An	T/R at 0.8 V,	IOL = 16 mA		0.5	
VOL	Low-level output voltage	Bn	An at 2 V,	CS at 0.8 V,] v
			T/R at 2 V,	$V_L = 2 V$,	0.75	1.2	Į
			$R_L = 18.5 \Omega$,	See Figure 1			
		An, T/R, or CS	VI = VCC			40	
ΉН	High-level input current	Bn	V _I = 2 V,	V _{CC} = 0 V or 5.25 V,			μΑ
		БП	An at 0.8 V,	T/R at 0.8 V		100	
IIL	Low-level input current at /	An, T/R, or CS	V _I = 0.4 V			400	μΑ
		4 4	An at 0 V,	Bn at 1.2 V,	40	400	
IOS Short-circuit output current		tat An	CS at 0.8 V,	T/R at 0.8 V	-40	-120	mA
Icc	Supply current					75	mA
C _{o(B)}	Driver output capacitance					4.5	pF

SN75ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

	PARAMETER		TES	T CONDITIONS	MIN	TYP† MAX	UNIT
VIK	Input clamp voltage at Dn	, En, TE, or RE	I _I = -18 mA			-1.5	V
VT	Receiver input threshold a	at Bn			1426	1674	mV
VOH	High-level output voltage	at Rn	Bn at 1.2 V, I _{OH} = -400 μA	RE at 0.8 V,	2.4		٧
		Rn	Bn at 2 V, IOL = 16 mA	RE at 0.8 V,		0.5	
VOL	Low-level output voltage	Bn	Dn at 2 V, TE at 0.8 V, R _L = 18.5 Ω,	En at 2 V, V _L = 2 V, See Figure 1	0.75	1.2	٧
		Dn, En, TE, or RE	VI = VCC			40	
۱н	High-level input current	Bn	V _I = 2 V, Dn at 0.8 V, TE at 0.8 V	V _{CC} = 0 V or 5.25 V, En at 0.8 V,		100	μΑ
ΙĮL	Low-level input current at	Dn, En, TE, or RE	V _I = 0.4 V	<u></u>		-400	μΑ
los	Short-circuit output current at Rn		Rn at 0, RE at 0.8 V	Bn at 1.2 V,	-40	- 120	mA
ICC	Supply current					40	mA
C _{o(B)}	Driver output capacitance					4.5	pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS056 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVER

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switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT		
tPLH	Propagation delay time, low-to-high-level output	An	Bn	CL at 0.8 V,	T∕R at 2 V,			19	ns		
tPHL	Propagation delay time, high-to-low-level output		DII	V _L = 2 V,	See Figure 2			18	lis		
tPLH	Propagation delay time low-to-high-level output		CS	D-	An and T/R at 2 V,	V _L = 2 V,			24		
tPHL	Propagation delay time, high-to-low-level output		Bn	See Figure 2				20	ns		
tPLH	Propagation delay time, low-to-high-level output	T/R	T/R	T/D	Bn	VI(An, Bn) = 5 V,	CS at 0.8 V,			25	
tPHL	Propagation delay time, high-to-low-level output			3 511	R_{L2} not connected, $R_{L1} = 18 \Omega$,	C _L = 30 pF, See Figure 3			35	ns	
tTLH	Transition time, low-to-high-level output			_		CS at 0.8 V,	T/R at 2 V,	1	3	11	
tTHL	Transition time, high-to-low-level output	An	Bn	V _L = 2 V,	See Figure 2	1	3	6	ns		

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS056 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVER

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN MAX	UNIT
^t PLH	Propagation delay time, low-to-high-level output	D-		20 0 0 V T/D 0 0 V C 5: 4	18	
^t PHL	Propagation delay time, high-to-low-level output	Bn	An	CS at 0.8 V, T/R at 0.8 V, See Figure 4	18	ns
^t PLZ	Output disable time from low level	cs	An	Bn at 2 V, T/ \overline{R} at 0.8 V, C _L = 5 pF, V _L = 5 V, R _{L1} = 390 Ω , R _{L2} not connected, See Figure 5	18	ns
^t PZL	Output enable time to low level	CS	An	Bn at 2 V, T/ \overline{R} at 0.8 V, C _L = 30 pF, V _L = 5 V, R _{L1} = 390 Ω, R _{L2} = 1.6 kΩ, See Figure 5	15	ns
^t PHZ	Output disable time from high level	CS	An	Bn at 0.8 V, T/\overline{R} at 0.8 V, $C_L = 5$ pF, V _L = 0, R _{L1} = 390 Ω , R _{L2} not connected, See Figure 5	8	ns
^t PZH	Output enable time to high level	CS	An	Bn at 0.8 V, T/\overline{R} at 0.8 V, $C_L=30$ pF, $V_L=0$, R_{L1} not connected, $R_{L2}=1.6$ k Ω , See Figure 5	17	ns
^t PLZ	Output disable time from low level	T/R	An	$\overline{\text{CS}}$ at 0.8 V, V _I (An, Bn) = 2 V, V _L = 5 V, R _{L1} = 390 Ω , R _{L2} not connected, C _L = 5 pF, See Figure 3	20	ns
^t PZL	Output enable time to low level	T/R	An	$\overline{\text{CS}}$ at 0.8 V, V _I (An, Bn) = 2 V, V _L = 5 V, R _{L1} = 390 Ω , R _{L2} = 1.6 k Ω , C _L = 30 pF, See Figure 3	40	ns
^t PHZ	Output disable time from high level	T/R	An	$\overline{\text{CS}}$ at 0.8 V, V _I (An, Bn) = 0, V _L = 0, R _{L1} = 390 Ω , R _{L2} not connected, C _L = 5 pF, See Figure 3	17	ns
^t PZH	Output enable time to high level	T/R	An	$\overline{\text{CS}}$ at 0.8 V, V _I (An, Bn) = 0, V _L = 0, R _{L1} not connected, R _{L2} = 1.6 k Ω , C _L = 30 pF, See Figure 3	15	ns
tw(NR)	Receiver noise rejection pulse duration	Bn	An or Rn	CS at 0.8 V, T/R at 0.8 V, See Figure 6	3	ns

SN75ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVER

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switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT		
tPLH	Propagation delay time, low-to-high-level output	D=	D-	TE at 0.8 V,	RE at 2 V,			19			
tPHL	Propagation delay time, high-to-low-level output	Dn or En	Bn	$V_L = 2 V$,	See Figure 2			18	ns		
tPLH	Propagation delay time, low-to-high-level output			TE	D-	Dn, En, RE at 2 V,	V _L = 2 V,			24	
^t PHL	Propagation delay time, high-to-low-level output	,	Bn	$R_{L1} = 18 \Omega$	See Figure 2			20	ns		
tтьн	Transition time, low-to-high-level output		Bn	RE at 2 V,	V _L = 2 V,	1	3	11			
THL	Transition time, high-to-low-level output	Dn or En	Bu	TE at 0.8 V,	See Figure 2	1	3	6	ns		

receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output					18	
tPHL	Propagation delay time, high-to-low-level output	Bn·	Rn	RE at 0.9 V, TE at 2 V,	See Figure 4	18	ns
^t PLZ	Output disable time from low level	RE	Rn	Bn at 2 V, \overline{TE} at 2 V, $C_L = 5 \text{ pF}$, $R_{L1} = 390 \Omega$, R_{L2} not connected,	$V_L = 5 V$, See Figure 5	18	ns
tPZL	Output enable time to low level	RE	Rn	Bn at 2 V, \overrightarrow{TE} at 2 V, $C_L = 30$ pF, $R_{L1} = 390 \Omega$, See Figure 5	$V_L = 5 V$, $R_{L2} 1.6 k\Omega$,	15	ns
^t PHZ	Output disable time from high level	RE	Rn	Bn at 0.8 V, $\overline{\text{TE}}$ at 2 V, $C_L = 5 \text{ pF}$, $R_{L1} = 390 \Omega$, R_{L2} not connected,	$V_L = 0$, See Figure 5	17	ns
^t PZH	Output enable time to high level	RE	Rn	Bn at 0.8 V, $\overline{\text{TE}}$ at 2 V, $C_L = 30 \text{ pF}$, R_{L1} not connected, $R_{L2} = 1.6 \text{ k}\Omega$,	$V_L = 0$, See Figure 5	17	ns
tw(NR)	Receiver noise rejection pulse duration	Bn	Cn	TE at 2.0 V, RE at 0.8 V, See Figure 6		3	ns

driver plus receiver

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN MAX	UNIT
	Propagation delay time,				40	
†PLH	low-to-high-level output	Dn	Rn	RE at 0.8 V, TE at 0.8 V, See Figure 7	40	1
	Propagation delay time,	Un		RE at 0.8 V, TE at 0.8 V, See Figure 7	40	ns
tPHL.	high-to-low-level output				40	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.



PARAMETER MEASUREMENT INFORMATION

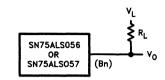
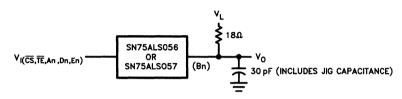
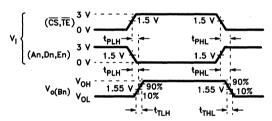


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



TEST CIRCUIT



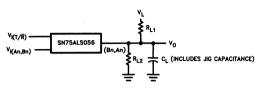
VOLTAGE WAVEFORMS

NOTE: $t_{\Gamma} = t_{f} \le 5$ ns from 10% to 90%.

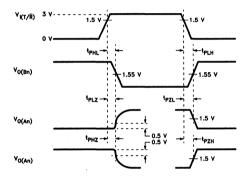
FIGURE 2. DRIVER PROPAGATION DELAY TIMES

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PARAMETER MEASUREMENT INFORMATION



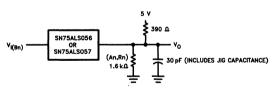
TEST CIRCUIT



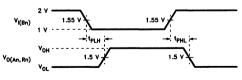
VOLTAGE WAVEFORMS

NOTE: $t_{\Gamma} = t_{f} \le 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/R TO An OR Bn



TEST CIRCUIT



VOLTAGE WAVEFORMS

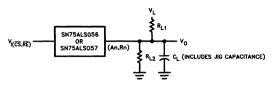
NOTE: $t_f = t_f \le 10$ ns from 10% to 90%.

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

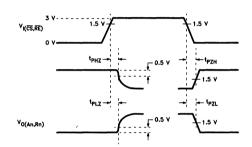


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PARAMETER MEASUREMENT INFORMATION



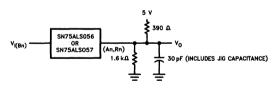
TEST CIRCUIT



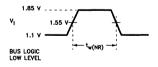
VOLTAGE WAVEFORMS

NOTE: $t_{\Gamma} = t_{f} \le 5$ ns from 10% to 90%.

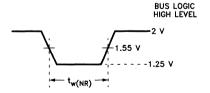
FIGURE 5. PROPAGATION DELAY FROM CS TO An OR RE TO Rn



TEST CIRCUIT



tw is increased until the output voltage fall just reaches 2 V.



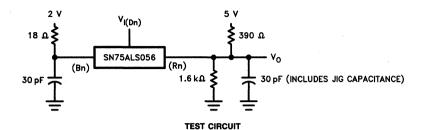
 t_{W} is increased until the output voltage rise just reaches 0.8 V. VOLTAGE WAVEFORMS

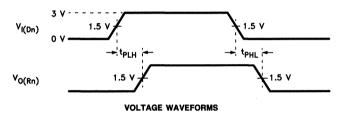
NOTE: $t_r = t_f \le 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY



PARAMETER MEASUREMENT INFORMATION





NOTE: $t_r = t_f \le 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

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 Supports Draft Futurebus + Standard (IEEE P896.1, 90 July 16) and Pi-Bus Standard 	SN54BCT979 WD PACKAGE SN74BCT979 DL PACKAGE
 Packaged in Plastic Shrink Small-Outline 300-mil Packages (SSOP) and Very Small Outline Flatpack (VSOW) 	V _{CC} 1 48 GBA AIO 2 47 LEAB
Open-Collector B Port Drives Load Impedances as Low as 10 Ω	AO0[] 3 46] B0 Al1 [] 4 45] GND
 BTL Logic Level 1-V Bus Swing Reduces Power Consumption 	AO1 [] 5 44]] GND GND [] 6 49]] B1 AI2 [] 7 42]] ERRA
 Latchable Transceiver With Output Sink of 24 mA at the A Bus and 100 mA at the B Bus 	AO2 8 41 B2 AI3 9 40 GND AO3 10 39 GND
Option to Generate and Check Parity or Feed-Through Data/Parity in Directions A-to-B or B-to-A	AI4 11 38 B3 GND 12 37 ODD/EVEN AO4 13 36 B4
Independent Latch Enables for A-to-B and B-to-A Directions	AI5[] 14 35]] SEL AO5[] 15 34]] B5 AI6[] 16 33]] GND
ODD/EVEN Parity-Select Pin	AO6 17 32 GND
 ERRA and ERRB Output Pins for Parity Checking 	GND[] 18 31] B6 AI7 [] 19 30] ERRB AO7 [] 20 29 [] B7
Ability to Simultaneously Generate and	APARI 21 28 GND

description

Check Parity

The 'BCT979 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data bus in either direction. It has a specified currentsinking capability of 24 mA at the A-bus and 100 mA at the B-bus.

ESD Protection Exceeds 2000 V Per

MIL-STD 883C, Method 3015

The 'BCT979 features independent latch enables (LEAB and LEBA) for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

When communication between buses occurs, parity is generated and passed on to either bus as APAR or BPAR. Error detection of the parity generated from Al0-Al7 and B0-B7 can be checked by ERRA and ERRB, provided that LEAB and LEBA are high and the mode select SEL is low. If SEL is high, the communication between buses is in a feed-through mode where parity is still generated and checked as ERRA and ERRB. BPAR. Error detection of the parity generated from Al0-Al7 and B0-B7 can be checked by ERRA and



GND

BPAR

GAB

27

26

APAROII 22

LEBA

V_{CC} 23

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The 'BCT979 features open-collector driver outputs at the B port (B0-B7 and BPAR) with a series Schottky diode to reduce capacitive loading to the bus. If a 2-V pullup is used on the bus, the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω .

The transceiver has a precision threshold set by an internal bandgap reference to give accurate input thresholds over Voc and temperature variations.

This transceiver is compatible with Backplane Transceiver Logic (BTL) technology at significantly reduced power dissipation per channel.

The SN54BCT979 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT979 is characterized for operation from 0°C to 70°C.

PARITY FUNCTION TABLE (SEE NOTE 1)

	INPUTS†	OUTI	OUTPUTS			
ODD/EVEN	Σ of inputs AO0-AO7 = H	APARI	BPAR‡	ERRA		
L	0, 2, 4, 6, 8	L	L	Н		
L	1, 3, 5, 7	L	н	L		
L	0, 2, 4, 6, 8	Н	L	L		
L	1, 3, 5, 7	Н	н	н		
н	0, 2, 4, 6, 8	L	н	L		
н	1, 3, 5, 7	L	L	н		
н	0, 2, 4, 6, 8	Н	н	н		
н	1, 3, 5, 7	Н	L	L		

[†] If LEAB = H, current Al0-Al7 and APARI data is used. If LEAB = L, latched Al0-Al7 and APARI data is used.

NOTE 1: Parity functions for the A bus are shown. Parity functions for the B bus are similar, but use B0-B7 and BPAR as inputs and APARO and ERRB as outputs.

FUNCTION TABLE

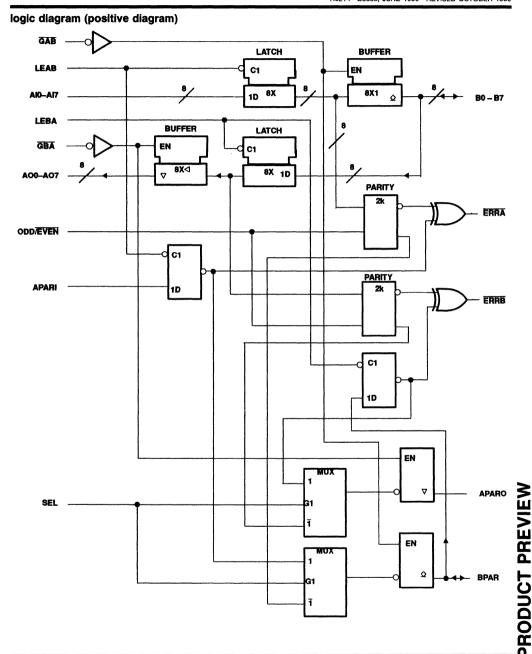
	CO	NTROL IN	PUTS	···	OPPRITORS
GAB	GBA	SEL	LEAB	LEBA	OPERATION§
Н	Н	X	Х	х	Isolation. AO0-AO7/APARO are in the high impedance state, and B0-B7/BPAR are high.
Н	L	L	×	н	B to A mode parity is generated from B0-B7 data and output on APARO, and is checked against BPAR with the result output on ERRB.
Н	L	L	X	L	B to A mode parity is generated from latched B0-B7 data and output on APARO, and is checked against BPAR with the result output on ERRB.
Н	L	н	X	н	B to A mode BPAR is output on APARO. Parity is generated from B0- B7 data, checked against BPAR, and output on ERRB.
Н	L	Н	X	L	B to A mode BPAR is output on APARO. Parity is generated from latched B0-B7 data, checked against BPARO, and output on ERRB.
L	Н	L	н	x	A to B mode parity is generated from Al0-Al7 data an <u>d outp</u> ut on BPAR, and is checked against APARI and output on ERRA.
L	н	L	L	X	A to B mode parity is generated from latched Al0-Al7 data and output on BPAR, and is checked against APARI and output on ERRA.
L	Н	Н	н	x	A to B mode APARI is output on BPAR. Parity is generated from AI0- AI7 data, checked against APARI, and output on ERRA.
L	Н	H	L	x	A to b mode APARI is output on BPAR. Parity is generated from latched AI0-AI7 data, checked against APARI, and output on ERRA.
L	L	Х	X	x	AO0-AO7/APARO and B0-B7/BPAR are active (high or low logic level).

[§] Parity is generated from Al0-Al7 and from B0-B7 based on the level present at ODD/EVEN. Parity is checked (AO0-AO7 against APARI and B0-B7 against BPAR) based on the level present at ODD/EVEN. See parity function table.



[‡] This is the value of BPAR if SEL = L. If SEL = H, BPAR = APARI.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	−0.5 V to 7 V
Input voltage range: B0-B7, BPAR	0.5 V to 5.5 V
Other Inputs	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	0.5 V to 7 V
Voltage applied to any output in the high state	0.5 V to VCC
Operating free-air temperature range: SN54BCT979	55°C to 125°C
SN74BCT979	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN	54BCT9	79	SN	74BCT9	79	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
V	High level inner truelte an	B0-B7, BPAR	1.6			1.6			V
VIH F	High-level input voltage	Other inputs	2			2			٧
V.	Law laveliand value	B0-B7, BPAR			1.475			1.475	
VIL	Low-level input voltage	Other inputs			0.8			0.8	V
VOH	High-level output voltage	B0-B7, BPAR			2			2	٧
^I IK	Input clamp current				-18			-18	mA
	18-b lead a standard and the	AO0-AO7, APARO,							
ЮН	High-level output current	ERRA, ERRB	-3					-3	mA
		AO0-AO7, APARO,			24		_		
lOL	Low-level output current	ERRA, ERRB	j					24	mA
		B0-B7, BPAR			100			100	mA
TA	Operating free-air temperature		-55		125	0		70	°C



TI0214--D3588, JUNE 1990--REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST SOURITIONS	SN54BCT979			SN	74BCT9	79	UNIT	
	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	MIN	TYP	MAX	UNII	
VIK		$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$			-1.2			-1.2	V	
ЮН	B0-B7, BPAR	V _{CC} = 5.5 V, V _{OH} = 2 V			100			100	μΑ	
	AO0-AO7, APARO,	$V_{CC} = 4.5 \text{ V, } I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		V	
VOH	ERRA, ERRB	$V_{CC} = 4.5 \text{ V, I}_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		V	
	AO0-AO7, APARO,	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.3	0.5				V	
V	ERRA, ERRB	V _{CC} = 4.5 V, I _{OL} = 24 mA					0.35	0.9	V	
VOL	DO DZ DDAD	V _{CC} = 4.5 V, I _{OL} = 80 mA	0.75		1.1	0.75		1.1	٧	
	B0-B7, BPAR	V _{CC} = 4.5 V, I _{OL} = 100 mA			1.15			1.15	V	
	LEAB, LEBA, GAB, GBA, SEL	V 0 V: - 7V			100			100	μΑ	
lį	ODD/EVEN, AI0-AI7, APARI	$V_{CC} = 0, V_{I} = 7 V$			100			100		
	B0-B7, BPAR	V _{CC} = 5.5 V, V _I = 5.5 V			1			1	mA	
	LEAB, LEBA, GAB, GBA, SEL	V F F V V: - 0.7 V	20		00			20	4	
lін	ODD/EVEN, AI0-AI7, APARI	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$					20	μΑ		
	B0-B7‡, BPAR	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.1 \text{ V}$			100			100	μΑ	
	LEAB, LEBA, GAB, GBA, SEL	V F E V V: - 0 E V	-c		0.6			0.0		
ŊĹ	ODD/EVEN, AI0-AI7, APARI	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$			-0.6			-0.6	μΑ	
	B0-B7‡	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.3 \text{ V}$			-100			- 100		
lozh	AO0-AO7, APARO	$V_{CC} = 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$			50			50	μΑ	
lozl	AO0-AO7, APARO	$V_{CC} = 5.5 \text{ V}, V_{O} = 0.5 \text{ V}$			-50			-50	μΑ	
los§	AO0-AO7, APARO	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$	-60		-150	-60		- 150	mA	
	Outputs low	$V_{CC} = 5.5 \text{ V, } I_{O} = 0$					69			
ICC	Outputs high	V _{CC} = 5.5 V, I _O = 0					17		mA	
	Outputs disabled	V _{CC} = 5.5 V, I _O = 0					21			

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements

				.5 V to 5.5 V, IN to MAX§	UNIT
			SN54BCT979	SN74BCT979]
			MIN MAX	MIN MAX	1
		Al0-Al7, APARI before LEAB↑	3	3	
t _{su}	Setup time	B0-B7, BPAR before LEBA ↑	5	5	ns
	11.140	AI0-AI7, APARI after LEAB ↑	1	1	
th	Hold time	B0-B7, BPAR after LEBA↑	0	0	ns
	Dulas dusation	LEAB high	5	5	
tw	Pulse duration	LEBA high	5	5	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW



[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

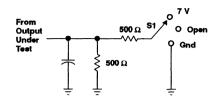
D3588, JUNE 1990-REVISED OCTOBER 1990-TI0214

switching characteristics (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 5 V, T _A = 25°C		I.5 V to 5.5 V, IIN to MAX†		
	(INPUT)	(OUTPUT)	'BCT979	SN54BCT97		UNI	
	(5.,	(66.1.61,	MIN TYP MAX				
tPLH			5.6	WINTER WINTER	WAX		
tPHL	⊢ AI	В	5.8	+	+	ns	
tPLH	-		5.6	+	+		
tPHL	⊢В	AO	5.8			ns	
tPLH			5.8				
tPHL	APARI	BPAR	6.1			n:	
tPLH			5.8				
tPHL	BPAR	APARO	6.1			n	
tPLH			8.1				
tPHL	AI, APARI	ERRA	8.1			n	
tPLH			8.1				
tPHL	B, BPAR	ERRB	8.1			n	
tPLH			10			 	
tPHL	ODD/EVEN	ERRA	10.7			n	
tPLH		-	10				
tPHL		ODD/EVEN ERRB		-		n	
tPLH			10.7	+			
tPHL	ODD/EVEN	APAR	10.7			n	
tPLH	ODD/EVEN		10.2	-			
tPHL		BPAR	10.7			n	
	LH SEL		6.3			ns	
tPHL		APARO, BPAR	5.8				
tPLH			6.6	 	 		
tPHL	LEAB	B, BPAR	6.3		+	ns	
tPLH	 		6.6	-	 		
tPHL	LEBA	AO, APARO	6.3	+	-	n	
tPLH	LEAB	ERRA	6.6		-	-	
tPHL	LEAB	ERRA	6.3	-		1	
tPLH	LEBA	ERRB	6.6				
tPHL	LEBA	ERRB	6.3			1	
tPZH			7.2				
tPZL	GBA	AO, APARO	9.5			n	
tPZH			7.2			<u> </u>	
tPZL	GAB	B, BPAR	9.5			j n	
tPHZ			6.8			<u> </u>	
tPLZ	- GBA	AO, APARO	5.5			r	
			6.8				
tPHZ	PHZ PLZ	AO, APARO	5.5			- n	

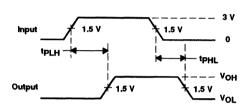


PARAMETER MEASUREMENT INFORMATION

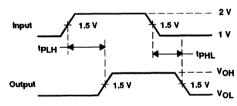


LOAD CIRCUIT FOR A OUTPUTS

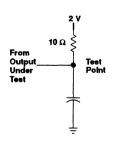
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	7 V
tPHZ/tPZH	GND



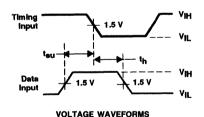
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES (A PORT)



SETUP AND HOLD TIMES

LOAD CIRCUIT FOR B OUTPUTS

FIGURE 1. LOAD CIRCUITS AND VOLTAGE WAVEFORMS



TI0279-D3565, JUNE 1990

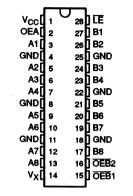
- Drives Heavily Loaded Backplanes With Equivalent Load Impedances Down to 10-0
- Compatible with Pi-Bus and IEEE 896 Futurebus Standards
- High-Drive (100 mA) Open-Collector Drivers
- High-Speed Operation Enhances Performance of Backplane Buses and **Facilitates Incident-Wave Switching**
- Reduced Voltage Swing (1 V) Produces Less **Noise and Reduces Power Comsumption**
- High-Impedance State During Power-Up and Power-Down
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

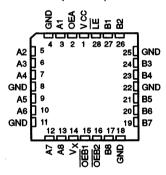
The 'F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high-performance wiredor bus. The B port inverting drivers are lowcapacitance open-collector with controlled ramp and are designed to sink 100 mA from 2 V. The B port inverting receivers have a 100-mV threshold region and a 4-ns glitch filter.

The 'F776 B port interfaces to Backplane Transceiver Logic (BTL™). BTL features a reduced (1-V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

SN54F776 ... JT PACKAGE SN74F776 ... DW OR NT PACKAGE (TOP VIEW)



SN54F776 ... FK PACKAGE (TOP VIEW)



Incident-wave switching is used, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

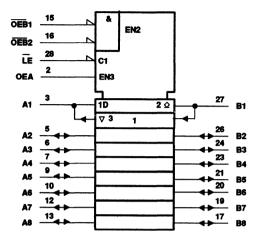
BTL offers low power consumption, EMI and crosstalk, low capacitive loading, superior noise margin, and low propagation delays. This results in a high bandwidth, reliable backplane. The 'F776 A port has TTL 3-state drivers and TTL receivers with a latch function. A separate high-level control voltage input (Vx) is provided to limit the A side output level to a given voltage level (such as 3.3 V). For 5 V systems, Vx is simply tied to Vcc.

The 'F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequences as follows:

- 1. When LE is low and OEBn is low, the B outputs are disabled until the LE circuitry takes control. Then the B outputs follow the A inputs. This causes a maximum of one transition during power-up or power-
- 2. If $\overline{\mathsf{LE}}$ is high or $\overline{\mathsf{OEB}}_{\mathsf{D}}$ is high, then the B outputs are disabled during power-up or power-down.

BTL is a trademark of National Semiconductor Corporation.

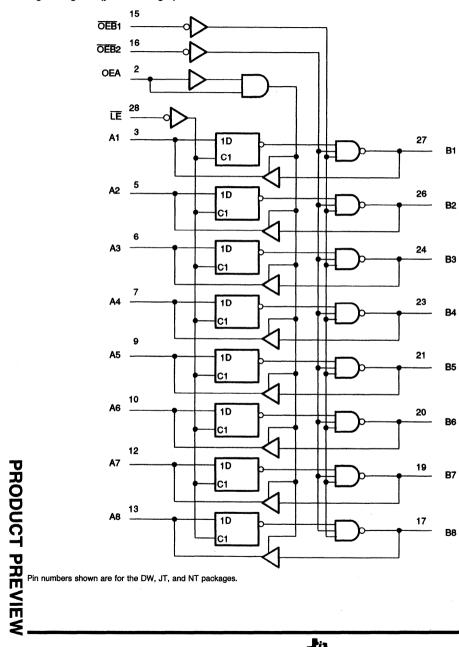
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

D3565, JUNE 1990-TI0279

logic diagram (positive logic)



FUNCTION TABLE

		Ī	NPUTS	;		LATCH	OUTPUTS		MODE
An	Bn†	LE	OEA	OEB1	OEB2	STATE	An	Bn	MODE
Н	Х	L	L	L	L	Н	Z	Н	A -Abid in a data from AA-D
L	Х	L	L	L	L	L	z	L	A at high impedance, data from A to B
X	X	Н	L	L	L	Qo	Z	Qo	A high impedance, latched data to B
_	_	L	Н	L	L	‡	‡	‡	Feedback A to B and B to A
_	Н	Н	Н	L	L	H§	Н	Ζ§	December 1 de la companya de la comp
-	L	н	Н	L	L	H§	L	Ζ§	Preconditioned latch enabling data transfer from B to A
_	_	Н	Н	L	L	Q _o	Qo	Qo	Latch state to A and B
Н	Х	L	L	Н	Х	Н	Z	Z	
L	х	L	L	Н	X	L	z	Z	
X	Х	н	L	Н	x	Qo	z	Z	Don't A skink importance
Н	Х	L	L	Х	н	н	Z	z	B and A at high impedance
L	Х	L	L	х	н	L	z	z	
X	Х	Н	L	х	н	Qo	z	z	
_	Н	L	Н	Н	Х	Н	Н	Z	
_	L	L	Н	н	x	L	L	z	
_	Н	Н	Н	н	x	Qo	н	z	
-	L	Н	н	н	×	Qo	L	z	Dat birt immediance data from Dita A
-	н	L	н	×	н	н	н	z	B at high impedance, data from B to A
-	L	L	н	×	н	L	L	z	
-	н	Н	Н	x	н	Qo	Н	z	
-	L	н	Н	×	н	Qo	L	z	

H = High-voltage level, L = Low-voltage level, X = Don't care, — = Input not externally driven, Z = High-impedance (Off) state, Qn₀ = High or low voltage level one setup time prior to the low-to-high <u>IE</u> transition

[†] Precaution should be taken to ensure the B inputs do not float. If they are permitted to float, the B inputs will take on the low level.

[‡] Condition will cause a feedback loop path; A to B and B to A.

[§] The latch must be preconditioned high such that B inputs can assume a high or low level while OEB1 and OEB2 are low and LE is high.

SN54F776, SN74F776 PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

D3565, JUNE 1990-TI0279

absolute maximum ratings over o	perating free-air temperature range	(unless otherwise noted)†
---------------------------------	-------------------------------------	---------------------------

	•
Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range	0.5 V to 7 V
Thresold control voltage, Vx	0.5 V to 7 V
Input current	-40 mA to 5 mA
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to VCC
Current into any output in the low state: SN54F776 (A1 thru A8)	40 mA
SN54F776 (B1 thru B8)	200 mA
SN74F776 (A1 thru A8)	48 mA
SN74F776 (B1 thru B8)	200 mA
Operating free-air temperature range: SN54F776	-55°C to 125°C
SN74F776	0°C to 70°C
Storage temperature range	-65°C to 150°C
esses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These	e are stress ratings only

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			S	N54F77	6	S	N74F77	В		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
	I the first and a second secon	B1 thru B8	1.6			1.8			v	
VIH High-level output voltag	High-level output voltage	All others	2			2			٧	
	Low-level output voltage	B1 thru B8			1.45			1.45		
VIL		All others			0.8			0.8	٧	
		A1 thru A8	}		-40			-40		
ŀΙΚ	Input clamp current	All others			-18			-18	mA	
ЮН	High-level output current	A1 thru A8			-3			-3	mA	
1	1111	A1 thru A8			20			24	Ι.	
IOL	Low-level output current	B1 thru B8			100			100	mA	
TA	Operating free-air temperature range		-55		125	0		70	°C	



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	5	N54F77	6	S	N74F77	3	UNIT
		TEST CONDITIONS	MIN	TYP†	MAX	MIN	TYP	MAX	UNII
	A1 thru A8				-0.5			-0.5	
VIK	B1 thru B8,	$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$			1.0			1.0	٧
	Control inputs				1.2			1.2	
1	B1 thru B8	V _{CC} = 5.5 V, V _{IL} = 1.45 V, V _{IH} 1.6 V,			100			100	
ЮН	Bi tillu bo	V _{OH} = 2.1 V			100			100	μΑ
		$V_{CC} = 4.5 \text{ V}, I_{OH} = -3 \text{ mA}, V_{X} = V_{CC}$	2.5	2.9		2.5			
VOH	A1 thru A8	$V_{CC} = 4.5 \text{ V, } I_{OH} = -0.4 \text{ mA,}$	2.5			2.5			V
		$V_X = 3.13 \text{ V or } 3.47 \text{ V}$	2.5			2.5			
	A1 thru A8	$V_{CC} = 4.5 \text{ V}, I_{OL} = 20 \text{ mA}, V_{X} = V_{CC}$		0.3	0.5			0.5	
VOL	B1 thru B8	$V_{CC} = 4.5 \text{ V}, I_{OL} = 100 \text{ mA}$			1.5			1.5	٧
		$V_{CC} = 4.5 \text{ V}, I_{OL} = 4 \text{ mA}$	0.4			0.4			
liH1‡	Control inputs	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$			20			20	^
чнт	B1 thru B8	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.1 \text{ V}$			100			100	μΑ
	Control inputs	$V_{CC} = 5.5 \text{ V}, V_{I} = 7 \text{ V}$		1	100			100	μΑ
IIH2 [‡]	A1 thru A8	$V_{CC} = 5.5 \text{V}, \text{V}_{\text{I}} = 5.5 \text{V}$		0.01	1			1	mA
	B1 thru B8			0.01	1				ША
lu.	Control inputs	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$			-20			-20	А
IIL.	B1 thru B8	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.3 \text{ V}$			- 100			-100	μΑ
lozh	A1 thru A8	$V_{CC} = 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$			70			70	μΑ
lozl	A1 thru A8	$V_{CC} = 5.5 \text{ V}, V_{O} = 0.5 \text{ V}$			-70			-70	μΑ
10.06	A1 thru A8 only	$V_{CC} = 5.5 \text{ V}, B_n \text{ at } 1.6 \text{ V}, \text{OEA}, \overline{\text{OEB}} 1, \text{ and}$	60	-75	150	-60		- 150	mA
los	AT UITU AG OTHY	OEB2 at 2.7 V	-60	-75	- 150	-60		- 150	IIIA
		$V_{CC} = 5.5 \text{ V}, V_{X} = V_{CC}, \overline{LE}, OEA, \overline{OEB}1,$							
ŀ		OEB2 and A1 thru A8 at 2.7 V,	1		±100			±100	μΑ
l.,		B1 thru B8 at 2 V							
١x		$V_{CC} = 5.5 \text{ V}, V_{X} = 3.13 \text{ V or } 3.47 \text{ V},$							
		LE and OEA at 2.7 V, OEB1, OEB2,			± 10			± 10	μΑ
L		A1 thru A8 and B1 thru B8 at 2 V							
ІССН		V _{CC} = 5.5 V			100		70	100	mA
ICCL		V _{CC} = 5.5 V			145		100	145	mA
ICCA		V _{CC} = 5.5 V			100		80	100	m/

timing requirements

		1	V _{CC} = 5 V T _A = 25°C 'F776		-	V to 5.5 N to MAX		UNIT
		′F776			'F776 SN54F776		F776	SN74F776
l		MIN N	XAN	MIN	MAX	MIN	MAX	
tsu	Setup time, A to LE	5		5		5		ns
th	Hold time, A to LE	0		0		0		ns
tw	Pulse duration, LE low	10		10		6		ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should exceed one second.

SN54F776, SN74F776 PI-BUS OCTAL BIDIRECTIONAL LATCHED TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

D3565, JUNE 1990-TI0279

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	CL R1 R2 T/	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25°C		-	C _L = R1 = R2 = R1 = R1 = R2 = R1 = R1 = R1	500 Ω,	(†	UNIT
tPLH			5.5	7.5	12	4.5	13	2	8	
tPHL	A	В	3.5	5.5	8	2.5	9	3	9	ns
t _{PLH}	_	_	5.5	7.5	12	4.5	13	5	12	
t _{PHL}	В	A	6	8.5	10.5	6	11.5	6	11	ns
tPLH .	TE .	В	3	5	8.5	2	11.5	2.5	10	
tPHL	LE	. В	4	6	9	3	9.5	3	9.5	ns
tPLH	<u>OEB</u> n	В	2	4.5	7.5	1.5	8.5	1.5	8.5	
tPHL	OEDn	P	4.5	7.5	10	3.5	10.5	3.5	10.5	ns
tPZH	OEA		8	10.5	14.5	7	16.5	7.5	15.5	
tPZL) OEA	A	8.5	12	14.5	8.5	18	8.5	17	ns
tPHZ	054		2	4.5	7	2	7.5	2	7.5	
tPLZ	OEA	A	2	4.5	7.5	2	8	2	8	ns
t _t ‡	B ports 1	.3 V to 1.7 V	0.5	2	4.5	0.5	4.5	0.5	4.5	ns
t _t ‡	B ports 1	.7 V to 1.3 V	0.5	2	4.5	0.5	4.5	0.5	4.5	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] Transition time is defined as the time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

General Information	
ACL LSI Products 2	
ACL Widebus™ Products 3	
BTL Transceiver Products 4	
Bus-Termination Array Products 5	
Clock Driver Products 6	
ECL/TTL Translator Products 7	
FIFO Products 8	
Low-Impedance Line Driver Products 9	
Memory Driver Products)
SCOPE™ Testability Products	
64BCT Series Products	
Mechanical Data	

SN74S1050 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3228, JULY 1989-REVISED MARCH 1990

Designed to Reduce Reflection Noise	D OR N PACKAGE (TOP VIEW)
 Repetitive Peak Forward Current 200 mA 	D01 [1 16] D12
 12-Bit Array Structure Suited for Bus- Oriented Systems 	D02
 ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015 	GND 5 12 GND D04 6 11 D09
Package Options Include Plastic "Small Outline" Packages and Standard Plastic	D05

description

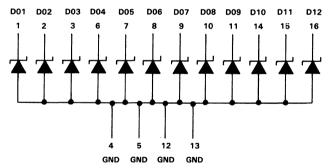
300-mil DIPs

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit highspeed Schottky diode array suitable for a clamp to GND.

Outline" Packages and Standard Plastic

The SN74S1050 is characterized for operation from 0°C to 70°C.

schematic diagram





D3228, JULY 1989-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Steady-state reverse voltage, V _R	7 V
Continuous forward current, IF: any D terminal from GND) mA
total through all GND terminals) mA
Repetitive peak forward current, FRM: any D terminal from GND) mA
total through all GND terminals	1 A
Continuous total power dissipation at (or below) 25 °C free-air temperature 625	mW
Operating free-air temperature range	o°C
Storage temperature range65°C to 15	0°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡These values apply for t_W ≤ 100 µs, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

	PARAMETER	TEST CONDITIONS MIN TYP§	MAX	UNIT
IR	Static reverse current	V _R = 7 V	5	μΑ
.,	Static forward voltage	I _F = 18 mA 0.75	0.95	V
VF		I _F = 50 mA 0.95	1.2	1 °
VFM	Peak forward voltage	lμ = 200 mA 1.45		V
C-	Total capacitance	V _R = 0, f = 1 MHz 5	10	
СТ	rotal capacitance	V _R = 2 V, f = 1 MHz 4	8	pF

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

	PARAMETER	AMETER TEST CONDITIONS			P [§] MAX	UNIT
	Internal acceptable accept	Total I _F = 1 A,	See Note 2		0.6 2	T ^
ا x	Internal crosstalk current	Total I _F = 198 mA,	See Note 2	0.	02 0.2	mA

[§]All typical values are at $T_A = 25$ °C.

NOTE 2: I_X is measured under the following conditions with one diode static and all others switching: Switching diodes: $t_W=100~\mu s$, duty cycle = 20%; static diode: $V_R=5~V$.

The static diode's input current is the internal crosstalk current Ix.

switching characteristics at 25 °C free-air temperature (see Note 3)

PARAMETER TEST CONDITIONS			TYP	MAX	UNIT
t _{rr} Reverse recovery time	$I_F = 10 \text{ mA}, I_{RM(REC)} = 10 \text{ mA}, I_{R(REC)} = 1 \text{ mA}, R_L = 100 \Omega$		8	16	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



D3228 JULY 1989-REVISED MARCH 1990

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2 was evaluated. The resulting waveforms with and without the diode are shown in Figure 3.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

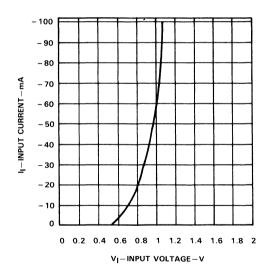


FIGURE 1. TYPICAL CURRENT-VOLTAGE CURVE



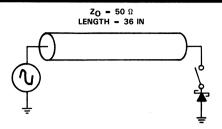
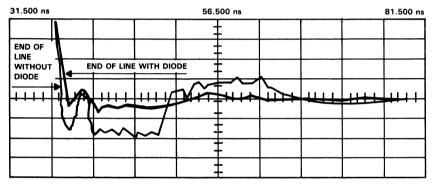


FIGURE 2. DIODE TEST SETUP



Y-COORDINATE = 1,800 VOLTS/DIV

TIMEBASE = 5.00 ns/VOLT VMARKER 1

= -1.353 VOLTS VMARKER 2 = -3.647 VOLTS OFFSET = 0.000 VOLTS DELAY = 56.500 ns

DELTA V = -2.293 VOLTS

FIGURE 3. SCOPE DISPLAY

SN74S1051 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3423, SEPTEMBER 1990

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

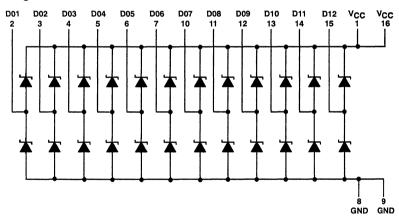
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

The 74S1051 is characterized for operation from 0°C to 70°C.

SN74S1051...D OR N PACKAGE (TOP VIEW)

			_	
Vcc[1	U	16] v _{cc}
D01[2		15	D12
D02[3		14	D11
D03[4		13	D10
D04[5		12	D09
D05[6		11	D08
D06[7		10	D07
GND[8		9] GND

schematic diagram



D3423, SEPTEMBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V _R	7 V
Continuous forward current, I _F : any D terminal from GND or to V _{CC}	50 mA
total through all GND or V _{CC} terminals	170 mA
Repetitive peak forward current [‡] , I _{FRM} : any D terminal from GND or to V _{CC}	200 mA
total through all GND or V _{CC} terminals	1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1) .	
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

	PARAMETER	TEST CO	ONDITIONS	MIN TYPS	MAX	UNIT
		7-1/	l _F = 18 mA	0.85	1.05	V
٧F		IF = 50 mA	1.05	1.3	· ·	
٧F		From GND	I _F = 18 mA	0.75	0.95	V
		1 Tom GND	IF = 50 mA	0.95	1.2	· •
VFM	Peak forward voltage		IF = 200 mA	1.45		V
	Static reverse current	To V _{CC}	V _R = 7 V		5	μА
l _R		From GND	- VH = / V		5	μΑ
C-		V _R = 0,	f = 1 MHz	8	16	pF
CT	Total capacitance	V _R = 2 V,	f = 1 MHz	4	8	Pi

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I Internal expectally assured	Total IF = 1 A,	See Note 3		0.8	2	A	
'	I _X Internal crosstalk current	Total IF = 198 mA,	See Note 3		0.02	0.2	mA

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
trr	Reverse recovery time	IF = 10 mA,	IRM(REC) = 10 mA,	iR(REC) = 1 mA,	R _L = 100 Ω		8	16	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



[‡] These values apply for t_w ≤ 100 μs, duty cycle ≤ 20%.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 mW/°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open circuited during the measurement of these characteristics.

NOTE 3: I_X is measured under the following conditions with one diode static and all others switching: switching diodes: t_W = 100 μs, duty cycle = 0.2; static diode: V_R = 5 V. The static diode's input current is the internal crosstalk current i_X.

D3423, SEPTEMBER 1990

TYPICAL APPLICATION INFORMATION

Large transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc), or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 and SN74S1053 diode termination arrays help suppress transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of transients is tracked by the current-voltage characteristic curve for that diode. Typical current-voltage curves for the SN74S1051 / S1053 are shown in Figures 1 and 2.

To illustrate how the diode arrays act to reduce transients at the end of a transmission line, the test setup in Figure 3 was evaluated. The resulting waveforms with and without the diode are shown in Figure 4.

The maximum effectiveness of the diode arrays in suppressing transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

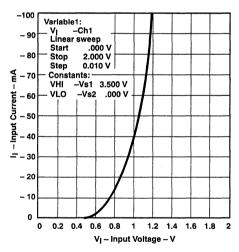


Figure 1. Typical Input Current vs Input Voltage (Lower Diode)

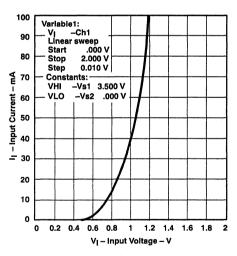


Figure 2. Typical Input Current vs Input Voltage (Upper Diode)

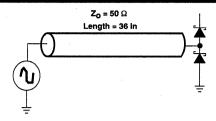


Figure 3. Diode Test Setup

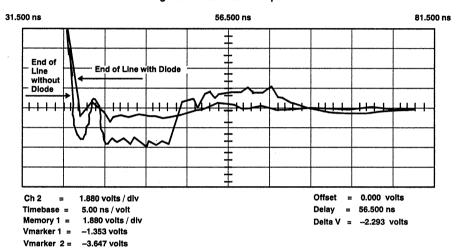


Figure 4. Scope Display

SN74S1052 16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3229, JULY 1989-REVISED MARCH 1990

Designed to Reduce Reflection Noise

- Repetitive Peak Forward Current . . .
 200 mA
- 16-Bit Array Structure Suited for Bus-Oriented Systems
- ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

OW OR N PACKAGE (TOP VIEW) 001 1 20 01

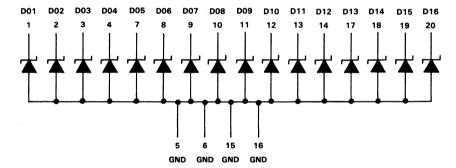
D01	Цı	$\bigcup 20$	L	D16
D02		19	巾	D15
D03	[]₃	18	巾	D14
D04	□₄	. 17	口	D13
GND	[]₅	16	Ð	GND
GND	[]6	. 15	卣	GND
D05	Ū۶	14	巾	D12
D06	Π٤	10	Þ	D11
D07	۵	1:	乜	D10
D08	ď١	0 1	ψ	D09

description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1052 is characterized for operation from 0° C to 70° C.

schematic diagram



SN74S1052 16 BIT SCHOTTKY BARRIER DIODE BUS TERMINATION ARRAY

D3228, JULY 1989-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, VR	v
Continuous forward current, IF: any D terminal from GND 50 m	
total through all GND terminals 170 m	
Repetitive peak forward current, FRM: any D terminal from GND	Α
total through all GND terminals	Α
Continuous total power dissipation at (or below) 25 °C free-air temperature 735 ml	Ν
Operating free-air temperature range	С
Storage temperature range65 °C to 150 °	С

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

	PARAMETER	TEST CONDITIONS		P [§] MAX	UNIT
IR	Static reverse current	V _R = 7 V		5	μΑ
۷E	Castin forward wells	I _F = 18 mA	0.	75 0.95	
٧F	F Static forward voltage	IF = 50 mA	0.	95 1.2	
VFM	Peak forward voltage	I _F = 200 mA	1.	45	V
C-	Total capacitance	$V_R = 0$, $f = 1 \text{ MHz}$		5 10	pF
СТ		$V_R = 2 V$, $f = 1 MHz$		4 8	pr pr

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

	PARAMETER TEST CONDITIONS		MIN	TYP§	MAX	UNIT
	Total I _F = 1 A, See Note 2		0.6	2		
	IX Internal crosstalk current	Total I _F = 270 mA, See Note 2		0.02	0.2	mA

 $^{^{\}S}$ All typical values are at $T_A = 25$ °C.

NOTE 2: Ix is measured under the following conditions with one diode static and all others switching:

Switching diodes: $t_W = 100 \mu s$, duty cycle = 20%; static diode: $V_R = 5 V$.

The static diode's input current is the internal crosstalk current lx.

switching characteristics at 25 °C free-air temperature (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tr	Reverse recovery time	$I_F = 10$ mA, $I_{RM(REC)} = 10$ mA, $I_{R(REC)} = 1$ mA, $R_L = 100 \Omega$		8	16	ns

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.





[‡]These values apply for $t_W \le 100 \mu s$, duty cycle $\le 20\%$.

SN74S1052 16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3228. JULY 1989-REVISED MARCH 1990

APPLICATION INFORMATION

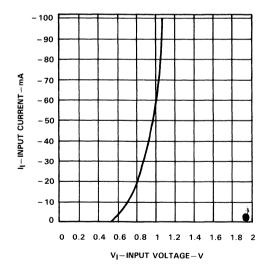
Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2 was evaluated. The resulting waveforms with and without the diode are shown in Figure 3.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.



VARIABLE 1: - CH1 LINEAR SWEEP START 0.000 V STOP -2.000 V STOP -0.010 VCONSTANTS: 3.5000 V ۷н V_{s1} 0.0000 V ٧ı v_{s2}

FIGURE 1. TYPICAL CURRENT-VOLTAGE CURVE



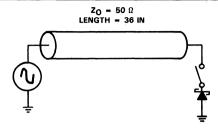
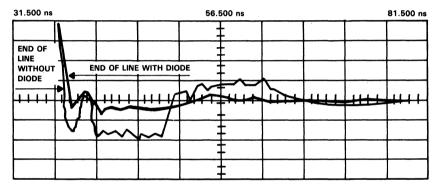


FIGURE 2. DIODE TEST SETUP



Y-COORDINATE = 1,800 VOLTS/DIV TIMEBASE = 5.00 ns/VOLT VMARKER 1 = -1.353 VOLTS VMARKER 2 = -3.647 VOLTS OFFSET = 0.000 VOLTS
DELAY = 56.500 ns
DELTA V = -2.293 VOLTS

FIGURE 3. SCOPE DISPLAY

SN74S1053 16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3424, SEPTEMBER 1990

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 200 mA
- 16-Bit Array Structure Suited for Bus-Oriented Systems
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

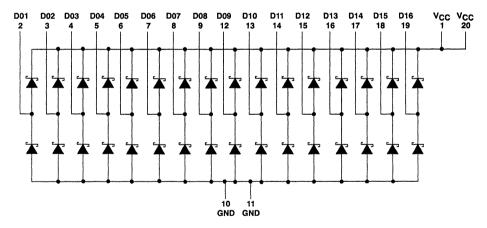
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

The 74S1053 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE (TOP VIEW)

Vcc[1,	20] v _{cc}
D01 [2	19	D16
D02 [3	18	D15
D03 [4	17	D14
D04 [5	16	D13
D05 [6	15	D12
D06 [7	14	D11
D07 [8	13	D10
D08 [9	12	D09
GND Î	10	11	OND

schematic diagram



SN74S1053 16-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3424, SEPTEMBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V _R	7 V
Continuous forward current, I _F : any D terminal from GND or to V _{CC}	
total through all GND or V _{CC} terminals	
Repetitive peak forward current [‡] , I _{FRM} : any D terminal from GND or to V _{CC}	200 mA
total through all GND or V _{CC} terminals	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1)	625 mW
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

	PARAMETER	TEST CO	ONDITIONS	MIN TYP§	MAX	UNIT
		T- 1/	I⊨ = 18 mA	0.85	1.05	V
VF	Chatia famound waltern	To VCC	IF = 50 mA	1.05	1.3	٧
٧-	Static forward voltage	From GND	IF = 18 mA	0.75	0.95	V
		Trom divid	IF = 50 mA	0.95	1.2	
VFM	Peak forward voltage		IF = 200 mA	1.45		V
1	I _R Static reverse current	To VCC	V _R = 7 V		5	
'R		From GND			5	μA
C-	Total capacitance $ V_{R} = 0, $ $V_{R} = 2 V, $	f = 1 MHz	8	16	pF	
CT		V _R = 2 V,	f = 1 MHz	4	8	Pi

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

multiple-diode operation

	PARAMETER	TEST CONDITIONS		MIN T	ΥP§	MAX	UNIT
I _X Internal crosstalk current	Total IF = 1 A,	See Note 3		0.8	2	mA	
	internal crosstalk current	Total I _F = 198 mA,	See Note 3		0.02	0.2	IIIA

[§] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	·	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t _{rr} Reverse recovery time	IF = 10 mA,	IRM(REC) = 10 mA,	iR(REC) = 1 mA,	R _L = 100 Ω		8	16	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



[‡] These values apply for $t_W \le 100 \mu s$, duty cycle $\le 20\%$.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 mW/°C.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open circuited during the measurement of these characteristics.

NOTE 3: I_X is measured under the following conditions with one diode static and all others switching: switching diodes: t_W = 100 μs, duty cycle = 0.2; static diode: V_R = 5 V. The static diode's input current is the internal crosstalk current I_X.

D3424, SEPTEMBER 1990

TYPICAL APPLICATION INFORMATION

Large transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc), or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 and SN74S1053 diode termination arrays help suppress transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of transients is tracked by the current-voltage characteristic curve for that diode. Typical current-voltage curves for the SN74S1051 / S1053 are shown in Figures 1 and 2.

To illustrate how the diode arrays act to reduce transients at the end of a transmission line, the test setup in Figure 3 was evaluated. The resulting waveforms with and without the diode are shown in Figure 4.

The maximum effectiveness of the diode arrays in suppressing transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

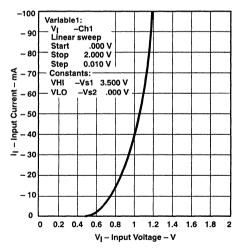


Figure 1. Typical Input Current vs Input Voltage (Lower Diode)

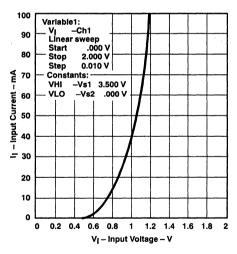


Figure 2. Typical Input Current vs Input Voltage (Upper Diode)

D3424, SEPTEMBER 1990

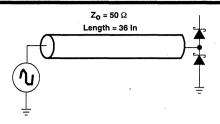


Figure 3. Diode Test Setup

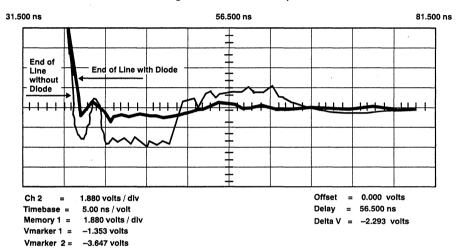


Figure 4. Scope Display

SDLS019 - D3492, APRIL 1990

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 300 mA
- 8-Bit Array Structure Suited for Bus-Oriented Systems

description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for GND clamp.

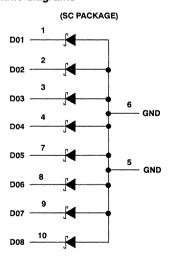
The SN74S1056 is characterized for operation from 0°C to 70°C.

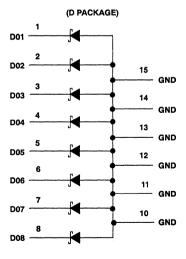
SC PACKAGE

D PACKAGE (TOP VIEW)

1		$\overline{}$		1
D01[1	\cup	16	NC
D02[2		15] GND
D03[3		14	GND
D04[4		13] GND
D05[5		12] GND
D06[6		11	GND
D07[7		10	GND
D08[8		9] NC
	l .			

schematic diagrams







SN74S1056 8-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3492, APRIL 1990 - SDLS019

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady state reverse voltage, V _R	7 V
Continuous forward current, I _F : any D terminal from GND	
total through all GND terminals	mΑ
Repetitive peak forward current, I _{FRM} ‡: any D terminal from GND	mΑ
total through all GND terminals	2 A
Continuous total power dissipation at (or below) 25°C free-air temperature	nW
Operating free-air temperature range)°C
Storage temperature range – 65°C to 150)°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

	PARAMETER	TEST CO	NDITIONS	MIN	TYP§	MAX	UNIT
lR	Static reverse current	V _R = 7 V				10	μΑ
.,	Static forward voltage	IF = 18 mA			0.65	0.85	
٧F		IF = 50 mA			0.8	1	V
VFM	Peak forward voltage	IF = 300 mA			1.41		٧
C-	Total capacitance	V _I = 0 V,	f = 1 MHz		11	13	pF
CT		V _I = 2 V,	f = 1 MHz		8	11	PΓ

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

	PARAMETER	TEST CONDITIONS			TYP§	MAX	UNIT
	Internal crosstalk	Total GND current = 1.2 A,	See Note 2		0.6	2	mA
'x	current	Total GND current = 126 mA,	See Note 2		0.01	0.1	mA

[§] All typical values are at T_A = 25°C.

NOTE 2: I_X is measured under the following conditions with one diode static, all others switching:

Switching diodes: tw = 100 µs, duty cycle = 20%;

Static diode: VR = 5 V

The static diode input current is the internal crosstalk current lx.

switching characteristics, T_A = 25°C (see Note 3)

PARAMETER	TEST CONDITIONS			TYP	MAX	UNIT
	·	I _F = 10 mA,				
t _{rr}	Reverse recovery time	$I_{RM(REC)} = 10 \text{ mA}, I_{R(REC)} = 1 \text{ mA},$		5	- 10	ns
1		$R_L = 100 \Omega$				

NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



[‡] These values apply for $t_W \le 100 \mu s$, duty cycle $\le 20\%$.

SDLS019 - D3492 APRIL 1990

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1056 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current-voltage for the SN74S1056 is shown in Figure 1.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 2(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 2(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

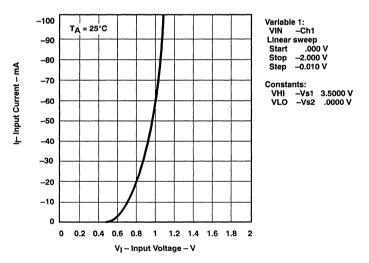
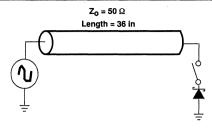
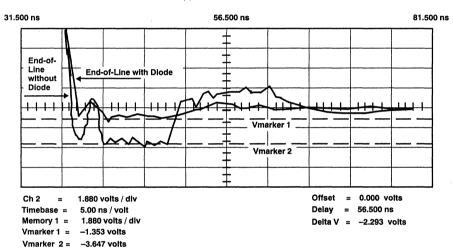


Figure 1. Typical Current-Voltage Curve

D3492, APRIL 1990 - SDLS019



(a) DIODE TEST SETUP



(b) SCOPE DISPLAY

Figure 2. Diode Test Setup and Scope Display

General Information
ACL LSI Products 2
ACL Widebus™ Products 3
BTL Transceiver Products 4
Bus-Termination Array Products 5
Clock Driver Products 6
ECL/TTL Translator Products 7
FIFO Products 8
Low-Impedance Line Driver Products 9
Memory Driver Products
SCOPE™ Testability Products
64BCT Series Products 12
Mechanical Data

PRODUCT PREVIEW

- Low Output Skew, Low Pulse Skew for Clock Distribution and Clock Generation Applications
- Four Outputs Toggle at the Clock Frequency, Four Outputs Switch at One-Half the Clock Frequency
- Advanced BiCMOS Design With TTL-Voltage-Compatible Inputs and Outputs
- f_{max} = 80 MHz
- High-Drive Outputs Eliminate the Need for External Buffering
- State-of-the-Art EPIC™-IIB BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Package Options Include Plastic "Small Outline" Packages and 300-mil DIPs

(TOP VIEW)					
Y3 [GND [Y4 [V CC G CLR [CLR [CLR [GND [1 2 3 4 5 6 7 8 9	VII	20 19 18 17 16 15 14 13 12	Y2 GND Y1 V _{CC} CLK GND V _{CC} Q4 GND	
Q2 [10	1	11] Q3	

DW OD N DAOKAOE

description

The 'ABT337 contains four buffered outputs that switch at the clock frequency and four divide-by-two outputs that switch at one-half the clock frequency. When \overline{G} is low and \overline{CLR} is high, the Y outputs follow the CLK input and the Q outputs switch on the low-to-high transition of CLK.

This clock driver is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. Taking $\overline{\text{CLR}}$ low asynchronously resets the Q outputs to a low level. High-drive outputs (\pm 48 mA) eliminate the need for external buffering of output signals.

The SN74ABT337 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

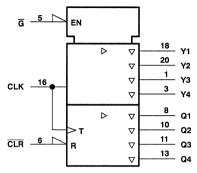
	INPUTS	3	OUT	PUTS
G	G CLR CLK		Y1-Y4	Q1-Q4
Н	X	X	Z	Z
L	L	L	L	L
L	L	Н	н	L
L	Н	L	L	Q_0
L	н	Н	н	Q ₀
L	н	1	1	toggle

 $\mathbf{Q}_0 =$ the level at the \mathbf{Q} outputs after the most recent low-to-high transition of CLK.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

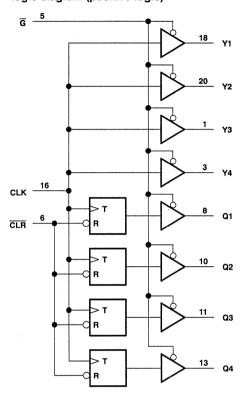


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC} –	0.5 V to 7 V
Input voltage range, V _I –	
Voltage applied to any output in the disabled or power-off state, $V_0 \dots -0.5 \text{ V}$ to	V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	– 18 mA
Current into any output in the low state, IO	96 mA
Storage temperature range	°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

recommended operating conditions

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	٧
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
VI	Input voltage	0	Vcc	V
loн	High-level output current		- 48	mA
lOL	Low-level output current		48	mA
TA	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	5 V, I _I = - 18 mA					- 1.2	V
Voн	V _{CC} = 4.5 V,	c = 4.5 V, I _{OH} = - 48 mA			3.5			٧
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA					0.5	٧
loz	V _{CC} = 5.5 V							μΑ
lį	V _{CC} = 5.5 V							μΑ
		VI = VCC or GND, Id		Outputs high				
Icc	V _{CC} = 5.5 V,		IO = 0	Outputs low				mA
		Outputs disabled						
Ci	VI = VCC or GND					5.5		pF
Co	VO = VCC or GND							pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (see Note 1)

			MIN	MAX	UNIT
fclock	Clock frequency		0	80	MHz
t _W		CLR low			
	Pulse duration	CLK high or low	4		ns
t _{su}	Setup time, CLR inactive before CLK↑				ns

switching characteristics over recommended operating free-air temperature range (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX	UNIT
fmax			MIN MAX	MHz
t _{PLH}	OLIV.	A=::. V == 0		
^t PHL	CLK	Any Y or Q		ns
^t PHL	CLR	Any Q		ns
^t PZH	G	Any Y or Q		ns
^t PZL	- G	Any 1 or Q		113
^t PHZ	G	Any Y or Q		ns
^t PLZ]	Any 1 of Q		113
^t sk(o)	CLK	Any Y or Q		ns
^t sk(p)	OLK	Ally 1 of Q		113

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D3427, OCTOBER 1989

- Low-Skew Propagation Delay Specifications for Clock Driver Applications
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

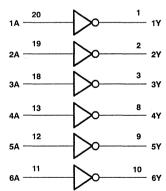
description

This device contains six independent inverters. They perform the Boolean function $Y = \overline{A}$.

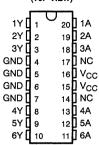
The 74AC11204 is designed specifically for applications requiring low skew between switching outputs.

The 74AC11204 is characterized for operation from 25°C to 70°.

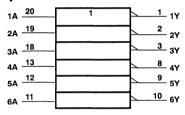
logic diagram (positive logic)



DW OR N PACKAGE (TOP VIEW)



logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUT	OUTPUT
Α	Υ
Н	L
L	Н

EPIC is a trademark of Texas Instruments Incorporated.

D3427, OCTOBER 1989

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 150mA
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.75	5	5.25	V
	V _{CC} = 4.75 V		3.3			
VIH	High-level input voltage	V _{CC} = 5.25 V	3.7			V
.,	Low lovel input veltage	V _{CC} = 4.75 V			1.4	
V_{IL}	Low-level input voltage VCC = 5.25 V				1.6	V
VI	Input voltage				Vcc	V
V _O	Output voltage		0		Vcc	V
1	Ligh level output surrent	V _{CC} = 4.75 V			- 24	
ІОН	High-level output current	V _{CC} = 5.25 V			- 24	mA
	1 - 1 - 1 - 1 - 1 - 1 - 1	V _{CC} = 4.75 V			24	
OL	Low-level output current VCC = 5.2				24	mA
Δt/Δν	Input transition rise or fall rate		0		10	ns/V
TA	Operating free-air temperature		25		70	°C

74AC11204 HEX INVERTER/CLOCK DRIVER

D3427, OCTOBER 1989

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T,	Δ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	UNII
		4.75 V	4.65			4.65		
	ΙΟΗ = - 50 μΑ	5.25 V	5.15			5.15		
VOH ·	I _{OH} = – 24 mA	4.75 V	4.19			4.05		٧
	IOH = - 24 MA	5.25 V	4.69			4.55		
	I _{OH} = 75 mA [†]	5.25 V				3.6		
		4.75 V			0.1		0.1	
	ΙΟL = 50 μΑ	5.25 V			0.1		0.1	
VOL	1- 044	4.75 V			0.36		0.44	٧
	I _{OL} = 24 mA	5.25 V			0.36		0.44	
	I _{OL} = 75 mA [†]	5.25 V					1.65	
i _l	V _I = V _{CC} or GND	5.25 V			± 0.1		± 1	μА
lcc	V _I = V _{CC} or GND, I _O = 0	5.25 V			4		40	μА
Ci	V _I = V _{CC} or GND	5 V		4				рF

The Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics, T_A = 25°C to 70°C, V_{CC} = 5 V \pm 0.25 V (see Notes 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH}	٨	V	3.7	5.7	
tPHL	A	Y	3.7	5.7	ns
tsk(o)	A	Y		1	ns

NOTES: 2. All specifications are valid only for all outputs switching simultaneously and in phase.

^{3.} Load circuit and voltage waveforms are shown in Section 1.

D3459, MARCH 1990

- Low Skew Propagation Delay Specifications for Clock Driving Applications
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

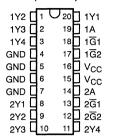
description

These devices contain dual-clock driver circuits that fan out one input signal to four outputs with minimum skew for clock distribution. They also offer two output-enable pins for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the A input.

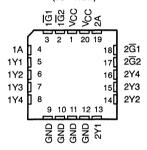
Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The 54AC11208 is characterized for operation over the full military temperature range of -55° C to 125°C. The 74AC11208 is characterized for operation from -40° C to 85°C.

54AC11208...J PACKAGE 74AC11208...DW OR N PACKAGE (TOP VIEW)



54AC11208 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLES

OUTPUT DATA CONTROL INPUT									
1G1	1G2	1A	1Y1	1Y2	1Y3	1Y4			
L	L	L	L	L	L	L			
L	L	Н	Н	Н	Н	H			
L	Н	х	L	L	L	L			
н	L	×	н	Н	Н	н			
Н	н	l x	z	Z	z	z			

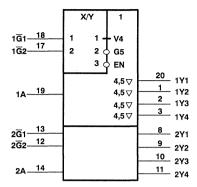
		DATA INPUT		OUT	PUTS	
2 <u>G</u> 1	2G2	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	н	Н	Н	Н	Н
L	Н	X	L	L	L	L
Н	L	Х	н	Н	Н	н
Н	н	х	z	Z	Z	Z

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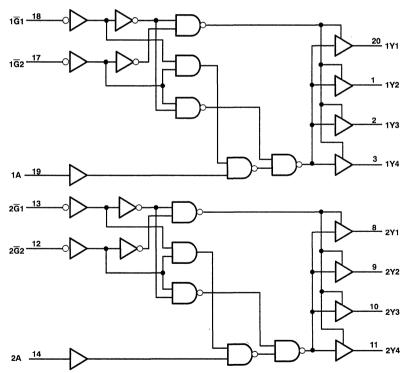
D3459, MARCH 1990

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.



54AC11208, 74AC11208 DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS

D3459, MARCH 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range V	0 5 1/+0 7 1/
Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	
Input clamp current, $I_{ K }$ ($V_1 < 0$ or $V_1 > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 200mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			54AC11208		74AC11208					
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage		3	5	5.5	3	5	5.5	V	
		V _{CC} = 3 V	2.1			2.1				
V _{IH} High-le	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			٧	
		V _{CC} = 5.5 V	3.85			3.85				
		V _{CC} = 3 V			0.9			0.9		
V_{IL}	Low-level input voltage	V _{CC} = 4.5 V			1,35			1.35	٧	
		V _{CC} = 5.5 V			1.65			1.65		
VI	Input voltage		0	04	Vcc	0		Vcc	٧	
Vo	Output voltage		0	~	Vcc	0		Vcc	٧	
		V _{CC} = 3 V	o PRIODI	30	-4			-4		
ЮН	High-level output current	V _{CC} = 4.5 V	100		- 24			- 24	mΑ	
		V _{CC} = 5.5 V	4		- 24			- 24		
		V _{CC} = 3 V			12			12		
lOL	Low-level output current	V _{CC} = 4.5 V			24			24	mA	
	V _{CC} = 5.5 V				24			24		
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V	
TA	Operating free-air temperature		- 55		125	- 40		85	°C	

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3459, MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COMPITIONS		T,	A = 25°C		54AC	11208	74AC1	1208	11117
PANAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		3 V	2.9			2.9		2.9		
	I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
Vall	I _{OH} = - 4 mA	3 V	2.58			2.4		2.48		V
VOH	Jan. 24 mA	4.5 V	3.94			3.7		3.8		٧
	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	I _{OH} = - 75 mA [†]	5.5 V						3.85		
		3 V			0.1		0.1		0.1	
	Ι _{ΟL} = 50 μΑ	4.5 V			0.1		€ 0.1		0.1	
		5.5 V			0.1	र ^ह र्दर	√ 6.1		0.1	
V	I _{OL} = 12 mA	3 V			0.36	4,42	0.5		0.44	V
VOL	la. 24 mA	4.5 V			0.36		0.5		0.44	٧
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
loz	V _I = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μА
l _l	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ
lcc	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μА
Ci	V _I = V _{CC} or GND	5 V		4						pF
c _o	V _I = V _{CC} or GND	. 5 V		10						рF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $_{\pm}$ 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T,	Δ = 25°C	;	54AC	1208	74AC11208		UNIT
FARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
^t PLH	1A and 2A	Any Y	4.8	11.1	13.1	4.8	15.6	4.8	14.6	ns
^t PHL	TA dilu ZA	Ally I	5.1	12.2	14.3	5.1	16.7	5.1	15.6	110
^t PLH	1Gn and 2Gn	Any Y	5.2	11.9	14.2	5.2	√06.9	5.2	15.8	ns
^t PHL		7 1119	7.8	13.3	15.7	7.8	18.4	7.8	17.4	
^t PZH	1G2 or 2G2	Any Y	5.1	11.8	14.2	\$ V	7 17.2	5.1	15.7	ns
^t PZL	1G1 or 2G1	Ally 1	6.8	16.3	19.5	6.8	23.8	6.8	22.8	110
tPHZ	1G2 or 2G2	Any Y	3.4	6.9	8.6	3.4	9.6	3.4	9.2	ns
t _{PLZ}	1G1 or 2G1		4.1	7.5	9.4	4.1	10.5	4.1	10.2	110

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

D3459, MARCH 1990

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

DADAMETED	FROM	TO	T,	A = 25°C	;	54AC	11208	74AC1	11208	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	14 104	A V	4.2	5.5	9	4.2	10.5	4.2	9.9	
^t PHL	1A and 2A	Any Y	4.2	7	9.3	4.2	10.8	4.2	10.1	ns
tPLH .	1Gn and 2Gn	A V	4.6	7.3	9.6	4.6	्रोत्तु.5	4.6	10.7	
[†] PHL		Any Y	4.8	7.7	10.2			4.8	11	ns
^t PZH	1G2 or 2G2	A V	4.3	7.2	9.4	Q4.3×	11.3	4.3	10.4	
t _{PZL}	1G1 or 2G1	Any Y	5.3	9	12.2	5.3	14.3	5.3	13.5	ns
t _{PHZ}	1G2 or 2G2	Any Y	3	5.4	7.5	3	8.5	3	8	ns
t _{PLZ}	1G1 or 2G1	Ally 1	3.7	5.7	7.5	3.7	8.5	3.7	8.2	115

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V \pm 0.25 V, T_A = 25°C to 70°C (see Notes 2 and 3)

PARAMETER	FROM	то	74/	ACT1120	8	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	ONII
t _{PLH}	1A and 2A	Any Y	6		8.5	
t _{PHL}	TA and 2A	Ally 1	6		8.5	ns
tsk(o)	1A and 2A	Any Y			1	ns

NOTES: 2. Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per bank	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	95	ρF
Pu		Outputs disabled		10	

^{3.} Specifications are valid for all outputs switching simultaneously and in-phase.

D3460, APRIL 1990

- Inputs are TTL-Voltage Compatible
- Low-Skew Propagation Delay Specifications for Clock Driver Applications
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices contain dual-clock driver circuits that fan out one input signal to four outputs with minimum skew for clock distribution. They also offer two output-enable pins for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the A input.

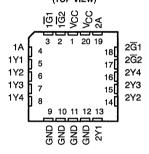
Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The 54ACT11208 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11208 is characterized for operation from – 40°C to 85°C

54ACT11208 ... J PACKAGE 74ACT11208 ... DW OR N PACKAGE (TOP VIEW)

	-	T	1
1Y2 [11,	\cup_{20}	1Y1
1Y3 [2	19	1A
1Y4 []3	18	1 <u>G</u> 1
GND [4	17	1 <u>G</u> 2
GND [5	16	l v _{cc}
GND [6	15	Vcc
GND []7	14	2A
2Y1 [8	13	2 <u>G</u> 1
2Y2 [9	12	2 <u>G</u> 2
2Y3 [10	11	2Y4

54ACT11208 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLES

	OUT		DATA INPUT	OUTPUTS					
I	1Ğ1	1G2	1A	1Y1	1Y2	1Y3	1Y4		
1	L	L	L	L	L	L	L		
	L	L	н	Н	Н	Н	Н		
	L	Н	×	L	L	L	L		
	Н	L	×	Н	Н	Н	Н		
	Н	Н	×	Z	Z	Z	Z		

	PUT TROL	DATA INPUT	OUTPUTS					
2G1	2G2	2A	2Y1	2Y2	2Y3	2Y4		
L	L	L	L	L	L	L		
L	L	н	н	н	Н	н		
L	Н	×	L	L	L	L		
Н	L	×	н	Н	Н	Н		
Н	Н	l x	z	Z	Z	Z		

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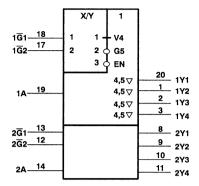
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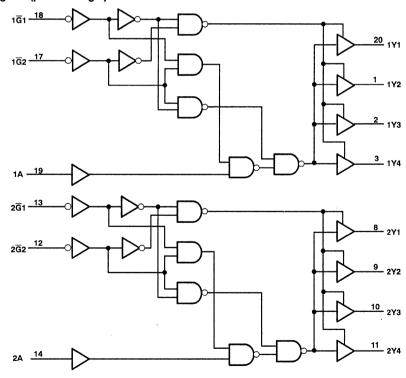
D3460, APRIL 1990

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.



54ACT11208, 74ACT11208 DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS

D3460, APRIL 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 200mA
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54ACT	11208	74ACT		
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	44.	2		٧
VIL	Low-level input voltage		8.6		0.8	V
VI	Input voltage	0	₹K VCC	0	VCC	٧
٧o	Output voltage	0 💉	Vcc	0	Vcc	٧
ЮН	High-level output current	"Cill	- 24		- 24	mA
lOL	Low-level output current	oRO.	24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	– 55	125	40	85	°C



NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

D3460, APRIL 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	T,	Δ = 25°C	;	54ACT	11208	74ACT11208		UNIT
PANAMETER	7E31 CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONLI
	ΙΟΗ = 50 μΑ	4.5 V	4.4			4.4		4.4		
	10Н = 100 ил	5.5 V	5.4			5.4		5.4		
Voн	I _{OH} = - 24 mA	4.5 V	3.94			3.7		3.8		v
100		5.5 V	4.94			4.7		4.8		·
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	I _{OH} = - 75 mA [†]	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
	10L = 50 tb (5.5 V			0.1		0.1		0.1	
VOL	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	v
101		5.5 V			0.36	70	0.5		0.44	·
	IOL = 50 mA [†]	5.5 V				46.00	1.65			
	IOL = 75 mA [†]	5.5 V	1			4			1.65	
loz	VO = VCC or GND	5.5 V			± 0.5		± 10		± 5	μΑ
4	VI = VCC or GND	5.5 V			± 0.1		± 1		± 1	μΑ
lcc	VI = VCC or GND, IO = 0	5.5 V	1		8		160		80	μA
Δlcc [‡]	One input at 3.4 V,	5.5 V			0.9		1		1	mA
	Other inputs at GND or VCC	5.5 V			0.5					
Ci	V _I = V _{CC} or GND	5 V		4						pF
Co	VO = VCC or GND	5 V		10						рF

Those more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T,	T _A = 25°C		54ACT11208		74ACT11208		UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	0.411
^t PLH	1A and 2A	Any Y	5.3	8.5	10.9	5.3	12.6	5.3	11.7	ns
t _{PHL}	I A and 2A		3.6	7.7	11	3.6	12.1	3.6	11.5	115
^t PLH	1Gn and 2Gn	Any Y	4.7	8.5	11.7	4.7	(13.7	4.7	12.8	ns
tPHL.	TGIT AND 2GIT	Ally I	4.4	8.4	11.3	4,40	₹3.2	4.4	12.4	115
tPZH	1G2 or 2G2	Any V	4.4	8.1	11.3	√4.4 </td <td>13.2</td> <td>4.4</td> <td>12.4</td> <td>ns</td>	13.2	4.4	12.4	ns
tPZL	1G1 or 2G1	Any Y	5	9.6	13.3	₹5	16.1	5	14.9	115
t _{PHZ}	1G2 or 2G2	Any Y	4.2	7.4	9.3	4.2	10.7	4.2	10.2	ns
tPLZ	1G1 or 2G1	rary t	5.4	7.5	9.2	5.4	10.3	5.4	9.9	

switching characteristics, V_{CC} = 5 V \pm 0.25 V, T_A = 25°C to 70°C (see Notes 2 and 3)

PARAMETER	FROM	то	74/	74ACT11208			
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	UNIT	
tPLH .	1A and 2A	Any Y	7.6		10.2	ns	
tPHL	1A and 2A	Any Y	6.6		9.8	ns	
t _{sk(o)}	1A and 2A	Any Y			. 1	ns	

NOTES: 2. Load circuit and voltage waveforms are shown in Section 1.



[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

^{3.} Specifications are valid for all outputs switching simultaneously and in-phase.

54ACT11208, 74ACT11208 DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS

D3460, APRIL 1990

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
<u> </u>	Cod Power dissipation capacitance per bank	Outputs enabled	C ₁ = 50 pF, f = 1 MHz	96	pF
C _{pd} Power dissipation c	Power dissipation capacitance per bank	Outputs disabled	OL = 50 pr, 1 = 1 Wil 12	12	

- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-µm Process
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

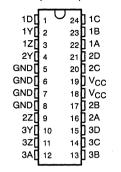
The 'AC11800 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic Y = ABCD and $Z = \overline{ABCD}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54AC11800 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11800 is characterized for operation from – 40°C to 85°C.

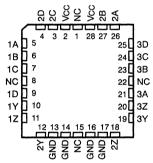
FUNCTION TABLE

INPUTS			OUT	PUTS	
Α	В	С	D	Y	Z
L	Х	X	Х	L	Н
×	L	Х	Х	L	н
×	X	L	X	L	н
x	Х	Х	L	L	н
н	Н	Н	Н	н	L

54AC11800 ... JT PACKAGE 74AC11800 ... DW OR NT PACKAGE (TOP VIEW)



54AC11800 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

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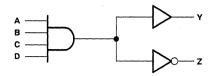
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3B 14 3C -

3D —

PRODUCT PREVIEW

logic diagram, each section (positive logic)



22 23 1B 24 1C 1 1D 16 2A 17 2B 20 9 2C 21 2D 12 10 **3A** 13

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$ 0.5 V to V_{CC} + 0.5 V$
Output voltage range, VO (see Note 1)	$\dots -0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 150mA
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

11



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

recommended operating conditions

			54AC11800			74AC11800			1111
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	٧
V _{IH} H		V _{CC} = 3 V	2.1			2.1			
	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			٧
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V	1		1.35			1.35	V
		V _{CC} = 5.5 V			1.65			1.65	
VI	Input voltage		0		Vcc	0		Vcc	V
Vo	Output voltage		0		Vcc	0		Vcc	V
		V _{CC} = 3 V			-4			-4	mA
ЮН	High-level output current	V _{CC} = 4.5 V			- 24			- 24	
		V _{CC} = 5.5 V			- 24			- 24	
		V _{CC} = 3 V			12			12	
lOL	Low-level output current	V _{CC} = 4.5 V			24			24	mA
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	T _A = 25°C			54AC1	1800	74AC11800		UNIT
PANAMEIEN	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONL
		3 V	2.9			2.9		2.9		
	I _{OH} = - 50 μA	4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
V/~	I _{OH} = - 4 mA	3 V	2.58			2.4		2.28		v
VOH	04 = 4	4.5 V	3.94			3.7		3.8		٧
	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		
	I _{OH} = - 50 mA [†]	5.5 V				3.85				
	I _{OH} = - 75 mA [†]	5.5 V						3.85		
	Ι _{ΟL} = 50 μΑ	3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
1/	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	.,
VOL	1	4.5 V			0.36		0.5		0.44	· ·
	I _{OL} = 24 mA	5.5 V			0.36		0.5		0.44	
	IOL = 50 mA†	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
11	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μΑ
Icc	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		80		40	μΑ
Ci	V _I = V _{CC} or GND	5 V		4						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Note 2)

	DADAMETER	FROM	TO	T _A = 25°C		54AC1	1800	74AC11800			
	PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	^t PLH	A or B	>	1.5	5.6	9.4	1.5	11.3	1.5	10.6	
-	t _{PHL}	AUID	1	1.5	5.1	7.4	1.5	8.7	1.5	8.2	ns

switching characteristics over recommended operating free-air temperature range,

 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM	то	T _A = 25°C		54AC11800		74AC11800		UNIT	
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
tPLH	A D	V	1.5	3.8	6.8	1.5	8	1.5	7.6	
^t PHL	A or B	Y	1.5	3.8	6.2	1.5	7.3	1.5	6.8	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5 V$, $T_A = 25 ^{\circ}C$

PARAMETER	TEST COND	DITIONS	TYP	UNIT	
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF,	f ≃ 1 MHz	27	pF	



- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- 500-mA Typical Latch-up Immunity at 125°C
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'ACT11800 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic Y = ABCD and $Z = \overline{ABCD}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54ACT11800 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11800 is characterized for operation from – 40°C to 85°C.

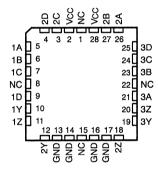
FUNCTION TABLE

	INP	OUTPUTS			
Α	В	С	D	Y	Z
L	X	Х	Х	L	Н
X	L	Χ	Х	L	Н
X	X	L	Х	L	Н
X	X	X	L	L	Н
Н	Н	Н	Н	Н	L

54ACT11800 . . . JT PACKAGE 74ACT11800 . . . DW OR NT PACKAGE (TOP VIEW)

		\Box		١.,
1D[]	1	$\overline{}$	24] 1C
1Y[2		23] 1B
1Z[3		22] 1A
2Y[4		21] 2D
GND[5		20] 2C
GND[6		19] V _{CC}
GND[7		18	V _{CC}
GND[8		17] 2B
2Z[9		16] 2A
3Y[10		15] 3D
3Z[11		14] 3C
3A[12		13] 3B

54ACT11800 . . . FK PACKAGE (TOP VIEW)



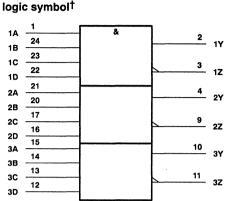
NC-No internal connection

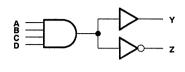
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D3591, JULY 199

logio overb

logic diagram (positive logic) (one section)





Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, IO (VO = 0 to VCC)	± 50mA
Continuous current through V _{CC} or GND pins	
Storage temperature range	– 65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT	11800	74ACT11800		l
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	٧
VIH	High-level input voltage	2			2	٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	Vcc	0	νcc	٧
Vo	Output voltage	0	Vcc	0	VCC	٧
ГОН	High-level output current		- 24		- 24	mA
lOL	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V	T,	A = 25°C	;	54ACT	11800	74ACT111800		UNIT
PANAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		4.5 V	4.4			4.4		4.4		
	IOH = - 50 μA	5.5 V	5.4			5.4		5.4		
Voн	I _{OH} = - 24 mA	4.5 V	3.94			3.7		3.8		.,
VOH		5.5 V	4.94			4.7		4.8		٧
	IOH = 50 mA [†]	5.5 V				3.85				
	I _{OH} = 75 mA [†]	5.5 V						3.85		
		4.5 V			0.1		0.1		0.1	
	IOL = 50 μA	5.5 V			0.1		0.1		0.1	
VOL	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
\ \OL	10L = 24 11A	5.5 V			0.36		0.5		0.44	\ \ \
	I _{OL} = 50 mA [†]	5.5 V					1.65			
	I _{OL} = 75 mA [†]	5.5 V							1.65	
11	VI = VCC or GND	5.5 V			± 0.1		± 0.1		± 0.1	μΑ
lcc	VI = VCC or GND, IO = 0	5.5 V			4		80		40	μА
∆ICC [‡]	One input at 3.4 V, Other inputs at GND or VCC	5.5 V			0.9		1		1	mA
Ci	V _I = V _{CC} or GND	5 V		4						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

Г		FROM	TO	T _A = 25°C		54ACT11800		74ACT11800			
	PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	^t PLH	A or B	V		3.8						
	[†] PHL	AUID	T		3.8						ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, TA = 25°C

PARAMETER	TEST CON	IDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF,	f = 1 MHz	27	pF

6-25

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

6-26

- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

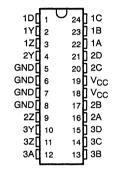
The 'AC11802 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic Y = A + B + C + D and $Z = \overline{A + B + C + D}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54AC11802 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11802 is characterized for operation from – 40°C to 85°C.

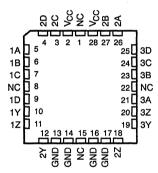
FUNCTION TABLE

	INP	OUTPUTS			
Α	В	С	D	Y	Z
Н	Х	Х	Х	Н	L
×	н	X	X	Н	L
х	Х	Н	Х	н	L
х	Х	X	Н	Н	L
L	L	L	L	L	н

54AC11802 . . . JT PACKAGE 74AC11802 . . . DW OR NT PACKAGE (TOP VIEW)



54AC11802 . . . FK PACKAGE (TOP VIEW)



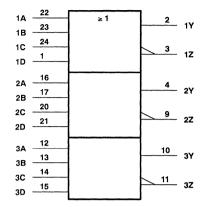
NC - No internal connection

EPIC is a trademark of Texas Instruments Incorporated.

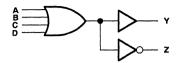


PRODUCT PREVIEW

logic symbol†



logic diagram (positive logic) (one section)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	- 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND pins	± 150mA
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11802, 74AC11802 TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS

D3593, JULY 1990

recommended operating conditions

			SN	54AC118	302	SN	74AC118	02	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		3	5	5.5	3	5	5.5	V
	High-level input voltage	V _{CC} = 3 V	2.1			2.1			
V_{IH}		V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 5.5 V	3.85			3.85			
		V _{CC} = 3 V			0.9			0.9	
V _I L	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} ≈ 5.5 V			1.65			1.65	
VI	Input voltage		0		Vcc	0		Vcc	V
Vo	Output voltage		0		Vcc	0		Vcc	V
		V _{CC} = 3 V			-4			-4	
ЮН	High-level output current	V _{CC} = 4.5 V			- 24			- 24	mA
		V _{CC} ≈ 5.5 V			- 24			- 24	
		V _{CC} = 3 V			12			12	
IOL	Low-level output current	V _{CC} = 4.5 V			24			24	mΑ
		V _{CC} = 5.5 V			24			24	
Δt/Δν	Input transition rise or fall rate		0		10	0		10	ns/V
TA	Operating free-air temperature		- 55		125	- 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS		T,	Δ = 25°C	54AC1	1802	74AC1	1802	UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP MAX	MIN	MAX	MIN	MAX	UNII
	10H = - 50 μΑ	3 V	2.9		2.9		2.9		
		4.5 V	4.4		4.4		4.4		
		5.5 V	5.4		5.4		5.4		
V	I _{OH} = - 4 mA	3 V	2.58		2.4		2.28		v
VOH	I _{OH} = - 24 mA	4.5 V	3.94		3.7		3.8		V
		5.5 V	4.94		4.7		4.8		
	IOH = - 50 mA [†]	5.5 V			3.85				
	I _{OH} = - 75 mA [†]	5.5 V					3.85		
		3 V		0.1		0.1		0.1	
	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	
		5.5 V		0.1		0.1		0.1	
V/- :	I _{OL} = 12 mA	3 V		0.36		0.5		0.44	.,
VOL	21 - 2	4.5 V		0.36		0.5		0.44	V
	I _{OL} = 24 mA	5.5 V		0.36		0.5		0.44	
	I _{OL} = 50 mA [†]	5.5 V				1.65			
	I _{OL} = 75 mA [†]	5.5 V						1.65	
l _l	V _I = V _{CC} or GND	5.5 V		± 0.1		± 1		± 1	μΑ
lcc	V _I = V _{CC} or GND, I _O = 0	5.5 V		4		80		40	μΑ
Ci	VI = VCC or GND	5 V		4					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Note 2)

	FROM	TO	T _A = 25°C		54AC11802		74AC11802			
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	A or B	Υ		5.6						
tPHL				5.1						ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM	TO	T _A = 25°C		54AC11802		74AC11802		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
tPLH	A or B	Υ		3.8						
^t PHL				3.8						ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT	١
C _{pd} Power dissipation capacitance per gate	C _L = 50 pF, f = 1 MHz	27	pF	ĺ

- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- 500-mA Typical Latch-Up Immunity at 125°C
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'ACT11802 contains three independent 4-input AND/NAND gates. They perform the Boolean functions in positive logic Y = A + B + C + D and $Z = \overline{A + B + C + D}$. These devices are designed to have low skew between outputs for clock driver applications.

The 54ACT11802 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11802 is characterized for operation from -40°C to 85°C.

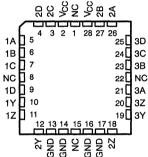
FUNCTION TABLE

	INP	OUT	PUTS		
Α	В	С	D	Υ	Z
Н	Х	Х	X	Н	L
X.	Н	Х	Х	Н	L
X	Х	Н	X	Н	L
X	X	X	Н	Н	L
L	L	L	L	L	Н

54ACT11802 ... JT PACKAGE 74ACT11802 ... DW OR NT PACKAGE (TOP VIEW)

			L
1D[1	O 24] 1C
1Y[2	23] 1B
1Z[3	22] 1A
2Y[4	21] 2D
GND[5	20	2C
GND[6	19] v _{cc}
GND[7	18] V _{CC}
GND[8	17] 2B
2Z[9	16] 2A
3Y[10	15] 3D
3Z[11	14] 3C
3A[12	13] 3B

54ACT11802 . . . FK PACKAGE (TOP VIEW)



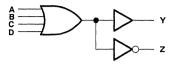
NC - No internal connection

EPIC is a trademark of Texas Instruments Incorporated.



logic symbol† 22 ≥ 1 23 24 1 16 2Α 17 2B 20 21 2D 12 зА 10 13 3B 14 11

logic diagram (positive logic) (one section)



Pin numbers shown are for DW, JT, and NT packages.

3D 15

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	— 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	\dots – 0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	0.5V to $ \text{V}_{\text{CC}} + 0.5 \text{V}$
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	± 20mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50mA
Continuous current through V _{CC} or GND pins	± 150mA
Storage temperature range	– 65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		54ACT1180		74ACT	11802	UNIT
		MIN			MIN MAX	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2			2	٧
VIL	Low-level input voltage		0.8		0.8	٧
VI	Input voltage	0	Vcc	0	Vcc	V
Vo	Output voltage	0	Vcc	0	Vcc	٧
10H	High-level output current		- 24		- 24	mA
lOL	Low-level output current		24		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	0	10	ns/V
TA	Operating free-air temperature	- 55	125	- 40	85	°C



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Pulbication 617-12.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54ACT11802, 74ACT11802 TRIPLE 4-INPUT OR/NOR CLOCK DRIVERS

D3594, JULY 1990

electrical characteristics over recomended operating free-air temperature range (unless otherwise noted)

			T,	_A = 25°C		54ACT	11802	74ACT		
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
	. 50 4	4.5 V	4.4			4.4		4.4		
	IOH = - 50 μA	5.5 V	5.4			5.4		5.4		
.,		4.5 V	3.94			3.7		3.8		v
Voн	I _{OH} = - 24 mA	5.5 V	4.94			4.7		4.8		٧
	IOH = - 50 mA †	5.5 V				3.85				
	IOH = -75 mA †	5.5 V						3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	
	ΙΟΓ = 50 μΑ	5.5 V			0.1		0.1		0.1	
.,	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	V
VOL		5.5 V			0.36		0.5		0.44	V
	IOL = 50 mA †	5.5 V					1.65			
	IOL = 75 mA †	5.5 V							1.65	
1μ	VI = VCC or GND	5.5 V			± 0.1		± 0.1		± 0.1	mA
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	mA
ΔICC [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA
Ci	VI = VCC or GND	5 V		4						pF

T Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Note 2)

	FROM	то	T,	Δ = 25°C	;	54AC	1802	74AC1	1802	I
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
[†] PLH	A or B	V		3.8						
^t PHL		T		3.8						ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT	l
Cpd Power dissipation capacitance per gate	C _L = 50 pF, f ≈ 1 MHz	27	pF	ı



[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather that 0 V to V_{CC}.

SN74AS303 . . . D[†] OR N PACKAGE (TOP VIEW)

Q3

Q4II 2

GND 3

GND 1 4

GND 1 5

റദി

Q5 1 6

7 <u>0</u>7[

16 1 02

15 T Q1

14 TCLR

13 1 VCC

12 VCC

11 CLK

10 PRE

a∏ <u>G</u>8

D3543, JULY 1990

- Maximum Output Skew of 1 ns
- Maximum Pulse Skew of 1 ns
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include Plastic"Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The SN74AS303 contains eight flip-flops designed to have low skew between outputs. The † Contact factory for information on availability of S.O. package.

eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. PRE and CLR inputs are provided to set the Q and $\overline{\mathbf{Q}}$ outputs high or low independent of the CLK pin.

The 'AS303 has output and pulse skew parameters $t_{sk(0)}$ and $t_{sk(0)}$ to ensure performance as a clock driver when a divide-by-two function is required.

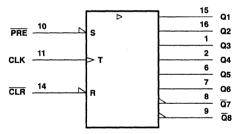
The SN74AS303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUT	PUTS
CLR	PRE	CLK	Q1-Q6	Q7-Q8
L	Н	×	L	Н
н	L	Х	н	L
L	L	X	L‡	L‡
н	н	†	\overline{Q}_0	Q_0
Н	Н	L	Q ₀	\overline{a}_{0}

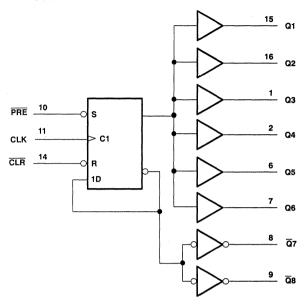
[‡] This configuration will not persist when PRE or CLR returns to its inactive (high) level.

logic symbol§



[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	
Input voltage, V _I	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range—65	°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ГОН	High-level output current			- 24	mA
loL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C



D3543, JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	ITIONS	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	i _I = – 18 mA			- 1.2	٧
Voн	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = - 2 mA	vcc-	2		V
VOH _	V _{CC} = 4.5 V,	I _{OH} = – 24 mA	2	2.8		· ·
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.3	0.5	V
lj .	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
Iн	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
IIL	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.5	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 50		- 150	mA
lcc	V _{CC} = 5.5 V,	See Note 1		40	70	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements (see Note 2)

		PARAMETER	MIN	MAX	UNIT
fclock	Clock frequency		0	80	MHz
		CLR or PRE low	5		
tw	Pulse duration	CLK high	4		ns
		CLK low	6		
t _{su}	Setup time before CLK↑	CLR or PRE inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f _{max} §				80		MHz
^t PLH		Q, \overline{Q}		2	9	ns
^t PHL	CLK	Q, Q	$R_L = 500 \Omega$, $C_L = 50 pF$	2	9	ns
t _{PLH}		. =		3	12	ns
t _{PHL}	PRE or CLR	Q, $\overline{\mathbf{Q}}$	$R_L = 500 \Omega$, $C_L = 50 pF$	3	12	ns
		Q			1	
^t sk(o)	CLK	Q	$R_L = 500 \Omega$, $C_L = 10 pF to 30 pF$		1	ns
		Q, Q			2	
t _{sk(p)}	CLK	Q, Q	$R_L = 500 \Omega$, $C_L = 10 pF to 30 pF$		1	ns
t _r					4.5	ns
tf					3.5	ns

§ f_{max} minimum values are at C_L = 0 to 30 pF.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS. NOTE 1: ICC is measured with CLK and PRE grounded, then with CLK and CLR grounded.

D3555, JULY 1990

Maximum Output Skew of 1 ns

- Maximum Pulse Skew of 1 ns
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include Plastic"Small Outline" Packages, and Standard Plastic 300-mil DIPs

description

The SN74AS304 contains eight flip-flops designed to have low skew between outputs. The eight outputs (in-phase with CLK) toggle on successive CLK pulses. PRE and CLR pins are provided to set the Q outputs high or low independent of the CLK input.

The SN74AS304 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(o)}$ to ensure performances as a clock driver when a divide-by-two function is required.

The SN74AS304 is characterized for operation from 0°C to 70°C.

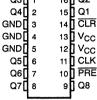
FUNCTION TABLE

INPUTS			OUTPUTS
CLR	PRE	CLK	Q1-Q8
L	Н	X	L
Н	L	X	н
L	L	×	L†
н	Н	1	\overline{Q}_0
н	Н	L	Q ₀

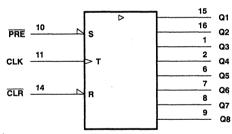
[†] This configuration will not persist when PRE or CLR returns to its inactive (high) level.

Q3 16N Q2 15 Q1

D OR N PACKAGE (TOP VIEW)

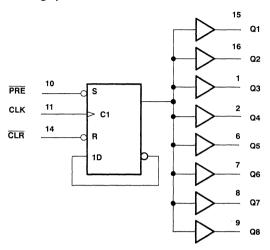


logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V ₁	7 V
Operating free-air temperature range)°C
Storage temperature range	٥°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

						
			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
ЮН	High-level output current				- 24	mA
lOL	Low-level output current				48	mA
TA	Operating free-air temperature		0		70	°C

SN74AS304 OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

D3555 JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	MIN TY	PT MAX	UNIT
VIK .	V _{CC} = 4.5 V,	l _l = – 18 mA		- 1.2	٧
Vou	V _{CC} = 4.5 V,	I _{OH} = - 2 mA	Vcc ⁻²		V
Voн	V _{CC} = 4.5 V,	I _{OH} = − 24 mA	2 2	2.8	ľ
VOL	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.5	V
l _l	V _{CC} = 5.5 V,	V _I = 7 V		0.1	mA
¹IH	V _{CC} = 5.5 V,	V _I = 2.7 V		20	μА
IL	V _{CC} = 5.5 V,	V _I = 0.4 V		- 0.5	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	- 50	- 150	mA
lcc	V _{CC} = 5.5 V,	See Note 1		45 75	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements (see Note 2)

		PARAMETER	MIN	NOM	MAX	UNIT
fclock	Clock frequency		0		80	MHz
		CLK high	4			
tw	Pulse duration	CLK low	6			ns
		CLR or PRE low	5			
t _{su}	Setup time before CLK↑	CLR or PRE inactive	6			ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max} §				80			MHz
^t PLH				2	6	9	
t _{PHL}	CLK	Q	$R_L = 500 \Omega$, $C_L = 50 pF$	2	6	9	ns
t _{PLH}	555 015		D 500 0 50 5	3	7	12	
^t PHL	PRE or CLR	Q	$R_L = 500 \Omega$, $C_L = 50 pF$	3	7	12	ns
tsk(o)	CLK	Q	$R_L = 500 \Omega$, $C_L = 10 pF to 30 pF$			1	ns
		Q1, Q8				1	
^t sk(p)	CLK	Q2 to Q7	$R_L = 500 \Omega$, $C_L = 10 pF to 30 pF$			1.5	ns
t _r						4.5	ns
tf						3.5	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. NOTE 1: I_{CS} is measured with CLK and PRE grounded, then with CLK and CLR grounded.

[§] f_{max} minimum values are at C_L = 0 to 30 pF.

- Maximum Output Skew of 1 ns
- Maximum Pulse Skew of 1 ns
- Center Pin V_{CC} and GND Configurations
 Minimize High-Speed Switching Noise
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

The SN74AS305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. PRE and CLR inputs are provided to set the Q and Q outputs high or low independent of the CLK pin.

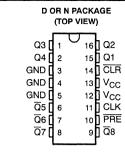
The SN74AS305 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to guarantee performances as a clock driver when a divide-by-two function is required.

The SN74AS305 is characterized for operation from 0°C to 70°C.

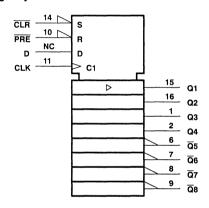
FUNCTION TABLE

INPUTS			OUTPUTS		
CLR	PRE	CLK	Q1-Q4	Q5-Q8	
L	Н	Х	L	Н	
Н	L	X	н	L	
L	L	X	H [†]	H†	
Н	Н	L	Q ₀	$\overline{\alpha}_0$	
Н	Н	1	$\overline{\Omega}_0$	Q_0	

[†] This configuration will not persist when PRE or CLR returns to its inactive (high) level.

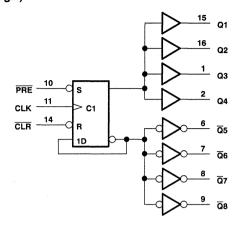


logic symbol‡



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}		
Input voltage, V _I		7 V
Operating free-air temperature range:	SN54AS305	– 55°C to 150°C
	SN74AS305	0°C to 70°C
Storage temperature range		– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vсс	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ЮН	High-level output current			- 24	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = – 18 mA			- 1.2	V
Voн	V _{CC} = 4.5 V		V _{CC} -2			V
VOH .	V _{CC} = 4.5 V,	I _{OH} = – 24 mA	2	2.8		V
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.3	0.5	٧
lį	$V_{CC} = 5.5 \text{ V},$	V _I = 7.0 V			0.1	mA
IH	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20	μΑ
ارا	$V_{CC} = 5.5 V$,	V _I = 0.4 V			0.5	mA
I _O	V _{CC} = 5.5 V,	V _I = 2.25 V	- 50		- 200	mA
lcc	V _{CC} = 5.5 V,	See Note 1		34	55	mA

 † All typical values are at VCC = 5 V, TA = 25°C. NOTE 1: ICC is measured with CLK and $\overline{\text{PRE}}$ grounded, then with CLK and $\overline{\text{CLR}}$ grounded.

timing requirements (see Note 2)

		PARAMETER	MIN	NOM	MAX	UNIT
fclock	Clock frequency		0		100	MHz
		CLK high	4			
tw	t _w Pulse duration	CLK low	5			ns
		CLR or PRE low	5			İ
t _{su}	Setup time	CLR or PRE inactive	6			ns

switching characteristics over recommended operating free-air temperature range (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	мах	UNIT
fmax [‡]				100			MHz
t _{PLH}	0114	7 0 5	$R_L = 500 \Omega$, $C_L = 50 pF$,	2	6	8	
t _{PHL}	CLK	Q, Q		2	6	8	ns
tPLH	PRE or CLR	Q, $\overline{\mathbf{Q}}$	V _{CC} = 4.5 V to 5.5 V	3	7	10	
tPHL.	PRE OF CLA	u, u		3	7	10	ns
tsk(o)	CLK	Q, Q	$R_L = 500 \Omega$,			1	ns
tsk(p)	CLK	u, u	C _L = 50 pF,			1	113
t _r or t _f			V _{CC} = 4.75 V to 5.25 V			3	ns

† f_{max} minimum values are at C_L = 0 to 30 pF.
NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

General Information	1
ACL LSI Products	2
ACL Widebus™ Products	3
BTL Transceiver Products	4
Bus-Termination Array Products	5
Clock Driver Products	6
ECL/TTL Translator Products	7
ECL/TTL Translator Products	
FIFO Products	8
FIFO Products	8
FIFO Products Low-Impedance Line Driver Products	8
FIFO Products Low-Impedance Line Driver Products Memory Driver Products	8 9 10

D3491, MARCH 1990

- 10KH Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus oriented functions such as memory address drivers. clock drivers. and oriented receivers and transmitters while eliminating the need for three-state overlap protection.

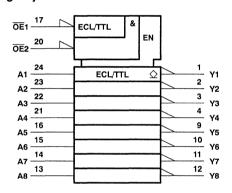
Two output enables, $\overline{\text{OE}}1$ and $\overline{\text{OE}}2$, are provided. These enable inputs are ANDed together with $\overline{\text{OE}}1$ being ECL-compatible and $\overline{\text{OE}}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5538 is characterized for operation from 0°C to 75°C.

DW OR NT PACKAGE (TOP VIEW)

	•		
Y1[Y2[Y3[Y4[V _{CC}] GND[GND[GND[GND[Y5[Y6]		23 22 21 20 19 18 17 16	A1 A2 A3 OE2 (TTL) VEE GND OE1 (ECL) A5 A6
Y7[-
Y8[12	13] A8

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

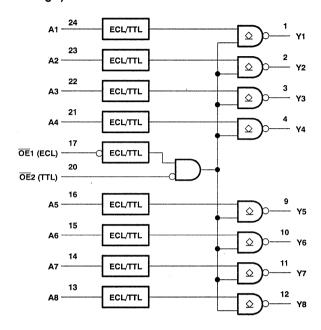
FUNCTION TABLE

OUTPUT ENABLE		DATA INPUT	OUTPUT (TTL)
OE1 OE2		Α	Υ
Н	Х	Х	Н
Х	Н	X	Н
L	L	L	н
L	L	Н	L



D3491, MARCH 1990

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	\dots $-0.5V$ to $7V$
Supply voltage range, VEE	
Input voltage range (TTL) (see Note 1)	– 1.2 V to 7 V
Input voltage range (ECL)	V _{EE} to 0 V
Input current range (TTL)	30 mA to 5 mA
Current into any output in the low state	96 mA
Voltage applied to any output in the high state	$\dots - 0.5 \text{ V to V}_{CC}$
Operating temperature range	0°C to 75°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



D3491, MARCH 1990

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage			5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	V
VIH	TTL high-level input voltage		2			٧
VIL	TTL low-level input voltage				0.8	V
		0°C	- 1170		- 840	mV
VIH	ECL high-level input voltage (see Note 2)	25°C	- 1130		- 810	mV
		75°C	- 1070		- 735	mV
		0°C	- 1950		- 1480	mV
VIL	ECL low-level input voltage (see Note 2)	25°C	- 1950		- 1480	mV
		75°C	- 1950		- 1450	mV
Vон	TTL high-level output voltage				5.5	V
lor	TTL low-level output current				48	mA
ΊΚ	TTL input clamp current				- 18	mA
TA	Operating free-air temperature		0	***************************************	75	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	T	TEST CONDITIO	NS		MIN	TYP [†]	MAX	UNIT	
VIK	OE2 only	V _{CC} = 4.5 V,	V _{EE} = - 4.94 V,	l _I = - 18 mA				- 1.2	V	
Ц	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 7 V				0.1	mA	
ΊΗ	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 2.7 V				20	μА	
ΗL	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 0.5 V				- 0.5	mA	
		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 840 V	0°C			350		
чн	A inputs and OE1	$V_{CC} = 5.5 V$,	V _{EE} = - 5.46 V,	V _I = - 810 V	25°C			350	μΑ	
		$V_{CC} = 5.5 \text{ V},$	V _{EE} = - 5.46 V,	V _I = - 735 V	75°C			350		
						0°C	0.5			
l _{IL}	A inputs and OE1	V _{CC} = 5.5 V,	$V_{EE} = -5.46 V_{r}$	$V_{I} = -1950 V$	25°C	0.5			μΑ	
					75°C	0.5				
ЮН		V _{CC} = 4.5 V,	V _{EE} = - 4.94 V,	V _{OH} = 5.5 V				250	μΑ	
VOL		V _{CC} = 4.5 V,	$V_{EE} = -5.2 \text{ V} \pm 5\%$	I _{OL} = 48 mA			0.38	0.55	٧	
ССН		V _{CC} = 5.5 V,	V _{EE} = 5.46 V				66	95	mA	
^I CCL		V _{CC} ≈ 5.5 V,	V _{EE} = - 5.46 V				79.5	114	mA	
IEE		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				- 23	- 33	mA	
Ci		V _{CC} = 5.5 V,	V _{EE} = - 5.2 V				5		рF	
Со		V _{CC} = 5.5 V,	V _{EE} = - 5.2 V				5		pF	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

SN10KHT5538 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS D3491, MARCH 1990

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	C _L R1 R2	UNIT		
			MIN	TYP	MAX	
^t PLH	Any A	Y	6.4	9.1	11.7	ns
t _{PHL}		T T	2.7	4.9	7.2	
tPLH		_	7	10.1	13.3	
t _{PHL}	OE1 (ECL)	ľ	3.6	6.2	8.8	ns
^t PLH	OE2 (TTL)	V	6.5	9.1	11.6	ns
^t PHL	0L2 (11L)	<u>'</u>	2.8	5.3	7.9	115

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.
NOTE 3: Load circuit and voltage waveforms are shown in Section 1.

D3493, APRIL 1990

- 100K Compatible
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- ECL and TTL Control inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

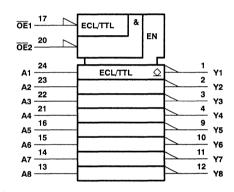
Two output enables, $\overline{OE}1$ and $\overline{OE}2$, are provided. These enable inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5538 is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE (TOP VIEW)

Y1[1 U	24 A1
Y2[2	23 A2
Y3[3	22 A3
Y4[4	21 🛮 A4
Vcc[5	20 OE2 (TTL)
GND[6	19 🕽 V _{EE}
GND[7	18 GND
GND[8	17 OE1 (ECL)
Y5[9	16 🛮 A5
Y6[10	15 🛮 A6
Y7[11	14 🛮 A7
Y8[12	13 🛮 A8
1		

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

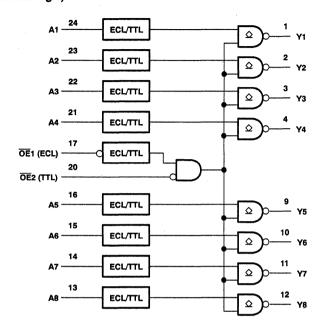
FUNCTION TABLE

	OUT	PUT BLE	DATA INPUT	OUTPUT (TTL)
	OE1 OE2		Α	Υ
	Н	Х	X	Н
1	Х	Н	х	н
	L	L	L	н
	L	L_	н	L



D3493, APRIL 1990

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Supply voltage range, VEE	– 8 V to 0 V
Input voltage range (TTL) (see Note 1)	– 1.2 V to 7 V
Input voltage range (ECL)	V _{EE} to 0 V
Input current range (TTL)	– 30 mA to 5 mA
Current into any output in the low state	96 mA
Voltage applied to any output in the high state	– 0.5 V to V _{CC}
Operating temperature range	0°C to 85°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



D3493, APRIL 1990

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	V
VEE	ECL supply voltage		- 4.2	- 4.5	- 4.8	V
		TTL	2			V
VIH	High-level input voltage	ECL (see Note 2)	- 1150		840	mV
	A section A section	TTL			0.8	٧
VIL	Low-level input voltage	ECL (see Note 2)	- 1810		- 1490	mV
Vон	TTL high-level output voltage				5.5	V
IOL	TTL low-level output current				48	mA
liK	TTL input clamp current				- 18	mA
TA	Operating free-air temperature		0		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Vik	OE2 only	V _{CC} = 4.5 V,	VEE = - 4.2 V,	l _j = – 18 mA			- 1.2	V
VOL		V _{CC} = 4.5 V,	VEE = - 4.5 V ± 0.3 V,	I _{OL} = 48 mA		0.38	0.55	٧
l _l	OE2 only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 7 V			0.1	mA
	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 2.7 V			20	
ИН	A inputs and OE1	V _{CC} = 5.5 V,	VEE = 4.8 V,	V _I = - 840 mV			350	μΑ
	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V ₁ = 0.5 V			- 0.5	mA
IIL	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 1810 mV	0.5			μΑ
ЮН		V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	V _{OH} = 5.5 V			250	μΑ
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			66	95	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			79.5	114	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 4.2 V			- 23	- 33	mA
Ci		V _{CC} = 5.5 V,	V _{EE} = - 4.5 V			5		pF
Со		V _{CC} = 5.5 V,	V _{EE} = - 4.5 V			5		рF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	UNIT		
			MIN	TYP†	MAX	
t _{PLH}	Any A		6.4	9.1	11.7	
^t PHL		Y	2.7	4.9	7.2	ns
tPLH	OE1 (ECL)		7	10.1	13.3	
t _{PHL}		Y	3.6	6.2	8.8	ns
^t PLH	ŌĒ2 (TTL)		6.5	9.1	11.6	
t _{PHL}		Y	2.8	5.3	7.9	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C. NOTE 3: Load circuit and voltage waveforms are shown in Section 1.



SN10KHT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

D3421, JANUARY 1990-REVISED OCTOBER 1990

10KH Compatible	DW OR NT PACKAGE (TOP VIEW)
 Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers 	Y1 1 24 A1 Y2 2 23 A2
ECL and TTL Output-Enable Inputs	Y3 🛛 3 22 🗍 A3
 Flow-Through Architecture Optimizes PCB Layout 	Y4 [] 4 21 [] A4 V _{CC} [] 5 20 [] OE2 (TTL) GND [] 6 19 [] V _{EE}
 Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise 	GND [7 18] GND GND [8 17] OE1 (ECL) Y5 [9 16] A5
 Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs 	Y6] 10 15] A6 Y7] 11 14] A7 Y8 [12 13] A8

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for 3-state overlap protection.

Two pins $\overline{\text{OE}}1$ and $\overline{\text{OE}}2$ are provided for output-enable control. These control inputs are ANDed together with $\overline{\text{OE}}1$ being ECL-compatible and $\overline{\text{OE}}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

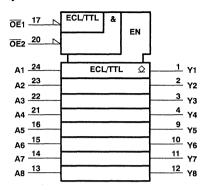
The SN10KHT5539 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

OUTPUT		DATA	OUTPUT
ENABLE		INPUT	(TTL)
OE1 OE2		A	Y
Х	Н	X	Н
н	X	x	н
L	L	L	L
L	L	Н	Н

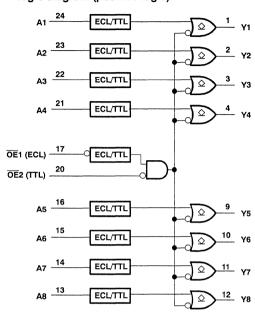
D3421, JANUARY 1990-REVISED OCTOBER 1990

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC}	0.5 V to 7 V
Supply voltage range, V _{FF}	
Input voltage range: TTL (see Note 1)	– 1.2 V to 7 V
ECL`	V _{EE} to 0 V
Input current range, TTL	- 30 mA to 5 mA
Current into any output in the low state	96 mA
Voltage applied to any output in the high state	0.5 V to V _{CC}
Operating free-air temperature range	0°C to 75°C
Storage temperature range	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

SN10KHT5539 **OCTAL ECL-TO-TTL TRANSLATOR** WITH OPEN-COLLECTOR OUTPUTS D3421, JANUARY 1990-REVISED OCTOBER 1990

recommended operating conditions

	1.		MIN	NOM	MAX	UNIT
V _{CC} TTL supply voltage			4.5	5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	٧
VIH	VIH TTL high-level input voltage					V
V _{IL} TTL low-level input voltage					0.8	V
		T _A = 0°C	1170		- 840	mV
VIH		T _A = 25°C	- 1130		-810	
		T _A = 75°C	- 1070		- 735	
		T _A = 0°C	- 1950		- 1480	
VIL	ECL low-level input voltage†	T _A = 25°C	- 1950		- 1480	mV
	T _A = 75°C		- 1950		- 1450	
Vон	TTL high-level output voltage				5.5	٧
ΙΚ	TTL input clamp current				- 18	mA
lOL	IOL Low-level output current				48	mA
TA	Operating free-air temperature range		0		75	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS		MIN	TYP‡	MAX	UNIT
VIK	OE2 only	V _{CC} = 4.5 V,	V _{EE} = - 4.94 V,	l _I = – 18 mA				- 1.2	V
ЮН		V _{CC} = 4.5 V,	V _{EE} = - 4.94 V,	V _{OH} = 5.5 V				250	μΑ
VOL	- August ser samurana en samura en samura en samura en samura en samura en samura en samura en samura en samura	V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$	I _{OL} = 48 mA			0.38	0.55	V
ų	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 7 V				0.1	mA
ΊΗ	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 2.7 V				20	μΑ
IIL	OE2 only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 0.5 V				- 0.5	mA
ΉΗ	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _i = - 840 mV	T _A = 0°C			350	μΑ
		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = - 810 mV	T _A = 25°C			350	
		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = - 735 mV	T _A = 75°C			350	
		V _{CC} = 5.5 V, V _{EE} = -1	V _{EE} = - 5.46 V,	••	T _A = 0°C	0.5			
ΊL	A inputs and OE1				T _A = 25°C	0.5			μΑ
	1				T _A = 75°C	0.5			
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				63	91	mA
ICCL		V _{CC} = 5.5 V,	VEE = - 5.46 V		, , , , , , , , , , , , , , , , , , , ,		79	114	mA
1EE		V _{CC} = 5.5 V,	VEE = - 5.46 V				- 22	- 32	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 5.2 V				6		pF
Co		V _{CC} = 5 V,	V _{EE} = - 5.2 V				5		pF

 $^{^\}ddagger$ All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

SN10KHT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

D3421, JANUARY 1990-REVISED OCTOBER 1990

switching characteristics over recommended ranges of operating supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega$			UNIT
			MIN	TYP†	MAX	
tPLH			6.2	9.3	12.4	
^t PHL	Any A	Y	2.6	4.9	7.3	ns
[†] PLH			7.1	10.3	13.5	
[†] PHL	OE1 (ECL)	Y	3.2	5.8	8.4	ns
^t PLH			6.5	9.5	12.4	
tPHL	OE2 (TTL)	Y	2.7	5.3	8	ns

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN100KT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

D3422, JANUARY 1990-REVISED OCTOBER 1990

100K Compatible	DW OR NT PACKAGE (TOP VIEW)
 Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers 	Y1 1 24 A1 Y2 2 23 A2
ECL and TTL Output-Enable Inputs	Y2 [] 2 23 [] A2 Y3 [] 3 22 [] A3
 Flow-Through Architecture Optimizes PCB Layout 	Y4
 Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise 	GND 7 18 GND GND 8 17 OE1 (ECL) Y5 9 16 A5
 Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs 	Y6

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters while eliminating the need for three-state overlap protection.

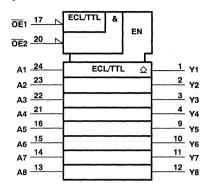
Two pins $\overline{OE}1$ and $\overline{OE}2$ are provided for output-enable control. These control inputs are ANDed together with $\overline{OE}1$ being ECL-compatible and $\overline{OE}2$ being TTL-compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5539 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

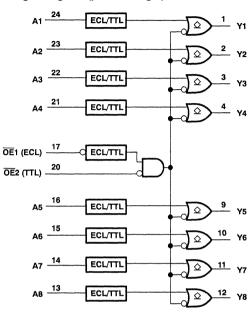
OUTPUT		DATA	OUTPUT
ENABLE		INPUT	(TTL)
OE1	OE2	A	Υ
Н	×	X	Н
X	Н	X	н
L	L	L	L
L	L	н	Н

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC}	
Supply voltage range, V _{EE}	– 8 V to 0 V
Input voltage range: TTL (see Note 1)	
ECL	V _{EE} to 0 V
Input current range: TTL	– 30 mA to 5 mA
Voltage applied to any output in the high state	– 0.5 V to V _{CC}
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 85°C
Storage temperature range	– 65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

SN100KT5539 OCTAL ECL-TO-TTL TRANSLATOR WITH OPEN-COLLECTOR OUTPUTS

D3422, JANUARY 1990-REVISED OCTOBER 1990

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	V
VEE	ECL supply voltage	- 4.2	- 4.5	- 4.8	٧
VIH	TTL high-level input voltage	2			٧
VIL	TTL low-level input voltage			0.8	V
VIH	ECL high-level input voltage [†]	- 1150		- 840	mV
VIL	ECL low-level input voltage [†]	- 1810		- 1490	mV
Vон	TTL high-level output voltage			5.5	٧
loL	TTL low-level output current			48	mA
^I IK	TTL input clamp current			- 18	mA
TA	Operating free-air temperature range	0		85	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	S	MIN	TYP‡	MAX	UNIT
VIK	OE2 only	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	lj = 18 mA			- 1.2	V
ЮН		V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	V _{OH} = 5.5 V			250	μΑ
VOL		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	IOL = 48 mA		0.38	0.55	V
l _i	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 7 V			0.1	mA
	OE2 only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 2.7 V			20	μΑ
Ιн	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _j = 840 mV			350	μΑ
	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
l _{IL}	A inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 1810 mV	0.5			μΑ
^I CCH		V _{CC} = 5.5 V,	VEE = - 4.8 V			63	91	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			79	114	mA
1EE		V _{CC} = 5.5 V,	VEE = - 4.2 V			- 22	- 32	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 4.5 V			6		pF
Co		V _{CC} = 5 V,	V _{EE} = - 4.5 V			5		pF

[‡] All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

SN100KT5539 **OCTAL ECL-TO-TTL TRANSLATOR** WITH OPEN-COLLECTOR OUTPUTS D3422, JANUARY 1990-REVISED OCTOBER 1990

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	то (оитрит)	R	L = 50 pl 1 = 500 £ 2 = 500 £	2,	UNIT
			MIN	TYP	MAX	1
tPLH	A A		6.2	9.3	12.4	
t _{PHL}	Any A	, , , , , , , , , , , , , , , , , , ,	2.6	4.9	7.3	ns
^t PLH	<u> </u>	_	7.1	10.3	13.5	
t _{PHL}	OE1 (ECL)	,	3.2	5.8	8.4	ns
tPLH	ŌĒ2 (TTL)	· ·	6.5	9.5	12.4	ns
tPHL temperature	OLZ (TTL)	'	2.7	5.3	8	2

[†] All typical values are at V_{CC} = 5 V, V_{EE} = - 4.5 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN10KHT5540 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3392, DECEMBER 1989

- 10KH Compatible
- ECL and TTL Control Inputs
- Inverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

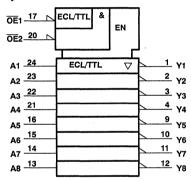
The SN10KHT5540 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

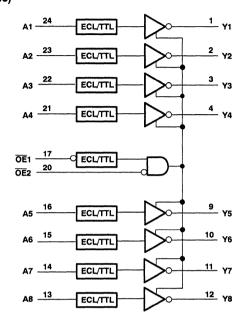
			,	
	OUTPUT		DATA	OUTPUT
	ENABLE		INPUT	(TTL)
	OE1	OE2	Α	Υ
İ	X	Н	X	Z
	н	×	x	z
	L	L	L	H.
į	L	L	н	L

DW OR NT PACKAGE (TOP VIEW) 24 A1 Y2 1 2 23 A2 Y3 🗖 3 22 A3 21 A4 20 OE2 (TTL) V_{CC} [] 5 GND I 6 19 VEE GND 7 18 GND GND 8 17 OE1 (ECL) Y5 ∏ 9 16 A5 Y6 1 10 15 A6 Y7 11 14 A7 Y8 12 13 A8

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.



SN10KHT5540 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3392, DECEMBER 1989

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-05Vto7V
Supply voltage range, V _{EE}	– 8 V to 0 V
Input voltage range (TTL) (see Note 1)	– 1.2 V to 7 V
Input voltage range (ECL)	V _{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to V _{CC}
Input current range (TTL)	- 30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	٧
VIH	TTL high-level input voltage		2			V
VIL	TTL low-level input voltage	-			0.8	٧
V _{IH} ‡		T _A = 0°C	1170		- 840	
		T _A = 25°C	- 1130		- 810	mV
		T _A = 75°C	- 1070		- 735	
	ECL low-level input voltage	T _A = 0°C	- 1950		- 1480	
V _{IL} ‡		T _A = 25°C	- 1950		- 1480	mV
	T _A = 75°C				- 1450	
ΊΚ	TTL input clamp current				- 18	mA
ЮН	High-level output current				- 15	mA
loL	Low-level output current				48	mA
TA	Operating free-air temperature				75	°C

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

SN10KHT5540 **OCTAL ECL-TO-TTL TRANSLATOR** WITH 3-STATE OUTPUTS

D3392, DECEMBER 1989

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER TEST CONDITIONS				MIN	TYP†	MAX	UNIT	
VIK	OE2 only	V _{CC} = 4.5 V,	VEE = - 4.94 V,	l _l = - 18 mA				- 1.2	٧
		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$,	I _{OH} = - 3 mA		2.4	3.3		
∨он		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$,	I _{OH} = - 15 mA		2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$,	1 _{OL} = 48 mA			0.38	0.55	V
lį	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _l = 7 V				0.1	mA
ΊΗ	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 2.7 V				20	μA
IIL	OE2 only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 0.5 V				- 0.5	mA
		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = - 840 mV	T _A = 0°C			350	
ΉΗ	Data inputs and OE1	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = - 810 mV	T _A = 25°C			350	μΑ
		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = - 735 mV	T _A = 75°C			350	
	Data inputs and OE1			T _A = 0°C	0.5				
liL.		Data inputs and OE1	1 V _{CC} = 5.5 V, V _{EE} = -5	$V_{EE} = -5.46 V_{r}$	$V_{i} = -1950 \text{mV}$	T _A = 25°C	0.5		
					T _A = 75°C	0.5			
lozh		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 2.7 V				50	μΑ
lozL		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _O = 0.5 V				- 50	μА
los‡		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 0		- 100		- 225	mA
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				67	97	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				84	120	mA
Iccz		V _{CC} = 5.5 V,	VEE = - 5.46 V				81	116	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				- 23	- 33	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 5.2 V				5		pF
Co		V _{CC} = 5 V,	V _{EE} = - 5.2 V				7		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R	L = 50 pl 1 = 500 £ 2 = 500 £	2,	UNIT
			MIN	TYP†	MAX	
t _{PLH}	А	Y	1.6	3.9	6.4	ns
tPHL	A	τ	1.6	4.2	6.4	115
^t PZH	ŌĒ1	Y	2.4	4.5	6.9	
tpZL	OEI	Υ	3.5	5.9	8.7	ns
tPHZ	ŌĒ1	Υ	2.8	5.2	8.1	ns
t _{PLZ}	021		2.2	4.6	8	110
^t PZH	ŌĒ2	Υ	1.4	3.3	6.1	ns
^t PZL	OLZ	,	2.5	4.7	7.9	113
t _{PHZ}	ŌĒ2	Y	1.6	4.1	6.5	
tPLZ	UE2	Υ	0.7	3.3	6.4	ns

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C. ‡ Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

SN100KT5540 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3393, DECEMBER 1989

100K Compatible

- **Inverting Outputs**
- **ECL and TTL Control Inputs**
- Flow-Through Architecture Optimizes PCB Lavout
- Center Pin V_{CC}, V_{EE}, and GND **Configurations Minimize High-Speed** Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, OE1 and OE2, are provided. These control inputs are ANDed together with OE1 being ECL compatible and OE2 being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

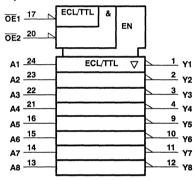
The SN100KT5540 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

OUTPUT		DATA	OUTPUT
ENABLE		ENABLE INPUT	
OE1 OE2		Α	Υ
X	Н	X	Z
Н	X	X	Z
L	L	L	Н
L	L	Н	L

DW OR NT PACKAGE (TOP VIEW) Y1 [1 24 N A1 Y2 1 2 23 A2 Y3 🗍 3 22 A3 Y4 🛮 4 21 A4 20 TOE2 (TTL) V_{CC} [] 5 GND 1 6 19 V_{EE} GND 7 18 GND GND 🖥 8 17 OE1 (ECL) Y5 🕇 9 16 A5 Y6 1 10 15 A6 Y7 11 14 A7 Y8 🚺 12 13 A8

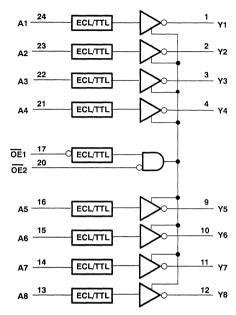
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	\dots - 0.5 V to 7 V
Supply voltage range, VEE	– 8 V to 0 V
Input voltage range: TTL (see Note 1)	– 1.2 V to 7 V
ECL	V _{EE} to 0 V
Voltage applied to any output in the high state	0.5 V to V _{CC}
Voltage applied to any output in the disabled or power-off state	– 0.5 V to 5.5 V
Input current range (TTL)	– 30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 85°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



SN100KT5540 OCTAL ECL-TO-TTL TRANSLATOR **WITH 3-STATE OUTPUTS**

D3393, DECEMBER 1989

recommended operating conditions.

		MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	٧
VEE	ECL supply voltage	4.2	- 4.5	- 4.8	٧
VIH	TTL high-level input voltage	2			٧
VIL	TTL low-level input voltage			0.8	٧
VIH	ECL high-level input voltage [†]	- 1150		- 840	mV
VIL	ECL low-level input voltage [†]	- 1810		- 1490	mV
^I IK	TTL input clamp current			- 18	mA
Іон	High-level output current			- 15	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		85	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	3	MIN	TYP‡	MAX	UNIT
VIK	OE2 only	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	l _l = - 18 mA			- 1.2	٧
		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	IOH = - 3 mA	2.4	3.3		
Vон		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	I _{OH} = - 15 mA	2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V},$	I _{OL} = 48 mA		0.38	0.55	٧
l ₁	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 7 V			0.1	mA
Iн	OE2 only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 2.7 V			20	μΑ
IIL	OE2 only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
lн	Data inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IH} = - 840 mV			350	μΑ
IIL	Data inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IL} = ~ 1810 mV	0.50			μΑ
lozh		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 2.7 V			50	μΑ
lozL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 0.5 V			- 50	μA
los§		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	VO = 0 V	- 100		- 225	mA
ICCH		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			67	97	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			84	120	mA
Iccz		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			81	116	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			- 22	- 33	mA
Ci		V _{CC} = 5 V,	V _{EE} = 4.5 V			5		pF
Co		V _{CC} = 5 V,	V _{EE} = 4.5 V			7		pF

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C. $^{\$}$ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

SN100KT5540 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS D3393, DECEMBER 1989

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER	PARAMETER FROM (INPUT)		C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP	MAX	
†PLH	^	Υ	1.6	3.9	6.4	
t _{PHL}	A	Ţ ,	1.6	4.2	6.4	ns
^t PZH			2.4	4.5	6.9	
^t PZL	ŌE1	Y	3.5	5.9	8.7	ns
t _{PHZ}	ŌĒ1	Υ	2.8	5.2	8.1	ns
t _{PLZ}	OL1	'	2.2	4.6	8	115
^t PZH	ŌĒ2	Y	1.4	3.3	6.1	
^t PZL	052	,	2.5	4.7	7.9	ns
tPHZ	<u> </u>	V	1.6	4.1	6.5	
t _{PLZ}	ŌĒ2	Y	0.7	3.3	6.4	ns

† All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN10KHT5541 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3370, OCTOBER 1989-REVISED OCTOBER 1990

10KH Compatible

- ECL and TTL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$, are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5541 is characterized for operation from 0°C to 75°C.

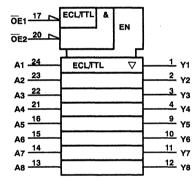
FUNCTION TABLE

	OUTPUT ENABLE				OUTPUT (TTL)
OE1	OE2	Α	Y		
X	Н	X	Z		
н	×	×	Z		
L	L	L	L		
L	L	н	н		

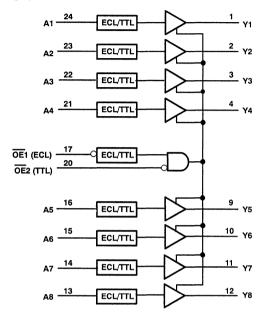
(TOP VIEW) 24 A1 Y2 1 2 23 T A2 Y3 🛮 3 22 A3 21 A4 Y4 🛮 4 Vcc 🛚 5 20 TOE2 (TTL) GND 6 19 VEE GND 7 18 GND GND 1 8 17 OE1 (ECL) Y5 🗖 9 16 A5 Y6 1 10 15 A6 Y7 11 14 A7 13 A8 Y8 12

DW OR NT PACKAGE

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN10KHT5541 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3370, OCTOBER 1989-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	0.5 V to 7 V
Supply voltage, VEE	8 V to 0 V
Input voltage (TTL) (see Note 1)	1.2 V to 7 V
Input voltage (ECL)	V _{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	$-0.5 \overline{V} $ to 5.5 V
Voltage applied to any output in the high state	0.5 V to V _{CC}
Input current (TTL)	30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	V
VIH	TTL high-level input voltage		2			V
VIL	TTL low-level input voltage				0.8	٧
		T _A = 0°C	- 1170		- 840	
V _{IH} ‡	ECL high-level input voltage	T _A = 25°C	- 1130		- 810	mV
		T _A = 75°C	- 1070		- 735	
		T _A = 0°C	- 1950		- 1480	
V _{IL} ‡	ECL low-level input voltage	T _A = 25°C	- 1950		- 1480	mV
		T _A = 75°C	- 1950		- 1450	
ЧK	TTL input clamp current				- 18	mA
ЮН	High-level output current				- 15	mA
lOL	Low-level output current				48	.mA
TA	Operating free-air temperature		0		75	°C

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3370, OCTOBER 1989-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP [†]	MAX	UNIT
VIK	OE2 only	V _{CC} = 4.5 V,	VEE = - 4.94 V,	I _I = 18 mA				- 1.2	٧
IJ	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 7 V				0.1	mA
ΊΗ	OE2 only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 2.7 V				20	μΑ
ΊL	OE2 only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 0.5 V				- 0.5	mA
			V _{EE} = - 5.46 V,		T _A = 0°C			350	
۱н	Data inputs and OE1	$V_{CC} = 5.5 \text{ V},$	V _{EE} = - 5.46 V,	V _I = - 810 mV	T _A = 25°C			350	μΑ
		V _{CC} = 5.5 V,	V _{EE} = 5.46 V,	$V_{ } = -735 \text{mV}$	T _A = 75°C			350	
					T _A = 0°C	0.5			
IIL	Data inputs and OE1	V _{CC} = 5.5 V,	$V_{EE} = -5.46 V_{r}$	$V_{ } = -1950 \text{ mV}$	T _A = 25°C	0.5			μΑ
					T _A = 75°C	0.5			
		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$,	10H = - 3 mA		2.4	3.3		V
VOH		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$,	IOH = 15 mA		2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$	I _{OL} = 48 mA			0.38	0.55	V
lozh		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 2.7 V				50	μΑ
lozL		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 0.5 V				- 50	μΑ
los‡		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	VO = 0		- 100		- 225	mA
ССН		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				64	97	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				80	120	mA
Iccz		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				77	116	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				- 22	- 33	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 5.2 V				5		pF
Co		V _{CC} = 5 V,	V _{EE} = - 5.2 V				7		pF

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R R	UNIT		
			MIN	TYP	MAX	
t _{PLH}	^	Υ	1.7	4	6.2	
t _{PHL}	Α	, · · · · · · · · · · · · · · · · · · ·	1.6	4	6.2	ns
^t PZH	ŌĒ1		2.6	4.7	6.7	
^t PZL	OE1	Y	3.2	5.9	8.5	ns
^t PHZ	ŌĒ1	Y	2.9	5.4	7.8	ns
t _{PLZ}	021	'	1.9	4.9	7.8	113
^t PZH	ŌĒ2	Υ	1.7	4	6.2	ns
t _{PZL}	OLZ	'	2.5	5.1	7.7	113
^t PHZ	ŌĒ2	Y	2.1	4.3	6.4	
t _{PLZ}	UE2	Υ	1.1	3.7	6.3	ns

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, V_{EE} = - 5.2 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C. ‡ Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.

D3384, NOVEMBER 1989-REVISED MAY 1990

- 100K Compatible
- ECL and TTL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment to a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

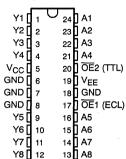
Two output-enable pins, $\overline{OE}1$ and $\overline{OE}2$ are provided. These control inputs are ANDed together with $\overline{OE}1$ being ECL compatible and $\overline{OE}2$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5541 is characterized for operation from 0°C to 85°C.

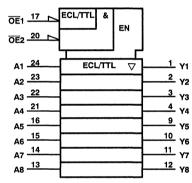
FUNCTION TABLE

OUT	OUTPUT		OUTPUT
ENABLE		ENABLE INPUT	
OE1	OE2	A	Υ
×	Н	Х	Z
Н	X	X	z
L	L	L	L
L	L	н	н

DW OR NT PACKAGE (TOP VIEW)

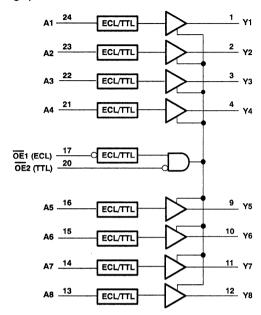


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





SN100KT5541 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS

D3384, NOVEMBER 1989-REVISED MAY 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Supply voltage range, V _{EE}	
Input voltage range (TTL) (see Note 1)	
Input voltage range (ECL)	V _{FF} to 0 V
Voltage applied to any output in the high state	
Voltage applied to any output in the disabled or power-off state	
Input current range (TTL)	30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 85°C
Storage temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	٧
VEE	ECL supply voltage	- 4.2	- 4.5	- 4.8	V
VIH	TTL high-level input voltage	2			٧
VIL	TTL low-level input voltage			0.8	٧
VIH	ECL high-level input voltage [‡]	- 1150		840	mV
VIL	ECL low-level input voltage [‡]	- 1810		- 1490	mV
ΊΚ	TTL input clamp current			- 18	mA
ЮН	High-level output current			- 15	mA
lOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		85	°C

The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

D3384, NOVEMBER 1989-REVISED MAY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	S	MIN	TYP	MAX	UNIT
VIK	OE2 only	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	l _l = – 18 mA			- 1.2	V
i ₁	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 7 V			0.1	mA
ΊΗ	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 2.7 V			20	μА
IIL	OE2 only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
ЧН	Data inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IH} = - 840 mV			350	μА
I _{IL}	Data inputs and OE1	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IL} = - 1810 mV	0.50			μА
		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	IOH = - 3 mA	2.4	3.3		V
Vон		V _{CC} = 4.5 V,	$V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V},$	I _{OH} = - 15 mA	2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$	I _{OL} = 48 mA		0.38	0.55	٧
lozh		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 2.7 V			50	μА
lozL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 0.5 V			- 50	μΑ
los‡		V _{CC} = 5.5 V,	VEE = - 4.8 V,	VO = 0 V	- 100		- 225	mA
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			64	97	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			80	120	mA
Iccz		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			77	116	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			- 22	- 33	mA
Ci		V _{CC} = 5 V,	VEE = 4.5 V			5		pF
Co		V _{CC} = 5 V,	V _{EE} = 4.5 V			7		pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -4.5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER	FROM (INPUT)			C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			
			MIN	TYP	MAX		
^t PLH	A	γ	1.7	4	6.2		
t _{PHL}	7	- 'T	1.6	4	6.2	ns	
^t PZH	OE1	Υ	2.6	4.7	6.7		
^t PZL	7 061	T	3.2	5.9	8.5	ns	
t _{PHZ}	OE 1	Υ	2.9	5.4	7.8	ns	
tPLZ	7	'	1.9	4.9	7.8	113	
^t PZH	OE2	Υ	1.7	4	6.2	ns	
tPZL	7	'	2.5	5.1	7.7	115	
tPHZ	. <u>OE</u> 2	Υ	2.1	4.3	6.4		
tPLZ	OE2	Y	1.1	3.7	6.3	ns	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -4.5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

SN10KHT5542, SN10KHT5543 OCTAL TTL-TO-ECL TRANSLATORS WITH OUTPUT ENABLE

D3136, AUGUST 1988-REVISED DECEMBER 1988

- 10KH Compatible
- ECL and TTL Control Inputs
- P-N-P Inputs Reduce DC Loading
- Flow-Through Architectures Optimizes PCB Lavout
- Center Pin VCC, VEE and GND Configurations Minimize High-Speed Switching Noise
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal TTL-to-ECL translators are designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. The designer has a choice of inverting ('5542) or true ('5543) outputs. Two pins, $\overline{\text{OE}}$ 1 and $\overline{\text{OE}}$ 2, are provided for output enable control. These control inputs are negative ANDed together, with $\overline{\text{OE}}$ 1 being ECL compatible and $\overline{\text{OE}}$ 2 being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment. The outputs, when disabled, go to a normal ECL logic low level.

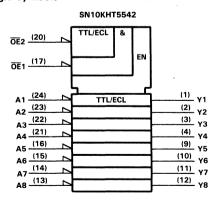
The SN10KHT5542 and SN10KHT5543 are characterized for operation from 0 °C to 75 °C.

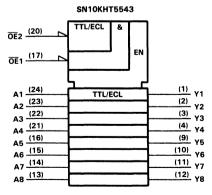
DW OR NT PACKAGE (TOP VIEW) Y1 ∏1 U 24 A1 Y2 🛮 2 23 A2 Y3 ∏3 22 A 3 Y4 114 21 A4 20 OE2 (TTL) GND [5 19 VCC GND [18 \ \rightarrow \rightarrow \text{FE} GND Π_7 17 OE1 (ECL) GND TIB 16∏ A5 Y5 ∏9 15 A6 Y6 ∏10 Y7 ∏11 14 A A 7 13 A8 Y8 🛮 12

FUNCTION TABLE

	PUT TROL	DATA INPUT	OUTPUT		
OE1	OE2	Α	15542 15543		
Н	Х	Х	L	L	
×	Н	х	L	L	
L	L	L	Н	L	
L	L	н	L	н	

logic symbols†





[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the torms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

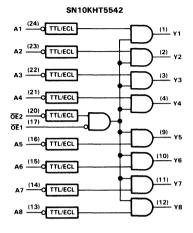


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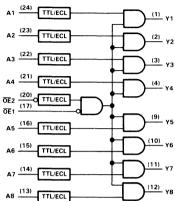
SN10KHT5542, SN10KHT5543 OCTAL TTL-TO-ECL TRANSLATORS WITH OUTPUT ENABLE

D3136, AUGUST 1988-REVISED DECEMBER 1988

logic diagrams (positive logic)



SN10KHT5543



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)

Supply voltage range, VCC
Supply voltage range, VEE
Input voltage range (TTL) (See Note 1)
Input voltage range (ECL)
Input current range (TTL)
Operating ambient temperature range
Storage temperature range

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM MAX	UNIT
V _{CC} TTL supply voltage			4.5	5.0 5.5	V
VEE ECL supply voltage			-4.94	-5.2 -5.46	٧
VIH TTL high-level input voltage			2		V
		0°C	- 1170	- 840	
VIH	ECL high-level input voltage [‡]	25°C	-1130	-810	mV V
	· · · · · · · · · · · · · · · · · · ·	75°C	- 1070	- 735	
VIL	TTL low-level input voltage			0.8	V
		0°C	- 1950	- 1480	
V_{IL}	ECL low-level input voltage [‡]	25°C	- 1950	- 1480	mV
	75°C		- 1950	~ 1450	
ΊΚ	TTL input clamp current			18	mA
TA Operating ambient temperature (see Note 3)			0	75	°C

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only. IOTES: 2. If unused, $\overline{OE}1$ should be tied directly to -2 V.

^{3:} Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse air flow greater than 500 linear ft/min is maintained.



NOTES:

SN10KHT5542 OCTAL TTL-TO-ECL TRANSLATOR WITH OUTPUT ENABLE

D3136, AUGUST 1988-REVISED DECEMBER 1988

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

	PARAMETER	TEST CONDITIONS		MIN	TYP [†] MAX	UNIT
VIK	A inputs and OE2	V _{CC} = 4.5 V, V _{EE} = -4.94 V, I _I = -18 mA			-1.2	٧
lį	A inputs and OE2	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = 7 \text{ V}$			0.1	mA
	A inputs and OE2	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = 2.7 \text{ V}$			20	
ļ.,,		$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = -840 \text{ mV}$	0°C		350	ایرا
ነነዘ	OE1 only	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = -810 \text{ mV}$	25°C		350	μΑ
		$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = -735 \text{ mV}$	75°C		350	
	A inputs and OE2	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = 0.5 \text{ V}$			- 500	
1			0°C	0.5		μΑ
11L	OE1 only	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = -1950 \text{ mV}$	25°C	°C 0.5]
			75°C	0.5		
			0°C	- 1020	- 840	
V _{OH} ‡		V _{CC} = 4.5 V, V _{EE} = -5.2 V, ±5%, See Note 3	25°C	-980	-810	mV
1			75°C	-920	- 735	
			0°C	- 1950	- 1630	
V _{OL} ‡		V _{CC} = 4.5 V, V _{EE} = -5.2 V, ±5%, See Note 3	= -5.2 V, ±5%, See Note 3 25°C -195	- 1950	- 1630	mV
			75°C	- 1950	- 1600	
Іссн		V _{CC} = 5.5 V, V _{EE} = -5.46 V			15 22	mA
ICCL		$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}$			17 25	mA
IEE		V _{CC} = 5.5 V, V _{EE} = -5.46 V			-78 -111	mA
Ci		$V_{CC} = 5 \text{ V}, V_{EE} = -5.2 \text{ V}, f = 10 \text{ MHz}$			5	pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
^t PLH	A=:: A	V	0.1	1.7	3.7	
^t PHL	Any A	T	0.1	1.6	3.3	ns
t _{PLH}	OE1 (ECL)	V	0.8	2.8	5	
tPHL] OET (ECL)	*	0.4	2.3	4.5	ns
t _{PLH}	OE2 (TTL)	V	0.8	3	5.3	
^t PHL	OEZ (TTL)	, , , , , , , , , , , , , , , , , , ,	0.6	2.5	4.7	ns∞
t _r		V		1.5		
t _f]	Y		1.5		ns

- 3. Outputs are terminated through a $50-\Omega$ resistor to -2 V.
- 4. Load circuit and switching waveforms are shown in Section 1.

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

SN10KHT5543 OCTAL TTL-TO-ECL TRANSLATOR WITH OUTPUT ENABLE

D3136, AUGUST 1988-REVISED DECEMBER 1988

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

	PARAMETER		TEST CONDITIONS		MIN	TYP† MAX	UNIT
VIK	A inputs and OE2	$V_{CC} = 4.5 V,$	$V_{EE} = -4.94 \text{ V}, I_{I} = -18 \text{ mA}$			- 1.2	V
l ₁	A inputs and OE2	$V_{CC} = 5.5 V$,	$V_{EE} = -5.46 \text{ V}, V_{I} = 7 \text{ V}$			0.1	mA
	A inputs and OE2	$V_{CC} = 5.5 V$,	$V_{EE} = -5.46 \text{ V}, V_{I} = 2.7 \text{ V}$			20	
l		$V_{CC} = 5.5 V,$	$V_{EE} = -5.46 \text{ V}, V_{I} = -840 \text{ mV}$	0°C		350	ا ما
lін	OE1 only	$V_{CC} = 5.5 V,$	$V_{EE} = -5.46 \text{ V}, V_{I} = -810 \text{ mV}$	25°C		350	μΑ
		$V_{CC} = 5.5 V$,	$V_{EE} = -5.46 \text{ V}, V_{I} = -735 \text{ mV}$	75°C		350	
	A inputs and OE2	$V_{CC} = 5.5 V,$	$V_{EE} = -5.46 \text{ V}, V_{I} = 0.5 \text{ V}$			- 500	
1				0°C	0.5		
ΊL	OE1 only	$V_{CC} = 5.5 V,$	$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}, V_{I} = -1950 \text{ mV}$	25°C 0.5		μΑ	
	İ			75°C	0.5		1
				0°C	- 1020	- 840	
VoH [‡]		""	$V_{EE} = -5.2 \text{ V}, \pm 5\%, \text{ See Note 3}$	25°C	- 980	-810	mV
1			75°C	-920	– 735		
				0°C	- 1950	- 1630	
V _{OL} ‡		$V_{CC} = 4.5 V$,	$V_{EE} = -5.2 \text{ V}, \pm 5\%, \text{ See Note 3}$	25°C	- 1950	- 1630	m∨
				75°C	- 1950	- 1600	
Іссн		$V_{CC} = 5.5 V,$	$V_{EE} = -5.46 \text{ V}$			17 25	mA
ICCL		$V_{CC} = 5.5 \text{ V}, V_{EE} = -5.46 \text{ V}$			15 22	mA	
IEE		$V_{CC} = 5.5 V,$	V _{EE} = -5.46 V			-77 -111	mA
Ci		V _{CC} = 5 V,	$V_{EE} = -5.2 \text{ V}, f = 10 \text{ MHz}$			5	pF

switching characteristics over recommended ranges of operating ambient temperature and supply voltage (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP [†]	MAX	UNIT
tPLH	Any A	V	0.1	1.5	3	
tPHL	Ally A		0.1	1.5	3.3	ns
t _{PLH}	OE1 (ECL)	V	0.6	2.2	4.3	
tPHL		r	0.5	2.4	4.3	ns
^t PLH	OE2 (TTL)	v	0.7	2.2	4.4	
tPHL	OEZ (TIL)	ļ , ,	0.5	2.6	4.7	ns
t _r		V		1.5		
t _f		, ·		1.5		ns

- 3. Outputs are terminated through a $50-\Omega$ resistor to -2 V.
- 4. Load circuit and voltage waveforms are shown in Section 1.



[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels and temperature only.

NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

SN10KHT5562, SN100KT5562 OCTAL TTL/ECL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3538, JUNE 1990

- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

The SN10KHT5562 and SN100KT5562 are noninverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50- Ω load terminated to -2 V.

The A and B ports have complementary outputenable inputs, both of which are ECL-compatible. When the A-port output enable (GBA) is high, the device transmits data from the B bus to the A bus. When GBA is low, the A outputs are in the high-impedance state. When $\overline{G}AB$ is low, the device transmits data from the A bus to the B bus; when $\overline{G}AB$ is high, the B outputs are in the high-impedance state.

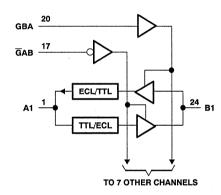
When GAB is low and $\overline{G}BA$ is high, the device is in the isolation mode.

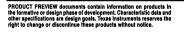
The SN10KHT5562 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5562 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE (TOP VIEW)

			_		
A1[1	U	24	b	B1
A2[2		23	1	B2
A3[3		22	1	B3
A4[4		21	1	B4
Vcc[5		20	þ	GBA
GND[6		19	þ	V_{EE}
GND[7		18	1	GND
GND[8		17	þ	GAB
A5[9		16	ם	B5
A6[10		15	1	B6
A7[11		14	b	B7
A8[12		13	1	B8
1	L				







SN10KHT5563, SN100KT5563 OCTAL TTL/ECL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3539, JUNE 1990

- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil

description

The SN10KHT5563 and SN100KT5563 are inverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50- Ω load terminated to -2 V.

The A and B ports have complementary outputenable inputs, both of which are ECL-compatible. When the A-port output enable (GBA) is high, the device transmits data from the B bus to the A bus; when GBA is low, the A outputs are in the high-impedance state. When $\overline{G}AB$ is low, the device transmits data from the A bus to the B bus; when $\overline{G}AB$ is high, the B outputs are in the high-impedance state.

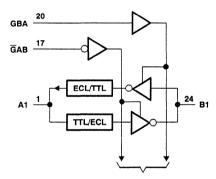
When GAB is low and $\overline{G}BA$ is high, the device is in the isolation mode.

The SN10KHT5563 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5563 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE (TOP VIEW)

		,		1
A1[1	U	24] B1
A2[2		23] B2
A3[3		22] B3
A4[4		21] B4
Vcc[5		20] GBA
GND[6		19] V _{EE}
GND[7		18] GND
GND[8		17] GAB
A5[9		16] B5
A6[10		15] B6
A7[11		14] B7
]8A	12		13] B8



TO 7 OTHER CHANNELS

DW OR NT PACKAGE

- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Lavout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil **DIPs**

description

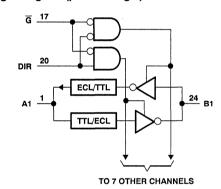
The SN10KHT5564 and SN100KT5564 are inverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50-Ω load terminated to -2 V.

When the output-enable input \overline{G} is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. When G is high. both buses are in the high-impedance state. Both G and DIR are ECL-compatible.

The SN10KHT5564 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5564 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

	(TOP VIEW)				
A1[A2] A3] A4[Vcc[GND[GND] A5[A6] A7]	1 2 3 4 5 6 7 8 9 10 11	24 B1 B2 B2 B3 B4 B4 B B B B B B B B B B B B B B B			
A8[12	13 B8			



- ECL and TTL Output-Enable Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

The SN10KHT5565 and SN100KT5565 are noninverting TTL/ECL transceivers designed to translate signals between ECL and TTL environments. The A port (TTL port) is designed to source 15 mA and sink 48 mA. The B port (ECL port) is designed to drive a 50- Ω load terminated to -2 V.

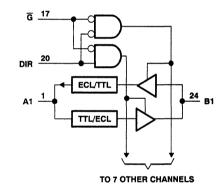
When the output-enable input \overline{G} is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. When \overline{G} is high, both buses are in the high-impedance state. Both \overline{G} and DIR are ECL-compatible.

The SN10KHT5565 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C.

The SN100KT5565 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

DW OR NT PACKAGE (TOP VIEW)

A1[1	J 24] B1
A2[2	23] B2
A3[3	22] B3
A4[4	21] B4
V _{CC} [5	20	DIR
GND[6	19] VEE
GND[7	18	GND
GND[8	17	j G
A5[]	9	16] B5
A6[]	10	15] B6
A7[11	14] B7
A8[12	13] B8



SN10KHT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

D3509, MAY 1990-REVISED OCTOBER 1990

10KH Compatible	DW OR NT PACKAGE (TOP VIEW)		
ECL and TTL Control Inputs	101 1 0 24 1 1D		
Noninverting Outputs	2Q[2 23] 2D		
 Flow-Through Architecture Optimizes PCB Layout 	3Q[] 3 22] 3D 4Q[] 4 21] 4D V _{CC} [] 5 20] ŌĒ (TTL)		
 Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise 	GND 6 19 VEE GND 7 18 GND GND 8 17 EE (ECL)		
 Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs 	5Q[] 9 16] 5D 6Q[] 10 15] 6D 7Q[] 11 14] 7D 8Q[] 12 13] 8D		

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight latches of the SN10KHT5573 are transparent D-type latches. While latch enable $(\overline{\text{LE}})$ is low, the Q outputs follow the data (D) inputs. When $\overline{\text{LE}}$ is high, the Q outputs are latched at the levels that were set up at the D inputs.

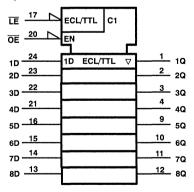
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components. Output-enable \overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5573 is characterized for operation from 0° to 75°C.

FUNCTION TABLE

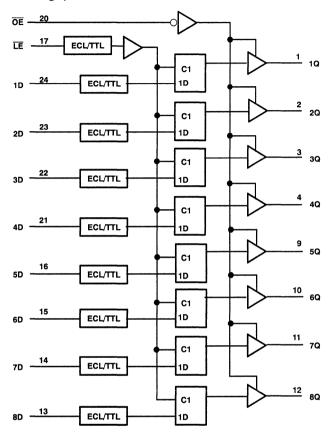
		OUTPUT CONTROL		OUTPUT (TTL)
	ŌĒ	ΙĒ	D	Q
	L	L	L.	L
	L	L	Н	н
	L	Н	×	Q_0
I	н	x	l x	z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.





SN10KHT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

D3509, MAY 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Supply voltage range, VEE	– 8 V to 0 V
Input voltage range, TTL (see Note 1)	– 1.2 V to 7 V
Input voltage range, ECL	V _{EE} to 0 V
Input current range, TTL	– 30 mA to 5 mA
Current into any output in the low state	96 mA
Voltage applied to any output in the disabled or power-off state	
Voltage applied to any output in the high state	– 0.5 V to V _{CC}
Operating free-air temperature range	0°C to 75°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	٧
VEE	ECL supply voltage		4.94	- 5.2	- 5.46	V
VIH	TTL high-level input voltage		2			V
VIL	TTL low-level input voltage				8.0	V
ΊΚ	TTL input clamp current				- 18	mA
		0°C	- 1170		- 840	
VIH	ECL high-level input voltage (see Note 2)	25°C	- 1130		- 810	mV
		75°C	- 1070		- 735	
		0°C	- 1950		- 1480	
VIL	ECL low-level input voltage (see Note 2)	25°C	- 1950		- 1480	mV
	75°C		- 1950		- 1450	
ЮН	High-level output current				- 15	mA
IOL	Low-level output current				48	mA
TA	Operating free-air temperature		0		75	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

SN10KHT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS D3509, MAY 1990-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
VIK	OE only	V _{CC} = 4.5 V,	V _{EE} = 4.94 V,	lj = – 18 mA				- 1.2	٧
lj.	OE only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 7 V				0.1	mA
ΊΗ	OE only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 2.7 V				20	μΑ
IL	OE only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 0.5 V				- 0.5	mA
		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = - 840 V	0°C			350	
Ιн	Data inputs and LE	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = - 810 V	25°C			350	μΑ
		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = – 735 V	75°C			350	
					0°C	0.5			
l _{IL}	Data inputs and LE	V _{CC} = 5.5 V,	$V_{EE} = -5.46 V$,	$V_{\parallel} = -1950 \text{ V}$	25°C	0.5			μА
					75°C	0.5			
		V _{CC} = 4.5 V,	$I_{OH} = -3 \text{ mA},$	V _{EE} = - 5.2 V ± 5%		2.4	3.3		
VOH		V _{CC} = 4.5 V,	IOH = - 15 mA,	VEE = - 5.2 V ± 5%		2	3.1		٧
VOL		V _{CC} = 4.5 V,	I _{OL} = 48 mA,	VEE = - 5.2 V ± 5%			0.38	0.55	V
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V,	V _{EE} = - 5.46 V				50	μА
^I OZL		V _{CC} = 5.5 V,	V _O = 0.5 V,	V _{EE} = - 5.46 V				- 50	μΑ
los‡		V _{CC} = 5.5 V,	V _O = 0 V,	V _{EE} = - 5.46 V		- 100		- 225	mA
ССН		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				62	89	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				78	111	mA
Iccz		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				75	108	mA
IEE		V _{CC} = 5.5 V,	VEE = 5.46 V				- 34	48	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 5.2 V				5		pF
Co		V _{CC} = 5 V,	V _{EE} = 5.2 V				7		pF

timing requirements

		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $V_{EE} = -4.94 \text{ V to } -5.46 \text{ V},$ $T_A = \text{MIN to MAX}^{\S}$	UNIT
		MIN MAX	
t _W	Pulse duration, LE high	4	ns
t _{su}	Setup time, data before LE↓	1	ns
th	Hold time, data after LE↓	1	ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[†] All typical values are at V_{CC} = 5 V, V_{EE} = - 5.2 V, and T_A = 25°C. ‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

SN10KHT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS D3509, MAY 1990-REVISED OCTOBER 1990

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX		R1 = 500 Ω , R2 = 500 Ω , T _A = MIN to		MAX	UNIT
			MIN	TYP	MAX			
^t PLH	D		1.9	3.9	6.4			
t _{PHL}		Q	2.3	4.2	6.8	ns		
^t PLH	Œ	Q	2.2	4	6.7	200		
tPHL	LE	ď	2.6	4.5	7.2	ns		
^t PZH	ŌĒ		1.1	3.2	5.9			
t _{PZL}	OE	Q	2.3	4.6	7.8	ns		
t _{PHZ}	ŌĒ	Q	1.8	4	5.9	ns		
t _{PLZ}	, JE .	4	0.6	3.4	6.5	115		

[†] All typical values are at V_{CC} = 5 V, V_{EE} = - 5.2 V, and T_A = 25°C. NOTE 3: Load circuit and voltage waveforms are shown in Section 1.7



SN100KT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

D3510, MAY 1990-REVISED OCTOBER 1990

13 BD

•	100K Compatible	DW OR NT PACKAGE (TOP VIEW)		
•	ECL and TTL Control Inputs	10/1	24 1D	
•	Noninverting Outputs	20 2	23 2D	
•	Flow-Through Architecture Optimizes PCB Layout	3Q[] 3 4Q[] 4 V _{CC} [] 5	22 3D 21 4D 20 0E (TTL)	
•	Center-Pin V _{CC} , V _{EE} , and GND Configurations Minimize High-Speed Switching Noise	GND [6 GND [7 GND [8	19 V _{EE} 18 GND 17 LE (ECL)	
•	Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs	5Q[] 9 6Q[] 10 7Q[] 11 8Q[] 12	16 5D 15 6D 14 7D 13 8D	

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The eight latches of the SN100KT5573 are transparent D-type latches. While latch enable (\overline{LE}) is low, the Q outputs follow the data (D) inputs. When LE is high, the Q outputs are latched at the levels that were set up at the D inputs.

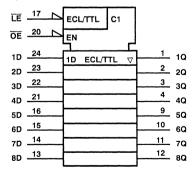
A buffered output-enable input (\overline{OE}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. Output-enable \overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5573 is characterized for operation from 0° to 85° C.

FUNCTION TABLE

	OUTPUT ENABLE		OUTPUT (TTL)
ŌĒ	ĹĒ	D	Q
L	L	L	L
L	L	н	н
L	Н	×	QO
Н	Х	X	Z

logic symbol[†]

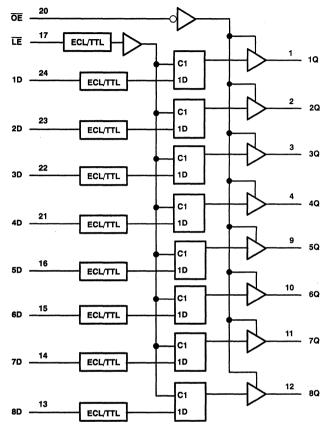


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Supply voltage range, VEE	– 8 V to 0 V
Input voltage range, TTL (see Note 1)	– 1.2 V to 7 V
Input voltage range, ECL	V _{EE} to 0 V
Input current range, TTL	30 mA to 5 mA
Current into any output in the low state	96 mA
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage applied to any output in the high state	\dots - 0.5 V to V _{CC}
Operating free-air temperature range	0°C to 85°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied, Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



PRODUCT PREVIEW

OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS D3510, MAY 1990-REVISED OCTOBER 1990

recommended operating conditions

		MIN	МОМ	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	٧
VEE	ECL supply voltage	- 4.2	- 4.5	- 4.8	V
VIH	TTL high-level input voltage	2			٧
VIL	TTL low-level input voltage			0.8	V
lк	TTL input clamp current			- 18	mA
VIH	ECL high-level input voltage [†]	- 1150		- 840	٧
VIL	ECL low-level input voltage [†]	- 1810		- 1490	V
¹он	High-level output current			- 15	mA
lOL	Low-level output current			48	mA
TA	Operating temperature	0		85	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
VIK	OE only	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	l _l = – 18 mA			- 1.2	٧
11	OE only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 7 V			0.1	mA
ΊΗ	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 2.7 V			20	μА
4L	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
ΊΗ	Data inputs and LE	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IH} = 840 mV			350	μА
IIL	Data inputs and LE	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IL} = - 1810 mV	0.50			μΑ
		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$	10H = - 3 mA	2.4	3.3		
∨он		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	I _{OH} = 15 mA	2	3.1		٧
VOL		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	I _{OL} = 48 mA		0.38	0.55	٧
lozh		V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _O = 2.7 V			50	μΑ
lozL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 0.5 V			- 50	μΑ
los§		V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _O = 0 V	- 100		- 225	mA
Іссн		V _{CC} = 5.5 V,	VEE = - 4.8 V			62	89	mA
ICCL		V _{CC} = 5.5 V,	VEE = - 4.8 V			77	111	mA
Iccz		V _{CC} = 5.5 V,	VEE = - 4.8 V			75	108	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			- 34	- 48	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 4.5 V			5		pF
Co		V _{CC} = 5 V,	V _{EE} = - 4.5 V			7		pF



[‡] All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, and T_A = 25°C. § Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

SN100KT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

D3510, MAY 1990-REVISED OCTOBER 1990

timing requirements

		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $V_{EE} = -4.2 \text{ V to } -4.8 \text{ V},$ $T_A = \text{MIN to MAX}^{\dagger}$	UNIT
		MIN MAX	1
tw	Pulse duration, LE high	4	ns
t _{su}	Setup time, data before LE↓	1	ns
th	Hold time, data after LE↓	1	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

			CL	= 50 pF,			
*			R1	= 500 Ω,			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	R2	R2 = 500 Ω,			
	(1147-01)	(0011-01)	TA	= MIN to	MAX		
		*	MIN	TYP‡	MAX	į l	
t _{PLH}			1.9	3.9	6.4		
t _{PHL}	D	Q	2.3	4.2	6.8	ns	
tPLH t	Œ	Q ·	2.2	4	6.7		
tPHL 1	LE	Δ	2.6	4.5	7.2	ns	
^t PZH	ŌĒ	Q	1.1	3.2	5.9		
t _{PZL}	OE .	ŭ	2.3	4.6	7.8	ns	
tPHZ	ŌĒ	Q	1.8	4	5.9	ns	
tPLZ	OE.	3	0.6	3.4	6.5	113	

 $[\]ddagger$ All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, and T_A = 25°C. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



SN10KHT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

D3417, JANUARY 1990-REVISED OCTOBER 1990

٠	10KH Compatible	DW OR NT PACKAGE (TOP VIEW)		
٠	ECL Clock and TTL Control Inputs	401	104-77-112	
•	Flow-Through Architecture Optimizes PCB Layout	1Q[] 1 2Q[] 2 3Q[] 3	24] 1D 23] 2D 22] 3D	
•	Center Pin V _{CC} , V _{EE} , and GND Configurations Minimize High-Speed Switching Noise	4Q[] 4 V _{CC} [] 5 GND[] 6 GND[] 7	21 4D 20 OE(TTL) 19 V _{EE} 18 GND	
•	Package Options Include "Small Outline" Packages and Standard Plastic DIPs	GND	17 CLK(ECL) 16 5D	
description		6Q[] 10 7Q[] 11 8Q[] 12	15 6D 14 7D 13 8D	

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment.

This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN10KHT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input (OE) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input \overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5574 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

1 OHOHOH IABLE							
11	NPUTS	OUTPUT (TTL)					
ŌĒ	CLK	D	Q				
L	1	L	L				
L	1	Н	Н				
L	L	Х	Qo				
н	X	х	z				



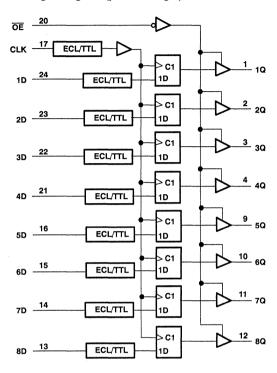
D3417, JANUARY 1990-REVISED OCTOBER 1990

logic symbol†

CLK 17 ECL/TTL >C1 ŌĒ ΕN 1 1Q 24 1D ECL/TTL 1D ∇ 2_ 2Q 23 2D 22 3 3Q 3D 4 21 40 4D 9___ 5Q 16 5D 10___ 6Q 15 6D 14 11 7Q 7D 13 12__ 8Q 8D

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN10KHT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

D3417, JANUARY 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Supply voltage range, V _{EE}	– 8 V to 0 V
Input voltage range: TTL (see Note 1)	– 1.2 V to 7 V
ECL	V _{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage applied to any output in the high state	$\dots \dots -0.5 \text{ V to V}_{CC}$
Input current range, (TTL)	– 30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	V
ViH	TTL high-level input voltage		2			٧
VIL	TTL low-level input voltage				0.8	V
ViH	ECL high-level input voltage [‡]	T _A = 0°C	- 1170		- 840	
		T _A = 25°C	- 1130		- 810	mV
		T _A = 75°C	- 1070		- 735	
		T _A = 0°C	- 1950		- 1480	
VIL	ECL low-level input voltage [‡]	T _A = 25°C	- 1950		- 1480	mV
	T _A = 75°C		- 1950		- 1450	
lik	TTL input clamp current				- 18	mA
ПОН	High-level output current				- 15	mA
lOL	Low-level output current				48	mA
TA	Operating free-air temperature range		0		75	°C

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

SN10KHT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

D3417, JANUARY 1990-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	3		MIN	TYP†	MAX	UNIT
٧ıĸ	OE only	V _{CC} = 4.5 V,	VEE = - 4.94 V,	l _l = 18 mA				- 1.2	٧
Voн		V _{CC} = 4.5 V,	$V_{EE} = -5.2 \text{ V} \pm 5\%$, $I_{OH} = -3 \text{ mA}$			2.4	3.3		
VOH		V _{CC} = 4.5 V,	$V_{EE} = -5.2 \text{ V} \pm 5\%$,	I _{OH} = - 15 mA		2	3.1		V
VOL		V _{CC} = 4.5 V,	VEE = - 5.2 V ±5%,	I _{OL} = 48 mA			0.38	0.55	٧
II	OE only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 7 V				0.1	mA
ΊΗ	OE only	V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = 2.7 V	*			20	μΑ
IIL	OE only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 0.5 V				- 0.5	mA
		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = – 840 mV	T _A = 0°C			350	
ЧH	Data inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 810 mV	T _A = 25°C			350	μΑ
		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _I = - 735 mV	T _A = 75°C			350	
					T _A = 0°C	0.5			
11L	Data inputs and CLK	V _{CC} = 5.5 V,	$V_{EE} = -5.46 V_{r}$	$V_{i} = -1950 \text{mV}$	T _A = 25°C	0.5			μΑ
	,				T _A = 75°C	0.5			
lozh		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 2.7 V				50	μΑ
IOZL		V _{CC} = 5.5 V,	VEE = - 5.46 V,	V _O = 0.5 V				- 50	μΑ
los‡		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _O = 0 V		- 100		- 225	mA
ІССН		V _{CC} = 5.5 V,	VEE = - 5.46 V				66	95	mA
CCL		V _{CC} = 5.5 V,	VEE = - 5.46 V				76	110	mA
Iccz		V _{CC} = 5.5 V,	VEE = - 5.46 V				74	106	mA
!EE		V _{CC} = 5.5 V,	VEE = - 5.46 V				- 43	- 61	mA
Ci		V _{CC} = 5.5 V,	V _{EE} = - 5.2 V,	f = 10 MHz			5		pF
Co		V _{CC} = 5.5 V,	V _{EE} = - 5.2 V,	f = 10 MHz			7		pF

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

timing requirements

			V _{CC} = 4.5 V to 5.5 V, V _{EE} = -4.94 V to -5.46 V, T _A = MIN to MAX [§]	UNIT	
			MIN MAX	1	
	B. I	CLK high	4		
tw	Pulse duration	Pulse duration	Pulse duration CLK low	4	ns
		Data high	1		
t _{su}	Setup time before CLK↑	Data low	1	ns	
tı.	Hold time after CLK↑	Data high	1		
th		Hold time after CLKT	Hold time after CERT	Data low	1

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{*} Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS D3417, JANUARY 1990-REVISED OCTOBER 1990

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω		2,	UNIT
		1	MIN	TYP	MAX	
fmax			200	300		MHz
tPLH			2.3	4.1	7	
t _{PHL}	CLK	Q	2.9	4.6	7.4	ns
tPZH			1.9	3.6	6.3	
tPZL	ŌĒ	Q	2.7	4.8	7.7	ns
tpHZ			2.1	3.9	6.1	
tPLZ	ŌĒ	Q	0.5	3.4	6.3	ns

† All typical values are at V_{CC} = 5 V, V_{EE} = - 5.2 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN100KT5574 **OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS**

D3418, JANUARY 1990-REVISED OCTOBER 1990

•	100K Compatible	DW OR NT PACKAGE (TOP VIEW)	
•	ECL Clock and TTL Control Inputs		
•	Flow-Through Architecture Optimizes PCB Layout	1Q[] 1	
•	Center Pin V _{CC} , V _{EE} , and GND Configurations Minimize High-Speed Switching Noise	4Q	
•	Package Options Include "Small Outline" Packages and Standard Plastic DIPs	GND[8 17] CLK(5Q[9 16] 5D 6Q[10 15] 6D	
desc	ription	70 11 14 7D	

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment.

This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN100KT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input (OE) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input \overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

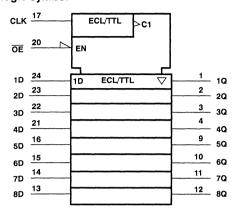
The SN100KT5574 is characterized for operation from 0°C to 85°C.

	FUNCT	ION	TABLE	
II	NPŲTS		OUTPUT (TTL)	
ŌĒ	CLK	D	Q	
L	1	L	L	_
L	1	Н	Н	
L	L	х	Qo	
н	х	х	z	

SN100KT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

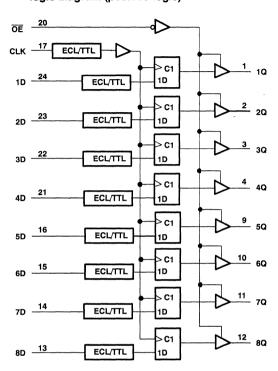
D3418, JANUARY 1990-REVISED OCTOBER 1990

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN100KT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS D3418, JANUARY 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Supply voltage range, V _{FF}	– 8 V to 0 V
Input voltage range: TTL (see Note 1)	– 1.2 V to 7 V
ECL	V _{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	– 0.5 V to 5.5 V
Voltage applied to any output in the high state	– 0.5 V to V _{CC}
Input current range, TTL	– 30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 85°C
Storage temperature range	- 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	٧
VEE	ECL supply voltage	- 4.2	- 4.5	- 4.8	V
VIH .	TTL high-level input voltage	2			٧
VIL	TTL low-level input voltage			0.8	٧
lik	TTL input clamp current			- 18	mA
VIH	ECL high-level input voltage [‡]	- 1150		- 840	mV
VIL	ECL low-level input voltage [‡]	- 1810		- 1490	mV
ЮН	High-level output current			- 15	mA
loL	Low-level output current			48	mA
TA	Operating temperature range	0		85	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS D3418, JANUARY 1990-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
VIK	OE only	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	lj = - 18 mA			- 1.2	٧
VOH		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	IOH = - 3 mA	2.4	3.3		
VOH		$V_{CC} = 4.5 V$,	$V_{EE} = -4.5 V \pm 0.3 V$,	IOH = - 15 mA	2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	I _{OL} = 48 mA		0.38	0.55	٧
II	OE only	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _I = 7 V			0.1	mA
ΊΗ	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _j = 2.7 V			20	μА
IIL	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
ΊΗ	Data inputs and CLK	V _{CC} = 5.5 V,	VEE = - 4.8 V,	V _{IH} = - 840 mV			350	μΑ
IIL	Data inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IL} = 1810 mV	0.50			μА
IOZH		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _O = 2.7 V			50	μΑ
IOZL		$V_{CC} = 5.5 V$,	VEE = - 4.8 V,	V _O = 0.5 V			- 50	μΑ
los‡		V _{CC} = 5.5 V,	VEE = - 4.8 V,	VO = 0 V	- 100		- 225	mA
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			66	95	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			76	110	mA
ICCZ		V _{CC} = 5.5 V,	VEE = - 4.8 V			74	106	mA
IEE		V _{CC} = 5.5 V,	VEE = - 4.8 V			- 43	- 61	mA
Ci		V _{CC} = 5.5 V,	VEE = - 4.5 V			5		pF
Co		V _{CC} = 5.5 V,	V _{EE} = - 4.5 V			7		рF

timing requirements

			V _{CC} = 4.5 V to 5.5 V, V _{EE} = -4.2 V to -4.8 V, T _A = MIN to MAX [§]	UNIT	
			MIN MAX	7	
		CLK high	4		
tw	Pulse duration	CLK low	4	ns	
		Data high	1		
th	Hold time after CLK†	Data low	1	ns	
	Setup time before CLK↑	Data high	1		
t _{su}	Setup time before CLK	Setup time before CLK	Data low	1	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C. ‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

SN100KT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

D3418, JANUARY 1990-REVISED OCTOBER 1990

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R-	L = 50 pl 1 = 500 s 2 = 500 s	2,	UNIT
,			MIN	TYP†	MAX	
f _{max}			200	300		MHz
t _{PLH}	CLK	0	2.3	4.1	7	
t _{PHL}	CLK	Q	2.9	4.6	7.4	ns
^t PZH	ŌĒ		1.9	3.6	6.3	
tPZL	OE	Q	2.7	4.8	7.7	ns
tPHZ	ŌĒ	Q	2.1	3.9	6.1	
t _{PLZ}	OE .	Q	0.5	3.4	6.3	ns

[†] All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



SN10KHT5575, SN100KT5575 OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

8Q 12

D3602, JULY 1990

ECL and TTL Control Inputs	DW OR NT PACKAGE (TOP VIEW)
Inverting Outputs	
 Flow-Through Architecture Optimizes PCB Layout 	$2\overline{Q}$ $\begin{bmatrix} 1 \\ 2 \end{bmatrix}$ $\begin{bmatrix} 23 \\ 3 \end{bmatrix}$ $\begin{bmatrix} 2D \\ 3\overline{Q} \end{bmatrix}$ $\begin{bmatrix} 3 \\ 4\overline{Q} \end{bmatrix}$ $\begin{bmatrix} 4 \\ 21 \end{bmatrix}$ $\begin{bmatrix} 4D \\ 4D \end{bmatrix}$
 Center-Pin V_{CC}, V_{EE}, and GND Configuration Minimizes High-Speed Switching Noise 	4Q [] 4 21 [] 4D V _{CC} [] 5 20 [] OE (TTL) GND [] 6 19 [] V _{EE} GND [] 7 18 [] GND
 Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs 	GND

description

The SN10KHT5575 and SN100KT5575 are octal ECL-to-TTL inverting translators designed to provide efficient translation between 10KH or 100KECL signal environments, respectively, and a TTL signal environment. These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight latches of the '5575 are transparent D-type latches. When latch enable (LE) is high, the \overline{Q} outputs follow the complements of the data (D) inputs. When LE is taken low, the \overline{Q} outputs are latched at the inverse of the levels that were set up at the D inputs.

A buffered output-enable input $\overline{(OE)}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The \overline{OE} input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN10KHT5575 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5575 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

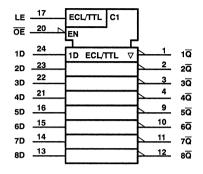
II	NPUTS	OUTPUT (TTL)	
ŌĒ	LE	D	Q
L	L	L	Н
L	L	Н	L
L	Н	Х	₫0
Н	Х	Х	z



SN10KHT5575, SN100KT5575 OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

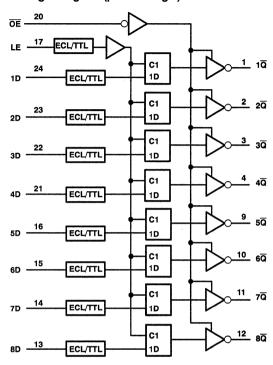
D3602, JULY 1990

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN10KHT5576, SN100KT5576 OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

13 N 8D

D3603, JULY 1990

ECL and TTL Control Inputs	DW OR NT PACKAGE (TOP VIEW)
 Flow-Through Architecture Optimizes PCB Layout 	1Q 1 1D
 Center-Pin V_{CC}, V_{EE}, and GND Configuration Minimizes High-Speed Switching Noise 	2Q [] 2 23] 2D 3Q [] 3 22] 3D 4Q [] 4 21] 4D V _{CC} [] 5 20 [] ŌE(TTL)
 Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs 	GND [] 6 19] V _{EE} GND [] 7 18] GND GND [] 8 17] CLK(ECL) 5 \overline{Q} [] 9 16 [] 5 D
description	6Q 10 15 6D

The SN10KHT5576 and SN100KT5576 are octal ECL-to-TTL inverting translators designed to provide efficient translation between an ECL signal environment and a TTL signal environment.

These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, receivers, and transmitters.

The eight flip-flops of the '5576 are edge-triggered D-type flip-flops. On the positive transition of the clock, the \overline{Q} outputs take on the complement of the logic levels that were set up at the D inputs. A buffered output-enable input (\overline{OE}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive give the device the capability to drive bus lines without need for interface or pullup components. The \overline{OE} input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN10KHT5576 is compatible with 10KH ECL and is characterized for operation from 0°C to 75°C. The SN100KT5576 is compatible with 100K ECL and is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

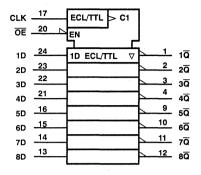
	INPUTS	OUTPUT (TTL)	
ŌĒ	CLK	D	ā
L	t	L	н
L	1	Н	L
L	L	Χ	\overline{a}_0
н	X	X	Z



SN10KHT5576, SN100KT5576 OCTAL ECL-TO-TTL TRANSLATORS WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

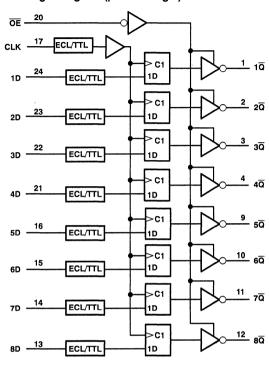
D3603, JULY 1990

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



D3484, APRIL 1990

- 10KH Compatible
- TTL Clock and ECL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic DIPs
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015

description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 10KH ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

The output-control input $\overline{\text{OE}}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5578 is characterized for operation from 0°C to 75°C.

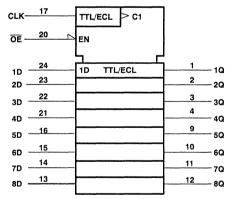
DW OR NT PACKAGE

1Q[1	(TOP VIEW)						
	2Q [3Q [4Q [GND [GND [GND [5Q [1 2 3 4 5 6 7 8	24 23 22 21 20 19 18 17] 2D] 3D] 4D] OE (ECL)] V _{CC}] V _{EE}] CLK(TTL)] 5D			
	_			<u> </u>			
6Q	GND[7	18	V _{EE}			
8Q[] 12 13[] 8D	6Q[7Q[10	15	6D			
	8Q[12	13] 8D			

FUNCTION TABLE

11	IPUTS	OUTPUT (ECL)	
ŌĒ	CLK	D	a
L	1	٦	L
L	Ť	Н	Н
L	L	Х	Q ₀
Н	Х	х	L

logic symbol†

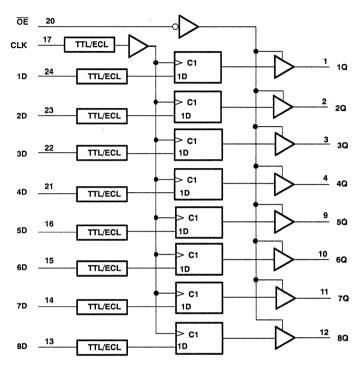


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



D3484, APRIL 1990

logic diagram (positive logic)



absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Supply voltage range, V _{FF}	
Input voltage range (TTL) (see Note 1)	– 1.2 V to 7 V
Input voltage range (ECL)	V _{EE} to 0 V
Input current range (TTL)	– 30 mA to 5 mA
Current out of any output	50 mA
Operating ambient temperature range	0°C to 75°C
Storage temperature range	- 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



SN10KHT5578 OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

D3484, APRIL 1990

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage		4.5	5	5.5	V
VEE	ECL supply voltage		- 4.94	- 5.2	- 5.46	V
VIH	TTL high-level input voltage		2			V
		0°C	- 1170		- 840	mV
ViH	ECL high-level input voltage [†]	25°C	- 1130		- 810	mV
		75°C	- 1070		- 735	mV
VIL	TTL low-level input voltage				0.8	٧
		0°C	- 1950		- 1480	mV
VIL	ECL low-level input voltage [†]	25°C	- 1950		- 1480	mV
		75°C	- 1950		- 1450	mV
Ιικ	TTL input clamp current				- 18	mA
TA	Operating ambient temperature (see Note 2)		0		75	°C

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITION	IS		MIN	TYP [‡]	MAX	UNIT
VIK	D inputs and CLK	V _{CC} = 4.5 V,	V _{EE} = - 4.94 V,	lj = 18 mA				- 1.2	V
ΙΙ	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 7 V				0.1	mA
ΊΗ	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = 2.7 V				20	μA
IIL	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = 5.46 V,	V _I = 0.5 V				0.5	mA
		V _{CC} = 5.5 V,	VEE = - 5.46 V,	$V_{I} = -840 \text{ V}$	0°C			350	
ΊΗ	OE only	V _{CC} = 5.5 V,	V _{EE} = - 5.46 V,	V _I = - 810 V	25°C			350	μΑ
		V _{CC} = 5.5 V,	VEE = 5.46 V,	V _I = - 735 V	75°C			350	
					0°C	0.5			
łμ	OE only	V _{CC} = 5.5 V,	$V_{EE} = -5.46 V_{r}$	$V_{I} = -1950 V$	25°C	0.5			μΑ
	1	75°C		75°C	0.5				
					0°C	- 1020		- 840	
V _{OH} †		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$	See Note 3	25°C	- 980		- 810	mV
					75°C	- 920		- 735	
					0°C	- 1950		- 1630	
V_{OL}^{\dagger}		V _{CC} = 4.5 V,	$V_{EE} = -5.2 V \pm 5\%$	See Note 3	25°C	- 1950		- 1630	mV
		1			75°C	- 1950		- 1600	
ІССН		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				17.5	25	mA
CCL		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				15	22	mA
^I EE		V _{CC} = 5.5 V,	V _{EE} = - 5.46 V				- 104	- 149	mA
Ci		V _{CC} = 5 V,	V _{EE} = - 5.2 V,	f = 10 MHz			4		pF

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only. ‡ All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.



NOTES: 2. Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse air flow greater than 500 linear ft/min is maintained.

^{3.} Outputs are terminated through a 50- Ω resistor to -2 V.

SN10KHT5578 OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE **EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE**

D3484, APRIL 1990

timing requirements

			V _{CC} = 4.5 V to V _{EE} = -4.94 V T _A = MIN to MA	to – 5.46 V,	UNIT
			MIN	MAX	
fclock	Clock frequency		0	180	MHz
	D	High	4		
tw	Pulse duration, CLK	Low	4		ns
	0	High	1.5		
tsu	Setup time, data before CLK↑	Low	2.5		ns
t _h Hold t	Hold time data ofter CLVA	High	1		
	Hold time, data after CLK†	Low	1		ns

switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	түр‡	MAX	UNIT
f _{max}			180			MHz
t _{PLH}	0114		0.8	2.2	4	
†PHL	CLK	Q ,	0.8	2.1	3.8	ns
tPLH t	ŌĒ		0.5	1.4	3.2	ns
t _{PHL}	OE .	Q	0.5	1.7	3.3	113
t _r		Y		1.5		ns
tf		Y		1.5		ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C. NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

SN100KT5578 OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

D3485, APRIL 1990-REVISED OCTOBER 1990

- 100K Compatible
- TTL Clock and ECL Control Inputs
- Noninverting Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic DIPs
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015

description

This octal TTL-to-ECL translator is designed to provide efficient translation between a TTL signal environment and a 100K ECL signal environment. This device is designed specifically to improve the performance and density of TTL-to-ECL CPU/bus-oriented functions such as memoryaddress drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the '5578 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

The output-control input \overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5578 is characterized for operation from 0°C to 85°C.

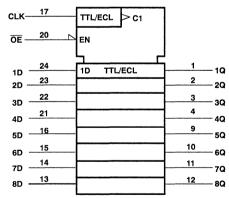
DW OR NT PACKAGE (TOP VIEW)

10[1 U	24	1D
2Q[2	23	2D
3Q[3	22	3D
4Q[4	21	4D
GND[5	20	OE(ECL)
GND[6	19	V_{CC}
GND[7	18	VEE
GND[8	17	CLK(TTL
5Q[9	16	5D
6Q[10	15	6D
7Q[11	14	7D
8Q[12	13	8D

Function Table

IN	IPUTS		OUTPUT (ECL)
ŌĒ	CLK	D	Q
L	1	L	L
L	1	н	Н
L	L	Х	Q_0
lн	Х	х	L

logic symbol†

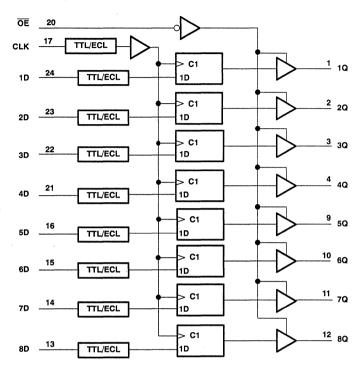


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



D3485, APRIL 1990-REVISED OCTOBER 1990

logic diagram (positive logic)



SN100KT5578 OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

D3485, APRIL 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	- 05 V to 7 V
Supply voltage range, V _{EE}	– 8 V to 0 V
Input voltage range (TTL) (see Note 1)	\dots – 1.2 V to 7 V
Input voltage range (ECL)	V _{EE} to 0 V
Input current range (TTL)	30 mA to 5 mA
Current out of any output	50 mA
Operating ambient temperature range	0°C to 85°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	TTL supply voltage	4.5	5	5.5	V
VEE	ECL supply voltage	- 4.2	- 4.5	- 4.8	V
VIH	TTL high-level input voltage	2			V
VIL	TTL low-level input voltage			0.8	V
ΊΚ	TTL input clamp current			- 18	mA
VIH	ECL high-level input voltage [‡]	- 1165		- 880	mV
VIL	ECL low-level input voltage‡	- 1810		- 1475	mV
TA	Operating ambient temperature (see Note 2)	0		85	°C

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted) (see Note 2)

	PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
VIK	D inputs and CLK	V _{CC} = 4.5 V,	V _{EE} = - 4.2 V,	lj = – 18 mA			- 1.2	V
11	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 7 V			0.1	mA
ΊΗ	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 2.7 V			20	μΑ
IIL	D inputs and CLK	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _I = 0.5 V			- 0.5	mA
ΊΗ	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IH} = - 880 mV			350	μΑ
1 _{IL}	OE only	V _{CC} = 5.5 V,	V _{EE} = - 4.8 V,	V _{IL} = - 1810 mV	0.50			μΑ
VOH [‡]		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	See Note 3	- 1020		- 880	mV
V _{OL} ‡		V _{CC} = 4.5 V,	$V_{EE} = -4.5 V \pm 0.3 V$,	See Note 3	- 1810		- 1620	mV
Іссн		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			17	24	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			14.5	21	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = - 4.8 V			- 104	149	mA .
Ci		V _{CC} = 5 V,	VEE = - 4.5 V,	f = 10 MHz		4		pF

[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only. § All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.



NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

NOTES: 2. Each 100KT series circuit has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained.

^{3.} Outputs are terminated through a 50- Ω resistor to – 2 V.

SN100KT5578 OCTAL TTL-TO-ECL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND OUTPUT ENABLE

D3485, APRIL 1990-REVISED OCTOBER 1990

timing requirements

			V _{CC} = 4.5 V V _{EE} = - 4.2 \ T _A = MIN to	/ to – 4.8 V,	UNIT	
	•		MIN	MAX		
fclock	Clock frequency		0 180			
	Pulse duration, CLK	High	1.5			
t _W		Low	2.5		ns	
	0	High	4			
t _{su}	Setup time, data before CLK†	Low	4		ns	
4.		High	1			
th	Hold time, data after CLK†	Low	1		ns	

switching characteristics over recommended ranges of supply voltage and operating ambient temperature (see Note 4)

PARAMETER	FROM (IINPUT)	TO (OUTPUT)	MIN	түр‡	мах	UNIT
f _{max}			180			MHz
t _{PLH}	0.14		0.8	2.3	4.1	
t _{PHL}	CLK	Q	0.8	2.2	3.8	ns
t _{PLH}	ŌĒ		0.5	1.4	3	
^t PHL	¬ 0₌	Q	0.5	1.7	3.4	ns
t _r		Y		1.5		ns
tę		Y		1.5		ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

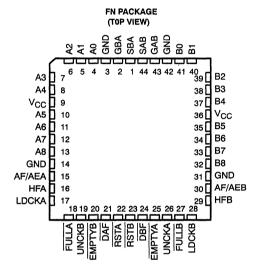
NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

[‡] All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.

General Information	1
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- Independent Asynchronous Inputs and **Outputs**
- Low-Power Advanced CMOS Technology
- **Bidirectional**
- 1024 Words by 9 Bits Each
- Programmable Almost Full/Almost Empty Flag

- Empty. Full, and Half-Full Flags
- Access Times of 25 ns With a 50-pF Load
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 22 ns Tvp
- **High Output Drive for Direct Bus Interface**



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ACT2235 is arranged as two 1024- by 9-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 40 MHz with access times of 25 ns in a bit-parallel format.

The 'ACT2235 consists of bus transceiver circuits, two 1024 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. GAB and GBA enable inputs are provided to control the transceiver functions. The SAB and SBA control inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transistion between stored and real-time data. Eight fundamental bus-management functions can be performed as shown on the operating modes page. multiplexed transmission of data directly from the data bus or from the internal FIFO memories. GAB and GBA



SN74ACT2235 1024 × 9 × 2 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY D3668, AUGUST 1990-REVISED OCTOBER 1990

functional description

Bus Lines (A0-A8, B0-B8). Data inputs and outputs for 9-bit-wide data.

Resets (RSTA, RSTB). A reset is accomplished in each direction by taking reset inputs RSTA and RSTB low. This initializes the empty flags EMPTYA and EMPTYB and the half-full flags HFA and HFB low. The full flags FULLA and FULLB and the almost full/almost empty flags (AF/AEA) and (AF/AEB) are initialized high. Both FIFOs must be reset upon power up.

Load Clocks (LDCKA, LDCKB). Data on the A bus (A0-A8) is written into FIFO A on a low-to-high transition of load clock A (LDCKA). Data on the B bus (B0-B8) is written into FIFO B on a low-to-high transition of load clock B (LDCKB). When the FIFOs are full, load clock signals have no effect on the data residing in memory.

Unload Clocks (UNCKA, UNCKB). Data in FIFO A is read to the B bus (B0-B8) on a low-to-high transition of unload clock A (UNCKA). Data in FIFO B is read to the A bus (A0-A8) on a low-to-high transition of unload clock B (UNCKB). When the FIFOs are empty, unload clock signals have no effect on data residing in memory.

G Enables (GAB, GBA). The G enables (GAB and GBA) control the transceiver output functions. When GBA is low, the A bus (A0-A8) is in the high-impedance state. When GAB is low, the B bus (B0-B8) is in the high-impedance state.

S Control Inputs (SAB, SBA). The S control inputs (SAB and SBA) select whether real-time or stored data is transferred. A low level selects real-time data, and a high level selects stored data. Eight fundamental bus-management functions can be performed as shown in the operating modes page.

Define Flag Inputs (DAF, DBF). The high-to-low transition of define A flag (DAF) stores the binary value on the A bus (A0-A8) as the almost empty/almost full offset value for FIFO A (X). The high-to-low transition of define B flag (DBF) stores the binary value of the B bus (B0-B8) as the almost full/almost empty offset value for FIFO B (Y).

Empty Flags (EMPTYA, EMPTYB). The empty flags (EMPTYA and EMPTYB) are low when their corresponding memories are empty and high when they are not empty.

Full Flags (FULLA, FULLB). The full flags FULLA and FULLB are low when their corresponding memories are full and high when they are not full.

Half-Full Flags (HFA, HFB). The half-full flags (HFA and HFB) are high when their corresponding memories contain 512 or more words and low when they contain 511 or less words.

Almost Full/Almost Empty flags (AF/AEA), (AF/AEB). The almost full/almost empty A flag (AF/AEA) is defined by the almost full/almost empty offset value for FIFO A (X). The AF/AEA flag is high when FIFO A contains X or less words or 1024 minus X words. The AF/AEA flag is low when FIFO A contains between X plus 1 or 1023 minus X words. The operation of the almost full/almost empty B flag (AF/AEB) is the same as AF/AEA for FIFO B.

Programming Procedure for AF/AEA

The almost full/almost empty flags (AF/AEA and AF/AEB) are programmed during each reset cycle. The almost full/almost empty offset value for FIFO A (X) and for FIFO B (Y) are either a user-defined value or the default values of X = 256 and Y = 256. Below are instructions to program AF/AEA using both methods. AF/AEB is programmed in the same manner for FIFO B.

User Defined X

Step 1: Take DAF from high to low. This stores A0 thru A8 as X.

Step 2: If RSTA is not already low, take RSTA low.

Step 3: With DAF held low, take RSTA high. This defines the AF/AEA flag using X.

Step 4: To retain the current offset for the next reset, keep DAF low.

Default X

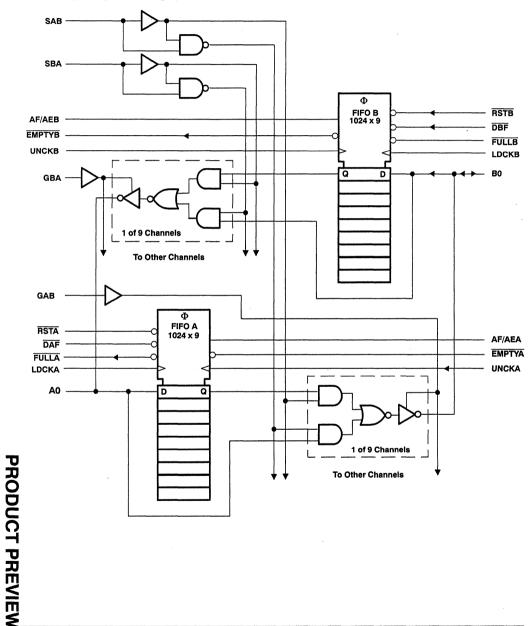
To redefine the AF/AE flag using the default value of X = 256, hold \overline{DAF} high during the reset cycle.





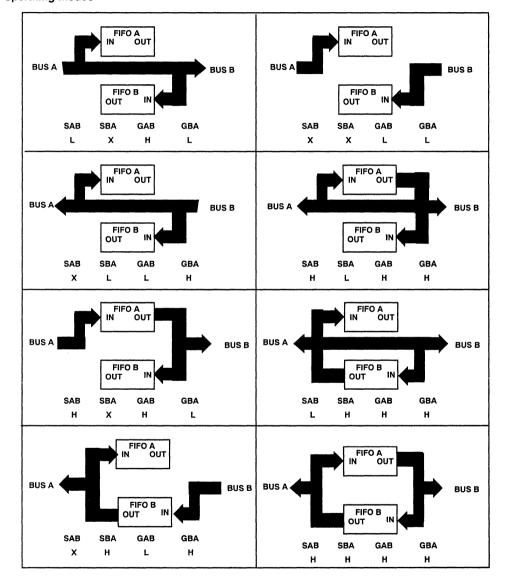
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



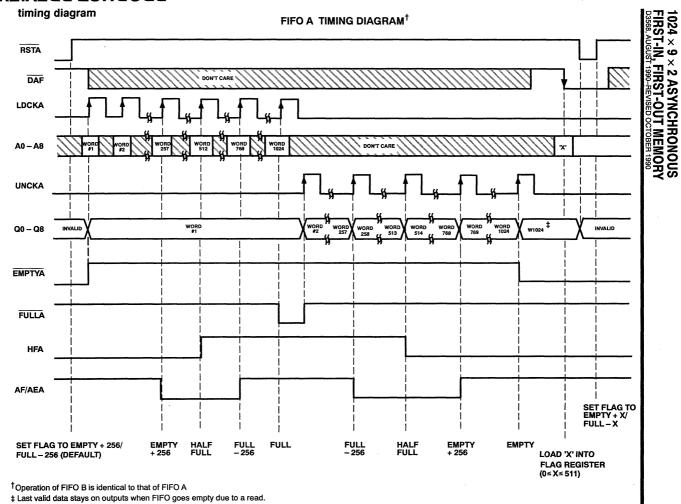


operating modes





PRODUCT PREVIEW



SELECT MODE CONTROL TABLE

CONTROL		OPER	ATION
SBA	SAB	A Bus	B Bus
L	L	Real Time B to A Bus	Real Time A to B Bus
н	L	FIFO B to A Bus	Real Time A to B Bus
L	н	Real Time B to A Bus	FIFO A to B Bus
н	н	FIFO B to A Bus	FIFO A to B Bus

OUTPUT ENABLE CONTROL TABLE

ENA	BLE	OPER	ATION
GBA	GAB	A Bus	B Bus
Н	Н	A Bus Enabled	B Bus Enabled
Н	L	A Bus Enabled	Isolation/Input to B Bus
L	Н	Isolation/Input to A Bus	B Bus Enabled
L	L	Isolation/Input to A Bus	Isolation/Input to B Bus

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage: Control inputs	7 V
I/O ports	
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SN74ACT2235 1024 × 9 × 2 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY D3568, AUGUST 1990-REVISED OCTOBER 1990

recommended operating conditions

	***************************************			MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	٧
VIH	High-level input voltage			2			V
VIL	Low-level input voltage					0.8	V
lari	High-level output current	A or B ports				-8	mA
ЮН	nigh-level output current	Status flags				-8	mA
la.	Low-level output current	A or B ports				16	mA
lOL	Low-level output current	Status flags				8	IIIA
f _{clock} Clock frequency	LDCKA or LDCKB		0		40	MHz	
	UNCKA or UNCKB		0		40	WHZ	
	RSTA or RSTB low						
	I DOWN	high					
	Pulse duration	LDCKA or LDCKB	low				ns
t _w	Pulse duration	LINOVA LINOVA	high				
		UNCKA or UNCKB	low				
		DAF or DBF high					
		Data before LDCKA or LDCKB↑					
		Define AF/AE: D0-D8 before DAF or DBF↓					
tsu	Setup time	Define AF/AE: DAF or DBF↓ before RSTA or RSTB↑					ns
		Define AF/AE (Default): DAF or DBF high before RSTA or	RSTB↑				
		RSTA or RSTB inactive (high) before LDCKA or LDCKB↑					
		Data after LDCKA or LDCKB↑					
		Define AF/AE: D0-D8 after DAF or DBF↓					
th	Hold time	Define AF/AE: DAF or DBF low after RSTA or RSTB↑					ns
		Define AF/AE (Default): DAF or DBF high after RSTA or F	STB↑				
		RSTA or RSTB inactive (high) after LDCKA or LDCKB↑					
TA	Operating free-air tempera	ature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDI	TIONS	MIN	TYP†	MAX	UN
VOH	High-level output voltage	V _{CC} = 4.5 V,	I _{OH} = – 8 mA	2.4			١
VOL	Low-level output voltage	V _{CC} = 4.5 V,	I _{OL} =16 mA			0.5	'
l _l	Input current	V _{CC} = 5.5 V,	VI = VCC or 0 V			± 5	μ
loz	High-impedance-state output current	V _{CC} = 5.5 V,	VO = VCC or 0 V			± 5	μ
ICC1 [‡]	Supply current	f _{clock} = 25 MHz§			200	230	m
ICC2 [‡]	Standby current	LDCKA or LDCKB = VIH,	VI = VIH or VIL		20	25	n
ICC3‡	Power down current	V _I = V _{CC} - 0.2 V or 0 V				400	μ
Ci	Input capacitance	V _I = 0 V,	f = 1 MHz		4		þ
Co	Output capacitance	V _O = 0 V,	f = 1 MHz		8		F
† All typic	cal values are at V _{CC} = 5 V, T _A = 25°C.					· · · · · · · · · · · · · · · · · · ·	
† All typic ‡ ICC tes	cal values are at V_{CC} = 5 V, T_A = 25°C. sted with outputs open. quencies greater than 25 MHz, I_{CC} = 200 m	nA + (6 mA • [f – 25]).					



switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX [†] ACT2235-XX ACT2235-28.5							UNIT
			MIN	TYP [‡]	MAX	MIN	MAX	MIN	MAX	
f _{max}	LDCK		40							
	UNCK		40				***************************************	l		MHZ
t _{pd}	LDCKA↑, LDCKB↑	B, A		22						ns
t _{pd}	UNCKA↑, UNCKB↑	B, A		20						ns
[†] PLH	LDCKA↑, LDCKB↑	EMPTYA, EMPTYB		12						ns
^t PHL	UNCKA†, UNCKB†	EMPTYA, EMPTYB		12						ns
^t PHL	RSTA↓, RSTB↓	EMPTYA, EMPTYB		12						ns
tPHL.	LDCKA†, LDCKB†	FULLA, FULLB		12						ns
t _{PLH}	UNCKA†, UNCKB†	FULLA, FULLB		12						ns
tPLH .	RSTA↓, RSTB↓	FULLA, FULLB		15						ns
^t PLH	RSTA↓, RSTB↓	AF/AEA, AF/AEB								ns
^t PLH	LDCKA↑, LDCKB↑	HFA, HFB								ns
[†] PHL	UNCKA†, UNCKB†	HFA, HFB								ns
^t PHL	RSTA↓, RSTB↓	HFA, HFB								ns
t _{pd}	SAB, SBA§	B, A		11						ns
t _{pd}	A, B	B, A		8						ns
t _{pd}	LDCKA†, LDCKB†	AF/AEA, AF/AEB		6						ns
t _{pd}	UNCKA†, UNCKB†	AF/AEA, AF/AEB		5						ns
ten	GBA, GAB	A, B		6						ns
^t dis	GBA, GAB	A, B		5						ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at 5 V, T_A = 25°C.

[§] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

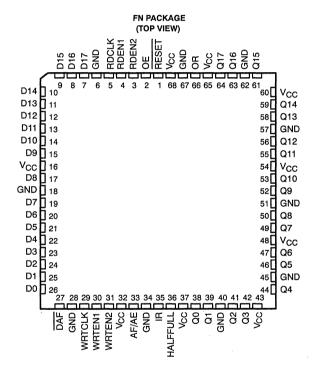
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

${\sf SN74ACT7801}$ 1024 × 18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

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- Independent Asynchronous Inputs and Outputs
- 1024 Words by 18 Bits Each
- Read and Write Operations Can Be Synchronized to Independent System Clocks
- Programmable Almost Full/Almost Empty Flag

- Input Ready, Output Ready, and Half Full Flags
- Cascadable in Word Width and/or Word Depth
- Fast Access Times of 15 ns With a 50-pF Load
- High Output Drive for Direct Bus Interface
- 3-State Q Outputs



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7801 is a 1024 by 18-bit FIFO for high speed and fast access times. It processes data at rates up to 40 MHz and access times of 15 ns in a bit-parallel format. Data outputs are noninverting with respect to the data inputs. Expansion is easily accomplished in both word-width and word-depth.

The SN74ACT7801 has normal input bus to output bus asynchronous operation. The special enable circuitry adds the ability to synchronize independent read and write (interrupts, requests) to their respective system clock.



1024 × 18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3489, APRIL 1990

inputs

Data In (D0-D17) — Data inputs for 18-bit wide data to be stored in the memory. Data lines D0-D8 also carry the Almost Full/Almost Empty Offset Value (X) on a high-to-low transition of Define Almost Full (DAF).

Reset (RESET) - A reset is accomplished by taking Reset (RESET) low and generating a minimum of four Read Clock (RDCLK) and Write Clock (WRTCLK) cycles. This ensures that the internal read and write pointers are reset and that the Output Ready flag (OR), the Half Full flag (HF), and the Input Ready flag (IR) are low; the Almost Full/Almost Empty flag (AF/AE) is high. The FIFO must be reset upon power up. With the Define Almost Full (DAF) at a low level, a low pulse on RESET defines the AF/AE status flag using the Almost Full/Almost Empty Offset Value (X), where X is the value previously stored. With DAF at a high level, a low level pulse on RESET defines the AF/AE flag using the default value of X = 256.

Write Enables (WRTEN1, WRTEN2) - The Write Enables (WRTEN1, WRTEN2) must be high before the rising edge of Write Clock (WRTCLK) for a word to be written into memory. The Write Enables do not affect the storage of the Almost Full/Almost Empty Offset Value (X).

Write Clock (WRTCLK) - Data is written into memory on a low-to-high transition of the Write Clock (WRTCLK) if the Input Ready status flag (IR) and the Write Enable control signals (WRTEN1, WRTEN2) are high, WRTCLK is a free running clock and functions as the synchronizing clock for all data transfers into the FIFO. The IR status flag is also driven synchronously with respect to the WRTCLK signal.

Read Enables (RDEN1, RDEN2) - Both Read Enables (RDEN1, RDEN2) must be high before the rising edge of Read Clock (RDCLK) to read a word out of memory. The Read Enables are not used to read the first word stored in memory.

Read Clock (RDCLK) - Data is read out of memory on a low-to-high transition at the Read Clock (RDCLK) input if the Output Ready status flag (OR), the Output Enable (OE), and the Read Enable control signals (RDEN1, RDEN2) are high. RDCLK is a free running clock and functions as the synchronizing clock for all data transfers out of the FIFO. The OR flag is also driven synchronously with respect to the RDCLK signal.

Define Almost Full (DAF) - The high-to-low transition of the Define Almost Full (DAF) input stores the binary value of Data Inputs D0-D8 as the Almost Full/Almost Empty Offset Value (X). With DAF held low, a low pulse on the Reset (RESET) defines the Almost Full/Almost Empty flag (AF/AE) using X.

Output Enable (OE) - Data Out (Q0-Q17) and the Output Ready flag (OR) are at a high-impedance state when the Output Enable (OE) is low. OE must be high before the rising edge of Read Clock (RDCLK) to read a word from memory.

outputs

Data Out (Q0-Q17) - The first data word to be loaded into the FIFO is moved to the Data Out (Q0-Q17) register on the rising edge of the third Read Clock (RDCLK) pulse to occur after the first valid write. The Read Enable (RDEN1, RDEN2) inputs do not affect this operation. Following data is unloaded on the rising edge of RDCLK when RDEN1, RDEN2, and the Output Ready flag (OR) are high.

Input Ready Flag (IR) - The Input Ready Flag (IR) is high when the FIFO is not full and low when the device is full. During reset, the IR flag is set low on the rising edge of the second Write Clock (WRTCLK) pulse. The IR flag is set high on the rising edge of the second WRTCLK pulse after reset RESET goes high. After the FIFO is filled and IR is set low, IR is set high on the second WRTCLK pulse to occur after the first valid read.

Output Ready Flag (OR) - The Output Ready Flag (OR) is high when the FIFO is not empty and low when it is empty. During reset, the OR flag is set low on the rising edge of the third Read Clock (RDCLK) pulse. The OR flag is set high on the rising edge of the third RDCLK pulse to occur after the first word is written into the FIFO. OR is set low on the rising edge of the first RDCLK pulse after the last word is read.

Half Full Status Flag (HF) - The Half Full flag (HF) is high when the FIFO contains 513 or more words and is low when it contains 512 or less words.



SN74ACT78011024 × 18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

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Almost Full/Almost Empty Status Flag (AF/AE) – The Almost Full/Almost Empty flag (AF/AE) is defined by the Almost Full/Almost Empty Offset Value (X). The AF/AE flag is high when the FIFO contains X + 1 or less words, or 1025 minus X or more words. The AF/AE flag is low when the FIFO contains between X + 2 and 1024 minus X words.

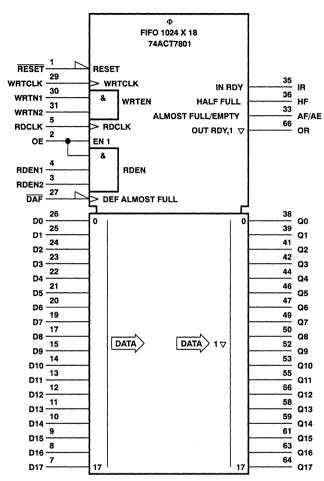
Programming Procedure for AF/AE—The Almost Full/Almost Empty flag (AF/AE) is programmed during each reset cycle. The Almost Full/Almost Empty Offset Value (X) is either a user-defined value or the default value of X = 256. Below are instructions to program AF/AE using both methods.

User-Defined X

- Step 1. Take DAF from high to low.
- Step 2. If RESET is not already low, take RESET low.
- Step 3. With DAF held low, take RESET high. This defines the AF/AE flag using X.
- Step 4. To retain the current offset for the next reset, keep DAF low.

Default X – To redefine the AF/AE flag using the default value of X = 256, hold \overline{DAF} high during the reset cycle.

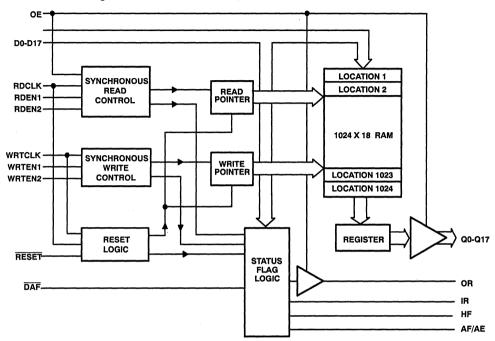
logic symbol†

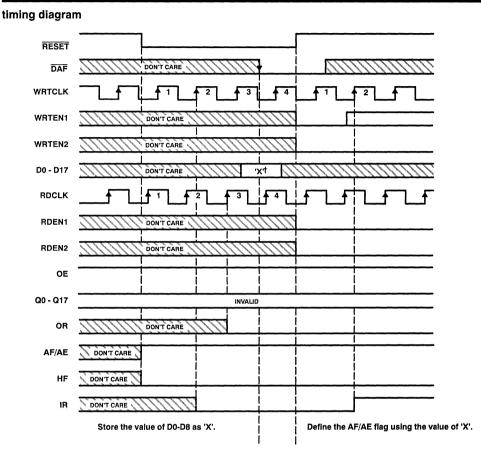


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984.

D3489 APRIL 1990

functional block diagram





^{†&#}x27;X' is the binary value of D0 - D8 only

Figure 1. Reset Cycle: Define AF/AE Using the Value of 'X'

D3489, APRIL 1990

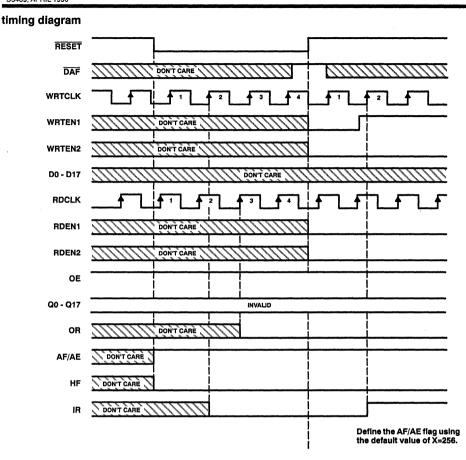


Figure 2. Reset Cycle: Define AF/AE Using the Default



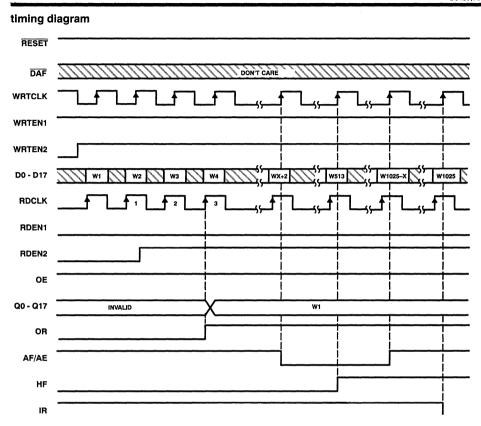
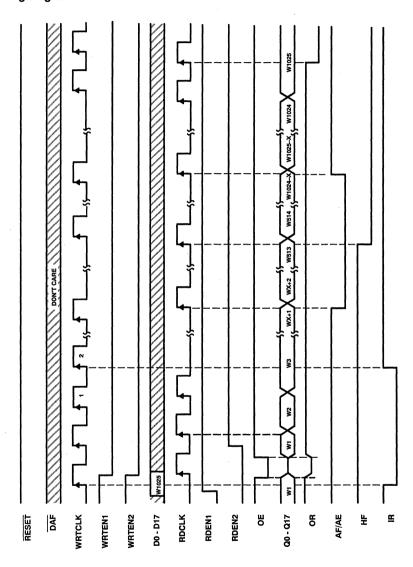


Figure 3. Write

timing diagram



dire 4. Rea

$$\rm SN74ACT7801$$ 1024 × 18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3489, APRIL 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –	- 0.5 V to 7 V
Input voltage	7 \
Voltage applied to a disabled 3-state output	
Operating free-air temperature range	0°C to 70°C
Storage temperature range – 65	°C to 150°C

recommended operating conditions

			ACT78	801-15	ACT78	01-18	ACT78	01-20	
		PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	٧
VIH	High-level input	voltage	2		2		2		٧
VIL	Low-level input	voltage		0.8		0.8		0.8	V
ЮН	High-level outpu	it current		- 8		- 8		- 8	mA
loL	Low-level outpu	t current		16		16		16	mA
fclock	Clock frequency	,	40		35		28.5		MHz
		Data in (D0-D17), high or low	10		12		14		
		WRTCLK high	7		8.5		10		
		WRTCLK low	15		15		15		
	5	RDCLK high	7		8.5		10		
tw	Pulse duration	RDCLK low	15		15		15		ns
		DAF high	10		10		10		
		WRTEN1, WRTEN2 high or low	10		10		10		
		OE, RDEN1, RDEN2 high or low	10		10		10		
		Data in (D0-D17) before WRTCLK†	5		5		5		
		WRTEN1, WRTEN2 before WRTCLK†	5		5		5		
		OE, RDEN1, RDEN2 before RDCLK†	5		5		5		
t _{su}	Setup time	RESET: RESET low before first WRTCLK and RDCLK†	7		7		7		ns
		Define AF/AE: D0-D8 before DAF↓	5		5		5		
		Define AF/AE: DAF↓ before RESET↑	7		7		7		
		Define AF/AE (default): DAF high before RESET↑	5		5		5		
		Data in (D0-D17) after WRTCLK↑	1		1		1		
		WRTEN1, WRTEN2 after WRTCLK↑	1		1		1		
		OE, RDEN1, RDEN2 after RDCLK†	1		1		1		
th	Hold time	RESET: RESET low after fourth WRTCLK and RDCLK↑	0		0		0		ns
		Define AF/AE: D0-D8 after DAF↓	1		1		1		
	ļ	Define AF/AE: DAF low after RESET↑	0		0		0		
		Define AF/AE (default): DAF high after RESET↑	1		1		1		
TA	Operating free-a	ir temperature	0	70	0	70	0	70	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST C	TEST CONDITIONS			MAX	UNIT
VOH	High-level output voltage	V _{CC} = 4.5 V,	IOH = - 8 mA	2.4			٧
VOL	Low-level output voltage	V _{CC} = 4.5 V,	I _{OL} = 16 mA			0.5	٧
lj .	Input current	V _{CC} = 5.5 V,	VI = VCC or 0			± 5	μΑ
loz	High-impedance-state output current	V _{CC} = 5.5 V,	VO = VCC or 0			± 5	μΑ
ICC1‡	Supply current	f _{clock} = 25 MHz§			200	230	mA
ICC2‡	Supply current, standby	WRTCLK = VIH,	VI = VIH or VIL		20	25	mA
ICC3 [‡]	Supply current, power down	V _I = V _{CC} - 0.2 V or	0			400	μА
Ci		V _I = 0,	f = 1 MHz		4		pF
Co		V _O = 0,	f = 1 MHz		8		рF

switching characteristics over recommended operating free-air temperature range (see Note 1)

						= 4.5 V to	5.5 V,			
					CL = !					
PARAMETER	FROM	то	1		_	500 Ω,				UNIT
	(INPUT)	(OUTPUT)			TA =	0°C to 70				
			AC	T7801-1	15	ACT78	801-18	ACT78	01-20	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	WRTCLK or RDCLK		40			35		28.5		MHz
t _{pd}	RDCLK†	Any Q	5	12	15	5	18	5	20	ns
t _{pd} ¶	RDCLK†	Any Q		10.5						ns
t _{pd}	WRTCLK†	IR	4		10	4	12	4	14	ns
t _{pd}	RDCLK†	OR	4		10	4	12	4	14	ns
t _{pd}	WRTCLK↑	AF/AE	7		20	7	22	7	24	ns
t _{pd}	RDCLK†	AF/AE	7		20	7	22	7	24	ns
t _{pd}	WRTCLK†	HF	6		19	6	21	6	23	ns
t _{pd}	RDCLK†	HF	6		19	6	21	6	23	ns
^t PLH	RESET↓	AF/AE	4		19	4	21	4	23	ns
^t PHL	RESET↓	HF	4		21	4	23	4	25	ns '
t _{en}	OE	Any Q, OR	2		11	2	11	2	11	ns
t _{dis}	OE	Any Q, OR	2		14	2	14	2	14	ns

This parameter is measured at 30 pF (see Figure 5).

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. † I_{CC} tested with outputs open. § For frequencies greater than 25 MHz, I_{CC} = 200 mA + (6 mA • [f – 25 MHz]).

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME

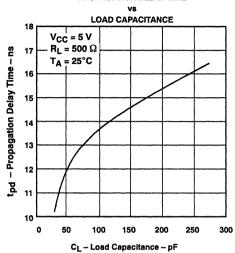


Figure 5

TYPICAL APPLICATION DATA

expanding the SN74ACT7801

The SN74ACT7801 is expandable in width and depth. Expanding in word depth offers special timing considerations:

- After the first data word is loaded into the FIFO, the word is unloaded and the Output Ready flag (OR)
 goes high after N x 3 Read Clock (RDCLK) cycles, where N is the number of devices used in depth
 expansion.
- 2. After the FIFO is filled and the Input Ready flag (IR) goes low and the first word is unloaded, the IR flag is set high after N × 2 Write Clock cycles, where N is the number of devices used in depth expansion.

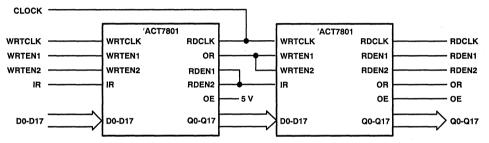


Figure 6. Word-Depth Expansion: 2048-Word by 18-Bit, N = 2

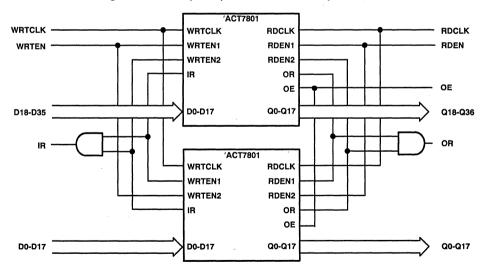


Figure 7. Word-Width Expansion: 1024-Word by 36-Bit

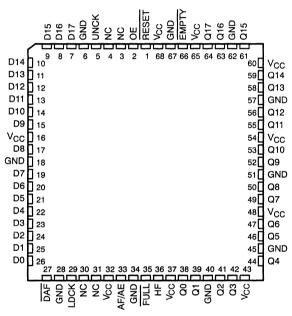


D3599, AUGUST 1990-REVISED OCTOBER 1990

- Independent Asynchronous Inputs and Outputs
- Low-Power Advanced CMOS Technology
- 1024 Words by 18 Bits Each
- Programmable Almost Full/Almost Empty Flag
- Empty, Full, and Half-Full Flags

- Fast Access Times of 25 ns With a 50-pF
- Fall-Through Time . . . 20 ns Typical
- Data Rates From 0 to 50 MHz
- High Output Drive for Direct Bus Interface
- 3-State Q Outputs

FN PACKAGE (TOP VIEW)



NC - No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ACT7802 is a 1024- by 18-bit FIFO for high-speed applications. It processes data in a bit-parallel format at rates up to 50 MHz and access times of 25 ns.

Data is written into the FIFO memory on a low-to-high transition on the Load Clock input (LDCK) and is read out on a low-to-high transition on the Unload Clock input (UNCK). The memory is full when the number of words clocked in exceeds by 1024 the number of words clocked out. When the memory is full, LDCK has no effect on the data in the memory; when the memory is empty, UNCK has no effect.

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SN74ACT7802 1024×18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3599, AUGUST 1990-REVISED OCTOBER 1990

The FIFO memory status is monitored by the Full (FULL), Empty (EMPTY), Half-Full (HF), and Almost Full/Almost Empty (AF/AE) flags. The FULL output is low when the memory is full; the EMPTY output is low when the memory is empty. The HF output is high when the memory contains 512 or more words and low when it contains less than 512 words. The level of the AF/AE flag is determined by both the number of words in the FIFO and a user-definable offset X. AF/AE is high when the FIFO is almost full or almost empty, i.e., when it contains X or less words or (1024-X) or more words. The Almost Full/Almost Empty offset value is either user-defined or the default value of 256; it is programmed during each reset cycle as follows:

- User-Defined X:
 - Take DAF low
 - Take RESET low
 - With DAF held low, take RESET high. This defines X as the value on D0-D8.
 - To retain the current offset, keep DAF low during the following reset cycle.
- Default X:
 - X defaults to 256 if DAF is held high during the reset cycle.

A low level on the Reset (RESET) input resets the FIFO internal clock stack pointers and sets FULL high, AF/AE high, HF low, and EMPTY low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up.

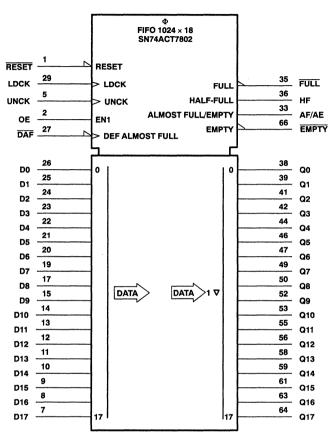
The Q outputs are noninverting and are in the high-impedance state when the Output Enable (OE) input is low.

When writing to the FIFO after a reset pulse or when the FIFO is empty, the first active transition on LDCK drives EMPTY high and causes the first word written to the FIFO to appear on the Q outputs. Therefore, an active transition on UNCK is not required to read the first word written to the FIFO. Each subsequent read from the FIFO requires an active transition on UNCK.

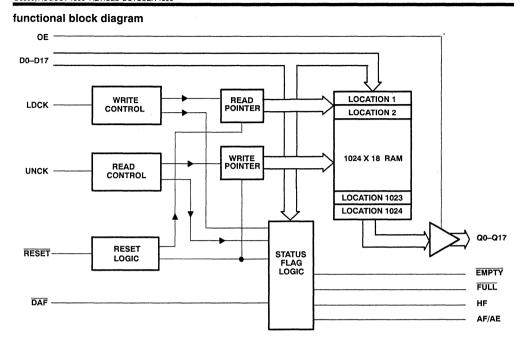
The 'ACT7802 can be cascaded in the word-width direction but not in the word-depth direction.



logicsymbol †

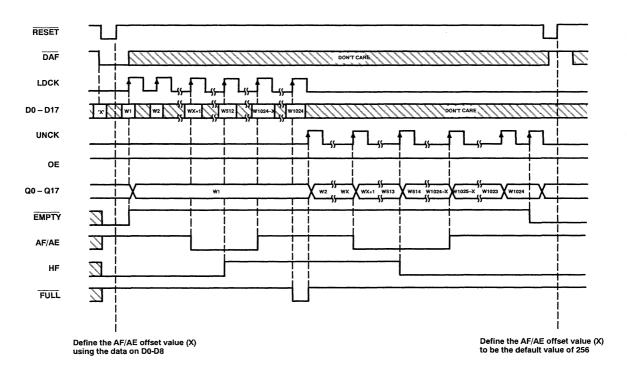


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984.





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 1024×18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

1024 × 18 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3599, AUGUST 1990-REVISED OCTOBER 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} Input voltage	
Voltage applied to a disabled 3-state output	
Operating free-air temperature range	. 0°C to 70°C
Storage temperature range	65°C to 150°C

recommended operating conditions

			ACT78	02-XX	ACT78	02-35	ACT780	2-28.5	
		•	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	4.5	5.5	٧
VIH	High-level input	voltage	2		2		2		٧
VIL	Low-level input	voltage		0.8					٧
ЮН	High-level outpo	ut current		-8		8		-8	mA
lOL	Low-level output	t current		16		16		16	mA
fclock	Clock frequency	/							MHz
		LDCK high							
		LDCK low							
		UNCK high							
t _W	Pulse duration	UNCK low							ns
		DAF high							
		RESET low							
		Data in (D0-D7) before LDCK†							
		RESET inactive (high) before LDCK↑							
	0.1.11	LDCK (inactive) before RESET↑							
tsu	Setup time	Define AF/AE: D0-D8 before DAF↓							ns
		Define AF/AE: DAF↓ before RESET↑							
		Define AF/AE (default): DAF high before RESET↑							
		Data in (D0-D7) after LDCK†							
		RESET inactive (high) after LDCK†							
th	Hold time	Define AF/AE: D0-D8 after DAF↓							ns
		Define AF/AE: DAF low after RESET↑							
		Define AF/AE (default): DAF high after RESET↑							
TA	Operating free-a	air temperature	0	70	0	70	0	70	°C



[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

D3599, AUGUST 1990-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST	TEST CONDITIONS			MAX	UNIT
Vон	High-level output voltage	V _{CC} = 4.5 V,	I _{OH} = – 8 mA	2.4			٧
VOL	Low-level output voltage	V _{CC} = 4.5 V,	I _{OL} = 16 mA			0.5	٧
Ŋ	Input current	V _{CC} = 5.5 V,	$V_I = V_{CC}$ or 0 V			± 5	μА
loz	High-impedance-state output current	V _{CC} = 5.5 V,	VO = VCC or 0 V			± 5	μА
ICC1 [‡]	Supply current	f _{clock} = 30 MHz			200		mA
ICC2‡	Supply current, standby	LDCK = VIH,	VI = VIH or VIL		20		mA
ICC3‡	Supply current, power down	V _I = V _{CC} - 0.2 V c	or 0		200		μΑ
Ci		V _I = 0 V,	f = 1 MHz				pF
Co		V _O = 0 V,	f = 1 MHz				pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPICAL APPLICATION DATA

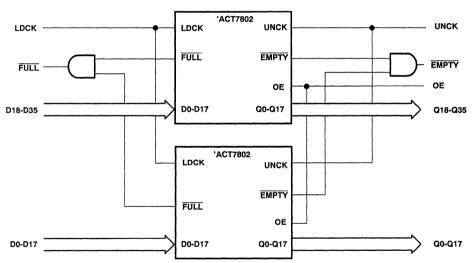


Figure 1. Word-Width Expansion: 1024-Word by 36-Bit



[‡] ICC tested with outputs open.

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3486, MARCH 1990

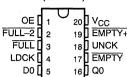
- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 14 ns Typ
- 3-State Outputs
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs

description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

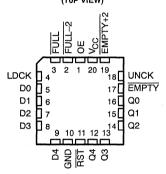


DW OR N PACKAGE

(TOP VIEW)

19 EMPTY+2 15 Q1 D1 Г 6 D2 1 7 14 DQ2 13 D Q3 рз П 8 D4 👖 12 Q4 9 11 RST GND [10

> FN PACKAGE (TOP VIEW)



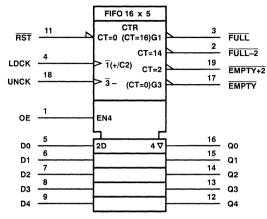
Status of the FIFO memory is monitored by the FULL, EMPTY, FULL-2, and FULL+2 output flags. The FULL output is low when the memory is full and high when it is not full. The FULL-2 output is low when the memory contains 14 data words. The EMPTY output is low when the memory is empty and high when it is not empty. The EMPTY+2 output is low when two words remain in memory.

A low level on the reset input (RST) resets the internal stack control pointers and also sets EMPTY low and sets FULL, FULL-2, and EMPTY+2 high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK after either a RST pulse or from an empty condition causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS229B is characterized for operation from 0°C to 70°C.

D3486, MARCH 1990

logic symbol†

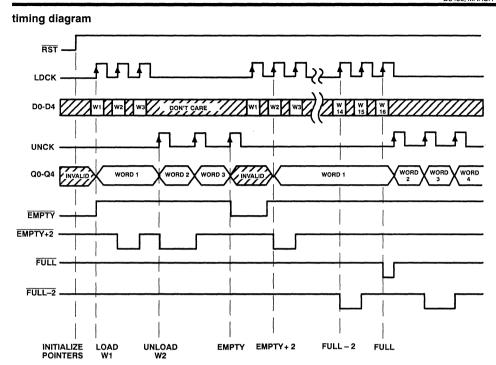


[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for DW and N packages.

D3486, MARCH 1990

logic diagram (positive logic) RING COUNTER 1 CTR DIV 16 Write Write 10 Address 11 12 13 14 CT=1 15 RING COUNTER 1 CTR 2 DIV 16 3 Read 10 Address 11 11 RAM 16 x 5 RST 13 EN 14 CT=1 15 16 16 1A, 3D 15 Q1 14 D2 Q2 13 9 12 Q4 COMP_{P=Q} 17 EMPTY P=Q+2 3 FULL P=Q-2 FULL-2 19 EMPTY+2 Pin numbers shown are for DW and N packages.





absolute maximum ratings over operating free-air temperature range (unless otherwise	noted)†
Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range 0	°C to 70°C
Storage temperature range	C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

D3486, MARCH 1990

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltge		2			V
VIL	Low-level input voltge	,			0.8	V
Jan.	High-level output curent	Q outputs			- 1.6	
ЮН	High-level output curent	Status flags			- 0.4	mA
	I I I I I I I I	Q outputs			24	
IOL	Low-level output curent	Status flags			8	mA
,	Ol all facilities	LDCK	0	0 40		
fclock	Clock frequency UN	UNCK	0		40	MHz
		RST low	18			
		LDCK low	15			
t _w	Pulse duration	LDCK high	10			ns
		UNCK low	15			
		UNCK high	10			
		Data before LDCK↑	8			
t _{su}	Setup time	RST (inactive) before LDCK↑	5			ns
		LDCK (inactive) before RST↑	5			
th	Hold time	Data after LDCK↑	5			ns
TA	Operating free-air temperature		0		70	°C

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs.

Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CON	MIN	TYPT	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	lμ = 18 mA			- 1.2	٧
V	Q outputs	V _{CC} = 4.5 V,	I _{OL} = - 2.6 mA	2.4	3.2		.,
VOH	Status flags	V _{CC} = 4.5 V to 5.5 V,	I _{OL} = - 0.4 mA	V _{CC} -2			7 V
	0	V _{CC} = 4.5 V,	IOL = 12 mA		0.25	0.4	
.,	Q outputs	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	V V μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ
VOL	Ctatus flags	V _{CC} = 4.5 V,	IOL = 4 mA		0.25	0.4	V
	Status flags	V _{CC} = 4.5 V,	IOL = 8 mA		0.35	0.5	
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V			20	μΑ
lozL		V _{CC} = 5.5 V,	V _O = 0.4 V			- 20	μΑ
l _l		V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
lн		V _{CC} = 5.5 V,	V _I = 2.7 V			20	μА
liL.		V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.2	mA
10‡		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		- 112	mA
Icc		V _{CC} = 5.5 V			85	140	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

${\bf SN74ALS229B} \\ {\bf 16 \times 5~ASYNCHRONOUS~FIRST-IN,~FIRST-OUT~MEMORY}$

D3486, MARCH 1990

switching characteristics (see Note 2)

			V _{CC} = 4.5 \ C _L = 50 pF,		
PARAMETER	FROM	то	R1 = 500 Ω		UNIT
r Anameren	(INPUT)	(OUTPUT)	R2 = 500 Ω		Olti
			$T_A = 0^{\circ}C$ to	70 °C	
			MIN	MAX	
	LDCK		40		
	UNCK		40		
^t pd	LDCK†	Any Q	6	30	ns
^t pd	UNCK†	Any Q	6	30	ns
t _{PLH}	LDCK†	EMPTY	5	25	ns
t _{PHL}	UNCK†	EMPTY	6	27	ns
t _{PHL}	RST↓	EMPTY	5	26	ns
t _{pd}	LDCK†	EMPTY+2	7	33	ns
t _{pd}	UNCK↑	EMPTY+2	9	35	ns
t _{PLH}	RST↓	EMPTY+2	9	33	ns
t _{pd}	LDCK†	FULL- 2	7	33	ns
t _{pd}	UNCK†	FULL- 2	9	35	ns
t _{PLH}	RST↓	FULL- 2	9	33	ns
^t PHL	LDCK†	FULL	6	27	ns
t _{PLH}	UNCK†	FULL	5	25	ns
tPLH	RST↓	FULL	8	31	ns
t _{en}	OE†	Q	2	15	ns
t _{dis}	OE1	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN74ALS232B 16×4 ASYNCHRONOUS FIRST IN, FIRST OUT MEMORY

D3247, FEBRUARY 1989

 Independent Asynchronous Inputs and Outputs

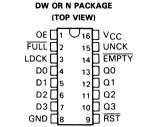
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs
- 16 Words by 4 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 14 ns Typ
- 3-State Outputs

description

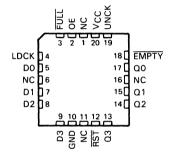
This 64-bit memory uses Advanced Low-Power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.



FN PACKAGE (TOP VIEW)



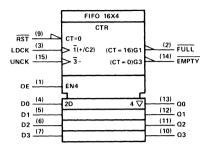
NC-No internal connection.

Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output is low when the memory is full and high when the memory is not full. The EMPTY output is low when the memory is empty and high when it is not empty.

A low level on the reset input (RST) resets the internal stack control pointers and also sets EMPTY low and sets FULL high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK after either a RST pulse or from an empty condition causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect either the FULL or EMPTY output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

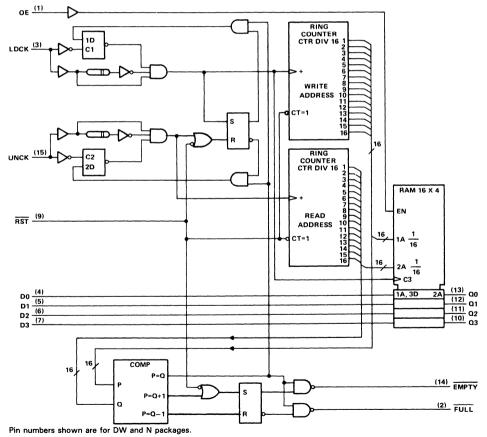
D3247, FEBRUARY 1989

logic symbol†



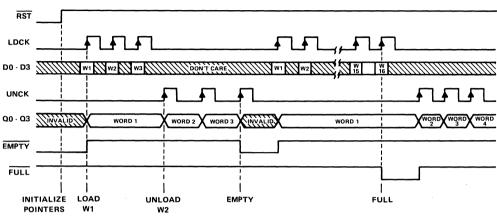
[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

logic diagram (positive logic)



D3247, FEBRUARY 1989





absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, ACC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range
Storage temperature range65 °C to 150 °C

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	V
1	High-level output current	Q outputs			- 2.6	1
ЮН	nigh-level output current	FULL, EMPTY			-0.4	mA
1	Lauriana antanà amana	Q outputs			24	4
lOL	Low-level output current	FULL, EMPTY			8	mA
	† Clast factories	LDCK	0 40	40	1	
Tclock	[†] Clock frequency	UNCK	0		40	MHz
		RST low	18			
		LDCK low	15			
tw	Pulse duration	LDCK high	10			ns
		UNCK low	15			İ
		UNCK high	10			ĺ
	C-1	Data before LDCK1	8			
t _{su}	Setup time	LDCK inactive before RST↑	5			ns
	11-14 4:	Data after LDCK↑	5			
th	Hold time	LDCK inactive after RST↑	5			ns
TA	Operating free-air temperature				70	°C

†The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz. NOTE 1: To ensure proper operation, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise

or glitching on the clock inputs that violates limits for maximum V_{IL}, minimum V_{IH}, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.



16 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3247, FEBRUARY 1989

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

ı	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	l _l = -18 mA			-1.2	٧
V	FULL, EMPTY	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2	2	-1.2 V 0.4 0.5 0.4 0.5 20 0.1 mA 20 20	V
VOH	Q outputs	$V_{CC} = 4.5 V,$	I _{OH} = −2.6 mA	2.4	3.2		·
	O outnuto	$V_{CC} = 4.5 V$	IOL = 12 mA		0.25	0.4	
VOL	Q outputs	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	V
VOL	FULL, EMPTY	$V_{CC} = 4.5 V,$	IOH = 4 mA		0.25	0.4] `]
	FULL, EIVIPTY	V _{CC} = 4.5 V,	IOL = 8 mA		0.35	-1.2 0.4 0.5 0.4 0.5 20 -20 0.1 20 -0.2	
lozh		$V_{CC} = 5.5 V,$	V _O = 2.7 V			20	μΑ
lozL		V _{CC} = 5.5 V,	V _O = 0.4 V			- 20	μΑ
4		V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
ЧН		V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
IIL		$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.2	mA
lo‡		$V_{CC} = 5.5 V,$	V _O = 2.25 V	- 30		-112	mA
ICC		V _{CC} = 5.5 V			80	125	mA

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	C _L R1 R2	= 50 pl = 500 s = 500 s = 500 s	=, n, n,	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0 °C to 70 °C		UNIT
	LDCK		MIN	TYP	MAX	MIN	MAX	
f _{max}	LDCK		 	50 50		40		MHz
^t pd	LDCK†	Any Q		14	23	6	30	ns
t _{pd}	UNCK↑	Any Q		15	23	6	30	ns
^t PLH	LDCK↑	EMPTY		13	20	5	25	ns
[†] PHL	UNCK†	EMPTY		15	22	6	27	ns
[†] PHL	RST↓	EMPTY	1	15	21	5	26	ns
[†] PHL	LDCK†	FULL		15	22	6	27	ns
[†] PLH	UNCK†	FULL		13	20	5	25	ns
^t PLH	RST↓	FULL		16	23	7	28	ns
t _{en}	OE↑	Q		5	12	1	14	ns
^t dis	OE↓	Q		5	12	1	16	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN74ALS233B 16×5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D4 Γ

GND

9

D3487, MARCH 1990

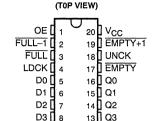
- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 14 ns Typ
- 3-State Outputs
- Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs

description

This 80-bit memory uses Advanced Low-Power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

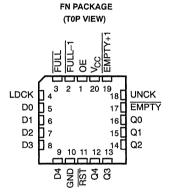
Data is written into memory on a low-to-high transition at the load clock input (LDCK) and is read out on a low-to-high transition at the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.



12 Q4

RST

DW OR N PACKAGE



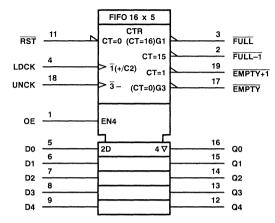
Status of the FIFO memory is monitored by the FULL, EMPTY, FULL—1, and FULL+1 output flags. The FULL output is low when the memory is full and high when it is not full. The FULL—1 output is low when the memory contains 15 data words. The EMPTY output is low when the memory is empty and high when it is not empty. The EMPTY+1 output is low when two words remain in memory.

A low level on the reset input (RST) resets the internal stack control pointers and also sets EMPTY low and sets FULL, FULL-1, and EMPTY+1 high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a RST pulse or from an empty condition, causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable input (OE) is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.

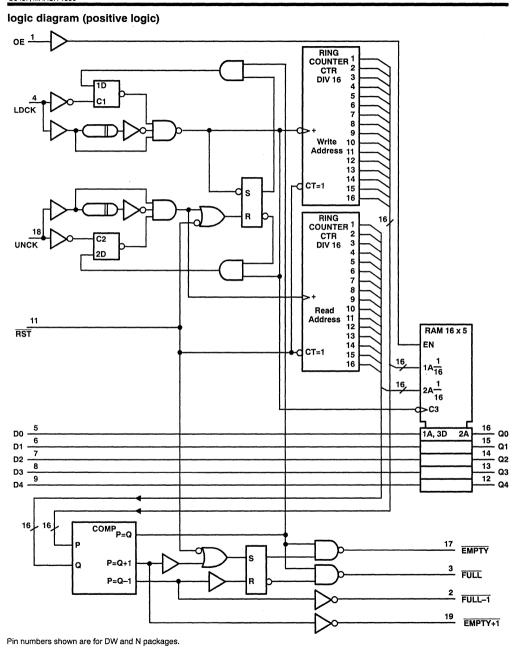
D3487, MARCH 1990

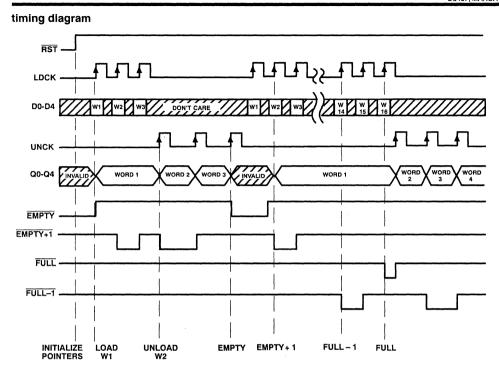
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for DW and N packages.

D3487, MARCH 1990





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)	t
Supply voltage, V _{CC}	' V
Input voltage, V ₁	' V
Voltage applied to a disabled 3-state output	i۷
Operating free-air temperature range	°C
Storage temperature range – 65°C to 150	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS233B 16×5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3487 MARCH 1990

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
lou	High-level output current	Q outputs			1.6	mA
ЮН	Thigh-level output current	Status flags			- 0.4	mA
1	I am lavel autout aumant	Q outputs			24	mA
OL	Low-level output current	Status flags			8	mA
	Olask frames	LDCK	0		40	MHz
fclock	Clock frequency	UNCK	0		40	
		RST low	18			ns
		LDCK low	15			
t _w	Pulse duration	LDCK high	10			
I _{OL}	•	UNCK low	15			1
		UNCK high	10		5 5.5 0.8 -1.6 -0.4 24 8 40	
		Data before LDCK†	8			
^t su	Setup time	RST (inactive) before LDCK↑	5			ns
		LDCK (inactive) before RST↑	5			
th	Hold time	Data after LDCK↑	5			ns
TA	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs.

Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CON	DITIONS	MIN	TYP†	MAX	UNIT
VIK		V _{CC} = 4.5 V,	l _l = – 18 mA			- 1.2	٧
Vон	Q outputs	V _{CC} = 4.5 V,	I _{OL} = 2.6 mA	2.4	3.2		V
тОп	Status flags	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = - 0.4 mA	V _{CC} ⁻²			
	0	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4	
.,	Q outputs	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	.,
VOL		V _{CC} = 4.5 V,	I _{OL} = 4 mA		0.25	0.4	V
	Status flags	V _{CC} = 4.5 V,	I _{OL} = 8 mA		0.35	0.4 0.5 20 20	
^I OZH		V _{CC} = 5.5 V,	V _O = 2.7 V			20	μΑ
lozL		V _{CC} = 5.5 V,	V _O = 0.4 V			- 20	μΑ
11		V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
ΊΗ		V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
IJL		V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.2	mA
10 [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		- 112	mA
Icc		V _{CC} = 5.5 V			88	133	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

D3487, MARCH 1990

switching characteristics (see Note 2)

			V _{CC} = 4.5 V C _L = 50 pF,		
PARAMETER	FROM	то	R1 = 500 Ω		UNIT
	(INPUT)	(OUTPUT)	$R2 = 500 \Omega$		
			$T_A = 0$ °C to		
			MIN	MAX	
	LDCK		40		
	UNCK		40		
t _{pd}	LDCK↑	Any Q	6	32	ns
t _{pd}	UNCK†	Any Q	6	30	ns
^t PLH	LDCK†	EMPTY	5	25	ns
t _{PHL}	UNCK†	EMPTY	6	27	ns
^t PHL	RST↓	EMPTY	5	25	ns
^t pd	LDCK↑	EMPTY+1	7	34	ns
t _{pd}	UNCK†	EMPTY+1	7	34	ns
tPLH	RST↓	EMPTY+1	8	31	ns
t _{pd}	LDCK∱	FULL- 1	9	33	ns
t _{pd}	UNCK†	FULL- 1	8	32	ns
t _{PLH}	RST↓	FULL- 1	11	32	ns
^t PHL	LDCK↑	FULL	6	27	ns
t _{PLH}	UNCK†	FULL	5	25	ns
^t PLH	RST↓	FULL	9	30	ns
ten	OE↑	Q	2	15	ns
t _{dis}	OE↓	Q	1	15	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS234, SN74ALS234 64 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

D2958, OCTOBER 1986-REVISED APRIL 1988

- Asynchronous Operation
- Organized as 64 Words of 4 Bits
- Data Rates From 0 to 30 MHz
- 3-State Outputs
- Similar to MMI67401B With Higher Speed and 3-State Outputs
- Dependable Texas Instruments Quality and Reliability

description

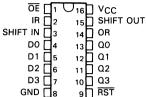
The SN54ALS234 and SN74ALS234 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS234 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or RST goes low.

SN54ALS234 . . . J PACKAGE
SN74ALS234 . . . DW OR N PACKAGE
(TOP VIEW)

OE TI U16T VCC



SN54ALS234 . . . FK PACKAGE SN74ALS234. . . FN PACKAGE

(TOP VIEW) 5 SHIFT IN 1 4 18 □ OR DO 1 5 17 F QO NC 6 16 NC D1 🗖 7 15 Q1 D2 | 8 14 🛛 Q2

NC-No internal connection

Status of the 'ALS234 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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8-48

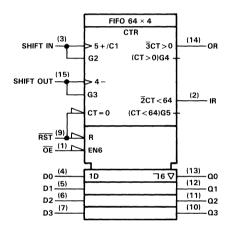
D2958, OCTOBER 1986-REVISED APRIL 1988

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input (\overline{RST}) . This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when \overline{RST} goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before \overline{RST} goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable (\overline{OE}) is high. \overline{OE} does not affect the IR and OR outputs.

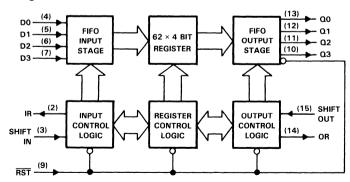
The SN54ALS234 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74ALS234 is characterized for operation from 0 °C to 70 °C.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



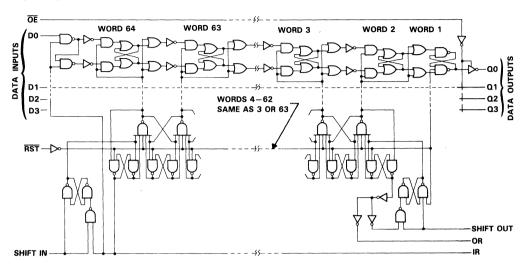
Pin numbers shown are for DW, J, and N packages.



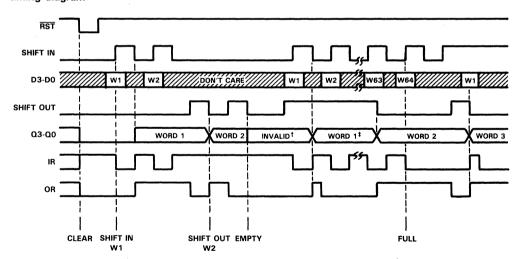
SN54ALS234, SN74ALS234 64 × 4 ASYNCHRONOUS FIRST-IN. FIRST-OUT MEMORIES

D2958, OCTOBER 1986-REVISED APRIL 1988

logic diagram (positive logic)



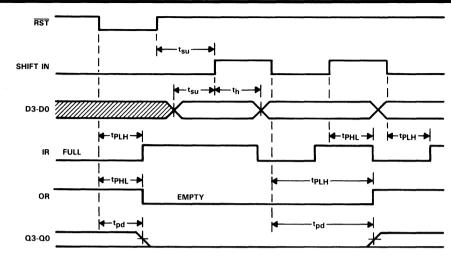
timing diagram



[†] The last data word shifted out of the FIFO remains at the output until a new word falls through or a RST pulse clears the FIFO.

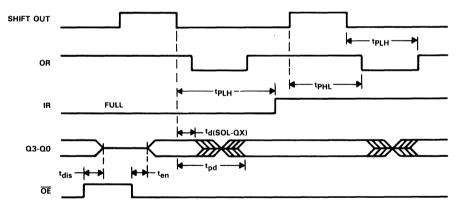
[‡] While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.

D2958, OCTOBER 1986-REVISED APRIL 1988



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS



D2958, OCTOBER 1986-REVISED APRIL 1988

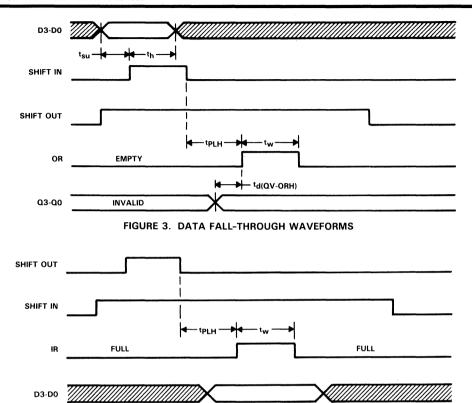


FIGURE 4. AUTOMATIC DATA-IN WAVEFORMS

D2958, OCTOBER 1986-REVISED APRIL 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

 Supply voltage, VCC
 7 V

 Input voltage
 7 V

 Voltage applied to a disabled 3-state output
 5.5 V

 Operating free-air temperature range:
 SN54ALS234
 -55 °C to 125 °C

 SN74ALS234
 0 °C to 70 °C

 Storage temperature range
 -65 °C to 150 °C

recommended operating conditions

			SN	54ALS2	234	SN	74ALS2	234	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
1	High level autout autout	Q outputs			- 1			-2.6	^
ЮН	High-level output current	IR and OR			-0.4			-0.4	mA
	1	Q outputs			12			24	
OL	Low-level output current	IR and OR			4			8	mA
f _{clock}	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t _w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		RST low	20			15			
	Cotus time before CHIET IN 1	Data	0			0			20
t _{su}	Setup time before SHIFT IN ↑	RST high (inactive)	15			15			ns
th	Hold time, data after SHIFT IN ↑		19			17			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADA	METER	TEST CON	DITIONS	SN	154ALS	234	SN	174ALS2	234	
PARA	METER	TEST CONDITIONS			TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
	a	$V_{CC} = 4.5 V$,	I _{OH} = -1 mA	2.4	3.3					
Vон	L [$V_{CC} = 4.5 V$,	I _{OH} ≈ -2.6 mA				2.4	3.2		V
	IR, OR	$V_{CC} = 4.5 V$,	$I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		
	0	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V] 4	V _{CC} = 4.5 V,	I _{OL} = 24 mA				/-	0.35	0.5	v
VOL	IR, OR	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	· •
	in, on	$V_{CC} = 4.5 V$,	IOL = 8 mA			0.4		0.35	0.5	
lozh		$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
IOZL		$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
1 ₁		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
Ιн		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IIL .		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lo‡		V _{CC} = 5.5 V,	V _O = 2.25 V	- 30		-112	-30		-112	mA
			ICCL		100	155		100	145	
Icc		$V_{CC} = 5.5 V$	Іссн		97	152		97	142	mA
			Iccz		103	158		103	148	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



D2958, OCTOBER 1986-REVISED APRIL 1988

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R: R: T,	CC = 5 L = 50 1 = 50 2 = 50 A = 25 'ALS234	pF, 0 Ω, 0 Ω, °C	SNE	V _{CC} = 4.1 C _L = 50 p R1 = 500 R2 = 500 T _A = MIN 54ALS234	F, Ω, Ω, to MAX		UNIT
	SHIFT IN		10000	35	IVIAA	25		30	····	
f _{max}	SHIFT OUT	·		35		25		30		MHz
tw [†]	IR high			15		7		8		ns
t _w ‡	OR high			19		7		8		ns
td(QV-ORH)	Q valid befor	e OR ↑		6	9	-5	12	- 5	12	ns
td(SOL-QX)	Q valid after	SHIFT OUT ↓		13		4		4		ns
t _{pd}	SHIFT IN ↓	а		600	800	350	1200	350	1000	ns
tPHL	SHIFT IN 1	IR		20	26	8	36	8	30	ns
^t PLH	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
tPLH [§]	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
^t pd	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
tPHL	SHIFT OUT 1	OR		23	27	7	39	7	33	ns
tPLH	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
^t PLH [§]	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
tPHL	RST↓	OR		22	26	10	40	10	34	ns
tPLH	RST↓	IR		17	21	6	31	6	27	ns
tPHL	RST↓	a		14	17	5	21	5	19	ns
[†] dis	ŌE ↑	a		7	13	2	16	2	15	ns
t _{en}	<u>OE</u> ↓	Q		6	12	2	15	2	13	ns

[†] The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).

[‡] The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3). § Data throughput or "fall through" times

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2958, OCTOBER 1986-REVISED APRIL 1988

TYPICAL APPLICATION INFORMATION

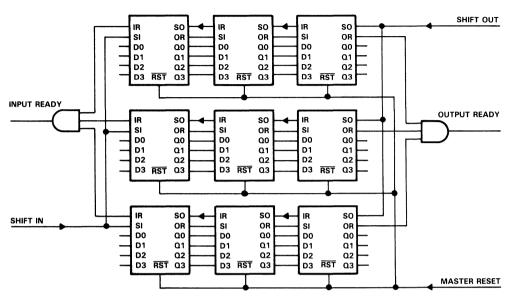


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

D2958 OCTOBER 1986

- Asynchronous Operation
- Organized as 64 Words of 5 Bits
- Data Rates From 0 to 25 MHz
- 3-State Outputs
- Dependable Texas Instruments Quality and Reliability

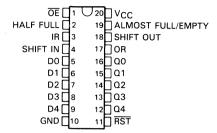
description

The SN54ALS235 and SN74ALS235 are 320-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 5 bits.

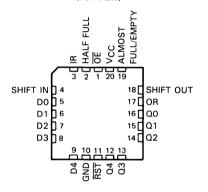
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS235 is designed to process data at rates from 0 to 25 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is emply, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or RST goes low.

SN54ALS235 . . . J PACKAGE SN74ALS235 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS235 . . . FK PACKAGE SN74ALS235. . . FN PACKAGE (TOP VIEW)



Status of the 'ALS235 FIFO memory is monitored by the Output Ready (OR), Input Ready (IR), Almost Full/Empty, and Half Full flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and stays low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full. The Almost Full/Empty flag is high when the FIFO contains eight or less words (see Figure 6). The Almost Full/Empty flag is low when the FIFO contains between nine and fifty-five words. The Half Full flag is high when the FIFO contains thirty-two or more words and is low when the FIFO contains thirty-one words or less (see Figure 7).

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. One propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low, when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output.

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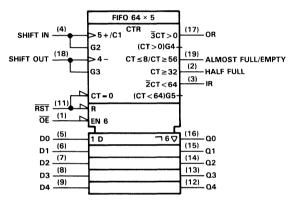
D2958, OCTOBER 1986

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input (\overline{RST}) . This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when \overline{RST} goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before \overline{RST} goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs and are at high impedance when Output Enable (\overline{OE}) is high. \overline{OE} does not affect the status flag outputs (see Figure 2).

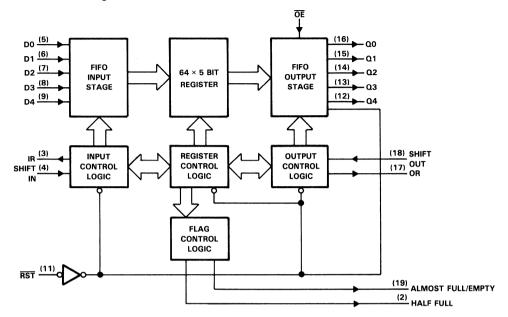
The SN54ALS235 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74ALS235 is characterized for operation from 0 °C to 70 °C.

logic symbol†



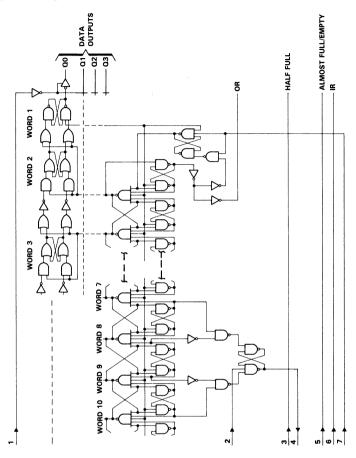
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram

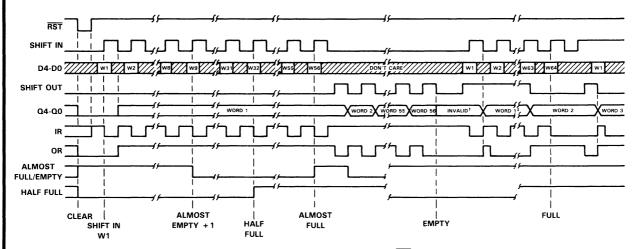


logic diagram (positive logic) CONTINUED ON NEXT PAGE WORD 31 WORD 33 WORD 32 WORD 54 WORD 55 WORD 56 NORD 57 WORD 63 NORD 64 D2-D3-Ė SHIFT OUT SHIFT IN DATA

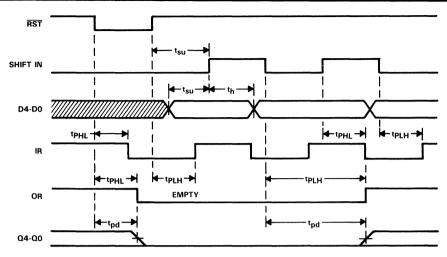
logic diagram (positive logic) (continued)





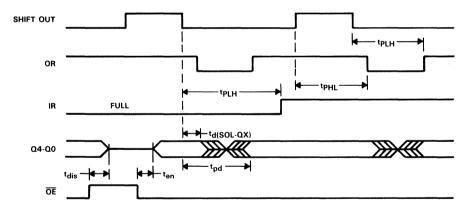


- †The last data word shifted out of the FIFO remains at the output until a new word falls through or a RST pulse clears the FIFO.
- [‡] While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until Shift Out is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS

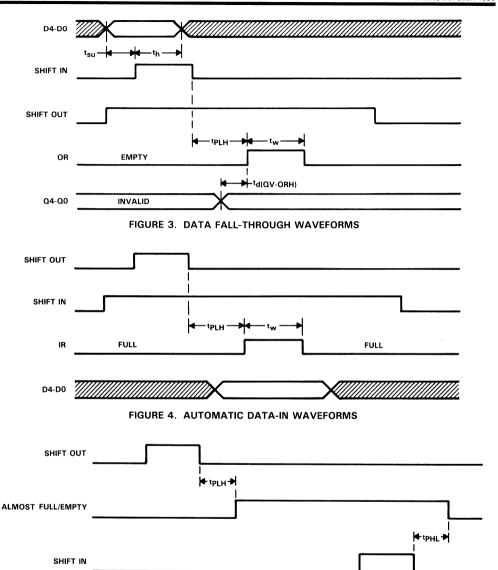
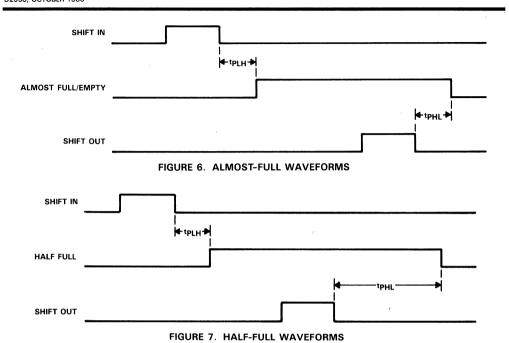




FIGURE 5. ALMOST-EMPTY WAVEFORMS



D2958, OCTOBER 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS23555°C to 125°C
SN74ALS235 0°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

			SN	I54ALS2	235	SN	74ALS2	235	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			٧
VIL	Low-level input voltage				0.8			0.8	V
1	High lavel and a second	Q outputs			- 1			-2.6	mA
ЮН	High-level output current	Flags			-0.4			-0.4	mA
1	1 1 1 1 1	Q outputs			12			24	mA
IOL	Low-level output current	Flags			4			8	mA
fclock	Clock frequency	SHIFT IN or SHIFT OUT	0		20	0		25	MHz
tw	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		RST low	20			15			
_	Catura time before CUIET IN t	Data	0			0			
t _{su}	Setup time before SHIFT IN ↑	RST high (inactive)	15			15			ns
th	Hold time, data after SHIFT IN ↑		19			17			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAR	AMETER	TECT CO	MOITIONE	SI	154ALS	235	SN	74ALS	235	UNIT
FARA	AIVIETEN	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.2			-1.2	V
	a	$V_{CC} = 4.5 V,$	I _{OH} = -1 mA	2.4	3.3					
∨он	<u> </u>	$V_{CC} = 4.5 V$,	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		V
	Flags	$V_{CC} = 4.5 V,$	$I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		
	Ω	$V_{CC} = 4.5 V,$	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
\/a.	u l	$V_{CC} = 4.5 V,$	I _{OL} = 24 mA					0.35	0.5	v
VOL	Flags	$V_{CC} = 4.5 V$,	IOL = 4 mA		0.25	0.4		0.25	0.4	· ·
	riags	$V_{CC} = 4.5 V,$	I _{OL} = 8 mA			0.4		0.35	0.5	
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozl		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20			- 20	μΑ
lj.		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
۱н		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IJL		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
10 [‡]		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 30		- 112	- 30		-112	mA
			ICCL		112	175		112	165	
Icc		$V_{CC} = 5.5 V$	ГССН		105	170		105	160	mA
			Iccz		115	180		115	170	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \, ^{\circ}\text{C}$.

[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



D2958, OCTOBER 1986

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R R T	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $R2 = 500 \Omega,$ $R4 = 500 \Omega,$ $R4 = 500 \Omega,$ $R5 = 500 \Omega,$ $R5 = 500 \Omega,$ $R6 = 500 \Omega,$ $R6 = 500 \Omega,$ $R7 = 25 \Omega$ $R7 = 100 \Omega$ $R8 = 100 \Omega$ $R9 = 100 \Omega$ R					UNIT	
	SHIFT IN			30		20		25		
fmax	SHIFT OUT			30		20		25		MHz
tw [†]	IR high			15		7		8		ns
t _w ‡	OR high			19		7		8		ns
td(QV-ORH)	Q valid befo	re OR 1		6	9	- 5	12	-5	12	ns
td(SOL-QX)	Q valid after	SHIFT OUT ↓		13		4		4		ns
t _{pd}	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
tPHL	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
tPLH	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
t _{PLH} §	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
tPHL	SHIFT IN ↓	ALMOST F/E		550	700	290	1050	290	880	ns
tPLH	SHIFT IN ↓	ALMOST F/E		85	115	40	170	40	150	ns
^t PLH	SHIFT IN ↓	HALF FULL		340	410	180	590	180	510	ns
t _{pd}	SHIFT OUT ↓	а		13	17	4	24	4	22	ns
tPHL	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
tPLH	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
t _{PLH} §	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
tPHL	SHIFT OUT ↓	ALMOST F/E		550	700	290	1050	290	880	ns
tPLH	SHIFT OUT ↓	ALMOST F/E		85	115	35	170	35	150	ns
tPHL	SHIFT OUT ↓	HALF FULL		340	410	170	590	170	510	ns
tpHL	RST↓	OR		22	26	10	40	10	34	ns
tpLH	RST↑	IR		12	18	5	24	5	22	ns
tPHL	RST↓	IR		12	18	5	24	5	22	ns
tpHL	RST↓	a		14	17	5	21	5	19	ns
t _{dis}	ŌĒ ↑	a		7	13	2	16	2	15	ns
t _{en}	ŌE ↓	Q		6	12	2	15	2	13	ns

[†] The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).

[‡]The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).

[§]Data throughput or "fall through" times

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION INFORMATION

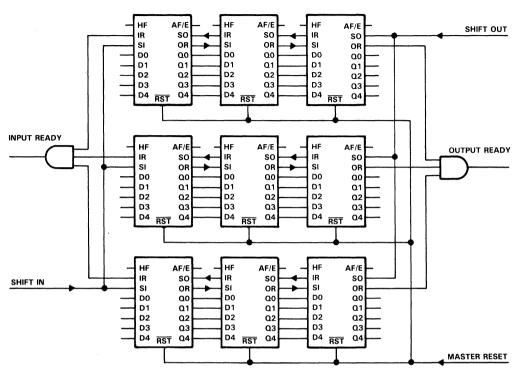


FIGURE 8. 192-WORD BY 15-BIT EXPANSION

D2958, OCTOBER 1986-REVISED APRIL 1988

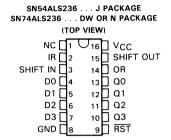
- Asynchronous Operation
- Organized as 64 Words of 4 Bits
- Data Rates From 0 to 30 MHz
- Pin-Compatible With MMI67401B With Higher Speed
- Dependable Texas Instruments Quality and Reliability

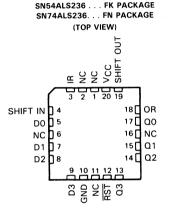
description

The SN54ALS236 and SN74ALS236 are 256-bit memories utilizing Advanced Low-Power Schottky IMPACT™ Technology. They feature high speed with fast fall-through times and are organized as 64 words by 4 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The 'ALS236 is designed to process data at rates from 0 to 30 megahertz in a bit-parallel format, word by word.

Data is written into memory on the rising edge of the Shift In input. When Shift In goes low, the first data word ripples through to the output (see Figure 1). As the FIFO fills up, the data words stack up in the order they were written. When the FIFO is full, additional Shift In pulses have no effect. Data is shifted out of memory on the falling edge of the Shift Out input (see Figure 2). When the FIFO is empty, additional Shift Out pulses have no effect. The last data word remains at the outputs until a new word falls through or $\overline{\text{RST}}$ goes low





NC-No internal connection.

Status of the 'ALS236 FIFO memory is monitored by the Output Ready (OR) and Input Ready (IR) flags. When the OR flag is high, valid data is available at the outputs. The OR flag is low when Shift Out is high and will stay low when the FIFO is empty. The IR status flag is high when the inputs are ready to receive more data. The IR flag is low when Shift In is high and stays low when the FIFO is full.

When the FIFO is empty, input data is shifted to the output automatically when Shift In goes low. If Shift Out is held high during this time, the OR flag pulses high indicating valid data at the outputs (see Figure 3).

When the FIFO is full, data can be shifted in automatically by holding Shift In high and taking Shift Out low. A propagation delay after Shift Out goes low, IR will go high. If Shift In is still high when IR goes high, data at the inputs are automatically shifted in. Since IR is normally low when the FIFO is full and Shift In is high, only a high-level pulse is seen on the IR output (see Figure 4).

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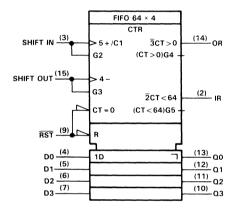
D2958, OCTOBER 1986-REVISED APRIL 1988

description (continued)

The FIFO must be reset after power up with a low-level pulse on the Master Reset input (\overline{RST}) . This sets Input Ready (IR) high and Output Ready (OR) low signifying that the FIFO is empty. Resetting the FIFO sets the outputs to a low logic level (see Figure 1). If Shift In is high when \overline{RST} goes high, the input data is shifted in and IR goes low and remains low until Shift In goes low. If Shift In goes low before \overline{RST} goes high, the input data will not be shifted in and IR goes high. Data outputs are noninverting with respect to the data inputs.

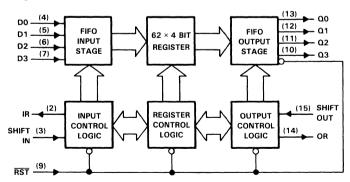
The SN54ALS236 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74ALS236 is characterized for operation from 0 °C to 70 °C.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

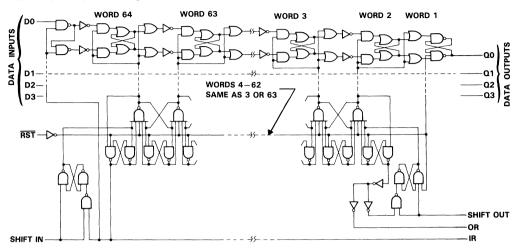
functional block diagram



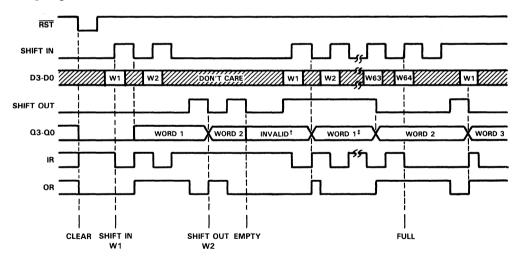
Pin numbers shown are for DW, J, and N packages.

D2958, OCTOBER 1986-REVISED APRIL 1988

logic diagram (positive logic)

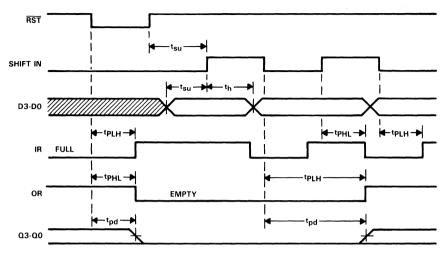


timing diagram



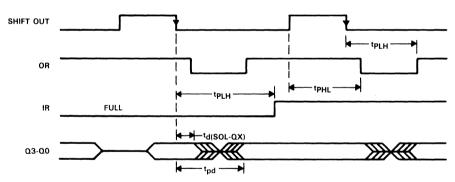
[†] The last data word shifted out of the FIFO remains at the output until a new word falls through or a RST pulse clears the FIFO.

[‡] While the output data is considered valid only when the OR flag is high, the stored data remains at the output. Any additional words written into the FIFO will stack up behind the first word and will not appear at the output until SHIFT OUT is taken low.



NOTE: SHIFT OUT is low

FIGURE 1. MASTER-RESET AND DATA-IN WAVEFORMS



NOTE: SHIFT IN is low

FIGURE 2. DATA-OUT WAVEFORMS

D2958, OCTOBER 1986-REVISED APRIL 1988

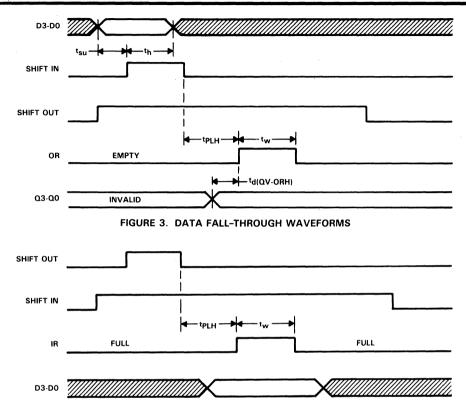


FIGURE 4. AUTOMATIC DATA-IN WAVEFORMS

D2958, OCTOBER 1986-REVISED APRIL 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage
Operating free-air temperature range: SN54ALS23655°C to 125°C
SN74ALS236 0°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

			SN	54ALS	236	SN	74ALS2	236	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	ONL
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	٧
1	High level systems systems	Q outputs			- 1			-2.6	mA
Іон	High-level output current	IR and OR			-0.4			-0.4	mA
		Q outputs			12			24	
lOL	Low-level output current	IR and OR			4			8	mA
fclock	Clock frequency	SHIFT IN or SHIFT OUT	0		25	0		30	MHz
t _w	Pulse duration	SHIFT IN or SHIFT OUT high or low	17			15			ns
		RST low	20			15			
	Control bodon CHIET IN 1	Data	0			0			
t _{su}	Setup time before SHIFT IN 1	RST high (inactive)	15			15			ns
th	Hold time, data after SHIFT IN ↑		19			17			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DAD	AMETER	TEST CO	MOITIONS	SI	154ALS	236	SN	174ALS2	236	UNIT
PAR	AMETER	TEST CONDITIONS			TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
V _{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			- 1.2			- 1.2	V
	Q	$V_{CC} = 4.5 V,$	$I_{OH} = -1 \text{ mA}$	2.4	3.3					
Voн	u	$V_{CC} = 4.5 V,$	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		V
	IR, OR	$V_{CC} = 4.5 V$,	$I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		
	Q	$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
V		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24 mA					0.35	0.5	v
VOL	IR, OR	$V_{CC} = 4.5 V$,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	·
		$V_{CC} = 4.5 V$,	IOL = 8 mA			0.4		0.35	0.5	
łį		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
ΉΗ		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
11L		$V_{CC} = 5.5 V$,	V _I = 0.4 V			-0.1			-0.1	mA
lo [‡]		$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 30		-112	- 30		-112	mA
		V _{CC} = 5.5 V	ICCL		100	155		100	145	A
lcc	cc	vCC = 2.2 v	Іссн		97	152		97	142	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.



[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

D2958, OCTOBER 1986-REVISED APRIL 1988

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$ 'ALS236 MIN TYP MAX		V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX SN54ALS236 SN74ALS236 MIN MAX MIN N				UNIT	
	SHIFT IN			35		25	- IIII-AA	30	111777	
^f max	SHIFT OUT			35		25		30		MHz
tw [†]	IR high			15		7		8		ns
t _w ‡	OR high			19		7		8		ns
td(QV-ORH)	Q valid before	OR ↑		6	9	~5	12	-5	12	ns
td(SOL-QX)	Q valid after SI	HIFT OUT ↓		13		4		4		ns
^t pd	SHIFT IN ↓	Q		600	800	350	1200	350	1000	ns
^t PHL	SHIFT IN ↑	IR		20	26	8	36	8	30	ns
^t PLH	SHIFT IN ↓	IR		16	21	6	28	6	25	ns
^t PLH [§]	SHIFT IN ↓	OR		600	800	350	1200	350	1000	ns
t _{pd}	SHIFT OUT ↓	Q		13	17	4	24	4	22	ns
tPHL	SHIFT OUT ↑	OR		23	27	7	39	7	33	ns
^t PLH	SHIFT OUT ↓	OR		20	24	6	33	6	30	ns
tPLH [§]	SHIFT OUT ↓	IR		600	800	350	1200	350	1000	ns
^t PHL	RST ↓	OR		22	26	10	40	10	34	ns
^t PLH	RST↓	IR		17	21	6	31	6	27	ns
^t PHL	RST↓	Q		14	17	5	21	5	19	ns

[†] The IR output pulse occurs when the FIFO is full, Shift In is high, and Shift Out is pulsed (see Figure 4).

[‡]The OR output pulse occurs when the FIFO is empty, Shift Out is high, and Shift In is pulsed (see Figure 3).

[§] Data Throughput or "fall through" times

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D2958, OCTOBER 1986-REVISED APRIL 1988

TYPICAL APPLICATION INFORMATION

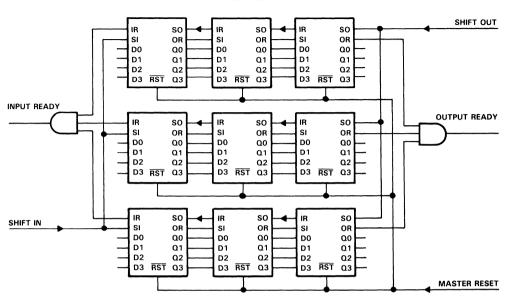


FIGURE 5. 192-WORD BY 12-BIT EXPANSION

SN74ALS2232A 64×8 ASYNCHRONOUS FIRST-IN. FIRST-OUT MEMORY

D3091, FEBRUARY 1988-REVISED MARCH 1990

- Independent Asynchronous Inputs and Outputs
- 64 Words by 8 Bits Each
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 20 ns Typ
- 3-State Outputs

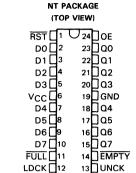
description

This 512-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 8 bits.

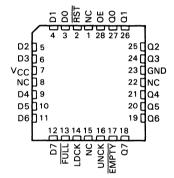
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output will be low when the memory is full, and high when the memory is not full. The EMPTY output will be low when the memory is empty, and high when it is not empty.





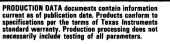


NC-No internal connection

A low level on the reset input (RST) resets the internal stack control pointers and also sets EMPTY low and FULL high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a RST pulse or from an empty condition, causes EMPTY to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not effect either the FULL or EMPTY output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2232A is characterized for operation from 0°C to 70°C.

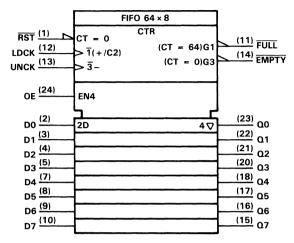
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D3091, FEBRUARY 1988-REVISED MARCH 1990

logic symbol†

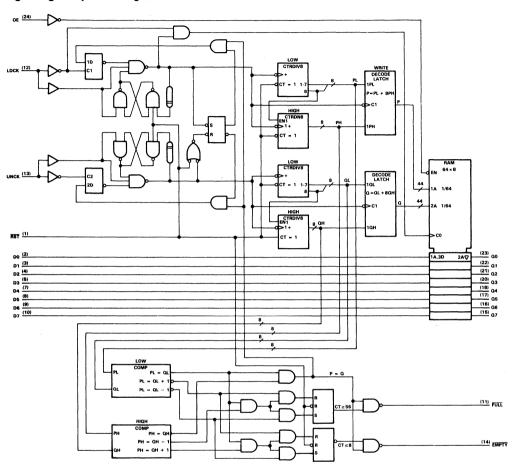


[†]This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

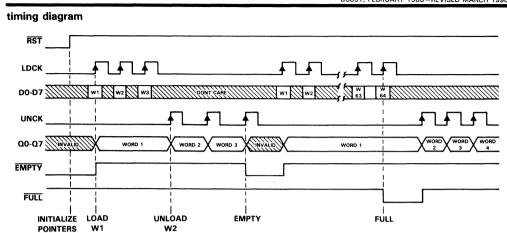
Pin numbers shown are for the NT package.

D3091, FEBRUARY 1988-REVISED MARCH 1990

logic diagram (positive logic)



Pin numbers shown are for the NT package.



absolute maximum ratings over operating free-air temperature range

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
lau	High lovel output ourrent	Q outputs			-2.6	mA
ЮН	High-level output current	FULL, EMPTY			-0.4	'''A
1	Law law law a control and a control	Q outputs			24	mA
IOL	Low-level output current	FULL, EMPTY			8	"
fclock	Clock frequency	LDCK, UNCK	0		40	MHz
		RST low	25			
	Pulse duration	LDCK low	13			
t_W		LDCK high	12			ns
		UNCK low	13]
		UNCK high	12			
t _{su1}	Setup time, data before LDCK1					ns
t _{su2}	Setup time, RST high (inactive) before LDCK1					ns
th	Hold time, data after LDCK†					ns
TA	Operating free-air temperature				70	°C

SN74ALS2232A 64×8 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3091, FEBRUARY 1988-REVISED MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER		TEST CONDITIONS	MIN T	ΥP [†]	MAX	UNIT
V _{IK}		$V_{CC} = 4.5 V,$	I _I = -18 mA			1.2	٧
	FULL, EMPTY	V _{CC} = MIN TO MAX,	I _{OH} = 0.4 mA	V _{CC} -2			٧
Vон	Q outputs	$V_{CC} = 4.5 \text{ V},$	I _{OH} = -2.6 mA	2.4	3.2		V
	Q outputs	I _{OL} = 12 mA		0.25	0.4		
VOL	Q outputs	V _{CC} =4.5 V	I _{OL} = 24 mA		0.35	0.5	v
\ VOL	FULL, EMPTY	VCC =4.5 V	i _{OL} = 4 mA	(0.25	0.4	•
	FOLL, EIVIFTT		I _{OL} = 8 mA		0.35	0.5	
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20	μΑ
lozL		$V_{CC} = 5.5 V,$	$V_0 = 0.4 V$			- 20	μΑ
lį ,		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1	mA
Ιн		$V_{CC} = 5.5 V,$	V ₁ = 2.7 V			20	μΑ
1	CLKS	V _{CC} = 5.5 V,	V _{IN} = 0.4 V			-0.2	mA
ll.	Others	VCC = 5.5 V,	VIN = 0.4 V			-0.1	
lo‡	Q outputs	V _{CC} = 5.5 V,	V _O = 2.25 V	- 20		- 130	mA
L10 .	FULL, EMPTY	VCC = 5.5 V,	VU = 2.25 V	- 20		-112	
Icc		V _{CC} = 5.5 V			175	270	mA

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

switching characteristics (see Note 1)

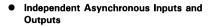
PARAMETER	FROM (INPUT)	то (ОИТРИТ)	TO $C_L = 50 \text{ pF},$ $C_L = 50 \text{ pI}$ (OUTPUT) $R1 = 500 \Omega,$ $R1 = 500 \Omega$ $R2 = 500 \Omega,$ $R2 = 500 \Omega$ $T_A = 25 ^{\circ}C$ $T_A = 0 ^{\circ}C$ to $T_A = 0 ^{\circ}C$		$C_L = 50 \text{ pF}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = 25^{\circ}$ C $T_A = 0^{\circ}$ C to 70		UNIT
fmax	LDCK				40		MHz
'max	UNCK				40		1411 12
^t pd	LDCK†	Any Q	18	26		30	ns
^t pd	UNCK↑	Any Q	18	24		27	ns
^t PLH	LDCK↑	EMPTY	12	16		18	ns
tPHL	UNCK†	EMPTY	12	17		20	ns
^t PHL	RST↓	EMPTY	12	17		20	ns
^t PHL	LDCK†	FULL	16	21		22	ns
tPLH	UNCK↑	FULL	10	15		18	ns
^t PLH	RST↓	FULL	13	19		23	ns
t _{en}	OE↑	Q	11	15		17	ns
^t dis	OE↑	Q	11	17		19	ns

Note 1: Load circuit and voltage waveforms are shown in Section 1.

[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN74ALS2233A 64×9 ASYNCHRONOUS FIRST-IN. FIRST-OUT MEMORY

D3092, FEBRUARY 1988-REVISED MARCH 1990



- 64 Words By 9 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 20 ns Typical
- 3-State Outputs

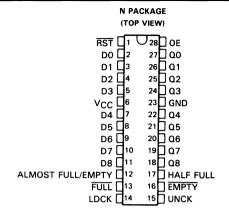
description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT—X™ technology and features high speed and fast fall-through times. It is organized as 64 words by 9 bits.

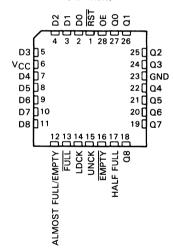
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The function is used as a buffer to couple two buses operating at different clock rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition of the load clock input (LDCK) and is read out on a low-to-high transition of the unload clock input (UNCK). The memory is full when the number of words clocked in exceeds by 64 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the FULL, EMPTY, ALMOST FULL/EMPTY, and HALF FULL output flags. The FULL output will be low when the memory is full and high when the memory is not full. The EMPTY output will be low when the memory is empty and high when it is not empty. The ALMOST FULL/EMPTY flag is high when the FIFO contains eight or less words or fifty-six or more words. The ALMOST FULL/EMPTY flag is low when the FIFO contains between nine and fifty-five words. The HALF FULL flag is high when the FIFO contains thirty-two or more words, and is low when the FIFO contains thirty-two words or less.



FN PACKAGE (TOP VIEW)



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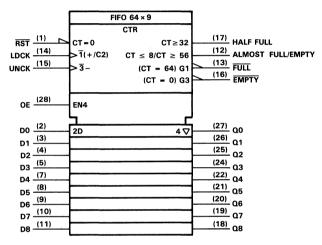
D3092, FEBRUARY 1988-REVISED MARCH 1990

description (continued)

A low level on the reset input (\overline{RST}) resets the internal stack control pointers and also sets EMPTY low and \overline{FULL} high. The outputs are not reset to any specific logic levels. The first low-to-high transition on LDCK, either after a \overline{RST} pulse or from an empty condition, causes \overline{EMPTY} to go high and the data to appear on the Q outputs. The first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at a high-impedance state when the output-enable input (OE) is low. The OE input does not affect either the \overline{FULL} or \overline{EMPTY} output flags. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

The SN74ALS2233A is characterized for operation from 0°C to 70°C.

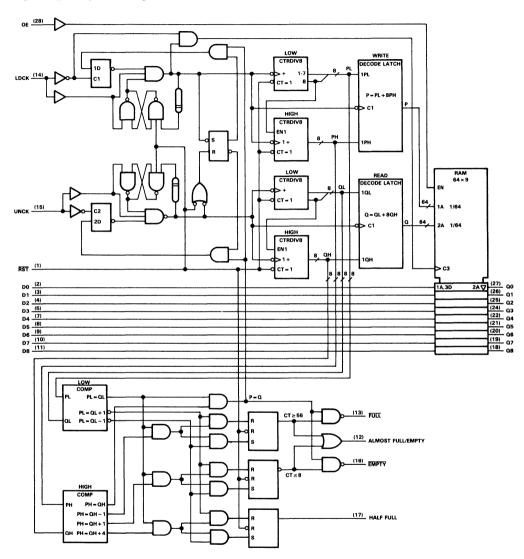
logic symbol†

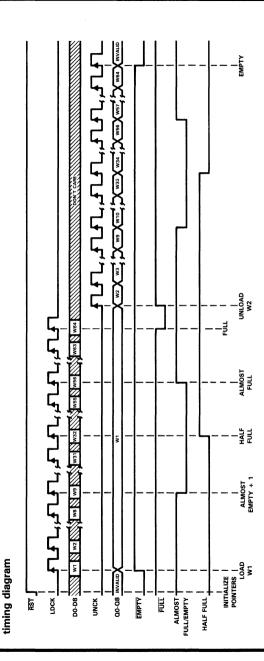


[†]This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for the N package.

logic diagram (positive logic)





64 × 9 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3092, FEBRUARY 1988-REVISED MARCH 1990

absolute maximum ratings over operating free-air temperature range

Supply voltage, VCC	. 7 V
Input voltage	. 7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range	70°C
Storage temperature range65°C to 1	50°C

recommended operating conditions

			N	MIN	NOM	MAX	UNIT
Vcc	Supply voltage			4.5	5	5.5	V
VIH	High-level input voltage	High-level input voltage					V
VIL	Low-level input voltage					0.8	V
lou	High lovel output outrant	Q outputs				-2.6	mA
ІОН	High-level output current	Flag outputs				-0.4	mA
lo.	Low-level output current	Q outputs				24	mA
IOL	Low-level output current	Flag outputs				8	mA
fclock	Clock frequency	LDCK, UNCK		0		40	MHz
		RST low		25			
	Pusle duration	LDCK low		13			
$t_{\mathbf{W}}$		LDCK high		12			ns
		UNCK low		13			
		UNCK high		12			
t _{su1}	Setup time, data before LDCK1			5			ns
t _{su2}	Setup time, RST high (inactive) before LDCK1			5			ns
th	Hold time, data after LDCK1			5			ns
TA	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDTIONS	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA			1.2	V
Vон	Flag outputs	V _{CC} = MIN TO MAX,	I _{OH} = 0.4 mA	V _{CC} -2	2		V
	Q outputs	$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA	2.4	3.2		· ·
	O Outmute		I _{OL} = 12 mA		0.25	0.4	
	Q Outputs	O Outputs VCC = 4.5 V	I _{OL} = 24 mA		0.35	0.5	V
V_{OL}	Flor outputo		I _{OL} = 4 mA		0.25	0.4	· ·
	riag outputs		I _{OL} = 8 mA		0.35	0.5	
lozh		$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20	μΑ
lozL		$V_{CC} = 5.5 \text{ V},$	V _O = 0.4 V			- 20	μΑ
I _I		$V_{CC} = 5.5 V,$	V _I = 7 V			0.1	mA
ΊΗ		$V_{CC} = 5.5 V,$	$V_{ } = 2.7 V$			20	μΑ
L	CLKs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2	mA
ηL	Others	J vCC = 5.5 v,	V = 0.4 V			-0.1	IIIA
lo‡	Q outputs	V _{CC} = 5.5 V,	V _O = 2.25 V	- 20		-130	mA
	Flag outputs] vcc = 5.5 v,		- 20		-112	IIIA
lcc		V _{CC} = 5.5 V			175	290	mA



[†] All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN74ALS2233A 64×9 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

D3092, FEBRUARY 1988-REVISED MARCH 1990

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	$\begin{array}{c} \text{VCC} = 5 \text{ V,} & \text{VCC} = 4.5 \text{ V to } 1.0 \text{ V} \\ \text{CL} = 50 \text{ pF,} & \text{CL} = 50 \text{ pF,} \\ \text{R1} = 500 \Omega, & \text{R1} = 500 \Omega, \\ \text{R2} = 500 \Omega, & \text{R2} = 500 \Omega, \\ \text{TA} = 25 \text{ °C} & \text{TA} = 0 \text{ °C to } 70 \text{ V} \\ \hline \text{MiN} & \text{TYP} & \text{MAX} & \text{MiN} & \text{MAX} \end{array}$			$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$		iO pF, iOO Ω, iOO Ω,	UNIT
	LDCK					40		MHz
fmax	UNCK					40		IVITIZ
^t pd	LDCK†	Any Q		18	26		30	ns
^t pd	UNCK†	Any Q		18	24		27	ns
tPLH	LDCK†	EMPTY		12	16		18	ns
tPHL	UNCK†	EMPTY		12	17		20	ns
tPHL	RST↓	EMPTY		12	17		20	ns
^t PHL	LDCK†	FULL		16	21		22	ns
^t PLH	UNCK†	FULL		10	15		18	ns
tPLH	RST↓	FULL		13	19		23	ns
^t PLH	LDCK†	ALMOST		22	27		30	ns
^t PHL	LDCKI	FULL/EMPTY		19	25		28	115
^t PLH	UNCK†	ALMOST		22	27		30	ns
^t PHL	UNCK	FULL/EMPTY		17	23		26	110
^t PLH	RST↓	ALMOST FULL/EMPTY		12	16		18	
^t PLH	LDCK†	HALF FULL		22	27		30	ns
^t PHL	RST↓	HALF FULL		28	32		35	ns
tPHL	UNCK↑	HALF FULL		16	22		25	ns
^t en	OE↑	Q		11	15		17	ns
^t dis	OE↓	α		11	17		19	ns

Note 1: Load circuits and voltage waveforms are shown in Section 1.

- Independent Asychronous Inputs and Outputs
- Bidirectional
- 32 Words by 9 Bits Each
- Programmable Depth
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 22 ns Typ
- 3-State Outputs

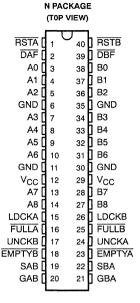
description

This 576-bit memory uses Advanced Low-Power Schottky IMPACT-X™ technology and features high speed and fast fall-through times. It consists of two FIFOs organized as 32 words by 9 bits each.

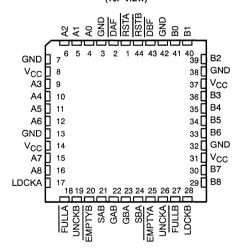
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

The 'ALS2238 consists of bus transceiver circuits, two 32 X 9 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enables GAB and GBA are provided to control the transceiver functions. The SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low level selects real-time data and a high selects stored data. Eight fundamental bus-management functions can be performed as shown on the operating modes page.

Data on the A or B data bus, or both, is written into the FIFOs on a low-to-high transition at the load clock input (LDCKA or LDCKB) and is read out on a low-to-high transition at the unload clock input (LNCKA or UNCKB). The memory is full when the number of words clocked in exceeds, by the defined depth, the number of words clocked out.



FN PACKAGE (TOP VIEW)



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SN74ALS2238 32 × 9 × 2 ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY

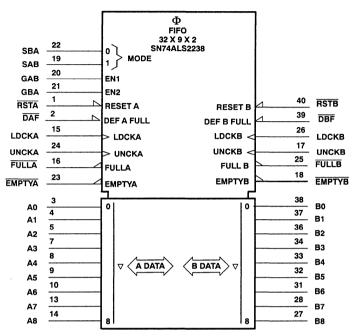
When the memory is full. LDCK signals have no effect on the data residing in memory. When the memory is empty. UNCK signals have no effect.

Status of the FIFO memories is monitored by the FULLA, FULLB, EMPTYA, and EMPTYB output flags. The FULLA and FULLB are definable full flags. A high-to-low transition on DAF stores the binary value of A0 through A4 into a register for use as the value of X. A high-to-low transition on DBF stores the binary value of B0 through B4 into a register for use as the value of Y. In this way, the depth of either FIFO can be defined to be one to thirty-two words deep. The value of X and Y must be defined after power-up or the stored value of X and Y will be ambiguous. The FULLA and FULLB outputs are low when their corresponding memories are full and high when the memories are not full.

The EMPTYA and EMPTYB outputs are low when their corresponding memories are empty and high when they are not empty. The status flag outputs are always active.

A low-level pulse on the RSTA or RSTB inputs resets the control pointers on FIFO A or FIFO B and also sets EMPTYA low and FULLA high or EMPTYB low and FULLB high. The outputs are not reset to any specific logic levels. With DAF at a low level, a low-level pulse on RSTA sets FIFO A to a depth of 32 minus X, where X is the value stored above. With DAF at a high level, a low level pulse on RSTA sets FIFO A to a depth of 32 words. The depth of FIFO B is set in a similar manner. The first low-to-high transition on LDCKA or LDCKB, either after a reset pulse or from an empty condition, will cause EMPTYA or EMPTYB to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Cascading is easily accomplished in the word-width direction, but is not possible in the word-depth direction.

logic symbol†

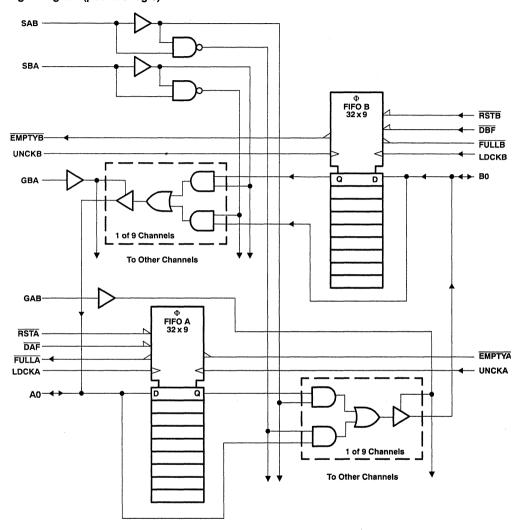


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984. Pin numbers shown are for the N package.

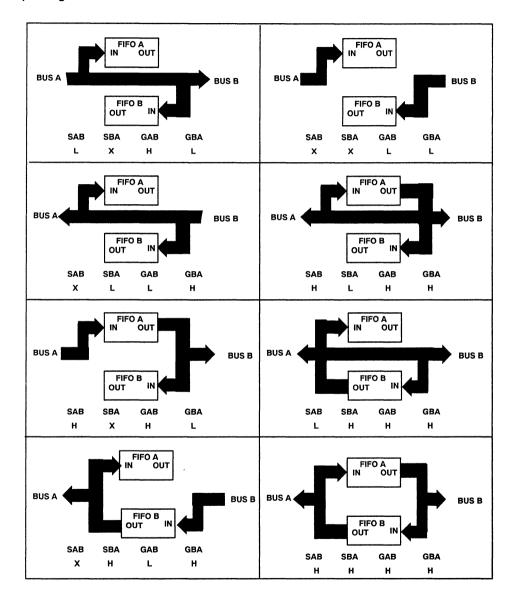


FIRST-IN, FIRST-OUT MEMORY D3501, APRIL 1990

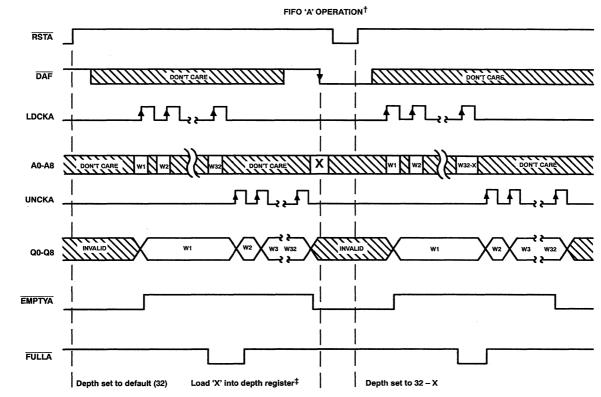
logic diagram (positive logic)



operating modes



timing diagram



[†] Operation of FIFO 'B' is the same as shown above.

^{† &#}x27;X' includes A0 through A4 only. A5 through A8 are ignored.

FUNCTION TABLES

SELECT MODE CONTROL TABLE

CON	TROL	OPER	ATION
SBA	SAB	A Bus	B Bus
L	٦	Real Time B to A Bus	Real Time A to B Bus
Н	L	FIFO B to A Bus	Real Time A to B Bus
L	Н	Real Time B to A Bus	FIFO A to B Bus
н	н	FIFO B to A Bus	FIFO A to B Bus

OUTPUT ENABLE CONTROL TABLE

CON	TROL	OPERATION OPERATION				
GBA	GAB	A Bus	B Bus			
Н	Н	A Bus Enabled	B Bus Enabled			
Н	L	A Bus Enabled	Isolation/Input to B Bus			
L	Н	Isolation/Input to A Bus	B Bus Enabled			
L	L	Isolation/Input to A Bus	Isolation/Input to B Bus			

programming procedure for depth of FIFO A[†]

PROGRAM:

- Step 1. With RSTA at a high level, take DAF from a high level to a low level. The high-to-low transition on DAF stores the binary value of A0-A4 for use as the value of 'X' in defining the depth of FIFO A.
- Step 2. With DAF held low, pulse the RSTA signal low. On the low-to-high transition of RSTA, FIFO A is set to a depth of 32 minus 'X', where X is the value of A0-A4 stored above.
- Step 3. To redefine the depth of FIFO A to 32 words, hold DAF at a high level and pulse the RSTA signal low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Voltage applied to a diabled 3-state output	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C
Maximum junction temperature	150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



[†] The programming procedures used to define the depth of FIFO B are the same as the procedure above.

$32 \times 9 \times 2$ ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY D3501, APRIL 1990

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	٧
VIH	High-level input voltage		2			٧
VIL	Low-level input voltage				8.0	٧
1		A or B Ports			15	mA
ЮН	High-level output current	Status flags			- 0.4	IIIA
,	Low-level output current	A or B Ports			24	mA
IOL	Low-level output current	Status flags			8	mA
. .	011-6	LDCKA or LDCKB	0		40	
fclock	Clock frequency	UNCKA or UNCKB	0		40	MHz
		RSTA or RSTB low	17			
	Pulse duration	LDCKA or LDCKB low	12.5			
tw		LDCKA or LDCKB high	10			ns
w		UNCKA or UNCKB low	12.5			113
		UNCKA or UNCKB high	10			
		DAF or DBF high	10			
		Data before LDCKA or LDCKB↑	7			
		Define Depth: D4-D0 before DAF or DBF↓	6			
t _{su}	Setup time	Define Depth: DAF or DBF↓ before RSTA or RSTB↑	45			ns
		Define Depth (32): DAF or DBF high before RSTA or RSTB†	32			
		LDCKA or LDCKB (inactive) before RSTA or RSTB↑	5			
		Data after LDCKA or LDCKB↑	3			
		Define Depth: D4-D0 after DAF or DBF↓	4			
th	Hold time	Define Depth: DAF or DBF low after RSTA or RSTB↑	0			ns
		Define Depth (32): DAF or DBF high after RSTA or RSTB↑	0			
		LDCKA or LDCKB (inactive) after RSTA or RSTB↑	5			
TA	Operating free-air temperat	lure	0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCKA or LDCKB and UNCKA or UNCKB clock inputs. Any excessive noise or glitching on the clock inputs (which violates the VIL, VIH, or minimum pulse duration limits) can cause a false clock or improper operation of the internal read and write pointers.

$32 \times 9 \times 2$ ASYNCHRONOUS BIDIRECTIONAL FIRST-IN, FIRST-OUT MEMORY D3501, APRIL 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CON	MIN	TYP†	MAX	UNIT	
VIK		V _{CC} = 4.5 V,	i _I = - 18 mA			- 1.2	V
	Status flags	V _{CC} = 4.5 V to 5.5 V,	IOH = - 0.4 mA	V _{CC} -2			
Vон		V _{CC} = 4.5 V,	IOH = - 2 mA	V _{CC} -2			V
*UH	A or B ports	V _{CC} = 4.5 V,	I _{OH} = – 3 mA	2.4	3.2		•
		VCC = 4.5 V to 5.5 V, IOH = - 0.4 mA VCC = 4.5 V, IOH = - 2 mA VCC = 4.5 V, IOH = - 3 mA VCC = 4.5 V, IOH = - 15 mA VCC = 4.5 V, IOH = - 15 mA VCC = 4.5 V, IOL = 12 mA VCC = 4.5 V, IOL = 24 mA VCC = 4.5 V, IOL = 4 mA VCC = 4.5 V, IOL = 8 mA VCC = 4.5 V, IOL = 8 mA VCC = 5.5 V, VI = 7 V	2				
	A or B newto	V _{CC} = 4.5 V,	I _{OL} = 12 mA		0.25	0.4	
V _{OL}	A or B ports	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	v
	Status flags	V _{CC} = 4.5 V,	I _{OL} = 4 mA		0.25	0.4	V
	Status flags	V _{CC} = 4.5 V,	IOL = 8 mA		0.35	0.4 0.5 0.4 0.5 0.1 0.2 20 40 -0.2 -0.4 -130 -100	
11	DAF, DBF, RSTA, RSTB, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA
	A or B ports	1		0.25	0.2		
IIH	DAF, DBF, RSTA, RSTB, GAB, GBA, SAB, SBA, LDCKA, LDCKB, UNCKA, UNCKB	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μА
	A or B ports [‡]	1			-1.2 2 4 3.2 2 0.25 0.4 0.35 0.5 0.25 0.4 0.35 0.5 0.1 0.2 20 40 -0.2 20 -0.4 20 -130 15 -100		
Iμ	DAF, DBF, RSTA, RSTB, GAB, GBA, SAB, SBA, LCKA, LDCKB, UNCKA, UNCKB	V _{CC} = 5.5 V,	V _I = 0.4 V			- 0.2	mA
	A or B ports‡					- 0.4	
10 [§]	A or B ports [‡]	V== EEV	V= 2.25 V	- 20		- 130	mA
103	Status flags	√CC = 5.5 V,	vO = 2.25 V	- 15		- 100	mA
ICC		V _{CC} = 5.5 V			190	350	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output ccurrent, I_{OS}.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	то (оитрит)	CL = 5 R1 = 5 R2 = 5 TA = 1	500Ω, 500Ω, VIIN to M	AX	UNIT
	LDCK		MIN 40	TYP	MAX	
fmax	UNCK		40			MHz
t _{pd}	LDCKA†, LDCKB†	B/A	7	22	33	ns
t _{pd}	UNCKA†, UNCKB†	B/A	7	20	29	ns
tPLH t	LDCKA↑, LDCKB↑	EMPTYA, EMPTYB	5	12	22	ns
tPHL the text of t	UNCKA↑, UNCKB↑	EMPTYA, EMPTYB	5	12	22	ns
t _{PHL}	RSTA↓, RSTB↓	EMPTYA, EMPTYB	5	12	22	ns
t _{PHL}	LDCKA†, LDCKB†	FULLA, FULLB	5	12	22	ns
t _{PLH}	UNCKA†, UNCKB†	FULLA, FULLB	5	12	23	ns
tLH	RSTA↓, RSTB↓	FULLA, FULLB	6	15	28	ns
t _{pd}	SAB/SBA [‡]	B/A	2	11	18	ns
t _{pd}	A/B	B/A	2	8	15	ns
t _{en}	GBA/GAB	A/B	2	6	15	ns
^t dis	GBA/GAB	A/B	1	5	12	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.



[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

General Information	
ACL LSI Products	2
ACL Widebus™ Products	3
BTL Transceiver Products	
Bus-Termination Array Products 5	5
Clock Driver Products	5
ECL/TTL Translator Products	
FIFO Products	3
Low-Impedance Line Driver Products)
Memory Driver Products	0
SCOPE™ Testability Products	1
64BCT Series Products	2
Mechanical Data	3

SN54BCT25240, SN74BCT25240 OCTAL 25-OHM LINE DRIVERS WITH 3-STATE OUTPUTS

TI0227-D3532, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

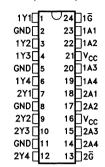
The 'BCT25240 is an octal inverting buffer/line driver. The outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω .

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the device transmits the inverted A-input data to the Y outputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

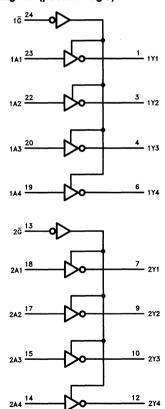
The distributed V_{CC} and GND pins of the 'BCT25240 reduce switching noise for more reliable system operation.

The SN54BCT25240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25240 is characterized for operation from 0°C to 70°C.

SN54BCT25240 ... JT PACKAGE SN74BCT25240 ... NT PACKAGE (TOP VIEW)



logic diagram (positive logic)





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SN54BCT25244, SN74BCT25244 OCTAL 25-OHM LINE DRIVERS WITH 3-STATE OUTPUTS

TI0226---D3533, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

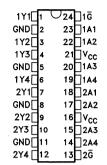
The 'BCT25244 is an octal noninverting buffer/ line driver. The outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω .

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the device transmits data from the A inputs to the Y outputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state.

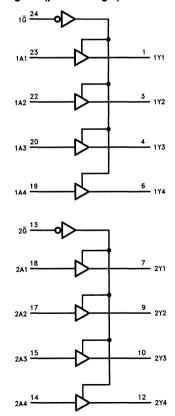
The distributed V_{CC} and GND pins of the BCT25244 reduce switching noise for more reliable system operation.

The SN54BCT25244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25244 is characterized for operation from 0°C to 70°C.

SN54BCT25244 ... JT PACKAGE SN74BCT25244 ... NT PACKAGE (TOP VIEW)



logic diagram (positive logic)





TI0220--- D3514, MAY 1990

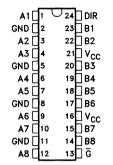
- State-of-the-Art BICMOS Design Significantly Reduces ICCZ
- Designed to Facilitate Incident Wave Switching for Line Impedances of 25 Ω or Greater
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- ESD Protection Exceeds 2000 V per Mil-STD-883C. Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

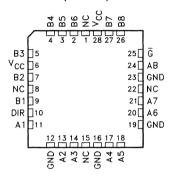
These 25 Ω octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \overline{G} can be used to disable the device so that the buses are effectively isolated.

These transceivers are capable of sinking 188 mA of I_{OL} current (A port), which facilitates switching 25 Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

SN54BCT25245 ... JT PACKAGE SN74BCT25245 ... DW or NT PACKAGE (TOP VIEW)



SN54BCT25245 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

The SN54BCT25245 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT25245 is characterized for operation from 0°C to 70°C.

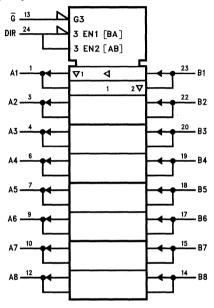
SN54BCT25245, SN74BCT25245 25-OHM OCTAL BUS TRANSCEIVERS

D3514, MAY 1990-TI0220

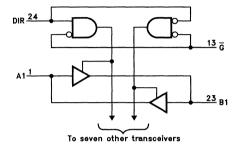
FUNCTION TABLE

ENABLE	INPUTS	OPERATION
Ğ	DIR	'BCT25245
L	L	B Data to A Bus
L	н	A Data to B Bus
н	х	Isolation

logic symbol†



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT25245, SN74BCT25245 25-OHM OCTAL BUS TRANSCEIVERS

TI0220-D3514, MAY 1990

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range (see Note 1): Control Inputs	0.5 V to 7 V
I/O ports	-0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state (B port)	-0.5 V to VCC
Input clamp current	
Current into any output in the low state: SN54BCT25245 (A port)	250 mA
(B port)	40 mA
SN74BCT25245 (A port)	376 mA
(B port)	
Operating free-air temperature range: SN54BCT25245	
SN74BCT25245	
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			′54	BCT252	45	'74BCT25245				
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage		2		120	2			٧	
VIL	Low-level input voltage				8.0			0.8	V	
١ĸ	Input clamp current			46	-18			18	mA	
1	I Balancia and a second	A1-A8		15	-53			-80		
ЮН	High-level output current	B1-B8		1900	-3			-3	mA	
		A1-A8	_0		125			188		
lOL	Low-level output current B1-B8		18		20			24	⊢ mA	
TA	Operating free-air temperature		-55		125	0		70	°C	

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN54BCT25245, SN74BCT25245 25-OHM OCTAL BUS TRANSCEIVERS

D3514, MAY 1990-TI0220

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'54	BCT252	45	'74	BCT252	45	UNIT
		TEST CONDITIONS		TYP†	MAX	MIN	TYP	MAX	UNII
VIK		V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	٧
		V _{CC} = 4.5 V, I _{OH} = -53 mA	2						
V	Any A	$V_{CC} = 4.5 \text{ V}, I_{OH} = -80 \text{ mA}$				2			v
VOH		$V_{CC} = 4.75 \text{V}, I_{OH} = -3 \text{mA}$				2.7			V
	Any B	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.4	3.3		2.4	3.3		
		V _{CC} = 4.5 V, I _{OL} = 94 mA		0.38	0.55	,	0.42	0.55	
	Any A	V _{CC} = 4.5 V, I _{OL} = 125 mA			0.8				
VOL	l	V _{CC} = 4.5 V, I _{OL} = 188 mA						0.7	٧
	AB	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.3	0.5				
	Any B	VCC = 4.5 V, IOL = 24 mA			7		0.35	0.5	
	A and B	V _{CC} = 5.5 V, V _I = 5.5 V		W.	0.25			0.25	4
l)	DIR and G	V _{CC} = 5.5 V, V _I = 5.5 V		a c	0.1			0.1	1 mA
1+	A and B	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$		<i>j</i> ~	70			70	
lH‡	DIR and G	V _{CC} = 5.5 V, V _I = 2.7 V		.5	20			20	μΑ
In t	A and B	$V_{CC} = 5.5 \text{ V}, V_I = 0.5 \text{ V}$		9	-0.6			-0.6	4
կլ‡	DIR and G	V _{CC} = 5.5 V, V _I = 0.5 V		2	-0.6			-0.6	mA
los	B port only¶	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$	-60		-150	-60		- 150	mA
lasu	A to B	Van - FFV		36	46		36	46	4
ICCH	B to A	V _{CC} = 5.5 V		63	77		63	77	mA
	A to B	V 55V		48	60		48	60	
ICCL	B to A	V _{CC} = 5.5 V		95	115		95	115	mA
Iccz		V _{CC} = 5.5 V		12	16		12	16	mA
Cin	G and DIR	$V_{CC} = 5.5 \text{ V}, V_1 = 2.5 \text{ V or } 0.5 \text{ V}$		8			8		pF
<u></u>	A port	V 55V V - 05V05V		18			18		
Cio	B port	V _{CC} = 5.5 V, V _I = 2.5 V or 0.5 V		8			8		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

¹ Testing for this parameter on the A port is not recommended.

TI0220-D3514, MAY 1990

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$		T,	C _L = R1 = R2 =	500 Ω,	(†	UNIT	
}			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Б	1.2	3.3	5.1	1.2	5.8	1.2	5.7	
tPHL		В	1.9	4.3	6.7	1.9	7.6	1.9	7.2	ns
tPLH	В	^	1.2	3.3	4.8	1.2	5.7	1.2	5.5	ns
t _{PHL}		A	2.1	4	5.6	2.1	6.4	2.1	6.2	113
tPZH	G		3.7	6.3	8.4	3.7	10.1	3.7	9.6	
tPZL	G	A	4.5	7.4	9.2	4.5	₃ 11.1	4.5	10.3	ns
tPHZ	G	A	1.8	3.7	5.5	1.8	6.4	1.8	6.2	
tPLZ	G	^	3.3	5.1	7.2	3.3	9.6	3.3	8.3	ns
tPZH	Ğ	В	3.4	5.7	7.9	3.4	9.2	3.4	8.9	
tPZL	G	В	4.3	6.6	8.7	4.3	10.1	4.3	9.7	ns
t _{PHZ}	G	В	2.7	4.5	6.3	2.7	7.2	2.7	6.9	
t _{PLZ}	G	B	1.7	4.5	6.8	1.7	8.3	1.7	7.5	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

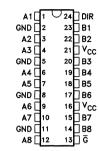
TI0283-D3601, JULY 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- The A Port Features Open-Collector Outputs
 That Provide High IoL to Allow for Heavy
 DC Loading on Open-Collector Outputs
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Local Bus-Latch Capability
- True Logic
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs

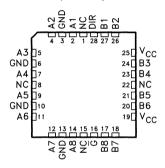
description

These noninverting 25- Ω octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{\mathbb{G}}$ can be used to disable the device so the buses are effectively isolated.

SN54BCT25641 ... JT PACKAGE SN74BCT25641 ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT25641 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

The A-port outputs of these transceivers are capable of sinking a large I_{OL}, which facilitates switching on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

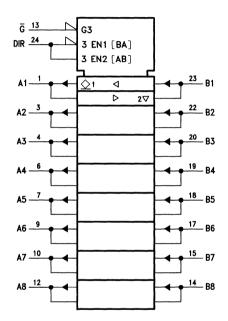
The SN54BCT25641 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT25641 is characterized for operation from 0°C to 70°C.

TI0283---D3601, JULY 1990

FUNCTION TABLE

ENABLE	INPUTS	OPERATION
Ğ	DIR	OPERATION
L	L	B DATA TO A BUS
L	Н	A DATA TO B BUS
н	X	ISOLATION

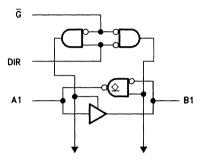
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin Numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



TO SEVEN OTHER TRANSCEIVERS

SCBS047---Ti0221---D3395, DECEMBER 1989---REVISED JUNE 1990

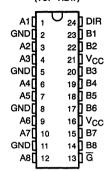
- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- The A Port Features Open-Collector Outputs Which Provide 188 mA IOL to Allow for Heavy DC Loading on Open-Collector Outputs
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs
- Eliminates Need for 3-State Overlap Protection on A Ports
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- ESD Protection Exceeds 2000 V per Mil-Standard-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

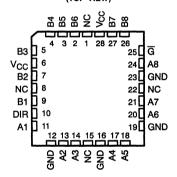
These 25 Ω octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \overline{G} can be used to disable the device so the buses are effectively isolated.

These transceivers are capable of sinking 188 mA of I_{OL} current (A port), which facilitates switching 25 Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed VCC and GND pins minimize the noise generated by the simultaneous switching of the outputs.

SN54BCT25642 ... JT PACKAGE SN74BCT25642 ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT25642 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

ENABLE	INPUTS	ODEDATION
Ğ	DIR	OPERATION
L	L	B Data to A Bus
L	Н	A Data to B Bus
н	X	Isolation

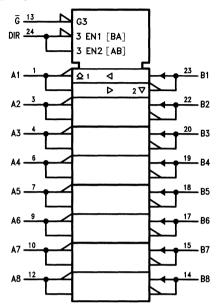
The SN54BCT25642 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT25642 is characterized for operation from 0°C to 70°C.

9-12

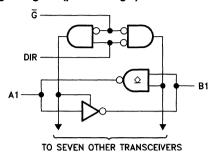
SN54BCT25642, SN74BCT25642 25-OHM OCTAL BUS TRANSCEIVERS

SCBS047-Ti0221-D3395, DECEMBER 1989-REVISED JUNE 1990

logic symbol†



logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, VCC			_ 0.5 V to 7 V
Input voltage range: Control Inputs (See	e Note 1)		-0.5 V to 7 V
I/O ports (See Not	te 1)		-0.5 V to 5.5 V
Voltage applied to any output in the dis	abled or power-off state		-0.5 V to 5.5 V
Voltage applied to any output in the hig	h state		-0.5 V to V _C C
Input clamp current	· · · · · · · · · · · · · · · · · · ·	• • • • • • • • • • • • • • • • • • • •	30 mA
Current into any output in the low state	: SN54BCT25642 (A ports)		250 mA
	(B ports)	١	40 mA
	SN74BCT25642 (A ports)		376 mA
•	(B ports)	١	48 mA
Operating free-air temperature range:	SN54BCT25642		-55°C to 125°C
	SN74BCT25642		0°C to 70°C
Storage temperature range			-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT25642, SN74BCT25642 25-OHM OCTAL BUS TRANSCEIVERS

D3395, DECEMBER 1989-REVISED JUNE 1990-TI0221-SCBS047

recommended operating conditions

		SN54BCT25642		SN74BCT25642					
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5,5	4.5	5	5.5	V
VIH	High-level input voltage		2	,	2/1	2			٧
VIL	Low-level input voltage			08	0.8			0.8	٧
Vон	VOH High-level output voltage (A1-A8)			75	5.5			5.5	٧
ΊΚ	Input clamp current		l a	2,	-18			-18	mA
ЮН	High-level output current (B1-B8)		20		-3			-3	mA
1	I am land a day to make the	A1-A8	Q.		125			188	
IOL Low-level output current		B1-B8			20			24	mA
TA	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST COMPLETIONS		SN54BCT25642			SN74BCT25642			Ī	
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	I _I = -18 mA				-1.2			-1.2	V
	A D	$V_{CC} = 4.75 V,$	IOH = -3 mA				2.7			v
Vон	Any B	$V_{CC} = 4.5 V$	IOH = -3 mA	2.4	3.3		2.4	3.3		V
		$V_{CC} = 4.5 V$	IOL = 94 mA		0.38	0.55		0.42	0.55	
	Any A	$V_{CC} = 4.5 V$	IOL = 125 mA			8.0				٧
Vo		$V_{CC} = 4.5 V$	I _{OL} = 188 mA						0.7	
VOL	Amy B	$V_{CC} = 4.5 V$	IOL = 20 mA		0.3	0.5				ν
	Any B	$V_{CC} = 4.5 V$	IOL = 24 mA					0.35	0.5	٧
ЮН	Any A	$V_{CC} = 4.5 V$	VOH = 5.5 V			6,0			0.1	mA
1.	A and B	$V_{CC} = 5.5 V$	V _I = 5.5 V			0.25			0.25	
Ŋ	DIR and G	$V_{CC} = 5.5 V$	V _I ≈ 5.5 V		08	0.1			0.1	mA
t+	A and B	$V_{CC} = 5.5 V$	V _I = 2.7 V		4	70			70	
11H [‡]	DIR and G	$V_{CC} = 5.5 V$	V _I = 2.7 V	QQC ^C	177	20			20	μA
1+	A anb B	$V_{CC} = 5.5 V$	V _I = 0.5 V	"O	,	-0.6			-0.6	4
կլ‡	DIR and G	$V_{CC} = 5.5 V$	V _I = 0.5 V	Q,		-0.6			-0.6	mA
los§	Any B	$V_{CC} = 5.5 V$	V _O = 0	-60		- 150	-60		- 150	mA
ICCL	A to B	V _{CC} = 5.5 V			40	64		40	64	mΑ
ССН	A to B	VCC = 5.5 V			25	40		25	40	mΑ
lccz	A to B	VCC = 5.5 V			7.6	13		7.6	13	mA
ICCL	B to A	V _{CC} = 5.5 V			78	125		78	125	mA
ІССН	B to A	V _{CC} = 5.5 V			34	55		34	55	mA
_	A Ports	V== = 5.5.V	V 05V ~ 05V		15			15		
C _{io}	B Ports	VCC = 5.5 V,	$V_1 = 2.5 \text{ V or } 0.5 \text{ V}$		8			8		рF
Ci	Control inputs	$V_{CC} = 5.5 V,$	V _I = 2.5 V or 0.5 V		8			8		pF

 $^{^\}dagger$ All typical values are at VCC = 5 V, TA = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 10 ms.

SN54BCT25642, SN74BCT25642 25-OHM OCTAL BUS TRANSCEIVERS

SCBS047-TI0221--D3395, DECEMBER 1989--REVISED JUNE 1990

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	ТО (ОИТРИТ)	CL R1 R2	C = 5 \ = 50 p = 500 (= 500 (= 25°)	F, Ω‡, Ω, C	Τ _Α	CL = R1 = 5 R2 = A = MIN	500 Ω‡, 500 Ω, I to MAX	;†	UNIT
			MIN	CT2564	2 MAX	'54BCT	25642 MAX	'74BCT	25642 MAX	
tPLH			0.8	3.2	6	0.8	6 .5	0.8	6.2	
t _{PHL}	A	В	0.5	2	3.9	0.5	4.1	0.5	4	ns
tPLH .	В	Α	1.5	3.2	4.7	1.5	₹ 7.4	1.5	6.3	
tPHL	В	^	1.7	4.5	4.8	1.7	6.7	1.7	5.9	ns
tPLH .	 G	A	2.8	5.5	10.4	2.8	12.9	2.8	11.6	ns
t _{PHL}	G	^	4.6	8.6	11.3	5.4	11.8	4.6	11.3	10
tPZH	G	В	3.3	5.7	8.1	3.3	9.7	3.3	9.1	no
tPZL	9	B	3.8	6.6	8.8	3.8	10.2	3.8	9.8	ns
t _{PHZ}	G	В	1.8	4.6	7	ି1.8	8	1.8	7.3	ns
tPLZ	9	B	1.4	4.3	6.7	1.4	8.4	1.4	7.3	118

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] For port A, R1 = 100 Ω .

SN54BCT25646, SN74BCT25646 OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0230-D3534, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25646 is an octal noninverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω . The B-port outputs are designed to source 3 mA and to sink 24 mA.

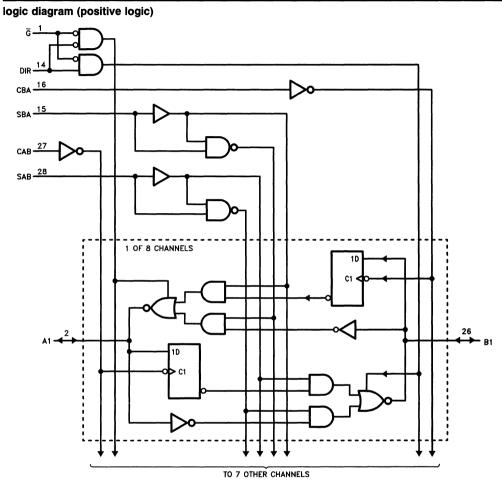
When the output-enable input \overline{G} is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. The 'BCT25646 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25646 reduce switching noise for more reliable system operation.

The SN54BCT25646 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT25646 is characterized for operation from 0°C to 70°C.

SN54BCT25646 ... JT PACKAGE SN74BCT25646 ... NT PACKAGE (TOP VIEW)

Ğ۵	1 -	28 SAB	
A1 [2	27 CAB	
GND [3	26 🗌 B1	
A2 [4	25 🗌 B2	
A3 [5	24 V _{CC}	
GND [6	23 🗌 B3	
A4 [7	22 🗌 B4	
A5 [8	21 B5	
GND [9	20 🗌 B6	
A6 [10	19 \ V _{CC}	
A7 []11	18 🗌 B7	
GND [12	17 🗌 B8	
_ 8A	13	16 CBA	
DIR [14	15 SBA	



SN54BCT25648, SN74BCT25648 OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0231-D3535, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25648 is an octal inverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω . The B-port outputs are designed to source 3 mA and to sink 24 mA.

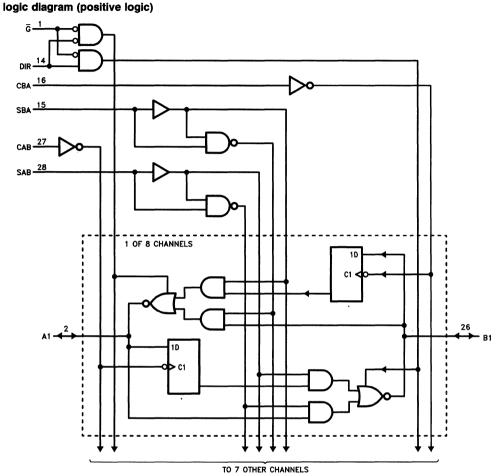
When the output-enable input \overline{G} is low, the device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (DIR) input. The 'BCT25648 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the inverse of the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the inverse of the current A bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25648 reduce switching noise for more reliable system operation.

The SN54BCT25648 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25648 is characterized for operation from 0°C to 70°C.

SN54BCT25648 ... JT PACKAGE SN74BCT25648 ... NT PACKAGE (TOP VIEW)

Ē [1	28	SAB
A1 [2	27	CAB
GND [3	26]B1
A2 [4	25	_B2
A3 [5	24	□v _{cc}
GND [6	23] B3
A4 🗌	7	22]B4
A5 [8	21] B5
GND [9	20]в6
A6 🗌	10	19	□v _{cc}
A7 🗌	11	18	_B7
GND [12	17] вв
A8 [13	16	CBA
DIR [14	15	SRA



SN54BCT25651, SN74BCT25651 OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0232-D3536, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25651 is an octal inverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω . The B-port outputs are designed to source 3 mA and to sink 24 mA.

The A and B ports have separate output-enable inputs. When the A-to-B enable (GAB) is high, the B-bus outputs are active (high or low logic levels); when GAB is low, the B-bus outputs are in the high-impedance state. GBA controls the A-bus outputs: when GBA is low, the A-bus outputs are active (high or low logic levels); when GBA is high, the A-bus outputs are in the high-impedance state.

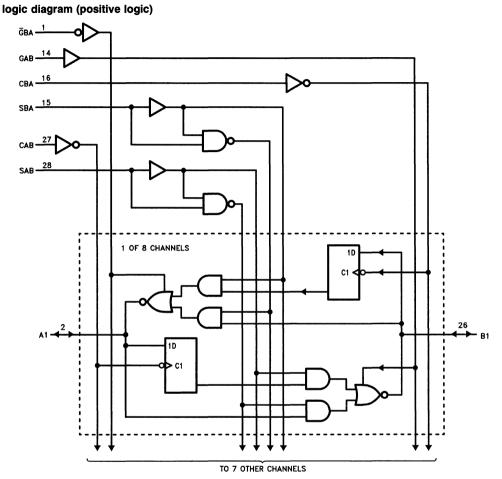
The 'BCT25651 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the inverse of the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the inverse of the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25651 reduce switching noise for more reliable system operation.

The SN54BCT25651 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25651 is characterized for operation from 0°C to 70°C.

SN54BCT25651 ... JT PACKAGE SN74BCT25651 ... NT PACKAGE (TOP VIEW)

ḠBA [1	28 SAB
A1 [2	27 CAB
GND [3	26 🗌 B1
A2 🗌	4	25 B2
A3 🗌	5	24 V _{CC}
GND 🗌	6	23 🗌 B3
A4 🗌	7	22 B4
A5 🗌	8	21 B5
GND [9	20 🗌 B6
A6 [10	19∏ V _{CC}
A7 🗌	11	18 🗌 B7
GND [12	17 🗌 B8
A8 [13	16 CBA
GAB [14	15 SBA





SN54BCT25652, SN74BCT25652 OCTAL 25-OHM REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0233--- D3537, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces Iccz
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25652 is an octal noninverting registered bus transceiver. The A-port outputs are designed to source up to 80 mA and to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω . The B-port outputs are designed to source 3 mA and to sink 24 mA.

The A and B ports have separate output-enable inputs. When the A-to-B enable (GAB) is high, the B-bus outputs are active (high or low logic levels); when GAB is low, the B-bus outputs are in the high-impedance state. GBA controls the A-bus outputs: when GBA is low, the A-bus outputs are active (high or low logic levels); when GBA is high, the A-bus outputs are in the high-impedance state.

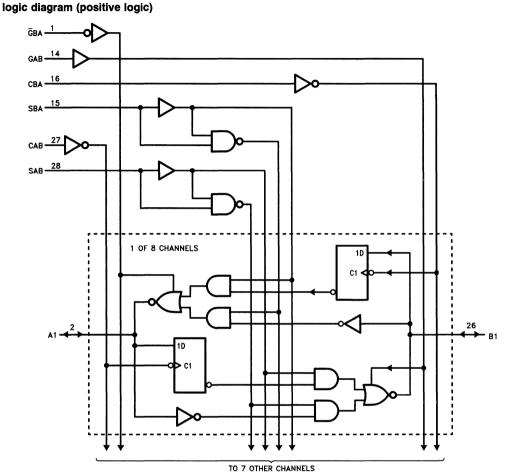
The 'BCT25652 can transmit either real-time or previously stored data. In the A-to-B mode, a low-to-high transition on the clock input (CAB) stores the data present at the A bus. When the select input (SAB) is high, the data stored on the previous low-to-high transition of CAB appears on the B bus. When SAB is low, the current A-bus data appears on the B bus. Data flow from the B bus to the A bus uses the CBA and SBA inputs.

The distributed V_{CC} and GND pins of the 'BCT25652 reduce switching noise for more reliable system operation.

The SN54BCT25652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT25652 is characterized for operation from 0°C to 70°C.

SN54BCT25652	 JT	PACKAGE
SN74BCT25652	 NT	PACKAGE

GBA □	1	∪ ₂₈	SAB
A1 🗌	2	27	CAB
GND [3	26]B1
A2 [4	25	□ B2
A3 🗌	5	24	□ v _{cc}
GND [6	23	□ B3
A4 🗌	7	22	☐ B4
A5 [8	21	□ B5
GND [9	20	□ B6
A6 🗌	10	19	□ v _{cc}
A7 🗌	11	18	□ B7
GND [12	17	_] B8
A8 🗌	13	16	CBA
GAR	14	15	SBA



SN54BCT25756, SN74BCT25756 OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

TI0242-D3562, JUNE 1990

- Open-Collector Version of 'BCT25240
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- State-of-the-Art BiCMOS Design Significantly Reduces ICC7
- Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)
- Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25756 is an open-collector version of the SN54BCT25240 and SN74BCT25240. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω .

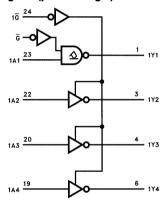
When the output-enable input $1\overline{G}$ (or $2\overline{G}$) is low, the device transmits the inverse of the appropriate A-input data to the corresponding Y outputs. Setting $1\overline{G}$ (or $2\overline{G}$) high turns the corresponding outputs off.

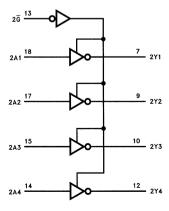
The SN54BCT25756 is characterized over the full military temperature range of -55°C to 125°C. The SN74BCT25756 is characterized for operation from 0°C to 70°C.

SN54BCT25756 ... JT PACKAGE SN74BCT25756 ... NT PACKAGE (TOP VIEW)

1Y1∐1	U24	∐1Ğ
GND 🛮 2	23]1A1
1Y2∐3	22]1A2
1Y3∐4	21	□vcc
GND∏5	20]1A3
1Y4∐6	19]1A4
2Y1∐7	18	_2A1
GND∏8	17]2A2
2Y2∏9	16	□v _{cc}
2Y3 🛮 1	0 15	_2A3
GND ☐ 1	1 14]2A4
2Y4 🛮 1	2 13]2Ġ

logic diagram (positive logic)







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SN54BCT25757, SN74BCT25757 OCTAL 25-OHM LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

TI0240-D3563, JUNE 1990

- 25-Ω Open-Collector Version of 'BCT2241
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)
- Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT25757 is a 25- Ω open-collector version of the SN54BCT2241 and SN74BCT2241. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω .

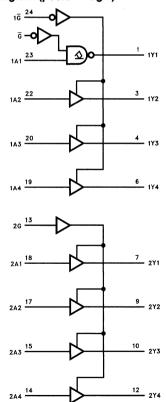
The 'BCT25757 has complementary output-enable inputs. When output-enable input $1\overline{G}$ is low, the device transmits the 1A-input data to the 1Y outputs; setting $1\overline{G}$ high turns the 1Y outputs off. Output enable 2G affects the 2Y outputs similarly, but is active-high.

The SN54BCT25757 is characterized over the full military temperature range of -55° C to 125°C. The SN74BCT25757 is characterized for operation from 0°C to 70°C.

SN54BCT25757 ... JT PACKAGE SN74BCT25757 ... NT PACKAGE (TOP VIEW)

_			
1 Y1∐	1	⊃ 24]1Ğ
GND□	2	23]1A1
1Y2[3	22]1A2
1Y3[4	21	□vcc
GND□	5	20	1A3
1Y4[6	19	□1A4
2Y1[7	18	□2A1
GND□	8	17	2A2
2Y2	9	16	□vcc
2Y3 🗌	10	15	□2A 3
GND	11	14	2A4
2Y4 🗆	12	13	2G

logic diagram (positive logic)





TI0241-D3564, JUNE 1990

- Open-Collector Outputs Drive Bus Lines or **Buffer Memory Address Registers**
- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- **Designed to Facilitate Incident-Wave** Switching for Line Impedances of 25 Ω or Greater
- Data Flow-Through Pinout (All Inputs Are on Opposite Side from Outputs)
- Distributed V_{CC} and GND Pins Reduce Switching Noise for More Reliable System Operation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil **DIPs**

description

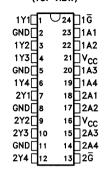
PRODUCT PREVIEW

The 'BCT25760 is an open-collector version of the SN54BCT25244 and SN74BCT25244. Its outputs are designed to sink up to 188 mA in order to facilitate incident-wave switching of transmission-line impedances down to 25 Ω .

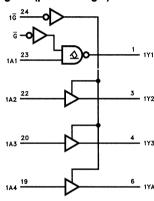
When the output-enable input $1\overline{G}$ (or $2\overline{G}$) is low, the device transmits the appropriate A-input data to the corresponding Y outputs. Setting 1G (or 2G) high turns the corresponding outputs off.

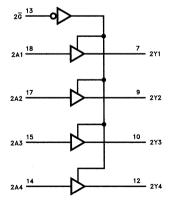
The SN54BCT25760 is characterized over the full military temperature range of -55°C to 125°C. The SN74BCT25760 is characterized for operation from 0°C to 70°C.

SN54BCT25760 ... JT PACKAGE SN74BCT25760 ... NT PACKAGE (TOP VIEW)



logic diagram (positive logic)





INSTRUMENTS

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TEXAS

General Information
ACL LSI Products 2
ACL Widebus™ Products
BTL Transceiver Products 4
Bus-Termination Array Products 5
Clock Driver Products
ECL/TTL Translator Products 7
FIFO Products 8
Low-Impedance Line Driver Products 9
Memory Driver Products 10
SCOPE™ Testability Products
64BCT Series Products 12
Mechanical Data

SN54ALS2240, SN74ALS2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D2910, JULY 1985-REVISED MAY 1986

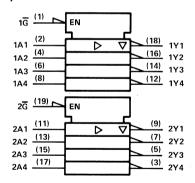
- Buffers/Line Drivers for Driving MOS Devices
- I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

The SN54ALS2240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS2240 is characterized for operation from 0°C to 70°C.

logic symbol†

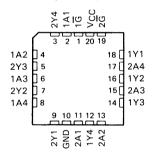


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ALS2240 . . . J PACKAGE SN74ALS2240 . . . DW OR N PACKAGE (TOP VIEW)

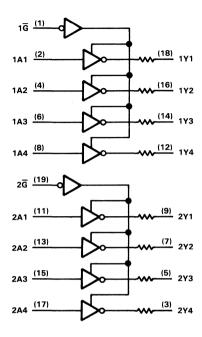
1G 1A1 2Y4 1A2 2Y3 1A3	1 2 3 4 5	19 18 17 16	V _C C 2 \overline{G} 1Y1 2A4 1Y2 2A3
	□4	17	
	Hັ		닏
2Y2	沜	14	1Y3
1A4	8	13	2A2
2Y1	□9	12] 1Y4
GND	10	11	2A1

SN54ALS2240 . . . FK PACKAGE (TOP VIEW)



D2910, JULY 1985-REVISED MAY 1986

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS2240	-55°C to 125°C
SN74ALS2240	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN	SN54ALS2240			SN74ALS2240			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
ViH	High-level input voltage	2			2			V	
VIL	Low-level input voltage	4		0.7			0.8	V	
TA	Operating free-air temperature	-55		125	0		70	°C	

SN54ALS2240, SN74ALS2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D2910, JULY 1985-REVISED MAY 1986

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COME	UTIONO	SN	54ALS2	240	SN	74ALS22	40	
PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0 - 0.4 mA	V _{CC} -2			V _{CC} -2			V
Vol	$V_{CC} = 4.5 \text{ V},$			0.15	0.5		0.15	0.5	V
VOL	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	l
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			20			20	μΑ
lozL	V _{CC} = 5.5 V,	$V_0 = 0.4 \text{ V}$			- 20			- 20	μΑ
l _l	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V			0.1			0.1	mA
lін	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΙΙL	$V_{CC} = 5.5 V$,	$V_1 = 0.4 V$			-0.1			-0.1	mA
lo [‡]	V _{CC} = 5.5 V,	$V_0 = 2.25 V$	-30		-112	-30		-112	mA
ЮН	V _{CC} = 4.5 V,	V _O = 2 V	- 15			-15			mA
loL	$V_{CC} = 4.5 \text{ V},$	V _O = 2 V	15			15			mA
		Outputs high		6	11		6	11	
^l cc	V _{CC} = 5.5 V	Outputs low		13	23		13	23	mA
		Outputs disabled		12	20		12	20	1

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	то (ОИТРИТ)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25 ^{\circ}C$ 'ALS2240	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to LS2240	M'AX	, ALS2240	UNIT	
			TYP	MIN	MAX	MIN	MAX	1	
^t PLH	A		6	2	14	2	10	ns	
^t PHL	1 ^	ľ	•	6	2	14	2	10	1 115
^t PZH	G	V	10	5	20	5	17	ns	
tPZL	ď	'	12	7	25	7	20] "15	
^t PHZ	G	γ	7	2	12	2	10		
t _{PLZ}	· ·	'	9	4	20	4	15	ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

SN54ALS2244, SN74ALS2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3286, SEPTEMBER 1988

- Buffers/Line Drivers for Driving MOS Devices
- P-N-P Inputs Reduce DC Loading
- Output Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

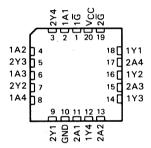
These octal buffers and line drivers are designed to drive the capacitive inputs of MOS devices and to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices feature high fan-out and improved fan-in.

The SN54ALS2244 is characaterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS2244 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

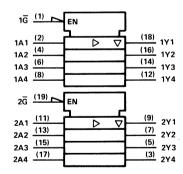
SN54ALS2244 . . . J PACKAGE SN74ALS2244 . . . DW OR N PACKAGE (TOP VIEW)

1Ğ 🏻	1 U	20	Vcc
1A1 🛮	2	19	2 <u>G</u>
2Y4 🛚	3	18	1Y1
1A2 🔲	4	17	2A4
2Y3 🗍	5	16	1Y2
1A3 🔲	6	15	2A3
2Y2 🔲	7	14	1Y3
1A4 🛚	8	13	2A2
2Y1 🔲	9	12	1Y4
GND 🛚	10	11	2A1

SN54ALS2244 . . . FK PACKAGE (TOP VIEW)

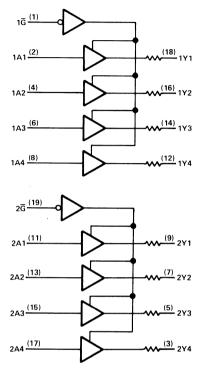


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage	7 V
Voltage applied to any output in the disabled or power-off state	5.5 V
Operating free-air temperature ranges: SN54ALS2244	-55°C to 125°C
SN74ALS2244	
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS2244, SN74ALS2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS D3286, SEPTEMBER 1988

recommended operating conditions

		SN	SN54ALS2244			SN74ALS2244		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2	ox	EAKEM	2			V
VIL	Low-level input voltage	9805	0000	0.7			0.8	٧
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN	54ALS2	244	SN74ALS2244			LIBILT
PARAMETER	TEST C	ONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	l _l = -18 mA			-1.2			-1.2	V
Voн	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	I _{OH} = -0.4 mA	Vcc-	2		Vcc-	2		V
Vo	V _{CC} = 4.5 V	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V
VOL	VCC = 4.5 V	IOL = 12 mA		0.45	0.8		0.45	0.8	V
IOH	$V_{CC} = 4.5 V$,	V ₀ = 2 V	- 15			- 15			mA
loL	$V_{CC} = 4.5 V$	V _O = 2 V	15	JUCT PR	EAIEA	15			mA
t _l	$V_{CC} = 5.5 \text{ V},$	V _I = 7 V	20 ₉₉ 9		0.1			0.1	mA
ΙΗ	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	V _I = 0.4 V			-0.1			-0.1	mA
lozh	$V_{CC} = 5.5 V$,	$V_0 = 2.7 V$			20			20	μΑ
lozL	$V_{CC} = 5.5 V$,	$V_0 = 0.4 V$			- 20			- 20	μΑ
lo‡	$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	-30		-112	-30		-112	mA
Іссн				11	17		11	17	
ICCL	$V_{CC} = 5.5 V$	Outputs open		14	22		14	22	mA
Iccz				15	23		15	23	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

switching characteristics (see Note 1)

PARAMETER	FROM (INTPUT)	$\begin{array}{c} V_{CC} = 4.5 \text{ V to S} \\ C_{L} = 50 \text{ pF}, \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_{A} = \text{MIN to MA} \\ \\ \text{SN54ALS2244} \qquad \text{SN} \end{array}$		F, Ω, Ω, to MAX		UNIT	
			SN54ALS2244		SN74ALS2244		
			MIN	MAX	MIN	MAX	
^t PLH	A	V	3	17	3	16	
^t PHL	1 ^	*	3	19	3	17	ns
^t PZH	G	_	1	PREV 18	1	17	
^t PZL] "	,	1 PRIDUCI	15	1	14	ns
^t PHZ	G	_	1	9	1	9	no
tPLZ		T	1	9	1	9	ns

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.



^{*} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS

JUNE 1984-REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Outputs Have 25-Ω Series Resistor, So No External Resistors are Required
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

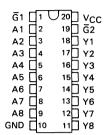
These octal buffers and line drivers are designed to drive capacitive input characteristics of MOS devices and have the performance of the popular SN54ALS24OA/SN74ALS24OA series. At the same time, they offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND with active-low inputs such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

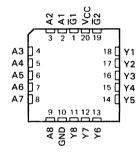
The 'ALS2540 offers inverting data and the 'ALS2541 offers true data at the outputs.

The SN54ALS' is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74ALS' is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN54ALS2540, SN54ALS2541 . . . J PACKAGE SN74ALS2540, SN74ALS2541 . . . DW OR N PACKAGE (TOP VIEW)

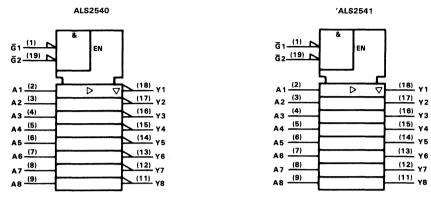


SN54ALS2540, SN54ALS2541 . . . FK PACKAGE (TOP VIEW)



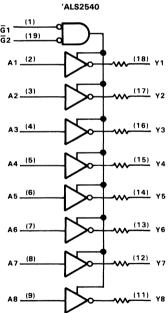
JUNE 1984-REVISED MAY 1986

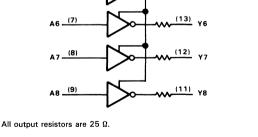
logic symbols†

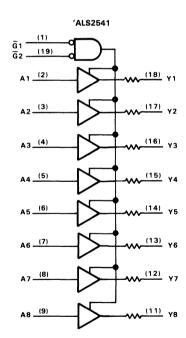


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)







JUNE 1984-REVISED MAY 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}
Input voltage
Voltage applied to a disabled 3-state output
Operating free-air temperature range: SN54ALS2540, SN54ALS2541 55 °C to 125 °C
SN74ALS2540, SN74ALS2541 0 °C to 70 °C
Storage temperature range65°C to 150°C

recommended operating conditions

		S	SN54ALS2540 SN54ALS2541			SN74ALS2540			
		s				SN74ALS2541			
		MIN	NOM	MAX	MIN	NOM	MAX		
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
IОН	High-level output current			-0.4			-0.4	mA	
loL	Low-level output current			12			12	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST O	TEST CONDITIONS		N54ALS N54ALS		1	74ALS2 74ALS2		UNIT
	ANAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONI
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2			-1.2	V
Vон			$5 \text{ V, I}_{OH} = -0.4 \text{ mA}$	V _{CC} -	2		Vcc-	2		V
VOL		$V_{CC} = 4.5 \text{ V},$			0.15	0.5		0.15	0.5	\ \
*OL	$V_{CC} = 4.5 V$,		I _{OL} = 12 mA		0.35	0.8		0.35	0.8	ľ
lozh		$V_{CC} = 5.5 V,$				20			20	μΑ
lozl		$V_{CC} = 5.5 V,$	V _O = 0.4 V			- 20			- 20	μΑ
ЮН		$V_{CC} = 4.5 \text{ V},$	V _O = 2 V	- 15			- 15			mA
IOL		$V_{CC} = 4.5 V,$	$V_0 = 2 V$	30			30			mA
11		$V_{CC} = 5.5 V$,	V _I = 7 V			0.1			0.1	mA
JIН		$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
IL		V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
lo‡		$V_{CC} = 5.5 V$,	V _O = 2.25 V	- 15		- 70	- 15		- 70	mA
			Outputs high		5	10		5	10	
	'ALS2540	$V_{CC} = 5.5 V$	Outputs low		13	22		13	22	mA
lcc			Outputs disabled		11	19		11	19	1
100	'ALS2541		Outputs high		6	14		6	14	
		$V_{CC} = 5.5 V$	Outputs low		15	25		15	V 0.5 0.8 20 μA -20 μA mA mA 0.1 mA 20 μA -70 mA 10 22 mA	
			Outputs disabled		13.5	22		13.5	22	1

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.



[‡]The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

JUNE 1984-REVISED MAY 1986

'ALS2540 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = 25 ^{\circ}C$	C _L R1 R2 T _A	C = 4.5 V = 50 pF, = 500 Ω , = 500 Ω , = MIN to	MAX		UNIT	
				'ALS2540	SN54A	LS2540	SN74A	LS2540	1
			TYP	MIN	MAX	MIN	MAX		
t _{PLH}	Α	V	7.5	2	14	2	12		
^t PHL	7 ^	^	5.6	2	13	2	11	ns	
tPZH	G	· · · · · · · · · · · · · · · · · · ·	9	5	18	5	15		
^t PZL	7	*	12.6	8	24	8	20	ns	
t _{PHZ}	G	· · · · · · · · · · · · · · · · · · ·	4	1	12	1	10		
t _{PLZ}		'	7	2	14	2	12	ns	

'ALS2541 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$		$V_{CC} = 4.5 \text{ V}$ $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to M}$			UNIT	
		}		'ALS2541	SN54A	LS2541	SN74ALS2541		
			TYP	MIN	MAX	MIN	MAX		
tPLH	Α	Y	8.7	2	17	2	15		
tPHL	7 1	1	7	2	14	2	12	ns	
tPZH	G		9	5	18	5	15		
tPZL]	Y	12.6	8	24	8	20	ns	
tPHZ	G		4	1	12	1	10	ns	
tpLZ] "	•	7	2	14	2	12	118	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

DECEMBER 1983-REVISED MAY 1986

- Octal Bus Transceivers for Driving MOS Devices
- I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Local Bus-Latch Capability
- Choice of True or Inverting Logic
- Package Options Include Plastic "Small Outline" Packages, Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

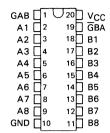
These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs $(\overline{G}BA)$ and GAB.

The enable inputs can be used to disable the device so that the buses are effectively isolated.

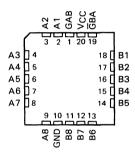
The dual-enable configuration gives the 'AS2620 or 'AS2623 the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'AS2623 or complementary for the 'AS2620.

The SN54AS2620 and SN54AS2623 are characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN74AS2620 and SN74AS2623 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

SN54AS' . . . J PACKAGE SN74AS' . . . DW OR N PACKAGE (TOP VIEW)



SN54AS' . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE

ENABLE	INPUTS	OPERATION				
GBA	A GAB 'AS2620		'AS2623			
L	L	B data to A bus	B data to A bus			
Н	Н	Ā data to B bus	A data to B bus			
Н	L	Isolation	Isolation			
		B̄ data to A bus,	B data to A bus,			
L	н	Ā data to B bus	A data to B bus			

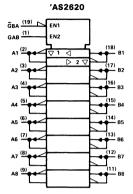
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.

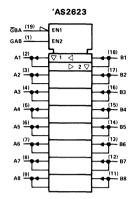


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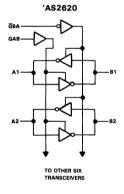
logic symbols†

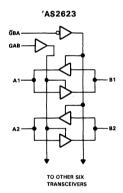




 $[\]dagger_{\mbox{These symbols are in accordance with ANSI/IEEE}$ Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





DECEMBER 1983-REVISED MAY 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage	a, V _{CC}
Input voltage:	All inputs
	I/O ports
Operating free	rair temperature range: SN54AS2620, SN54AS2623 – 55 °C to 125 °C
	SN74AS2620, SN74AS2623
Storage tempe	erature range

recommended operating conditions

			SN54AS2620 SN54AS2623		SN74AS2620 SN74AS2623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			8.0	V
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST COND	ITIONS	1	54AS2		SN74AS2620 SN74AS2623			UNIT
			,		TYP†	MAX	MIN	TYPt	MAX	
VIK		V _{CC} = 4.5 V,	I ₁ = -18 mA			-1.2			-1.2	٧
Voн		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I _{OH} = -2 mA	V _{CC} -2			VCC-2			V
		V _{CC} = 4.5 V,	IOL = 1 mA		0.15	0.4		0.15	0.4	
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 12 mA		0.35	0.7		0.35	0.7	V
	Control inputs	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	
iį.	A or B ports	$V_{CC} = 5.5 V$,	V _I = 5.5 V			0.1			0.1	mA
	Control inputs		- F F V V - 2 7 V			20			20	
ΉΗ	A or B ports‡	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			70			70	μΑ
	Control inputs					-0.5			-0.5	
ηL	A or B ports‡	$V_{CC} = 5.5 V$,	$V_I = 0.4 V$			-0.75			-0.75	mA
lo§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 \text{ V}$	- 50		- 150	- 50		- 150	mA
ЮН		V _{CC} = 4.5 V,	V _O = 2 V	-35			-35			mA
lOL		$V_{CC} = 4.5 V,$	V _O = 2 V	35			35			mA
			Outputs high		62	100		62	100	
	'AS2620	$V_{CC} = 5.5 V$	Outputs low		74	121		74	121	
1			Outputs disabled		48	77		48	77	
ICC			Outputs high		57	93		57	93	mA
	'AS2623	$V_{CC} = 5.5 V$	Outputs low		116	189		116	189	
			Outputs disabled		72	116		72	116	

[†]All typical values are at VCC = 5 V, T_A = 25 °C ‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

^{\$}The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

DECEMBER 1983-REVISED MAY 1986

'AS2620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$\begin{array}{c} V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,} \\ C_L = 50 \text{ pF,} \\ R1 = 500 \Omega, \\ R2 = 500 \Omega, \\ T_A = \text{MIN to MAX} \\ \hline SN54AS2620 \qquad SN74AS26. \end{array}$			UNIT	
			MIN	MAX	MIN	MAX	
t _{PLH}	А	В	1	9.5	1	8	
t _{PHL}		Б	1	7.5	1	6.5	ns
^t PLH	В	Α	1	9.5	1	8	
^t PHL		A	1	7.5	1	6.5	ns
tPZH	ĞВА	Α	1	11	1	10	
tPZL	GBA	[1	12	1	11	ns
^t PHZ	ĞВА	Α	1	7.5	1	6	ne
^t PLZ	GBA	(1	15	1	12	ns
^t PZH	GAB	В	1	9	1	8	ne
^t PZL	GAB .	ر ا	1	9	1	8	ns
^t PHZ	GAB	В	1	12	1	11	ne
tPLZ	UAB	B		12	1	11	ns

'AS2623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
				AS2623		AS2623	
			MIN	MAX	MIN	MAX	
tPLH	А	В	1	9.5	1	8.5	ns
^t PHL		В	1	8.5	1	7.5	115
t _{PLH}	В	Α	1	10	1	9	ns
tPHL	ь	^	1	9	1	7.5	115
^t PZH	G BA	А	1	12.5	1	11	
tpZL	GDA	^	1	12	1	11	ns
^t PHZ	GBA	Α	1	8.5	1	7.5	
tPLZ	GBA	^	1	13	1	12	ns
tPZH	GAB	В	1	13	1	12	
tPZL	UAB	5	1	13.5	1	12	ns
^t PHZ	0.15	В	1	7.5	1	7	
^t PLZ	GAB	В	1	14.5	1	12.5	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

DECEMBER 1983-REVISED MAY 1986

- Octal Bus Transceivers for Driving MOS Devices
- I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required
- Choice of True or Inverting Logic
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so the buses are effectively isolated.

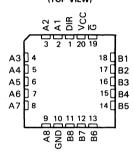
The SN54AS' family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74AS' family is characterized for operation from 0 °C to 70 °C.

SN54AS' . . . J PACKAGE SN74AS' . . . DW or N PACKAGE

(TOP VIEW)

DIR 🗌	1	U 20	□vcc
A1 [2	19	ĪĒ
A2 [3	18	B1
A3 [4	17	B2
A4 [5	16	B3
A5 [6	15	B4
A6 [7	14	B5
A7 🗆	8	13	B6
A8 [9	12	B7
GND	10	11	1 B8

SN54AS' . . . FK PACKAGE (TOP VIEW)

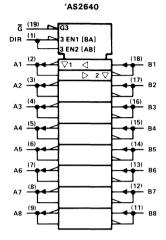


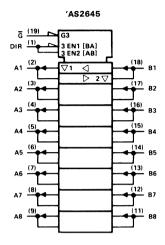
FUNCTION TABLE

CONTROL		OPERATION					
		'AS2640	'AS2645				
Ğ	DIR	A52040	A32045				
L	L	B data to A bus	B data to A bus				
L	н	Ā data to B bus	A data to B bus				
н х		Isolation	Isolation				

DECEMBER 1983—REVISED MAY 1986

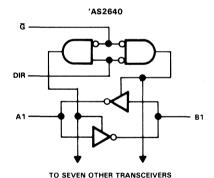
logic symbols†





[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagrams (positive logic)



A1 B1

DECEMBER 1983-REVISED MAY 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54AS2640, SN54AS2645	-55°C to 125°C
SN74AS2640, SN74AS2645	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

			N54AS2 N54AS2			74AS26 74AS26		UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2	-		2			V
VIL	Low-Ivel input voltage			0.8			0.8	V
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	404447770	TF0T 00110	1710110		SN54A	S'		SN74AS	•	
	ARAMETER	TEST COND	IIIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	I _I = -18 mA	1		-1.2			-1.2	٧
Vон		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	IOH = -2 mA	Vcc-	2		vcc-	- 2		٧
VOL		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 1 mA		0.15	0.4		0.15	0.4	V
VOL		$V_{CC} = 4.5 V$,	I _{OL} = 12 mA		0.35	0.7		0.35	0.7	v
4	Control inputs	V _{CC} = 5.5 V,	V _I = 7 V	1		0.1			0.1	mA
4	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1			0.1	11174
ΙН	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
4H	A or B ports [‡]	VCC = 5.5 V,	V ₁ - 2.7 V			70			70	μΑ
lu .	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.5			-0.5	mA
llL.	A or B ports [‡]	VCC = 5.5 V,	VI = 0.4 V			-0.75			-0.75	IIIA
lo§		$V_{CC} = 5.5 V$,	$V_0 = 2.25 V$	- 50		- 150	- 50		- 150	mA
ТОН		V _{CC} = 4.5 V,	V ₀ = 2 V	-35			- 35			mA
lOL		V _{CC} = 4.5 V,	V _{OL} = 2 V	35			35			mA
			Outputs high		37	58		37	58	
	'AS2640		Outputs low		78	123		78	123	
lcc		V _{CC} = 5.5 V	Outputs disabled		51	80		51	80	mA
'CC		VCC = 5.5 V	Outputs high		58	95		58	95	ı mA
	'AS2645		Outputs low		95	155		95	155	
	1		Outputs disabled		73	119		73	119	

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

For I/O ports, the parametes I_I_{II} and I_{II} include the off-state output current.

§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

SN54AS2640, SN54AS2645 SN74AS2640, SN74AS2645 OCTAL BUS TRANSCEIVERS/MOS DRIVERS DECEMBER 1983—REVISED MAY 1986

'AS2640 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 4 C _L = 50 R1 = 50 R2 = 50 T _A = Mil	0Ω, 0Ω,	5 V,	UNIT
			SN54/	AS2640	SN74		
			MIN	MAX	MIN	MAX	
^t PLH	A D	0 4	1	9.5	1	7.5	
^t PHL	A or B	B or A	1	7	1	6.5	ns
tPZH		A D	2	11	2	9	
^t PZL	G	A or B	2 12		2	10	ns
tPHZ	G	A D	1	8	1	7	
tPLZ .	<u> </u>	A or B	2	15	2	13	ns

'AS2645 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		C _L = 50 R1 = 500 R2 = 500 T _A = MIN	Ω, Ω, N to MAX		UNIT
			SN54#	NS2645	SN74		
			MIN	MAX	MIN	MAX	
tPLH .	A 2	2	1	12	1	10	
tPHL	A or B	B or A	1	11	1	9.5	ns
tPZH	G	A 0	1	13	1	11.5	
tPZL	G	A or B	1	13	1	10.5	ns
tPHZ	G	A or B	1	9	1	8	
tPLZ	L	A or B	1	13	1	12	ns

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

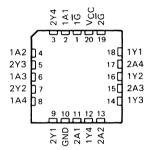
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2241 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{\mathbf{G}}$ (active-low output control) inputs, and complementary \mathbf{G} and $\overline{\mathbf{G}}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT2240 is characterized for operation from 0°C to 70°C.

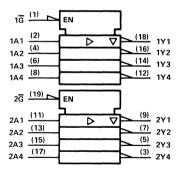
SN54BCT2240 . . . J PACKAGE SN74BCT2240 . . . DW OR N PACKAGE (TOP VIEW)



SN54BCT2240 . . . FK PACKAGE (TOP VIEW)



logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

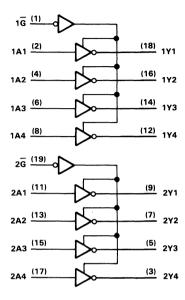


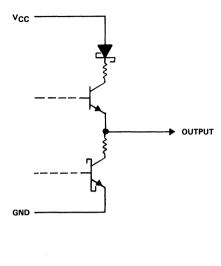
SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

logic diagram (positive logic)

schematic of each output





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

voltage, Vcc	0.5 V to 7 V
oltage (see Note 1)	
applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
applied to any output in the high state	0.5 V to VCC
amp current	30 mA
into any output in the low state	24 mA
ng free-air temperature range: SN54BCT2240	-55°C to 125°C
SN74BCT2240	0°C to 70°C
temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN	54BCT2	240	SN74BCT2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	٧
ΊΚ	Input clamp current			- 18			- 18	mA
ЮН	High-level output current			-12			-12	mA
loL	Low-level output current			12			12	mA
TA	Operating free-air temperature	- 55		125	0		70	°C



SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN	54BCT2	240	SN	74BCT2	240	UNIT
PANAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	ONIT
VIK	$V_{CC} = 4.5 V,$	I _{OH} = -18 mA			-1.2			-1.2	V
Voн	V _{CC} = 4.5 V	IOH = -1 mA	2.4	3.3		2.4	3.3		v
VOH	VCC = 4.5 V	I _{OH} = -12 mA	2	3.2		2	3.2		•
	V _{CC} = 4.5 V	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	v
VOL	VCC = 4.5 V	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	٧
l _l	$V_{CC} = 5.5 V,$	V ₁ = 5.5 V			0.1			0.1	` mA
ΊΗ	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	V _I = 0.5 V			- 1			- 1	mA
IOZH	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50			50	μΑ
IOZL	$V_{CC} = 5.5 V$,	$V_0 = 0.5 V$			- 50			- 50	μΑ
los‡	$V_{CC} = 5.5 V,$	V _O = 0	- 100		- 225	- 100		- 225	mA
ІССН				19	32		19	32	
ICCL	$V_{CC} = 5.5 V$,	Outputs open		46	76		46	76	mA
Iccz				6	8		6	8	

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R R:	CC = 5 L = 50 1 = 50 2 = 50 A = 25	pF, Ο Ω, Ο Ω,		V _{CC} = 4.5 C _L = 50 pF R1 = 500 R2 = 500 T _A = MIN	:, Ω Ω,	V ,	UNIT
			7	3CT224	0	SN5	4BCT2240	SN74BCT2240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH		Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	no
tPHL	- A	, T	0.5	2.8	4	0.5	4.6	0.5	4.4	ns
^t PZH	G		2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns
^t PZL] "		4.3	8.8	10.9	4.3	12.9	4.3	12.4	115
tPHZ	<u>_</u> <u>_</u> <u>_</u> <u>_</u> _		2	5.3	7.1	2	9.2	9.2 2 8.7		
tPLZ	7 6	Y	2.2	6.7	8.5	2.2	12.2	2.2	10.6	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

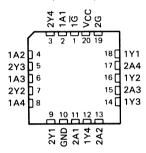
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{G} (active-low output control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2241 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74BCT2241 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

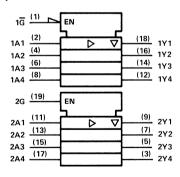
SN54BCT2241 . . . J PACKAGE SN74BCT2241 . . . DW OR N PACKAGE (TOP VIEW)

> 1<u>G</u> ∏1 U20∐ VCC 1A1 ∏2 19 7 2G 18 T1Y1 2Y4 T3 1A2 🗌 17 72A4 2Y3 75 16 1Y2 1A3 ∏6 15 2A3 2Y2 Π 7 14 T 1Y3 1A4 🛮 8 13 2A2 2 1 □ 9 12 1Y4 GND ☐10 11 2A1

SN54BCT2241 . . . FK PACKAGE (TOP VIEW)



logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

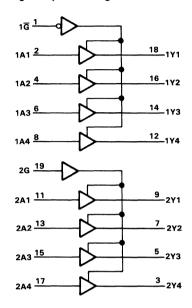


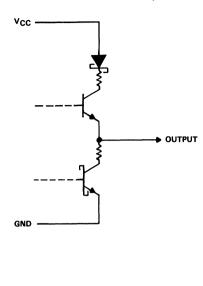
SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

logic diagram (positive logic)

schematic of each output





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, VCC	0.5 V to 7 V
Input voltage (see Note 1)	
Voltage applied to any output in the disabled or power-off state	-0.5~V to $5.5~V$
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	30 mA
Current into any output in the low state	24 mA
Operating free-air temperature range: SN54BCT2241	-55°C to 125°C
SN74BCT2241	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54B	CT2241	SN	UNIT		
		MIN N	OM MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5 5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2		2			V
VIL	Low-level input voltage	Á	0.8			0.8	٧
ΙK	Input clamp current		- 18			- 18	mA
ЮН	High-level output current	20,2	-12			- 12	mA
lOL	Low-level output current	de.	12			12	mA
TA	Operating free-air temperature	- 55	125	0		70	°C

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54BCT2241, SN74BCT2241 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST CONDITIONS	SN	54BCT2	241	SN	74BCT2	241	UNIT
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _{OH} = -18 mA			-1.2			-1.2	٧
	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3		2.4	3.3		
VoH	VCC = 4.5 V	I _{OH} = -12 mA	2	3.2		2			V
	$V_{CC} = 4.75 \text{ V}$	I _{OH} = -3 mA				2.7			
V	V _{CC} = 4.5 V	I _{OL} = 1 mA		0.38	0.55		0.15	0.5	V
VOL	VCC = 4.5 V	I _{OL} = 12 mA		- K-1			0.42	0.8	V
Ч	$V_{CC} = 5.5 V,$	V _I = 5.5 V		- del	0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V$,	V _I = 2.7 V		S.	20			20	μΑ
կլ	$V_{CC} = 5.5 V,$	V _I = 0.5 V	1	,	- 1			- 1	mA
lozh	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$	4.		50			50	μΑ
İOZL	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$		_	- 50			- 50	μΑ
los‡	$V_{CC} = 5.5 V,$	V _O = 0	- 100		- 225	- 100		- 225	mA
Іссн				23	37		23	37	
ICCL	$V_{CC} = 5.5 V,$	Outputs open		48	76		48	76	mA
Iccz				6	9		6	9	
Ci	$V_{CC} = 5 V$,	V _I = 2.5 V or 0.5 V		6			6		pF
Co	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		11			11		pF

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C R R: T,	CC = 5 L = 50 1 = 50 2 = 50 A = 25 BCT224	pF, Ο Ω, Ο Ω, •°C	SN54	$V_{CC} = 4.5$ $C_L = 50 \text{ pF}$ $R1 = 500$ $R2 = 500$ $T_A = MIN$ $BCT2241$, Ω, Ω, to MAX	V, 4BCT2241	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tpLH	A	Y	1.1	3	4.4	1.1	5,1	1.1	4.9	
^t PHL	7 ^	· ·	2.9	4.9	6.6	2.9	3. (2 7 .2	2.9	6.9	ns
tPZH	G or \overline{G}	Y	2.7	6	7.8	2.7	<i>₹</i> ₹₹ 9.4	2.7	8.9	
tPZL] Gord	<u> </u>	4.1	7.7	9.4	4.1	10.9	4.1	10.3	ns
tPHZ	G or \overline{G}	Y	2.5	5.2	7.2	,2:. 5	9.7	2.5	8.7	
tPLZ] G or G	ľ	3.2	7.1	9.5	3.2	12.9	3.2	, 11.3	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



^{*}Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

- BiCMOS Design Substantially Reduces Standby Current
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2241, these devices provide the choice of selected combinations of inverting outputs, symmetrical \overline{G} (active-low input control) inputs, and complementary G and \overline{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74BCT2244 is characterized for operation from 0°C to 70°C.

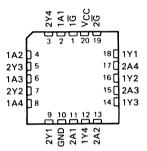
FUNCTION TABLE (each buffer)

INP	UTS	OUTPUT
Ğ	Α	Υ
Н	Х	Z
L	L	L
L	н	н

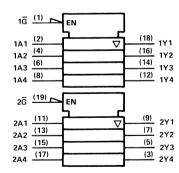
SN54BCT2244 . . . J PACKAGE SN74BCT2244 . . . DW OR N PACKAGE (TOP VIEW)

1G	Ц	1	U	20	Vcc	
1A1		2		19	2G	
2Y4		3		18	1Y1	
1A2	П	4		17	2A4	
2Y3	П	5		16	1Y2	
1A3	П	6		15	2A3	
2Y2	Ц	7		14	1Y3	
1A4		8		13	2A2	
2Y1	C	9		12	1Y4	
GND	Ц	10		11	2A1	

SN54BCT2244 . . . FK PACKAGE (TOP VIEW)



logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

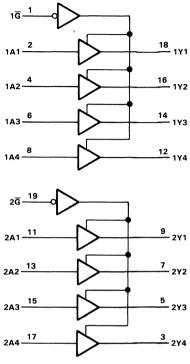


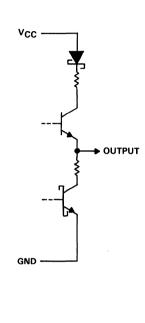
SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057. SEPTEMBER 1988-REVISED OCTOBER 1990

logic diagram (positive logic)

schematic of each output





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _C C
Input voltage (see Note 1)
Voltage applied to any output in the disabled or power-off state0.5 V to 5.5 V
Voltage applied to any output in the high state
Input clamp current
Current into any output in the low state
Operating free-air temperature range: SN54BCT224455°C to 125°C
SN74BCT2244 0°C to 70°C
Storage temperature range65 °C to 150 °C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.



SN54BCT2244, SN74BCT2244 OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

D3057, SEPTEMBER 1988-REVISED OCTOBER 1990

recommended operating conditions

		SN54BCT2244			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	ONT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			0.8	٧
lik	Input clamp current			- 18			- 18	mA
ЮН	High-level output current			-12			- 12	mA
loL	Low-level output current			12			12	mA
TA	Operating free-air temperature	- 55		125 -	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		SN	54BCT2	244	SN	LINUT		
PARAMETER	TEST C	CONDITIONS		TYP	MAX	MIN	TYP [†]	MAX	UNIT
VIK	$V_{CC} = 4.5 V$,	I _I = -18 mA			-1.2			-1.2	V
V	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.4			2.4			v
Voн	VCC = 4.5 V	IOH = -12 mA	2			2			
Va	V 4 5 V	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	v
VOL	V _{CC} = 4.5 V	IOL = 12 mA		0.35	0.8		0.35	0.8	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
4	$V_{CC} = 5.5 V,$	V _I = 5.5 V			0.1			0.1	mA
ЧН	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			20			20	μΑ
IĮL	$V_{CC} = 5.5 V,$	V ₁ = 0.5 V			- 1			– 1	mA
lozн	V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μΑ
lozL	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$			- 50			- 50	μΑ
los‡	$V_{CC} = 5.5 V,$	V _O = 0	- 100		-225	- 100		- 225	mA
¹ ССН				23	37		23	37	
^I CCL	$V_{CC} = 5.5 V$,	Outputs open		53	77		53	77	mA
ICCZ				6.5	10		6.5	10	.
Ci	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		6			6		
Co	V _{CC} = 5 V,	V _O = 2.5 V or 0.5 V		11			11		pF

switching characteristics (see Note 2)

PARAMETER	FROM (INTPUT)	TO (OUTPUT)	C _L R1 R2 T _A	= 50 = 500 = 500 = 25	C = 5 V, = 50 pF, = 500 Ω, = 500 Ω, = 25°C		V _{CC} = 4.5 C _L = 50 pF R1 = 500 s R2 = 500 s T _A = MIN s SN54BCT2244		Ω, Ω,	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH		Y	0.5	3	4.4	0.5	5.2	0.5	4.9	
^t PHL	Α	Y	1.6	4.6	6.3	1.6	7.1	1.6	6.7	ns
^t PZH	G	Y	2.4	6.1	7.7	2.4	9.1	2.4	8.7	
tPZL	u	,	3.9	7.6	9.4	3.9	10.8	3.9	10.4	ns
^t PHZ	G	Y	1.7	5.2	6.9	1.7	8.1	1.7	7.8	
tPLZ		'	2.8	6.5	8.3	2.8	10.9	2.8	9.8	ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.



 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

PRODUCT PREVIEW

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CC7}
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

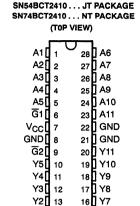
description

The 'BCT2410 is a noninverting 11-bit buffer/line driver specifically designed to drive MOS DRAMs of up to 4 megabits. It is also suitable for use with wide data paths or buses carrying parity. The outputs, which are designed to source 1 mA and sink 12 mA, include $25-\Omega$ series resistors to reduce overshoot and undershoot.

The output-enable inputs $\overline{G}1$ and $\overline{G}2$ are routed internally to a two-input AND gate with active-low inputs. When both $\overline{G}1$ and $\overline{G}2$ are low, the Y outputs are active (high or low logic state). When either $\overline{G}1$ or $\overline{G}2$ is high, the Y outputs are in the high-impedance state.

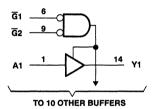
The multiple ground pins of the 'BCT2410 reduce switching noise for more reliable system operation.

The SN54BCT2410 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT2410 is characterized for operation from 0°C to 70°C.



logic diagram (positive logic)

Y1 1 14



15 Y6



D3531, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CC7}
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs

description

The 'BCT2411 is an inverting 11-bit buffer/line driver specifically designed to drive MOS DRAMs of up to 4 megabits. It is also suitable for use with wide data paths or buses carrying parity. The outputs, which are designed to source 1 mA and sink 12 mA, include $25-\Omega$ series resistors to reduce overshoot and undershoot.

The output-enable inputs $\overline{G}1$ and $\overline{G}2$ are routed internally to a two-input AND gate with active-low inputs. When both $\overline{G}1$ and $\overline{G}2$ are low, the Y outputs are active (high or low logic state) and reflect the inverse of the data at the A inputs. When either $\overline{G}1$ or $\overline{G}2$ is high, the Y outputs are in the high-impedance state.

The multiple ground pins of the 'BCT2411 reduce switching noise for more reliable system operation.

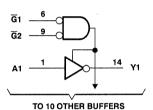
The SN54BCT2411 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT2411 is characterized for operation from 0°C to 70°C.

SN54BCT2411 ... JT PACKAGE SN74BCT2411 ... NT PACKAGE

(TOP VIEW)

A1 [1	28] A6
A2[2	27] A7
A3[3	26	BA [
A4[4	25] A9
A5[5	24] A10
Ğ1[6	23] A11
V _{CC} [7	22	GND
GND[8	21	GND
G2[9	20] Y11
Y5[10	19] Y10
Y4[11	18] Y9
Y3[12	17] Y8
Y2[13	16] Y7
Y1[14	15] Y6

logic diagram (positive logic)





SN54BCT2827B, SN74BCT2827B 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

D2977, APRIL 1987-REVISED JULY 1990

- BiCMOS Design Substantially Reduces Iccz
- Output Ports Have Equivalent 25-Ω
 Resistors, So No External Resistors Are
 Required
- Specifically Designed to Drive MOS DRAMs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Power-Up High-Impedance State
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

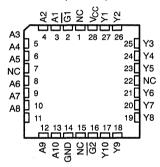
These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so if either $\overline{G1}$ or $\overline{G2}$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

SN54BCT2827B ... JT PACKAGE SN74BCT2827B ... DW OR NT PACKAGE (TOP VIEW)

	1 t	, ,	_
G1[1	24] V _{CC}
A1[2	23] Y1
A2[3	22] Y2
A3[4	21] Y3
A4[5	20] Y4
A5[6	19] Y5
A6[7	18] Y6
A7[8	17] Y7
]8A	9	16] Y8
A9[10	15] Y9
A10[11	14	Y10
GND[12	13] G2

SN54BCT2827B . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

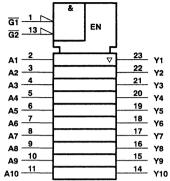
The SN54BCT2827B is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT2827B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

	INPUTS		OUTPUT
G1	G2	Α	Y
L	L	L	L
L	L	Н	н
Н	Х	Х	z
x	Н	Χ	z

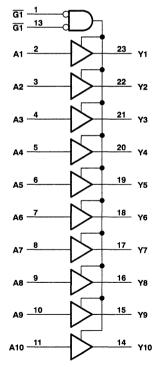
D2977, APRIL 1987-REVISED JULY 1990

logic symbol[†]



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



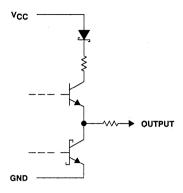
Pin numbers shown are for DW, JT, and NT packages.



SN54BCT2827B, SN74BCT2827B 10-BIT BUFFERS BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

D2977 APRIL 1987-REVISED JULY 1990

schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range (see Note 1)	
Voltage applied to any output in the disabled or power-off state	– 0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to V _{CC}
Input clamp current	
Current into any output in the low state: SN54BCT2827B	24 mA
SN74BCT2827B	24 mA
Operating free-air temperature range: SN54BCT2827B	55°C to 125°C
SN74BCT2827B	0°C to 70°C
Storage temperature range	– 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN5	SN54BCT2827B			SN74BCT2827B			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5 .5	4.5	5	5.5	٧	
VIH	High-level input voltage	2	. /	7/6	2			٧	
VIL	Low-level input voltage		OP	0.8			0.8	٧	
lik	Input clamp current		<u>.c``</u>	- 18			- 18	mA	
ГОН	High-level output current		20	-1			- 1	mA	
loL	Low-level output current	OFFIC		12			12	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

D2977, APRIL 1987-REVISED JULY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN5	SN54BCT2827B SN74BCT2827B					
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
VIK	V _{CC} = 4.5 V,	l _I = 18 mA			- 1.2			- 1.2	V
Voн	V _{CC} = 4.5 V to 5.5 V	IOH = 1 mA	V _{CC} -2			V _{CC} -2			
\/	V 45V	I _{OL} = 1 mA		0.15	0.5		0.15	0.5	V
VOL		I _{OL} = 12 mA		0.35	0.8		0.35	0.8	V
lozh	V _{CC} = 5.5 V,	V _O = 2.7 V			20 🖓			20	μΑ
lozL	V _{CC} = 5.5 V,	V _O = 0.5 V		, P.P.E.	- 20			- 20	μΑ
IOL(sink)	V _{CC} = 4.5 V,	V _O = 2 V	50	16/4		50			mA
I _I	V _{CC} = 5.5 V,	V _I = 5.5 V	PROF	70°	0.1			0.1	mA
Iн	V _{CC} = 5.5 V,	V _I = 2.7 V	200		20			20	μΑ
¹ IL	V _{CC} = 5.5 V,	V _I = 0.5 V	64		- 0.2			- 0.2	mA
10‡	V _{CC} = 5.5 V,	V _I = 2.25 V	- 30		- 112	- 30		- 112	mA
CCL	V _{CC} = 5.5 V,	Outputs open		28	44		28	44	mA
lccz	V _{CC} = 5.5 V,	Outputs open		3.8	6		3.8	6	mA
Ci	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V		5			5		pF
Co		V = 2.5 V 01 U.5 V		8			8		pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2 T _A	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}\text{C}$		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω , R2 = 500 Ω , T_A = MIN to MAX§			UNIT	
			'BCT2827B		SN54BCT2827B		SN74BCT2827B			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	А	Y	0.9	3.6	5.2	0.9	6.6	0.9	6	
t _{PHL}			2	5.1	7.2	2	8.2	2	7.8	ns
^t PZH	G	Y	2.8	5.6	8		(10.7	2.8	10.7	ns
t _{PZL}			5.6	8.9	11	<6.6<	13.7	5.6	12.9	
tPHZ	G	Y	3.2	6.7	9.3	3.2	11.8	3.2	10.9	ns
†PLZ			2.7	5.3	7.1	2.7	9.5	2.7	8.3	113

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuit and voltlage waveforms are shown in Section 1.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, IOS.

SN54BCT2828B, SN74BCT2828B 10-BIT BUS/MOS MÉMORY DRIVERS WITH 3-STATE INVERTING OUTPUTS

D3635, SEPTEMBER 1990

- BiCMOS Design Substantially Reduces ICCZ
- Output Ports Have Equivalent 25-Ω
 Resistors, So No External Resistors Are Required
- Specifically Designed to Drive MOS DRAMs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Data Flow-Thru Pinout (All Inputs on Opposite Side From Outputs)
- Power-Up High-Impedance State
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

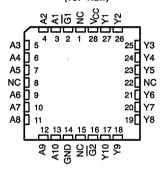
These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so if either $\overline{G1}$ or $\overline{G2}$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

SN54BCT2828B ... JT PACKAGE SN74BCT2828B ... DW OR NT PACKAGE (TOP VIEW)

<u>G1</u> [1 U	24 V _{CC}
A1[2	23 Y1
A2[3	22] Y2
A3[4	21 🛚 Y3
A4[5	20 🛮 Y4
A5[6	19 🛮 Y5
A6[7	18 Y6
A7[8	17 Y7
]8A	9	16 Y8
A9[10	15 Y9
A10[11	14 Y10
GND[12	13 G2

SN54BCT2828B . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

The SN54BCT2828B is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT2828B is characterized for operation from 0°C to 70°C.

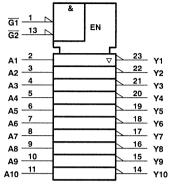
FUNCTION TABLE

	INPUTS		
G1	G2	Α	Υ
L	L	L	Н
L	L	н	L
Н	Х	X	z
X	Н	Х	z

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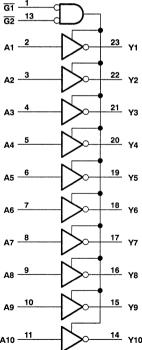


logic symbol†

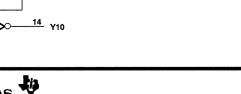


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

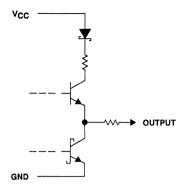
logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to	o 7 V
Input voltage range (see Note 1) – 0.5 V to	o 7 V
Voltage applied to any output in the disabled or power-off state	5.5 V
Voltage applied to any output in the high state	Vcc
Input clamp current	0 mA
Current into any output in the low state	4 mA
Operating free-air temperature range: SN54BCT2828B55°C to 12	25°C
SN74BCT2828B	70°C
Storage temperature range – 65°C to 19	50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage ratings may be exceeded if the input clamp current ratings is observed.

recommended operating conditions

		SN5	SN54BCT2828B		SN74BCT2828B			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage	2			2			٧
VIL	Low-level input voltage			0.8			8.0	٧
lik	Input clamp current			- 18			- 18	mA
Іон	High-level output current			-1			- 1	mA
loL	Low-level output current			12			12	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

SN54BCT2828B, SN74BCT2828B 10-BIT BUFFERS BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING OUTPUTS

D3635 SEPTEMBER 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2828B			SN7	UNIT		
FANAMETER			MIN	TYP†	MAX	MIN	TYP [†]	MAX	OMI
VIK	V _{CC} = 4.5 V,	I _I = - 18 mA			- 1.2			- 1.2	V
Voн	V _{CC} = 4.5 V to 5.5 V	IOH = - 1 mA	V _{CC} ⁻²			V _{CC} ⁻²			٧
V	V _{CC} = 4.5 V	IOL = 1 mA		0.15	0.5		0.15	0.5	V
VOL		I _{OL} = 12 mA		0.35	0.8		0.35	8.0	
^I OZH	V _{CC} = 5.5 V,	V _O = 2.7 V			20			20	μΑ
^I OZL	V _{CC} = 5.5 V,	V _O = 0.5 V			- 20			- 20	μА
IOL(sink)	V _{CC} = 4.5 V,	V _O = 2 V	50			50			mA
l ₁	V _{CC} = 5.5 V,	V _O = 7 V			0.1			0.1	mA
ΊΗ	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
ΊL	V _{CC} = 5.5 V,	V _I = 0.5 V			- 0.2			- 0.2	mA
10 [‡]	V _{CC} = 5.5 V,	V _I = 2.25 V	- 30		- 112	- 30		- 112	mA
^I CCL	V _{CC} = 5.5 V,	Outputs open		28			28		mA
lccz	V _{CC} = 5.5 V,	Outputs open		3.5			3.5		mA
Ci	V _{CC} = 5 V,	$V_{CC} = 5 \text{ V}, \qquad V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$		5			5		pF
Co		V1 - 2.5 V 01 0.5 V		8			8		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

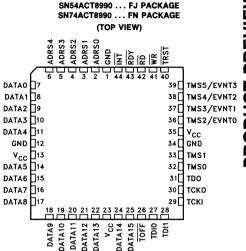


[†] The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, IOS.

General Information
ACL LSI Products 2
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ECL/TTL Translator Products 7
FIFO Products 8
Low-Impedance Line Driver Products 9
Memory Driver Products 10
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Mechanical Data

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- Members of the Texas Instruments SCOPE™ **Family of Testability Products**
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Control Operation of up to Six Parallel **Target Scan Paths**
- Each Include Four Bidirectional Event Pins for Additional Test Capability
- Accommodate Delay to Target of up to 31 **Clock Cycles**
- 30-MHz Operation
- Execute Instructions for up to 232 Clock **Cvcles**
- Scan Data up to 232 Bits in Length
- Inputs are TTL-Voltage Compatible
- Compatible With TI's ASSET™ (Automated System Support for Emulation and Test)
- VLSI Devices, Each Containing Over 34,000 **Transistors**
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- Packaged in 44-pin Plastic and Ceramic **Leaded Chip Carriers**



description

The 'ACT8990 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8990 test bus controller (TBC) is designed to control the operation of an IEEE Standard 1149.1 (JTAG) scan test path by taking input from a host and generating the proper signals to interface with the target device(s). The target(s) can be moved from any stable state to another stable state, loaded with instructions, and resulting test data scanned out to be read by the host. Four EVENT pins are provided to allow real-time interaction between the ACT8990 and its target(s). The EVENT pins can be configured to generate interrupt requests when some user-definable condition is present.

A 32-bit counter can be preset to allow a predetermined number of clock cycles or instruction executions to occur and can be programmed to set an interrupt flag when it reaches a count of zero.

Two 16-bit serial buffers (read and write) are implemented for the host interface.

The SN54ACT8990 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

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SN54ACT8990. SN74ACT8990 TEST BUS CONTROLLERS

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description (continued)

The 'ACT8990 implements all the low-level functions, enabling the host to use higher-level abstraction such as:

- -States of IEEE Standard 1149.1 for control.
- Variables indicating command finish, buffer full or empty for status.
- -Strings and buffers for data.

The target interface may connect without external logic to:

- -Six parallel chains of IEEE Standard 1149.1 targets, each with its own separate TMS signal. The parallel chains share one or two TDI signals, one TDO signal, and one TRST signal and TCK signal.
- Fanout devices that support many targets requiring two separate TMS signals for target selection and target control.
- Local targets (on-board the 'ACT8990) with one TDI input and remote targets with the other TDI input.

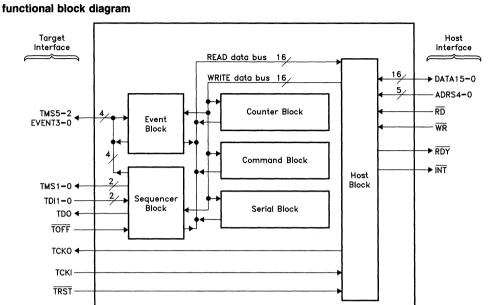
The target interface has four event detectors and two 16-bit event counters to support asynchronous functions. The 'ACT8990 can connect to the target via a retimed link with up to 31 bits of delay. This may be required when the clock rate is high and either the target is at a distance or the link involves fanout or buffer/driver devices. The 'ACT8990 operates with a clock period down to 33 ns (>30 MHz) over the commercial temperature range of 0° to 70°.

The host interface has a 16-bit data bus. The critical host interface timing is independent of the clock period.

The major functions of the 'ACT8990 are controlled by specific commands:

- The STATE command controls the target interface and target state diagrams. It can change the state to any stable state.
- -The EXECUTE command causes the target to execute instructions that have been shifted into it. It uses the Run-Test/Idle state. It can execute instructions for a fixed time or until an event occurs.
- -The SCAN command circulates data among targets and transfers data between the 'ACT8990 and targets. It uses the Shift-IR or Shift-DR states. It uses the read and write buffers, which can each hold two 16-bit data words.





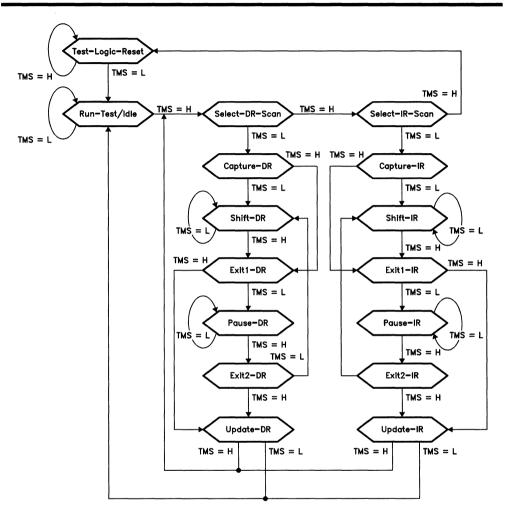


FIGURE 1. TAP STATE DIAGRAM

PRODUCT PREVIEW

state diagram description

The 'ACT8990 controls 1149.1 targets by generating and accepting TMS, TDO and TDI signals compatible with the IEEE Standard 1149.1 state diagram shown in Figure 1. There are six stable states (indicated by a looping arrow) and ten unstable states (indicated by two exiting arrows) in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. Only one register should be manipulated at a time.

Test-Logic-Reset

In this state, the test logic is inactive, and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK, causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO enables to the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO enables to a low level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this state only.

state diagram description (continued)

Capture-IR

The instruction register is preloaded with the IR status word and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR. TDO goes from the high-impedance state to the active state.

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

The latches shadowing the instruction register are updated with the new instruction.

terminal descriptions

The signal pins on the 'ACT8990 (Terminal Function Table) are separated into two main categories: host interface and target interface.

host interface terminals

DATA15-0

These bidirectional pins form the 16-bit interface between the host and the controller. Information is written to and read from the registers via the DATA15-0 pins.

ADRS4-0

The address pins are used to select the register to be written to or read from.

RD

 $\overline{\text{RD}}$ is the strobe for reading data from a selected register. When low, $\overline{\text{RD}}$ acts as the output enable for the DATA15-0 bus.

WR

WR is the strobe for writing data to a selected register.

INT

This output has high-impedance capability and is used to output an interrupt signal to the host.

RD

RDY is asserted low during recovery time from a read or write operation or when certain accesses to the 'ACT8990 are not allowed.

TRST

A software reset occurs when TRST is asserted low.

TOFF

All I/O and output pins are in the high-impedance state when TOFF is low.



terminal descriptions (continued)

target interface terminals

TD11-0

The test data in pins are the serial input pins for shifting test data from the target(s) into the 'ACT8990.

TDO

The test data out pin is the serial output from the 'ACT8990.

TMS1-0

The test mode selects are used to interface the TBC to target(s) and direct them through their states.

TCKI

Operation of the 'ACT8990 is synchronous to the TCKI input.

TCKO

Test clock out is the buffered TCKI signal and is distributed to the target(s).

EVNT3-0/TMS5-2

These pins are configurable to act as event pins or test-mode-select pins. As event pins, they can be set to output interrupt flags based on user-definable input conditions. As test-mode-select pins, they can control up to four additional scan paths.

TERMINAL FUNCTIONS

SIGNAL	GROUP	TYPE	DESCRIPTION
DATA15-0	Host Interface	1/0	Data Bus
ADRS4-0		Input	Address Bus
RD		Input	Read Strobe
WR		Input	Write Strobe
RDY		Output	Ready
INT		Output	Interrupt
TMS1-0		Output	Test Mode Select
EVNT3-0/TMS5-2		1/0	Event Pins/TMS
TDO		Output	Test Data Out
TCKO		Output	Test Clock Out
TCKI	Target Interface	Input	Test Clock In
TDi1-0	7	Input	Test Data In
TOFF		Input	Test Off
TRST		Input	Test Reset
Vcc			5 V Power
GND	Power		Ground

terms

JTAG

The Joint Test Action Group is the originator of IEEE Standard 1149.1.

SCOPE

System Controllability and Observability Partitioning Environment. This is the family name for Texas Instruments testability products.

host

The device directing the activity of the 'ACT8990 (processor-based system), typically a personal computer or other workstation.



SN54ACT8990, SN74ACT8990 TEST BUS CONTROLLERS

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terms (continued)

target

One or more devices controlled by the 'ACT8990 through its target interface. The target(s) must be IEEE Standard 1149.1-compatible.

fanout device

This is a device that allows the 'ACT8990 to control many parallel targets.

clock

The system test clock used by the controller and its target(s). The clock is input on TCKI and output on TCKO.

off and on

Output and bidirectional buffers are considered "off" when in a high-impedance state and "on" when in the active state and able to output a logic high or low level.

direct link

This is a connection between the 'ACT8990 and targets that involves delaying the target interface signals by less than one clock period. It can either be a "pin-to-pin" connection or a connection via "buffer/driver" devices.

retimed link

This is a connection between the 'ACT8990 and targets that involves delaying the target interface signals by one or more clock periods. It typically involves flip-flops distributed along a cable, within a fanout device, or on a board.

major command

Selected through the major command register, major commands instruct the controller to perform operations on the target(s) such as scan, state change, or the execution of an instruction. Major commands typically take many clock cycles to complete. There are three major commands: STATE, EXECUTE, and SCAN.

dead and alive

Major commands are dead, and the alive status bit (status1 register bit 15) is zero when the state machine implementing it is inactive. They are alive, and the alive status bit is one when the state machine is active.

awake and asleep

Alive major commands may be in one of two conditions. If awake, the awake status bit (status1 register bit 14) is one and the command actively performs its functions or ends. Otherwise, it is asleep, and the awake status bit is zero.

begin, suspend, resume, and end

Major commands begin when they become alive, suspend when they become asleep, resume when they become awake, and end when they go to the end state.

finish

Major commands finish when they become dead after reaching the end state and setting the finish flag.

minor command

Selected through the minor command register, minor commands instruct the controller to perform some functions within itself, such as SET, RESET, CLEAR or initiate a major command. Minor commands typically take few clock cycles to complete.



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terms (continued)

null registers and null bits

These are registers and bits where no logic is implemented. Writes to them are ignored, and reads from them return zeroes.

sequence acceptor

The sequence acceptor accepts inputs from the TDI1-0 pins and link delay register and decodes them to determine which state is being returned from direct and retimed links.

link delay register

The link delay register uses the mode-source signal from the generator to produce a delayed-mode-source signal for the sequence acceptor. It models the delay in a direct or retimed link.

sequence generator

The sequence generator generates outputs on the TDO and TMS5-0 pins and to the link delay register to control the target state.

passing zero

A counter passes zero when it is operated at the all-zeroes value. Its value changes to all ones (if it decrements) or is updated (if it reloads). Other actions may also occur.

recirculate data

Data that was previously received from the target and is sent back by the shifter-FIFO.

overwrite data

Data sent to the target from the write buffer to replace data previously received from the target.

operation

clock

The timing of most of the 'ACT8990 functions is synchronous to the clock signal (TCKI). This signal is output on the test clock output (TCKO) to provide a signal that has undergone delays due to output buffers similar to those of the target interface outputs. TCKO may also be set to one, zero, or the high-impedance state by the clock format, clock data, and clock off bits in the control3 register.

reset

The two methods of initializing the 'ACT8990 are hardware reset and software reset. The reset timing is detailed in Figure 2.

Asserting the active-low TRST input causes a hardware reset that initializes the output and bidirectional pins:

- -DATA15-0, INT, RDY, and TMS5-2/EVENT 3-0 take on the high-impedance state.
- -TDO and TMS1-0 output the logic high level.
- TCKO outputs the clock.

The effects of TRST on DATA15-0, INT, RDY and EVENT3-0 are immediate and asynchronous to the clock, while its effects on TMS1-0, TDO and TCKO are synchronous, occurring a few periods after TRST goes low. This means that during the initial power-on reset by TRST, these four signals are undefined for a few clock periods but, during later assertions of TRST, the changes on these pins are synchronous.

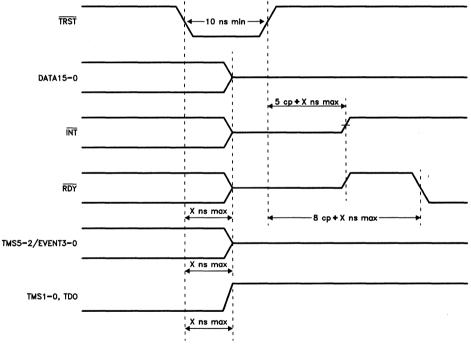
Taking TRST high causes hardware reset to end and software reset to begin. Note that if TOFF and TRST are both asserted, then all output and bidirectional pins are in the high-impedance state.

operation (continued)

A software reset occurs automatically after the hardware reset ends or when a RESET command is written to the minor command register. It initializes all internal logic as well as the output and bidirectional pins synchronously to the clock:

- -The INT and RDY pins output the logic high level.
- -The TMS5-2 and EVENT3-0 pins take on the high-impedance state.
- -The TDO and TMS1-0 pins output the logic high level.
- -The TCKO pin outputs the clock.
- -The major commands become dead.
- The data buffers and shifter-FIFO are emptied.
- -Counter1, counter20 and counter21 bits are all set to zero.
- -The host interface register bits are all set to zero.

Hardware reset requires up to 5 clock periods after TRST is taken high. Software reset requires up to 8 clock periods after TRST is taken high or up to 8.5 clock periods after the rising edge of WR.



"cp" is the clock period.
"X" is a value to be determined.

FIGURE 2. RESET TIMING DIAGRAM



architecture

The 'ACT8990 is constructed internally from six logic blocks, thirty-eight I/O buffers, and separate 16-bit read-data and write-data buses. This is summarized in the functional block diagram.

host interface

The host interface is constructed from the host block shown in Figure 3. The host block is the host-interface data-transfer and control logic. It also holds the hardware and software reset logic. Its four sections are:

- The data bus logic: transfers data between the data bus pins and the independent internal 16-bit read and write data buses.
- The address and access logic: operates during accesses by the host. It synchronizes the host signals to the clock, selects the registers to be accessed and controls the data bus logic and asserts RDY during the recovery time.
- -The interrupt logic: asserts the INT pin based on the interrupt flag and enable signals.
- -The reset logic: generates asynchronous and synchronous reset control signals in response to the assertion of the TRST pin or writing RESET commands.

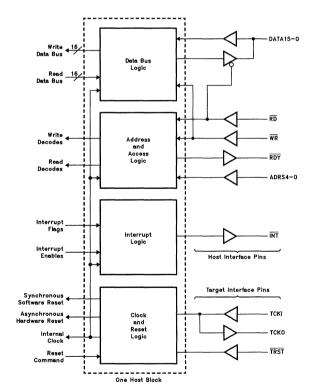


FIGURE 3. HOST INTERFACE



architecture (continued)

interrupts via the host interface

The 'ACT8990 asserts INT to make an interrupt request to the host when matching flag status bits and enable control bits are set. The flags are set by the 'ACT8990 when specific events occur. They are set or cleared by the host, either individually by SET or CLEAR commands or all at once by a RESET command. The enable bits are used by the host to select which flags may generate interrupt requests.

accesses via the host interface

The host asserts $\overline{\text{WR}}$ or $\overline{\text{RD}}$ to write or read registers via the host interface. The host interface logic is designed so that the assertion of $\overline{\text{WR}}$ and $\overline{\text{RD}}$ can be asynchronous to the clock. The write and read timing is detailed in Figures 4 and 5.

WR is the strobe for the DATA15-0 and ADRS4-0 pins, which are sampled on its rising edge. Their setup and hold times are relative to this edge. The sampled address and data are synchronous to the clock and used to load the selected register.

 $\overline{\text{RD}}$ is the output enable for the DATA15-0 pins. The setup and hold times for $\overline{\text{RD}}$ and ADRS4-0 are relative to the time at which the host samples DATA15-0.

RDY is asserted during the recovery time following the rising edge of RD or WR.

recovery time

The host must not access registers during the recovery time in which $\overline{\text{RDY}}$ is asserted. This occurs when internal control signals are generated that require several clock periods to become synchronous to the clock and complete their operations. The recovery time rules are:

- -Writes are ignored while a write is completing and reads give invalid data while a write to the same address is completing. This requires up to 3.5 clock periods from the rising edge of WR to its next rising edge or to the falling edge of RD.
- Reads from the status and capture registers give invalid data while a minor command is completing. This requires up to 4.5 clock periods from the rising edge of \overline{WR} to the falling edge of \overline{RD} .
- Reads from the read buffer register give invalid data while a previous read is completing. This requires up to 4.5 clock periods from the rising edge of RD to its next falling edge.
- Writes are ignored and reads give invalid data during a software reset initiated by a RESET command.
 This requires up to 8.5 clock periods from the rising edge of WR to its next rising edge or to the falling edge of RD.
- -Writes are ignored and reads give invalid data during hardware and software resets initiated by asserting TRST. This requires up to 6.5 clock periods from the rising edge of TRST to the rising edge of WR or the falling edge of RD.

These rules may be met:

- Explicitly by the host software spacing accesses or polling RDY.
- Implicitly by the host hardware using RDY to delay later accesses until the recovery time is ended.

RDY is asserted asynchronously when TRST is taken high or on the rising edge of RD or WR, then later negated after a rising edge of the clock.



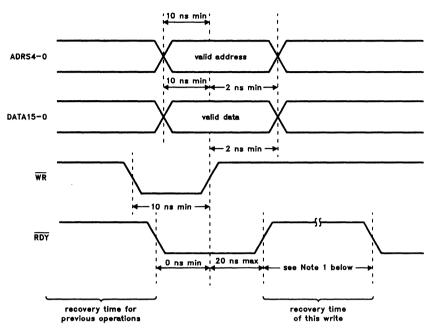


FIGURE 4. HOST WRITE TIMING DIAGRAM

NOTE 1:

NOTE 1:

Register recovery time is 3.5 cp + 30 ns max.

Minor command recovery time is 4.5 cp + 30 ns max.

Software reset recovery time is 8.5 cp + 30 ns max.

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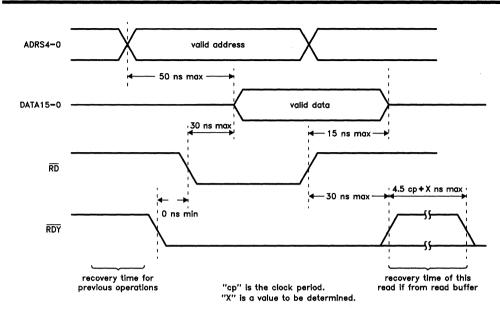


FIGURE 5. HOST READ TIMING DIAGRAM

register set

The 'ACT8990 has five address inputs (ADRS4-0) to select any one of the twenty-four 16-bit registers. When ADRS4-0 has values 00000-10111, the host is able to access a register via DATA15-0. When ADRS4-0 has values 11000-11111, then writes are ignored and all zeroes are read.

The 24 registers are listed in Table 3. For the convenience of the host, functions are partitioned as control and status, then arranged on byte boundaries to minimize the register space. Some register bits contain functions used only during manufacturing test.

The design of null registers and null bits is such that writing to them has no effect and reading from them obtains all zeroes.

control and status functions

The host configures the 'ACT8990 by writing to the control and update registers before, during, or after commands. These registers can be freely accessed by the host as their bits are not altered by the 'ACT8990.

The host examines the 'ACT8990 by reading the status and capture registers. Before reading them, the host must first write an OPERATE2 command to capture information in the status and capture registers. These register bits then indicate the 'ACT8990 state at the time of the command. The reason for this is that the reading of these registers is asynchronous to the changes in the 'ACT8990 internal flags and signals which occur every clock period. Thus the flags and signals cannot be read directly. The OPERATE2 command logic captures the values of the flags and signals in the clock period in which it executes.



register set (continued)

minor commands

Minor commands are begun by the host when it writes to the minor command register. They instruct the controller to perform some functions within itself. These commands require only a few clock periods and the $\overline{\text{RDY}}$ pin is asserted while they are alive. The minor commands are as follows:

- -The CLEAR0/1 and SET0/1 commands modify selected interrupt flags.
- -The OPERATEO/1 commands affect the operation of major commands.
- The OPERATE2 command operates functions related to the status registers and counters.
- The RESET command resets selected functions or the entire 'ACT8990.

major commands

Major commands are selected by the value in the major command register. They instruct the controller to perform operations on the target(s). They are begun by the host when an OPERATEO/1 command is written to the minor command register or, if the major command is the EXECUTE command, it may be begun by an event detection. The major commands may require many clock periods. They affect the awake and alive status bits (status1 register bits 14 and 15). When they finish, the finish flag (status0 register bit 15) is set and an interrupt may occur.

The STATE command controls the target state without performing any other explicit action. It can change the state from its current stable state to any stable state. It is used to implement:

- Exiting and entering the Test-Logic-Reset state.
- Additional state changes between other EXECUTE and SCAN commands.
- Context switches between parallel targets.
- -Context switches between the data and control paths of a fanout expander.

The EXECUTE command makes the target execute instructions that have been shifted into it. It uses the Run-Test/Idle state. The instructions may be executed for up to 2^{32} clock periods. They can be executed for a fixed time or until an event occurs. Their execute times may also be benchmarked.

The SCAN command circulates data among targets and transfers data between the 'ACT8990 and targets. It uses the Shift-IR or Shift-DR states. The data may be up to 2^{32} bits long. During these operations, the read and write buffers can each hold up to two 16-bit words of data at a time.

counter1

This synchronous 32-bit counter is used to count the number of execute states sent by EXECUTE commands and data bits shifted by SCAN commands. It is configured by the bits in the control8 register and can be used independently of the commands.

The counter1 update registers and the capture registers load and store this counter. The host writes initial values to the update registers and reads current and final values from the capture registers. Reset fills counter1 and its update and capture registers with zeroes.

Counter1 can be loaded from the update register:

- By an OPERATE2 command, usually before EXECUTE and SCAN commands.
- When it passes zero, if the counter1 reload control bit is set.

Counter1 can be stored to the capture registers by an OPERATE2 command, usually during and after EXECUTE and SCAN commands.

register set (continued)

Counter1 is operated:

- By an OPERATE2 command.
- By a SCAN command sending scan states.
- As decided by the counter1 operate control bits:
 - Not at all.
 - When sending execute states during an EXECUTE command.
 - Throughout an EXECUTE command.
 - When a selected event detector detects an event on an EVENT pin directly or via counter20/21.
 - When a low level occurs on a selected EVENT pin.
 - When a high level occurs on a selected EVENT pin.

The effects of counter1 when passing zero are:

- -SCAN commands are ended. The counter1 scan flag is sent and an interrupt may occur.
- EXECUTE commands are either not affected, suspended or ended as decided by the counter1 pause and end control bits. The counter1 execute flag is set and an interrupt may occur.
- If neither a SCAN nor EXECUTE command is alive, the counter1 execute flag is set and an interrupt may occur.

When an EXECUTE or SCAN command ends or aborts, the difference between the initial value written to the counter1 update registers and final value read from the capture registers is the number of execute states sent or data bits shifted. A later command may complete the actions of this command if the counter is not loaded again.

data buffers and shifter-FIFO

The target's data and instruction registers are operated on as a number of modules each containing a string of data. These strings are accessed with one or more SCAN commands that operate the data buffer and shifter-FIFO functions of the 'ACT8990. The data buffers and shifter-FIFO are configured by the values of the bits in the control4 register. These functions are shown in Figure 9.

On the host interface, these strings are handled as parallel data by the data buffers. On the target interface, the strings are handled as serial data by the shifter-FIFO. The data buffers and shifter-FIFO are loaded and stored by the transfer functions that are described in the next section.

The write buffer is accessed via the write buffer register. It is used by the SCAN commands to pass data to TDO. The read buffer is accessed via the read buffer register. It is used by the SCAN commands to store data from TDI via the shifter-FIFO. Reset empties the data buffers.

The data buffers can each hold up to two 16-bit words of data. Their status is indicated by the write empty inverted, read full, write OK inverted and read OK status bits. These data buffers and their status bits are operational at all times. Thus, the write buffer can be written to before a SCAN command begins and the read buffer can be read from after a SCAN command finishes.

When the write buffer1-0 control bits are 00, 01, or 10, the write buffer is unused. This reduces writes on the host interface as the send data is not taken from the buffer. Instead, send data is either all zeroes, all ones, or recirculate data (data received from the target by the shifter-FIFO). Options 00 and 01 provide an efficient way of sending the BYPASS and EXTEST instructions. Option 10 provides an efficient way of bypassing strings that are of no interest. In option 11, the write buffer holds data that the host writes.

On the target interface, the target data and instruction registers are in series with the shifter-FIFO. The shifter-FIFO is an extra module containing a null string. This module is positioned such that SCAN commands operate on it first before the target strings. An extra SCAN command may bypass this null string by recirculating it before other SCAN commands access all the strings. Reset fills the shifter-FIFO and its null string with ones. These features of the architecture are shown in Figure 6.



register set (continued)

The shifter-FIFO provides serial-to-parallel conversion and compensates for the delay that occurs to returned data when a retimed link connects the 'ACT8990 and targets. If allows SCAN commands to scan continuously without sleeping even though there is a delay between the sending of data bits on TDO and the return of matching data bits on TDI. The length of the shifter-FIFO sets the upper limit on the length of the retimed links for continuous scanning. The shifter-FIFO can be configured as 16 or 32 bits long by the serial length control bit.

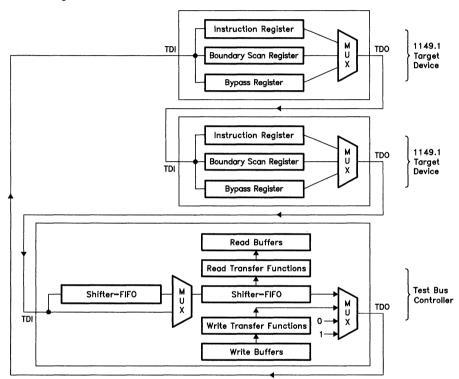


FIGURE 6. SCAN PATH OF THE TEST BUS CONTROLLER AND TARGET(S)

transfer functions

The strings of data in the shifter-FIFO, the target data and instruction registers may represent arithmetic quantities. In this case, the format of the strings may be interpreted as LSB first (least significant bit nearest TDO) or MSB first (most significant bit nearest TDO). These features of the architecture are shown in Figure 7.

The transfer functions convert data between the two serial formats used by the target data and instruction registers and the one parallel format used by the host. They are configured by the values of the bits in the control4 register. Physically, the transfer functions manipulate the bits in strings as they are passed from the serial-FIFO to the read buffer and from the write buffer to TDO. These functions are shown in Figures 6 and 9.



transfer functions (continued)

In the data buffers, bits 15 and 0 always represent the most and least significant bits in the word, respectively. The data buffers may hold whole words of 16 bits or partial words of less than 16 bits. When the read buffer holds a partial word, the upper bits that are not part of it are zero. When the write buffer holds a partial word, the upper bits that are not part of it are ignored.

The transfer format control bit (bit 11 of the control4 register) configures the transfer functions for operation with LSB-first or MSB-first strings:

- LSB-first format strings are passed between the host and target least significant word and bit first. Bit 0 of whole and partial words in the data buffers is sent and received first. The last word passed through the data buffers may be a partial word if the string is not a word multiple. In the target, the bit nearest TDO is considered the least-significant bit.
- MSB-first format strings are passed between the host and target most significant word and bit first. Bit 15 of whole words and a lower bit of partial words in the data buffers is sent and received first. The first word passed through the data buffers may be a partial word if the string is not a word multiple. In the target, the bit nearest TDO is considered the most-significant bit.

The value of the transfer format bit has no direct effect on data in the data buffers or shifter-FIFO. It only affects the formatting of data when it is loaded or stored. If different modules in the target contain data in different formats, they can be accessed by separate SCAN commands and the transfer format switched between commands.

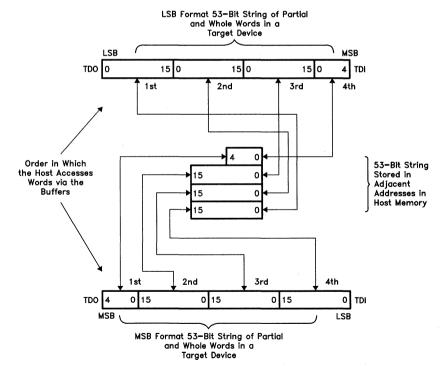


FIGURE 7. FORMAT OF STRINGS IN TARGET DEVICES AND THE HOST MEMORY



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target interface

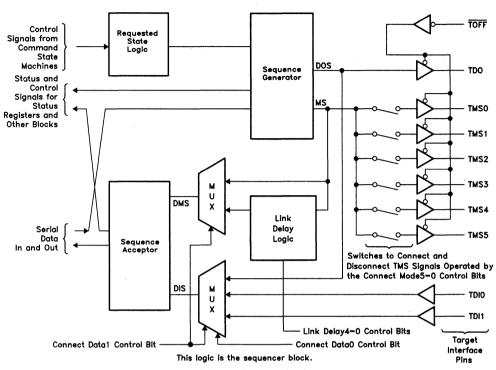
The target interface is constructed from the sequencer block and the event block shown in Figures 8 through 10. They are detailed below:

The sequencer block is the target interface state machine. It is used by the major commands and has four sections:

- The requested state logic uses signals from the command blocks (command decode logic and major command state machines) to request that the sequence generator hold or change its state.
- The sequence generator is directed by the requested state logic to generate sequences on TMS5-0, output data on TDO, and generate the target interface state3-0 status bits on status2 register.
- -The link delay logic generates a delayed-mode source for use by the sequence acceptor, from the mode source in the sequence generator, that matches the returned signals from the link delay logic.
- The sequence acceptor accepts data in source (DIS) and delayed mode source (DMS) signals and uses them to decide what state is being returned. It inputs data from the TDI1-0 input to the serial block (shifter-FIFO) (Figure 9). It indicates to the command block (Figure 10) (command state machines, counter control and status logic, and serial control and status logic) when temporary, scan, and execute states are being returned.

The event block (Figure 11) is used by the EXECUTE commands. It has three sections:

- The four event detectors are used for synchronization, masking, edge, and level detection logic for the EVENT pins and counter20/21. They output event detect flags for the command block (Figure 10) (command state machines and status logic).
- -The event counter logic is the counter2 update registers (counter20 and counter21) and their control logic.
- The event input/output logic turns the output buffers on or off and outputs a value based on the countrol5 register event on and event data control bits. It inputs values to the status1 register event level status bits.



[&]quot;MS" is the mode source signal.

FIGURE 8. SEQUENCE BLOCK

[&]quot;DMS" is the delayed-mode source signal.

[&]quot;DOS" is the data-out source signal.

[&]quot;DIS" is the data—in source signal.

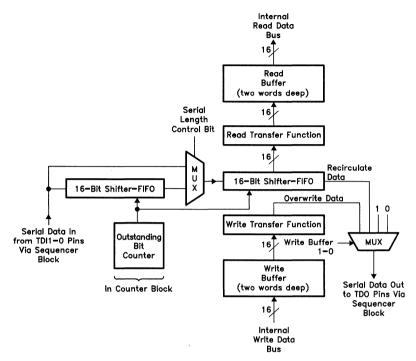


FIGURE 9. SERIAL BLOCK

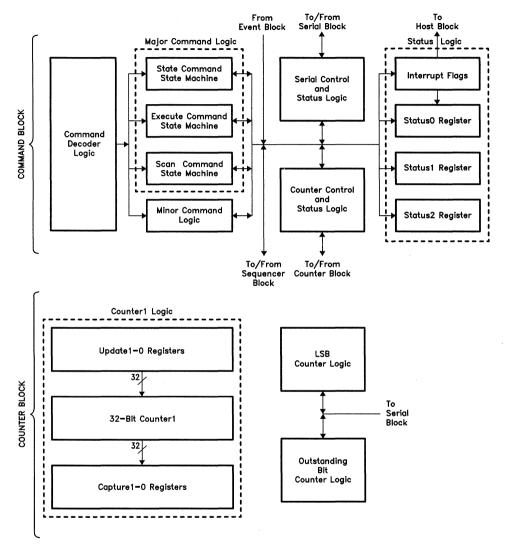
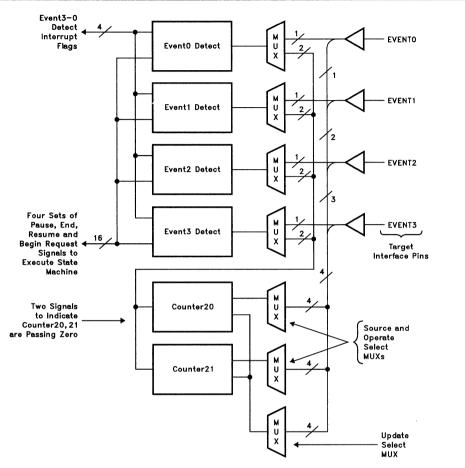
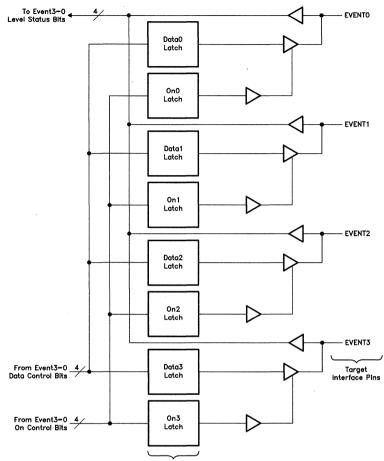


FIGURE 10. COMMAND AND COUNTER FUNCTIONS



This logic is part of the event block.

FIGURE 11. EVENT DETECTORS AND COUNTERS



The Latches Retime the Outputs to the falling edge of the Clock

This logic is part of the event block.

FIGURE 12. EVENT INPUT AND OUTPUT LOGIC

control functions

The control logic for the majority of the commands included in the 'ACT8990 is in the command and counter blocks (Figure 10). The command block has six sections:

- The command decode logic holds the major command opcodes while the commands are executed. It also selects which state machine to activate.
- The major command state machines are state machines for the STATE, EXECUTE and SCAN commands.



control functions (continued)

- -The minor command logic generates control signals based on minor commands.
- The counter control and status logic outputs control signals and inputs status signals for the counter block.
- The serial control and status logic outputs control signals and inputs status signals for the serial block (Figure 9).
- -The status logic consists of the interrupt flags and status2-0 registers.

The counter block is the counter used by the major commands. It has three sections:

- -The counter1 logic consists of the counter1 update registers, counter1, and the capture registers. Signals from the command block (counter control and status logic) update and operate this counter during SCAN and EXECUTE commands.
- -The LSB counter logic is two internal 4-bit counters that track the count of the least-significant bits of data sent and received during SCAN commands.
- -The outstanding bit counter is an internal 6-bit counter that tracks the difference in the number of bits sent and returned during SCAN commands and temporary states sent and returned during STATE and EXECUTE commands.

data transfer functions

The data transfer logic for the SCAN command is in the serial block (see Figure 9). The serial block consists of the data buffers, shifter-FIFO, and transfer functions required by the SCAN commands. It has three sections:

- The data buffers are the read and write buffers that are each 16-bits wide and two levels deep. They are used to read recirculate data and write overwrite data during SCAN commands.
- The shifter-FIFO is a 16/32 bit shifter and 16/32-to-1 multiplexer that operates as a shifter-FIFO to send recirculate data.
- The transfer functions are a 16-to-1 multiplexer that provides the write transfer function and a partial barrel shifter and mask logic that provides the read transfer function.

target interface configuration

The reset value of the target interface is the same whether the device is in IEEE Standard 1149.1 mode or TI internal manufacturing test mode. After reset, the control registers configure the 'ACT8990 for immediate operation via the TMS1-0 pins. Changes to register values to alter the configuration should be made before major commands are executed. The register bits of concern are:

- -If the machine format1-0 bits of the control3 register are 00, the target interface state machines are formatted for IEEE Standard 1149.1 operation. When 01, 10 or 11 they are configured for TI internal manufacturing test.
- If the out format1-0 bits of the control3 register are 00, the target interface pins are formatted for IEEE Standard 1149.1 operation. When 01, 10 or 11 they are configured for TI internal manufacturing test
- If the mode format53, 42, 31 and 20 bits of the control3 register are 1, the matching TMS/EVENT pin outputs TMS signals. When 0, the pin inputs or outputs EVENT signals.

target interface internal signals

The 'ACT8990 has several important internal signals (Figure 8) that are related to those output and input on the target interface pins:

- -The mode source is the test-mode-select signal that is generated internally and output on TMS5-0.
- -The delayed mode source is the delayed test-mode-select signal that is generated and accepted internally.



data transfer functions (continued)

- The data out source is the test-data-out signal output on TDO or looped back to the data in source.
- -The data in source is the signal selected as the test-data-in signal. It is the data out source of the sequence generator or the TDI1 or TDI0 pins.

target interface pins

The target interface timing is detailed in Figures 13 through 16. The target interface pins are as follows:

- The TCKI and TCKO pins input and output the test clock signal used by targets.
- The TDO pin is the test-data-out signal used to send data to targets.
- -The TDI1-0 pins are test-data-in signals used to receive data from targets.
- -The TMS5-0 pins are test-mode-select signals used to control the target test logic.
- -The EVENT3-0 pins input and output extra signals.
- -The TOFF pin is the test-off signal that, when low, turns the target interface output buffers off.
- -The TRST pin is the test-reset signal that, when low, turns the host interface output buffers off and resets the 'ACT8990.

TMS/EVENT pins

The four TMS/EVENT pins are shared by the TMS5-2 outputs, the EVENT3-0 I/Os, and by counter20 and counter21. The mode format53, -42, -31, and -20 control bits (control3 register bits 3-0) configure these pins as TMS or EVENT signals.

When configured as TMS5-2 outputs, they can be turned off together by the mode off control bit (control3 register bit 6). They are used as TMS5-2 outputs controlled by the connect mode5-2 control bits (control2 register bits 5-2).

When configured as EVENT3-0 inputs and outputs, they can be turned off together by the event off control bit (control3 register bit 7). They are used as:

- General purpose I/O bits. Each input pin is readable from a status1 register bit. Each output buffer's data and the on/off condition is decided by the event data and the event on control bits in the control5 register. They can be used as inputs or push-pull, open-drain or open-source outputs.
- Event detectors. Each EVENT input has an event detector controlled by eight control6 or control7 register bits. They detect single synchronous or asynchronous events.
- Event counters. Counter20 and counter21 can be configured to count asynchronous edges on EVENT inputs. Passing zero may be detected by the event detectors.

target interface states

The target interface has a set of states indicated by sequences on the TMS5-0 outputs. The current state of the target interface can be read from the target interface state3-0 bits in the status2 register. These states and sequences allow the 'ACT8990 to control the target.

The target interface has two state groups:

- Temporary states are those states that the target remains in for one clock period only, then goes to one of two other states depending on the value of TMS.
- Stable states are those states that the target can remain in, or go to another state from, depending on the value of TMS.



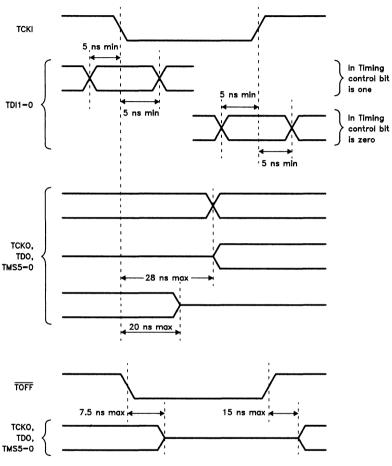


FIGURE 13. TIMING DIAGRAM

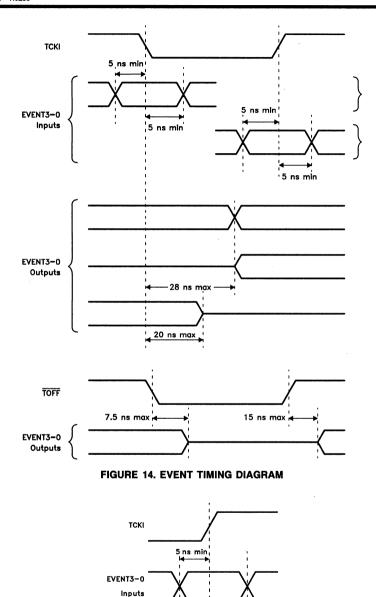


FIGURE 15. ASYNCHRONOUS EVENT TIMING DIAGRAM



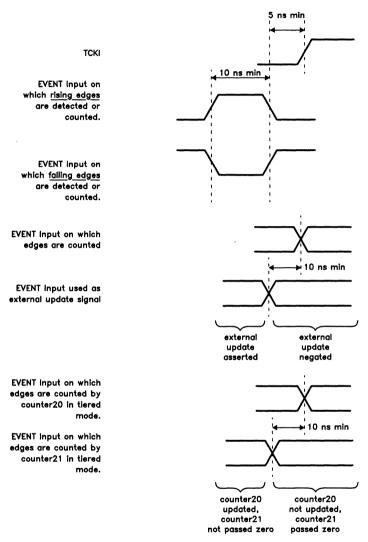


FIGURE 16. ASYNCHRONOUS EVENT EDGE TIMING DIAGRAM



event detection and counting

The detection of events occurring on the EVENT pins is either done by the event detectors alone or by counter20 and counter21 in combination with the event detectors.

event detectors

The four event detectors are shown in Figure 11. Each is controlled by eight bits in the control7 and control8 registers and has an event detect interrupt flag. Each has a matching EVENT pin on which it can detect the following:

- Synchronous events with a repetition rate less than once per 2 clock periods may be detected on the matching EVENT pin.
 - -One followed by a zero (synchronous falling edge).
 - -Zero followed by a one (synchronous rising edge).
 - -Zero followed by a zero.
 - -One followed by a one.
- Asynchronous events with a repetition rate less than once per 3 clock periods may be detected on the matching EVENT pin.
 - Falling edge.
 - Rising edge.
- Asynchronous events counted by counter20 and counter21. These counters are updated and operated in response to asynchronous levels and edges on any of the EVENT pins as configured by the control9 register. Many asynchronous events may be detected each clock period since counter updating and operation are not tied to the clock.
 - -Counter20 passing zero.
 - -Counter21 passing zero.

Event detection is always masked when the EVENT pin is in the output mode. It may also be selectively masked, as decided by the detect mask control bits, (control6 register bits 5 and 13) when scan, pause, and the associated temporary states (capture, exit1, and exit2) are returned.

When an event is detected, the following actions may occur:

- Interrupt requests may be issued to the host by setting an event detect flag.
- EXECUTE commands may be affected by setting the suspend, end, resume, or begin request status bits (status1 register bits 8-11).
- Counter1 may be operated.

event counters

Counter20 and counter21 are asynchronous 16-bit counters as shown in Figure 11. They are configured by bits in the control9 register. They are used to count asynchronous events on the EVENT pins. Counter20 or counter21 passing zero may be detected by an event detector that can request an EXECUTE command to suspend, end, resume, or begin. They can also be used independently of commands.

The counter2 update registers are used to load the counters with initial values. These counters have no capture registers, so their values cannot be read by the host. Reset causes counter20, counter21 and their update registers to be filled with zeroes.

Because these counters are asynchronous, changes in the values of the control9 register bits may create logical hazards that, in turn, cause spurious operation of the counters. This can be avoided by holding them in the update condition during configuration changes. The update inverted control bits are set to zero and the other bits are changed, then the update inverted bits are set to one.



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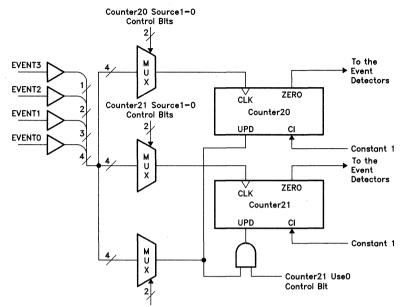
event detection and counting (continued)

The event counters are updated from the counter2 update registers as follows:

- Both counters are loaded by an OPERATE2 command before EXECUTE commands are begun.
- Either counter20 only, or both counter20 and counter21, are loaded by an external update. This is a selected level on an EVENT as configured by the external update enable, polarity and source1-0 control bits.
- When their individual update inverted control bits are zero.
- By the 'ACT8990 if their individual reload control bits are set when the counter passes zero.

The event counters are incremented when a selected edge on an EVENT pin occurs, as configured by their individual reload, operate and source1-0 control bits. Also, they are used as separate or tiered 16-bit counters or concatenated as one 32-bit counter as selected by the counter2 use1-0 control bits (control9 register bits 10-9):

- Separate use means events are counted as decided by the control9 register and OPERATE2 command bits. They are independent 16-bit counters (see Figure 17).
- -Tiered use is similar to separate use except that counter20 is held updated until the first time counter21 passes zero (see Figure 18).
- Concatenated use means events are counted as decided by the control9 register and OPERATE2 command bits only. They are a single 32-bit counter (see Figure 19).



External Update Source1-0 Control Bits

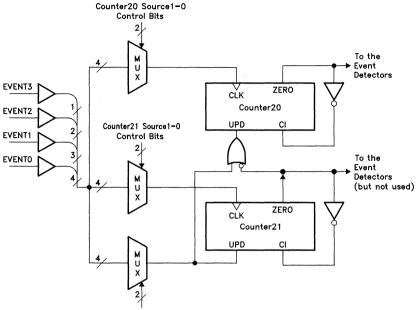
CLK is the counter clock input.

UPD is the counter asynchronous update input.

CI is the counter carry input.

ZERO is the counter passing-zero output.

FIGURE 17. SEPARATE USE OF COUNTER20 AND COUNTER21



External Update Source1-0 Control Bits

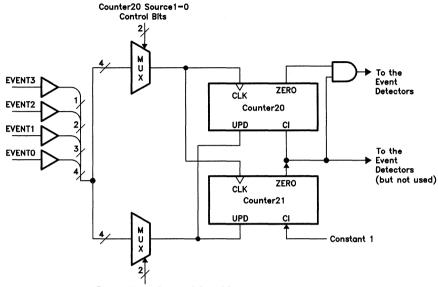
CLK is the counter clock input

UPD is the counter asynchronous update input

CI is the counter carry input

ZERO is the counter passing-zero output

FIGURE 18. TIERED USE OF COUNTER20 AND COUNTER21



External Update Source1-0 Control Bits

CLK is the counter clock input

UPD is the counter asynchronous update input

CI is the counter carry input

ZERO is the counter passing-zero output

FIGURE 19. CONCATENATED USE OF COUNTER20 AND COUNTER21

ter listing			
ADRS4-0	REGISTER NAME	REGISTER USAGE	ACCESSIBILITY
00000	Control0	Interrupt enable control	Read-write
00001	Control1	Host and test control	Read-write
00010	Control2	Target interface control	Read-write
00011	Control3	Target interface control	Read-write
00100	Control4	Target interface control	Read-write
00101	Control5	Event output control	Read-write
00110	Control6	Event detector control	Read-write
00111	Control7	Event detector control	Read-write
01000	Control8	Counter1 control	Read-write
01001	Control9	Counter20/Counter21 control	Read-write
01010	Minor Command	Minor commands	Read-write
01011	Major Command	Major commands	Read-write
01100	Counter1 Update0	Counter1 update	Read-write
01101	Counter1 Update1	Counter1 update	Read-write
01110	Counter2 Update0	Counter20 update	Read-write
01111	Counter2 Update1	Counter21 update	Read-write
10000	Status0	Interrupt flag status	Read-only
10001	Status1	Status capture	Read-only
10010	Status2	Status capture	Read-only
10011	Status3	Null	Read-only
10100	Capture0	Counter1 capture	Read-only
10101	Capture1	Counter1 capture	Read-only
10110	Read Buffer	Read buffer	Read-only
10111	Write Buffer	Write buffer	Write-only

control0 register bits

BIT	DESCRIPTION
0	Event0 Detect Enable
1	Event1 Detect Enable
2	Event2 Detect Enable
3	Event3 Detect Enable
4	Counter1 Execute Enable
5	Counter1 Scan Enable
6	Nutl
7	Null
8	Suspend Enable
9	End Enable
10	Resume Enable
11	Begin Enable
12	Buffer Error Enable
13	Buffer Ready Enable
14	Abort Enable
15	Finish Enable

control0 register bit description

The control0 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control0 register address (from ADRS4-ADRS0) is 00000.

event0 detect enable

The status of this bit determines if an interrupt is asserted when the event0 detect flag is set.

No interrupt is asserted.An interrupt is asserted.

event1 detect enable

The status of this bit determines if an interrupt is asserted when the event1 detect flag is set.

No interrupt is asserted.An interrupt is asserted.

event2 detect enable

The status of this bit determines if an interrupt is asserted when the event2 detect flag is set.

No interrupt is asserted.An interrupt is asserted.

event3 detect enable

The status of this bit determines if an interrupt is asserted when the event3 detect flag is set.

No interrupt is asserted.An interrupt is asserted.

counter1 execute enable

The status of this bit determines if an interrupt is asserted when the counter1 execute flag is set.

No interrupt is asserted.An interrupt is asserted.

counter1 scan enable

The status of this bit determines if an interrupt is asserted when the counter1 scan flag is set.

No interrupt is asserted.An interrupt is asserted.

suspend enable

The status of this bit determines if an interrupt is asserted when the suspend flag is set.

No interrupt is asserted.An interrupt is asserted.

end enable

The status of this bit determines if an interrupt is asserted when the end flag is set.

No interrupt is asserted.An interrupt is asserted.

resume enable

The status of this bit determines if an interrupt is asserted when the resume flag is set.

No interrupt is asserted.
 An interrupt is asserted.

control0 register bit description (continued)

begin enable

The status of this bit determines if an interrupt is asserted when the begin flag is set.

No interrupt is asserted.

An interrupt is asserted.

buffer error enable

The status of this bit determines if an interrupt is asserted when the buffer error flag is set.

No interrupt is asserted.

An interrupt is asserted.

buffer ready enable

The status of this bit determines if an interrupt is asserted when the buffer ready flag is set.

No interrupt is asserted.

An interrupt is asserted.

abort enable

The status of this bit determines if an interrupt is asserted when the abort flag is set.

0 No interrupt is asserted.

An interrupt is asserted.

finish enable

The status of this bit determines if an interrupt is asserted when the finish flag is set.

No interrupt is asserted.

An interrupt is asserted.

control1 register bits

1

BIT	DESCRIPTION
0	Observe Enable0
1	Observe Enable1
2	Capture Enable0
3	Capture Enable1
4	Unused
5	Unused
6	Unused
7	Unused
8	Serial Data Test
9	Link Delay Test
10	Serial Buffer Test
11	Counter Test
12	Flag Test
13	Unused
14	Unused
15	Unused

control1 register bit description

The control1 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control1 register address (from ADRS4-ADRS0) is 00001.

This register holds the control bits for the host interface and the manufacturing test functions. The bits in the upper byte must not be set when any major command is alive.

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control1 register bit description (continued)

observe enable0

This bit enables the reading of the observe3-0 registers via the status3-0 register locations. The observe2-0 registers make key internal flip-flops observable for manufacturing test. The observe3 register makes the design revision number observable for manufacturing test and normal operation.

Normal operation.

Observe enabled.

observe enable1

This bit enables the reading of the observe5-4 registers via the capture1-0 register locations. These observe registers make the values of counter20 and counter21 observable for manufacturing test.

Normal operation.
Observe enabled.

capture enable0

This bit enables continuous capturing of the status3-0 registers for normal operation and manufacturing test.

Normal operation.Capture enabled.

capture enable1

This bit enables continuous capturing of the capture1-0 registers for normal operation and manufacturing test.

Normal operation.Capture enabled.

serial data test

This bit configures the shifter-FIFO, LSB counters, outstanding bit counter, and write and recirculate multiplexers for normal operation or manufacturing test.

Normal operation.

Enable manufacturing test.

link delay test

This bit configures the link delay register for normal operation or manufacturing test.

Normal operation.

Enable manufacturing test.

control1 register bit description (continued)

serial buffer test

This bit configures the write buffers, shifter-FIFO, read transfer functions, and read buffer for manufacturing test.

Normal operation.

Enable manufacturing test.

counter test

This bit configures counter1 and counter20/21 for manufacturing test.

Normal operation.

Enable manufacturing test.

flag test

This bit configures the interrupt- and the execute-command request flags for manufacturing test.

Normal operation.

Enable manufacturing test.

control2 register bits

BIT	DESCRIPTION	
0	Connect Mode0	
1	Connect Mode1	
2	Connect Mode2	
3	Connect Mode3	
4	Connect Mode4	
5	Connect Mode5	
6	Null	
7	Null	
8	Null	
9	Null	
10	Null	
11	Null	
12	Null	
13	Null	
14	Null	
15	Null	

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control2 register bit description

The control2 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control2 register address (from ADRS4-ADRS0) is 00010.

connect mode0

The status of this bit determines if TMS0 is connected to the mode source.

- The mode source is disconnected from TMS0, whose value remains constant.
 - The mode source is connected to TMS0, whose value follows that of the mode source.

connect mode1

The status of this bit determines if TMS1 is connected to the mode source.

- The mode source is disconnected from TMS1, whose value remains constant.
- The mode source is connected to TMS1, whose value follows that of the mode source.

connect mode2

The status of this bit determines if TMS2 is connected to the mode source.

- The mode source is disconnected from TMS2, whose value remains constant.
- The mode source is connected to TMS2, whose value follows that of the mode source.

connect mode3

The status of this bit determines if TMS3 is connected to the mode source.

- The mode source is disconnected from TMS3, whose value remains constant.
- The mode source is connected to TMS3, whose value follows that of the mode source.

connect mode4

The status of this bit determines if TMS4 is connected to the mode source.

- The mode source is disconnected from TMS4, whose value remains constant.
- The mode source is connected to TMS4, whose value follows that of the mode source.

connect mode5

The status of this bit determines if TMS5 is connected to the mode source.

- The mode source is disconnected from TMS5, whose value remains constant.
- 1 The mode source is connected to TMS5, whose value follows that of the mode source.

control3	register	bits
----------	----------	------

BIT	DESCRIPTION
0	Mode Format20
1	Mode Format31
2	Mode Format42
3	Mode Format53
4	Clock Off
5	Data Off
6	Mode Off
7	Event Off
8	Out Format0
9	Out Format1
10	Machine Format0
11	Machine Format1
12	Clock Data
13	Clock Format
14	Null
15	Null

control3 register bit description

The control3 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control3 register address (from ADRS4-ADRS0) is 00011.

This register holds the format control bits that select the target interface output signals and turns their output buffers off and on. The clock off bit has precedence over the clock data and format bits. The TCKO pin control logic is designed so that changes in the values of the clock off, data, and format bits cause hazard-free changes in the configuration of the TCKO pin.

mode format20

This bit configures the TMS2/EVENT0 pin to be an EVENT input/output or a TMS output.

0

EVENT input/output.

1 TMS output.

mode format31

This bit configures the TMS3/EVENT1 pin to be an EVENT input/output or a TMS output.

0

EVENT input/output.

1 TMS output.

mode format42

This bit configures the TMS4/EVENT2 pin to be an EVENT input/output or a TMS output.

0

EVENT input/output.

1 TMS output.

mode format53

This bit configures the TMS5/EVENT3 pin to be an EVENT input/output or a TMS output.

0

EVENT input/output.

1 TMS output.

The changes in the state of the output pins caused by the clock, data mode, and event off bits are clean; spurious signal values do not occur.

clock off

This bit turns the TCKO output on or off.

0 On. 1 Off.



control3 register bit description (continued)

data off

This bit turns the TDO output on or off.

0 On. 1 Off.

mode off

This bit turns all pins operating as TMS outputs on or off.

0 On. 1 Off.

event off

This bit turns all pins operating as EVENT outputs on or off.

0 On. 1 Off.

out format1-0

These bits decide the format of several target interface outputs. The effect on the TMS1-0 pins is:

They output the TMS signal for IEEE Standard 1149.1 operation.
They output other signals for TI internal manufacturing test mode.
They output other signals for TI internal manufacturing test mode.
They output other signals for TI internal manufacturing test mode.

The effect on the TDO pin is:

00 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for IEEE Standard 1149.1 operation.

01 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.

10 It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.

It outputs data in the Shift-DR and Shift-IR states, and outputs the logic high level in other states for TI internal manufacturing test mode.

machine format1-0

11

01

These bits decide the format of the sequencer block state machines.

The sequencer block state machines state diagram is that of IEEE Standard 1149.1.

The sequencer block state machines state diagram is that required by TI internal

manufacturing test mode.

10 The sequencer block state machines state diagram is that required by TI internal

manufacturing test mode.

11 The sequencer block state machines state diagram is that required by TI internal

manufacturing test mode.

clock data

This bit selects the output level on the TCKO pin when the clock format bit is one.

A constant zero is output.A constant one is output.

clock format

This bit configures the TCKO pin to output either the clock or a logic level determined by the clock data bit.

The clock is output.

A level is output.



control4	register	bits
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BIT	DESCRIPTION
0	Link Delay0
1	Link Delay1
2	Link Delay2
3	Link Delay3
4	Link Delay4
5	Serial Length
6	Connect Data0
7	Connect Data1
8	Write Buffer0
9	Write Buffer1
10	Read Buffer
11	Transfer Format
12	In Timing0
13	In Timing1
14	Null
15	Null

control4 register bit description

The control4 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control4 register address (from ADRS4-ADRS0) is 00100.

link delay 4-0

These bits decide the length of the link delay register. The mode source is passed through the link delay register to generate a delayed-mode source which allows the 'ACT8990 internal functions to decode the TDI and EVENT signals. The length of the link delay register is set by the host to match the length of the direct or retimed link. If the link is direct, then these 5 bits are set to all zeroes. If the link is retimed, then these bits are set to a binary value equal to the number of clock cycles by which the mode source is to be delayed.

serial length

This bit configures the shifter-FIFO length as 16 or 32 bits.

0 16 bits. 1 32 bits.

connect data1-0

These bits select the data-in source to be used as either the data-out source for loopback operation or one of the TDI1-0 inputs.

00-01 The data-out source is used as the data-in source and the TDI1-0 inputs are ignored. The connect mode bits are ignored and the TMS outputs are disconnected from the mode source and hold their prior values. The link delay bits are ignored and the link delay register is bypassed, so a zero link delay is used.

The TDI0 input is the data-in source; the TDI1 input is ignored.
The TDI1 input is the data-in source; the TDI0 input is ignored.

write buffer1-0

This bit selects the write buffer option. Options 00 and 01 provide an efficient way of sending the BYPASS and EXTEST instructions. Option 10 provides an efficient way of bypassing strings that are of no interest. In option 11 the write buffer is used.

control4 register bit description (continued)

00 Send zeroes.
01 Send ones.
10 Send recirculate data from the shifter-FIFO.
11 Send overwrite data from the write buffer.

read buffer

This bit selects the read buffer option. In option 1, the read buffer is used.

Ignore receive data.

1 Read receive data into the read buffer.

transfer format

This bit selects the data format used by the transfer functions.

0 LSB-first format.1 MSB-first format.

in timing0

This bit configures the TDI1-0 inputs to be sampled on the falling or rising edge of TCKI. Together with the use of TCKI or TCKO as the clock for the target devices, this simplifies the connections of the 'ACT8990 to targets operating at high clock rates.

0 Rising edge.

1 Falling edge.

in timing1

This bit configures the EVENT3-0 inputs to be sampled on the falling or rising edge of TCKI. Together with the use of TCKI or TCKO as the clock for the target devices, this simplifies the connections of the 'ACT8990 to targets operating at high clock rates.

0 Rising edge.1 Falling edge.

control5 register bits

BIT	DESCRIPTION
0	Event0 Data
1	Event1 Data
2	Event2 Data
3	Event3 Data
4	Null
5	Null
6	Null
7	Null
8	Event0 On
9	Event1 On
10	Event2 On
11	Event3 On
12	Null
13	Null
14	Null
15	Null

control5 register bit description

The control5 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control5 register address (from ADRS4-ADRS0) is 00101.



control5 register bit description (continued)

This register holds the control bits for the four EVENT pin output buffers.

event0 data

This bit determines the EVENTO value when the output buffer is on.

0 Zero.

1 One.

event1 data

This bit determines the EVENT1 value when the output buffer is on.

0 Zero.

1 One.

event2 data

This bit determines the EVENT2 value when the output buffer is on.

0 Zero.

1 One.

event3 data

This bit determines the EVENT3 value when the output buffer is on.

Zero.
 One.

event0 on

This bit determines whether the EVENT0 output buffer is off or on.

Off.

1 On.

event1 on

This bit determines whether the EVENT1 output buffer is off or on.

0 Off.1 On.

event2 on

This bit determines whether the EVENT2 output buffer is off or on.

0 Off. 1 On.

event3 on

This bit determines whether the EVENT3 output buffer is off or on.

0 Off. 1 On.

PRODUCT PREVIEW control6 register bits

BIT	DESCRIPTION
0	Detect0 Suspend
1	Detect0 End
2	Detect0 Resume
3	Detect0 Begin
4	Detect0 Sync
5	Detect0 Mask
6	Detect0 Select0
7	Detect0 Select1
8	Detect1 Suspend
9	Detect1 End
10	Detect1 Resume
11	Detect1 Begin
12	Detect1 Sync
13	Detect1 Mask
14	Detect1 Select0
15	Detect1 Select1

control6 register bit description

The control6 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control6 register address (from ADRS4-ADRS0) is 00110.

No more than one bit in each group of suspend, end, resume, and begin bits should be set at any time. Such a configuration has no application, as it causes several conflicting request flags to be set when an event is detected.

detect0 suspend

This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No.

1 Yes.

detect0 end

This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.

0 No.

1 Yes.

detect0 resume

This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.

0 No.

1 Yes.

detect0 begin

This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.

0 No.

1 Yes.

detect0 sync

This bit selects asynchronous or synchronous event detection.

0 Asynchronous. Synchronous. 1

control6 register bit description (continued)

detect0 mask

This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.

0 Not masked.

1 Masked.

detect0 select1-0

These bits select the event to be detected.

If the detect0 sync bit is zero:

00 A falling edge on EVENTO.

01 A rising edge on EVENT0.

10 Counter20 passing zero.

Counter21 passing zero.

If the detect0 sync bit is one:

00 A one, then zero on EVENTO.

01 A zero, then one on EVENTO.

10 A zero, then zero on EVENTO.

11 A one, then one on EVENT0.

detect1 suspend

11

This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No.

1 Yes.

detect1 end

This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.

0 No.

1 Yes.

detect1 resume

This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.

0 No.

1 Yes.

detect1 begin

This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.

No.

1 Yes.

detect1 sync

This bit selects asynchronous or synchronous event detection.

Asynchronous.

Synchronous.

detect1 mask

This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.

Not masked.

1 Masked.



control6 register bit description (continued)

detect1 select1-0

These bits select the event to be detected.

If the detect1 sync bit is zero:

A falling edge on EVENT1.

01 A rising edge on EVENT1.

10 Counter20 passing zero.

11 Counter21 passing zero.

If the detect1 sync bit is one:

A one, then zero on EVENT1.

01 A zero, then one on EVENT1.

10 A zero, then zero on EVENT1. 11 A one, then one on EVENT1.

control7 register bits

BIT	DESCRIPTION
0	Detect2 Suspend
1	Detect2 End
2	Detect2 Resume
3	Detect2 Begin
4	Detect2 Sync
5	Detect2 Mask
6	Detect2 Select0
7	Detect2 Select1
8	Detect3 Suspend
9	Detect3 End
10 ,	Detect3 Resume
11	Detect3 Begin
12	Detect3 Sync
13	Detect3 Mask
14	Detect3 Select0
15	Detect3 Select1

control7 register bit description

The control7 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control7 register address (from ADRS4-ADRS0) is 00111.

No more than one bit in each group of suspend, end, resume, and begin bits should be set at any time. Such a configuration has no application, as it causes several conflicting request flags to be set when an event is detected.

detect2 suspend

This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No.

1 Yes.

detect2 end

This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.

0 No. 1

Yes.



control7 register bit description (continued)

detect2 resume

This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.

0 No. 1 Yes.

detect2 begin

This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.

0 No. 1 Yes.

detect2 sync

This bit selects asynchronous or synchronous event detection.

0 Asynchronous.1 Synchronous.

detect2 mask

This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR. Exit1-DR. Exit2-DR. Capture-IR. Exit1-IR and Exit2-IR are returned.

0 Not masked.1 Masked.

detect2 select1-0

These bits select the event to be detected.

If the detect2 sync bit is zero:

A falling edge on EVENT2.
A rising edge on EVENT2.
Counter20 passing zero
Counter21 passing zero.

If the detect2 sync bit is one:

A one, then zero on EVENT2.
A zero, then one on EVENT2.
A zero, then zero on EVENT2.
A one, then one on EVENT2.

detect3 suspend

This bit determines whether event detection sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No. 1 Yes.

detect3 end

This bit determines whether event detection sets the end request flag and so may cause EXECUTE commands to end.

0 No. 1 Yes.

datact? recume

This bit determines whether event detection sets the resume request flag and so may cause EXECUTE commands to resume.

0 No.1 Yes.



control7 register bit description (continued)

detect3 begin

This bit determines whether event detection sets the begin request flag and so may cause EXECUTE commands to begin.

0 No. 1 Yes.

detect3 sync

PRODUCT PREVIEW

This bit selects asynchronous or synchronous event detection.

0 Asynchronous.1 Synchronous.

detect3 mask

This bit determines whether event detection is masked when scan, pause, and the associated temporary states Capture-DR, Exit1-DR, Exit2-DR, Capture-IR, Exit1-IR and Exit2-IR are returned.

0 Not masked.1 Masked.

detect3 select1-0

These bits select the event to be detected.

If the detect3 sync bit is zero:

A falling edge on EVENT3.
A rising edge on EVENT3.
Counter20 passing zero
Counter21 passing zero.

If the detect3 sync bit is one:

A one, then zero on EVENT3.
A zero, then one on EVENT3.
A zero, then zero on EVENT3.
A one, then one on EVENT3.

control8 register bits

BIT	DESCRIPTION
0	Counter1 Suspend
1	Counter1 End
2	Counter1 Reload
3	Counter1 Operate0
4	Counter1 Operate1
5	Counter1 Operate2
6	Counter1 Source0
7	Counter1 Source1
8	Unused
9	Unused
10	Unused
11	Unused
12	Unused
13	Unused
14	Unused
15	Unused



control8 register bit description

The control8 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control8 register address (from ADRS4-ADRS0) is 01000.

counter1 suspend

This bit determines whether the counter passing zero sets the suspend request flag and so may cause EXECUTE commands to suspend.

0 No. 1 Yes.

counter1 end

This bit determines whether the counter passing zero sets the end request flag and so may cause EXECUTE commands to end.

0 No.

1 Yes

counter1 reload

This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.

0 It is decremented to the value of all ones.

It is loaded from its update register. 1

counter1 operate2-0

These bits determine when the counter is operated. If based on an event detector or EVENT pin, the counter1 source1-0 bits select the particular pin.

000 It is not operated at any time. 001 It is not operated at any time.

010 Whenever EXECUTE commands send execute states.

011 Whenever EXECUTE commands are alive.

100 By an event detector. 101

By an event detector.

110 By a logic low level on an EVENT pin. 111 By a logic high level on an EVENT pin.

counter1 source1-0

These bits determine which EVENT pin level or event detection operates the counter when selected by counter1 operate2-0.

00 EVENT0 or event detector0.

01 EVENT1 or event detector1.

10 EVENT2 or event detector2.

11 EVENT3 or event detector3.

PRODUCT PREVIEW control9 register bits

BIT	DESCRIPTION
0	External Update Polarity
1	External Update Source0
2	External Update Source1
3	Counter20 Update Inverted
4	Counter20 Reload
5	Counter20 Operate
6	Counter20 Source0
7	Counter20 Source1
8	External Update Enable
9	Counter2 Use0
10	Counter2 Use1
11	Counter21 Update Inverted
12	Counter21 Reload
13	Counter21 Operate
14	Counter21 Source0
15	Counter21 Source1

control9 register bit description

The control9 register is set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The control9 register address (from ADRS4-ADRS0) is 01001.

external update polarity

This bit determines whether logic low or high level on an EVENT pin causes the external updating.

Logic low. 0 1 Logic high.

external update source1-0

These bits determine which EVENT pin externally updates the counter.

EVENT0 is used. 01 EVENT1 is used. 10 EVENT2 is used. EVENT3 is used. 11

counter20 update inverted

This bit determines whether the counter is updated from its update register.

It is updated. 0 1 It is not updated.

counter20 reload

This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.

0 It is decremented to the value of all ones.

It is loaded from its update register. 1

counter20 operate

This bit determines when the counter is operated by an EVENT pin as selected by counter20 source1-0.

It is operated by falling edges. It is operated by rising edges. 1



PRODUCT PREVIEW

control9 register bit description (continued)

counter20 source1-0

These bits determine which EVENT pin operates the counter.

00 EVENT0 is used.
01 EVENT1 is used.
10 EVENT2 is used.
11 EVENT3 is used.

external update enable

This bit determines whether the counters may be externally updated from their update registers asynchronously by an EVENT pin.

They may not be updated asynchronously.
They may be updated asynchronously.

counter2 use1-0

These bits determine whether counter20 and counter21 are used as separate or tiered 16-bit counters or concatenated as one 32-bit counter.

00 or 01 Separate counters.
10 Tiered counters.
11 Concatenated counters.

These bits also decide if counter20 only or both counter20 and counter21 may be updated asynchronously by a signal on an event pin.

00 Only counter20 may be externally updated.

01. 10. or

11 Both counter20 and counter21 may be externally updated.

counter21 update inverted

This bit determines whether the counter is updated from its update register.

0 It is updated.1 It is not updated.

counter21 reload

This bit determines whether the counter is loaded from its update register or decremented to all ones when it passes zero.

0 It is decremented to the value of all ones.

1 It is loaded from its update register.

counter21 operate

This bit determines when the counter is operated by an EVENT pin as selected by counter21 source1-0.

0 It is operated by falling edges.1 It is operated by rising edges.

counter21 source1-0

These bits determine which EVENT pin operates the counter.

00 EVENT0 is used.
01 EVENT1 is used.
10 EVENT2 is used.
11 EVENT3 is used.



PRODUCT PREVIEW minor command register bits

BIT	DESCRIPTION
0	Minor Opcode0
1	Minor Opcode1
2	Minor Opcode2
3	Minor Opcode3
4	Minor Opcode4
5	Minor Opcode5
6	Minor Opcode6
7	Minor Opcode7
8	Null
9	Null
10	Null
11	Null
12	Minor Opcode12
13	Minor Opcode13
14	Minor Opcode14
15	Minor Opcode15

minor command register bit description

The minor command register is set by the host to select a particular minor command to be executed and to direct its operations while it is alive. The bits are not altered by the device. The minor command register address (from ADRS4-ADRS0) is 01010.

The act of writing to the minor command register causes the selected minor command to begin.

The minor commands require only a few clock periods to complete their operations, during which the RDY pin is asserted. They do not affect the awake and alive status bits during their operations. They do not affect the finish interrupt flag when they finish.

Note that the operate 0/1 minor commands are used to begin the major command selected by the value of the major command register.

minor opcode7-0

0000

The minor opcode7-0 bits specify options for the command.

minor opcode15-12

The minor opcode15-12 bits select the minor command: Coloot o CLEADO command

0000	Select a CLEARU Command.
0001	Select a CLEAR1 command.
0010	Select a SET0 command.
0011	Select a SET1 command.
0100	Select an OPERATE0 command.
0101	Select an OPERATE1 command.
0110	Select an OPERATE2 command.
0111	Select a RESET command.
1XXX	No effect



minor command register bit description (continued)

CLEAR

This command is used to selectively clear the interrupt flags in the lower byte (bits 7-0) of the status0 register.

The CLEAR0 command is selected by minor opcode15-12 bits = 0000.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected

7	Unused.
6	Unused.
5	Clear the interrupt flag in bit 5.
4	Clear the interrupt flag in bit 4.
3	Clear the interrupt flag in bit 3.
2	Clear the interrupt flag in bit 2.
1	Clear the interrupt flag in bit 1.
0	Clear the interrupt flag in bit 0.

CLEAR1

This command is used to selectively clear the interrupt flags in the upper byte (bits 15-8) of the status0 register.

The CLEAR1 command is selected by minor opcode15-12 bits = 0001.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Clear the interrupt flag in bit 15.
6	Clear the interrupt flag in bit 14.
5	Clear the interrupt flag in bit 13.
4	Clear the interrupt flag in bit 12.
3	Clear the interrupt flag in bit 11.
2	Clear the interrupt flag in bit 10.
1	Clear the interrupt flag in bit 9.
0	Clear the interrupt flag in hit 8

SETO

This command is used to selectively set the interrupt flags in the lower byte (bits 7-0) of the status0 register.

The SET0 command is selected by minor opcode 15-12 bits = 0010.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Unused.
6	Unused.
5	Set the interrupt flag in bit 5.
4	Set the interrupt flag in bit 4.
3	Set the interrupt flag in bit 3.
2	Set the interrupt flag in bit 2.
1	Set the interrupt flag in bit 1.
0	Set the interrupt flag in bit 0.

minor command register bit description (continued)

SET1

This command is used to selectively set the interrupt flags in the upper byte (bits 15-8) of the status0 register.

The SET1 command is selected by minor opcode15-12 bits = 0011.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected

7	Set the interrupt flag in bit 15.
6	Set the interrupt flag in bit 14.
5	Set the interrupt flag in bit 13.
4	Set the interrupt flag in bit 12.
3	Set the interrupt flag in bit 11.
2	Set the interrupt flag in bit 10.
1	Set the interrupt flag in bit 9.
0	Set the interrupt flag in bit 8.

OPERATEO

This command is used to:

- Begin STATE, SCAN, or EXECUTE commands.
- Abort SCAN or EXECUTE commands.
- Enable EXECUTE commands to begin (usually from an EVENT pin).

This command is also used to selectively clear the request flags (observable in the status1 register) used by EXECUTE commands. The similar OPERATE1 command is used to selectively set them. These flags affect the EXECUTE command in the following ways:

- Request it to begin or end.
- Request an awake command to resume.
- Request an asleep command to resume.

When the command acknowledges the request, the request flag is cleared and a matching acknowledge-interrupt flag is set. The affected command will alter the awake and alive status bits and set the appropriate finish, abort, suspend, end, resume, or begin interrupt flag when it responds.

The OPERATEO command is selected by minor opcode15-12 bits = 0100.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7 Regin a STATE SCAN or EXECUTE command.

•	begin a CTATE, COAR OF EXECUTE Command.
6	Abort a SCAN or EXECUTE command.
5	Enable an EXECUTE command to begin.
4	Unused.
3	Clear the EXECUTE command begin-request flag.
2	Clear the EXECUTE command resume-request flag.
1	Clear the EXECUTE command end-request flag.
0	Clear the EXECUTE command suspend-request flag.

OPERATE1

This command is used to:

- Begin STATE, SCAN, or EXECUTE commands.
- Abort SCAN or EXECUTE commands.
- Enable EXECUTE commands to begin (usually from an EVENT pin).



minor command register bit description (continued)

This command is also used to selectively set the request flags (observable in the status1 register) used by EXECUTE commands. The similar OPERATE0 command is used to selectively clear them. These flags affect the EXECUTE command in the following ways:

- Request it to begin or end.
- Request an awake command to suspend.
- Request an asleep command to resume.

When the command acknowledges the request, the request flag is cleared and a matching acknowledge-interrupt flag is set. The affected command will alter the awake and alive status bits and set the appropriate finish, abort, suspend, end, resume, or begin interrupt flag when it responds.

The OPERATE1 command is selected by minor opcode15-12 bits = 0101.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

7	Begin a STATE, SCAN or EXECUTE command.
6	Abort a SCAN or EXECUTE command.
5	Enable an EXECUTE command to begin.
4	Unused.
3	Set the EXECUTE command begin-request flag.
2	Set the EXECUTE command resume-request flag.
1	Set the EXECUTE command end-request flag.
0	Set the EXECUTE command suspend-request flag.

OPERATE2

The OPERATE2 command is used to operate various functions.

The OPERATE2 command is selected by minor opcode15-12 bits = 0110.

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

- 7 Unused.
- 6 Capture status2, status1 and status0.
- 5 Update counter21.
- 4 Update counter20.
- 3 Unused.
- 2 Capture counter1.
- Operate counter1.
- 0 Update counter1.

RESET

This command is used to software-reset either selected functions or the entire 'ACT8990.

The RESET command is selected by minor opcode15-12 bits = 0111.

PRODUCT PREVIEW

minor command register bit description (continued)

The minor opcode7-0 bits specify options for the command. If a bit is zero, then the specified option is not selected.

- 7 Unused.6 Unused.
- 5 Unused. 5 Unused.
- 4 Unused.
- 3 Reset the request flag.2 Reset the data buffers.
- Reset the interrupt flags.
- Software reset the entire 'ACT8990.

major command register bits

BIT	DESCRIPTION
0	Major Opcode0
1	Major Opcode1
2	Major Opcode2
3	Major Opcode3
4	Major Opcode4
5	Major Opcode5
6	Major Opcode6
7	Major Opcode7
8	Major Opcode8
9	Null
10	Null
11	Null
12	Major Opcode12
13	Major Opcode 13
14	Major Opcode14
15	Major Opcode15

major command register bit description

The major command register is set by the host to select a particular major command to be executed and to direct its operations while it is alive. The bits are not altered by the device. The major command register address (from ADRS4-ADRS0) is 01011.

The act of writing an OPERATEO/1 minor command with bit 7 set, causes the selected major command to begin.

The major commands may require many clock periods to complete their operations, during which the awake and alive status bits are affected. When they finish, the finish interrupt flag is set. The major commands do not assert the \overline{RDY} pin.

Note that the major command register should not be written to while a major command is alive.

major opcode8-0

The major opcode8-0 bits specify options for the command.



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major command register bit description (continued)

major opcode15-12

The major opcode15-12 bits select the major command:

0000 No effect.

0001 Select a STATE command to change the target-interface state.

0010 Select an EXECUTE command to cause the IEEE Standard 1149.1 target to execute an

nstruction.

0011 Select a SCAN command to scan data and instructions between the IEEE Standard 1149.1

target and the 'ACT8990.

01XX No effect. 1XXX No effect.

Major commands cause the 'ACT8990 to interface with its IEEE Standard 1149.1 target(s). There are three major commands: STATE, EXECUTE, and SCAN.

STATE

The STATE command is used to change the state of the target interface and target(s) from their current state to the state selected by the major opcode2-0 bits.

During the STATE command no action other than the state change occurs:

- The event detectors and counters are ignored.
- Counter1 is ignored and not operated, even if the Run-Test/Idle state is entered.
- The data buffers are ignored and not loaded from or stored to, even if the Shift-DR or Shift-IR states are entered.
- The shifter-FIFO is ignored and not operated, even if the Shift-DR or Shift-IR states are entered.

The command (see Figure 20) has two operating states that can be used together with the major opcode2-0 bits by the Sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to. The states are:

- Dead: the command is either finished or not vet begun.
- End: the Sequencer block is moving the target interface to the state selected by the major opcode2-0 bits.

If the current state and selected state are different, the state change (see Figure 1) uses the following rules:

- If the current state is Test-Logic-Reset, then the change occurs first through the stable Run-Test/Idle state, then via temporary states only.
- If the current state is not Test-Logic-Reset, then the change occurs via temporary states only.

If the current state and selected state are the same, the state change (see Figure 1) uses the following rules:

- -If major opcode2 is 0 (the state is Test-Logic-Reset or Run-Test/Idle), then no change occurs.
- If major opcode2 is 1 (the state is Shift-DR, Shift-IR, Pause-DR or Pause-IR), then the change occurs via temporary states only through the matching update and capture states, returning to the same state.

The STATE command can be begun only by OPERATE0/1 minor commands. Note that the EXECUTE command can be configured to behave like the STATE command by going directly to its end state after it begins, the difference being that the EXECUTE command can be begun by a signal on an EVENT pin via the event detectors and counters.



PRODUCT PREVIEW major command register bit description (continued)

The STATE command is selected by major opcode15-12 bits = 0001. The major opcode11-4 bits are ignored.

The major opcode2-0 bits select the end state (the state of the target after the command ends).

Test-Logic-Reset.

Test-Logic-Reset.

Run-Test/Idle.

Run-Test/Idle.

Shift-DR. Shift-IR.

Pause-DR.

Pause-IR.

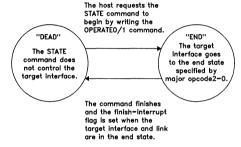


FIGURE 20. STATE DIAGRAM OF THE STATE COMMAND

major command register bit description (continued)

EXECUTE

The EXECUTE command is used to make the target(s) execute instructions (in the Run-Test/Idle state) that have been shifted into their instruction register(s).

The command (see Figure 21) has four operating states (dead, execute, sleep and end) that are used together with the major opcode bits by the sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to.

The combination of the command operating states and changes between these states caused by minor commands, counter1, the event detectors, and counters allow the target(s) instructions to begin, suspend, resume and end under host software or the 'ACT8990 hardware control.

When the 'ACT8990 is configured for IEEE Standard 1149.1 target(s) (by setting the machine format1-0 and output format1-0 control bits to zero), the command operating states are:

- Dead: the command is either finished or not yet begun.
- Execute: the target interface is in (or moving to) the Run-Test/Idle state in which IEEE Standard 1149.1 target(s) execute their instruction(s).
- Sleep: the target interface is in (or moving to) the Pause-DR or Pause-IR states (as selected by the major opcode3 bit) in which IEEE Standard 1149.1 target(s) may not execute their instruction(s).
- End: the command is about to finish and the sequencer block is moving the target interface to a state selected by the major opcode2-0 bits.

The command state may be changed by:

- Host software: the OPERATE0/1 minor commands may set and clear flags to request the command to begin, suspend, resume or end.
- Host software: the OPERATEO/1 minor commands may request the command to abort.
- The EXECUTE command itself: its major opcode4 bit may be set to automatically suspend itself every time it enters the execute state.
- -The event detectors and counters: they may set flags to request the command to begin, suspend, resume or end.
- Counter1: it may set flags to request the command to suspend or end.

The command is suspended by an EVENT pin via an event detector, by an OPERATE0/1 command, or by counter1 passing zero. The executing command goes to the sleep state selected by the major opcode3 bit in which it does not operate counter1.

major command register bit description (continued)

The command is ended by an EVENT pin via an event detector, by an OPERATE0/1 command, or by counter1 passing zero. The executing or sleeping command goes to the end state selected by the major opcode2-0 bits and finishes. End requests have priority over suspend or resume requests.

The command is resumed by an EVENT pin via an event detector or by an OPERATE0/1 command. The sleeping command goes to the execute state selected by the major opcode3 bit in which it may operate counter1.

The command is begun by an EVENT pin via an event detector or by an OPERATE0/1 command. The dead command goes to the end, sleep or execute state selected by the major opcode7-6 bits. Attempts to set the begin-request flag are ignored until they are enabled by OPERATE0/1 commands.

The command is aborted by an OPERATEO/1 command. The executing or sleeping command goes to the sleep state selected by the major opcode3 bit and finishes. Abort requests have priority over suspend or resume requests.

The alive status bit is asserted when the command begins and negated when it finishes. The awake status bit is one (the command is awake) when the target interface is moving to or already in the execute or end states. The awake status bit is zero (the command is asleep) when the target interface is moving to or already in the sleep state.

This command allows only one contiguous block of execute states to be outstanding in the retimed link. If the command is asleep and a resume request occurs, the device will not respond until the link is empty of execute states. If the command is asleep or executing and an end or abort request occurs, the device responds immediately.

The command finishes when the link is empty of execute and temporary states and holds only the end or sleep state. It then sets the finish flag (and possibly the abort flag).

The EXECUTE command is selected by major opcode15-12 bits = 0010.

The major opcode11-9 bits are ignored.

The major opcode8 bit selects suspend and resume options.

- The command clears only the respective suspend or resume requests when it suspends or resumes.
- 1 The command clears both suspend and resume requests when it either suspends or resumes.

The major opcode7-6 bits select the begin options.

00 or 01	The command goes directly to the end state when it begins. It is similar to a STATE
	command but may be begun by EVENT pins.

- The command goes directly to the sleep state when it begins.
- The command goes directly to the execute state when it begins.

The major opcode5-4 bits select suspend, end, and abort options.

00	The command pauses or ends when counter1 passes zero.
01	The command pauses or ends when counter1 passes zero

- 10 The command does not use counter1 and ends after a single execute state is sent.
- 11 The command does not use counter1 and aborts after a single execute state is sent.

The major opcode3 bit selects the execute and sleep states for IEEE Standard 1149.1 operation if machine format1-0 bits are 00. If machine format1-0 bits are 01, 10, or 11, then other states are selected for TI internal manufacturing test mode.

0	Use Run-Test/Idle and Pause-DR states.
1	Lieo Run-Teet/Idle and Pause-IR states

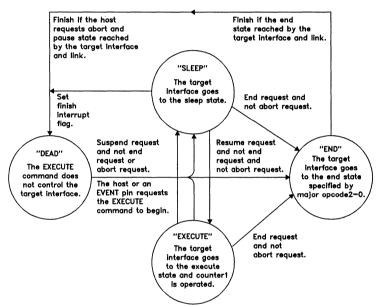


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major command register bit description (continued)

The major opcode2-0 bits selects the end state.

000	Test-Logic-Reset.
001	Test-Logic-Reset.
010	Run-Test/Idle.
011	Run-Test/Idle.
100	Shift-DR.
101	Shift-IR.
110	Pause-DR.
111	Pause-IR.



- NOTES: 1. The begin, end, suspend, and resume requests are caused by either the host writing OPERATEO/1 commands, by the detection and counting of events on event pins, or by counter1 passing zero.
 - 2. Counter1 passing zero can cause pause or end requests.
 - When the command begins, the target interface goes to the execute, pause, or end states as selected by major opcode5-4.

FIGURE 21. STATE DIAGRAM OF THE EXECUTE COMMAND



major command register bit description (continued)

SCAN

The SCAN command is used to scan instructions and data (in the Shift-IR or Shift-DR states) between the 'ACT8990 parallel write and read buffers and the target(s) serial instruction or data registers.

The command (see Figure 22) has four operating states (dead, scan, sleep and end) that are used together with the major opcode bits by the sequencer block to select which IEEE Standard 1149.1 state the target interface and target(s) should be held in or moved to.

The combination of the command operating states and changes between these states allow the command to perform all low-level scan functions. The host functions are limited to the following: 1) before the command begins, selecting the number of bits to be scanned by loading the value into counter1 and 2) during the command, capturing the write and read buffer status in status2 register and appropriately loading data to the write buffer or storing data from the read buffer.

When the 'ACT8990 is configured for IEEE Standard 1149.1 target(s) (by setting the machine format1-0 and output format1-0 control bits to zero), the SCAN command operating states are:

- Dead: the command is either finished or not yet begun.
- Scan: the target interface is in (or moving to) the Shift-DR or Shift-IR state (as selected by the major opcode3 bit) in which the 'ACT8990 will scan data between itself and the target(s).
- Sleep: the target interface is in (or moving to) the Pause-DR or Pause-IR state (as selected by the major opcode3 bit) in which the 'ACT8990 will not scan data between itself and the target(s).
- End: the command is about to finish and the sequencer block is moving the target interface to a state selected by the major opcode2-0 bits.

The command state may be changed by:

- Host software: the OPERATEO/1 minor commands may request the command to abort.
- The Write Buffer: the command suspends and resumes the scanning of data (by entering its sleep and scan states) depending on the availability of data in the write buffer.
- The Read Buffer: the command suspends the resumes the scanning of data (by entering its sleep and scan states) depending on the availability of space in the read buffer.
- -Counter1: the command ends (by entering its end state) when counter1 passes zero and the correct number of bits have been scanned.

major command register bit description (continued)

The target registers are treated as a number of modules each containing a string of data. Each string is accessed with one or more SCAN commands. The string length is defined as one plus the value of the counter1 register, giving a range of one to 2³² bits per SCAN command. The command ends when counter1 passes zero, decrements to all ones, and all data bits are sent. The command then goes to the end state and finishes.

The SCAN command may be aborted by an OPERATEO/1 command. It responds in either the scan or the sleep states when on a word boundary by going to the sleep state and finishing.

The alive status bit is asserted when the command begins and negated when it finishes. The awake status bit is one (the command is awake) when the target interface is moving to or already in the scan or end states. The awake status bit is zero (the command is asleep) when the target interface is moving to or already in the sleep state.

The SCAN command does not allow the number of outstanding data bits to exceed the shifter-FIFO length as selected by the serial length control bit.

The command finishes when the link is empty of scan and temporary states and holds only the stable end or sleep state. It then sets the finish flag (and possibly the abort flag).

The SCAN command is selected by major opcode15-12 bits = 0011.

The major opcode11-6 bits are ignored.

The major opcode5-4 bits select the suspend, end, and abort options.

The command ends when counter1 passes zero.

01 The command ends when counter1 passes zero and suspends after all bits are sent.

The command does not use counter1 and ends after a single bit is sent.

11 The command does not use counter1 and aborts after a single bit is sent.

The major opcode3 bit selects the scan and sleep states.

Use Shift-DR and Pause-DR states.
 Use Shift-IR and Pause-IR states.

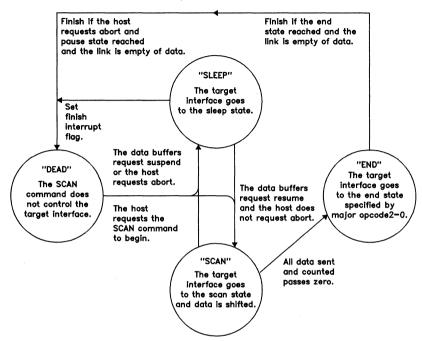
The major opcode2-0 bits select the end state.

000 Test-Logic-Reset.
001 Test-Logic-Reset.
010 Run-Test/Idle.
011 Run-Test/Idle.
100 Shift-DR.
110 Pause-DR

Pause-IR.

111

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NOTES: 1. The data buffers request suspend if read is full and write is empty.

- 2. The data buffers request resume if read is not full and write is not empty.
- 3. The command is begun and aborted by the host writing OPERATEO/1 commands.

FIGURE 22. STATE DIAGRAM OF THE SCAN COMMAND

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counter1 update0, counter1 update1 register bits

ВІТ	DESCF	IPTION	
	COUNTER1 UPDATE0	COUNTER1 UPDATE1	
0	Counter1 Update0	Counter1 Update16	
1	Counter1 Update1	Counter1 Update17	1
2	Counter1 Update2	Counter1 Update18	
3	Counter1 Update3	Counter1 Update19	İ
4	Counter1 Update4	Counter1 Update20	
5	Counter1 Update5	Counter1 Update21	
6	Counter1 Update6	Counter1 Update22	
7	Counter1 Update7	Counter1 Update23	
8	Counter1 Update8	Counter1 Update24	- 1
9	Counter1 Update9	Counter1 Update25	i
10	Counter1 Update10	Counter1 Update26	
11	Counter1 Update11	Counter1 Update27	1
12	Counter1 Update12	Counter1 Update28	- 1
13	Counter1 Update13	Counter1 Update29	1
14	Counter1 Update14	Counter1 Update30	
15	Counter1 Update15	Counter1 Update31	l

counter1 update1-0 registers bit description

The counter1 update1-0 registers are set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The counter1 update0 register address (from ADRS4-ADRS0) is 01100. The counter1 update1 register address (from ADRS4-ADRS0) is 01101.

Counter1 update registers load the 32-bit counter used in major commands. Registers 0 and 1 are the least and most significant words. Bits 0 and 15 are the least and most significant bits of each register. Reset causes the counter1 update register bits to be reset to all zeroes. Counter1 is usually loaded before major commands begin. It is also reloaded from these registers when it passes zero during EXECUTE commands if the counter control bits are appropriately set.

These registers are loaded to the counter by the OPERATE2 command.

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counter2 update0, counter2 update1 register bits

DIT	DESCRIPTION	
BIT	COUNTER2 UPDATE0	COUNTER2 UPDATE1
0	Counter2 Update0	Counter2 Update16
1	Counter2 Update1	Counter2 Update17
2	Counter2 Update2	Counter2 Update18
3	Counter2 Update3	Counter2 Update19
4	Counter2 Update4	Counter2 Update20
5	Counter2 Update5	Counter2 Update21
6	Counter2 Update6	Counter2 Update22
7	Counter2 Update7	Counter2 Update23
8	Counter2 Update8	Counter2 Update24
9	Counter2 Update9	Counter2 Update25
10	Counter2 Update10	Counter2 Update26
11	Counter2 Update11	Counter2 Update27
12	Counter2 Update12	Counter2 Update28
13	Counter2 Update13	Counter2 Update29
14	Counter2 Update14	Counter2 Update30
15	Counter2 Update15	Counter2 Update31

counter2 update1-0 registers bit description

The counter2 update1-0 registers are set by the host to configure the 'ACT8990 before a command is executed. The bits are not altered by the device. The counter2 update0 register address (from ADRS4-ADRS0) is 01110. The counter2 update1 register address (from ADRS4-ADRS0) is 01111.

Counter2 update registers load counter20 and counter21. When concatenated, registers 0 and 1 are the least and most significant words. Bits 0 and 15 are the least and most significant bits of each register. Reset causes the counter2 update register bits to be reset to all zeroes. Counter20/21 are usually loaded before major commands begin. They are also reloaded from these registers when they pass zero or as decided by an EVENT pin (external update) if the counter control bits are appropriately set.

These registers are loaded to the counter by the OPERATE2 command and when the counter20 and counter21 update inverted control bits are zero.

status0 register bits

BIT	DESCRIPTION
0	Event0 Detect
1	Event1 Detect
2	Event2 Detect
3	Event3 Detect
4	Counter1 Execute
5	Counter1 Scan
6	Null
7	Null
8	Suspend Acknowledge
9	End Acknowledge
10	Resume Acknowledge
11	Begin Acknowledge
12	Buffer Error
13	Buffer Ready
14	Abort
15	Finish

status0 register bit description

The host may only read the status0 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status0 register address (ADRS4-ADRS0) is 10000.

This register holds the interrupt flag bits that indicate a specific status condition that has occurred in the device. If the matching interrupt-enable bit in the control0 register is set, then the $\overline{\text{INT}}$ pin will be asserted. The interrupt flags are selectively cleared and set by the CLEAR0/1 and SET0/1 commands.

These bits are loaded from the interrupt flags by an OPERATE2 command.

event0 detect

This flag indicates if an event has been detected by event detector0.

0 No.

1 Yes.

event1 detect

This flag indicates if an event has been detected by event detector1.

0 No.

1 Yes.

event2 detect

This flag indicates if an event has been detected by event detector2.

0 No.

1 Yes.

event3 detect

This flag indicates if an event has been detected by event detector3.

0 No.

1 Yes.

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status0 register bit description (continued)

counter1 execute

This flag indicates if counter1 has passed zero, as configured by the control8 register, usually for an EXECUTE command.

No. 1 Yes.

counter1 scan

This flag indicates if counter1 has passed zero during a SCAN command.

Yes.

suspend acknowledge

This flag indicates if an EXECUTE command has responded to a suspend request.

No. Yes.

end acknowledge

This flag indicates if an EXECUTE command has responded to an end request.

Yes.

resume acknowledge

This flag indicates if an EXECUTE command has responded to a resume request.

No. 0 1 Yes.

begin acknowledge

This flag indicates if an EXECUTE command has responded to a begin request.

No. Yes.

buffer error

This bit indicates if a buffer error has occurred (i.e., an over-write or under-read to the write and read buffers).

0 No. Yes.

buffer ready

This bit indicates if the data buffers are ready for reading. This occurs when:

- -Only the write buffer is used and becomes empty.
- -Only the read buffer is used and becomes full.
- Both are used, where the write buffer becomes empty and the read buffer becomes full.

No. Yes.

0

1

This flag indicates if a major command has aborted.

No. 1 Yes.

finish

This flag indicates if a major command has finished.

No. 1 Yes.



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status1	registe	r bits
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BIT	DESCRIPTION
0	Event0 Level
1	Event1 Level
2	Event2 Level
3	Event3 Level
4	Null
5	Null
6	Null
7	Null
8	Suspend Request
9	End Request
10	Resume Request
11	Begin Request
12	· Null
13	Null
14	Awake
15	Alive

status1 register bit description

The host may only read the status1 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status1 register address (ADRS4-ADRS0) is 10001.

These bits are loaded from the internal status signals by an OPERATE2 command.

event0 level

This flag indicates the level of this pin.

0 Low. 1 High.

event1 level

This flag indicates the level of this pin.

0 Low.1 High.

event2 level

This flag indicates the level of this pin.

0 Low. 1 High.

event3 level

This flag indicates the level of this pin.

0 Low. 1 High.

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status1 register bit description (continued)

suspend request

This flag indicates if an EXECUTE command has been requested to suspend.

0 No

1 Yes.

end request

This flag indicates if an EXECUTE command has been requested to end.

0 No.

1 Yes.

resume request

This flag indicates if an EXECUTE command has been requested to resume.

) No

1 Yes.

begin request

This flag indicates if an EXECUTE command has been requested to begin.

No.

Yes.

awake

1

This status bit indicates the state of major commands.

O A major command is alive and asleep, or none are alive.

1 A major command is alive and awake, or ending.

The target-interface send functions are moving towards or already in the execute or scan state when awake during EXECUTE or SCAN commands. The target-interface send functions are moving towards or already in the end state selected by major opcode2-0 when ending during STATE, EXECUTE or SCAN commands.

alive

This status bit indicates the state of major commands.

0 No command is alive.

A major command is alive.

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BIT	DESCRIPTION
0	Target Interface State0
1	Target Interface State1
2	Target Interface State2
3	Target Interface State3
4	Null
5	Null
6	Null
7	Null
8	Write OK Inverted
9	Write Empty Inverted
10	Null
11	Null
12	Read OK
13	Read Full
14	Null
15	Null

status2 register bit description

The host may only read the status2 register. It is used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The status2 register address (ADRS4-ADRS0) is 10010.

These bits are loaded from the internal status signals by an OPERATE2 command.

target interface state2-0

These bits indicate which stable state the target interface is sending.

000	Test-Logic-Reset.
001	Test-Logic-Reset.
010	Run-Test/Idle.
011	Run-Test/Idle.
100	Shift-DR.
101	Shift-IR.
110	Pause-DR.
111	Pause-IR.

target interface state3

This bits indicates if the target interface is sending a stable state or a temporary state.

- 0 The target is in the stable state indicated by bits 2-0.
- 1 The target interface is in a temporary state and bits 2-0 are all zeroes.

write OK inverted

This bit indicates the status of the write buffer at all times. It is active if at least one word of the buffer is empty.

O At least one word of the serial write buffer is empty.

1 The serial write buffer is full.



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status2 register bit description (continued)

write empty inverted

This bits indicates the status of the write buffer at all times. If the buffer is empty, two words may be written into it

0 The serial write buffer is empty.

1 The serial write buffer is not empty.

read OK

This bit indicates the status of the read buffer at all times. When active, at least one word is full and may be read.

0 The serial read buffer is empty.

At least one word of the serial read buffer is full.

read full

1

The status of this bit indicates the condition of the serial read buffer at all times.

At least one word of the serial read buffer is empty.

Both words of the serial read buffer are full.

status3 register bits

BIT	DESCRIPTION
0	Null
1	Null
2	Null
3	Null
4	Null
5	Null
6	Null
7	Null
8	Null
9	Null
10	Null
11	Null
12	Null
13	Null
14	Null
15	Null

status3 register bit description

The status3 register address (ADRS4-ADRS0) is 10011.

All bits in this register are null; writes have no effect and reads obtain zeroes.

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capture0, cap	oture 1	reaister	bits
---------------	---------	----------	------

DIT	BIT DESCRIPTION		
DII	CAPTURE0	CAPTURE1	
0	Capture0	Capture16	
1	Capture1	Capture17	
2	Capture2	Capture18	
3	Capture3	Capture19	
4	Capture4	Capture20	
5	Capture5	Capture21	
6	Capture6	Capture22	
7	Capture7	Capture23	
8	Capture8	Capture24	
9	Capture9	Capture25	
10	Capture10	Capture26	
11	Capture11	Capture27	
12	Capture12	Capture28	
13	Capture13	Capture29	
14	Capture14	Capture30	
15	Capture15	Capture31	

capture 1-0 registers bit description

The host may only read the capture1-0 registers. They are used to examine the 'ACT8990 during and after commands. The bits are altered by the device when an OPERATE2 command occurs. The capture0 register address (ADRS4-ADRS0) is 10100. The capture1 register address (ADRS4-ADRS0) is 10101.

These registers hold the value of counter1. They are loaded from counter1 by an OPERATE2 command or when the capture enable1 bit is set.

capture 15-0

The capture0 register stores the current value of the counter1 least significant word. Bits 0 and 15 are the least and most significant bits, respectively. Reset causes this register to reset to all zeroes.

capture31-16

The capture1 register stores the current value of the counter1 most significant word. Bits 16 and 31 are the least and most significant bits, respectively. Reset causes this register to be reset to all zeroes.

SN54ACT8990, SN74ACT8990 TEST BUS CONTROLLERS

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PRODUCT PREVIEW read buffer register bits

BIT	DESCRIPTION
0	Read Buffer0
1	Read Buffer1
2	Read Buffer2
3	Read Buffer3
4	Read Buffer4
5	Read Buffer5
6	Read Buffer6
7	Read Buffer7
8	Read Buffer8
9	Read Buffer9
10	Read Buffer10
11	Read Buffer11
12	Read Buffer12
13	Read Buffer13
14	Read Buffer14
15	Read Buffer15

read buffer register bit description

The host may only read this register. It is used to access the read buffer used by the SCAN commands. The read buffer register address (ADRS4-ADRS0) is 10110.

read buffer15-0

These bits are the most significant word of the two words that make up the read buffer.

write buffer register bits

BIT	DESCRIPTION	
0	Write Buffer0	
1	Write Buffer1	
2	Write Buffer2	
3	Write Buffer3	
4	Write Buffer4	
5	Write Buffer5	
6	Write Buffer6	
7	Write Buffer7	
8	Write Buffer8	
9	Write Buffer9	
10	Write Buffer10	
11	Write Buffer11	
12	Write Buffer12	
13	Write Buffer13	
14	Write Buffer14	
15	Write Buffer15	

write buffer register bit description

The host may only write to this register. It is used to access the write buffer used by the SCAN commands. The write buffer register address (ADRS4-ADRS0) is 10111.

write buffer15-0

These bits are the most significant word of the two words that make up the write buffer.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC		
Input voltage range, V _I (see Note 1)	V to VCC	+ 0.5 V
Output voltage range, VO (see Note 1)0.5	V to VCC	+ 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$)		±50 mA ■
Continuous output current, IO (VO = 0 to VCC)		±50 mA ▶
Continuous current through VCC or GND pin	±	± 200 mA 🕻
Storage temperature range	-65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN	SN54ACT8990		SN74ACT8990			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNII	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	٧	
VIH	High-level input voltage	2			2			٧	
VIL	Low-level input voltage			0.8			0.8	٧	
٧ı	Input voltage	0		VCC	0		Vcc	٧	
۷o	Output voltage	0		Vcc	0		Vcc	٧	
ЮН	High-level output current			-8			-8	mA	
lOL	Low-level output current			8			8	mA	
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V	
TA	Operating free-air temperature	-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADALIETEO		7507 001101710110	TA = 25°C SN54		SN54AC	T8990	SN74AC	T8990			
PARAMETER Vo		Vcc	TEST CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN MAX		UNIT	
		457	IOH = -20 μA	4.4			4.4		4.4			
۷он		4.5 V	IOH = -8 mA	3.7			3.7		3.7		٧	
		5.5 V	IOH = -20 μA	5.4			5.4		5.4			
		4.5 V to 5.5 V	IOL = 20 μA			0.1		0.1		0.1	V	
VOL	4.5 V to 5.5 V	IOL = 8 mA			0.5		0.5		0.5	. •		
	ADRS, RD, WR, TCKI	5.5 V	V _I = V _{CC} or GND			±1		±1		±1	μΑ	
lj .	All ash are	EEV	VI = VCC			±1		±1		±1	A	
	All others	5.5 V	VI = GND		-70						μΑ	
	TDO, TMS, INT, RDY	5.5 V	VO = VCC or GND			±10		±10		±10	μΑ	
IOZ All others†		5.5 V	VO = VCC			±10		±10		±10		
		5.5 V	VO = GND		-70						μΑ	
ICC		5.5 V	$V_I = V_{CC}$ or GND, $I_O = 0$					450		450	μΑ	

[†] For I/O ports, the parameter IOZ includes the input leakage current.

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=	timina	requirements	over	recommended	operating	free-air	temperature	range	(see	Note	2)
	unning	requirements	OAGI	recommenueu	operaning	II ee-ali	tellipel atul e	ıanye	(366	HOLE	41

			SN54AC	T8990	SN74AC	T8990	
			MIN	MIN MAX		MAX	UNIT
fclock	Clock frequency						MHz
		TCKI high or low					
	Pulse duration	TRST low					
tw	Puise duration	WR low					ns
		EVENT3-0 high or low					
	TDI1-0 before TCKI↑						
t _{su}	Setup time	EVENT3-0 before TCKI ↑					ns
		ADRS4-0 and DATA15-0 before WR↑					
		TDI1-0 after TCKI↑					
th	Hold time	EVENT3-0 after TCKI↑					ns
		ADRS4-0 and DATA15-0 after WR↑					
		TRST high to RDY low					
t _r	Recovery time	WR ↑ to RDY low					ns
		RD↑ to RDY low					

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V

DADAMETED	FROM	то	SN54AC	T8990	SN74AC	T8990	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
f _{max}	TCKI	1					MHz
tPLZ	TRST↓	RDY, INT, DATA15-0					
tPHZ	IH211	ADY, INT, DATA15=0					ns
tPZL	TRST↓	RDY, INT, DATA15-0					
^t PZH	1001 \$	AD1, IN1, DA1A15=0					ns
†PLZ	TRST ↓	TMS/EVENT					ns
^t PHZ		TWIS/EVENT					110
tPZL	TRST ↓	TMS/EVENT					ns
^t PZH	11101 \$	TM6/EVEN1					110
tPLZ	RD↑	DATA15-0					ns
tPHZ	101	BATA10-0					110
[†] PZL	RD↑	DATA15-0					ns
tPZH		DATA15=0					113
tPLZ	TCKI ↓	TCKO, TMS5-0, TDO					ns
tPHZ	101114	10KG, 1MG5-0, 12G					113
[†] PZL	TCKI ↓	TCKO, TMS5-0, TDO					ns
^t PZH		10KG, 1MG5 6, 126					
^t PLZ	TOFF ↓	TCKO, TMS5-0, TDO					ns
[†] PHZ		1010, 11100 0, 120					
tPZL	TOFF ↓	TCKO, TMS5-0, TDO					ns
tPZH		Toke, thice o, the					
tPLZ	TCKÎ ↓	EVENT3-0					ns
tPHZ		272.110					
tPZL	тскі ↓	EVENT3-0					ns
tPZH	, U						
tPLZ	TOFF ↓	EVENT3-0					ns
tPHZ	.311.						
tPZL	TOFF J	EVENT3-0					ns
^t PZH							,,,

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switching characteristics over recommended operating free-air temperature range, VCC = 5 V \pm 0.5 V (continued)

DADAMETED	FROM	то	TO SN54ACT8990 SN74		SN74AC	T8990	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MIN MAX MIN		MAX	UNIT
^t PLH	TRST ↑	INT, RDY					
tPHL	inoi j	INT, ADT					ns
tPLH	TRST↓	TDO, TMS1-0					ns
tPLH	ADRS4-0	DATA15-0					
tPHL	ADR34-0	DATA15-0					ns
tPLH	WR↑	RDY					
tPHL	AAL!	nD1					ns
tPLH .	RD↓	DATA15-0					
tPHL	µn1	DATA15-0					ns
tPLH	RD↑	RDY					ns
tPHL	RDY ↓	RD					ns
tPLH .	TCKI	ĪNT					
tPHL	TON	INI					ns
tPLH	тскі↓	TCKO, TMS5-0, TDO					
tPHL	1001	1CKO, 1M95-0, 1DO					ns
tPLH	TOFF ↑	TCKO, TMS5~0, TDO					
tPHL	IOFF	1CKO, 1M95-0, 1DO					ns
tPLH .	тскі↓	EVENT3-0					
tPHL	IONIT	EVEN13-U					ns
tPLH .	TOFF ↑	EVENTO O					
tPHL	TOFF	EVENT3-0					ns

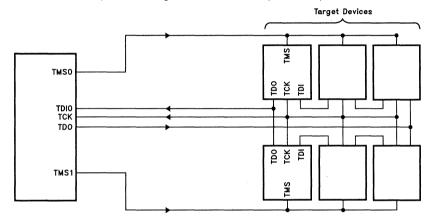
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APPLICATION INFORMATION

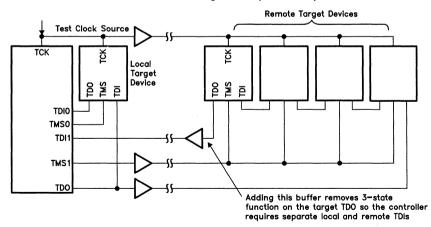
direct links

A direct link is a connection between the 'ACT8990 and targets that does not delay the target interface signals more than one clock period. Typically, it is pin to pin or uses TTL buffer devices. This method is used when the output buffer delay plus external buffer and cable delays meet the required setup timing values.

A direct link to a target is shown in Figure 23. The 'ACT8990 TDI, TDO, and TMS pins are connected to the TDO, TDI, and TMS pins of the target. The test clock is input and output on the TCKI and TCKO pins.



Two Parallel Chains of Targets with Separate TMS Inputs



Local and Remote Targets with Separate TMS Inputs and TDO Outputs

FIGURE 23. DIRECT LINKS TO TARGETS



APPLICATION INFORMATION (continued)

retimed links

A retimed link is an arrangement of one or more flip-flops in the connection between the 'ACT8990 and the target. Retimed links buffer and retime the target interface signals to meet the proper setup and hold time requirements between the 'ACT8990 and its targets. This may be required when the clock rate is high and either the target is at a distance or the connection involves fanout or TTL buffer devices. The length of the link is the total number of flip-flops in the outgoing and return paths. The 'ACT8990 supports retimed links up to 31 bits long.

A retimed link to a target is shown in Figure 24. The TDI, TDO, and TMS pins of the 'ACT8990 are connected to the target TDO, TDI, and TMS pins. The test clock is input and output on the TCKI and TCKO pins. The presence of the flip-flops delays the signals at the TDI1-0 and EVENT3-0 pins relative to the target interface state at the TMS5-0 and TDO outputs. To provide the major commands, data buffers and shifter-FIFO with the delayed mode source signal required to operate with retimed links, the mode source is passed through a link delay register whose length, set by the link delay4-0 control bits, matches the link itself. This is shown in Figure 8.

The STATE command finishes only when the requested state and equal numbers of temporary states have been sent and returned so that the whole link is in one stable state.

The EXECUTE command allows only one contiguous block of execute states to be outstanding in the retimed link. It decodes the mode source and the delayed mode source to identify execute states as they are sent and returned. This ensures that the end of a prior block of states being returned has been reached before the next block of states is sent. This command finishes only when the requested end state and equal numbers of temporary states have been sent and returned so that the whole link is in one stable state.

The SCAN command does not allow the number of outstanding data bits (the difference between the number of bits sent on TDO and the number of bits received on TDI) to exceed the shifter-FIFO length selected by the serial length control bit (control4 register bit 5). The number of outstanding data bits is counted by decoding the mode source and the delayed mode source to identify scan states as they are sent and returned. The SCAN command is used to control the operation of the shifter-FIFO. The scan command finishes only when the requested end state has been sent and returned so that the whole retirned link is in one stable state.

For retimed links shorter than the selected shifter-FIFO length, the 'ACT8990 scans data continuously without suspending the SCAN command. This is because it sends data bits from the shifter-FIFO until matching data bits are returned from the target. The 'ACT8990 compensates for the delay of data within the link without a reduction in the data transfer rate.

For retimed links longer that the selected shifter-FIFO length, the 'ACT8990 scans data in bursts and periodically suspends the SCAN command. This is because all of the data bits from the shifter-FIFO are sent before matching data bits are returned from the target. The 'ACT8990 compensates for the delay of data within the link, but at a reduced data transfer rate. The host sees this as a slowing in the filling and emptying of the data buffer as the suspend and resume commands are handled with the 'ACT8990.

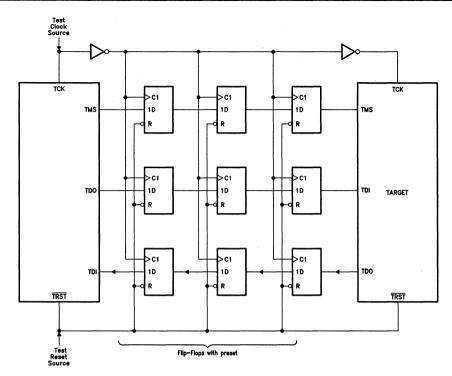


FIGURE 24. RETIMED LINK TO TARGET

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APPLICATION INFORMATION (continued)

target switching

When the 'ACT8990 is linked to several parallel targets, its architecture allows the host to operate on them individually or in groups. A target may be operated on individually by setting the corresponding connect mode control bit to one while holding the other targets in some selected stable state with their connect mode control bits set to zero. Targets may be operated on as a group when the connect mode control bits for all targets in the group are set to one and all other connect mode control bits are set to zero.

Target switching is the method provided to suspend operations on one target and resume operations on any other target. To support target switching, the host must maintain records of the stable state, the link delay value, and the shifter string value for the targets that it is not currently operating on.

When the host decides to suspend operations on target A, it allows any major command that is alive to finish (end state). The connect data1 control bit is set to zero to disconnect all TMS pins and enter the loopback mode. The data in the shifter-FIFO from target A is stored and replaced with the data from target B by a short SCAN command whose end state matches that of target B. The link delay4–0 control bits and connect mode5-0 bits are set to match the link to target B. The connect data1 control bit is set to one to connect all TMS pins and target B may be operated on.

SN54ACT8994 ... FK PACKAGE SN74ACT8994 ... FN PACKAGE

(TOP VIEW)

D1∏5

DO 🗌 6

CLK1 17

CLK2 8

CLK3 9

TMS | 10

TCK | 11

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D8

24 TD9

22 | D11

20 □ D13

19∏D14

21 | D12

23 TD10

- Members of the Texas Instruments SCOPE™ Family of Testability Products
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Operation is Synchronous to the JTAG Test Clock (Offline Mode) or System Clock(s) (Online Mode)
- Each Contain a 1024-Word by 16-Bit Random-Access Memory (RAM) to Store the States of a Digital Bus
- Direct Memory Access (DMA) Speeds Memory and Register File Read/Write Operations
- Perform Parallel Signature Analysis (PSA) of Inputs with User-Definable Tap Bits
- Inputs Are Maskable During PSA Operations
- Cascaded PSA Mode Allows Compression of Data Paths > 16 Bits in Width
- Compatible with Ti's ASSET™ (Automated Support System for Emulation and Test) Software
- Each Contain Ti's Event Qualification Module for Real-Time System Test
- Eight Protocols for On-line Signal Monitoring and Test Operations
- Inputs are TTL-Voltage Compatible
- Power-Down Mode When RAM is Idling Reduces Power Dissipation
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic and Ceramic Chip Carriers

description

The 'ACT8994 digital bus monitor (DBM) is designed to monitor and/or store the value of a digital bus up to sixteen bits in width. It resides in parallel with the bus being monitored.

Data clocked into the device can be stored in a scannable random-access memory (RAM). Up to 1024 words of sixteen bits can be stored. A parallel signature analysis (PSA) can also be performed on the data or on the contents of the memory. This allows the designer to check the signature after a predetermined number of clock cycles and examine up to 1024 prior patterns if an error is detected.

The 'ACT8994 can be operated in an on-line or off-line mode. In the on-line mode, the device operates synchronously to one or more of the external clock (CLK1-CLK3) inputs and/or the JTAG test clock (TCK) generated by the programmable clock interface (PCI) circuit, which allows real-time system tests to be performed by using the system clock(s) to control operation of the device.

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TI0285-D3604, JULY 1990

description (continued)

In the off-line mode, the device operates synchronously to TCK according to IEEE Standard 1149.1. The test access port (TAP) monitors TCK and the level of the test mode select (TMS) input to issue control signals and direct the device through its states (see Figure 1).

In the on-line mode, the event qualification module (EQM) allows data sample, storage, and/or PSA operations to be performed according to one of eight protocols. Register files in the EQM store compare patterns that allow the user to define specific values of the 16-bit bus for which the test operations are to be performed. Additional register files are provided for data mask patterns that cause the device to ignore data appearing on any combination of the data (D) inputs. Event-qualification-in (EQI) and event-qualification-out (EQO) pins allow global event qualification test schemes to be developed. Eight event-qualification protocols include various start/stop, start/pause/resume, and do-while algorithms.

The 1024-word by 16-bit RAM can be serially written to or read from one address at a time or via direct memory access (DMA) instructions provided to speed transfer of large amounts of data to and from the RAM. DMA is also implemented for accessing the register files in the EQM. IEEE Standard 1149.1-compatible read and write instructions are included.

There are two methods for initiating 'ACT8994 DMA operations. The first method monitors the serial data stream on the test data in (TDI) input and starts DMA when an expected 8-bit pattern is recognized. The second method initiates DMA when the TAP enters the Shift-DR TAP state from Pause-DR.

Many of the functional characteristics of the 'ACT8994 are user-definable, greatly increasing the flexibility and versatility of the device. Any combination of data bits can be masked from PSA and/or storage operations, and the user defines the tap bits for parallel signature generation. Many of the internal error and status signals can be output via EQO to monitor real-time test operations.

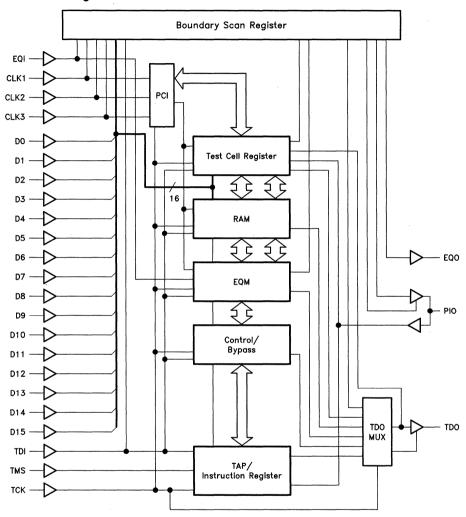
The RAM can be powered down when it is not being accessed, greatly decreasing total power dissipation.

The polynomial input/output (PIO) is a bidirectional pin used when cascading more than one DBM in a PSA operation. PIO is used as a feedback TAP for the PSA algorithm.

The device contains nine serial shift registers. For all registers, the most significant bit (MSB) is defined to be the bit nearest TDI. The least significant bit (LSB) is defined to be the bit nearest test data out (TDO).

The SN54ACT8994 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ACT8994 is characterized for operation from 0°C to 70°C.

functional block diagram



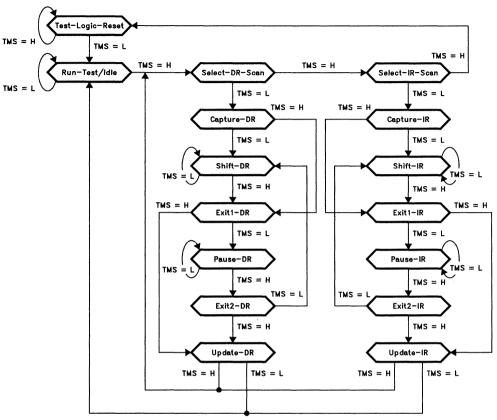


FIGURE 1. TAP STATE DIAGRAM

signal descriptions

TDI—Test Data In

One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting data through the instruction register or one of the data registers. An internal pullup forces TDI high if left floating or if a board continuity failure leaves the pin open.

TDO-Test Data Out

One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting data through the instruction register or data registers.

TCK-Test Clock

One of the four pins required by IEEE Standard 1149.1. Operation of the 'ACT8994 in the off-line mode is synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.

TMS-Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8994 through its states (see Figure 1). An internal pullup forces TMS high if left floating or if a board continuity failure leaves the pin open.

D15-D0-Data Inputs

This sixteen-bit bus inputs data to be compressed and/or stored. Each bit can be individually masked so that it is not comprehended during test operations.

CLK1/CLK2/CLK3—Clock 1-Clock 3

In the on-line mode, operation of the 'ACT8994 is synchronous to one or a combination of these clocks and/or TCK. The programmable clock interface (PCI) circuit monitors the clock inputs and issues the online clock to the device.

PIO-Polynomial Input/Output

This I/O pin is used when cascading more than one DBM to provide signature analysis on more than sixteen bits. Its configuration as an input or output depends on the significance (most, middle, or least) of the DBM in the scan path.

EQI—Event Qualification In

This pin accepts data from the outside world when the 'ACT8994 operates in the on-line mode. This allows test operations to be performed when a user-defined condition exists. Eight protocols for on-line test operations are implemented in the 'ACT8994.

EQO—Event Qualification Out

This pin outputs signals when certain conditions have been observed. It can be configured to output sixteen different error and status signals during on-line monitoring. When more than one DBM is in use, the EQO outputs are typically wire-ANDed or wire-ORed together to implement global qualification schemes.

state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. No more than one register should be manipulated at a time.

The function performed in any state occurs on the rising edge of TCK after the state is entered, and the function is also performed on the rising edge of TCK on the cycle in which the TAP state changes. For example, the first shift operation in Shift-DR occurs on the first rising edge of TCK after the TAP has entered Shift-DR from either Capture-DR or Exit2-DR and the last shift occurs on the rising edge of TCK in which the TAP state changes from Shift-DR to Exit1-DR.

Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Passing through the Test-Logic-Reset state is equivalent to a power-down/power-up operation. All registers are set to their reset values during Test-Logic-Reset.

Run-Test/idle

The TAP must pass through this state before executing any test operations. Storage and PSA operations in the off-line mode are executed in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP exits either of them on the next TCK cycle. These states are provided to steer the TAP to the data and instruction register shift states.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by the selected register on the rising edge of TCK in Capture-DR.

Shift-DR

In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK rising edge after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

On the falling edge of TCK as the TAP enters Shift-DR from Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO enables to the level dictated by the LSB of the selected data register. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO enables to a low level as the bypass register, which preloads with a logic 0, is selected after a reset.

If the TAP enters Shift-DR from Exit2-DR, TDO enables to the value present before it was last disabled.

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During DMA operations, data is transferred to or from the RAM or register files while the TAP is in the Shift-DR state. During a DMA write operation, data is serially input via TDI but is not shifted out via TDO. When a DMA write operation is active, the value of TDO is unknown.

During a DMA read operation, data is serially output via TDO and TDI is ignored.

state diagram description (continued)

During DMA operations, data is transferable. Shift-DR state. During a DMA write operation is active, in the properties of the properties of the properties.

During a DMA read operation, data is selected by the properties of the properties. These are temporary states used to ensure the properties of the high-impedance state on the falling the properties.

Pause-DR

The TAP can remain in this state independent. These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

When the TAP state changes from Shift-DR to Exit1-DR, the last shift occurs on the TCK cycle in which

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data. The device can also be configured to begin DMA read or write operations on either the RAM or the EQM register files if the TAP enters Pause-DR and then returns to Shift-DR via Exit2-DR.

Update-DR

If the current instruction calls for the shadow latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state.

Capture-IR

The instruction register is preloaded with the IR status word (see instruction register description) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP enters Shift-IR from Capture-IR, TDO enables to a high level. If the TAP enters Shift-IR from Exit2-IR, TDO enables to the value present before it was last disabled.

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to

When the TAP state changes from Shift-IR to Exit1-IR, the last shift occurs on the TCK cycle in which the state changes.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data. EQO can be configured to output an error signal during Pause-IR if an invalid instruction has been loaded.



state diagram description (continued)

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction. If an invalid instruction is present in the IR and the TAP enters this state, the BYPASS instruction is executed. If the TAP does not pass through Test-Logic-Reset before the next Capture-IR TAP state, Bit 7 of the IR preloads with a logic 0 during Capture-IR.

TARI	F 1	REGISTER	SHMMARY

REGISTER NAME	SYMBOL	LENGTH (BITS)	FUNCTION/CONTENTS	
Instruction	IR	8	Issue command and control information to the device	
Test Cell	TCR	16	PSA operations, compare functions on D inputs	
Control	CTLR	45	Configuration and enable control, data mask and PSA tap bits	
RAM	RAMR	26/16 [†]	Address and read/write data for 1024 x 16 RAM	
Event Qualification 1	EQR1	32	Control signals, EQM test instruction, 16-bit loop counter	
Event Qualification 2	EQR2	56/48†	Address and data for event count, expected data, and compare mask data	
Boundary Scan	BSR	24	Capture and force test data at I/O periphery	
Header	HR	8	DMA triggering/compare pattern	
Bypass	BR	1	Removes the 'ACT8994 from the scan path	

[†] The length of this register depends on the current instruction. See Instruction register opcode descriptions for details.

'ACT8994 registers

The device contains nine serial shift registers that contain the configuration data needed to run various test operations. Included in the registers are one eight-bit instruction register and eight data registers of varying lengths. Any register can be accessed via the TAP to load new data and/or examine existing data. Table 1 summarizes the registers, and Figure 2 shows how the data registers are connected. The select signals for MUX1 in the diagram are determined by the current instruction. The select signal for MUX2 is issued by the TAP. Unless one of the four DMA instructions is active, one of the registers between TDI and TDO is always selected for shift operations.

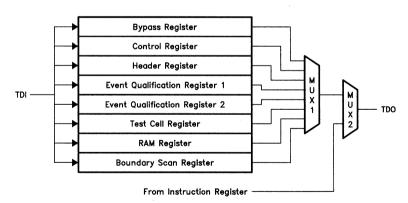


FIGURE 2. DATA REGISTER DIAGRAM

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instruction register description

The eight-bit instruction register (IR) contains the current instruction to the device. All operations of the device are dependent on the current instruction, which is decoded and latched to provide the proper control and enable signals for the test operation to be performed. The instructions supported in the 'ACT8994, a description of the test, and the selected data register (i.e., the data register placed between TDI and TDO for any subsequent shift operations) are shown in Table 2.

The reset value of the IR is 81h. (In this datasheet, the values of registers are often given in hexadecimal format, indicated by the 'h' following the value.) During Capture-IR, the instruction register preloads with the IR status word (see Table 3), which contains two status bits. IRERR and OVF.

All valid instructions exhibit even parity. If the IR value does not exhibit even parity and the TAP enters the pause-IR state, the error signal IRERR (a logic 0) is generated and is output via EQO if the appropriate bits in the control register are set. If an invalid instruction is updated, IRERR stays active and is loaded into bit 7 of the IR during the next Capture-IR TAP state (unless the TAP passes through Test-Logic-Reset in the interim). When an invalid instruction is loaded (i.e., when the TAP enters Update-IR while an invalid instruction is in the IR), the BYPASS instruction is executed.

The overflow (OVF) status signal is generated if the RAM address counter is incremented past its maximum value of 3FFh during a DMA or storage operation. OVF is active-high and is written to bit 6 of the IR during Capture-IR. A bit in the control register can be set to prohibit the address counter from overflowing, but OVF is still asserted if the test attempts to do so.

Figure 3 shows the instruction register bits and order of scan.

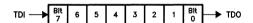


FIGURE 3. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

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TABLE 2. INSTRUCTION REGISTER OPCODES

BINARY	HEV VALUE	INICTOLICAL	CELECTED DATA DEGLESTS
OPCODE	HEX VALUE	INSTRUCTION	SELECTED DATA REGISTER
00000000	00h	EXTEST	Boundary Scan
10000001	81h	BYPASS	Bypass
10000010	82h	SAMPLE/PRELOAD	Boundary Scan
00000011	03h	BYPASS	Bypass
10001000	88h	RUNN	Bypass
00001001	09h	RUNT	Bypass
10001110	8Eh	SCANCN	Control
00010001	11h	SCANEQN	Event Qualification 1
01100000	60h	READFILE	Event Qualification 2
11100001	E1h	WRITEFILE	Event Qualification 2
11100010	E2h	READRAM	RAM
01100011	63h	WRITERAM	RAM
11100100	E4h	DMARIN	RAM†
01100101	65h	DMAROUT	RAM†
01100110	66h	DMAFIN	Event Qualification 2†
11100111	E7h	DMAFOUT	Event Qualification 2 [†]
11101000	E8h	SCANTCR	Test Cell
01101001	69h	READTCR	Test Cell
01101010	6Ah	INITRAM	Bypass
11101011	EBh	TOGRAM	Bypass
01101100	6Ch	PSARAM	Bypass
11101101	EDh	SCANHDR	Header
All other		BYPASS	Bypass

[†] DMA instructions are executed while in the Shift-DR TAP state and the normal TDI-TDO data flow is inhibited. The indicated data register is selected only if the TAP leaves and re-enters Shift-DR without loading a new instruction. If this happens, the DMA operation is aborted.

TABLE 3. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUE‡
7	IRERR
6	OVF
5	0
4	0
3	0
2	0
1	0
0	1

[‡] This value is loaded in the instruction register during the Capture-IR TAP state. The reset value of IRERR = 1. The reset value of OVF = 0.

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register scan timing

Figure 4 shows a timing diagram that illustrates an instruction register scan and a data register scan (in this case, the bypass register) with the TAP beginning in the Test-Logic-Reset state. All register scans, with the exception of the DMA instructions, are executed in the same fashion. Note that the value of TDI is a "don't care" until the first TCK rising edge after the TAP enters Shift-IR or Shift-DR (because the first shift does not occur until then) and that the last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR or from Shift-DR to Exit1-DR. Also note that TDO is active only when the TAP state is Shift-IR or Shift-DR.

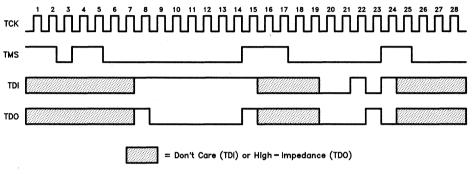


FIGURE 4. REGISTER SCAN TIMING

Other concepts are illustrated in the figure. As a BYPASS instruction (FFh) is shifted into the IR, the reset IR status word (81h) is shifted out via TDO. After the IR is updated with BYPASS (cycle 16), the TAP moves through Select-DR-Scan and Capture-DR to Shift-DR and data is shifted through the bypass register. Since the bypass register is one bit wide (see **bypass register description**), the data is delayed by one bit from TDI to TDO. Another important note is that the last bit shifted into the bypass register (a logic 1 during TCK cycle 24) is not shifted out to the next device in the scan path.

For both the instruction register scan and data register scan, TDO becomes active on the falling edge of TCK as the TAP enters the appropriate shift state. During the instruction register scan, TDO enables to a high level because the LSB of the instruction register always preloads with a logic 1. During the bypass register scan, TDO enables to a low level because the bypass register always preloads with a logic 0.

PRODUCT PREVIEW

instruction register opcode descriptions

The basic functions of each instruction are described herein. Example executions for several instructions follow data register descriptions.

FXTEST

The boundary scan register is selected in the scan path. Data appearing at the input pins is captured and data previously loaded into the output boundary scan cells is applied from the outputs.

BYPASS

The bypass register is selected in the scan path. All other registers retain their states.

SAMPLE/PRELOAD

Data appearing at the I/O pins is captured on the rising edge of TCK in Capture-DR. The boundary scan register is selected in the scan path.

RUNN

The test operation specified by OP3-OP0 (bits 44-41 in the control register) is performed in the on-line test mode as controlled by the EQM. While RUNN is executing, operation of the device, except for the TAP, is synchronous to the on-line clock generated by the PCI circuit.

Test operations running under RUNN become active at the falling edge of TCK in Update-IR and remain active until they either terminate normally according to the selected protocol (i.e., the protocol reaches END OF TEST) or a new instruction is loaded and updated. This allows RUNN to operate in the background mode. If an instruction register scan occurs while RUNN is active and the new instruction loaded and updated is also RUNN, no disruption in the on-line test will occur (cascaded PSA operations are affected, however. See **cascaded PSA operations**).

RUNT

The test operation specified by OP3-OP0 (bits 44-41 in the control register) is performed in the off-line test mode and is synchronous to TCK. Test operations running under RUNT are active only while the TAP is in the Run-Test/Idle state. The test begins on the first rising edge of TCK after entering Run-Test/Idle and terminates at either the end of the protocol or on the TCK cycle in which the TAP state changes to Select-DR-Scan.

SCANCN

The control register is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their states.

SCANEQN

The event qualification register 1 is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their states.

READFILE

The event qualification register 2 is configured as a 56-bit register and placed in the scan path. During the Capture-DR TAP state, the EQM register file data at the address appearing in bits 39 through 36 is loaded into bits 55 through 40 and the register file data at the address appearing in bits 3 through 0 is loaded into bits 35 through 20 (expected data) and 19 through 4 (compare mask data). During the Update-DR TAP state, the register file addresses for the next Capture-DR/Shift-DR operation are latched. The address and data are offset by one cycle, meaning that the data referenced by a particular address is loaded into the register during the next Capture-DR state.

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instruction register opcode descriptions (continued)

WRITEFILE

The event qualification register 2 is configured as a 56-bit register and placed in the scan path. During the Update-DR TAP state, the data in bits 55 through 40 is loaded into the EQM register file at the address appearing in bits 39 through 36 and the data appearing in bits 35 through 20 (expected data) and 19 through 4 (compare mask data) is loaded into the register file at the address appearing in bits 3 through 0.

RFADRAM

The RAM register is configured as a 26-bit register and placed in the scan path. During the Capture-DR TAP state, the RAM data at the address appearing in bits 9 through 0 is loaded into bits 25 through 10. During the Update-DR TAP state, the RAM address for the next Capture-DR/Shift-DR operation is latched. The address and data are offset by one cycle, meaning that the data referenced by a particular address is loaded into the RAM during the next Capture-DR state.

WRITERAM

The RAM register is configured as a 26-bit register and placed in the scan path. During the Update-DR TAP state, the data in bits 25 through 10 is loaded into the RAM at the address appearing in bits 9 through 0.

DMAFIN

During this DMA instruction, data is loaded via TDI into the register files adjacent to the event qualification register 2 for storing the event count, expected data, and compare data values. While DMAFIN is executing, the output from TDO is meaningless. DMAFIN executes while the TAP is in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAFIN is the current instruction, the event qualification register 2 is selected in the scan path and the register file write is aborted. During DMAFIN, the event qualification register 2 is configured as a 48-bit register (the eight address bits are disregarded).

DMAFOUT

The register files of event qualification register 2 are read using this DMA instruction. Data is output via TDO and the data at TDI is ignored. DMAFOUT executes in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAFOUT is the current instruction, the event qualification register 2 is selected in the scan path and the register file read is aborted. During DMAFOUT, the event qualification register 2 is configured as a 48-bit register (the eight address bits are disregarded).

DMARIN

During this DMA instruction, data is loaded via TDI into the RAM. While DMARIN is executing, the output from TDO is meaningless. DMARIN executes while the TAP is in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMARIN is the current instruction, the RAM register is selected in the scan path and the RAM write is aborted.

During DMARIN, the RAM register is configured as a 16-bit register (the ten address bits are disregarded).

DMAROUT

The RAM is read using this DMA instruction. Data is output via TDO and the data at TDI is ignored. DMAROUT executes in the Shift-DR state. If the TAP leaves and returns to Shift-DR while DMAROUT is the current instruction, the RAM register is selected in the scan path and the RAM read is aborted. During DMAROUT, the RAM register is configured as a 16-bit register (the ten address bits are disregarded).

SCANTCR

The test cell register is placed in the scan path. During Capture-DR, the data appearing at the D inputs is preloaded. All other registers retain their last states.



instruction register opcode descriptions (continued)

READTCR

The test cell register is placed in the scan path. During Capture-DR, the current value of the register is preloaded. All other registers retain their last states. This instruction is primarily useful for reading the results of a PSA operation.

INITRAM

The RAM register is configured as a 26-bit register and selected in the scan path. The value present in RAMR bits 25 through 10 is loaded into the RAM at consecutive addresses beginning with the address contained in RAMR bits 9 through 0. This instruction executes while the TAP is in the Run-Test/Idle state. On each TCK cycle, the RAM address is incremented and the data is loaded into the appropriate RAM location. The first pattern is written into the RAM on the first rising TCK edge after entering Run-Test/Idle, and the last pattern is written on the rising edge of TCK as the TAP state changes from Run-Test/Idle to Select-DR-Scan. The same pattern is written each time.

TOGRAM

The RAM register is selected in the scan path. This instruction is similar to INITRAM, the only difference being that the data to be loaded into the RAM (RAMR bit 25 through 10) is toggled on each TCK cycle. The first pattern written is the true data (the value loaded into the register during Shift-DR). This instruction is useful when a checkerboard pattern or alternating ones and zeroes are to be loaded into the RAM, usually for testing purposes.

PSARAM

The contents of the RAM are loaded into the test cell register on each TCK cycle while the TAP is in Run-Test/Idle. A PSA operation is performed on each pattern, and the resulting signature can be read using READTCR. This instruction is useful for performing a self-test on the RAM. By loading a known pattern or set of patterns using INITRAM or TOGRAM and following with PSARAM, the generated signature can be compared against a known value to verify the RAM functionality.

SCANHDR

The header register is selected in the scan path. All other registers retain their states.

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data register descriptions

The following sections contain descriptions of the various data registers in the 'ACT8994. The length of the register, order of scan, and function of the bits are explained. The use of many of the signals described will become apparent later in the datasheet.

control register description

The 45-bit control register (CTLR) issues configuration, control, and enable signals to the device. Table 4 lists the signals of the CTLR. The function of each signal is explained below.

Bits 44-41 OP3-OP0

These four bits control the test operation to be performed during RUNN and RUNT (see Table 15 and **RUNN, RUNT opcode descriptions**). The primary function of the 'ACT8994 is to execute various test operations according to OP3-OP0.

Bit 40 SELDP

During RUNN, either current or registered data may be input into the TCR and/or RAM. Current data is the data present at the D inputs at the rising edge of the clock issued by the PCI. Registered data is the data present at the prior rising edge of the clock. Using registered data allows the device to capture the pattern that preceded the expected data pattern.

If SELDP = 0, use current data as input.

If SELDP = 1, use registered data as input.

Bit 39 HALTM

The RAM can be configured to allow address rollovers (i.e., increment address from 3FFh to 000h) or to halt RAM writes after an address of 3FFh. When rollovers are not allowed, no additional writes to memory are performed after writing to address 3FFh and the address counter stops at 0000h. The overflow status bit, OVF (see instruction register description) is set independently of HALTM if an INITRAM, TOGRAM, or DMARIN instruction attempts to continue RAM writes after writing to address 3FFh.

If HALTM = 0, allow address counter to roll over after reaching 3FFh.

If HALTM = 1, do not allow additional RAM writes after reaching 3FFh.

Bit 38 PARENA

The parity error signal generated when an instruction is loaded (IRERR) can be output via EQO during the Pause-IR TAP state. PARENA enables and disables this function.

If PARENA = 0, disable parity error output from EQO.

If PARENA = 1, enable parity error output from EQO.

The polarity of the error signal (active-high or active-low) is determined by EQR1 bit 23.

Bit 37 CMPSEL

During RUNN, either current or registered data may input to the EQM to be compared against expected data during EQM-controlled test operations. Along with SELDP (CTLR bit 40), CMPSEL determines the alignment of data during on-line test operations. See alignment of compare and data signals under RUNN for illustrations of the use of current and registered data.

If CMPSEL = 0, use current data as compare input.

If CMPSEL = 1, use registered data as compare input.

control register description (continued)

trol register description (continued)

Bit 36 POLSEL

The polarity of the clock generated by the programmable clock interface (PCI) circuit is controlled by POLSEL. (Bits 35–32 determine the logic equation of the clock).

If POLSEL = 0, use true (noninverted) clock from PCI.

If POLSEL = 1, use inverted clock from PCI.

Bits 35-32 SELD-SELA

The PCI generates the internal clock signal for the on-line EQM protocols according to these four bits.

See Table 14 and PCI description for details.

Bits 31–16 PTAP15-PTAP00

The algorithm used to generate parallel signatures is partially configured using these bits. One of the inputs to the exclusive-OR gates used during PSA is a feedback bit from the LSB of a shift register. The

inputs to the exclusive-OR gates used during PSA is a feedback bit from the LSB of a shift register. The a PTAP bits determine which stages of the shift register use the feedback bit as an input.

If PTAPxx = 0, exclude the feedback bit from shift register stage xx.

If PTAPxx = 1, include the feedback bit from shift register stage xx.

See parallel signature analysis operations for details of the PTAP bits and their use.

Bits 15-0 DATMSK15-DATMSK00

Any combination of data inputs can be masked during parallel signature analysis operations in the TCR. The inputs are masked using the appropriate DATMSKxx signal. When an input is masked, it is ignored and has no effect on the generated signature.

If DATMSKxx = 0, include Dxx in PSA operation.

If DATMSKxx = 1, mask (exclude) Dxx from PSA operation.

During Capture-DR, the control register preloads with its current value. The reset value of the CTLR is 0000 0000 0000h. The register bits and order of scan are illustrated in Figure 5.

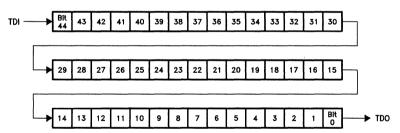


FIGURE 5. CONTROL REGISTER BITS AND ORDER OF SCAN

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TABLE 4. CONTROL REGISTER BITS

BIT NUMBER	SIGNAL	DESCRIPTION
44	OP3	RUNN, RUNT Opcode Bit 3
43	OP2	RUNN, RUNT Opcode Bit 2
42	OP1	RUNN, RUNT Opcode Bit 1
41	OP0	RUNN, RUNT Opcode Bit 0
40	SELDP	Current/Registered Data Select for TCR/RAM Input
39	HALTM	RAM Address Overflow Enable
38	PARENA	Instruction Register Parity Enable
37	CMPSEL	Current/Registered Data Select for EQM Compare
36	POLSEL	PCI Clock Polarity Select
35	SELD	PCI Clock Select D
34	SELC	PCI Clock Select C
33	SELB	PCI Clock Select B
32	SELA	PCI Clock Select A
31	PTAP15	PSA Tap for input D15
30	PTAP14	PSA Tap for input D14
29	PTAP13	PSA Tap for input D13
28	PTAP12	PSA Tap for input D12
27	PTAP11	PSA Tap for input D11
26	PTAP10	PSA Tap for input D10
25	PTAP9	PSA Tap for input D9
24	PTAP8	PSA Tap for input D8
23	PTAP7	PSA Tap for input D7
22	PTAP6	PSA Tap for input D6
21	PTAP5	PSA Tap for input D5
20	PTAP4	PSA Tap for input D4
19	PTAP3	PSA Tap for input D3
18	PTAP2	PSA Tap for input D2
17	PTAP1	PSA Tap for input D1
16	PTAP0	PSA Tap for input D0
15	DATMSK15	Data mask for PSA on input D15
14	DATMSK14	Data mask for PSA on input D14
13	DATMSK13	Data mask for PSA on input D13
12	DATMSK12	Data mask for PSA on input D12
11	DATMSK11	Data mask for PSA on input D11
10	DATMSK10	Data mask for PSA on input D10
9	DATMSK9	Data mask for PSA on input D9
8	DATMSK8	Data mask for PSA on input D8
7	DATMSK7	Data mask for PSA on input D7
6	DATMSK6	Data mask for PSA on input D6
5	DATMSK5	Data mask for PSA on input D5
4	DATMSK4	Data mask for PSA on input D4
3	DATMSK3	Data mask for PSA on input D3
2	DATMSK2	Data mask for PSA on input D2
1	DATMSK1	Data mask for PSA on input D1
0	DATMSK0	Data mask for PSA on input D0

event qualification register 1 description

The event qualification register 1 (EQR1) is a 32-bit register that contains select and enable signals for event-qualified testing. It also contains the 16-bit loop counter, which controls the number of times an EQM protocol is executed. Table 5 lists the EQR1 signals.

Bits 31-29 CMD2-CMD0

These three bits determine the event qualification protocol to be executed as shown in Table 17. See event qualification protocols.

Bit 28 SYNEOT

The EOT (end-of-test) signal is active while an event protocol is in the EOT state. It can be cleared synchronously (when a new protocol begins executing) or asynchronously (when the internal RUN signal becomes inactive), depending on the value of SYNEOT.

If SYNEOT = 0, clear EOT asynchronously.

If SYNEOT = 1, clear EOT synchronously.

Bit 27 RACDIS

The RAM address is cleared (set to 000h) at the beginning of an event protocol. RACDIS can be configured to disable this feature.

If RACDIS = 0, the RAM address clear is enabled.

If RACIDS = 1, the RAM address clear is disabled.

Bits 26-23 EQOSELD-EQOSELA

Several status signals and the instruction register parity error signal can be output via EQO during event-qualified testing. The EQO output signal is selected with these four bits according to Table 18.

Bits 22-20 EQISELC-EQISELA

The EQI (event) input to the EQM can be configured to input one of seven different signals during event-qualified testing. This signal is used as the event that triggers certain operations according to the protocol being executed. The input is configured according to these three bits as shown in Table 16.

Bit 19 LCNTDIS

The event loop counter keeps track of the number of times an event protocol has been executed and sets $\overline{\text{LCMIN}}$ low when the value of the counter decrements to one. The loop counter can be disabled with LCNTDIS. If LCNTDIS is set high, the protocol continues execution until a new instruction is loaded in the IR.

If LCNTDIS = 0, the event loop counter is enabled and decrements according to the protocol being executed.

If LCNTDIS = 1, the event loop counter is disabled and does not decrement. Under this condition, LCMIN never becomes active unless the loop counter was originally loaded with the value 0001h.

Bit 18 ECNTDIS

The event counter can be disabled using ECNTDIS in the same way as the loop counter can be disabled using LCNTDIS. When ECNTDIS is set high, the test specified during on-line testing is never executed because all protocols are triggered to begin an operation when the event counter has decremented to one. This feature is useful if EQO is being used to output an internal status signal related to the state of the bus being monitored.

If ECNTDIS = 0, the event counter is enabled and decrements each time an event is observed.

If ECNTDIS = 1, the event counter is disabled and ECMIN never becomes active.

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event qualification register 1 description (continued)

Bit 17 POPDIS

During protocol execution, new expected and compare data is often loaded after a protocol has completed a DO TEST loop. The loading of new data can be disabled with POPDIS. If the same expected and compare data are to be used throughout the protocol, setting POPDIS high reduces the amount of data that must be loaded in the EQM register files prior to test execution.

If POPDIS = 0, new data is loaded prior to each event protocol execution.

If POPDIS = 1, the current expected and compare data is used for each event protocol execution.

Bit 16 ENACMP

One of the signals that can be output via EQO is the compare term (CTERM), an asynchronous signal that is active (a logic 1) when the data appearing at the D inputs matches the expected value in the register file. This signal can be output as soon as a match is found (first matching pattern after RUNN has been updated in the IR) or when the event protocol starts execution (internal signal RUN goes active).

If ENACMP = 0, EQO becomes active after protocol execution begins.

If ENACMP = 1, EQO becomes active as soon as a match is found.

Bits 15-0 LCNT15-LCNT00

These bits contain the number of times the event protocol is to be executed. While an event protocol is active, these bits are configured as a counter and decrement prior to each execution. When the value of LCNT15-LCNT00 is 0001h, the status signal $\overline{\text{LCMIN}}$ becomes active (goes to a logic 0).

During Capture-DR, the EQR1 preloads with its current value. The reset value of the EQR1 is 0000 0000h. The register bits and order of scan are illustrated in Figure 6.

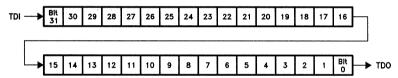


FIGURE 6. EVENT QUALIFICATION REGISTER 1 BITS AND ORDER OF SCAN

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TABLE 5. EVENT QUALIFICATION REGISTER 1 BITS

BIT NUMBER	SIGNAL	DESCRIPTION
31	CMD2	EQM Protocol Select 2
30	CMD1	EQM Protocol Select 1
29	CMD0	EQM Protocol Select 0
28	SYNEOT	Synchronous/Asynchronous End Of Test Flag
27	RACDIS	RAM Address Clear Strobe Disable
26	EQOSELD	EQO Select D
25	EQOSELC	EQO Select C
24	EQOSELB	EQO Select B
23	EQOSELA	EQO Select A
22	EQISELC	EQI Select C
21	EQISELB	EQI Select B
20	EQISELA	EQI Select A
19	LCNTDIS	Loop Count Disable
18	ECNTDIS	Event Count Disable
17	POPDIS	Expected and Compare Data Pop Disable
16	ENACMP	Compare Term Enable
15	LCNT15	Loop Count 15
14	LCNT14	Loop Count 14
13	LCNT13	Loop Count 13
12	LCNT12	Loop Count 12
11	LCNT11	Loop Count 11
10	LCNT10	Loop Count 10
9	LCNT09	Loop Count 09
8	LCNT08	Loop Count 08
7	LCNT07	Loop Count 07
6	LCNT06	Loop Count 06
5	LCNT05	Loop Count 05
4	LCNT04	Loop Count 04
3	LCNT03	Loop Count 03
2	LCNT02	Loop Count 02
1	LCNT01	Loop Count 01
0	LCNT00	Loop Count 00

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event qualification register 2 description

The event qualification register 2 (EQR2) is used to load the event counter and expected and mask data for event-qualified operations. Depending on the current instruction, it is either 48 or 56 bits in length and can be thought of as three 16-bit segments that hold data to be loaded into or out of register files and two four-bit segments that hold the register file address. One four-bit address segment serves the event counter and the other serves both the expected and mask data register files.

n During execution of the IEEE Standard 1149.1-compatible instructions READFILE and WRITEFILE, the register 📺 is 56 bits long. During the Capture-DR and Update-DR TAP states, the data appearing in the register's 16-bit m segments is loaded into or out of the address specified by one of the register's two four-bit seaments.

During execution of the DMA instructions DAMFIN and DMAFOUT, the register is 48 bits long, containing only m the three 16-bit data segments. Loading and unloading of the register files occurs in the Shift-DR TAP state as a continuous data stream is shifted in through TDI or out through TDO. On each 48th TCK, the data in the register is loaded into or out of the register file and the register file address is incremented for the next read or write.

Bits 55-40 EVCNT15-EVCNT00

These bits hold the data to be parallel-loaded into or out of the event counter register file.

Bits 39-36 EVADR3-EVADR0

These bits contain the address of the event counter register file.

Bits 35-20 EXPDATA15-EXPDATA00

These bits hold the data to be parallel-loaded into or out of the expected data register file.

Bits 19-4 MSKDAT15-MSKDAT00

These bits hold the data to be parallel-loaded into or out of the compare mask data register file.

ECADR3-ECADR0

These bits contain the address of the expected data and compare mask data register files. The same address is used for these registers for any of the four instructions that access the EQR2.

The three register files associated with the EQR2 are each 16 bits wide and 16 words deep. The register signals are shown in Table 6 and the register bits and order of scan are shown in Figure 7. Note that in two places (between bits 40 and 39 are between bits 4 and 3) the order of scan breaks in two. This illustrates the dependence of the register length on the instruction used to access it. The reset value of the EQR2 is 00 0000 0000 000h.

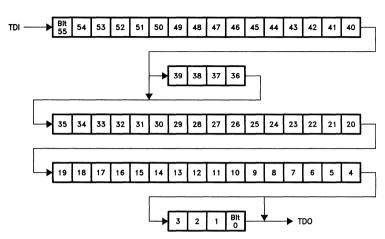


FIGURE 7. EVENT QUALIFICATION REGISTER 2 BITS AND ORDER OF SCAN

TABLE 6. EVENT QUALIFICATION REGISTER 2 BITS

BIT NUMBER	SIGNAL	DESCRIPTION	
55	EVCNT15	Event Counter Data 15	
54	EVCNT14	Event Counter Data 14	
53	EVCNT13	Event Counter Data 13	
52	EVCNT12	Event Counter Data 12	
51	EVCNT11	Event Counter Data 11	
50	EVCNT10	Event Counter Data 10	
49	EVCNT09	Event Counter Data 09	
48	EVCNT08	Event Counter Data 08	
47	EVCNT07	Event Counter Data 07	
46	EVCNT06	Event Counter Data 06	
45	EVCNT05	Event Counter Data 05	
44	EVCNT04	Event Counter Data 04	
43	EVCNT03	Event Counter Data 03	
42	EVCNT02	Event Counter Data 02	
41	EVCNT01	Event Counter Data 01	
40	EVCNT00	Event Counter Data 00	
39	EVADR3	Event Counter Address 3	
38	EVADR2	Event Counter Address 2	
37	EVADR1	Event Counter Address 1	
36	EVADR0	Event Counter Address 0	
35	EXPDAT15	Expected Data 15	
34	EXPDAT14	Expected Data 14	
33	EXPDAT13	Expected Data 13	
32	EXPDAT12	Expected Data 12	
31	EXPDAT11	Expected Data 11	
30	EXPDAT10	Expected Data 10	
29	EXPDAT09	Expected Data 09	
28	EXPDAT08	Expected Data 08	
27	EXPDAT07	Expected Data 07	
26	EXPDAT06	Expected Data 06	
25	EXPDAT05	Expected Data 05	
24	EXPDAT04	Expected Data 04	
23	EXPDAT03	Expected Data 03	
22	EXPDAT02	Expected Data 02	
21	EXPDAT01	Expected Data 01	
20	EXPDAT00	Expected Data 00	

TABLE 6. EVENT	QUALIFICATION	REGISTER 2	BITS ((continued)
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BIT NUMBER	SIGNAL	DESCRIPTION	
19	MSKDAT15	Mask Data 15	
18	MSKDAT14	Mask Data 14	
17	MSKDAT13	Mask Data 13	
16	MSKDAT12	Mask Data 12	
15	MSKDAT11	Mask Data 11	
14	MSKDAT10	Mask Data 10	
13	MSKDAT09	Mask Data 09	
12	MSKDAT08	Mask Data 08	
11	MSKDAT07	Mask Data 07	
10	MSKDAT06	Mask Data 06	
9	MSKDAT05	Mask Data 05	
8	MSKDAT04	Mask Data 04	
7	MSKDAT03	Mask Data 03	
6	MSKDAT02	Mask Data 02	
5	MSKDAT01	Mask Data 01	
4	MSKDAT00	Mask Data 00	
3	EMADR3	Expected and Mask Address 3	
2	EMADR2	Expected and Mask Address 2	
1	EMADR1	Expected and Mask Address 1	
0	EMADR0	Expected and Mask Address 0	

header register description

The header register (HR) is an eight-bit register used to initiate DMA write operations on the RAM and on the EQM register files. When a DMA write instruction (DMAFIN or DMARIN) is active, the DMA controller compares data being shifted from TDI to TDO against the current value of the HR. If the value of the HR is anything other than 00h, the DMA operation begins on the first TCK cycle after the DMA controller finds a match between the data flow and the HR.

When the value of the HR is 00h, DMA write operations are not initiated by the TDI-TDO data flow but when the TAP state changes from Shift-DR to Pause-DR and back to Shift-DR.

The reset value of the HR is 00h. Figure 8 shows the register bits and order of scan.

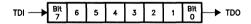


FIGURE 8. HEADER REGISTER BITS AND ORDER OF SCAN

RAM register description

The RAM register (RAMR) is used to load the address and data for RAM read and write operations. Depending on the current instruction, it is either 26 or 16 bits in length and can be thought of as one 16-bit segment that holds data to be loaded into or out of the RAM and one ten-bit segment that holds the RAM address.

During execution of the IEEE Standard 1149.1-compatible instructions READRAM and WRITERAM, the register is 26 bits long. During the Capture-DR and Update-DR TAP states, the data appearing in the register's 16-bit segment is loaded into or read from the RAM at the address specified by the register's ten-bit address segment.

During execution of the DMA instructions DAMRIN and DMAROUT, the register is 16 bits long, containing only the 16-bit data segment. Loading and unloading of the RAM occurs in the Shift-DR TAP state as a continuous data stream is shifted in through TDI or out through TDO. On each 16th TCK, the data in the register is loaded into or out of the RAM and the RAM address is incremented for the next read or write.

Bits 25-10 RAMDAT15-RAMDAT00

These bits hold the data to be parallel-loaded into or out of the addressed RAM location.

Bits 9-0 RAMADR9-RAMADR0

These bits contain the RAM address for read and write operations.

The RAM is 16 bits wide and 1024 words deep. The signals of the register are shown in Table 7 and the register bits and order of scan are shown in Figure 9. Just as with the EQR2, the break in data flow between bits 10 and 9 indicates the dependence of the register length on the current instruction.

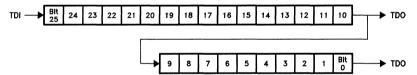


FIGURE 9. RAM REGISTER BITS AND ORDER OF SCAN

TABLE 7. RAM REGISTER BITS

BIT NUMBER	SIGNAL	DESCRIPTION
25	RAMDAT15	RAM Data 15
24	RAMDAT14	RAM Data 14
23	RAMDAT13	RAM Data 13
22	RAMDAT12	RAM Data 12
21	RAMDAT11	RAM Data 11
20	RAMDAT10	RAM Data 10
19	RAMDAT09	RAM Data 09
18	RAMDAT08	RAM Data 08
17	RAMDAT07	RAM Data 07
16	RAMDAT06	RAM Data 06
15	RAMDAT05	RAM Data 05
14	RAMDAT04	RAM Data 04
13	RAMDAT03	RAM Data 03
12	RAMDAT02	RAM Data 02
11	RAMDAT01	RAM Data 01
10	RAMDAT00	RAM Data 00
9	RAMADR9	RAM Address 9
8	RAMADR8	RAM Address 8
7	RAMADR7	RAM Address 7
6	RAMADR6	RAM Address 6
5	RAMADR5	RAM Address 5
4	RAMADR4	RAM Address 4
3	RAMADR3	RAM Address 3
2	RAMADR2	RAM Address 2
1	RAMADR1	RAM Address 1
0	RAMADR0	RAM Address 0

test cell register description

The test cell register (TCR) is a 16-bit register. It performs parallel signature analysis operations on the data inputs or the contents of the RAM and stores the resulting signature to be scanned out and compared against an expected value. The TCR can be accessed by two instructions, SCANTCR and READTCR.

The TCR also contains the results of the SAMPLE/PRELOAD instruction, in which the current value of the D15-D0 data bus is captured.

The reset value of the TCR is 0000h.

The register bits and order of scan are shown in Figure 10.

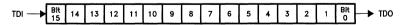


FIGURE 10. TEST CELL REGISTER BITS AND ORDER OF SCAN

boundary scan register description

The boundary scan register (BSR) is a 24-bit register that includes a boundary scan cell for all the non-JTAG I/O pins of the device and one internal directional signal for PIO. The BSR is used to capture the data appearing at the device periphery and to apply data from device outputs.

The reset value of the BSR depends on the current data at the I/O boundary.

Table 8 lists the signals of the BSR. The register bits and order of scan are shown in Figure 11.

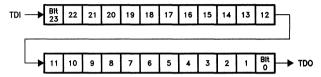


FIGURE 11. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

TABLE 8. BOUNDARY SCAN REGISTER CONFIGURATION

BIT NUMBER	SIGNAL	DESCRIPTION	
23	D15	Data Input 15	
22	D14	Data Input 14	
21	D13	Data Input 13	
20	D12	Data Input 12	
19	D11	Data Input 11	
18	D10	Data Input 10	
17	D9	Data Input 9	
16	D8	Data Input 8	
15	D7	Data Input 7	
14	D6	Data Input 6	
13	D5	Data Input 5	
12	D4	Data Input 4	
11	D3	Data Input 3	
10	D2	Data Input 2	
9	D1	Data Input 1	
8	D0	Data Input 0	
7	CLK3	Clock 3	
6	CLK2	Clock 2	
5	CLK1	Clock 1	
4	PIO_IN	PIO Input Signal	
3	PIO_OUT	PIO Output Signal	
2	ENPIO	PIO Direction Control	
1	EQI	Event Qualification Input	
0	EQO	Event Qualification Output	

bypass register description

The bypass register (BR) is a one-bit register required by IEEE Standard 1149.1. It is included to provide an abbreviated scan path through the 'ACT8994 when the current test operations do not require it to load or read one of the other registers.

The bypass register is the selected data register at power-up. The BR is also selected if an invalid instruction is loaded in the IR.

The BR preloads with 0h during the Capture-DR TAP state. The register bit is illustrated in Figure 12.



FIGURE 12. BYPASS REGISTER BIT AND ORDER OF SCAN

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instruction execution examples

The following section illustrates the execution of several instructions as well as the resulting data. For these examples, assume that the relevant instruction has been loaded and updated in the IR prior to the data that is shown in the example.

The WRITERAM instruction is illustrated by the data in Table 9. In the table, the term "scan sequence" means the data register Capture/Shift/Exit/Update sequence is used for scanning a data register and updating the contents. During each scan sequence, the data in bits 25 through 10 is loaded into the RAM at the address appearing in bits 9 through 0. Note that during scan sequence 4, RAM address 000h is written to a second time, erasing the data written during sequence 1.

The WRITEFILE instruction executes similarly to WRITERAM, with the event qualification register 2 being used to access the register files in the EQM.

TABLE 9. WRITERAM EXECUTION

204112501151125	RAM REGISTER C	ONTENTS	RAM CONTENTS†	
SCAN SEQUENCE	BITS 25 → 10	BITS 9 → 0	ADDRESS	DATA
1	0101 0101 0101 0101	00 0000 0000	00 0000 0000	0101 0101 0101 0101
2	1010 1010 1010 1010	00 0000 0001	00 0000 0001	1010 1010 1010 1010
3	1111 0000 1111 0000	00 0000 0010	00 0000 0010	1111 0000 1111 0000
4	0000 1111 0000 1111	00 0000 0000	00 0000 0000	0000 1111 0000 1111
5	1111 0000 0000 1111	00 0000 0011	00 0000 0011	1111 0000 0000 1111

[†] The RAM contents are updated on the falling edge of TCK in Update-DR.

Table 10 illustrates the offset between data and address used by the READRAM instruction. In this example, READRAM is used to read the contents of the RAM, which is assumed to be the data written using the WRITERAM instruction in the prior example.

Since the data read during the Capture-DR TAP state is taken from the current address (bits 9 through 0), scan sequence 1 is used to load the first address to be read and the remainder of the register is a "don't care". During scan cycle 2, two things happen. First, during Capture-DR, the data in RAM address 000h is preloaded into bits 25 through 10 of the register. Second, the next address to be read is scanned into the register during Shift-DR. The value scanned into bits 25 through 10 during Shift-DR is irrelevant since these bits will be overwritten with data from the RAM during the Capture-DR TAP state of scan sequence 3.

READFILE executes similarly to READRAM, with the event qualification register 2 accessing the EQM's register files.

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TABLE 10. READRAM EXECUTION

OO AN OF CUENOF	RAM REGISTER CONTENTS†		
SCAN SEQUENCE	BITS 25 → 10	BITS 9 → 0	
1	XXXX XXXX XXXX XXXX	00 0000 0000	
2	0000 1111 0000 1111	00 0000 0001	
3	1010 1010 1010 1010	00 0000 0010	
4	1111 0000 1111 0000	00 0000 0011	
5	1111 0000 0000 1111	XX XXXX XXXX	

[†] The data in bits 25 through 10 is the value of the RAM as captured in the register. The data in bits 9 through 0 is the next address to be read as scanned in via TDI

The READRAM, WRITERAM, READFILE, and WRITEFILE instructions are useful when a small amount of data is to be written to or read from the RAM or EQM register files and are provided for strict adherence to IEEE Standard 1149.1. However, DMA instructions are often more efficient when large amounts of data are to be transferred. DMAFIN, the DMA instruction to load the register files, is illustrated in Table 11. For this example, the user wishes to load the register files with all ones and then return to the Run-Test/Idle state. The table shows the procedure required to do this using DMAFIN. Recall that there are two methods to initiate DMA operations, one using the header register and one using the Pause-DR TAP state. This example initiates DMA using the Pause-DR method, which means that the value of the HR must be 00h (see header register description). Assume that at TCK cycle 0 the TAP is moving from Update-IR to Run-Test/Idle after having loaded and updated 66h (DMAFIN) in the IR.

TABLE 11. DMAFIN EXECUTION

TCK CYCLE	TMS‡	TDI‡	COMMENT	
0	L	X	Update-IR → Run-Test/Idle	
1	н	x	Run-Test/Idle → Select-DR-Scan	
2	L	x	Select-DR-Scan → Capture-DR	
3	L	x	Capture-DR → Shift-DR	
4	н	X	Shift-DR → Exit1-DR	
5	L	x	Exit1-DR → Pause-DR, start DMA during next Shift-DR	
6	н	×	Pause-DR → Exit2-DR	
7	L	X	Exit2-DR → Shift-DR	
8-774	L	н	Load register files using Shift-DR state, loop for 767 TCK cycles	
775	н	Н	Shift-DR → Exit1-DR, perform last shift	
776	н	X	Exit1-DR → Update-DR	
777	L	x	Update-DR → Run-Test/Idle	

[‡] Value must be present at the rising edge of TCK.

The DMA instruction for loading the RAM, DMARIN, executes similarly to that in Table 12. In this example, the other method of initiating DMA, comparing the TDI-TDO data flow against the contents of the header register, is illustrated. Prior to executing DMARIN, the user has executed SCANHDR and loaded the HR with F9h, which is used as the trigger pattern for the DMA RAM write.

x = don't care.

TARI	E 12	DMADIN	EXECUTION	ı

PH			TABLE 1	2. DMARIN EXECUTION
Õ	TCK CYCLE	TMS†	TDI†	COMMENT
Ŏ	0	L	Х	Update-IR → Run-Test/Idle
Č	1	н	×	Run-Test/Idle → Select-DR-Scan
Ö	2	L	x	Select-DR-Scan → Capture-DR
ĭ	3	L	x	Capture-DR → Shift-DR
	4	L	н	Shift-DR, begin looking for header pattern (F9h)
ַע	5	L	н	
PRE	6	L	н	
Щ	7	L	L	
VIEW	8	L	L	
m	9	L	н	
<	10	L	н	
<	11	L '	н	
	12	L	н	
	13	L	н	Prior eight bits now match the value of the HR, begin DMA next cycle
	14-1036	L	L	Load RAM using Shift-DR state, loop for 1023 TCK cycles
	1037	н	L	Shift-DR → Exit1-DR, perform last shift
	1038	н	×	Exit1-DR → Update-DR
	1039	L	×	Update-DR → Run-Test/Idle

†Value must be present at the rising edge of TCK.

The fastest way (fewest clock cycles required) to load the RAM is to use INITRAM or TOGRAM. These instructions are applicable when the same data pattern is to be loaded in each RAM location or when the data in each location is to be the inverse of the data in an adjacent location. To begin the procedure, the user should load the IR with WRITERAM and scan the RAMR with the data to be written and the starting address. After this is complete, scan the IR with INITRAM or TOGRAM and loop in the Run-Test/Idle state as shown in Table 13 for 1023 TCK cycles (if the entire RAM is to be loaded). The final RAM location is written to as the TAP state changes from Run-Test/Idle to Select-DR-Scan.

Assume that the RAMR has been loaded with the value 3AAA800h. Bits 9 through 0 (the ten address bits) are 000h, and bits 25 through 10 (the sixteen data bits) are AAAAh, If INITRAM is executed according to the table, each RAM location will contain the value AAAAh. If TOGRAM is executed instead of INITRAM, the RAM will contain alternating patterns of AAAAh and 5555h, beginning with AAAAh in location 000h and ending with 5555h in location 3FFh.

TABLE 13. INITRAM, TOGRAM EXECUTION

TCK CYCLE	TMS‡	COMMENT		
0	L	Update-IR → Run-Test/Idle		
1-1023	L	Loop in Run-Test/Idle, load RAM		
1024	н	Run-Test/Idle → Select-DR-Scan, start next operation		

* Value must be present at the rising edge of TCK.

PCI description

The programmable clock interface (PCI) circuit generates the on-line clock used for test operations run under the RUNN instruction. By driving the CLK1, CLK2, and/or CLK3 inputs with system clock, status, interrupt, ready, or any of a number of other signals, the user can synchronize on-line test operations to different system conditions. The device issues its on-line clock according to one of several logic equations (see Table 14). The PCI increases the flexibility of the device by allowing on-line test operations to be triggered by multiple real-time system signals.

TABLE 14. PCI LOGIC EQUATIONS

POLSEL	SELD	SELC	SELB	SELA	RUNN
(CTLR BIT 36)	(CTLR BIT 35)	(CTLR BIT 34)	(CTLR BIT 33)	(CTLR BIT 32)	ON-LINE CLOCK (OCLK)
0	0	0	0	0	TCK†
0	0	0	0	1	CLK1†
0	0	0	1	0	CLK2†
0	0	0	1	1	CLK3†
0	0	1	0	0	CLK1⊕CLK2
0	0	1	0	1	CLK1●CLK2
0	0	1	1	0	CLK1●CLK2
0	0	1	1	1	CLK1 CLK2
o	1	0	0	0	CLK1+CLK2+CLK3
0	1	0	0	1	CLK1●CLK2●CLK3
0	1	0	1	0	CLK1 ●CLK2 ●CLK3
0	1	0	1	1	CLK1•CLK2•CLK3
0	1	1	0	0	CLK1•CLK2•CLK3
0	1	1	0	1	CLK1●CLK2●CLK3
0	1	1	1	0	CLK1 CLK2 CLK3
0	1	1	1	1	CLK1●CLK2●CLK3
1	0	0	0	0	TCK
1	0	0	0	1	CLK1
1	0	0	1	0	CLK2
1	0	0	1	1	CLK3
1	0	1	0	0	CLK1+CLK2
1	0	1	0	1	CLK1+CLK2
1	0	1	1	0	CLK1+CLK2
1	0	1	1	1	CLK1+CLK2
1	1	0	0	0	CLK1+CLK2+CLK3
1	1 1	0	0	1	CLK1+CLK2+CLK3
1	1	0	1	0	CLK1+CLK2+CLK3
1	1	0	1	1	CLK1 + CLK2 + CLK3
1	1	1	0	0	CLK1 + CLK2 + CLK3
1	1	1	0	1	CLK1+CLK2+CLK3
1	1	1	1	0	CLK1 + CLK2 + CLK3
1	1	1	1	1	CLK1 + CLK2 + CLK3

[†] Available for both RUNN and RUNT.

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TABLE 15. RUNN. RUNT OPCODES

OP3 (CTLR BIT 44)	OP2 (CTLR BIT 43)	OP1 (CTLR BIT 42)	OP0 (CTLR BIT 41)	OPCODE/FUNCTION
0	0	0	0	Sample
0	0	0	1	Sample
0	0	1	0	Sample
0	0	1	1	Sample
0	1	0	0	PSA, no cascade
0	1	0	1	PSA, MSD cascade
0	1	1	0	PSA, MID cascade
0	1	1	1	PSA, LSD cascade
1	0	0	0	Trace
1	0	0	1	Trace
1	0	1	0	Trace
1	0	1	1	Trace
1	1	0	0	Trace and PSA, no cascade
1	1	0	1	Trace and PSA, MSD cascade
1	1	1	0	Trace and PSA, MID cascade
1	1	1	1	Trace and PSA, LSD cascade

RUNN, RUNT opcode description

The primary functions of the 'ACT8994 are those opcodes run under the RUNN and RUNT instructions. The test operation performed is determined by OP3-OP0 (CTLR bits 44 through 41) as shown in Table 15. During the event protocols (see **event protocol description**), the opcodes below are executed in the DO TEST state:

SAMPLE

The data at the D inputs is captured in the TCR, taking a snapshot of the current data.

PSA

A parallel signature analysis is performed on the data appearing at the D inputs. The TCR is configured as a linear-feedback shift register (LFSR) according to the conditions previously loaded in PTAP15-PTAP00. See parallel signature analysis operations for details of PSA tests.

Four opcodes initiate the PSA operation, and there are four different options for cascading more than one DBM (see **cascaded PSA operations**):

No cascade: The PIO pin is placed in the high-impedance state, and the device's TDI and TDO pins perform their normal function.

MSD cascade: The device is configured as the most significant device in a multiple-DBM PSA chain. The TDI input is ignored and the LFSR data is shifted out via TDO to a middle significant DBM. PIO is configured as an input.

MID cascade: The device is configured as a middle significant device (neither most nor least significant) in a multiple-DBM PSA chain. TDI accepts serial LFSR input, and the LFSR data is shifted out via TDO. PIO is configured as an input.

LSD cascade: The device is configured as the least significant device in a multiple-DBM PSA chain. TDI is the serial input in the LFSR chain, and TDO is placed in the high-impedance state. PIO is configured as an output.

RUNN, **RUNT** opcode description (continued)

TRACE

The data appearing at the D inputs is stored in the RAM. The RAM address is cleared to 000h prior to execution (unless RACDIS = 1) and is incremented after each write cycle. The device can be configured to allow write cycles to continue after the maximum address is reached (thus overwriting data) or to discontinue write cycles after RAM address 03FFh has been written to.

TRACE/PSA

The TRACE and PSA operations are executed simultaneously. The same PSA cascading options available under PSA are available under TRACE/PSA.

event qualification module description

The EQM controls test operations in the on-line mode. It contains an event controller to issue enable and control signals, a programmable clock interface circuit to issue the on-line clock, and register files to store the loop counter, event counter, expected (compare) data, and mask data.

When RUNN is the current instruction, on-line test operations are active according to one of eight protocols. The protocols are state machines synchronous to the on-line clock (in the descriptions and diagrams of EQM operations and protocols, the on-line clock is referred to as OCLK). There are eight protocols that may be executed, all of which use three status signals to determine the next state. Those signals are EVENT, ECMIN, and LCMIN.

EVENT is an active-high signal and indicates that a protocol is to be triggered. Table 16 lists the signals that may be chosen to assert EVENT.

EVENT = 1 if the selected condition(s) exists.

EVENT = 0 otherwise.

ECMIN, the event counter minimum indicator, is an active-low signal and becomes active (goes low) when the event counter (EQR2 bits 55 through 40) has decremented to one, indicating that the event has occurred the specified number of times. Note that the event counter does not necessarily decrement on each match found. There must be one non-event between events for the EQM to recognize the events as separate and decrement the event counter (this is illustrated in Figure 13). In the example of the figure, the event counter is set to 2h and the expected data pattern (EQR2 bits 15 through 0) is 0001h.

 $\overline{\text{ECMIN}} = 0$ if the event counter = 1.

 $\overline{\text{ECMIN}} = 1$ otherwise.

LCMIN, the loop counter minimum indicator, is an active-low signal and becomes active (goes low) when the loop counter (EQR1 bits 15 through 0) has decremented to one, indicating that the event protocol has executed the specified number of times.

 $\overline{\text{LCMIN}} = 0$ if the loop counter = 1.

 $\overline{\text{LCMIN}} = 1$ otherwise.



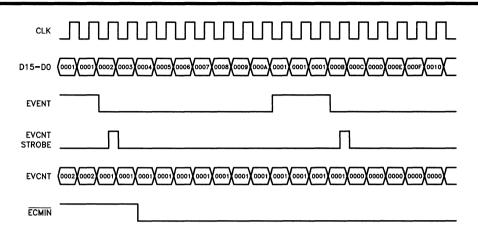


FIGURE 13. EVENT COUNTER

TABLE 16. EVENT SELECT

EQISELC (EQR1 BIT 22)	EQISELB (EQR1 BIT 21)	EQISELA (EQR1 BIT 20)	EVENT†
0	0	0	CTERM
0	0	1	DCTERM
0	1	0	EQI
0	1	1	EQI
1	0	0	DEQI
1	0	1	DEQI
1	1	0	L
1	1	1	L

[†] EVENT is the active-high signal used for triggering EQM protocols.

EVENT signal descriptions

CTERM

This asynchronous signal becomes active when the EQM compare cells detect a match between the D input data and the expected data from the EQM register files. CTERM is enabled by ENACMP in the EQR1 to become active either on the first match after the RUNN instruction is executed or on the first match after an event protocol has started.

DCTERM

DCTERM is a synchronized version of CTERM. DCTERM becomes active on the first rising edge of OCLK after CTERM becomes valid.

EQI

EQI is the level present at the EQI input pin.

EQI

EQI is the inverse of the level present at the EQI input pin.

DEQI

The synchronized version of EQI is DEQI, which becomes valid on the rising edge of OCLK.

DEQI

DEQI is the inverse of DEQI.

The on-line test operations implemented using the RUNN instruction are executed according to one of eight protocols. CMD2-CMD0 are decoded as shown in Table 17 to select the protocol.

TABLE 17, EQM PROTOCOL DECODE

70	, JULY 1990—Ti028				·					
¥		CMD2 (EQR1 BIT 32)	CMD1 (EQR1 BIT 31)	CMD0 (EQR1 BIT 30)	SELECTED EQM PROTOCOL					
ס		0	0	0	Protocol 1					
$\boldsymbol{\varpi}$		0	0	1	Protocol 2					
Ш		0	1	0	Protocol 3					
<		0	1	1	Protocol 4					
兩		1	0	ed as shown in Table 17 to select the protocol. EQM PROTOCOL DECODE CMD0 (EQR1 BIT 30) SELECTED EQM PROTOCOL 0 Protocol 1 1 Protocol 2 0 Protocol 3						
		1	0							
~	The on-line test operations implemented using the RUNN instruction are executed eight protocols. CMD2-CMD0 are decoded as shown in Table 17 to select the protocols. CMD2-CMD0 are decoded as shown in Table 17 to select the protocol and the proto	Protocol 7								
		1	1	1	Protocol 8					

The state machines for the eight on-line protocols are shown in Figures 14 through 21. Decisions are made by the protocol state machine based on the values of the internal signals EVENT, ECMIN, and LCMIN as shown in the figures. The term DO TEST in the figures refers to the RUNN opcode selected by OP3-OP0. Although any of the opcodes may be executed with any of the protocols, certain tests are more compatible with some protocols than with others.

The EQM operates synchronously to the on-line clock, OCLK, which is issued by the PCI as described earlier (see PCI description).

The EQM register files hold the expected and compare mask data used for triggering test operations as well as the event and loop counters. The addresses of the register files and the RAM are reset to all zeroes prior to the execution of any protocol.

There are two counters associated with the protocols. Each counter performs one of two functions during the protocol execution. The event counter keeps track of the number of times EVENT (which is based on some signal(s) as selected by the current protocol) becomes active, and decrements accordingly, or it delays the start of test execution for a certain number of OCLK cycles. The loop counter keeps track of the number of times the protocol has been executed or specifies the number of clocks for which a test is to be executed. The protocol terminates when the loop counter has decremented.

Protocols can be initiated by the signal present on EQI. This is useful when a test operation is to be triggered by a signal from the outside world. The signal input to EQI is configurable as shown previously in Table 16 to provide additional flexibility.

In Figures 14 through 21, four signals are indicated in the state diagrams, and they represent actions that occur at certain points in the execution of the protocols. The four signals are:

DEC: decrement the event counter.

DLC: decrement the loop counter.

LEV: load the event counter with a new value from the register file.

LND: load new expected and compare mask data from the register file.

As new data is loaded into either the event counter or expected and compare mask data, the register file address increments automatically. Data is not erased as it is loaded, and the 16-word deep register files can be re-used (i.e., increment from file address Fh to 0h and beyond) in the same test operation.



event qualification protocols (continued)

In the protocols and descriptions, the term "event" refers to the signal, as determined according to Table 16, selected to activate the state diagram signal EVENT.

In the protocol descriptions that follow, LCNT and ECNT represent the values of the loop counter and event counter, respectively.

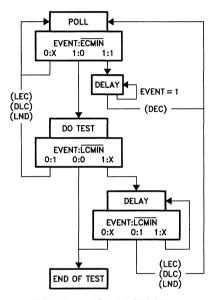


FIGURE 14. EQM PROTOCOL 1

Protocol 1 (see Figure 14) executes a test after an event has been observed a specified number of times and repeats the test for the number of times specified by the loop counter. The test executes once (after the event counter has decremented) for each loop count. Protocol 1 can be summarized as:

For LCNT times do
Begin
After ECNT events, DO TEST
End
END OF TEST

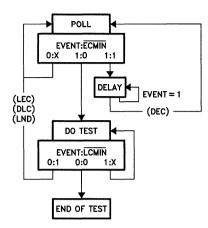


FIGURE 15. EQM PROTOCOL 2

Protocol 2 (see Figure 15) is similar to protocol 1, the difference being that the specified test executes while the event is valid, rather than only once after the event is observed. This protocol provides a dowhile test and is useful when EQI is used to trigger EVENT. The protocol can be summarized as:

For LCNT times do
Begin
After ECNT events, DO TEST while EVENT = 1
End
END OF TEST

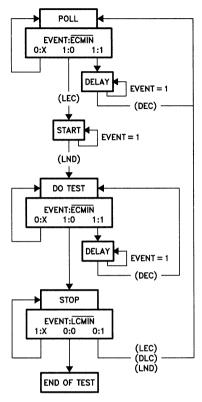


FIGURE 16. EQM PROTOCOL 3

Protocol 3 (see Figure 16) recognizes separate start and stop events. The test begins execution after a certain event occurs and stops after another (possibly different) event occurs. If the start and stop events are patterns (i.e., one of the compare terms is used as the event trigger), they are contained in consecutive register file locations. Protocol 3 can be summarized as:

```
For LCNT times do
Begin
After ECNT events, start DO TEST
After ECNT events, stop DO TEST
End
END OF TEST
```

Note that, although ECNT appears twice in the protocol summary, the user can specify different values for the start and stop events, as the event counter is reloaded after the test begins.

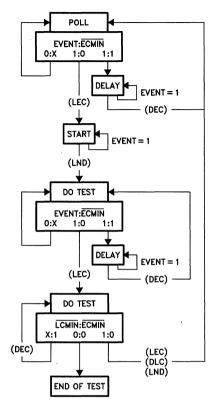


FIGURE 17. EQM PROTOCOL 4

Protocol 4 (see Figure 17) is similar to Protocol 3, the difference being that after the stop event has occurred, the test continues for some number of OCLKs. Protocol 4 can be summarized as:

```
For LCNT times do
Begin
After ECNT events, start DO TEST
After ECNT events, stop DO TEST after ECNT OCLKs
End
END OF TEST
```

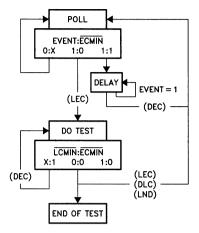


FIGURE 18. EQM PROTOCOL 5

Protocol 5 (see Figure 18) specifies that the test be executed for some number of OCLKs after an event has occurred and can be summarized as:

For LCNT times do
Begin
After ECNT events, DO TEST for ECNT OCLKs
End
END OF TEST

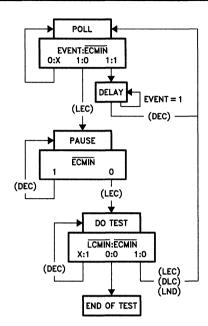


FIGURE 19. EQM PROTOCOL 6

Protocol 6 (see Figure 19) includes a pause for ECNT OCLKs after the triggering event has been observed.

For LCNT times do
Begin
After ECNT events, pause for ECNT OCLKs
DO TEST for ECNT OCLKs
End
END OF TEST

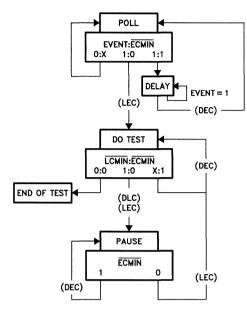


FIGURE 20. EQM PROTOCOL 7

During protocol 7 (see Figure 20), a test is executed after an event occurs without an intermediate pause; following that, the pause/test algorithm is implemented. The protocol summary is:

After ECNT events, DO TEST for ECNT OCLKs For (LCNT-1) times do Begin
Pause for ECNT OCLKs

DO TEST for ECNT OCLKs

End

END OF TEST

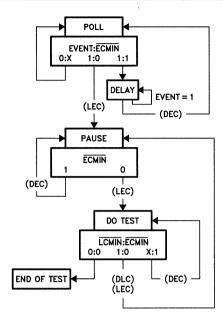


FIGURE 21. EQM PROTOCOL 8

Protocol 8 (see Figure 21) starts a pause/test algorithm after a number of events are observed and can be summarized as:

```
After ECNT events, For LCNT times do Begin
Pause for ECNT OCLKs
DO TEST for ECNT OCLKs
End
END OF TEST
```

EQO output during RUNN

Any of several internal status signals can be selected to be output via EQO during online testing as shown in Table 18.

TABLE 18, EQO SELECT[†]

EQOSELD (EQR1 BIT 26)	EQOSELC (EQR1 BIT 25)	EQOSELB (EQR1 BIT 24)	EQOSELA (EQR1 BIT 23)	EQO OUTPUT SIGNAL
0	0	0	0	Н
0	0	0	1	L
0	0	1	0	EOT
0	0	1	1	EOT
0	1	0	0	RUN
0	1	0	1	RUN
0	1	1	0	TGATE
0	1	1	1	TGATE
1	0	0	0	CTERM
1	0	0	1	CTERM
1	0	1	0	DCTERM
0	0	1	1	DCTERM
1	1	0	0	Н
1	1	0	1	L.
1	1	1	0	Н
1	1	1	1	L

[†] This table is valid unless PARENA = 1 (CTLR Bit 38) and the TAP is in the Pause-DR state. See control register bit description for details.

CTERM

This asynchronous signal becomes active when the EQM compare cells detect a match between the D input data and the expected data from the EQM register files. CTERM is enabled by ENACMP in the EQR1 to become active either on the first match after the RUNN instruction is executed or on the first match after an event protocol has started. CTERM is the inverse of CTERM. This is the same signal discussed earlier as one of the signals that may be selected to assert EVENT.

DCTERM

DCTERM is a synchronized version of CTERM. DCTERM becomes active on the first rising edge of OCLK after CTERM becomes valid. DCTERM is the inverse of DCTERM. This is the same signal discussed earlier as one of the signals that may be selected to assert EVENT.

RUN

The RUN status signal indicates that an event protocol is active, but not necessarily that a test operation is being performed (i.e., the protocol state machine may or may not be in DO TEST). RUN becomes active as soon as an event protocol begins execution and goes inactive after the protocol has terminated. RUN is the inverse of RUN.

TGATE

TGATE is active (high) when a test operation under an event qualification protocol is executing (i.e., the protocol state machine is in DO TEST). TGATE is the inverse of TGATE.

EQO output during RUNN (continued)

EOT

The EOT signal goes high when an event protocol enters the end-of-test state, meaning that the event protocol has terminated. EOT is the inverse of EOT.

Figure 22 illustrates the relationship of the internal status signals to the test operation.

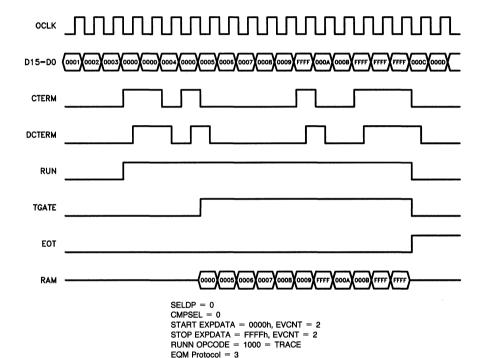


FIGURE 22. EQM STATUS SIGNALS

operation under RUNT

Under RUNT, which is active only in the Run-Test/Idle state, the current data at the D inputs (i.e., the value of D15-D0 at the rising edge of the selected clock) is input into the TCR and/or RAM. Figure 23

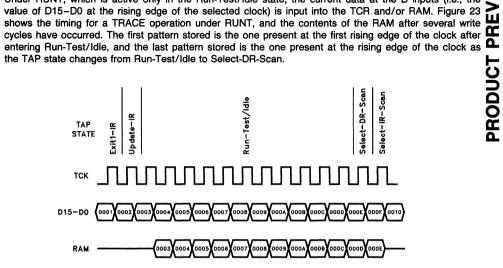


FIGURE 23. RUNT TIMING DIAGRAM

alignment of compare and data signals under RUNN

Under RUNN, several options are available for the compare function and storage of data as controlled by SELDP and CMPSEL (CTLR bits 40 and 37, respectively). The data input in both the RAM (and/or TCR) and the EQM compare circuitry can be delayed one clock cycle to implement the desired test methodology. The four options are illustrated in Figures 24 through 27, which illustrate the alignment of compare and data signals for a portion of a TRACE operation under RUNN. In the figures, the compare pattern to start the operation is 0003h and the compare pattern to stop the operation is 000Fh. The data alignment is the same for any test that runs under RUNN.

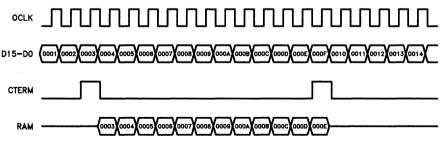
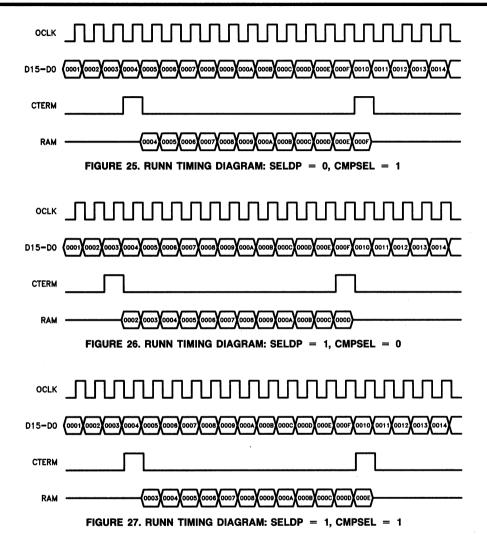


FIGURE 24. RUNN TIMING DIAGRAM: SELDP = 0. CMPSEL = 0



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parallel signature analysis operations

The TCR can be configured by OP3-OP0 to perform PSA operations on the D inputs. Additionally, multiple DBMs can be cascaded to perform PSA on more than 16 bits with the PIO pin configured for feedback.

PSA operations use an LFSR technique to perform exclusive-OR functions on pairs of data and use the result as the input to an adjacent D-type flip-flop. Parallel signature analysis can be performed under RUNN and RUNT and as a self-test operation on the RAM.

The flexibility of the device in performing PSA operations is greatly enhanced by the DATMSK bits and PTAP bits of the control register. The user can configure the device such that any combination of the D inputs can be ignored during PSA and select the feedback (FBAK) bit from the operation as an input to one of the exclusive-OR gates in each shift register stage.

The basic configuration for parallel signature analysis is shown in Figure 28. On each clock cycle the results of exclusive-OR functions are shifted to another cell as one of the inputs for the next exclusive-OR. A unique signature is developed and can be scanned out for comparison against an expected or known value.

The output of the shift register stages is determined by the various input signals as shown in Table 19.

PSA operations do not affect storage in the RAM when a simultaneous PSA/TRACE operation is being performed.

INPUTS OUTPUT PTAPnn FBAK DATMSKnn $Q_n = 1^{\dagger}$ Qnt ō o n O X ٥ Х 0 0 1 1 0 Х 0 1 0 1 n х 0 1 1 n 0 х 1 X 0 0 0 х 1 х 1 0 0 0 n n n n n n 1 n 0 0 1 х 0 0 х Λ Λ 0 0 0 0 1 1 х n 1 1 Х

TABLE 19. PSA TRUTH TABLE

 $^{^{\}dagger}$ Q_n = the value of register n after the rising edge of CLK. Q_{n-1} = the value of register (n-1) prior to the rising edge of CLK. See Figure 28.

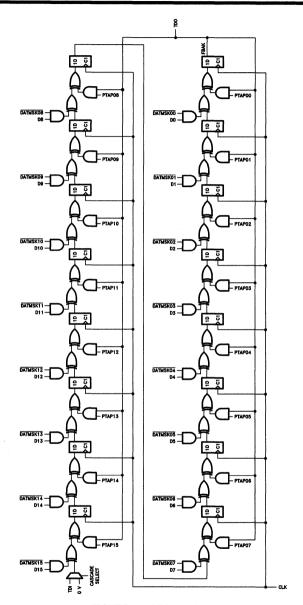


FIGURE 28. PSA CIRCUIT

cascaded PSA operations

More than one 'ACT8994 can be cascaded to perform PSA operations on buses wider than 16 bits. The RUNN and RUNT opcodes include options for configuring the device for stand-alone signatures or as the most significant device (MSD), mid significant device (MID), or least significant device (LSD) in a cascaded configuration.

Figure 29 shows a configuration in which three devices are cascaded. When the PSA opcode includes configuration as an MSD or MID, the PSA circuit is configured such that PIO is an input and replaces, in the circuit of Figure 28, the Q output of register 0 (Q_0) as the FBAK bit. Q_0 is routed through TDO to drive the TDI input of the next device in the chain. A device configured as a MSD ignores its TDI input.

When the PSA opcode configures a device as the LSD, Q_0 is used to drive PIO, now enabled and used as an output, which is tied to the PIO inputs of the MSD and MID(s). The TDO pin of an LSD is in the high-impedance state.

During a cascaded PSA operation, the TDI and TDO pins of the device are used in the shifting of data. Although an instruction register scan can occur while RUNN is active, and updating the IR with another RUNN instruction will not affect device operations, the scanning of data through the IR will contaminate the signature being generated. When a cascaded PSA operation is active, it is recommended that the device go to the Run-Test/Idle state for the duration of the test.

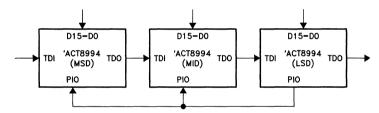


FIGURE 29. CASCADED PSA CONFIGURATION

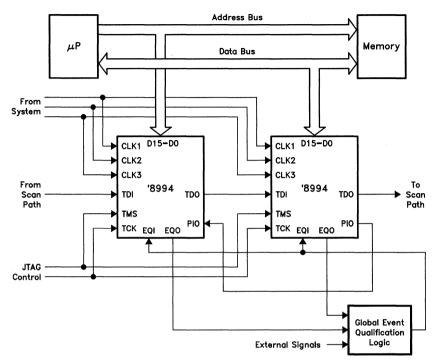


FIGURE 30. TYPICAL DBM APPLICATION

Figure 30 shows a typical application of the 'ACT8994. In the figure, two DBMs reside in parallel with a microprocessor and memory. The CLK inputs, used for on-line operations under RUNN, are driven by system signals (interrupt, clock, enable, control, etc.). The DBMs are configured for cascaded PSA operations by connecting their PIO pins.

Global event qualification schemes are implemented by combining, in the global event qualification logic block, the EQO outputs of the DBMs with some external qualifiers chosen by the user.

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PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage range, VCC0.5	V to 7 V
Input voltage range, V _I (see Note 1)	+ 0.5 V
Output voltage range, VO (see Note 1)	+ 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA 💺
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$)	±50 mA 🖺
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through V _{CC} or GND ±	:200 mA 🕻
Storage temperature range65°C to 100°C t	to 150°C 🖹

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			'54ACT8994		94 '74ACT8994			
			MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	٧	
VIH	High-level input voltage		2		2		٧	
VIL	Low-level input voltage			0.8		0.8	٧	
VI	Input voltage		0	Vcc	0	VCC	٧	
Vo	Output voltage		0	Vcc	0	VCC	٧	
	High-level output current	EQO		-3.4		-4	mA	
ЮН		PIO		-12		-16		
		TDO		-20		-24		
		EQO		3.4		4		
IOL	Low-level output current	PIO		12		16	mA	
02	TDO			20		24		
TA	Operating free-air temperature	•	-55	125	0	70	ç	

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TED	TEGT COMPLITIONS	'54AC'	T8994	'74AC	Г8994	LIMIT
IEH	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNIT
E00	$V_{CC} = 4.5 \text{ V, I}_{OH} = -3.4 \text{ mA}$	3.7				
EQU	$V_{CC} = 4.5 \text{ V, I}_{OH} = -4 \text{ mA}$			3.7		
DIO	$V_{CC} = 4.5 \text{ V, } I_{OH} = -12 \text{ mA}$	3.7				v
FIO	$V_{CC} = 4.5 \text{ V}, I_{OH} = -16 \text{ mA}$			3.7		٧
TDO	$V_{CC} = 4.5 \text{ V}, I_{OH} = -20 \text{ mA}$	3.7				
100	$V_{CC} = 4.5 \text{ V}, I_{OH} = -24 \text{ mA}$			3.7		
E00	$V_{CC} = 4.5 \text{ V}, I_{OL} = 3.4 \text{ mA}$		0.5			
	$V_{CC} = 4.5 \text{ V, } I_{OL} = 4 \text{ mA}$				0.5	
	$V_{CC} = 4.5 \text{ V, } I_{OL} = 12 \text{ mA}$		0.5			٧
FIO	$V_{CC} = 4.5 \text{ V}, I_{OL} = 16 \text{ mA}$				0.5	٧
TDO	$V_{CC} = 4.5 \text{ V, } I_{OL} = 20 \text{ mA}$		0.5	5		
100	$V_{CC} = 4.5 \text{ V, I}_{OL} = 24 \text{ mA}$				0.5	
PIO, TDO	$V_{CC} = 5.5 \text{ V}, V_O = V_{CC} \text{ or GND}$		±10		±5	μΑ
	$V_{CC} = 5.5 \text{ V}, V_{I} = V_{CC} \text{ or GND}$		±1		±1	μΑ
	$V_{CC} = 5.5 \text{ V}, V_I = V_{CC} \text{ or GND, } I_O = 0$		200		200	μΑ
	$V_{CC} = 5.5 \text{ V}, V_I = V_{CC} \text{ or GND, } I_O = 0$		175		175	mA
		EQO	TER TEST CONDITIONS MIN STATE	EQO	TEST CONDITIONS	TEST CONDITIONS MIN MAX MIN MAX MAX MIN MAX M

[†] For I/O pins, the parameter IOZ includes the input leakage current.

timing requirements over recommended operating free-air temperature range

			'54AC	T8994	'74AC'	T8994	115117	
			MIN	MIN MAX MIN MAX		MAX	UNIT	
		TCK	0	35	0	35	N 41.1-	
fclock		Any CLK	0	35	0	35	MHz	
	Dulas duration	TCK high or low	10		10			
tw	Pulse duration	Any CLK high or low	10		10		ns	
		TMS before TCK ↑	10		10			
		Any D before TCK ↑	10		10			
		Any D before any CLK	10		10			
tsu	Setup time	TDI before TCK ↑	10		10		ns	
		PIO before TCK ↑	10		10			
		PIO before any CLK	10		10			
		EQI before any CLK	10		10			
		TMS after TCK ↑	5		5			
		Any D after TCK ↑	5		5			
		Any D after any CLK	5		5			
th	Hold time	TDI after TCK ↑	5		5		ns	
		PIO after TCK ↑	5		5			
		PIO after any CLK	5		5			
		EQI after any CLK	5		5			
td	Delay time	Power-up to TCK ↑	100		100		ns	

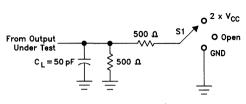
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

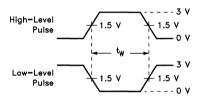
242445752	FROM	то	'54ACT	'54ACT8994		T8994	
PARAMETER	(INPUT)	(TUGTUO)	MIN	MAX	MIN	MAX	UNIT
	TCK		35		35		NAL 1-
fmax	Any CLK		35		35		MHz
tPLH .	Any D	EQO					
^t PHL	Ally D	EGO					ns
t₽LH	тск↓	TDO					ns
^t PHL	TOK \$	100					115
tPLH .	тск↓	PIO					ns
^t PHL	16K ‡	FIO					115
t _{PLH}	тск↓	EQO					ns
t _{PHL}	TOK \$	EGO					113
tPLH	EQI	EQO					ns
tPHL	LGI	LGO					115
tPLH	Any CLK	TDO					ns
t _{PHL}	Ally OER						113
tPLH	Any CLK	PIO					ns
tPHL the tensor of the tensor	Any OER	110					113
tPLH tPLH	Any CLK	EQO					ns
tPHL tPHL	7 my out	240					110
^t PZH	тск↓	TDO					ns
^t PZL	10114	150					110
^t PHZ	тск↓	TDO					ns
tPLZ	1384	150					,10
^t PZH	тск↓	PIO					ns
^t PZL	10114	110					110
^t PHZ	TCK↓	PIO					ns
tPLZ	1014	110					

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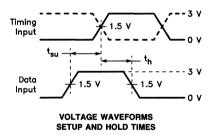
PARAMETER MEASUREMENT INFORMATION

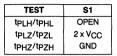


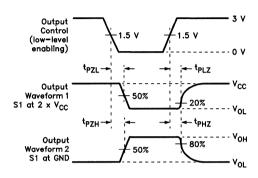
LOAD CIRCUIT FOR OUTPUTS



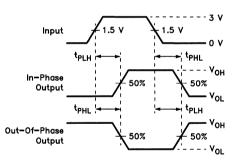
VOLTAGE WAVEFORMS PULSE DURATIONS







VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

SN54ACT8997, SN74ACT8997 SCAN PATH LINKERS WITH 4-BIT IDENTIFICATION BUSES

TI0286-D3597, APRIL 1990

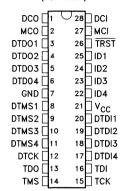
Members of the Texas Instruments SCOPE™ Family of Testability Products

- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Select Up to Four Secondary Scan Paths to Be Included in a Primary Scan Path
- Allow Partitioning of System Scan Paths
- Six Data Registers: Control, Select, Counter, Boundary Scan, ID Bus, Bypass
- Include Eight-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals
- Include Four-Bit Identification Bus for Scan Path Communication
- Inputs are TTL Compatible
- Compatible with Ti's ASSET™ (Automated Support System for Emulation and Test) Software
- Can be Cascaded Horizontally or Vertically
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

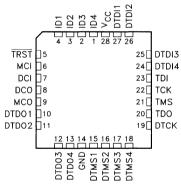
description

The 'ACT8997 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

SN54ACT8997 ... JT PACKAGE SN74ACT8997 ... DW OR NT PACKAGE (TOP VIEW)



SN54ACT8997 ... FK PACKAGE (TOP VIEW)



The 'ACT8997 enhances the scan capability of Tl's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs), which can be individually selected by the 'ACT8997 to be included in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select up to four SSPs to be included in a primary scan path. Any combination of the SSPs can be selected at a time. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

Any of the device's six data registers, or the instruction register, may be placed in the device's scan path (i.e., placed between TDI (test data in) and TDO (test data out) for subsequent shift and scan operations).

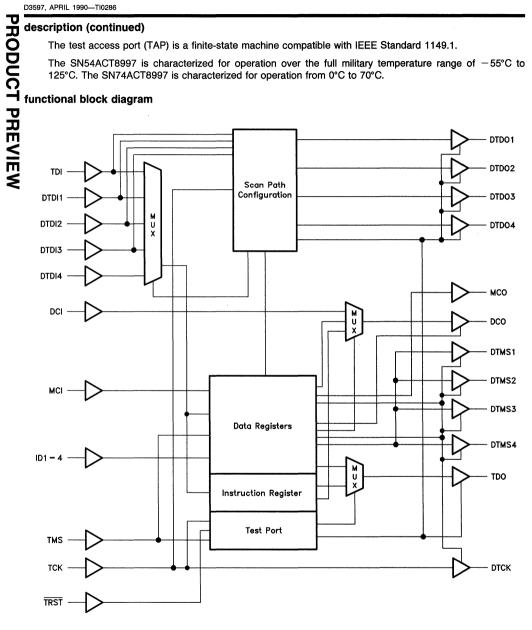
All operations of the device except counting are synchronous to the test clock pin, TCK. The eight-bit programmable up/down counter can be used to count transitions on the DCI (device condition input) pin and output interrupt signals via the DCO (device condition output) pin. The device can be configured to count on either the rising or falling edge of DCI.

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The test access port (TAP) is a finite-state machine compatible with IEEE Standard 1149.1.

The SN54ACT8997 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ACT8997 is characterized for operation from 0°C to 70°C.



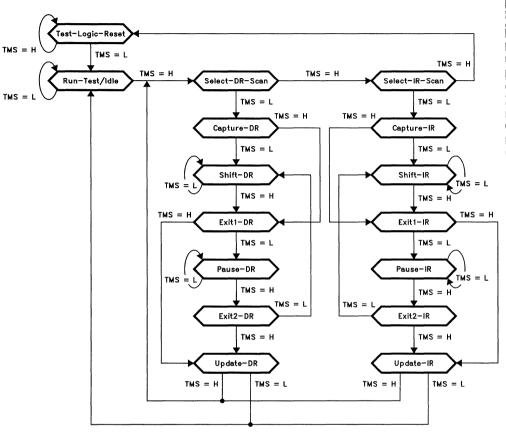


FIGURE 1. TAP STATE DIAGRAM

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state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state which does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset

In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. During device operation, the TAP returns to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; and the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK in Shift-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the logic low level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

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state diagram description (continued)

Shift-IR

In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state of from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.

signal descriptions

TDI-Test Data In

One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller. An internal pullup forces TDI to a high level if left unconnected.

TDO—Test Data Out

One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK—Test Clock

One of the four pins required by IEEE Standard 1149.1. All operations of the 'ACT8997, except for the count function, are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TMS-Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8997 through its states. An internal pullup forces TMS to a high level if left unconnected.

TRST—Test Reset

This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, TRST causes the 'ACT8997 to go to the Test-Logic-Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces TRST to a high level if left unconnected.



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signal descriptions (continued)

DTMS1-DTMS4-Device Test Mode Select 1-4

Any combination of these four pins can be selected to follow the TMS pin to direct the secondary scan path(s) through the states in Figure 1. The unselected DTMS pins can be independently set to a high or low level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI-Master Condition Input

This pin receives interrupt and protocol signals from a PBC. The level on MCI is buffered and output on MCO.

MCO-Master Condition Output

This pin transmits interrupt and protocol signals to the secondary scan path(s).

DCI—Device Condition Input

This pin receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, the DCl pin is configured as the counter clock.

DCO-Device Condition Output

DCO is configured by the control register to output protocol and interrupt signals, and may be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as:

- 1) Active-high or active-low (reset condition = active-low).
- 2) Open-drain or three-state (reset condition = open-drain).

DTDI1-DTDI4-Device Test Data In 1-4

These pins receive the serial test data outputs of the selected secondary scan path(s).

DTDO1-DTDO4-Device Test Data Out 1-4

These pins output serial test data to the TDI input(s) of the secondary scan path(s).

DTCK-Device Test Clock

This pin outputs the buffered test clock TCK to the secondary scan path(s).

ID1-ID4-Identification 1-4

This four-bit data bus can be hardwired to provide indentification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers.

functional block description

The 'ACT8997 is intended to link secondary scan paths for inclusion in a primary scan path. Any combination of the four secondary scan paths can be linked, or the device can be bypassed entirely.

The least significant bit (LSB) of any value scanned into any register of the device is the first bit shifted in (nearest to TDO). The most significant bit (MSB) is the last bit shifted in (nearest to TDI).

The 'ACT8997 is divided into functional blocks as detailed below.

test port

The test port decodes the signals on TCK, TMS, and $\overline{\text{TRST}}$ to control the operation of the circuit. The test port includes a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.



functional block description (continued)

instruction register

The instruction register (IR) is an eight-bit wide serial shift register that issues commands to the device. Data is input to the instruction register via TDI (or one of the DTDI pins) and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

data registers

Six parallel data registers are included in the 'ACT8997: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

scan path configuration circuit

This circuit decodes bits in the select and control registers to determine which, if any, of the secondary scan paths are to be included in the primary scan path.

TABLE 1. REGISTER SUMMARY

REGISTER NAME	LENGTH (BITS)	FUNCTION				
Instruction	8	Issue command information to the device.				
Control	10	Configuration and enable control.				
Counter	8	Count events on DCI, output interrupts via DCO.				
Select	8	Select one or more secondary scan paths.				
Boundary Scan	10	Capture and force test data at device periphery.				
ID Bus	4	Provide identification code.				
Bypass	1	Remove the 'ACT8997 from the scan path.				

instruction register description

The instruction register (IR) is an eight-bit serial register that outputs control signals to the device. Table 2 lists the instructions implemented in the 'ACT8997, and the data register selected by each instruction. The MSB of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal, IRERR, is generated internally as shown in Table 3. The 'ACT8997 can be configured to output IRERR via DCO if the TAP enters the Pause-IR state.

During the Capture-IR state, the IR status word is loaded. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.



instruction register description (continued)

TABLE 2. INSTRUCTION REGISTER OPCODES

BINARY CODE BIT 7 → BIT 0 MSB → LSB	HEX VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER		
00000000	00	EXTEST	Boundary Scan	Boundary Scan		
10000001	81	BYPASS†	Bypass Scan	Bypass		
10000010	82	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan		
00000011	03	INTEST	Boundary Scan	Boundary Scan		
10000100	84	BYPASS†	Bypass Scan	Bypass		
00000101	05	BYPASS†	Bypass Scan	Bypass		
00000110	06	BYPASS†	Bypass Scan	Bypass		
10000111	10000111 87		Bypass Scan	Bypass		
10001000	88	COUNT	Count	Counter		
10001001	09	COUNT	Count	Counter		
00001010	0A	BYPASS†	Bypass Scan	Bypass		
10001011	8B	BYPASS†	Bypass Scan	Bypass		
00001100	0C	BYPASS†	Bypass Scan	Bypass		
10001101	8D	BYPASS	Bypass Scan	Bypass		
10001110	8E	SCANCN	Control Register Scan	Control		
00001111	0F	SCANCT	Control Register Scan	Control		
11111010	FA	SCANCNT	Counter Scan	Counter		
01111011	7B	READONT	Counter Read	Counter		
11111100	FC	SCANIDB	ID Bus Register Scan	ID Bus		
01111101	7D	READIDB	ID Bus Register Read	ID Bus		
01111110	7E	SCANSEL	Select Register Scan	Select		
ALL OTHER		BYPASS	Bypass Scan	Bypass		

[†] A SCOPE opcode exists but is not supported by the 'ACT8997.

instruction register description (continued)

TABLE 3. IRERR FUNCTION TABLE

NUMBER OF INSTRUCTION REGISTER BITS = 1	IRERR
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

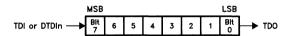


FIGURE 2. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

TABLE 4. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUET
7	IRERR (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	0
1	0
0	1

[†] This value is loaded in the instruction register during the Capture-IR TAP state.

instruction register opcode descriptions

The operation of the 'ACT8997 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the Shift-DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8997.

boundary scan

This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data appearing at input pins included in the boundary scan register is captured. Data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path, and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

The counter register begins counting on each DCI transition. The count begins from the value present in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while in the Run-Test/Idle TAP state.

counter register read

The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan

The control register is placed in the scan path for a subsequent shift operation.

ID bus register scan

The ID bus register (a subset of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data appearing on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read

The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan

The select register is placed in the scan path for a subsequent shift operation.



control register description

The control register (CTLR) is a ten-bit serial register that controls the enable and select functions of the 'ACT8997. A reset operation forces all bits to a logic low level. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 9-Up/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 8-Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 10 = 0.

Bit 7—DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active-low). When active-low, DCO does not invert the signal selected to drive it. When active-high, DCO inverts the selected signal.

Bit 6/Bit 5—DCO Source Select 1/DCO Source Select 0

DCO can be used to output the IRERR signal generated by the 'ACT8997 (see Table 3). Bits 6 and 5 can be set to output IRERR via DCO on the falling edge of TCK in the Pause-IR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 4-Parity Mask

The signal $\overline{\text{IRERR}}$ can be masked from appearing on DCO even if bits 6 and 5 are set such that it is output in the Pause-IR state (reset condition = do not mask $\overline{\text{IRERR}}$).

Bit 3—DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open-drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The three-state configuration allows the DCO output to be connected to a bus.

Bit 2—DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

Bit 1-DCI Polarity Select

The level at the DCI input can be inverted before being applied to the internal logic of the device (reset condition = do not invert DCI).

Bit 0-Device Test Pins Output Enable

DTCK, DTDO, and the DTMS1-4 pins can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control register.

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0

0

0

2

1

0

Disable DCO

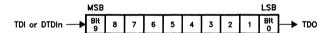
Enable DCO

DCI = DCI

PRODUCT PREVIEW

VALUE FUNCTION 0 Configure counter to count up Configure counter to count down n Do not stop counting when the count reaches 00000000 Stop counting when the count reaches 00000000 ō Configure DCO as an active-low output Configure DCO as an active-high output 1 DCO = H or L (depends on CTLR Bit 7) 00 01 DCO = IRERR 6, 5 $\overline{DCO} = \overline{CE}$, an internal logic 0 generated when the count is 00000000 10 11 DCO = DCI 0 Do not mask IRERR from DCO Mask IRERR from DCO 1 0 Configure DCO as an open-drain output 3 Configure DCO as a 3-state output

TABLE 5. CONTROL REGISTER BIT MAPPING



DCI = \overline{DCI} (invert the DCI signal before applying it to the internal logic)

Enable DTCK, DTDO1-4, and DTMS1-4

Disable DTCK, DTDO1-4, and DTMS1-4

FIGURE 3. CONTROL REGISTER BITS AND ORDER OF SCAN

SN54ACT8997, SN74ACT8997 SCAN PATH LINKERS WITH 4-BIT IDENTIFICATION BUSES

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TABLE 6. DCO FUNCTION TABLE

DCI	INTERNAL	CONTROL REGISTER BITS‡							DCO	
DCI	IRERR	CE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	DCO
Х	X	Х	X	Х	X	Х	0	0	X	Н
Х	X	Х	Х	Х	Х	Х	1	0	X	Z
X	X	X	0	0	0	X	X	1	X	Н
X	Х	X	1	0	0	Х	Х	1	X	L
X	X	X	0	0	1	1	X	1	Х	Н
X	X	Х	1	0	1	1	Х	1	Х	L
Х	0	Х	0	0	1	0	Х	1	Х	L in Pause-IR [§] , H otherwise
Х	1	Х	0	0	1	0	Х	1	Х	Н
Х	0	Х	1	0	1	0	Х	1	Х	H in Pause-IR§, L otherwise
X	1	X	1	0	1	0	X	1	Х	L
X	X	0	0	1	0	X	X	1	Х	L
Х	Х	0	1	1	0	Х	Х	1	Х	Н
Х	Х	1	0	1	0	Х	Х	1	Х	Н
X	X	1	1	1	0	Х	Х	1	Х	L
L	X	Х	0	1	1	Х	Х	1	0	L
L	X	X	0	1	1	Х	Х	1	1	H
L	X	Х	1	1	1	Х	Х	1	0	H
L	Х	Х	1	1	1	Х	Х	1	1	L
Н	Х	X	0	1	1	Х	Х	1	0	Н
Н	Х	Х	0	1	1	Х	Х	1	1	L
Н	X	Х	1	1	1	Х	Х	1	0	L
Н	X	Х	Х	1	1	1	Х	X	1	Н

[†] These signals are generated as described elsewhere in this datasheet.

[‡] The control register must contain these values after the TAP has passed through its most recent Update-DR state.

[§] DCO becomes active on the falling edge of TCK as the TAP enters the Pause-IR state and becomes inactive on the falling edge of TCK as the TAP enters Exit2-IR.

select register description

The select register (SR) is an eight-bit serial register that determines which, if any, of the seconday scan paths will be included in the primary scan path. A reset operation forces all bits to a logic 0.

The register is divided into four two-bit sections, each of which controls one SSP. Figure 4 shows the mapping of the bits to the SSPs and the order of scan. For each SSP, the higher-order bit is the MSB and the lower-order bit is the LSB (e.g., bit 3 is the MSB of SSP2 and bit 2 is the LSB of SSP2).

Although any combination of SSPs can be selected, the order of scan for each combination is fixed (see data flow description for details).

The SR bit decoding is shown in Table 7.

TABLE 7. SELECT REGISTER BIT DECODING

MSB	LSB	DTMSn SOURCE	DTDOn STATUS
0	0	Н	Z
0	1	L	Z
1	Х	TMS	Active [†]

† The DTDO1-4 outputs are active only in the Shift-IR and Shift-DR TAP states.

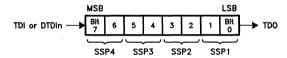


FIGURE 4. SELECT REGISTER BITS AND ORDER OF SCAN

boundary scan register/ID bus register description

The boundary scan register (BSR) is a ten-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 8 lists the device signal for each of the ten BSCs that comprise the BSR.

The four BSCs connected to the ID1-4 pins form a subset of the BSR called the ID bus register (IDBR) The IDBR can be scanned without accessing the remaining BSCs of the BSR.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

TABLE 8. BOUNDARY SCAN REGISTER BIT MAPPING

BIT	PIN NAME	SIGNAL DESCRIPTION
9	MCI	Master Condition In
8	MCO	Master Condition Out
7	DCI	Device Condition In
6	DCOTS†	Enable control for DCO in 3-state configuration (active-low)
5	DCOOD†	Enable control for DCO in open-drain configuration (active-low)
4	DCO	Device Condition Out
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

[†] This internal signal cannot be observed from the I/O pins of the device.

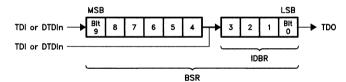


FIGURE 5. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

bypass register description

The bypass register (BR) is a one-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8997 from the primary scan path when neither it nor any of the secondary scan paths are needed for the current test operation. At power up, the BR is placed in the scan path. During Capture-DR, the BR is preloaded with a logic low level.

Figure 6 shows the order of the scan for the bypass register.

FIGURE 6. BYPASS REGISTER BITS AND ORDER OF SCAN

counter register description

The counter register (CNTR) is an eight-bit serial register that performs a binary count if configured to do so by the control register; it uses the DCI pin as its clock. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out. Many of the features of the CNTR are configured by a bit in the control register, including:

- 1) Count direction up or down (control register bit 9).
- 2) Stop counting when the value of the register is 00000000 (control register bit 8).
- 3) DCI transition on which the counter counts (control register bit 1).

An internal signal, \overline{CE} , is generated as a logic low level when the value of the CNTR is 00000000. For any other value of the CNTR, \overline{CE} is high.

The counter register can be used to count events occurring on the secondary scan path(s) and can output interrupt signals via DCO when the count has reached zero.

Figure 7 shows the order of scan for the counter register.

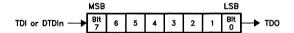
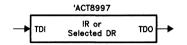


FIGURE 7. COUNTER REGISTER BITS AND ORDER OF SCAN

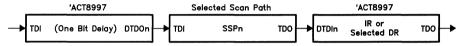
data flow description

The direction of serial data flow in the 'ACT8997 is dependent on the current instruction and value of the select register. Figure 8 shows the data flow when one or more SSPs have been selected. When more than one SSP has been selected, the order of scan is determined by which SSPs have been selected, as shown in Table 9. Note that the 'ACT8997 adds one bit of delay from TDI or DTDI to DTDO.

no secondary scan path selected



one secondary scan path selected



multiple secondary scan paths selected

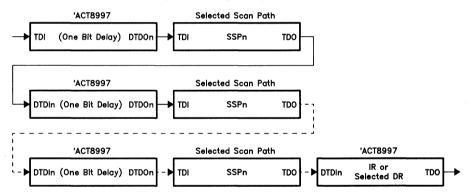


FIGURE 8. DATA FLOW IN THE 'ACT8997

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TABLE 9. SCAN PATH CONFIGURATIONS

	SR BIT SSPn CONFIGURATION		N	COAN DATH CONFIGURATION!!!				
7	5	3	1	SSP4	SSP3	SSP2	SSP1	SCAN PATH CONFIGURATION ^{†‡}
0	0	0	0	Inactive	Inactive	Inactive	Inactive	TDI-SPL-TDO
0	0	0	1	Inactive	Inactive	Inactive	Active	TDI-(1)-SSP1-SPL-TDO
0	0	1	0	Inactive	Inactive	Active	Inactive	TDI-(1)-SSP2-SPL-TDO
0	0	1	1	Inactive	Inactive	Active	Active	TDI-(1)-SSP1-(1)-SSP2-SPL-TDO
0	1	0	0	Inactive	Active	Inactive	Inactive	TDI-(1)-SSP3-SPL-TDO
0	1	0	1	Inactive	Active	Inactive	Active	TDI-(1)-SSP1-(1)-SSP3-SPL-TDO
0	1	1	0	Inactive	Active	Active	Inactive	TDI-(1)-SSP2-(1)-SSP3-SPL-TDO
0	1	1	1	Inactive	Active	Active	Active	TDI-(1)-SSP1-(1)-SSP2-(1)-SSP3-SPL-TDO
1	0	0	0	Active	Inactive	Inactive	Inactive	TDI-(1)-SSP4-SPL-TDO
1	0	0	1	Active	Inactive	Inactive	Active	TDI-(1)-SSP1-(1)-SSP4-SPL-TDO
1	0	1	0	Active	Inactive	Active	Inactive	TDI-(1)-SSP1-(1)-SSP2-(1)-SSP4-SPL-TDO
1	0	1	1	Active	Inactive	Active	Active	TDI-(1)-SSP2-(1)-SSP4-SPL-TDO
1	· 1	0	0	Active	Active	Inactive	Inactive	TDI-(1)-SSP3-(1)-SSP4-SPL-TDO
1	1	0	1	Active	Active	Inactive	Active	TDI-(1)-SSP1-(1)-SSP3-(1)-SSP4-SPL-TDO
1	1	1	0	Active	Active	Active	Inactive	TDI-(1)-SSP2-(1)-SSP3-(1)-SSP4-SPL-TDO
1	1	1	1	Active	Active	Active	Active	TDI-(1)-SSP1-(1)-SSP2-(1)-SSP3-(1)-SSP4-SPL-TDO

[†] The scan path configuration is the order of scan, beginning with the TDI pin of the 'ACT8997 and ending with the TDO pin of the 'ACT8997.

[‡] A '(1)' indicates one bit of delay through the 'ACT8997.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

olute maximum ratings over operating free-air temperature range (unles	
Supply voltage range, V _C	-0.5 V to Voc + 0.5 V
Output voltage range, V _O (see Note 1)	-0.5 V to Vcc + 0.5 V ₩
Input clamp current, I _K ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA 👺
Output clamp current, IOK ($V_I < 0$ or $V_I > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V _{CC} or GND pin	
Storage temperature range	−65°C to 150°C ⊃
esses beyond those listed under "absolute maximum ratings" may cause permanent damage to the devic I functional operation of the device at these or any other conditions beyond those indicated under "recomi implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliabi E 1: The input and output voltage ratings may be exceeded if the input and output current ratings are o	mended operating conditions" is O

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			'54AC	'54ACT8997		'74ACT8997		
			MIN	MAX	MIN MAX		UNIT	
VCC	Supply voltage		4.5	5.5	4.5	5.5	٧	
VIH	High-level input voltage		2		2		٧	
۷ _{IL}	Low-level input voltage			0.8		8.0	٧	
٧١	Input voltage		0	Vcc	0	Vcc	٧	
Vo	Output voltage		0	Vcc	0	VCC	٧	
1	I lieb level extend extend	TDO, DTDO1-4, MCO		-8.5		-10	-l m∆	
ЮН	High-level output current	DTMS1-4, DCO, DTCK		- 13.6		-16		
		TDO, DTDO1-4, MCO		8.5		10	mA	
1	Law law law day day day	DCO		13.6		16		
lOL	Low-level output current	DTMS1-4		20.4		24		
		DTCK		40.8		48		
TA	Operating free-air temperature	•	-55	125	0	70	°C	

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	DINKO	TEST COMPLETIONS		'54AC'	T8997	'74ACT8997			
PARAMETER	PIN(S)	TEST CONDITIONS	Vcc	MIN	MAX	MIN	MAX	UNIT	
	TDO, DTDO1-4, MCO	$I_{OH} = -8.5 \text{mA}$	4.5 V	3.7				V	
	100, 01001-4, MCO	$I_{OH} = -10 \text{ mA}$	4.5 V			3.7		٧	
VOH	DTMS1-4, DCO, DTCK	$I_{OH} = -13.6 \text{mA}$	4.5 V	3.7				V	
	DIMIST-4, DCO, DTCK	IOH = -16 mA	4.5 V			3.7		٧	
	TDO, DTDO1-4, MCO	IOL = 8.5 mA	4.5 V		0.5			v	
	100, D1001-4, MCO	IOL = 10 mA	4.5 V				0.5	٧	
VOL	DCO	IOL = 13.6 mA	4.5 V		0.5			v	
		IOL = 16 mA	4.5 V				0.5	V	
	DTMS1-4	IOL = 20.4 mA	4.5 V		0.5			v	
		IOL = 24 mA	4.5 V				0.5	· ·	
	DTCK	$I_{OL} = 40.8 \text{ mA}$	4.5 V		0.5			>	
	BICK	IOL = 48 mA	4.5 V				0.5	٧	
loz†	DTDO1-4, DTMS1-4, DCO, DTCK	VO = VCC or GND	5.5 V		± 10		±5	μΑ	
	MCI, DCI, TCK, ID1-4	V _I = V _{CC} or GND	5.5 V		±1		± 1		
11	TDI, DTDI1-4, TMS, TRST	V _I = V _{CC} or GND	5.5 V	-0.1	-20	-0.1	-20	μΑ	
lcc		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		100		100	μΑ	
ΔICC [‡]		One input at V_{IH} or V_{IL} , Other inputs at V_{CC} or GND	5.5 V		2		0.5	mA	

[†] For I/O pins, the parameter IOZ includes the input leakage current.

timing requirements over recommended ranges of operating free-air temperature and supply voltage

			'54AC	T8997	'74ACT8997					
			MIN	MAX	MIN MAX		UNIT			
	Clash for an annual	TCK								
fclock	Clock frequency	DCI (Count mode)					MHz			
	Dulas desertion	TCK high or low								
tw	Pulse duration	DCI high or low (Count mode)					ns			
		TMS before TCK ↑								
	Setup time	TDI before TCK ↑								
		Any DTDI before TCK ↑								
t _{su}		MCI before TCK ↑					ns			
		DCI before TCK ↑								
		Any ID before TCK ↑								
		TMS after TCK ↑								
		TDI after TCK ↑								
		Any DTDI after TCK ↑								
th	Hold time	MCI after TCK ↑					ns			
		DCI after TCK ↑								
		Any ID after TCK↑					1			
td	Delay time	Power up to TCK ↑					ns			

[‡] This is the increase in supply current for each input being driven at TTL levels rather than VCC or GND.

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage

DADAMETED	FROM	то	'54ACT8997		'74ACT8997		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MIN MAX		MAX	UNII	
	TCK			20		20		
fmax	DCI (Count mode)	DCI (Count mode)		20		20	MHz	
tPLH	TOK							
t _{PHL}	— TCK↓	TDO					ns	
tPLH .	тск↓	TOV I						
^t PHL	TOK	An DTMS					ns	
^t PLH	тск↓	Any DTDO						
^t PHL	TON \$	Ally D1DO					ns	
+-	TOV	DCO (open-drain)						
tPLH	TCK↓	DCO (three-state)					ns	
tm: ::	тск↓	DCO (open-drain)						
^t PHL	100.4	DCO (three-state)					ns	
t _{PLH}	TMS	Any DTMS					ns	
^t PHL	TMS	Ally DT M3					TR	
tPLH	MCI	мсо					nr	
^t PHL	IVICI	IVICO					ns	
t	DCI	DCO (open-drain)						
tPLH	DOI	DCO (three-state)					ns	
ł	DCI	DCO (open-drain)						
[†] PHL	DCI DCO (three-state)						ns	
tPLH	тск	DTCK						
tPHL	100	DICK					ns	

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (continued)

PARAMETER	FROM	то	'54AC	T8997	'74ACT8997		UNI
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UN
tPHZt	— тск↓	DTCK					١ ۾
^t PLZ	101.4						ns
^t PHZ	— тск↓	TDO					ns
tPLZ	TOR \$	100					
tPHZ	— тск↓	Any DTDO					n
tPLZ	1000	Ally B1 B0					
^t PHZ	— тск↓	DCO					n
tPLZ	1000						
tPHZ	— тск↓	Any DTMS					n
tPLZ	100.4	Any Divis					
tPZH	— тск↓	DTCK					n
tPZL	1000	BTOK					
tPZH	— тск↓	тро					
tPZL	100.4	100					'
tPZH	— тск↓	Any DTDO					l ,
tPZL	100.4	Any Broo					
tPZH	— тск↓	DCO					,
tPZL	161(4)	Bee					
^t PZH	— тск↓	Any DTMS					n
tPZL	101.4	Ally Di Wo					"

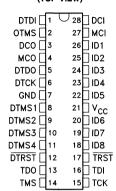
APPLICATION INFORMATION SUBSYSTEM TDO SSP4 TCK TMS TDI TDO SSP3 TCK TMS TDI TDO SSP2 TCK TMS TDI TDO SSP1 TCK TMS DTDI DTDO DTMS DTCK 1-4 DCI мсо 'ACT8997 V_{CC} or GND ----ID2 V_{CC} or GND ----ID3 V_{CC} or GND -ID4 TDI DCO TRST TMS TCK MCI TDO TDO INT1 RSTOUT PBC **TMSOUT** TO REMAINDER OF SCAN PATH TCKOUT INT2 TDI

SN54ACT8999, SN74ACT8999 SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES

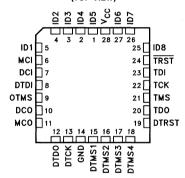
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- Members of the Texas Instruments SCOPE™
 Family of Testability Products
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Select One of Four Secondary Scan Paths to Be Included in a Primary Scan Path
- Allow Partitioning of System Scan Paths
- Provide Communication between Primary and Remote Test Bus Controllers
- Six Data Registers: Control, Select, Counter, Boundary Scan, ID Bus, Bypass
- Include Eight-Bit Programmable Binary Counter to Count or Initiate Interrupt Signals
- Include Eight-Bit Identification Bus for Local or Global Bus Communication
- Inputs are TTL Compatible
- Compatible with Tl's ASSET™ (Automated Support System for Emulation and Test) Software
- Can be Cascaded Horizontally or Vertically
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN54ACT8999 ... JT PACKAGE SN74ACT8999 ... DW OR NT PACKAGE (TOP VIEW)



SN54ACT8999 ... FK PACKAGE (TOP VIEW)



description

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The 'ACT8999 is a member of Texas Instruments SCOPE™ testability IC family. This family of components facilitates testing of complex circuit board assemblies.

The 'ACT8999 enhances the scan capability of Tl's SCOPE™ family by allowing augmentation of a system's primary scan path with secondary scan paths (SSPs). The SSPs can be individually selected by the 'ACT8999 for inclusion in the primary scan path. The device also provides buffering of test signals to reduce the need for external logic.

By loading the proper values into the instruction register and data registers, the user can select one of four secondary scan paths. This has the effect of shortening the scan path to allow maximum test throughput when an individual subsystem (board or box) is to be tested. By selecting the bypass register, all secondary scan paths can be removed from a primary scan path.

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Texas VI

SN54ACT8999, SN74ACT8999 SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES

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description (continued)

Any of the device's six data registers, or the instruction register, may be placed in the device's scan path (i.e., placed between TDI (test data in) and TDO (test data out) for subsequent shift and scan operations).

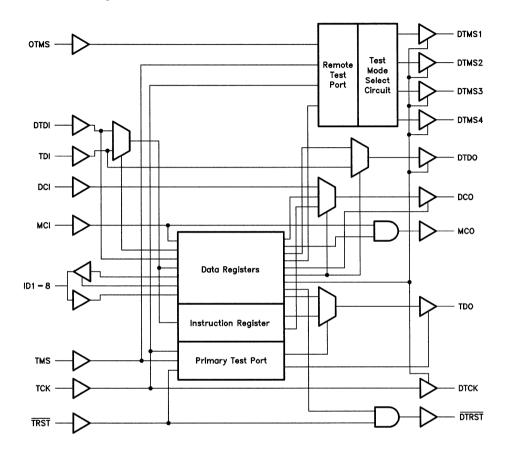
All operations of the device except counting are synchronous to TCK (test clock). The eight-bit programmable up/down counter can be used to count transitions on the DCI (device condition input) pin and output interrupt signals via the DCO (device condition output) pin. The device can be configured to count on either the rising or falling edge of DCI.

If a system's test architecture contains more than one test bus controller, the eight-bit bidirectional bus can be used to interface a higher-level primary bus controller (PBC) with one or more lower-level remote bus controllers (RBCs). A protocol allows the PBC to pass control of the 'ACT8999 to an RBC, freeing the PBC for other tasks. The eight-bit bus can also be hardwired to provide one of 256 codes for subsystem identification.

The test access port (TAP) is a finite-state machine compatible with the IEEE Standard 1149.1.

The SN54ACT8999 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ACT8999 is characterized for operation from 0°C to 70°C.

functional block diagram



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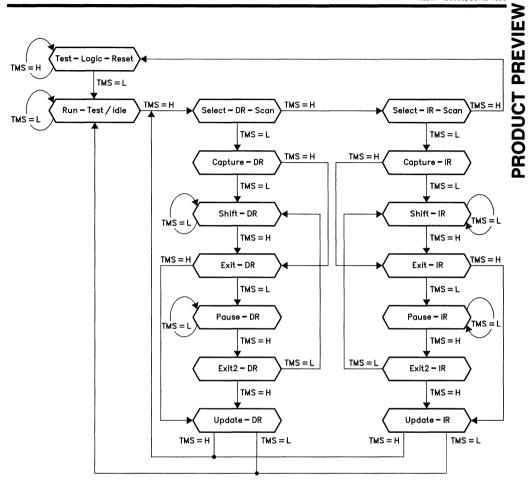


FIGURE 1. TAP STATE DIAGRAM

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state diagram description

The TAP proceeds through the states in Figure 1 according to IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to manipulate a data register and one to manipulate the instruction register. No more than one register can be manipulated at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In this state, the test logic is inactive and an internal reset signal is applied to all registers in the device. Also, during device operation, the TAP returns to this state in no more than five TCK cycles if TMS (test mode select) is high. The TMS pin has an internal pullup that forces it to a high level if left unconnected or if a board defect causes it to be open-circuited.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The TAP may retain this state indefinitely, and no registers are modified while in Run-Test/Idle.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states; the TAP exits either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path (i.e., between TDI and TDO). Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change.

Shift-DR

In this state, data is serially shifted through the selected data register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). On the falling edge of TCK, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present before it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the low level.

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated only during this state.

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state diagram description (continued)

Capture-IR

The instruction register is preloaded with the IR status word (see Table 4) and placed in the scan path.

Shift-IR

In this state, data is serially shifted through the instruction register, from TDI to TDO, on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). On the falling edge of TCK in Shift-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO takes on the high level.

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. TDO changes from the active state to the high-impedance state on the falling edge of TCK as the TAP changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

In this state, the latches shadowing the instruction register are updated with the new instruction.



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signal descriptions

TDI-Test Data In

One of the four pins required by IEEE Standard 1149.1, TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller. An internal pullup resistor forces TDI to a high level if left unconnected.

TDO-Test Data Out

One of the four pins required by IEEE Standard 1149.1, TDO is the serial output for shifting information from the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK—Test Clock

One of the four pins required by IEEE Standard 1149.1. Operation of the 'ACT8999, except for the count function, is synchronous to TCK. Data appearing at the device inputs is captured on the rising edge of TCK; outputs change on the falling edge of TCK.

TMS-Test Mode Select

One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the 'ACT8999 through its state machine. An internal pullup resistor forces TMS to a high level if left unconnected.

TRST—Test Reset

This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, TRST causes the 'ACT8999 to enter the Test-Logic-Reset state and to configure the instruction register and data registers to their power-up values. TRST is also output, without inversion, via DTRST (device test reset). An internal pullup forces TRST to a high level if left unconnected.

OTMS—Optional Test Mode Select

This pin can be used instead of TMS to control (with TCK) the select register. This is useful when a remote bus controller is available to control the secondary scan path(s). An internal pullup resistor forces OTMS to a high level if left unconnected.

DTMS1-DTMS4-Device Test Mode Select 1-4

Either none or one of these four output pins can be selected to follow the TMS pin or OTMS pin to include a secondary scan path in the primary scan path. The unselected DTMS pins can be independently set to a static high or low level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI—Master Condition Input

This pin receives interrupt and protocol signals from a PBC.

MCO-Master Condition Output

This pin transmits interrupt and protocol signals to an RBC and/or the secondary scan path(s). It also outputs an active-low error signal during the Pause-DR TAP state if an RBC loads an invalid value in the select register.

DCI—Device Condition Input

This pin receives interrupt and protocol signals from an RBC and/or the secondary scan path(s). When the counter register is instructed to count up or down, the DCl pin is configured as the counter clock.

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signal descriptions (continued)

DCO—Device Condition Output

DCO is configured by the control register to output protocol and interrupt signals to a PBC. It can also be configured by the control register to output an error signal if the instruction register or select register are loaded with invalid values. DCO is further configured by the control register as:

- 1) Active-high or active-low (reset condition = active-low).
- 2) Open-drain or three-state (reset condition = open-drain).

DTDI—Device Test Data In

This pin receives the serial test data output of the selected secondary scan path.

DTDO—Device Test Data Out

This pin outputs serial test data to the TDI input(s) of the secondary scan paths.

DTCK—Device Test Clock

This pin outputs the buffered test clock TCK to the secondary scan path(s).

DTRST—Device Test Reset

This active-low output transmits a reset signal to the secondary scan path(s). DTRST can be asserted by a bit in the control register or by setting TRST low.

ID1-ID8-Identification 1-8

This eight-bit data bus can be used to communicate with an RBC and pass data and control instructions. By wiring pullup and pulldown resistors to these pins, one of 255 unique identification codes can be assigned to the device, allowing a test controller to verify or determine the identity of the subsystem under test



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functional block description

The 'ACT8999 implements two separate functions in one package. The primary function of the device is to include a selected secondary scan path in the system's primary scan path to enable a PBC to perform controlling and observing test functions on the selected path. This is accomplished by driving the TMS pin(s) of a secondary scan path with one of the DTMS pins of the device. This approach allows a system to have built-in testability at all levels without requiring that the primary system scan path always include all subsystem scan paths. As a result, test throughput is improved and the amount of test data that must be interpreted is reduced. The device includes error detection circuitry that prevents the user from inadvertently activating more than one secondary scan path at a time.

Another function of the device is provided by the 8-bit identification bus. This bus can be hard-wired with pullup and pulldown resistors to supply an identification code to the test controller(s) to verify that test operations are being performed on the proper portion of the system. The bus can also transfer data and instructions to another device, such as a local or remote bus controller, and pass control of the scan path select function to that device. This frees the primary controller to activate another secondary scan path elsewhere in the system or perform higher-level test control functions. When the RBC is ready to return control of the device, interrupt signals alert the primary controller.

The least significant bit (LSB) of any value to be scanned into any register of the device is defined to be the first bit shifted in (nearest to TDO). The most significant bit (MSB) is defined to be the last bit shifted in (nearest to TDI).

The 'ACT8999 is divided into functional blocks as detailed below.

test ports

The test ports decode the signals on TCK, TMS, OTMS, and TRST to control the operation of the circuit. The test ports include a TAP that issues the proper control instructions to the data registers according to the IEEE Standard 1149.1 protocol. The TAP state diagram is shown in Figure 1.

Two test ports are included on the 'ACT8999, allowing different test controllers to command different sections of the device.

TMS circuit

The TMS circuit decodes bits in the select and control registers to determine which one, if any, of the DTMS pins (which provide mode select signals to the secondary scan path(s)) will follow the TMS pin or OTMS pin. The unselected DTMS pins are set by the circuit to a static high or low level.

instruction register

The instruction register (IR) is an eight-bit-wide serial shift register that issues commands to the device. Data is input into the instruction register via TDI or DTDI and shifted out via TDO. All device operations are initiated by loading the proper instruction or set of instructions into the IR.

data registers

Six parallel data registers are included in the 'ACT8999: bypass, control, counter, boundary scan, ID bus, and select. The ID bus register is a part of the boundary scan register. Each data register is serially loaded via TDI or DTDI and outputs data via TDO.

Table 1 summarizes the registers in the 'ACT8999.

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TABLE 1. REGISTER SUMMARY

REGISTER NAME	LENGTH (BITS)	FUNCTION	
Instruction	8	Issue command information to the device	
Remote Instruction	8	Issue command information to the select register	
Control	13	Configuration and enable control	
Counter	8	Count events on DCI, output interrupts via DCO	
Select	8	Select one of four DTMS pins to follow TMS or OTMS	
Boundary Scan	15	Capture and force test data at device periphery	
ID Bus	8	Pass test commands and data between a PBC and RBC(s)	
Bypass	1	Remove the 'ACT8999 from the scan path	

instruction register description

The instruction register is an eight-bit serial shift register that outputs commands to the device. Table 2 lists the instructions implemented in the 'ACT8999 and the data register selected by each instruction.

The most significant bit of the IR is an even-parity bit. If the value scanned into the IR during Shift-IR does not contain even parity, an error signal, IRERR, is generated internally as shown in Table 3. The 'ACT8999 can be configured to output IRERR via DCO if the TAP enters the Pause-IR state.

The IR status word is loaded during the Capture-IR state. The IR status word contains information about the most recently loaded values of the instruction and select registers and the logic level present at the DCI input. The IR status word is encoded as shown in Table 4.

Figure 2 illustrates the order of scan for the instruction register.

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TABLE	INCTO	LICTION	REGISTER	ODCODEC
IADLE	Z. INSTR	LIL I IL IN	REGISTER	UPLANES

BINARY CODE	HEX			CEL COTED
BIT 7 \rightarrow BIT 0	VALUE	SCOPE OPCODE	DESCRIPTION	SELECTED
$MSB \rightarrow LSB$	VALUE			DATA REGISTER
00000000	00	EXTEST	Boundary Scan	Boundary Scan
10000001	81	BYPASS†	Bypass Scan	Bypass
10000010	82	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan
0000011	03	INTEST	Boundary Scan	Boundary Scan
10000100	84	BYPASS†	Bypass Scan	Bypass
00000101	05	BYPASS†	Bypass Scan	Bypass
00000110	06	BYPASS†	Bypass Scan	Bypass
10000111	87	BYPASS†	Bypass Scan	Bypass
10001000	88	COUNT	Count	Counter
00001001	09	COUNT	Count	Counter
00001010	0A	BYPASS†	Bypass Scan	Bypass
10001011	8B	BYPASS†	Bypass Scan	Bypass
00001100	0C	BYPASS†	Bypass Scan	Bypass
10001101	8D	BYPASS	Bypass Scan	Bypass
10001110	8E	SCANCN	Control Register Scan	Control
00001111	0F	SCANCT	Control Register Scan	Control
11111010	FA	SCANCNT	Counter Scan	Counter
01111011	7B	READCNT	Counter Read	Counter
11111100	FC	SCANIDB	ID Bus Register Scan	ID Bus
01111101	7D	READIDB	ID Bus Register Read	ID Bus
01111110	7E	SCANSEL	Select Register Scan	Select
ALL OTHER		BYPASS	Bypass Scan	Bypass

[†] A SCOPE™ opcode exists but is not supported by the 'ACT8999.

TABLE 3. IRERR FUNCTION TABLE

NUMBER OF INSTRUCTION REGISTER BITS = 1	IRERR
0, 2, 4, 6, 8	1
1, 3, 5, 7	0

TABLE 4. INSTRUCTION REGISTER STATUS WORD

IR BIT	VALUE‡
7	IRERR (see Table 3)
6	0
5	0
4	0
3	Level present at DCI input (1 = H, 0 = L)
2	SRERR (see Table 8)
1	0
0	1

[‡] This value is loaded in the instruction register during the Capture-IR TAP state.



FIGURE 2. INSTRUCTION REGISTER BITS AND ORDER OF SCAN

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instruction register opcode descriptions

The operation of the 'ACT8999 is dependent on the instruction loaded into the instruction register. Each instruction selects one of the data registers to be placed between TDI or DTDI and TDO during the shift DR TAP state.

All the required instructions of IEEE Standard 1149.1 are implemented in the 'ACT8999.

boundary scan

This instruction implements the required EXTEST and INTEST operations of IEEE Standard 1149.1. The boundary scan register (which includes the ID bus register) is placed in the scan path. Data on input pins included in the boundary scan register is captured; data previously loaded into the output pins included in the boundary scan register is forced through the outputs.

bypass scan

This instruction implements the required BYPASS operation of IEEE Standard 1149.1. The bypass register is placed in the scan path and preloads with a logic 0 during Capture-DR.

sample boundary

This instruction implements the required SAMPLE/PRELOAD operation of IEEE Standard 1149.1. The boundary scan register is placed in the scan path and data appearing at the inputs and outputs included in the boundary scan register is sampled on the rising edge of TCK in Capture-DR.

count

The counter register begins counting on each DCI transition. The count begins at the value in the register before the count instruction was loaded. The counter can be programmed to count up or down on either the low-to-high or high-to-low transition of DCI. Counting occurs only while the device is in the Run-Test/Idle TAP state.

counter register read

The counter register is placed in the scan path. During Capture-DR, the prior preloaded value of the counter is loaded into the counter register. At Update-DR, a new preload value is loaded.

counter register scan

The counter register is placed in the scan path. During Capture-DR, the current value of the counter is loaded in the counter register. At Update-DR, a new preload value is loaded.

control register scan

The control register is placed in the scan path for a subsequent shift operation.

ID bus register scan

The ID bus register (part of the boundary scan register) is placed in the scan path for a subsequent shift operation. The data on the ID bus is loaded into the ID bus register on the rising edge of TCK in Capture-DR.

ID bus register read

The ID bus register is placed in the scan path for a subsequent shift operation. The register is not preloaded during Capture-DR.

select register scan

The select register is placed in the scan path for a subsequent shift operation



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control register description

The control register (CTLR) is a 13-bit serial register that controls the enable and select functions of the 'ACT8999. A reset operation forces all bits to a logic 0. The contents of the control register are latched and decoded during the Update-DR TAP state. The specific function of each bit is listed in Table 5.

The enable and select functions of the control register bits are mapped as follows:

Bit 12—Up/Down

This bit sets the count mode of the counter register (reset condition = count up).

Bit 11-Latch on Zero

The counter register can be configured to stop counting when its value is 00000000 and ignore subsequent transitions on the counter clock, DCI. The latch-on-zero option is valid only in the count-down mode (reset condition = do not latch on zero). The value of this bit has no effect on the operation of the counter if CTLR bit 12 = 0.

Bit 10-DCO Polarity Select

DCO can be configured as an active-low or active-high output (reset condition = active-low). When active-low, DCO does not invert the signal selected to drive it; when active-high, DCO inverts the selected signal.

Bit 9/Bit 8-DCO Source Select 1/DCO Source Select 0

DCO can be used to output two error signals generated by the 'ACT8999: IRERR (see Table 3) and SRERR (see Table 8). Bits 9 and 8 can be set to output IRERR via DCO on the falling edge of TCK in the Pause-IR state and SRERR via DCO on the falling edge of TCK in the Pause-DR state. DCO can also be configured to become active when the value of the counter is 00000000, to follow DCI, or be set to a static high or low level (reset condition = static high level).

Bit 7-Parity Mask

The internal error signals can be masked from appearing on DCO even if bits 9 and 8 are set such that IRERR and SRERR will be output in the Pause-IR and Pause-DR states (reset condition = do not mask IRERR or SRERR).

Bit 6-DCO Drive Select

DCO can be configured as either an open-drain or 3-state output (reset condition = open-drain). The open-drain configuration allows multiple DCO outputs to be used in a wired-OR or wired-AND application. The three-state configuration allows the DCO output to be connected to a bus.

Bit 5-DCO Enable

When configured as a 3-state output, DCO can be placed in the high-impedance state (reset condition = disabled). If configured as an open-drain output and disabled, DCO outputs a high level.

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control register description (continued)

Bit 4-DCI Polarity Select

The level at the DCI input can be inverted before being applied to the internal logic of the device (rese condition = do not invert DCI).

Bit 3—Device Test Pins Output Enable

DTCK, DTDO, and the DTMS1-4 pin can be placed in the high-impedance state (disabled) with this bit (reset condition = enabled).

Bit 2-ID Bus Enable

The ID bus (ID1-8) is a bidirectional bus. The output buffers are enabled and disabled with this bit (reset condition = output buffers disabled).

Bit 1—Remote Bus Controller Enable

An RBC can issue protocol and data instructions to the select register if the 'ACT8999 is configured to allow it (reset condition = RBC disabled). When an RBC is enabled, the TAP in the select register operates according to the OTMS signal.

Bit 0-Device Test Reset

DTRST can be configured to output a reset signal independently of the level on TRST (reset condition = no reset signal issued).

Several control register bits affect the functionality of the DCO output. The DCO function table is given in Table 6.

Figure 3 illustrates the order of scan for the control registers.



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		TABLE 5. CONTROL REGISTER BIT MAPPING
BIT	VALUE	FUNCTION
12	0	Configure counter to count up.
12	1	Configure counter to count down.
11	0	Do not stop counting when the count reaches 00000000.
'''	1	Stop counting when the count reaches 00000000.
10	0	Configure DCO as an active-low output.
10	1	Configure DCO as an active-high output.
	00	DCO = H or L (depends on CTLR Bit 10).
9.8	01	DCO = (IRERR ● SRERR).
9,0	10	DCO = $\overline{\text{CE}}$, an internal logic 0 generated when the count is 00000000.
	11	DCO = DCI.
7	0	Do not mask IRERR and SRERR from DCO.
	1	Mask IRERR and SRERR from DCO.
6	0	Configure DCO as an open-drain output.
6	1	Configure DCO as a 3-state output.
5	0	Disable DCO.
5	1	Enable DCO.
4	0	DCI = DCI.
4	1	$DCI = \overline{DCI}$ (invert the DCI signal before applying it to the internal logic).
3	0	Enable DTCK, DTDO, and DTMS1-4.
3	1	Disable DTCK, DTDO, and DTMS1-4.
2	0	Disable ID1-8.
	1	Enable ID1-8.
1	0	Disable RBC.
	1	Enable RBC.
0	0	DTRST = TRST.
U	1	DTRST = L.



FIGURE 3. CONTROL REGISTER BITS AND ORDER OF SCAN

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TADI	-	DCO	FUNCTI	\sim NI	TADIE

DCI	INTERN	IAL SIGNA	\LS†		CO	NTROL	REGIST	TER BIT	S‡		DCO
DCI	IRERR	SRERR	CE	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	DC0
Х	Х	Х	Х	Х	Х	Х	X	0	0	Х	Н
Х	Х	Х	Х	Х	Х	Х	Х	1	0	Х	Z
Х	Х	Х	Х	0	0	0	Х	X	1	Х	Н
Х	Х	Х	Х	1	0	0	Х	Х	1	Х	L
X	X	Х	Х	0	0	1	1	X	1	Х	Н
Х	X	Х	Х	1	0	1	1	Х	1	Х	L
Х	0	Х	Х	0	0	1	0	Х	1	Х	L in Pause-IR [§] , H otherwise
Х	Х	0	Х	0	0	1	0	Х	1	Х	L in Pause-DR [§] , H otherwise
Х	1	1	Х	0	0	1	0	X	1	X	Н
Х	0	Х	Х	1	0	1	0	Х	1	Х	H in Pause-IR [§] , L otherwise
Х	Х	0	Х	1	0	1	0	Х	1	Х	H in Pause-DR [§] , L otherwise
Х	1	1	Х	1	0	1	0	Х	1	Х	L
Х	Х	Х	0	0	1	0	Х	Х	1	Х	L
X	Х	Х	0	1	1	0	Х	X	1	Х	Н
X	Х	Х	1	0	1	0	X	X	1	X	Н
Х	Х	Х	1	1	1	0	X	X	1	Х	L
L	Х	Х	Х	0	1	1	X	X	1	0	L
L	Х	Х	Х	0	1	1	Х	Х	1	1	Н
L	Х	Х	Х	1	1	1	Х	Х	1	0	Н
L	Х	Х	Х	1	1	1	X	Х	1	1	L
Н	Х	Х	Х	0	1	1	X	X	1	0	Н
Н	Х	Х	Х	0	1	1	X	X	1	1	L
Н	Х	Х	Х	1	1	1	X	X	1	0	L
Н	Х	X	Х	1	1	1	Х	Х	1	1	Н

[†] These signals are generated as described elsewhere in this datasheet.

[‡] The control register must contain these values after the TAP has passed through its most recent Update-DR state.

[§] DCO is active on the falling edge of TCK as the TAP enters the appropriate pause state (Pause-IR or Pause-DR) and is inactive on the falling edge of TCK as the TAP enters the appropriate exit2 state (Exit2-IR or Exit2-DR).

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select register description

The select register (SR) is an eight-bit serial register that determines which one, if any, of the DTMS lines follows the TMS or OTMS input. A reset operation forces all bits to a logic 0. The register is divided into four two-bit sections, each of which controls one DTMS output. Figure 4 shows the mapping of the bits to the DTMS outputs and the order of scan. For each DTMS pin, the higher order bit is the MSB and the lower order bit is the LSB (e.g., bit 3 is the MSB of DTMS2 and bit 2 is the LSB of DTMS2).

Only one of the four DTMS outputs can be selected to drive a secondary scan path with TMS or OTMS. If the select register is loaded with an invalid value, an error signal, SRERR, is generated internally as shown in Table 8. If the TAP enters the Pause-DR state, SRERR may be output via DCO (see Table 8). If the TAP enters the Update-DR state while an invalid value is in the SR, all four DTMS outputs are set to a high level. The SR bit decoding is shown in Table 7.

The SR can also be accessed from an RBC. A test port in the register contains a TAP that can be enabled by the control register to monitor the values of TCK and OTMS to perform scan operations on the SR.

TABLE 7. SELECT REGISTER BIT DECODING

MSB	LSB	DTMSn SOURCE
0	0	High
0	1	Low
1	0	OTMS
1	1	TMS

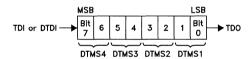


FIGURE 4. SELECT REGISTER BITS AND ORDER OF SCAN

TABLE 8. SRERR FUNCTION TABLE

			SELECT RE	GISTER BITS				SRERR
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	SHERH
0	Х	0	Х	0	Х	0	Х	1
1	Х	0	X	0	Х	0	Х	1
0	Х	1	Х	0	Χ	0	Х	1
0	Х	0	Х	1	Х	0	Х	1
0	X	0	X	0	X	1	X	1
1	Х	1	Х	X	Х	Х	X	0
1	X	Х	Х	1	Х	Х	X	0
1	X	Х	X	Х	Х	1	Х	0
Х	X	1	X	1	X	Х	Х	0
Х	Х	1	Х	Х	Х	1	Х	0
X	Х	Х	Х	1	Х	1	Х	0

boundary scan register/ID bus register description

The boundary scan register (BSR) is a 15-bit serial register that can be used to capture data appearing at selected device inputs, force data through device outputs, and apply data to the device's internal logic. The BSR is made up of boundary scan cells (BSCs). Table 9 lists the device signal for each of the fifteen BSCs that comprise the BSR.

The eight BSCs connected to the ID1-8 pins form a subset of the BSR called the ID bus register (IDBR) The IDBR can be scanned without accessing the remaining BSCs of the BSR.

The IDBR is used when the ID bus is enabled to allow communication between a PBC and one or more RBCs.

Figure 5 illustrates the order of scan for the boundary scan register and ID bus register.

TABLE 9. BOUNDARY SCAN REGISTER BIT MAPPING

BIT	PIN NAME	SIGNAL DESCRIPTION
. 14	MCI	Master Condition In
13	MCO	Master Condition Out
12	DCI	Device Condition In
11	DCOTS†	Enable control for DCO in 3-state configuration (active-low)
10	DCOOD†	Enable control for DCO in open-drain configuration (active-low)
9	DCO	Device Condition Out
8	IDB0E†	Enable control for ID bus (active-low)
7	ID8	Identification Bus Bit 8
6	ID7	Identification Bus Bit 7
5	ID6	Identification Bus Bit 6
4	ID5	Identification Bus Bit 5
3	ID4	Identification Bus Bit 4
2	ID3	Identification Bus Bit 3
1	ID2	Identification Bus Bit 2
0	ID1	Identification Bus Bit 1

[†] This internal signal cannot be observed from the I/O pins of the device.

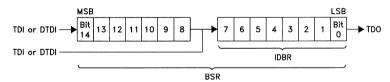


FIGURE 5. BOUNDARY SCAN REGISTER BITS AND ORDER OF SCAN

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bypass register description

The bypass register (BR) is a one-bit serial register. The function of the BR is to provide a means of effectively removing the 'ACT8999 from the primary scan path when it is not needed for the current test operation or other function of the PBC. At power-up, the BR is placed in the scan path.

Figure 6 shows the order of the scan for the bypass register.



FIGURE 6. BYPASS REGISTER BITS AND ORDER OF SCAN

counter register description

The counter register (CNTR) is an eight-bit serial register that performs a binary count if configured to do so by the control register; it uses the DCI pin as its clock. The counter can be preloaded with an initial value before counting begins, and the current value of the counter can be scanned out. Many of the features of the CNTR are configured by a bit in the control register, including:

- 1) Count direction (up or down).
- 2) Stop counting when the value of the register is 00000000.
- 3) DCI transition on which the counter counts (low-to-high or high-to-low).

An internal signal, \overline{CE} , is generated as a logic 0 when the value of the CNTR is 00000000. For any other value of the CNTR, $\overline{CE} = 1$.

The counter register can be used to count events occurring on the secondary scan path(s) and can output interrupt signals via DCO when the count has reached zero.

Figure 7 shows the order of scan for the counter register.

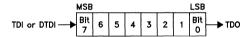


FIGURE 7. COUNTER REGISTER BITS AND ORDER OF SCAN

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enabling a remote bus controller

Bit 1 in the control register allows a remote bus controller to control parts of the 'ACT8999. When an RBC is enabled, the remote test port (RTP) in the select register is activated. The remote test port operates according to the same state diagram as the primary test port but only has access to the select register. Operation of the RTP is synchronous to TCK. OTMS is the RTP's mode select pin.

The RTP contains an eight-bit instruction register. Data is shifted in via DTDI and shifted out via DTDO. As shown in Table 10, only one instruction selects something other than the bypass register to be included in the scan path. When SCANSEL is executed, the select register is placed between DTDI and DTDO. The function of the select register, and the decoding of the select register bits by the TMS circuit, is identical regardless of which test port accesses the register.

An internal error signal, $\overline{\text{RSRERR}}$, is generated if an RBC loads an invalid value in the select register, and the MCO output goes low if the $\overline{\text{RSRERR}}$ is active and the remote TAP enters the Pause-DR state. The function table for $\overline{\text{RSRERR}}$ is shown in Table 11.

The RTP does not have access to the control register, so it cannot disable itself. The PBC must reset bit 1 in the control register to return control of the select register to the primary test port.

TABLE 10. REMOTE TEST PORT INSTRUCTION REGISTER OPCODES

BINARY CODE BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
01111110	SCANSEL	Select Register Scan	Select
ALL OTHER	BYPASS	Bypass Scan	Bypass

TABLE 11. RSRERR FUNCTION TABLE

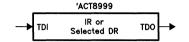
		S	ELECT RE	GISTER BIT	S			DODEDO	woot
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RSRERR	MCO†
0	X	0	Х	0	Х	0	X	1	MCI
1	X	0	X	0	X	0	Х	1	MCI
0	X	1	Х	0	Х	0	X	1	MCI
0	X	0	Х	1	Х	0	X	1	MCI
0	Х	0	Х	0	Х	1	Х	1	MCI
1	Х	1	Χ.	У	Х	Х	Х	0	L
1	X	Х	Х	1	Х	Х	Х	0	L
1	X	X	Х	Х	X	1	Х	0	L
Х	X	1	X	1	Х	Х	Х	0	L
Х	X	1	Х	Х	X	1	Х	0	L
Х	Х	Х	Х	1	Х	1	Х	0	L

[†] This table is valid only when the remote TAP is in the Pause-DR state. Under any other condition, MCO = MCI.

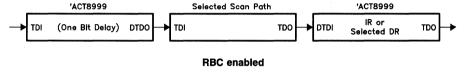
The direction of set the data flow for the selected, the 'ACTE TRIES TO THE TRIES T

The direction of serial data flow in the 'ACT8999 is dependent on the current instruction. Figure 8 shows the data flow for the different operating modes of the device. Note that when a secondary scan path is selected, the 'ACT8999 adds one bit of delay from TDI to DTDO.

RBC disabled, no secondary scan path selected



RBC disabled, secondary scan path selected



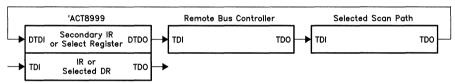


FIGURE 8. DATA FLOW IN THE 'ACT8999

bus communication protocol

The eight-bit identification bus (ID1-8) allows data transfer between a PBC and an RBC. Control register bit 2 configures the 'ACT8999 to transmit or receive command and test data via the ID bus register. The DCI, DCO, MCI, and MCO pins are used to signal the PBC and RBC(s) that a data transfer is required. The 'ACT8999 can accommodate either local or global handshake protocol depending on the number of DCO inputs that the PBC can accommodate.

Figure 9 shows a protocol for local communication between the PBC and an RBC. In this mode, communication is initiated by the PBC by driving the MCI input of the 'ACT8999 to a low level. MCI is buffered and output on MCO, which notifies the RBC that control of a scan path is to be relinquished. Prior to activating the MCI signal, the PBC scans the value 00000000 into the IDBR and enables the output buffers of ID1–8. When the RBC recognizes that MCO has gone low, it samples the ID bus and looks for the 00000000 value to verify that the PBC is going to issue further commands. Upon verifying the value on the ID bus, the RBC drives DCI low, which is buffered and output via DCO. (In this example, DCI is configured as noninverting and DCO is configured as active-low.) When the PBC sees that DCO is active, it takes MCI high, forcing MCO high. When the PBC sees that MCO is high, it takes DCO high (inactive), completing one handshake cycle.

A similar operation can ensue when the RBC initiates communication with the PBC as shown in Figure 9. Commands and test data can be exchanged between two bus controllers via the ID bus.

Figure 10 shows one way of using the ID bus to interface a PBC to multiple RBCs. The timing is similar to the local communication example in Figure 9 except that the PBC waits for all RBCs to acknowledge transmissions before switching MCI.

local PBC to RBC handshake protocol

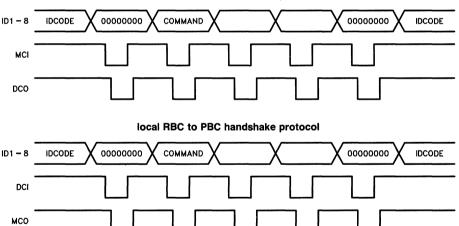


FIGURE 9. LOCAL BUS COMMUNICATION PROTOCOL

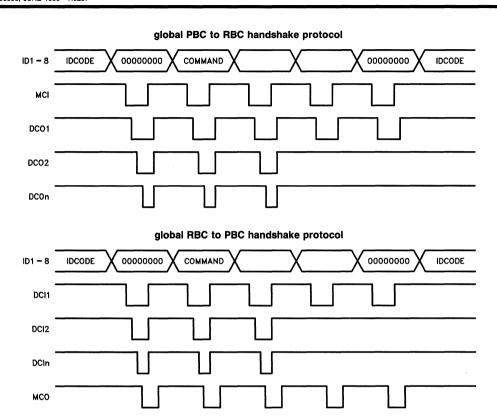


FIGURE 10. GLOBAL BUS COMMUNICATION PROTOCOL

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage range, V _I (see Note 1)	VCC + 0.5 V
Output voltage range, VO (see Note 1)0.5 V to V	VCC + 0.5 V
Input clamp current, IJK (VI < 0 or VI > VCC)	±20 mA
Output clamp current, IOK (VI < 0 or VI > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through VCC or GND pin	. ± 200 mA
Storage temperature range6	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			′54AC	T8999	'74AC	T8999	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	
VIH	High-level input voltage		2		2		v
VIL	Low-level input voltage			0.8		0.8	V
Vон	High-level output voltage	DCO		5.5		5.5	
VI	Input voltage		0	Vcc	0	VCC	V
Vo	Output voltage		0	Vcc	0	VCC	· •
		ID1-8		-1.6		-2	
ЮН	High-level output current	TDO, DTDO, MCO		-8.5		-10	
		DTMS1-4, DCO, DTRST, DTCK		- 13.6		-16	
		ID1-8		1.6		2	
	•	TDO, DTDO, MCO		8.5		10	mA
loL	Low-level output current	DTMS1-4, DCO		13.6		16	
		DTRST		20.4		24	
		DTCK		40.8		48	
TA	Operating free-air temperature		55	125	0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED TEXT COMPLETIONS			'54ACT8999		'74ACT8999		
	PARAMETER	TEST CONDITIONS	Vcc	MIN	MAX	MIN	MAX	UNIT
ЮН	DCO (open-drain)	$V_{O} = 5.5 \text{ V}$	5.5 V		20		10	μΑ
	ID1-8	IOH = -1.6 mA	4.5 V	3.7				
	101-6	$I_{OH} = -2 \text{ mA}$	4.5 V			3.7		
Va	TDO, DTDO, MCO	IOH = -8.5 mA	4.5 V	3.7				v
V OH	TDO, DTDO, MCO	I _{OH} = -10 mA	4.5 V			3.7		l v
	DTMS1-4, DCO (3-state),	IOH = -13.6 mA	4.5 V	3.7				
	DTRST, DTCK	IOH = -16 mA	4.5 V			3.7		
	ID1-8	I _{OL} = 1.6 mA	4.5 V		0.5			
	ID1-8	I _{OL} = 2 mA	4.5 V				0.5	
	TDO, DTDO, MCO	I _{OL} = 8.5 mA	4.5 V		0.5			
	TDO, DTDO, MICO	I _{OL} = 10 mA	4.5 V				0.5	
V	DTMS1-4, DCO	I _{OL} = 13.6 mA	4.5 V		0.5			v
VOL		I _{OL} = 16 mA	4.5 V	1			0.5	'
	DTRST	i _{OL} = 20.4 mA	4.5 V		0.5			Ì
	ופאוע	I _{OL} = 24 mA	4.5 V				0.5	1
	DTOV	IOL = 40.8 mA	4.5 V		0.5			
	DTCK	I _{OL} = 48 mA	4.5 V				0.5	1
loz†	ID1-8, DTDO, DTMS1-4, DTCK	V _O = V _{CC} or GND	5.5 V		±10		±5	μА
	DCO	V _O = V _{CC} or GND	5.5 V		±20		±10	1
	MCI, DCI, TCK	V _I = V _{CC} or GND	5.5 V		±1		± 1	
lj	TDI, DTDI, TMS, OTMS, TRST	VI = VCC or GND	5.5 V	-0.1	-20	-0.1	-20	μА
Icc		V _I = V _{CC} or GND, I _O = 0	5.5 V		100		100	μΑ
ΔICC [‡]		One input at VIH or VIL, Other inputs at VCC or GND	5.5 V		2		0.5	mA

[†] For I/O pins, the parameter IOZ includes the input leakage current.

[‡] This is the increase in supply current for each input being driven at TTL levels rather than VCC or GND.

PRODUCT PREVIEW

SN54ACT8999, SN74ACT8999 SCAN PATH SELECTORS WITH 8-BIT BIDIRECTIONAL DATA BUSES

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timing requirements over recommended ranges of operating free-air temperature and supply voltage

			′54AC	T8999	'74AC	T8999	LINIT
			MIN	MAX	MIN	MAX	UNIT
		TCK	0	20	0	20	MHz
^f clock		DCI (Count mode)	0	20	0	20	IVIHZ
	Dules duration	TCK high or low					
tw	Pulse duration	DCI high or low (Count mode)					ns
		TMS before TCK ↑					
		OTMS before TCK ↑					
		TDI before TCK ↑					
tsu	Setup time	DTDI before TCK ↑					ns
		MCI before TCK↑					
		DCI before TCK ↑					
		Any ID before TCK ↑			MIN MA		
		TMS after TCK ↑					
		OTMS after TCK ↑					
		TDI after TCK ↑					
th	Hold time	DTDI after TCK ↑					ns
		MCI after TCK ↑					
		DCI after TCK ↑					
		Any ID after TCK ↑					
td	Delay time	Power up to TCK↑					ns

PARAMETER	FROM	то	′54ACT8999	'74ACT8999	
PAHAMETER	(INPUT)	(OUTPUT)	MIN MAX	MIN MAX	UNIT
4	TCK		20	20	MHz
fmax	DCI (Count mode)	,	20	20	IVITIZ
tPLH	— тск↓	TDO			ns
tPHL	1000	150			113
tPLH	— тск↓	DTRST			ns
tPHL	101.4	211101			- 113
tPLH	— TCK J	Any DTMS			ns
tPHL_	751.4	7 my B i me			1,0
tPLH	— тск↓	DTDO			ns
tPHL	1010	D150			, 10
tPLH .	— тск↓	Any ID			ns
tPHL		7,			
tPLH	— TLK↓	мсо			ns
tPHL_					
tPLH	тск↓	DCO (open-drain)			ns
7 617		DCO (three-state)			
t _{PHL}	TCK↓	DCO (open-drain)			ns
		DCO (three-state)			
tPLH	TMS	Any DTMS			ns
tPHL .					
tPLH .	— отмs	Any DTMS			ns
tPHL		• • • • • • • • • • • • • • • • • • • •			
tPLH	мсі	мсо			ns
tPHL		B00 (1.:.)			
tPLH	DCI	DCO (open-drain)			ns
		DCO (three-state)			
tPHL	DCI	DCO (open-drain)			ns
		DCO (three-state)			
tPLH	TRST	DTRST			ns
t _{PHL}					
tPLH	— tck	DTCK			ns
^t PHL					

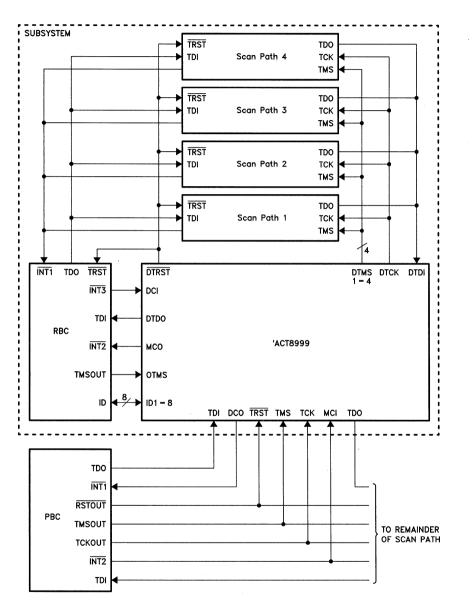
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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (continued)

PARAMETER	FROM	то	′54ACT8999	774ACT8999	UNIT
PANAMEIEN	(INPUT)	(OUTPUT)	MIN MA	X MIN MAX	UNII
^t PHZ	тск↓	DTCK			
t _{PLZ}	TON	DICK			ns
^t PHZ	— тск↓	TDO			ns
tPLZ	TON	100			115
t _{PHZ}	— тск↓	DTDO			ns
^t PLZ	TORT	B186			110
^t PHZ	тск↓	DCO			ns
^t PLZ	TORT	ВСС			115
^t PHZ	— тск↓	Any DTMS			ns
tPLZ	TORT	Any Drivio			113
^t PHZ	— тск↓	Any ID			ns
^t PLZ	101(4)	Ally ID			113
^t PZH	— тск↓	DTCK			ns
^t PZL	101(4)	BTOK			113
^t PZH	— тск↓	TDO			ns
^t PZL	TOK	100			113
₹PZH	— тск↓	DTDO			ns
^t PZL	1010	B180			113
^t PZH	— тск↓	DCO			ns
^t PZL	101.4				113
^t PZH	— тск↓	Any DTMS			ns
^t PZL	101.4	Ally D I WIG			113
^t PZH	— тск↓	Any ID			ns
^t PZL	101.4	Ally ID			113

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APPLICATION INFORMATION



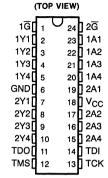
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- Members of Texas Instruments SCOPE™
 Family of Testability Products
- Octal Test Integrated Circuits
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Functionally Equivalent to SN54/74F244 and SN54/74BCT244 in the Normal Function Mode
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High (10 V) on TMS Pin
- SCOPE™ Instruction Set
 - Conform to the IEEE 1149.1 Boundary Scan
 - Provide Data Compression of Inputs
 - Provide Pseudo-Random Pattern Generation from Outputs
 - Sample Input/Toggle Output Mode
 - Output to High-Impedance-State Mode
- Fabricated Using TI's State-of-the-Art BiCMOS Technology
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

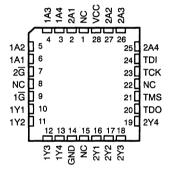
description

The SN54BCT8244 and SN74BCT8244 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit

SN54BCT8244 ... JT PACKAGE SN74BCT8244 ... DW OR NT PACKAGE



SN54BCT8244 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are functionally equivalent to the SN54/74F244 and SN54/74BCT244 octal buffers. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal buffers.

In the test mode, the normal operation of the SCOPE™ octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

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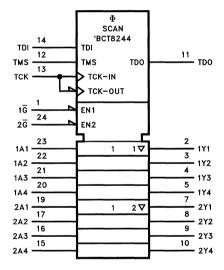
description (continued)

The SN54BCT8244 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT8244 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (NORMAL MODE)

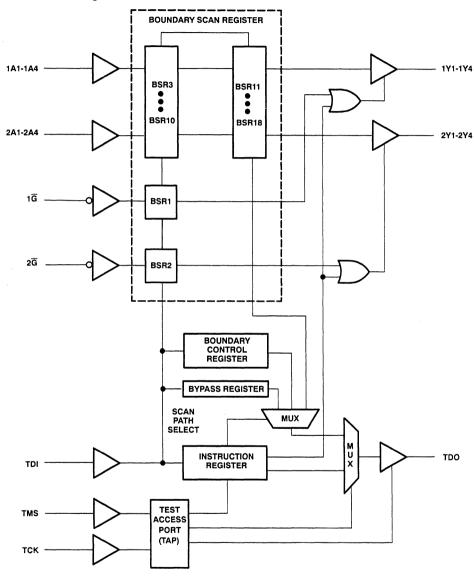
OUTPUT ENABLE	DATA INPUT	OUTPUT
G	A	Y
Н	Х	Z
L	L	L
L	н	н

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

functional block diagram



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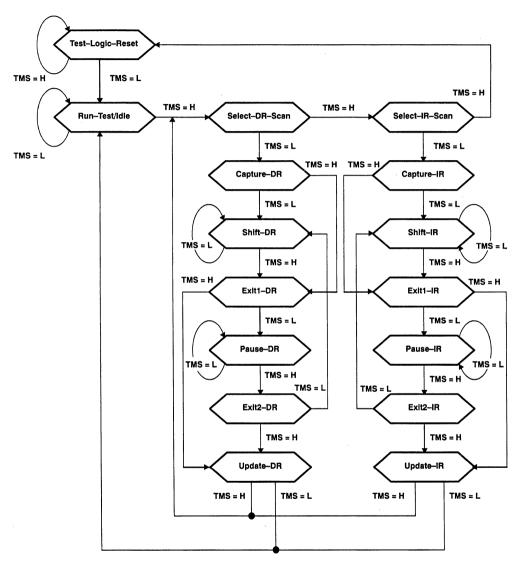


FIGURE 1. TAP STATE DIAGRAM

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state diagram description

The TAP proceeds through the states of Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset

In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR

While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

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state diagram description (continued)

Capture-IR

The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a logic 0.

Shift-IR

While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8244 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and from where to preload the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8244. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.



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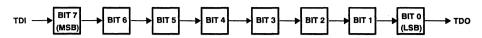


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

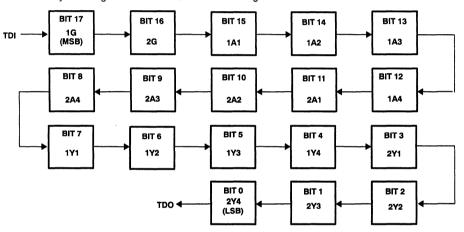


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to inplement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

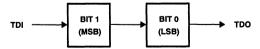


FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN



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data register descriptions (continued)

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a low level during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.

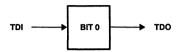


FIGURE 5. BYPASS REGISTER ORDER OF SCAN

Table 1. Instruction Register Opcodes

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

[†] The SCOPE™ instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8244.

[‡] X = Don't care.

[§] This symbol (§) indicates that a SCOPE™ opcode exists but is not supported in the 'BCT8244.

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instruction register opcode descriptions

The 'BCT8244 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan

This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan

Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary

Conforms to the IEEE Standard 1149.1 SAMPLE/PRELOAD instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance

The device outputs are placed in the high-impedance state, the bypass register is selected in the scan path. Device inputs remain operational and the internal logic function will be performed.

control boundary to 1/0

The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.

boundary run test

A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)
 - Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.
- pseudo-random pattern generation (PRPG)
 - A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.
- simultaneous PSA and PRPG
- Both PSA and PRPG operations are performed as shown in Figure 8.
- sample inputs/toggle outputs
 - Data appearing at the functional inputs is sampled on each TCK rising edge and the functional outputs are toggled on each TCK falling edge.

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instruction register opcode descriptions (continued)

boundary read

The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan

The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test

The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs

Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are as shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two enable inputs, $1\overline{G}$ and $2\overline{G}$, are ignored during these operations.

Table 2. Boundary Control Register Opcodes

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

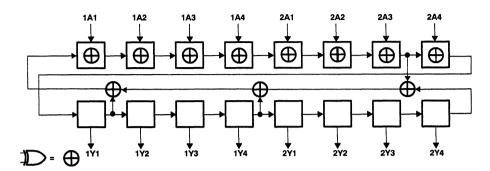


FIGURE 6. 16-BITS PSA CONFIGURATION

A PSA operation on the eight data inputs proceeds as the eight data outputs are held static.

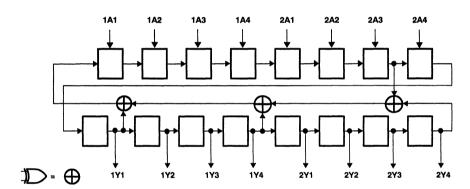


FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the eight data outputs proceeds while the eight data inputs are ignored.

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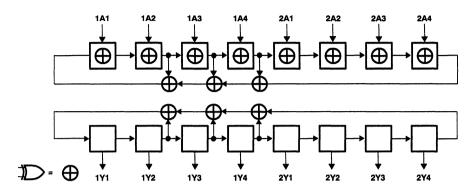


FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an eight-bit PSA operation proceeds on the eight data inputs, while an 8-bit PRPG operation proceeds from the eight data outputs.

timing description

All test operations of the 'BCT8244 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins after the falling edge of TCK.

The 'BCT8244 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

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Table 3. Explanation of Timing Example

TOK OVOLE(O)	TAP STATE	DECODIPTION (COMMENT					
TCK CYCLE(S)	AFTER TCK	DESCRIPTION/COMMENT					
1	Test-Logic-Reset	Recycle on reset state.					
2	Run-Test/Idle	Begin advancing towards desired state.					
3	Select-DR-Scan						
4	Select-IR-Scan						
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.					
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.					
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.					
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP					
14	EXILI-IN	advances from Shift-IR to Exit1-IR.					
15	Undete ID	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of					
15	Update-IR	TCK #15.					
16	Select-DR-Scan						
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.					
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.					
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value					
19-20	Shiit-DR	shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.					
21	Exit1-DR						
22	Update-DR						
23	Select-DR-Scan						
24	Select-IR-Scan						
25	Test-Logic-Reset	Test operation completed.					

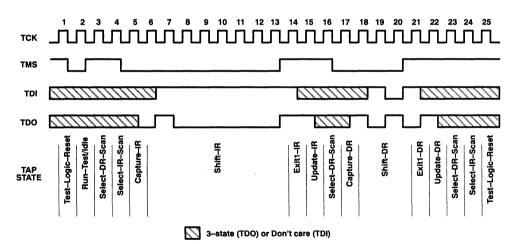


FIGURE 9. TIMING EXAMPLE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range (TMS)	
Voltage applied to any output in the disabled or power-off state	
Voltage applied to any output in the high state	-0.5 V to V _{CC}
Current into any output in the low state: SN54BCT8244 (TDO)	40 mA
SN54BCT8244 (Any Y)	96 mA
SN74BCT8244 (TDO)	48 mA
SN74BCT8244 (Any Y)	128 mA
Operating free-air temperature range: SN54BCT8244	-55°C to 125°C
SN74BCT8244	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN	54BCT8	244	SN	74BCT82	244	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2			2			٧
VIHH	Double high-level input voltage	TMS	10		12	10		12	٧
VIL	Low-level input voltage			,	0.8			0.8	٧
ΊΚ	Input clamp current			60	-18			-18	mA
1	1 E-b 11	TDO		25	-3			-3	mA
ЮН	High-level output current	Any Y	1	7	-12			- 15	mA
1	I am land a day a mant	TDO	@ [©]		20			24	^
IOL Low-level output current	Low-level output current	Any Y	4		48			64	mA
TA	Operating free-air temperature		-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER TEST CONDITIONS		iono	SN	54BCT82	244	SN	74BCT82	244			
PAH	AMETER		TEST CONDITI	UNS	MIN	TYP	MAX	MIN	TYP†	MAX	UNIT
VIK		$V_{CC} = 4.5 V$	I _I = -18 mA				-1.2			-1.2	V
		$V_{CC} = 4.75 V$		IOH = -3 mA	2.7	3.4		2.7	3.4		
	Any Y			IOH = -3 mA	2.4	3.4		2.4	3.4		
Va.,	Ally			IOH = -12 mA	2	3.2					٧
VOH		$V_{CC} = 4.5 V$		IOH = -15 mA				2	3.1		•
	TDO			IOH = -1 mA	2.5	3.4		2.5	3.4		
	100			IOH = -3 mA	2.4	3.3		2.4	3.3		
	Any Y			IOL = 48 mA		0.38	0.55				
\v	Ally f	V _{CC} = 4.5 V		IOL = 64 mA					0.42	0.55	٧
VOL	TDO	7 VCC - 4.5 V		IOL = 20 mA		0.3	0,5				v
	100			IOL = 24 mA			**		0.35	0.5	
ll .		$V_{CC} = 5.5 V$,	$V_{I} = 5.5 V$				0.1			0.1	mA
lн		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$		-1	100	- 100	-1		-100	μΑ
ІНН	TMS	$V_{CC} = 5.5 V,$	$V_I = 10 V$		200		1			1	mA
IL		$V_{CC} = 5.5 V,$	$V_{I} = 0.5 V$		100 P		-200			-200	μΑ
lozu	Any Y	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$		100		50			50	^
lozh	TDO	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$		-1		-100	-1		-100	μΑ
1071	Any Y	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-50			-50	μΑ
lozL	TDO	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-200			-200	μΛ
los‡		$V_{CC} = 5.5 V,$	$V_O = 0$		-100		-225	-100		- 225	mA
				Outputs high		3.5	7.5		3.5	7.5	
Icc		$V_{CC} = 5.5 V,$	Outputs open	Outputs low		31	52		31	52	mΑ
				Outputs disabled		1.5	3.5		1.5	3.5	
Ci			$V_{ } = 2.5 V or C$).5 V		10			10		рF
Co		$V_{CC} = 5 V$	$V_0 = 2.5 V or$	0.5 V		18			18		pF

timing requirements

				V _{CC} = 5 V, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX§				
			'BC1	8244	'54BC	T8244	'74BC	'74BCT8244		
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency	TCK	0	20	0	20	0	20	MHz	
	51.1.0	TCK high or low	25		25		25			
t _w Pulse duration	TMS reset high	50		50	and the second	50		ns		
		TMS before TCK ↑	15		15	37	15			
_	0.1.5	TDI before TCK ↑	6		6	G .	6			
t _{su}	Setup time	Any A before TCK ↑	6		6	Sys.	6		ns	
		Any G before TCK ↑	- 6		6		6			
		TMS after TCK ↑	0		0		0			
_		TDI after TCK ↑	4.5		4.5		4.5		1	
th	Hold time	Any A after TCK ↑	4.5		4.5		4.5		ns	
		Any G after TCK↑	4.5		4.5		4.5		1	
td	Delay time, power-up to TCK ↑		100		100		100		ns	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

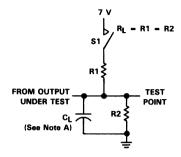
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switching characteristics (see Figure 10)

			_	C = 5	. 1	٧c	C = 4.5 CL =	V to 5.5	٧,	
			_	= 50 p			i l			
	FROM	то	ŀ				R1 = 1			
PARAMETER	(INPUT)	(OUTPUT)	1	= 500		_	R2 =			UNIT
					C .			to MAX		
				3CT8244		'54BC		'74BC'		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	TCK		20			20		20		MHz
tPLH	Any A	Y	1.6	5.6	7.6	1.6	10.3	1.6	8.8	ns
t _{PHL}	Ally A	"	1.7	6	8.2	1.7	10.7	1.7	9.6	110
tPLH .	тск↓	Y	6.5	13.4	17	6.5	25.2	6.5	21.4	ns
t _{PHL}	101.1	'	5.7	13	16.3	5.7	23.7	5.7	20.5	115
tPLH	тск↓	TDO	3	11.1	14.3	3	21	3	17.9	
tPHL		100	3	10.8	13.9	3	19.8	3	17.2	ns
tPLH t		Υ .	7.5	17.3	22	7.5	33.3	7.5	27.5	
^t PHL	тск↑	Υ	7.5	18.1	22.8	7.5	34.2	7.5	28.3	ns
^t PZH	A	V	2.3	6.6	8.7	2.3	11.6	2.3	10.4	
tPZL	Any G	Y	2.6	7.9	10	2.6	13.2	2.6	12	ns
t _{PZH}	TOU !	.,	7.2	13.8	17.5	7.2	25.7	7.2	22.3	
tPZL	тск↓	Y	7.3	15.1	18.9	7.3	27.3	7.3	23.8	ns
^t PZH	TOUL	TDO	3.4	7.8	10.1	3.4	13.9	3.4	12.3	
tPZL	тск↓	TDO	4.4	9.4	11.8	4.4	15.3	4.4	14	ns
tPHZ	Any G	Y	1.7	6.2	8.2	1.7	10.7	1.7	9.9	
tPLZ		1	1	6	8.1	1	11	1	9.6	ns
tPHZ	тск↓		4	11.5	14.8	4	21.9	4	19	I
tPLZ		Y	5.2	12.1	15.5	5.2	23.4	5.2	19.9	ns
tPHZ	TOV I	TDO	4	8.6	11	4	15.3	4	14	
tPLZ	тск↓	TDO	3.9	8	10.5	3.9	14.7	3.9	12.9	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

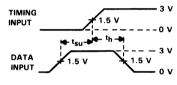
PARAMETER MEASUREMENT INFORMATION



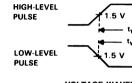
SWITCH POSITION TABLE

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
t _{PHZ}	Open
tPLZ	Closed

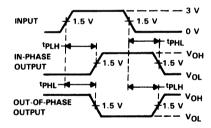
LOAD CIRCUIT



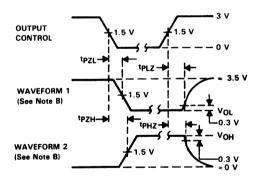
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_f = 3$ ns. For testing pulse duration: $t_f = 1$ to 3 ns. $t_f = 1$ to 3 ns. Pulse polarity can be either a high-to-low-to-high or low-to-high-to-low.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS



SN54BCT8245, SN74BCT8245 SCAN TEST DEVICES WITH OCTAL BUS TRANSCEIVERS

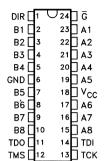
TI0038--- D3514, MAY 1990

- Members of Texas Instruments SCOPE™
 Family of Testability Products
- Octal Test Integrated Circuits
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus Protocol
- Functionally Equivalent to SN54/74F245 and SN54/74BCT245 in the Normal Function Mode
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High (10 V) on TMS Pin
- SCOPE™ Instruction Set
 - Conform to the IEEE 1149.1 Boundary
 - Provide Data Compression of Inputs
 - Provide Pseudo-Random Pattern Generation from Outputs
 - Sample Input/Toggle Output Mode
 - Output to High-Impedance-State Mode
- Fabricated Using TI's State-of-the-Art BiCMOS Technology
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

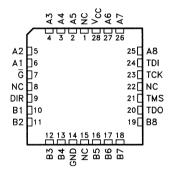
description

The SN54BCT8245 and SN74BCT8245 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54BCT8245 ... JT PACKAGE SN74BCT8245 ... DW OR NT PACKAGE (TOP VIEW)



SN54BCT8245 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

In the normal mode, these devices are functionally equivalent to the SN54/74F245 and SN54/74BCT245 octal bus transceivers. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal bus transceivers.

SCOPE is a trademark of Texas Instruments Incorporated.



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description (continued)

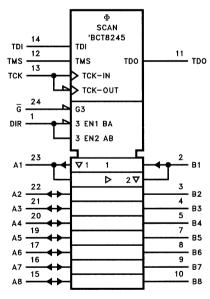
In the test mode, the normal operation of the SCOPE™ octal bus transceiver is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8245 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT8245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (Normal Mode)

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

logic symbol†

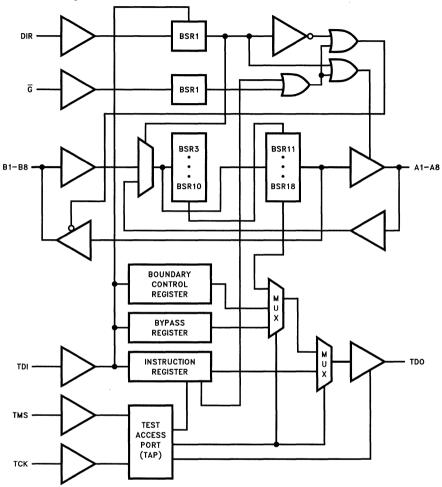


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



D3514, MAY 1990-TI0038

functional block diagram



TI0038-D3514, MAY 1990

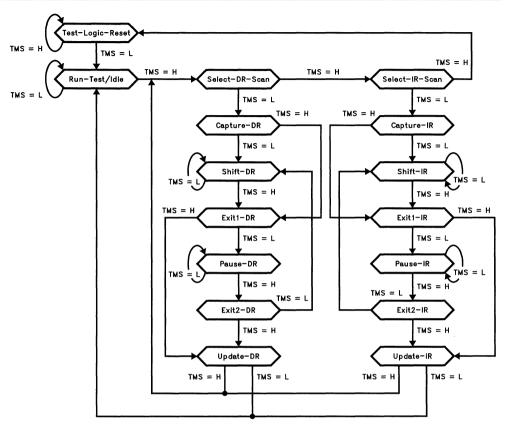


FIGURE 1. TAP STATE DIAGRAM

D3514, MAY 1990-TI0038

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset

In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR

While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

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state diagram description (continued)

Capture-IR

The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation. TDO will enable to a low level.

Shift-IR

While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR, Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8245 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8245. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.



D3514, MAY 1990-TI0038

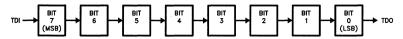


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figures 3 and 4. Note that the order of scan depends on the level of the DIR signal, which determines the direction of data flow (A to B or B to A).

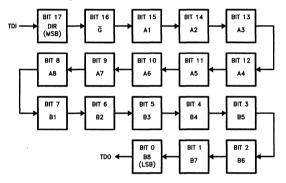


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN (A TO B MODE)

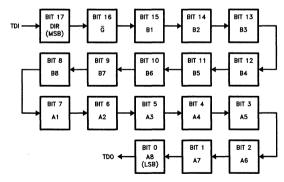


FIGURE 4. BOUNDARY SCAN REGISTER ORDER OF SCAN (B TO A MODE)

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data register descriptions (continued)

boundary control register

The boundary control register (BCR) contains two bits and is used to inplement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 5.

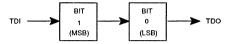


FIGURE 5. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 6.

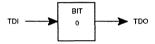


FIGURE 6. BYPASS REGISTER ORDER OF SCAN

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TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE§	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X000001	BYPASS*	Bypass Scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS*	Bypass Scan	Bypass	Normal
X0000101	BYPASS*	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS*	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

[†] The SCOPE™ instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8245.

instruction register opcode descriptions

The 'BCT8245 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan

This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan

Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary

Conforms to the IEEE Standard 1149.1 SAMPLE/PRELOAD instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance

The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational and the internal logic function will be performed.

control boundary to 1/0

The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.



[‡] X = Don't care.

[§] A SCOPE™ opcode exists but is not supported in the 'BCT8245.

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instruction register opcode descriptions (continued)

boundary run test

A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)
 - Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figures 7 and 8 show the algorithm through which the signature is generated.
- pseudo-random pattern generation (PRPG)
 - A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figures 9 and 10 show the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.
- simultaneous PSA and PRPG
 - Both PSA and PRPG operations are performed as shown in Figures 11 and 12.
- sample inputs/toggle outputs
 - Data appearing at the functional inputs is sampled on each TCK rising edge and the functional outputs are toggled on each TCK falling edge.

boundary read

The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan

The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test

The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs

Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

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tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 7 through 12. The enable input \overline{G} is ignored during PSA and PRPG operations, and DIR is not used except to determine the direction of data flow.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
. 00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode

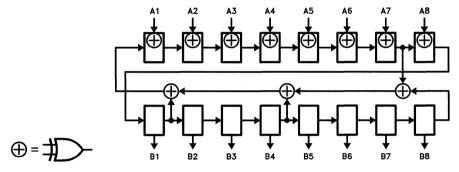


FIGURE 7. 16-BIT PSA CONFIGURATION (A TO B MODE)

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

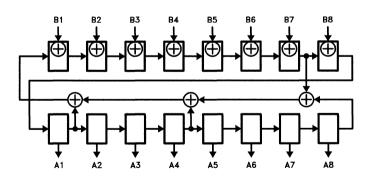


FIGURE 8. 16-BIT PSA CONFIGURATION (B TO A MODE)

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

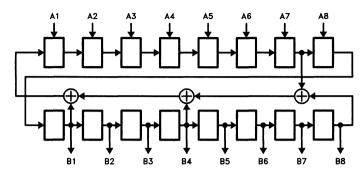


FIGURE 9. 16-BIT PRPG CONFIGURATION (A TO B MODE)

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

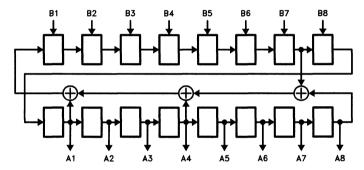


FIGURE 10. 16-BIT PRPG CONFIGURATION (B TO A MODE)

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

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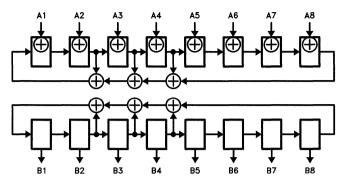


FIGURE 11, 8-BIT PSA AND PRPG CONFIGURATION (A TO B MODE)

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

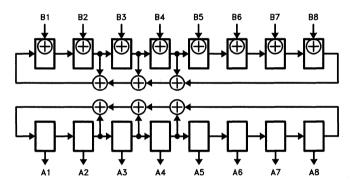


FIGURE 12. 8-BIT PSA AND PRPG CONFIGURATION (B TO A MODE)

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

timing description

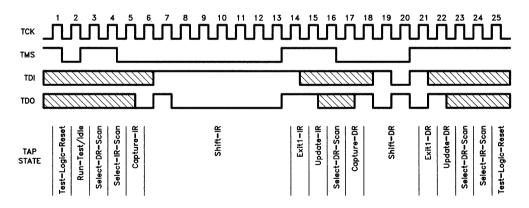
All test operations of the 'BCT8245 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8245 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 13. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

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TADIE	2	EVDI	MALTION	OF TIMING	EVAMBLE
IABLE	-35	EXPL	ANAIIUN	OF HIMING	EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state
2	Run-Test/Idle	Begin advancing towards desired state
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7-13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP
14		advances from Shift-IR to Exit1-IR.
15	Lindata ID	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of
15	Update-IR	TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19–20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value
19-20	Shiit-Dh	shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed



3-state (TDO) or Don't Care (TDI)

FIGURE 13. TIMING EXAMPLE

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SN74BCT8245 0°C to 70°C

Storage temperature range – 65°C to 150°C

recommended operating conditions

			SN	4BCT82	245	SN7	74BCT82	245	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2		5.5	2		5.5	٧
VIHH	Double high-level input voltage	TMS	10	W	12	10		12	٧
VIL	Low-level input voltage			ð.	0.8			0.8	٧
ΊΚ	Input clamp current			j.	- 18			-18	mA
	I E-b II	Any A, TDO		3	-3			-3	4
ЮН	High-level output current	Any B		43	- 12			-15	mA
•		Any A, TDO		is.	20			24	
IOL	Low-level output current	Any B	Q		48			64	mA
TA	Operating free-air temperature		-55		125	0		70	°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN	54BCT82	45	SN74BCT8245			
	ARAMETER	TEST CONDITIO	ons	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2			-1.2	٧
		V _{CC} = 4.75 V	IOH = -1 mA	2.7	3.4		2.7	3.4		
	Any A, TDO	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		
		VCC = 4.5 V	$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		
Vон		V _{CC} = 4.75 V	$I_{OH} = -3 \text{ mA}$	2.7	3.4		2.7	3.4		٧
	Any B		IOH = -3 mA	2.4	3.4		2.4	3.4		
	Ally B	V _{CC} = 4.75 V	$I_{OH} = -12 mA$	2	3.2					
			IOH = -15 mA				2	3.1		
	Any A, TDO	V _{CC} = 4.5 V	$I_{OL} = 20 \text{ mA}$		0.3	0.5				
VOL	Ally A, 100	VCC - 4.5 V	IOL = 24 mA		, i			0.35	0.5	V
VOL	Any B	VCC = 4.5 V	IOL = 48 mA		0.38	0.55				•
		VCC - 4.5 V	IOL = 64 mA		64			0.42	0.55	
l _I	Except A or B	$V_{CC} = 5.5 \text{ V}, V_{I} = 5.5 \text{ V}$			e e	0.1			0.1	mA
'	Any A or B	$V_{CC} = 5.5 \text{ V}, V_{I} = 5.5 \text{ V}$			žu.	0.25			0.25	1117
ήH‡		$V_{CC} = 5.5 V, V_{I} = 2.7 V$		-1	- 35	-100	-1	- 35	- 100	μΑ
ЧНН	TMS	$V_{CC} = 5.5 \text{ V}, V_{I} = 10 \text{ V}$			A.	1			1	mA
IIL‡		$V_{CC} = 5.5 V, V_{I} = 0.5 V$		6	~ – 70	-200		-70	- 200	μΑ
lozh	TDO	$V_{CC} = 5.5 \text{V}, V_{O} = 2.7 \text{V}$		-1	- 35	-100	-1	-35	- 100	μΑ
IOZL	TDO	$V_{CC} = 5.5 V, V_O = 0.5 V$			-70	-200		-70	-200	μΑ
los§		$V_{CC} = 5.5 V, V_O = 0$		-100		-225	-100		- 225	mA
			Outputs high		3.6	7.5		3.6	7.5	
ICC*		V _{CC} = 5.5 V, Outputs Open			35	52		35	52	mΑ
			Outputs disabled		1.5	3.5		1.5	3.5	
Ci		$V_{CC} = 5.5 V, V_{I} = 0.5 V$			8			8		pF
Cio		$V_{CC} = 5.5 \text{V}, V_{O} = 0.5 \text{V}$			14			14		рF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

^{*} ICCH and ICCL are measured in the A to B mode.

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timing requirements

				V _{CC} = 5 V, T _A ≈ 25°C		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $T_A = \text{MIN to MAX}^{\dagger}$				
			'BCT	8245	'54BCT8245		'74BCT8245		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency	TCK	0	20	0	20	0	20	MHz	
	Dulas dunation	TCK high or low	25		25		25			
tw	Pulse duration	TMS reset high			50		50		ns	
		TMS before TCK ↑	12		12	4	12			
	0.1	TDI before TCK ↑	6		6	34.8	6			
tsu	Setup time	Any A or B before TCK↑	6		(6)	7¢.	6		ns	
		DIR or G before TCK↑	6		⟨ 6⟨	7	6		1	
		TMS after TCK ↑	0		₹0		0			
		TDI after TCK ↑	4.5		4.5		4.5		1	
th	Hold time	Any A or B after TCK↑	4.5		4.5		4.5		ns	
		DIR or G after TCK↑	4.5		4.5		4.5		1	
^t d	Delay time	Power-up to TCK ↑	100		100		100		ns	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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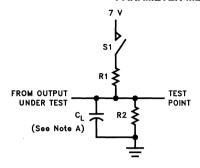
switching characteristics (see Figure 14)

			1	C = 5		٧c	C = 4.5		٧,	
ļ			CL	$C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$			$C_L = 50 pF$,			
			R1				R1 =	500 Ω,		
PARAMETER	FROM (INPUT)	TO	R2	= 500	Ω,		R2 =	500 Ω,		UNIT
	(INPUT)	(OUTPUT)	_ T,	4 = 25°	С	T,	a = MIN	l to MA)	(†	
]			'I	BCT8245	5	'54BC	T8245	'74BC	T8245	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	TCK		20			20		20		MHz
^t PLH	A or B	B or A	1.6	5.5	7.6	1.6	9.6	1.6	8.7	ns
^t PHL	A or B	B or A	1.7	5.7	8	1.7	9.9	1.7	9.4	ns
t _{PLH}	TCK ↓	A or B	3.9	10.9	15.7	3.9	21.5	3.9	19.8	ns
t _{PHL}	TCK↓	A or B	3.9	10.8	15.3	3.9	21.5	3.9	19.5	ns
tPLH .	TCK↓	TDO	3.2	8.5	12.3	3.2	16.8	3.2	15.4	ns
tPHL	TCK↓	TDO	3.2	8.3	12	3.2	16.2	3.2	15	ns
tPLH .	TCK↑	A or B	6.2	13.9	21	6.2	. 29	6.2	25	ns
t _{PHL}	TCK↑	A or B	6.6	15	22	6.6	29	6.6	26	ns
^t PZH	Ğ	A or B	2.3	6.3	8.7	2.3	11.1	2.3	10.6	ns
^t PZH	TCK↓	A or B	4.7	11.7	16.7	4.7	23.1	4.7	21.1	ns
^t PZH	TCK↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
tPZL	G	A or B	2.6	8.2	11.7	2.6	14.3	2.6	13.8	ns
tPZL	TCK↓	A or B	5.5	13.6	19.7	5.5	26.8	5.5	24.8	ns
tPZL	TCK↓	TDO	3.2	7.6	10.6	3.2	13.2	3.2	12.6	ns
tPHZ	Ğ	A or B	1.7	6	8.4	1.7	10.2	1.7	9.6	ns
tpHZ	TCK↓	A or B	3.4	9.1	13.2	3.4	18.7	3.4	17.3	ns
tPHZ	TCK↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
tPLZ	G	A or B	1.5	5.6	8	1.5	10.5	1.5	9.7	ns
tPLZ	TCK↓	A or B	3.6	10	14.6	3.6	19.5	3.6	17.8	ns
tPLZ	TCK↓	TDO	2.2	5.9	8.7	2.2	12.7	2.2	11.6	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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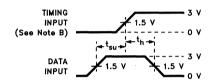
PARAMETER MEASUREMENT INFORMATION



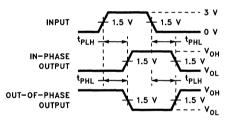
SWITCH FO	SITION TABLE
TEST	S1

TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
t _{PHZ}	Open
tPLZ	Closed

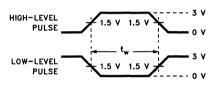
LOAD CIRCUIT



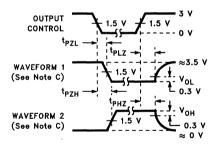
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 14. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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Members of Texas Instruments SCOPE™ Family of Testability Products

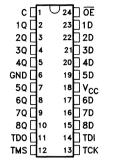
- Octal Test Integrated Circuits
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Functionally Equivalent to SN54/74F373 and SN54/74BCT373 in the Normal Function Mode
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin
- SCOPE™ Instruction Set
 - Conform to the IEEE 1149.1 Boundary Scan
 - Provide Data Compression of Inputs
 - Provide Pseudo-Random Pattern Generation From Outputs
 - Sample Input/Toggle Output Mode
 - Output to High-Impedance State Mode
- Fabricated Using TI's State-of-the-Art BiCMOS Technology
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

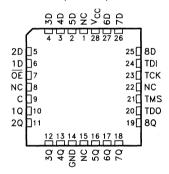
The SN54BCT8373 and SN74BCT8373 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

SN54BCT8373 ... JT PACKAGE SN74BCT8373 ... DW OR NT PACKAGE

(TOP VIEW)



SN54BCT8373 ... FK PACKAGE (TOP VIEW)



NC-No internal connection

In the normal mode these devices are functionally equivalent to the SN54/74F373 and SN54/74BCT373 octal D-type latches. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ octal latches.

SCOPE is a trademark of Texas Instruments Incorporated.



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description (continued)

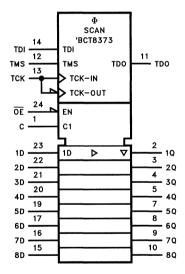
In the test mode the normal operation of the SCOPE™ octal latch is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS (test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8373 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT8373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)

11	NPUTS	OUTPUT	
OE	С	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
н	Χ	Х	z

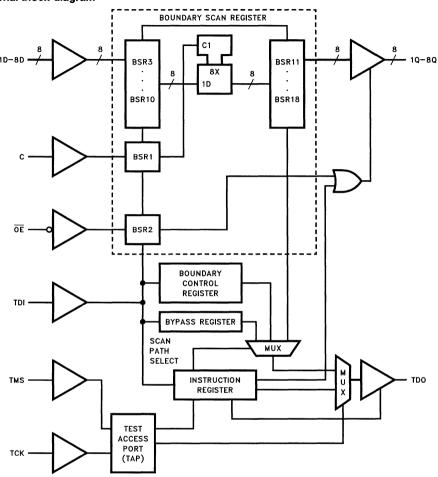
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

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functional block diagram



D8373 JUNE 1990-TI0222

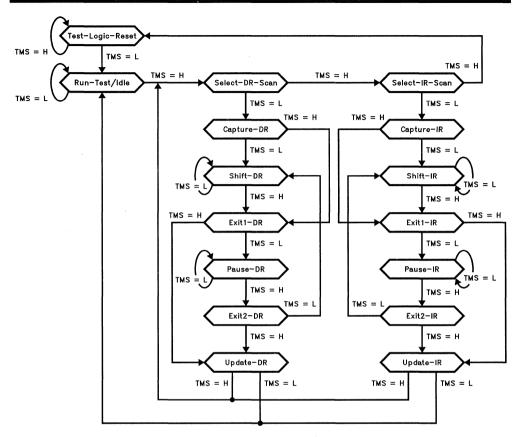


FIGURE 1. TAP STATE DIAGRAM

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state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

Test-Logic-Reset

In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR

While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

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state diagram description (continued)

Capture-IR

The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-IR

While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK, and outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8373 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8373. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.



FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN

data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device, and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

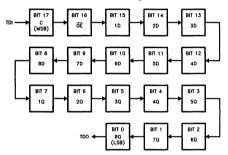


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to implement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

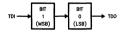


FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.



FIGURE 5. BYPASS REGISTER ORDER OF SCAN



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TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

[†] The SCOPE instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8373.

instruction register opcode descriptions

The 'BCT8373 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan

This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan

Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary

Conforms to the IEEE Standard 1149.1 SAMPLE instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance

The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational, and the internal logic function will be performed.

control boundary to 1/0

The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.



[‡] X = Don't care.

[§] A SCOPE opcode exists but is not supported in the 'BCT8373.

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instruction register opcode descriptions (continued)

boundary run test

A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register, and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)

Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.

- pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.

- simultaneous PSA and PRPG

Both PSA and PRPG operations are performed as shown in Figure 8.

- sample inputs/toggle outputs

Data appearing at the functional inputs is sampled on each TCK rising edge, and the functional outputs are toggled on each TCK falling edge.

boundary read

The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan

The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test

The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs

Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these TAP bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two control inputs, C and \overline{OE} , are ignored during these operations.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode



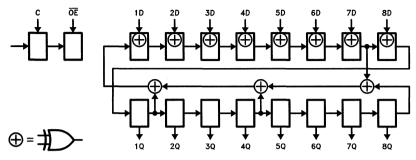


FIGURE 6. 16-BIT PSA CONFIGURATION

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

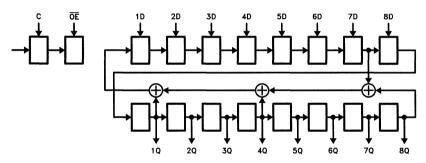


FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the eight data outputs proceeds while the inputs are ignored.

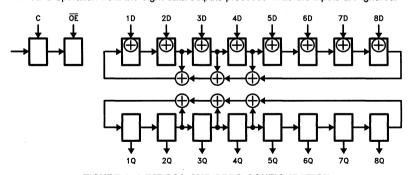


FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.



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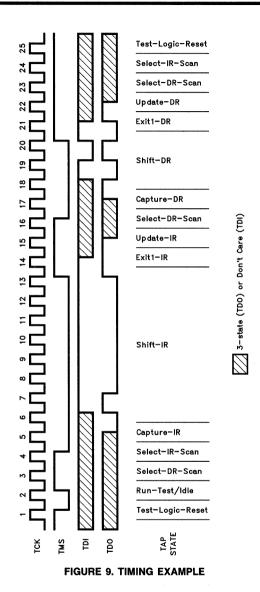
timing description

All test operations of the 'BCT8373 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8373 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7–13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
	E 114 IB	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP
14	Exit1-IR	advances from Shift-IR to Exit1-IR.
4-		The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of
15	Update-IR	TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
40.00	Orig DD	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value
19–20	Shift-DR	shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	-0.5 V to 7 V
Input voltage range, V _I (except TMS)	-0.5 V to 7 V
Input voltage range, V _I (TMS)	-0.5 V to 12 V
Voltage applied to any output in the disabled or power-off state	-0.5~V to $5.5~V$
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state: SN54BCT8373 (TDO)	40 mA
SN54BCT8373 (Any Q)	96 mA
SN74BCT8373 (TDO)	48 mA
SN74BCT8373 (Any Q)	128 mA
Operating free-air temperature range: SN54BCT8373	-55°C to 125°C
SN74BCT8373	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN	SN54BCT8373			SN74BCT8373		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
VIH	High-level input voltage		2		-22	2			٧
VIHH	Double high-level input voltage	TMS	10	8.6	12	10	8.6	12	٧
VIL	Low-level input voltage			29	0.8			0.8	٧
ΊΚ	Input clamp current				-18			- 18	mA
1	High level and an arrange	TDO		2	-3			-3	
ЮН	High-level output current	Any Q	- A		-12			-15	mA
1	1 1 1 1 1	TDO	4		20			24	
lOL	Low-level output current	Any Y			48			64	mA
TA	Operating free-air temperature		-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					SN	54BCT83	73	SN	74BCT83	373	
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	MIN	TYP	MAX	UNIT	
VIK		$V_{CC} = 4.5 V,$	$I_{\rm I} = -18 \rm mA$				-1.2			-1.2	٧
		V _{CC} = 4.75 V		IOH = -3 mA	2.7	3.4		2.7	3.4		
	4			IOH = -3 mA	2.4	3.4		2.4	3.4		
V	Any Q			IOH = -12 mA	2	3.2					v
VOH		$V_{CC} = 4.5 V$		$I_{OH} = -15 \text{ mA}$				2	3.1		V
	TDO	}		IOH = -1 mA	2.5	3.4		2.5	3.4		
	100			IOH = -3 mA	2.4	3.3		2.4	3.3		
	40			I _{OL} = 48 mA		0.38	0.55				
V	Any Q	V 45V		IOL = 64 mA					0.42	0.55	v
VOL	TDO	V _{CC} = 4.5 V		IOL = 20 mA		0.3	0.5				٧
	100			IOL = 24 mA			il.		0.35	0.5	
IJ		$V_{CC} = 5.5 V$,	V _I = 5.5 V			0 P	0.1			0.1	mA
ΊΗ		$V_{CC} = 5.5 V$	$V_{ } = 2.7 V$		-1	435	-100	1	-35	-100	μΑ
IHH	TMS	$V_{CC} = 5.5 V$	V _I = 10 V		-	0.3	1		0.3	1	mA
IL		$V_{CC} = 5.5 V$	$V_{ } = 0.5 V$		600,	-70	-200		-70	-200	μА
	Any Q	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$		8,		50			50	
IOZH	TDO	$V_{CC} = 5.5 V,$	V _O = 2.7 V		-1	-35	-100	-1	-35	100	μΑ
1	Any Q	$V_{CC} = 5.5 V$,	$V_{O} = 0.5 V$				-50			-50	
IOZL	TDO	$V_{CC} = 5.5 V$	V _O = 0.5 V			-70	-200		-70	-200	μΑ
los‡		$V_{CC} = 5.5 V$	V _O = 0		-100		-225	-100		-225	mA
				Outputs high		3.5	7		3.5	7	
ICC		$V_{CC} = 5.5 V,$	Outputs open	Outputs low		35	52		35	52	mA
				Outputs disabled		1.5	3.5		1.5	3.5	
Ci		V _{CC} = 5 V,	$V_1 = 2.5 \text{V or } 0$).5 V		10			10		pF
Ci	ŌĒ	V _C C = 5 V,	V _I = 0.5 V			8			8		pF
Co		V _{CC} = 5 V,	V _O = 2.5 V or	0.5 V		14			14		pF
A 11 A	-1	t Voc = 5 V Ta	0500								

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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timing requirements

			V _{CC} = 5 V, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX [†]					
			'BCT8373		'54BCT8373		'74BCT8373		UNIT		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency	TCK	0		20	0	20	0	20	MHz	
tw	Pulse duration	TCK high or low	25			25		25		T	
·w	r dioc daration	TMS reset high	50			50	dens.	50		ns	
		TMS before TCK ↑	15			15	14	15			
t _{su}	Setup time	TDI before TCK ↑	6			6	E.	6		ns	
'Su	cotup unio	Any D before TCK ↑	6			6	42.	6			
		OE before TCK↑	6			6	r.:	6			
		TMS after TCK ↑	0			o,		0			
th	th Hold time	TDI after TCK ↑	4.5			4.5		4.5			
iii	Any D after TCK ↑				4.5		4.5		ns		
		OE after TCK↑	4.5			4.5		4.5			
tpu		Wait time, power up to TCK↑	100			100		100		ns	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

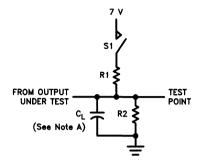
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switching characteristics (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	CC = 5 = 50 p = 500 = 500 A = 25°	ο F, Ω, Ω,	_	C _L = R1 = R2 =	500 Ω,		UNIT
				BCT837		′54BC		′74BC		
	TCK	L	MIN 20	TYP	MAX	MIN 20	MAX	MIN 20	MAX	MHz
fmax	TOK	T	20	5.6	9	20	11.5	20	10	MILIZ
tPLH	D	Any Q	2	5.5	9	2	10.6	2	10	ns
tPHL to use			3	6.7	10.5	3	12.9	3	11.4	
tPLH tPHL	С	Q	3	6.7	10.5	3	12.8	3	11.6	ns
			3.9	10.9	15.7	3.9	21.5	3.9	19.8	
tPLH tPHL	тск↓	Any Q	3.9	10.8	15.7	3.9	21.5	3.9	19.5	ns
tPLH			3.2	8.5	12.3	3.2	16.8	3.2	15.4	
tPHL	TCK↓	TDO	3.2	8.3	12	3.2	16.2	3.2	15.4	ns
tPLH		Any Q	6.2	13.7	21	6.2	29	6.6	25	ns
tPHL	TCK↑		6.6	15.7	22	6.6	29.6	6.6	26	
tPZH			2.4	5.6	9	2.4	11.1	2.4	10.6	
tPZL	ŌĒ	Any Q	3	6.8	10.9	3		3	12	ns
tPHZ		 	2.5	5.7	9.5	2.5	7 7 Zec	2.5	10	
tPLZ	ŌĒ	Any Q	2.4	5.5	9	2.4	20	2.4	9.6	ns
tPZH			4.7	11.7	16.7	4.7	23.1	4.7	21.1	
tPZL	TCK↓	Any Q	5.5	13.6	19.7	5.5	24.4	5.5	22.9	ns
tPHZ			3.4	9	13.2	3.4	18.7	3.4	17.3	
tPLZ	тск↓	Any Q	3.6	10	14.6	3.6	19.5	3.6	17.8	ns
tPZH		 	6.9	15.5	21.7	6.9	30	6.9	27	
tPZL	TCK↑	Any Q	7.8	17.6	24.9	7.8	32	7.8	29	ns
tPHZ			5	12.7	18.3	5	25.5	5	22.8	
tPLZ	TCK↑	Any Q	4.6	12.2	17.5	4.6	24.7	4.6	22	ns
tPZH			2.4	6.2	9	2.4	11.3	2.4	10.8	
tPZL	тск↓	TDO	3.2	7.6	10.6	3.2	13.2	3.2	12.6	ns
tPHZ			2.6	7.1	10.2	2.6	13	2.6	12.8	
tPLZ	TCK↓	TDO	2.2	5.9	8.7	2.2	12.7	2.2	11.6	ns

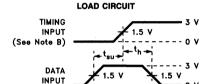
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

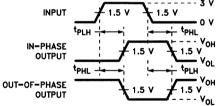


SWITCH POSITION TABLE

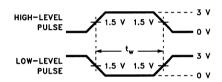
TEST	S1
tPLH	Open
tPHL	Open
tPZH	Open
tPZL	Closed
tPHZ	Open
tPLZ	Closed



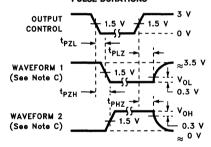
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS



SN54BCT8374, SN74BCT8374 SCAN TEST DEVICES WITH OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

TI0223-D3641, JUNE 1990

Members of Texas Instruments SCOPE™ Family of Testability Products

- Octal Test Integrated Circuits
- Compatible With the IEEE Standard 1149.1 (JTAG) Serial Test Bus
- Functionally Equivalent to SN54/74F374 and SN54/74BCT374 in the Normal Function Mode
- Test Operation Synchronous to Test Access Port (TAP)
- Implement Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin
- SCOPE™ Instruction Set
 - Conform to the IEEE 1149.1 Boundary Scan
 - Provide Data Compression of Inputs
 - Provide Pseudo-Random Pattern Generation From Outputs
 - Sample Input/Toggle Output Mode
 - Output to High-Impedance State Mode
- Fabricated Using TI State-of-the-Art BiCMOS Technology
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

The SN54BCT8374 and SN74BCT8374 are members of Texas Instruments SCOPE™ testability IC family. This family of components blends test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

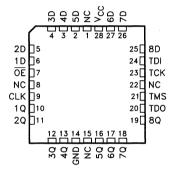
SN54BCT8374 ... JT PACKAGE SN74BCT8374 ... DW OR NT PACKAGE (TOP VIEW)

CLK TI V24 TOE 10 ∏2 23 1 D 20 □3 22 | D 30 □4 21 7 3D 40 ∏5 20 T 4D GND ∏6 19 5D 5Q 🗆 7 18∐ V_{CC} 6Q ∏8 17 6D 70 ∏9 16 7 D 15 🗌 8D 8Q 🛮 10 TDO []11 14 TDI

SN54BCT8374 ... FK PACKAGE (TOP VIEW)

13 TCK

TMS 12



NC-No internal connection

In the normal mode these devices are functionally equivalent to the SN54/74F374 and SN54/74BCT374 octal D-type flip-flops. In the test mode, the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ octal flip-flops.

In the test mode the normal operation of the SCOPE™ octal flip-flop is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the IEEE Standard 1149.1 specification. Four dedicated test pins are used to control the operation of the test circuitry: TDI (test data in), TDO (test data out), TMS

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SN54BCT8374, SN74BCT8374 SCAN TEST DEVICES WITH OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

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description (continued)

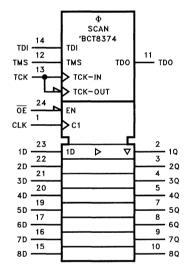
(test mode select), and TCK (test clock). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8374 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74BCT8374 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (Normal Mode) (Each Flip-Flop)

	INPUTS	OUTPUT	
OE	CLK	Q	
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	X	Х	z

logic symbol†

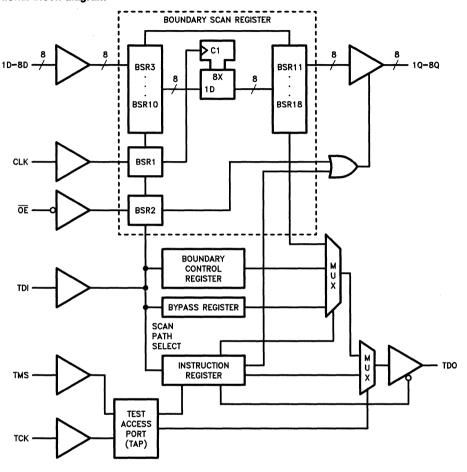


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.



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functional block diagram



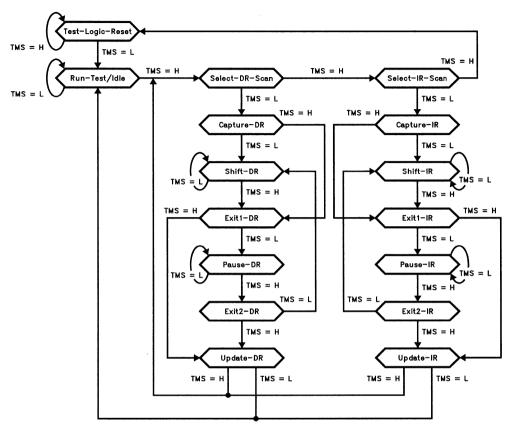


FIGURE 1. TAP STATE DIAGRAM

state diagram description

The TAP proceeds through the states shown in Figure 1 according to the IEEE Standard 1149.1. There are six stable states (indicated by a looping arrow in Figure 1) and ten unstable states in the diagram. A stable state is defined as a state the TAP can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram, one to manipulate a data register and one to manipulate the instruction register. It is necessary to finish manipulating one register before accessing another.

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state diagram description (continued)

Test-Logic-Reset

In this state, the test logic is not active and the device operates in its normal function mode. The state diagram is constructed such that the TAP will return to this state in no more than five TCK cycles if TMS is high. The TMS pin has an internal pullup resistor that will force it high if left unconnected, or if a board defect causes it to be open-circuited. The device powers up in the Test-Logic-Reset state.

Run-Test/Idle

The TAP must pass through this state before executing any test operations. The test operations controlled by the boundary control register (see Table 2) are performed while in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in these states, and the TAP will exit either of them on the next TCK cycle.

Capture-DR

The selected data register is placed in the scan path. Depending on the current instruction, data may or may not be loaded or captured by that register on the rising edge of TCK causing the TAP state to change. On the falling edge of TCK in Capture-DR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to a low level.

Shift-DR

While in this state, data is serially shifted through the selected data register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR).

Exit1-DR, Exit2-DR

These are temporary states used to end the shifting process. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-DR to Exit1-DR.

Pause-DR

The TAP can remain in this state indefinitely. The Pause-DR state provides the capability of suspending and resuming shift operations without loss of data.

Update-DR

If the current instruction calls for the latches in the selected data register to be updated with current data, the latches are updated during this, and only this, state. TDO goes to the high-impedance state on the falling edge of TCK in Update-DR.

Capture-IR

The instruction register is preloaded with a 10000001 pattern and placed in the scan path. On the falling edge of TCK in Capture-IR, TDO goes from the high-impedance state to the active state. If the TAP has not passed through the Test-Logic-Reset state since the last scan operation, TDO will enable to the level present when it was last disabled. If the TAP has passed through the Test-Logic-Reset state since the last scan operation. TDO will enable to a low level.

Shift-IR

While in this state, data is serially shifted through the instruction register from TDI to TDO on each TCK cycle. The first shift does not occur until the first TCK cycle after entering this state (i.e., no shifting occurs during the TCK cycle in which the TAP changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR).



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state diagram description (continued)

Exit1-IR. Exit2-IR

These are temporary states used to end the shifting process. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. The last shift occurs on the TCK cycle in which the TAP state changes from Shift-IR to Exit1-IR.

Pause-IR

The TAP can remain in this state indefinitely. The Pause-IR state provides the capability of suspending and resuming shift operations without loss of data.

Update-IR

The latches shadowing the instruction register are updated with the new instruction. TDO goes to the high-impedance state on the falling edge of TCK in Update-IR.

instruction register description

Serial test information is conveyed by means of a 4-wire test bus. Commands, data, and control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals for the bus and generate the appropriate on-chip control signals for the test structures in the device. The TAP monitors two signals from the bus, TCK and TMS. Figure 1 shows the TAP state diagram. The functional block diagram illustrates the IEEE Standard 1149.1 4-wire test bus and boundary scan architecture, and the relationship between the TAP, the test bus, and the boundary scan test elements.

Data is captured on the rising edge of TCK. Outputs change after the falling edge of TCK.

As shown in the functional block diagram, the 'BCT8374 contains an eight-bit instruction register and three data registers: the 18-bit boundary scan register, the two-bit boundary control register, and the one-bit bypass register. Any register can be thought of as a serial shift register with a shadow latch on each bit. Latches may be loaded during the Update-DR and Update-IR TAP states.

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the test operation to be performed, the state of the functional inputs and outputs (whether or not the device will perform its normal function during the test operation), which of the three data registers is to be selected for inclusion in the scan path during the next data register scan operation, and the source of the data preloaded in the data register during the Capture-DR state. Table 1 lists the instructions supported by the 'BCT8374. Any SCOPE™ instructions not supported default to BYPASS.

The IR is loaded during the Capture-IR state with the value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path.

The instruction register order of scan is shown in Figure 2.

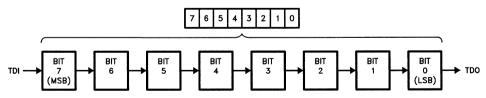


FIGURE 2. INSTRUCTION REGISTER ORDER OF SCAN



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data register descriptions

boundary scan register

The boundary scan register (BSR) contains 18 bits, one for each functional input and output on the device. The BSR is used to store test data that is to be applied internally and/or externally to the device, and to capture and store data that is applied to the functional inputs and outputs of the device. The origination of the value loaded in the BSR during the Capture-DR state is determined by the current instruction.

The boundary scan register order of scan is shown in Figure 3.

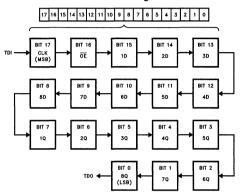


FIGURE 3. BOUNDARY SCAN REGISTER ORDER OF SCAN

boundary control register

The boundary control register (BCR) contains two bits and is used to implement additional test operations not included in the SCOPE™ instruction set, including pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) operations. The BCR retains its current value during the Capture-DR state. The BCR resets to the PSA operation.

The boundary control register order of scan is shown in Figure 4.

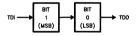


FIGURE 4. BOUNDARY CONTROL REGISTER ORDER OF SCAN

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation. The bypass register is loaded with a logic 0 during the Capture-DR state.

The bypass register order of scan is shown in Figure 5.



FIGURE 5. BYPASS REGISTER ORDER OF SCAN



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TABLE 1. INSTRUCTION REGISTER OPCODES

BINARY CODE†‡ BIT 7 → BIT 0	SCOPE OPCODE	DESCRIPTION	SELECTED	MODE
MSB → LSB	00012010022	2233	DATA REGISTER	
X0000000	EXTEST	Boundary Scan	Boundary Scan	Test
X0000001	BYPASS§	Bypass Scan	Bypass	Normal
X0000010	SAMPLE	Sample Boundary	Boundary Scan	Normal
X0000011	INTEST	Boundary Scan	Boundary Scan	Test
X0000100	BYPASS§	Bypass Scan	Bypass	Normal
X0000101	BYPASS§	Bypass Scan	Bypass	Normal
X0000110	TRIBYP	Control Boundary to High-Impedance	Bypass	Modified Test
X0000111	SETBYP	Control Boundary to 1/0	Bypass	Test
X0001000	BYPASS§	Bypass Scan	Bypass	Normal
X0001001	RUNT	Boundary Run Test	Bypass	Test
X0001010	READBN	Boundary Read	Boundary Scan	Normal
X0001011	READBT	Boundary Read	Boundary Scan	Test
X0001100	CELLTST	Boundary Self-test	Boundary Scan	Normal
X0001101	TOPHIP	Boundary Toggle Outputs	Bypass	Test
X0001110	SCANCN	Boundary Control Register Scan	Boundary Control	Normal
X0001111	SCANCT	Boundary Control Register Scan	Boundary Control	Test
ALL OTHER	BYPASS	Bypass Scan	Bypass	Normal

[†] The SCOPE instruction set specifies even parity in the eight-bit instruction. This feature is not implemented in the 'BCT8374.

instruction register opcode descriptions

The 'BCT8374 runs test instructions based on the value scanned into the instruction register. The test functions are defined as follows:

boundary scan

This instruction simultaneously executes the IEEE Standard 1149.1 EXTEST and INTEST instructions. The boundary scan register is selected in the scan path. Data appearing at the device inputs and outputs is captured. Data previously loaded into the boundary scan register is applied to the device inputs and through the device outputs.

bypass scan

Conforms to the IEEE Standard 1149.1 BYPASS instruction. The one-bit bypass register is selected in the scan path. A logic 0 is loaded in the bypass register. The device operates in the normal mode.

sample boundary

Conforms to the IEEE Standard 1149.1 SAMPLE instruction. Data appearing at the device inputs and outputs is sampled without affecting normal device operation. The boundary scan register is selected in the scan path.

control boundary to high-impedance

The device outputs are placed in the high-impedance state. The bypass register is selected in the scan path. Device inputs remain operational, and the internal logic function will be performed.

control boundary to 1/0

The data in the boundary scan register is applied to the functional inputs and through the device outputs. The bypass register is selected in the scan path.



[‡] X = Don't care.

[§] A SCOPE opcode exists but is not supported in the 'BCT8374.

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instruction register opcode descriptions (continued)

boundary run test

A test operation is run as decoded by the boundary control register. The desired test must be preloaded in the boundary control register, and the TAP placed in the Run-Test/Idle state. The four test operations decoded by the boundary control register are:

- parallel signature analysis (PSA)

Data appearing on the functional data inputs is compressed into sixteen bits. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 6 shows the algorithm through which the signature is generated.

- pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated at the functional outputs. An initial seed value should be scanned into the boundary scan register prior to performing this operation. Figure 7 shows the algorithm through which the patterns are generated. Note that a seed value of all zeroes will not produce additional patterns.

- simultaneous PSA and PRPG

Both PSA and PRPG operations are performed as shown in Figure 8.

- sample inputs/toggle outputs

Data appearing at the functional inputs is sampled on each TCK rising edge, and the functional outputs are toggled on each TCK falling edge.

boundary read

The boundary scan register is selected in the scan path. No load operation is performed prior to shifting. This instruction is useful for inspecting data after a PSA operation.

boundary control register scan

The two-bit boundary control register is placed in the scan path. This register must be loaded prior to executing a boundary run test operation.

boundary self-test

The boundary scan register is selected in the scan path. This operation tests the logic in the boundary scan cells by loading the inverse of the current value of the cells. By loading a known value in the boundary scan register, executing CELLTST, and inspecting the resulting data through a scan operation, the integrity of the boundary scan register can be verified.

boundary toggle outputs

Functional outputs are toggled on each TCK falling edge. Data appearing on the device's functional inputs is not captured.

tap bits for PSA and PRPG

The BCR opcodes are shown in Table 2. The use of these tap bits and the algorithms used for 8- and 16-bit PSA and PRPG operations are shown in Figures 6 through 8. The two control inputs, CLK and \overline{OE} , are ignored during these operations.

TABLE 2. BOUNDARY CONTROL REGISTER OPCODES

BINARY CODE BIT 1 → BIT 0 MSB → LSB	DESCRIPTION
00	Sample inputs/toggle outputs
01	PRPG/16-bit mode
10	PSA/16-bit mode
11	Simultaneous PRPG and PSA/8-bit mode



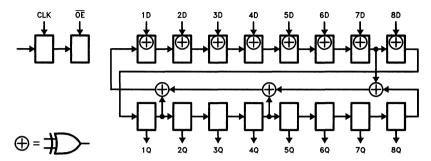


FIGURE 6. 16-BIT PSA CONFIGURATION

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

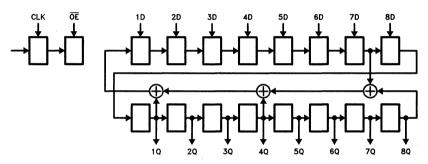


FIGURE 7. 16-BIT PRPG CONFIGURATION

A PRPG operation from the 8 data outputs proceeds while the inputs are ignored.

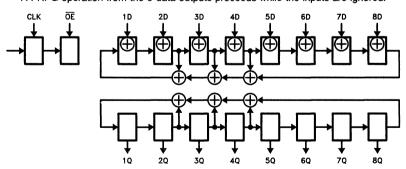


FIGURE 8. 8-BIT PSA AND PRPG CONFIGURATION

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.



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timing description

All test operations of the 'BCT8374 are synchronous to TCK. Data on the TDI, TMS, and functional inputs is captured on the rising edge of TCK. Data appears on the TDO and functional output pins on the falling edge of TCK.

The 'BCT8374 is advanced through its state diagram (see Figure 1) by changing the value of TMS and applying a clock pulse to TCK. A simple timing example is shown in Figure 9. In this example, the device begins in the Test-Logic-Reset state and is loaded with an instruction to select the bypass register in the scan path. The binary logic value 101 is shifted through the bypass register from TDI to TDO, and the device is returned to the Test-Logic-Reset state. Table 3 explains the function of the test circuitry during each TCK cycle.

TABLE 3. EXPLANATION OF TIMING EXAMPLE

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION/COMMENT
1	Test-Logic-Reset	Recycle on reset state.
2	Run-Test/Idle	Begin advancing towards desired state.
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	IR loads with 10000001; TDO becomes active after falling edge of TCK.
6	Shift-IR	Ready to shift in instruction; TDI must be active before next clock.
7-13	Shift-IR	A BYPASS instruction (11111111) is serially loaded into the IR.
14	Exit1-IR	Note that TMS goes high prior to TCK #14. The last bit of the instruction is shifted in as the TAP
14	EXILI-IN	advances from Shift-IR to Exit1-IR.
15	Hadata ID	The IR is updated with the new instruction. TDO goes inactive (high-impedance) on the falling edge of
15	Update-IR	TCK #15.
16	Select-DR-Scan	
17	Capture-DR	The bypass register loads with a logic 0; TDO becomes active.
18	Shift-DR	The bypass register is now in the scan path. Data will shift from TDI to TDO.
19-20	Shift-DR	The binary value '101' is shifted from TDI to TDO through the bypass register. Note that the last value
19-20	Shiit-DH	shifted in (a logic 1) remains in the bypass register and is not shifted to the next test element.
21	Exit1-DR	
22	Update-DR	
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed.

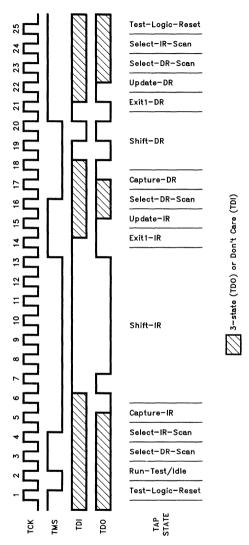


FIGURE 9. TIMING EXAMPLE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	0.5 V to 7 V
Input voltage range, V _I	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state: SN54BCT8374 (TDO)	40 mA
SN54BCT8374 (Any Q)	96 mA
SN74BCT8374 (TDO)	48 mA
SN74BCT8374 (Any Q)	128 mA
Operating free-air temperature range: SN54BCT8374	-55°C to 125°C
SN74BCT8374	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN	54BCT8	374	SN7	74BCT83	374	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.5	5	5.5	٧
ViH	High-level input voltage		2		120	2			٧
VIHH	Double high-level input voltage	TMS	10		12	10		12	٧
VIL	Low-level input voltage			AQ.	0.8			0.8	٧
ΊK	Input clamp current			1	-18			-18	mA
• -	I Pate to a decide to the second	TDO	A	2	-3			-3	
ЮН	High-level output current	Any Q	40		-12			- 15	mA
		TDO	Q.		20			24	
IOL	Low-level output current	Any Y			48			64	mA
TA	Operating free-air temperature		-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8374			SN74BCT8374				
				MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
V _{IK} V _{CC} = 4.5		$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{ mA}$				-1.2			-1.2	٧
		V _{CC} = 4.75 V		IOH = −3 mA	2.7	3.4		2.7	3.4		
	A O			IOH = -3 mA	2.4	3.4		2.4	3.4		
	Any Q	$V_{CC} = 4.5 V$		IOH = -12 mA	2	3.2					٧
VOH				IOH = -15 mA				2	3.1		٧
	TDO	V 45V		IOH = -1 mA	2.5	3.4		2.5	3.4		
	100	$V_{CC} = 4.5 V$		IOH = -3 mA	2.4	3.3		2.4	3.3		
	A O	V 45V		IOL = 48 mA		0.38	0.55				
	Any Q	$V_{CC} = 4.5 V$		IOL = 64 mA					0.42	0.55	v
VOL	TDO	V _{CC} = 4.5 V		IOL = 20 mA		0.3	0,5				٧
TDO		VCC = 4.5 V		IOL = 24 mA			-35		0.35	0.5	
lj		$V_{CC} = 5.5 V,$	$V_{ } = 5.5 V$			-68	0.1			0.1	mA
lіН		$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$		-1	A	-100	-1		-100	μΑ
Інн	TMS	$V_{CC} = 5.5 V,$	$V_I = 10 V$		100		1			1	mA
IIL		$V_{CC} = 5.5 V,$	$V_I = 0.5 V$				-200			-200	μΑ
lozu	Any Q	$V_{CC} = 5.5 V$	$V_0 = 2.7 V$		40		50			50	^
lozh	TDO	$V_{CC} = 5.5 V,$	$V_0 = 2.7 V$		-1		- 100	-1		-100	μΑ
lon	Any Q	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-50			-50	^
IOZL	TDO	$V_{CC} = 5.5 V,$	$V_0 = 0.5 V$				-200			-200	μΑ
los‡		$V_{CC} = 5.5 V,$	$V_O = 0$		-100		- 225	- 100		-225	mA
				Outputs high		3.5	7		3.5	7	
Icc	ì	$V_{CC} = 5.5 V$, Outputs op	Outputs open	Outputs low		35	52		35	52	mA
				Outputs disabled		1.5	3		1.5	3	
Ci			$V_1 = 2.5 V or 0$			10			10		pF
Co		$V_{CC} = 5 V$	$V_O = 2.5 \text{ V or}$	0.5 V		14			14		рF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

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timing requirements

			l l	V _{CC} = 5 V, T _A = 25°C		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $T_{A} = \text{MIN to MAX}^{\dagger}$				LINUT
			,	BCT837	4	'54BC	T8374	'74BCT8374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	TCK	0		20	0	20	0	20	MHz
		CLK	0		70	. 0	70	0	70	IVITIZ
		TCK high or low	25			25		25		
tw	Pulse duration	CLK high or low	5			5		5		ns
		TMS reset high	50			50	Air.	50		
		Data before CLK↑	3			3	34	3		
		TMS before TCK ↑	12			12	il.	12		
tsu	Setup time	TDI before TCK ↑	6			6	Q.,	6		ns
		Any D before TCK ↑	6			6		6		
		OE before TCK ↑	6			6		6		
		Data after CLK ↓	2			2		2		
		TMS after TCK ↑	0			0		0		
th	Hold time	TDI after TCK ↑	4.5			4.5		4.5		ns
		Any D after TCK ↑	4.5			4.5		4.5		
		ŌE after TCK↑	4.5			4.5		4.5		
t _{pu}		Wait time, power up to TCK↑	100			100		100		ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TI0223-D3641, JUNE 1990

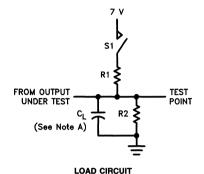
switching characteristics (see Figure 10)

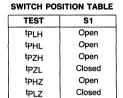
			1	C = 5'		٧c	C = 4.5 CL =		٧,	
		,	1	= 500		$R1 = 500 \Omega$				
PARAMETER	FROM	то	R2	= 500	Ω,		R2 =	500 Ω,		UNIT
	(INPUT)	(OUTPUT)	Т,	4 = 25°	c	T,	4 = MIN	to MAX	(†	
				3CT8374			T8374	'74BC		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax	TCK		20			20		20		MHz
₹PLH	OLIK	AO	3	7.1	10	3	12.5	3	11.5	
tPHL	CLK	Any Q	3	7.4	10.5	3	12.5	3	12	ns
tPLH	TOV I	AO	3.9	10.9	15.7	3.9	21.5	3.9	19.8	
tPHL	TCK↓	Any Q	3.9	10.8	15.3	3.9	21.5	3.9	19.5	ns
tPLH .	TOV	TD0	3.2	8.5	12.3	3.2	16.8	3.2	15.4	
t _{PHL}	TCK↓	TDO	3.2	8.3	12	3.2	16.3	3.2	15	ns
t _{PLH}	TOV A	40	6.2	13.9	21	6.2	29	6.2	25	
[†] PHL	TCK↑	Any Q	6.6	15	22	6.6	29.6	6.6	26	ns
tpZH	ŌĒ	A==: 0	2.4	6.5	9	2.4	11	2.4	10.6	
^t PZL	OE	Any Q	3	7.8	10.9	3	12.9	3	12	ns
[†] PHZ	ŌĒ	A O	2.5	7.1	9.5	2.5	10.9	2.5	10	
^t PLZ	OE	Any Q	2.4	6.4	9	2.4	10.5	2.4	9.5	ns
tPZH	тск↓	Q	4.7	11.7	16.7	4.7	23.1	4.7	21.1	
^t PZL	ICK	l Q	5.5	13.6	19.7	₿5.5	24.4	5.5	22.9	ns
tPHZ	тск↓	A O	3.4	9	13.2	3.4	18.7	3.4	17.3	
^t PLZ	I CK \$	Any Q	3.6	10	14.6	3.6	19.5	3.6	17.8	ns
^t PZH	тск↓	TDO	2.4	6.2	9	2.4	11.3	2.4	10.8	ns
^t PZL	101.1	100	3.2	7.6	10.6	3.2	13.2	3.2	12.6	115
^t PHZ	тск↓	TDO	2.6	7.1	10.2	2.6	13	2.6	12.8	ns
tPLZ	ION	100	2.2	5.9	8.7	2.2	12.7	2.2	11.6	115

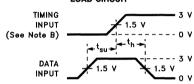
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

D3641, JUNE 1990-TI0223

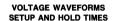
PARAMETER MEASUREMENT INFORMATION

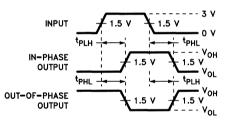




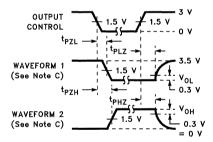


HIGH-LEVEL PULSE 1.5 V 1.5 V LOW-LEVEL PULSE 1.5 V 1.5 V





VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. CL includes probe and jig capacitance.

- B. Input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \, \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 10. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

General Information
ACL LSI Products 2
ACL Widebus™ Products 3
BTL Transceiver Products 4
Bus-Termination Array Products 5
Clock Driver Products 6
ECL/TTL Translator Products 7
FIFO Products
Low-Impedance Line Driver Products 9
Memory Driver Products
SCOPE™ Testability Products
64BCT Series Products 12
Mechanical Data

SN64BCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

TI0280-D3595, JULY 1990

•	State-of-the-Art	BICMOS	Design
	Significantly Red	duces IC	CZ

- High-Impedance State During Power-Up and Power-Down
- 3-State Outputs Drive Bus Lines or Buffer **Memory Address Registers**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs

description

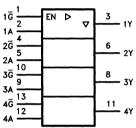
These bus buffers feature independent line drivers with three-state outputs. Each output is disabled when the associated G is high.

SN64BCT125 is characterized operation from -40°C to 85°C and 0°C to 70°C.

D or N PACKAGE (TOP VIEW)

1 G 🗆	1	U14 □ V _{CC}
1A [2	13 4G
1Y [3	12 4A
2Ğ 🗌	4	11 4Y
2A 🗌	5	10∏ 3Ğ
2Y 🗌	6	9 🗍 3A
GND [7	8 3Y

logic symbol†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INP	UTS	OUTPUT
Ğ	Α	Y
L	Н	Н
L	L	L
н	Х	Z

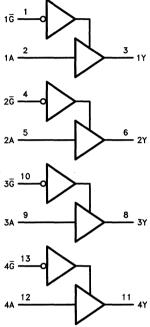
H = high level,

L = low level,



D3595, JULY 1990—TI0280

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	. −0.5 V to 7 V
Input voltage range, V _I (see Note 1)	. −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN64BCT125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

TI0280--- D3595, JULY 1990

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
lik	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	MIN	TYP	MAX	UNIT	
VIK	V _{CC} = 4.5 V, I _I = -18 mA				-1.2	٧
\/-··	V 45V	IOH = -3 mA	2.4	3.3		٧
VOH	V _{CC} = 4.5 V	IOH = −15 mA	2	3.1		٧
VOL	V _{CC} = 4.5V	IOH = 64 mA		0.42	0.55	٧
IOZH	$V_{CC} = 0 \text{ V to } 5.5 \text{ V}, V_{O} = 2.7 \text{ V}$				50	mA
IOZL	V _{CC} = 0 V to 5.5 V, V _O = 0.5 V				-50	μΑ
lo-	\overline{G} at 0.8 V, $V_{CC} = 0$ to 1.3 V (power up)				±50	
loz	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$	V _{CC} = 1.3 V to 0 (power down)			±50	μΑ
lį .	V _{CC} = 0, V _I = 7 V				0.1	mA
۱н	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$				25	μΑ
ΙΙL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$				-20	mA
los‡	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$		-100		-225	mA
ICCL	V _{CC} = 5.5 V			46	49	mA
ССН	V _{CC} = 5.5 V			19	31	mA
Iccz	V _{CC} = 5.5 V			6	12	mA
Ci	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V			4		pF
Co	V _{CC} = 5 V, V _O = 2.5 V or 0.5 V			9		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_{L} = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$ $T_{A} = 25^{\circ}C$		TA =	V _{CC} = 4.5 v C _L = 5 R1 = 5 R2 = 5 - 40°C to 85°C	i0 pF, i00 Ω, i00 Ω	0°C to 70°C	UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	A		1.6	3.5	5.2	1.6	6	1.6	5.7	
tPHL	Α	Y	2.7	5	6.9	2.7	8	2.7	7.7	ns
tPZH	G	Υ	3.4	6.7	9	3.4	11.1	3.4	10.3	
tPZL	G	Y	5	8.2	10.4	5	12.8	5	11.7	ns
tPHZ	<u></u>	V	3	5.8	7.4	3	9.4	3	8.9	
tPLZ	G	G Y		5.5	7.3	2.8	9.9	2.8	8.6	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS051—TI0299—D3622, JULY 1990—REVISED OCTOBER 1990

D or N PACKAGE

(TOP VIEW)

•	State-of-the-Art BiCMOS Design
	Significantly Reduces ICCZ

- High-Impedance State During Power-Up and Power-Down
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs

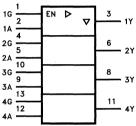
logic symbol†

1G	14 13 12 11 10 9	V _{CC} 4G 4A 4Y 3G 3A
2Y	9 8	3A 3Y

description

These bus buffers feature independent line drivers with three-state outputs. Each output is disabled when the associated G is high.

The SN64BCT126 is characterized for operation from -40°C to 85°C and 0°C to 70°C .



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

	INP	UTS	OUTPUT
i	G	Α	Y
	Н	Н	Н
	Н	L	L
	L	Х	Z

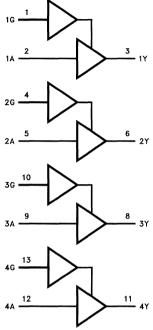
H = high level,L = low level,

X = irrelevant

12-6



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.



SN64BCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

D3622, JULY 1990-REVISED OCTOBER 1990-TI0299-SCBS051

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
lк	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	ç

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	MIN	TYP	MAX	UNIT	
VIK	$V_{CC} = 4.5 \text{ V, I}_{I} = -18 \text{ mA}$				-1.2	٧
1/	V 45V	IOH = -3 mA	2.4	3.3		.,
VOH	V _{CC} = 4.5 V	IOH = -15 mA	2	3.1		٧
VOL	V _{CC} = 4.5V	IOH = 64 mA		0.42	0.55	٧
lozh	V _{CC} = 0 V to 5.5 V, V _O = 2.7 V				50	mA
lozl	VCC = 0 V to 5.5 V, VO = 0.5 V				-50	μΑ
1	G at 0.8 V,	V _{CC} = 0 to 1.3 V (power up)			±50	
loz	V _O = 2.7 V or 0.5 V			±50	μΑ	
lı	V _{CC} = 0, V _I = 7 V				0.1	mA
lін	V _{CC} = 5.5 V, V _I = 2.7 V				25	μΑ
IIL	$V_{CC} = 5.5 \text{ V}, V_{I} = 0.5 \text{ V}$				-20	mA
los‡	$V_{CC} = 5.5 \text{ V}, V_{O} = 0$		-100		- 225	mA
ICCL	V _{CC} = 5.5 V			35	51	mA
ICCH	V _{CC} = 5.5 V			21	33	mA
Iccz	V _{CC} = 5.5 V			5	8	mA
Ci	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V			4		pF
Co	V _{CC} = 5 V, V _O = 2.5 V or 0.5 V			9		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega$			V _{CC} = 4.5 V C _L = 5 R1 = 5 R2 = 8	60 pF, 00 Ω,		UNIT		
				TA = 25°C		T _A = -40°C to 85°C		T _A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α		1.5	3.6	4.9	1.5	5.6	1.5	5.4	
tPHL		Y	2.7	5.3	6.9	2.7	7.7	2.7	7.4	ns
tPZH	G		2.6	4.8	6.4	2.6	7.2	2.6	10.7	
tPZL	G	G Y	3.7	6.4	8.3	3.7	10.5	3.7	10	ns
tPHZ	G	V	3.2	6.6	8.2	3.2	9.6	3.2	9.1	
tPLZ		Y	3.4	6.5	8	3.4	12.3	3.4	10.7	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS049---TI0206---D3499, MAY 1990

- State-of-the-Art BiCMOS Design
 Substantially Reduces Standby Current
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include "Small Outline"
 Packages, and Standard Plastic 300-mil DIPs

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT241 and 'BCT244, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\bf G}$ (active-low output control) inputs, and complementary $\bf G$ and $\overline{\bf G}$ inputs.

The SN64BCT240 is characterized for operation from -40°C to 85°C and 0°C to $70^{\circ}\text{C}.$

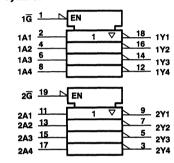
FUNCTION TABLE (each buffer)

INP	UTS	OUTPUT
Ğ	Α	Υ
L	Н	L
L	L	Н
Н	X	z

DW OR N PACKAGE (TOP VIEW)

1 <u>G</u> [70	20] v _{cc}
1A1 [2		2 <u>G</u>
	3	18] 1Y1
_	4	17] 2A4
2Y3 🛛	5	16] 1Y2
1A3 [6	15	2A3
2Y2 🛛	7	14] 1Y3
1A4 []	8] 2A2
2Y1 []	9	12] 1Y4
GND [10	11] 2A1

logic symbol†



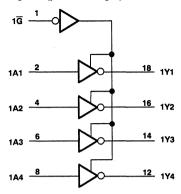
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

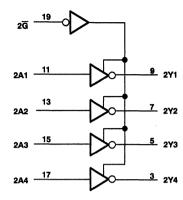


SN64BCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3499, MAY 1990-TI0206-SCBS049

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	−0.5 V to 7 V
Input voltage range (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	V
lik	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
IOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

SN64BCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS049-TI0206-D3499, MAY 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	$I_{\parallel} = -18 \text{ mA}$				-1.2	٧
	V 45V		IOH = -3 mA	2.4	3.3		
Voн	V _{CC} = 4.5 V		IOH = -15 mA	2	3.1		V
	$V_{CC} = 4.75 V$		IOH = -3 mA	2.7			
VOL	V _{CC} = 4.5 V		IOH = 64 mA		0.42	0.55	٧
lozh	$V_{CC} = 0 V \text{ to } 5.5 V,$	$V_0 = 2.7 V$				50	μΑ
IOZL	$V_{CC} = 0 V \text{ to } 5.5 V,$	$V_0 = 0.5 V$				-50	μΑ
10-	G at 0.8 V,	VO = 2.7 V or 0.5 V	V _{CC} = 0V to 2.3 V (power up)			±50	μΑ
loz	Galu.ov,	VO - 2.7 V OF 0.5 V	V _{CC} = 1.8 V to 0 V (power down)			±50	μΑ
łį	$V_{CC} = 0 V \text{ to } 5.5 V,$	V _I = 5.5 V				0.1	mA
lн	$V_{CC} = 5.5 V,$	$V_1 = 2.7 V$				20	μΑ
IIL	$V_{CC} = 5.5 V,$	$V_{ } = 0.5 V$				-1	mA
los‡	$V_{CC} = 5.5 V,$	VO = 0V		-100		- 225	μΑ
ICCL	V _{CC} = 5.5 V				19	31	mA
ICCH	V _{CC} = 5.5 V				46	71	mA
Iccz	$V_{CC} = 5.5 V$				6	9	mA
Ci	$V_{CC} = 5.5 V,$	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			6		pF
Co	VCC = 5.5 V	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$			11		pF

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V,$ $C_{L} = 50 pF,$ $R1 = 500 Ω,$ $R2 = 500 Ω$ $T_{A} = 25^{\circ}C$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega$ $T_{A} = -40^{\circ}\text{C to } 85^{\circ}\text{C} T_{A} = 0^{\circ}\text{C to } 70^{\circ}\text{C}$				UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
tPLH		_	0.5	4.8	0.5	6.4	0.5	5.6		
tPHL	A	, r	0.4	3.5	0.4	4.5	0.4	4	ns	
tPZH	G	V	1	7.9	1	9.2	1	8.8		
tPZL	<u> </u>	Y	Y	1	9.4	1	10.8	1	10.5	ns
tPHZ	G	Y	1	6.8	1	8.5	1	8.1		
tPLZ	_ G	Y	1	8.1	1	10.6	1	9.5	ns	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS046-TI0207-D3428, FEBRUARY 1990

- State-of-the-Art BiCMOS Design
 Substantially Reduces Standby Current
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include "Small Outline"
 Packages and Standard Plastic 300-mil DIPs

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{\mathbf{G}}$ (active-low output-enable) inputs, and complementary \mathbf{G} and $\overline{\mathbf{G}}$ inputs.

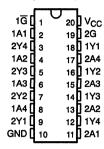
The SN64BCT241 is characterized for operation from -40°C to 85°C and 0°C to 70°C.

FUNCTION TABLES

INPU	JTS	OUTPUT	
1Ğ	1A	1Y	
L	Н	Н	
L	L	L	
н	X	z	

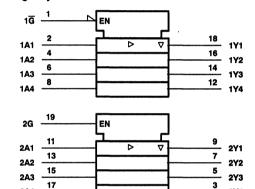
٢	INP	UTS	OUTPUT
	2G	2A	2Y
Γ	Н	Н	Н
	Н	L	L
١	L	Х	z

DW OR N PACKAGE (TOP VIEW)



logic symbol†

2A4



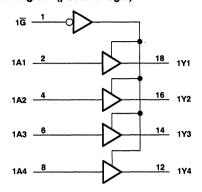
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

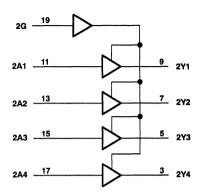
2Y4



SCBS046-TI0207-D3428, FEBRUARY 1990

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	-0.5 V to 7 V
Input voltage range	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5~V to $5.5~V$
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ΙK	Input clamp current			- 18	mA
ЮН	High-level output current			- 15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

SN64BCT241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3428, FEBRUARY 1990-TI0207-SCBS046

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	l _l = -18 mA				-1.2	٧
			IOH = -3 mA	2.4	3.3		
Voн	V _{CC} = 4.5 V		IOH = -15 mA	2	3.1		٧
	V _{CC} = 4.75 V		IOH = −3 mA	2.7			
VOL	V _{CC} = 4.5 V		IOH = 64 mA		0.42	0.55	V
lozh	$V_{CC} = 0 V \text{ to } 5.5 V$	V _O = 2.7 V				50	mA
lozL	$V_{CC} = 0 V \text{ to 5.5 V},$	$V_0 = 0.5 V$				-50	μΑ
	<u> </u>		V _{CC} = 0 V to 2.3 V (power up)			± 50	
loz	G at 0.8 V,	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$	V _{CC} = 1.8 V to 0 V (power down)			±50	μΑ
l _l	$V_{CC} = 0 V \text{ to } 5.5 V,$	V _I = 5.5 V				0.1	mA
ΊΗ	$V_{CC} = 5.5 V,$	V _I = 2.7 V				20	μΑ
, G or G	V 55V					-1	mA
IL Any A	$V_{CC} = 5.5 V$	$V_I = 0.5 V$				-1.6	mA
los‡	$V_{CC} = 5.5 V,$	VO = 0		-100		- 225	mA
ICCL	V _{CC} = 5.5 V				23	43	mA
ГССН	V _{CC} = 5.5 V				53	85	mA
Iccz	V _{CC} = 5.5 V				4	10	mA
Ci	$V_{CC} = 5 V$,	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			6		pF
Co	$V_{CC} = 5 V$,	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			11		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_L = 50 pF$, R1 = 500 Ω, R2 = 500 Ω, $T_A = 25^{\circ}C$		$\begin{array}{c} \text{V}_{\text{CC}} = 4.5 \text{V to } 5.5 \text{V}, \\ \text{C}_{\text{L}} = 50 \text{pF} \\ \text{R1} = 500 \Omega, \\ \text{R2} = 500 \Omega, \\ \text{T}_{\text{A}} = \text{MIN TO MAX}^{\dagger} \end{array}$				UNIT
			'BC	'BCT241		40°C to 85°C	$T_A = 0$	0°C to 70°C	
			MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	Υ	0.5	4.5	0.5	5.2	0.5	4.9	
tPHL	^	r	1	5.4	1	6.3	1	5.9	ns
^t PZH	G or G	Υ	1	7.8	1	9.1	1	8.7	
tPZL	Gord	T	1	8.6	1	10	1	9.4	ns
^t PHZ	Ğ or G	Υ	1	6.8	1	8.4	1	8.1	
tPLZ	Gord	ľ	1	8.1	1	11	1	9.9	ns

Ą

^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS027-Ti0208-D3249, FEBRUARY 1989-REVISED AUGUST 1989

- 3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and Power Down
- P-N-P Inputs Reduce DC Loading
- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{\mathbb{G}}$ (active-low output control) inputs, and complementary \mathbb{G} and $\overline{\mathbb{G}}$ inputs.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT244 is characterized for operation from -40° C to 85°C.

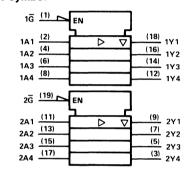
FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
1G, 2G	Α	Υ
Н	Х	Z
L	L	L
L	н	н

DW OR N PACKAGE (TOP VIEW)

1G	ī	U20	۷cc
1A1	2	19	2G
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1 Y 4
GND	10	11	2A1

logic symbol†

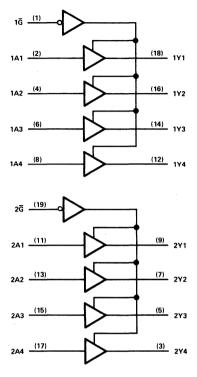


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



D3249. FEBRUARY 1989—REVISED AUGUST 1989—TI0208—SCBS027

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	. −0.5 V to 7 V
Input voltage	0.5 V to 7 V
Voltage applied to any output in the disbled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN64BCT244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS027--TI0208--D3249, FEBRUARY 1989--REVISED AUGUST 1989

recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
ΊΚ	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
loL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$		$I_{\parallel} = -18 \text{ mA}$			-1.2	V
Vau	VCC = 4.5 V		IOH = -3 mA	2.4	3.3		v
VOH	VCC - 4.5 V		$I_{OH} = -15 \text{mA}$	2	3.1		V
VOL	V _{CC} = 4.5 V		IOL = 64 mA		0.42	0.55	٧
lį	$V_{CC} = 5.5 V,$				0.1	mA	
ΙΗ	$V_{CC} = 5.5 V,$				20	μΑ	
ŊL	V _{CC} = 5.5 V,				-1	mA	
^I OZH	$V_{CC} = 0 V \text{ to } 5.5 V,$				50	μΑ	
lozl	$V_{CC} = 0 V \text{ to } 5.5 V,$		V _O = 0.5 V			-50	μΑ
lo=	G at 0.8 V,	V _{CC} = 0 V to	2.3 V (power up)			±50	
loz	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$	$V_{CC} = 1.8 V$	V _{CC} = 1.8 V to 0 V (power down)			±50	μΑ
los‡	$V_{CC} = 5.5 V,$		$V_O = 0$	-100		-225	mA
Іссн			Outputs high		23	40	mA
ICCL	V _{CC} = 5.5 V		Outputs low		53	80	mA
lccs			Outputs disabled		4	10	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$		C _L = R1 = R2 =	5 V to 5.5 V, 50 pF, 500 Ω , 500 Ω , N TO MAX§	UNIT	
			MIN.	'BCT244 MIN TYP MAX		SN64BCT244 MIN MAX]
tPLH			1.2	2.5	4.4	0.9	5.3	
tPHL	Α Α	Y	1.7	3.2	5	1.4	6	ns
tPZH	G	V	2	5.7	7.8	2	9	
^t PZL	1 6	Y	2	5.9	8.1	2	9.4	ns
^t PHZ	G	Y	2	5.4	6.7	2	8	
^t PLZ	1 6	Y	2	6.1	7.6	2	9.8	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{*} Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS040-TI0209-D3250, JANUARY 1990

 BiCMOS Design Substantially Reduces Standby Current

- 3-State True Outputs Drive Bus Lines Directly
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal bus transceivers are designed for asynchronous communication between data buses. Implementing the control function minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\overline{G}) can disable the device so that the buses are effectively isolated.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

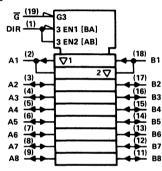
The SN64BCT245 is characterized for operation from -40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	н	A data to B bus
н	×	Isolation

DW OR N PACKAGE (TOP VIEW) U20 VCC A1 ∏2 19∏ G A2 🛛 3 18 B1 ΑЗΠ 17 B2 16 B3 A4 ∏5 А5 ∏6 15 B4 A6 □7 14 B5 13 B6 A7 [12 B7 A8 ∏9 11 B8 GND 110

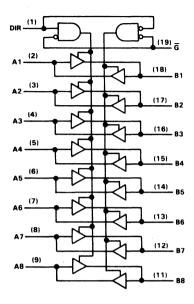
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cumply veltage range Van	051/4071/
Supply voltage range, V _{CC}	
Input voltage range (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _C C
Current into any output in the low state	128 mA
Operating free-air temperature range:	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				MIN	NOM	MAX	UNIT
Vcc	Supply Voltage			4.5	5	5.5	٧
VIH	High-level input voltage			2			٧
VIL	/IL Low-level input voltage				0.8	٧	
İIK	Input clamp current					-18	mA
1		A1-A8				-3	mA
ЮН	High-level output current	B1-B8				- 15	mA
		A1-A8				24	mA
IOL	Low-level output current	B1-B8				64	mA
TA	Operating free-air temperature			-40		85	°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN64BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D3250, JANUARY 1990-TI0209-SCBS040

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT		
VIK		$V_{CC} = 4.5 V$		I _{IK} = -18 mA			-1.2	٧
	Any A			IOH = -1 mA	2.5	3.4		
٧он	Any B	$V_{CC} = 4.5 V$		IOH = -3 mA	2.4	3.3		V
	Ally b			IOH = -15 mA	2	3.1		
٧	Any A	V _{CC} = 4.5 V		IOL = 24 mA		0.35	0.5	v
VOL	Any B	ACC = 4.9 A		IOL = 64 mA		0.42	0.55	V
	Power up	G at 0.8 V,	Voc - 0 to 2 2 V	V _O = 2.7 V			70	μΑ
I	Powerup	Galu.ov,	$V_{CC} = 0 \text{ to } 2.3 \text{ V}$	V _O = 0.5 V			-0.65	mA
loz	Power down	G at 0.8 V,	V 0 V +- 0	V _O = 2.7 V			70	μΑ
	Power down	G at 0.6 V,	$V_{CC} = 2 V \text{ to } 0$	V _O = 0.5 V		*.	-0.65	mA
lı‡	A and B	$V_{CC} = 0 V \text{ to } 5.5 V,$		V _I = 5.5 V			1	4
ıĮ₹	DIR and G	$V_{CC} = 0 V \text{ to } 5.5 V,$		V _I = 5.5 V			0.1	mA
liH‡	A and B	V _{CC} = 5.5 V,		V _I = 2.7 V			70	Δ
'IH'	DIR and G	VCC - 5.5 V,		V - 2.7 V			20	μΑ
i	A and B	V _{CC} = 5.5 V,		V _I = 0.5 V			-0.65	4
ΊL	DIR and G	ACC = 2.2 A'		VI = 0.5 V	-		-1.2	mA
16	Any A	V 55V		V 0	-60		- 150	A
los	Any B	$V_{CC} = 5.5 V$,		$V_O = 0$	-100		-225	mA
ССН		$V_{CC} = 5.5 V,$		See Note 2		36	57	
ICCL		$V_{CC} = 5.5 V,$		See Note 2		57	90	mA
ICCZ		V _{CC} = 5.5 V			-	10	15	
Cin	G and DIR					7		
CIO	A to B	$V_{CC} = 5 V$,		$V_{\parallel} = 2.5 V \text{ or } 0.5 V$		9		pF
CIO	B to A			•		12		

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = R1 =	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$			
			T _A =	25°C	$T_A = 40^\circ$	C to 85°C	TA = 0°	C to 70°C	
	Į.		MIN	MAX	MIN	MAX	MIN	MAX	
^t PLH	A B	D A	1	6	1	7.2	1	7	
tPHL	A or B	B or A	1.5	6.6	1.5	7.6	1.5	7	ns
tPZH	G	4 B	1.5	9.4	1.5	11.2	1.5	10.9	
^t PZL] G	A or B	1.5	10.2	1.5	11.8	1.5	11.6	ns
tPHZ	- <u>G</u>	A D	1.5	8.3	1.5	9.7	1.5	9.3	
tPLZ	- G	A or B	1.5	7.8	1.5	9.6	1.5	9.1	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: ICCH and ICCL are measured in the A to B mode.

SN64BCT306 DUAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS048-TI0210-D3488, MARCH 1990

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and **Power Down**
- P-N-P Inputs Reduce DC Loading
- State-of-the-Art BiCMOS Design **Substantially Reduces Standby Current**
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include "Small Outline" Packages, and Standard Plastic DIPs

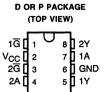
description

These dual buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

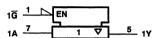
The SN64BCT306 is characterized operation from -40°C to 85°C and 0°C to 70°C.

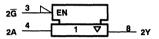
FUNCTION TABLE

OUTPUT ENABLE G	DATA INPUT A	OUTPUT Y
Н	X	Z
L	L	L
L	н	н



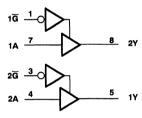
logic symbol†





† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN64BCT306 DUAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3488. MARCH 1990-TI0210-SCBS048

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, VCC	-0.5 V to 7 V
Input voltage range	_ 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			٧
VIL	Low-level input voltage			0.8	٧
ΊΚ	Input clamp current			-18	mA
ЮН	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP‡	MAX	UNIT		
VIK	$V_{CC} = 4.5 V,$, I _I = -18 mA				-1.2	٧
	1 Voo = 4 5 V		IOH = -3 mA	2.4	3.3		,
VOH			I _{OH} = -15 mA	2	3.1		٧
VOL	V _{CC} = 4.5 V	I _{OH} = 64 mA			0.42	0.55	٧
lozh	$V_{CC} = 0 V \text{ to } 5.5 V,$	$5 \text{ V}, \text{ V}_{\text{O}} = 2.7 \text{ V}$				50	mA
lozL	$V_{CC} = 0 V \text{ to } 5.5 V,$	$V_{O} = 0.5 V$				-50	μΑ
1	O-+00V		V _{CC} = 0 V to 2.3 V (power up)			±50	μΑ
loz	G at 0.8 V,	$V_{O} = 2.7 \text{V} \text{ or } 0.5 \text{V}$	V _{CC} = 1.8 V to 0 V (power down)			±50	μΑ
h	$V_{CC} = 0 V \text{ to } 5.5 V,$	V _I = 5.5 V				0.1	mA
lН	$V_{CC} = 5.5 V$,	V _I = 2.7 V				20	μΑ
ΙΙL	$V_{CC} = 5.5 V$,	V _I = 0.5 V				-1	mA
los§	$V_{CC} = 5.5 V,$	VO = 0 V		-100		-225	mA
ICCL	V _{CC} = 5.5 V				53	80	mA
ССН	VCC = 5.5 V	/ _{CC} = 5.5 V			23	40	mA
lccz	V _{CC} = 5.5 V			4	10	mA	

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT306 DUAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS048-Ti0210-D3488, MARCH 1990

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL = R1 = R2 =	500 Ω, 500 Ω 25°C		V _{CC} = 4.5 C _L = 9 R1 = 9 R2 = 9 O°C to 85°C	50 pF, 500 Ω, 500 Ω T _A = 0°	C to 70°C	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
tPLH	Α	V	1.2	4.4	0.9	5.3	0.7	5	
tPHL	^	т	1.7	5	1.4	6	1.4	5.5	ns
tPZH	G		2	7.8	2	9	2	8.7	
tPZL	G	,	2	8.1	2	9.4	2	8.9	ns
tPHZ_	G	V	2	6.7	2	8	2	7.7	200
tPLZ	G	Y	2	7.6	2	9.8	2	8.9	ns

SN64BCT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

TI0290-D3251, JUNE 1990

- 8-Latches in a Single Package
- Full Parallel Access for Loading
- State-of-the-Art BiCMOS Design Significantly Reduces ICC
- 3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

DW OR N PACKAGE (TOP VIEW)

OE [1	U 20	□v _{cc}
1Q []2	19] 8Q
1D [3	18	8D
2D []4	17] 7D
2Q []5	16] 7Q
3Q []6	15] 6Q
3D [7	14] 6D
4D []8	13] 5D
4Q []9	12] 5Q
GND [10	11	С

FUNCTION TABLE (each latch)

	INPUTS	OUTPUT	
ŌĒ	ENABLE C	D	Q
L	Н	Н	Н
L	н	L	L
L	L	Х	Q ₀
н	×	Х	Z

The eight latches of the 'BCT373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface components.

The output enable (\overline{OE}) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

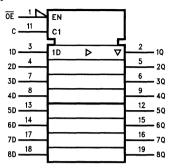
The outputs are in a high-impedance state during power up and power down when the supply voltage is less than approximately 3 V.

The SN64BCT373 is characterized for operation from -40° C to 85°C.

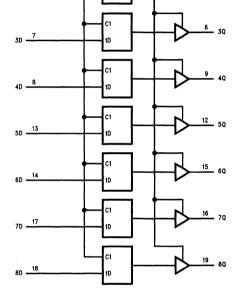
logic diagram (positive logic)

TI0290--- D3251, JUNE 1990

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	. −0.5 V to 7 V
Input voltage, (see Note 1)	0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	. −0.5 V to 7 V
Voltage applied to any output in the high state	-0.5 V to VCC
Input clamp current	30 mA
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

VCC	Supply voltage	MIN 4.5	NOM 5	MAX 5.5	AU /
VIH	High-level input voltage	2		0.0	
VIL	Low-level input voltage			0.8	1
IIK	Input clamp current			-18	١
ЮН	High-level output current			-15	m
IOL	Low-level output current			64	m
TA	Operating free-air temperature	-40		85	۰

electrical characteristics over recommended operating free-air temperature range (unless

PARAMETER	TEST CONDITIONS				TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	I _I = -18 mA	THE STATE OF THE S			-1.2	٧
	V 45V		IOH = -3 mA	2.4	3.3		٧
VOH	$V_{CC} = 4.5 V$		IOH = -15 mA	2	3.1		٧
VOL	V _{CC} = 4.5 V		$I_{OL} = 64 \text{ mA}$			0.55	٧
Vozh	V _{CC} = 0 to 5.5 V,	V _O = 2.7 V				50	μΑ
VozL	$V_{CC} = 0 \text{ to } 5.5 \text{ V},$	V _O = 0.5 V				-50	μΑ
OE at 0.8 V, V _{CC} = 0 to 2.35 V (power up)					±50	^	
102	$V_{O} = 2.7 \text{ V or } 0.5 \text{ V}$ $V_{CC} = 2 \text{ V to 0 (power down)}$					±50	μΑ
lį	$V_{CC} = 5.5 V$,	V _I = 5.5 V				0.4	mA
lн	$V_{CC} = 5.5 V$,	V _I = 2.7 V				20	μΑ
liL.	$V_{CC} = 5.5 V$	V _I = 0.5 V				-0.6	mA
los‡	$V_{CC} = 5.5 V$	V _O = 0		-100		-225	mA
ICCL	V _{CC} = 5.5 V				37	60	mA
ІССН	V _{CC} = 5.5 V				2	5	mA
Iccz	V _{CC} = 5.5 V				5	8	mA
Ci	$V_{CC} = 5 V$,	$V_1 = 2.5 \text{ V or } 0.5 \text{ V}$ 6					pF
Co	$V_{CC} = 5 V$,	$V_{O} = 2.5 \text{V or } 0.5 \text{V}$				pF	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements

			V _{CC} = 5 V, T _A = 25°C		V = 4.5 V	to 5.5 V		
		′вст			'BCT373 T _A = -40°C to 85°C			T _A = 0°C to 70°C
		MIN	MAX	MIN	MAX	MIN	MAX	
tsu	Setup time, data before enable C↓	2		2		2		ns
th	Hold time, data after enable C↓	5.5		5.5		5.5		ns
t _W	Pulse duration, enable C high	7.5		7.5		7.5		ns

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

SN64BCT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

TI0290-D3251, JUNE 1990

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L R1 R2	C = 5 = 50 p = 500 = 500 = 25°	ο F, Ω, Ω,		= 4.5 V CL = 50 R1 = 50 R2 = 5	0 pF, 00 Ω, 00 Ω		UNIT	
			'	BCT373	3	T _A = -	i°C	T _A =			1
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
tPLH	D	Any Q	2	5.9	7.7	1.5	10.1	2	9.3	ns	1
t _{PHL}	U	Ariy Q	2	6.7	8.5	1	10.3	1.5	9.5	TIS	1
tPLH .	С	Anyo	2	6.2	8.2	2	10.1	2	9.3		
tPHL.	U	Any Q	2	5.9	7.8	2	9.2	2	8.8	ns	1
tPZH	ŌĒ	A=O	1	7.8	9.6	1	12.3	1	11.8		١.
tPZL	OE.	Any Q	1	8.2	10.2	1	12.5	1	12	ns	
t _{PHZ}	ŌĒ	A== 0	1	4.9	6.6	1	7.4	1	7		l
tPLZ	UE .	Any Q	1	5	6.7	1	8.1	1	7.4	ns	

SN64BCT374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

TI0256-JUNE 1990

- 8 D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Buffered Control Inputs
- State-of-the-Art BiCMOS Design Significantly Reduces Icc
- 3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'BCT374 are edgetriggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

OE 🛛 1	∪20∏V _{CC}
1Q 🔲 2	19 🗌 8Q
1D 🛚 3	18 🗌 8D
2D 🛮 4	17 🗌 7D
2Q 🛮 5	16 7Q
3Q ∏6	15 🗌 6Q
3D ∏7	14 🗌 6D

13 5D

12 5Q

11∏ CLK

DW OR N PACKAGE (TOP VIEW)

FUNCTION TABLE (each flip-flop)

4D ∏8

4Q 🗍 9

GND T10

	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	<u> </u>	Н	Н
L	1	L	L
L	L	Х	Q ₀
L	н	Х	Q ₀
L	1	Х	Q ₀ Q ₀ X ₀
Н	Χ	Х	Z

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pull up components.

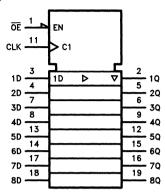
The output-enable (\overline{OE}) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down when the supply voltage is less than approximately 3 V.

The SN64BCT374 is characterized for operation from -40°C to 85°C and 0°C to 70°C.

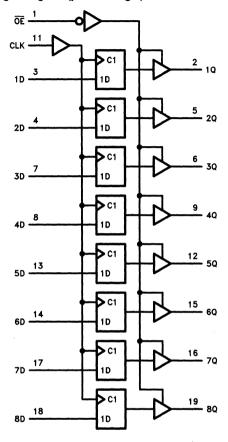
TI0256-JUNE 1990

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	-0.5 V to 7 V
Input voltage (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V _{CC}
Input clamp current	30 mA
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input negative-voltage rating may be exceeded if the input-clamp-current rating is observed.



Voc	Supply voltage	MIN	NOM 5	MAX	V
Vcc	'- <i>'</i>	4.5	- 5	5.5	
VIH	High-level input voltage	2			
VIL	Low-level input voltage			0.8	٧
ΙK	Input clamp current			-18	mΑ
ЮН	High-level output current			-15	mA
lOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT	
VIK	$V_{CC} = 4.5 V,$	$I_{\parallel} = -18 \text{mA}$					1.2	V
	V 45V		IOH = -3 mA		2.4	3.3		
VOH	V _{CC} = 4.5 V		IOH = -15 mA		2	3.1		V
VOL	V _{CC} = 4.5 V		I _{OL} = 64 mA			0.42	0.55	٧
lozн	$V_{CC} = 0 V \text{ to } 5.5 V$	/ _{CC} = 0 V to 5.5 V, V _O = 2.7 V					50	μΑ
IOZL	$V_{CC} = 0 V \text{ to 5.5 V},$	0 V to 5.5 V, V _O = 0.5 V					-50	μΑ
1	OE at 0.8 V,	V _{CC} = 0 V to 2.35 V (power up)					±50	
loz	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$	V _{CC} = 2 V to 0 V (power down)					±50	μΑ
lį.	$V_{CC} = 5.5 V,$	V _I = 5.5 V	V _I = 5.5 V				0.4	mA
lН	V _{CC} = 5.5 V,	V _I = 2.7 V					20	μΑ
ijĽ	$V_{CC} = 5.5 V,$	V ₁ = 0.5 V					-0.6	mA
los‡	V _{CC} = 5.5 V,	VO = 0 V			-100		-225	mA
ICCL	V _{CC} = 5.5 V					37	60	mA
ICCH	V _{CC} = 5.5 V	= 5.5 V				2	5	mA
ICCZ	V _{CC} = 5.5 V					5	8	mA
Ci	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V				6		pF
Co	V _C C = 5 V,	V _O = 2.5 V or 0.5 V				10		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements

		V _{CC} =		1	/CC = 4.5	V to 5.5 V		
		'BCT374		T _A = -40°C to 85°C		T _A = 0°C to 70°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		70		70		70	MHz
t _{su}	Setup time, Data before CLK↑	6.5		6.5		6.5	. !	ns
th	Hold time, Data before CLK ↑	0		0		0		ns
tw	Pulse duration, CLK high	7		8		7		ns

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS TI0256—JUNE 1990

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL R1 R2 T,	= 50 p = 500 s = 500 s = 500 s A = 25° BCT374	F, Ω, Ω, C		V _{CC} = 4.5 V C _L = 5 R1 = 5 R2 = 5	50 pF, 00 Ω, 500 Ω T _A = 0	°C to 70°C	UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax			70			70		70		MHz
tPLH	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	
tPHL	CLK	l Q	2	7.1	8.8	2	10.6	2	10	ns
tPZH	ŌĒ		1	8.3	10.1	1	12.7	1	12.3	
tPZL) OE	Q	1	8.6	10.6	1	13	1	12.7	ns
tPHZ	ŌĒ		1	4.7	6.3	1	7.1	1	6.8	
tPLZ] OE	Q	1	4.8	6.3	1	7.5	1	6.8	ns

SN64BCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCBS031--TI0211--D3254, FEBRUARY 1989

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State True Outputs Drive Bus Lines or Buffer Memory Address Registers
- High-Impedance State During Power Up and Power Down
- P-N-P Inputs Reduce DC Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

These octal buffers and line drivers are designed to have the performance of the popular SN64BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed-circuit-board layout.

The three-state control gate is a 2-input AND gate with active-low inputs so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

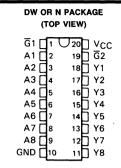
The outputs are in the high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT541 is characterized for operation from -40°C to 85°C.

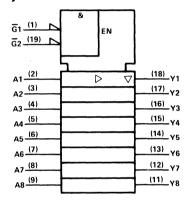
FUNCTION TABLE

	IN	PUTS	3	OUTPUT
	Ğ1	G2	Α	Υ
	L	L	L	L
ĺ	L	L	Н	н
	Н	Χ	Χ	Z
	Х	Н	Χ	z

Z = High Impedance

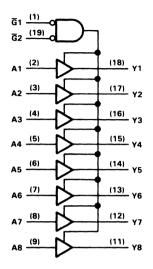


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, VCC	-0.5 V to 7 V
Input voltage	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to VCC
Current into any output in the low state	128 mA
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
VIH	High-level input voltage	2			٧
٧ıL	Low-level input voltage			0.8	٧
lк	Input clamp current			-18	mA
ЮН	High-level output current			- 15	mA
IOL	Low-level output current			64	mA
TA	Operating free-air temperature	-40		85	°C

D3254, FEBRUARY 1989-TI0211-SCBS031

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†					TYP‡	MAX	UNIT
VIK	$V_{CC} = 4.5 V$	lj = -18 mA					-1.2	٧
Vou	$V_{CC} = 4.5 V$	C = 4.5 V			2.4	3.3		V
VOH					2	3.1		٧
VOL	V _{CC} = 4.5 V			IOL = 64 mA		0.42	0.55	٧
lozh	V _{CC} = 0 V to 5.5 V, V _O = 2.7 V					50	μΑ	
IOZL	$V_{CC} = 0 V \text{ to } 5.5 V,$	$V_0 = 0.5 V$					-50	μΑ
10-	G at 0.8 V,		$V_{CC} = 0 V to 2$	2.35 V (power up)			±50	4
loz	$V_0 = 2.7 \text{ V or } 0.5 \text{ V}$		$V_{CC} = 2 V to 0$	0 (power down)			±50	μΑ
lį	$V_{CC} = 5.5 V$	$V_I = 7 V$					0.1	mA
ИН	$V_{CC} = 5.5 V,$	V _I = 2.7 V					20	μΑ
IL	$V_{CC} = 5.5 V,$	V _I = 0.5 V					-0.6	mΑ
los	$V_{CC} = 5.5 V,$	VO = 0			100		- 225	mA
ICCL	$V_{CC} = 5.5 V$					47	72	mA
ICCH	$V_{CC} = 5.5 V$					27	40	mA
Iccz	$V_{CC} = 5.5 V$	/ _{CC} = 5.5 V				5	7	mA
Ci	$V_{CC} = 5 V$,	$C = 5 \text{ V}, \qquad V_{\parallel} = 2.5 \text{ V or } 0.5 \text{ V}$				5		рF
Co	V _{CC} = 5 V,	$V_{j} = 2.5 \text{ V or } 0.5 \text{ V}$				10		PΓ

switching characteristics

PARAMETER	FROM (INPUT)	то (оитрит)	C _L R1 R2	C = 5 = 50 p = 500 = 500 = 25°	νF, Ω, Ω, C	CL = R1 = R2 = TA = N	3.5 V to 5.5 V, = 50 pF, = 500 Ω, = 500 Ω, NIN to MAX [†]	UNIT
			MIN	TYP	MAX	MIN	MAX	
tPLH		Υ	2.1	3.7	5.3	1.7	6.3	
tPHL	A	Y	3.7	5.5	7.5	3.2	8.7	ns
^t PZH	G	Y	5.3	7.2	9.3	4.4	11	
tPZL	G	Ť	6	8	10.4	5.4	12.4	ns
tPHZ	~	v	3.5	5.6	7.6	3	9.1	
tPLZ	G	G Y	3.4	5.2	7.2	3	9.4	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN64BCT543 OCTAL REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DW OR NT PACKAGE

TI0224--- D3526, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs

description

The SN64BCT543 is a noninverting octal bus transceiver. It contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB and LEBA) and output-enable (GAB and GBA) inputs permit independent control for either direction of data flow.

When the A-to-B chip enable ($\overline{\text{CEAB}}$) is high, the latches are in storage mode and the B outputs are in the high-impedance state. When $\overline{\text{CEAB}}$ is low, latch characteristics and B-output functionality are controlled by $\overline{\text{LEAB}}$ and $\overline{\text{GAB}}$ as follows:

- -when LEAB is low, the latches are transparent; taking LEAB high stores the data present at the A inputs.
- when GAB is low, the B outputs are active (high or low logic level) and reflect the data present in the A-to-B latches; when GAB is high, the B outputs are in the highimpedance state.

B-to-A data flow is controlled via the CEBA, LEBA, and GBA inputs in a manner analogous to that described above for A-to-B data flow.

The SN64BCT543 features power-up three-state circuitry for hot-card insertion applications.

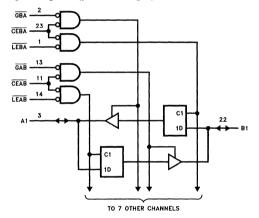
The SN64BCT543 is characterized for operation from 0°C to 70°C and from -40°C to 125°C.

(TOP VIEW) IEBA ∏1 U24 VCC GBA ∏2 23 CEBA 22 B1 A1 ∏3 **A2** □ 21 B2 A3 ∏5 20 B3 19 B4 A4 🛛 6 18 B5 А5 П A6 ∏8 17 B6 16 B7 A7 ∏9 15 B8 A8 ∏10 CEAB 11 14 LEAB

13 GAB

logic diagram (positive logic)

GND T12





SN64BCT2240 OCTAL BUFFER/MOS DRIVERS WITH 3-STATE OUTPUTS

TI0225---D3527, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C. Method 3015
- Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs

description

The SN64BCT2240 is an inverting octal buffer/ MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include $33-\Omega$ series resistors to reduce overshoot and undershoot.

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the Y outputs reflect the inverse of the data present at the A inputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

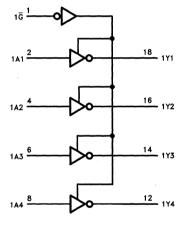
The SN64BCT2240 features power-up threestate circuitry for hot-card insertion applications.

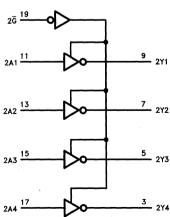
The SN64BCT2240 is characterized for operation from 0°C to 70°C and from -40°C to 125°C.

DW	OR N PACKAGE	
	(TOP VIEW)	

1 G [[U 20	□vcc
1 A 1 🔲 :	2 19]2Ğ
2Y4[]:	3 18]1Y1
1A2[]	4. 17]2A 4
2Y3[]	5 16]1Y2
1A3[]	6 15]2A3
2Y2[]	7 14]1Y3
1A4∐	B 13]2A2
2Y1∐:	9 12]1Y4
GND 🗍	10 11]2A1

logic diagram (positive logic)







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SN64BCT2241 OCTAL BUFFER/MOS DRIVERS WITH 3-STATE OUTPUTS

TI0228-D3528, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs

description

The SN64BCT2241 is a noninverting octal buffer/MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include $33\text{-}\Omega$ series resistors to reduce overshoot and undershoot.

The SN64BCT2241 features complementary output-enable inputs $1\overline{G}$ and 2G. The 1Y outputs are active (high or low logic level) when active-low enable $1\overline{G}$ is low; when $1\overline{G}$ is high, the 1Y outputs are in the high-impedance state. The 2Y outputs are active when 2G is high and in the high-impedance state when 2G is low.

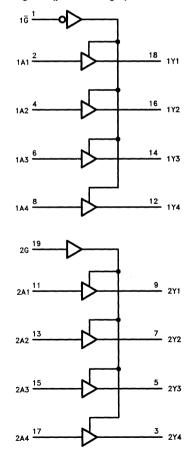
The SN64BCT2241 features power-up threestate circuitry for hot-card insertion applications.

The SN64BCT2241 is characterized for operation from 0°C to 70°C and from -40°C to 125°C

DW OR N PACKAGE (TOP VIEW)

1Ğ∐	1	U 20	□v _{cc}
1 A 1 🗌	2	19]2G
2Y4[3	18]1Y1
1A2	4	17]2A4
2Y3[5	16]1Y2
1A3[6	15]2A3
2Y2[7	14]1Y3
1A4[]	8	13]2A2
2Y1[9	12]1Y4
GND 🛚	10	11	2A1

logic diagram (positive logic)





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SN64BCT2244 OCTAL BUFFER/MOS DRIVERS WITH 3-STATE OUTPUTS

TI0229-D3529, JUNE 1990

- State-of-the-Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include "Small-Outline" Packages and Standard 300-mil DIPs

description

The SN64BCT2244 is a noninverting octal buffer/MOS driver specifically designed to drive MOS DRAMs. The outputs, which are designed to source or sink up to 12 mA, include $33-\Omega$ series resistors to reduce overshoot and undershoot

When the output-enable inputs $1\overline{G}$ and $2\overline{G}$ are low, the Y outputs reflect the data present at the A inputs. When $1\overline{G}$ and $2\overline{G}$ are high, the outputs are in the high-impedance state. Enable $1\overline{G}$ affects only the 1Y outputs; enable $2\overline{G}$ affects only the 2Y outputs.

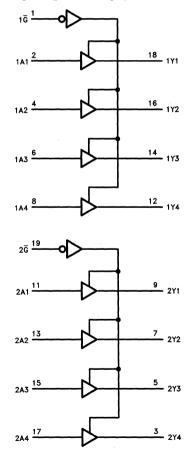
The SN64BCT2244 features power-up threestate circuitry for hot-card insertion applications.

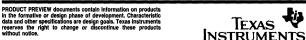
The SN64BCT2244 is characterized for operation from 0°C to 70°C and from -40°C to 125°C.

DW OR N PACKAGE (TOP VIEW)

1Ğ∐ī	U 20	□vcc
1A1 2	19	2Ğ
2Y4∐3	18]1Y1
1A2∐4	. 17]2A4
2Y3∏5	16]1Y2
1A3∐6	15]2A3
2Y2∐7	14]1Y3
1A4∐8	13]2A2
2Y1∐9	12]1Y4
GND 1	0 11	2A1

logic diagram (positive logic)





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SN64BCT25245 25-OHM OCTAL BUS TRANSCEIVERS

TI0278--- D3587, JUNE 1990

State-of-the-Art BiCMOS Design Significantly Reduces ICCZ	DW or NT PACKAGE (TOP VIEW)				
Designed to Facilitate Incident Wave Switching for Line Impedances of 25- Ω or Greater	A1 1 24 DIR GND 2 23 B1 A2 3 22 B2				
 Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs 	A3				
 Data Flow-Through Pinout (All inputs on Opposite Side From Outputs) 	A5				
 High-Impedance State During Power Up and Power Down 	A7 10 15 B7 GND 11 14 B8				
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015 	A8				
Package Options Include Plastic "Small Outline" Packages, and Standard Plastic					

description

300-mil DIPs

These $25-\Omega$ octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input \overline{G} can be used to disable the device so the buses are effectively isolated.

These transceivers are capable of sinking 188 mA of I_{OL} current through the A port, which facilitates switching 25- Ω transmission lines on the incident wave. They are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers. The distributed V_{CC} and GND pins minimize the noise generated by the simultaneous switching of the outputs.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V. The SN64BCT25245 is characterized for operation from -40° C to 85° C and 0° C to 70° C.

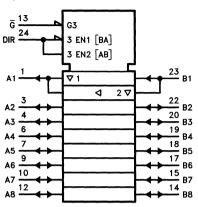
FUNCTION TABLE, EACH SECTION

ENABLE	INPUTS	OPERATION
G	DIR	'64BCT25245
L	L	B Data To A Bus
L	Н	A Data To B Bus
Н	X	Bus Isolation

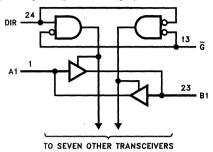


D3587, JUNE 1990-TI0278

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 7 V
Input voltage: Control Inputs (see Note 1)	. −0.5 V to 7 V
I/O ports (see Note 1)	-0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	. −0.5 V to 7 V
Voltage applied to any output in the high state (B Port)	-0.5 V to VCC
Input clamp current	30 mA
Current into any output in the low state: A Port	376 mA
B Port	48 mA
Operating free-air temperature range:	
	-40°C to 85°C
Storage temperature range	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN64BCT25245 25-OHM OCTAL BUS TRANSCEIVER

TI0278-D3587, JUNE 1990

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	V _{CC} Supply voltage				5.5	٧
VIH	High-level input voltage		2			٧
VIL	V _{IL} Low-level input voltage				0.8	٧
ΊΚ	Input clamp current				-18	mA
1	High level output a went	A1-A8			-80	mA
IOH	High-level output current B1-B8				-3	mA
1	Law lavel author author	A1-A8			188	mA
lOL	Low-level output current B1-B8				24	mA
TA	Operating free-air temperature		-40		85	°C

SN64BCT25245 25-OHM OCTAL BUS TRANSCEIVER

D3587, JUNE 1990-TI0278

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST COND	TEST CONDITIONS			MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$				-1.2	V
	A A	$V_{CC} = 4.75 \text{ V, I}_{OH} = -3 \text{ mA}$		2.7			
Vон	Any A	$V_{CC} = 4.5 \text{ V, I}_{OH} = -80 \text{ mA}$		2			٧
	Any B	$V_{CC} = 4.5 \text{ V, I}_{OH} = -3 \text{ mA}$		2.4	3.3		
	A A	V _{CC} = 4.5 V, I _{OL} = 94 mA			0.42	0.55	
VOL	Any A	$V_{CC} = 4.5 \text{ V}, I_{OL} = 188 \text{ mA}$				0.7	٧
	Any B	$V_{CC} = 4.5 \text{V}, \text{IOL} = 24 \text{mA}$			0.35	0.5	
	Power Up	G -+ 0.0 V V 0.4-0.0 V	$V_0 = 2.7 V$			70	μΑ
	Power up	\overline{G} at 0.8 V, $V_{CC} = 0$ to 2.3 V	$V_0 = 0.5 V$			-0.6	mA
loz	Dawe Dawe	5	$V_0 = 2.7 V$			70	μΑ
	Power Down	\overline{G} at 0.8 V, $V_{CC} = 0$ to 2 V	$V_0 = 0.5 V$			-0.6	mA
1.	A and B	$V_{CC} = 0 \text{ to } 5.5 \text{ V}, V_{I} = 5.5 \text{ V}$	V _{CC} = 0 to 5.5 V, V _I = 5.5 V			0.25	mA
ή	DIR and G	V _{CC} = 0 to 5.5 V, V _I = 5.5 V				0.1	
1+	A and B	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$				70	
ΙΗ‡	DIR and G	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$				20	μΑ
IIL‡	A and B	V _{CC} = 5.5 V, V _I = 0.5 V V _{CC} = 5.5 V, V _I = 0.5 V				-0.6	4
	DIR and G					-0.6	mA
los	B port only¶	$V_{CC} = 5.5 \text{ V}, V_{O} = 0 \text{ V}$				150	mA
ICCL	A to B	V 55V			48	60	
ICCH	7 4 10 6	V _{CC} = 5.5 V			36	46	mA
ICCL	Dan A	V			95	115	mA
ІССН	B to A	V _{CC} = 5.5 V			63	77	mA
ICCZ		V _{CC} = 5.5 V			12	16	mA
Cin	G and DIR	V _{CC} = 5.5 V, V _I = 2.5 V or 0.5 V			8		pF
Cio	A port	V F F V V - 0 F V - 0 F V			18		
Cio	B port	$V_{CC} = 5.5 \text{ V}, V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			8		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed 10 ms.

Testing for this parameter on the A port is not recommended.

TI0278--- D3587, JUNE 1990

switching characteristics (see Note 2), (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	C _L R1 R2 T <i>j</i>	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = 25^{\circ}C$ $^{\circ}64BCT25245$		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_{A} = -40^{\circ}\text{C to } 85^{\circ}\text{C} \qquad T_{A} = 0^{\circ}\text{C to } 70^{\circ}\text{C}$			UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tPLH	Α		1.2	3.3	5.1	1.2	5.7	1.2	5.7	
tPHL		В	1.9	4.3	6.7	1.9	7.3	1.9	7.2	ns
^t PLH	В		1.2	3.3	4.8	1.2	5.5	1.2	5.5	
tPHL		Α	2.1	4	5.6	2.1	6.3	2.1	6.2	ns
tPZH	G		3.7	6.3	8.4	3.7	9.7	3.7	9.6	
tPZL	G	A	4.5	7.4	9.2	4.5	10.6	4.5	10.3	ns
tPHZ	G		1.8	3.7	5.5	1.8	6.2	1.8	6.2	
tPLZ	G	A	3.3	5.1	7.2	3.3	8.8	3.3	8.3	ns
^t PZH	G	В	3.4	5.7	7.9	3.4	8.9	3.4	8.9	
tPZL		В	4.3	6.6	8.7	4.3	9.9	4.3	9.7	ns
tPHZ	G	В	2.7	4.5	6.3	2.7	6.9	2.7	6.9	
tPLZ		B	1.7	4.5	6.8	1.7	7.7	1.7	7.5	ns

NOTE 2: For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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Bus-Termination Array Products	5
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Memory Driver Products	10
SCOPE™ Testability Products	11
	12
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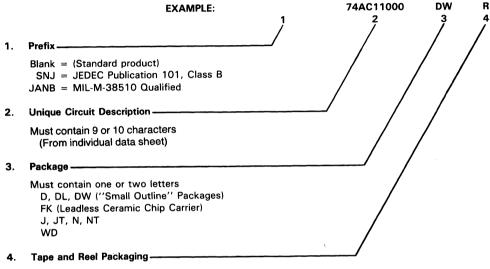
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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

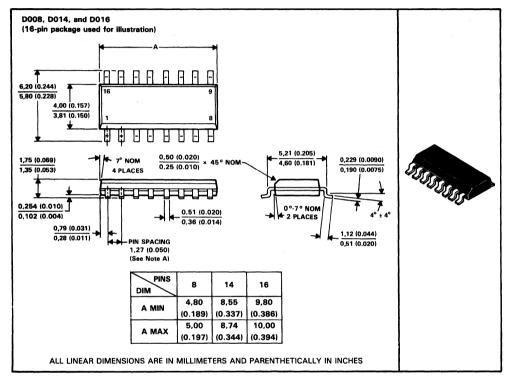


Must be designated by the letter R and valid for surface mount packages only. All orders for tape and reel must be for whole reels.



D008, D014 and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

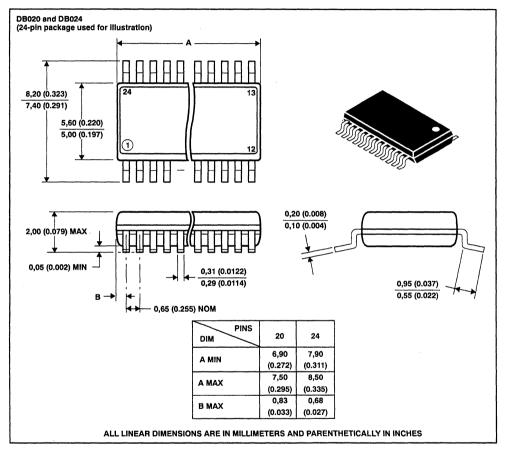


NOTES: A. Leads are within 0,125 (0.005) radius of true position at maximum material dimension.

- B. Lead tips to be planar within $\pm 0,051$ (0.002).
- C. Body dimensions do not include mold flash or protrusion.
- D. Mold protrusion shall not exceed 0,15 (0.006).
- E. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).

DB020 and DB024 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Body dimensions do not include mold flash or protrusion.

B. Mold protrusion does not exceed 0,15 (0.006).

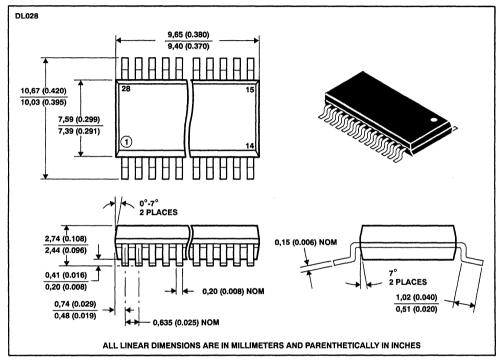
C. Interlead flash is controlled by TI statistical process control (additional information available through TI field office).

D. Lead tips are planar within ± 0.05 (0.002).



DL028 plastic "small outline" package

This "small outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

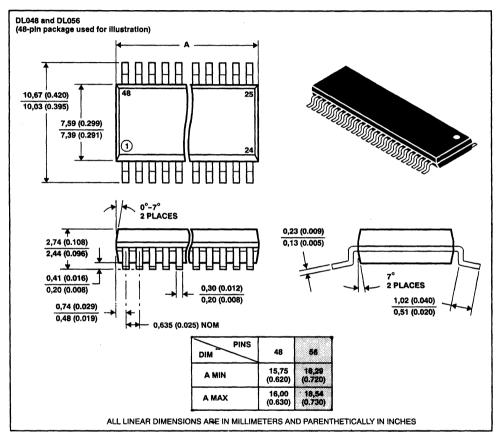


NOTES: A. Body dimensions do not include mold flash or protrusion.

- B. Mold protrusion does not exceed 0,15 (0.006).
- C. Interlead flash is controlled by TI statistical process control (additional information available through TI field office).
- D. Lead tips are planar within $\pm 0,05$ (0.002).

DL048 and DL056 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



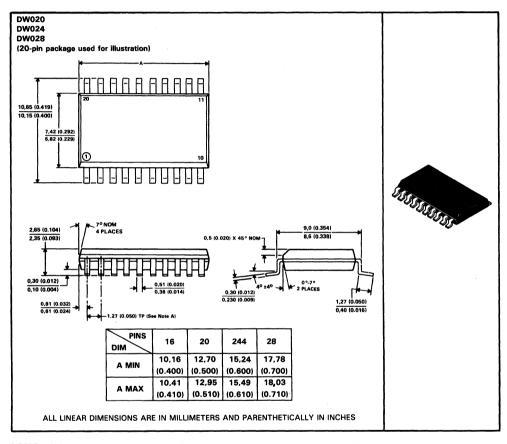
NOTES: A. Body dimensions do not include mold flash or protrusion.

- B. End protrusion shall not exceed 0,15 (0.006).
- C. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).
- D. Lead tips to be planar within $\pm 0,05$ (0.002).



DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



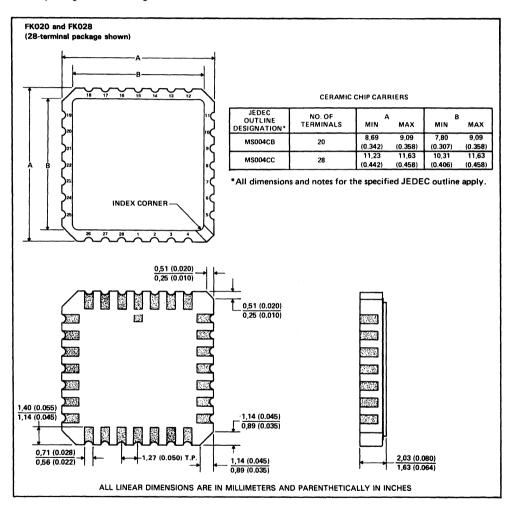
NOTES: A. Leads are within 0,125 (0.005) radius of true position at maximum material dimension.

- B. Lead tips to be planar within $\pm 0,051$ (0.002).
- C. Body dimensions do not include mold flash or protrusion.
- D. Mold protrusion shall not exceed 0,15 (0.006).
- E. Interlead flash shall be controlled by TI Statistical Process Control (Additional information is available through TI field offices).

FK020 and FK028 ceramic chip carrier packages

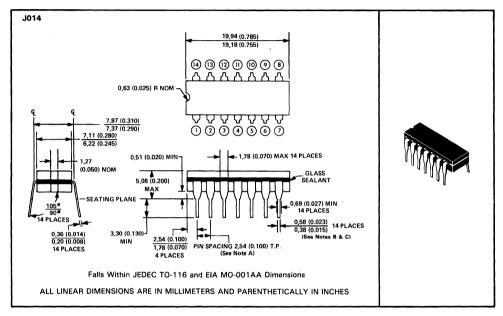
Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.



J014 ceramic dual-in-line package

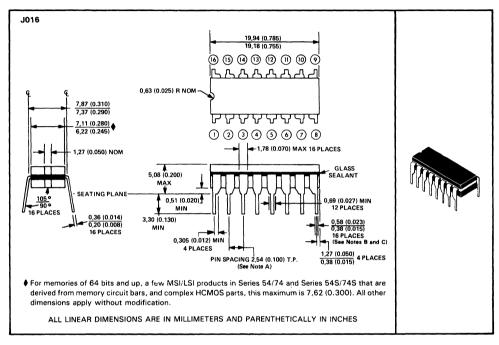
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J016 ceramic dual-in-line package

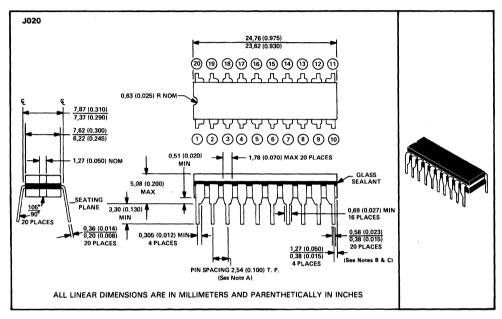
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J020 ceramic dual-in-line package

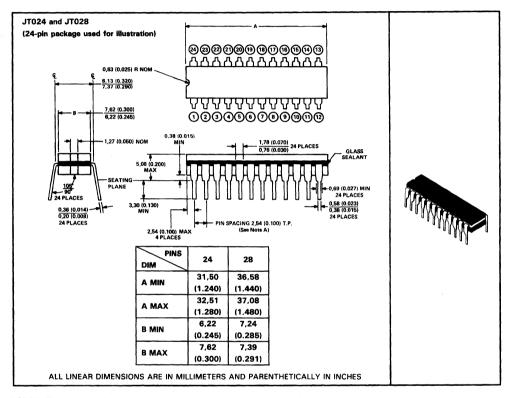
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JT024 and JT028 ceramic dual-in-line packages

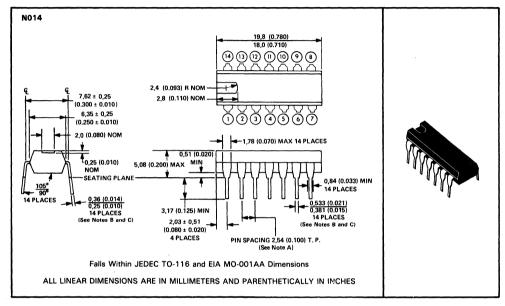
Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") pins require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

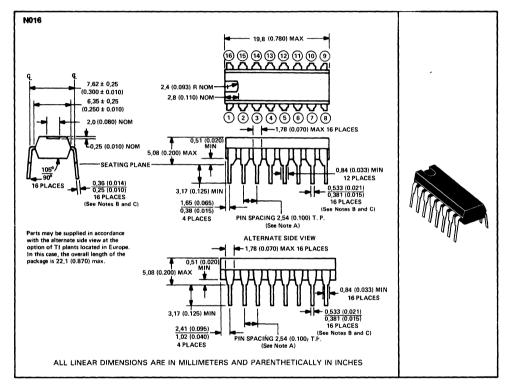


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



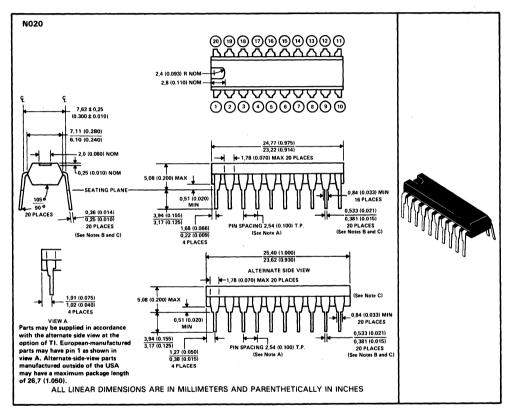
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.



N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

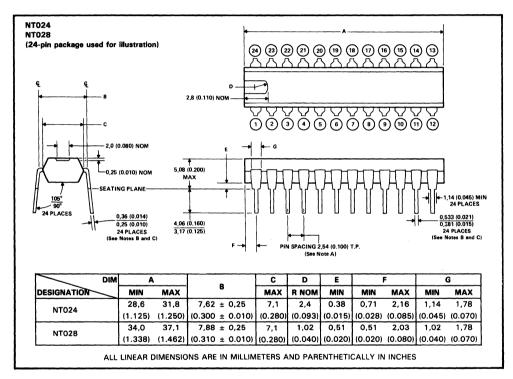
- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.



NT024 and NT028 plastic dual-in-line packages

Each of these packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin and 28-pin packages, the letter N is used by itself since the 24-pin and 28-pin packages may be available in more than one row-spacing. For the 24-pin and 28-pin packages, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

B. This dimension does not apply for solder-dipped leads.

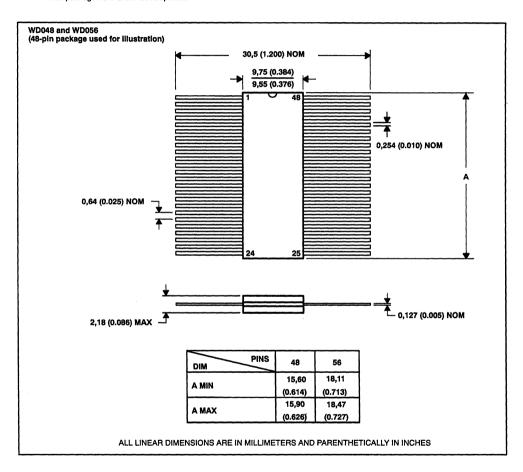
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

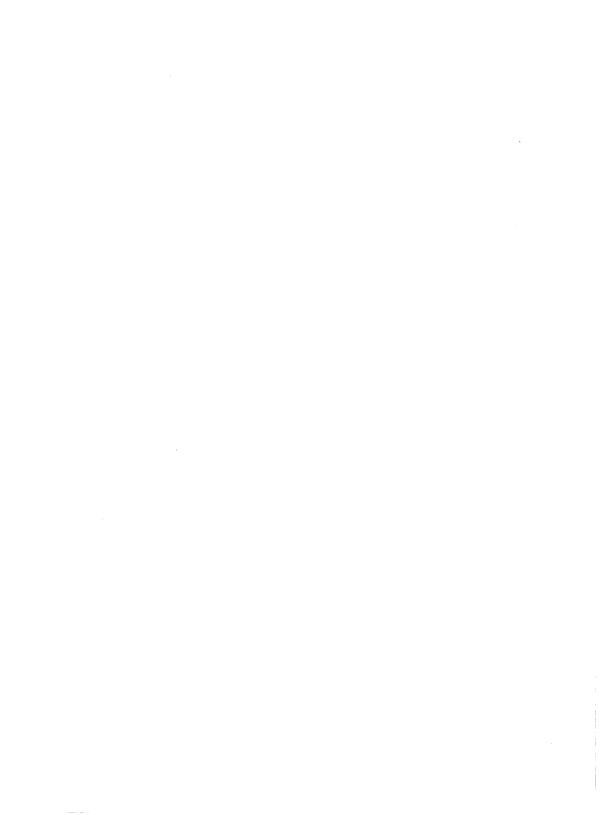


WD048 and WD056 ceramic flat packages†

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

[†] These packages are under development.





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