



Interface Circuits

Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers

Data Book

Data Book

Interface Circuits Data Transmission and Control Circuits,

Peripheral Drivers/Power Actuators, Display Drivers

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Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers



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INTRODUCTION

In the 1990 Interface Circuits Data Book, the Linear Products Division of Texas Instruments presents technical information on various products for electronic media and electronic devices.

TI's Interface circuits represent technologies from classic bipolar through BIDFET, Advanced Low-Power Schottky (ALS), IMPACT™, LinBiCMOS™, and Advanced LinCMOS™ processes. The ALS and IMPACT™ oxide-isolated technologies provide the Interface family with improved speed-power characteristics. LinBiCMOS™ and Advanced LinCMOS™ technologies feature a step-function improvement in impedance, speed, power dissipation, and threshold stability.

This data book provides information on the following types of products:

- Data-Transmission Circuits
- High-Current Actuators and Peripheral Drivers
- High-Voltage Display Drivers
- Asynchronous Communication Elements
- Intelligent-Power Devices

The data-transmission line drivers, receivers, and transceivers, which support many popular data transmission standards, connect electronic devices and systems at high data rates over significant cable lengths. The high-current actuators and peripheral drivers combine both logic control and high-current drive capability in a single package. For flat-panel, AC-plasma, vacuum fluorescent, and electroluminescent display applications, the high-voltage display drivers provide cost-effective and reliable service.

Among TI's new products in the 1990 Interface Data Book are Asynchronous Communication Elements (ACEs) and Intelligent-Power devices. The ACEs provide complete universal interface capabilities between electronic systems, which minimize device components and power dissipation while increasing data rates. The Intelligent-Power devices are useful for applications that require high energy loads and load protection circuits operating in harsh electrical environments.

These Interface products range from the classic line driver to the Asynchronous Communication Element. New surface-mounted packages (8 to 68 leads) include both ceramic and plastic chip carriers, and the small-outline (D) plastic packages that optimize board density with minimum impact on power dissipation capability.

The alphanumeric index provides a quick method of locating the correct device type, with new products as indicated. The selection guide includes a functional description of each product with information on key parameters and packaging types. A cross-reference table listing other manufacturers with the TI direct or nearest replacement devices is also available. Ordering information and mechanical data are in the last section of this data book.

While this volume offers design and specification data only for Interface components, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that you will discover the new 1990 *Interface Circuits Data Book* to be a significant addition to your collection of technical literature.

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DATA TRANSMISSION AND CONTROL CIRCUITS SELECTION GUIDE

line transceivers (continued)

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| | Single-Ended | 8 | SN55ALS057 | J,W | 2-239 |
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| APPLICATION | TRANSLATORS PER PACKAGE | DEVICE TYPE | PACKAGE | PAGE NUMBER |
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controllers

| DESCRIPTION | FUNCTION | PRODUCT FEATURES | DEVICE TYPE | PACKAGE | PAGE NUMBER |
|----------------------|---|--|----------------|----------|----------------|
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| ACE [†] | Single ACE with Parallel Port and without FIFO [‡] | Programmable Interface Characteristics | TL16C451 | FN | 2-903 |
| ACE [†] | Dual ACE with Parallel Port and without FIFO [‡] | Programmable Interface Characteristics | TL16C452 | FN | 2-903 |
| ACE [†] | Single ACE with FIFO [‡] | Functional Upgrade of the 16C450 | TL16C550A | FN,N | 2-925 |
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 $^{^\}dagger \text{ACE--Asynchronous Communications Element} \\ ^\dagger \text{FIFO--First In First Out}$

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| AM26LS33C | AM26LS33AC | 2-11 | μA9637AM | uA9637AM | 2-961 |
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| μA55108M | SN55108B | 2-87 | MC1489A | SN75189A | 2-231 |
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DISPLAY DRIVERS SELECTION GUIDE

electroluminescent display drivers

| DESC. | PRODUCT FEATURES | DRIVERS PER PKG | INPUT COMPATIBILITY | POWER SUPPLY | TYPE | PKG |
|-------------------|--|-----------------------|------------------------|--|--|-------|
| , | 225-V open-drain DMOS outputs Serial-in, parallel-out architecture | | | | SN55551 SN55552 | FD |
| | 50-mA current sink output capability Extremely low steady-state power consumption Left side (SNXX551) and right side (SNXX552) drivers enhance circuit layout | 32 | | | SN65551 SN65552 SN75551 SN75552 | FN, N |
| ROW DRIVERS | Monolithic BIDFET integrated circuits Very low steady-state power consumption 300-mA output capability High-voltage open-collector N-P-N outputs | | CMOS | V _{CC1} (logic) = 10.8 V to 15 V | SN65557 SN65558 SN75557 SN75558 | FN |
| | 225-V totem-pole BIDFET output structures | | | | SN55563A SN55564A | FJ |
| | 70-mA output source/sink capability Very low steady-state power consumption 3-state capabilities Selectable open-source or open-drain output | 34 | | | SN65563A SN65564A SN75563A SN75564A | FN |
| | 60-V totem-pole BIDFET output structures | | | | SN55553 SN55554 | FD |
| COLUMN DRIVERS | Serial-in, parallel-out architecture 15-mA sink or source output capability Top (SNXX553) and bottom (SNXX5554) drivers enhance circuit layout | 32 | CMOS | V _{CC1} (logic) = 10.8 V to 15 V | SN65553 SN65554 SN75553 SN75554 | FN, N |
| DRIVERS | 90-V output voltage swing capability 15-mA output source and sink current capability High-speed serially-shifted data input Totem-pole outputs Latches on all driver outputs | | | | SN65555 SN65556 SN75555 SN75556 | FN, N |

vacuum fluorescent display drivers

| DESC. | PRODUCT FEATURES | DRIVERS PER PKG | INPUT COMPATIBILITY | POWER SUPPLY | ТҮРЕ | PKG |
|---|--|-----------------------|------------------------|--|----------------------|------|
| | Serial-in, parallel-out architecture 60-V totem-pole outputs 25-mA current source output capability On-board latches | 12 | TTL | V _{CC1} (logic) = 5 V to 15 V, V _{CC2} (display) = 0 to 60 V | SN65512B SN75512B | DW,N |
| ANODE, GRID DRIVERS | All features same as SN65512B except: • 32 bits for large format displays | 32 | CMOS, TTL | V _{CC1} (logic) = 5 V to 15 V, V _{CC2} (display) = 0 to 130 V | SN65518 SN75518 | FN,N |
| FOR SEGMENT OR DOT MATRIX FORMATS | Serial-in, parallel-out architecture 60-V totem-pole outputs 40-mA current source output Improved direct replacement for UCN4810A and TL4810A | 10 | CMOS | V _{CC1} (logic) = 5 V to 15 V, V _{CC2} (display) = 0 | TL4810B | DW,N |
| | 70-V output voltage swing capability Drives up to 20 lines Direct replacement for Sprague UCN5812 | 20 | | to 60 V | TL5812 | FN,N |

dc plasma and gas discharge display drivers

| DESC. | PRODUCT FEATURES | DRIVERS PER PKG | INPUT COMPATIBILITY | POWER SUPPLY | TYPE | PKG |
|-------------------------|--|-----------------------|------------------------|---|----------------------|-----|
| SCAN LINE DRIVERS | 180-V open drain parallel outputs 220-mA parallel output sink current Left side (SN751506) and right side (SN751516) drivers enhance circuit layout | | | V _{CC} (logic) = 4 V to 6 V | SN751506 SN751516 | FT |
| DATA LINE DRIVERS | - 120-V open collector P-N-P parallel outputs Two parallel high-speed 16-bit shift registers Latches on all driver outputs Top (SN751508) and bottom (SN751518) drivers enhance circuit layout | 32 | CMOS | V _{CC} (logic) = 4.5 V to 5.5 V | SN751508 | FT |

DISPLAY DRIVERS SELECTION GUIDE

ac plasma display drivers

| DESC. | PRODUCT FEATURES | DRIVERS PER PKG | INPUT COMPATIBILITY | POWER SUPPLY | ТҮРЕ | PKG · |
|---------|--|-----------------------------------|------------------------|--|----------------------|-----------|
| | High-speed serial-in, parallel-out architecture (8 MHz) | 32 (8 bits with 1 of 4 selectors) | | V _{CC1} (logic) = 10.8 V to 13.2 V V _{CC2} (display) = 0 | SN55500E | FD, JD |
| | • Fast output transitions (150 ns typ) | | | to 100 V | SN65500E | FN, N |
| AXIS | 15-mA output current capability | | смоѕ | | SN75500E | , , , , , |
| DRIVERS | X-axis driver (SNXX500) Y-axis driver (SNXX501) | 32 | | | SN55501E | FD, JD |
| | Military temperature packages available (SN55500, SN55501) | 32×1 | | | SN65501E SN75501E | FN, N |

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PERIPHERAL DRIVERS/ACTUATORS SELECTION GUIDE

General-Purpose Drivers and Actuators

| SWITCHING VOLTAGE MAX (V) | OFF- STATE VOLTAGE MAX (V) | OUTPUT CURRENT (mA) | DRIVERS PER PACKAGE | OUTPUT CLAMP DIODES | INPUT CAPABILITY | FUNCTION | DELAY TIME TYP (ns) | ТҮРЕ | PKG | PAGE |
|---------------------------------|-------------------------------------|---------------------------|---------------------------|---------------------------|----------------------|-------------------------------------|------------------------------|---------------------|-----------|---------------|
| 20 | 30 | 300 | 2 | NO | TTL | AND | 18 | SN55451B | FK,JG | 4-23 |
| 20 | 30 | 300 | 2 | NO | TTL | NAND | 25 | SN55452B | 1 ' | |
| 20 | 30 | 300 | 2 | NO | TTL | OR | 18 | SN55453B | | |
| 20 | 30 | 300 | 2 | NO | TTL | NOR | 26 | SN55454B | | |
| 20 | 30 | 300 | 2 | NO | TTL | AND | 18 | SN75451B | | 4-23 |
| 20 | 30 | 300 | 2 | NO | TTL | NAND | 25 | SN75452B | | 4-23 |
| 20 | 30 | 300 | 2 | NO | TTL | OR | 18 | SN75453B | | 4-23 |
| 20 | 30 24 | 300 500 | 2 | NO YES | TTL | NOR MOS DRIVER | 26 35 | SN75454B SN75372 | D,P | 4-23 4-39 |
| 24 | 24 | 500 | 4 | YES | TTL | MOS DRIVER | 35 | SN75374 | D,N | 4-39 |
| 30 | 35 | 300 | 2 | NO | TTL | AND | 28 | SN55461 | FK,JG | |
| 30 | 35 | 300 | 2 | NO | TTL | NAND | 38 | SN55462 | FK,JG | |
| 30 | 35 | 300 | 2 | NO | TTL | OR | 28 | SN55463 | FK,JG | |
| 30 | 35 | 300 | 2 | NO | TTL | NOR | 35 | SN55464 | FK,JG | |
| 30 | 35 | 300 | 2 | NO | TTL | AND | 28 | SN75461 | D,P | 4-31 |
| 30 | 35 | 300 | 2 | NO | TTL | NAND | 38 | SN75462 | D,P | 4-31 |
| 30 | 35 | 300 | 2 | NO | TTL | OR | 28 | SN75463 | D,P | 4-31 |
| 30 | 24 | 1000 | 8 | YES | TTL,CMOS | SERIAL TO PARALLEL POWER CHIP | 2000 | TPIC2801 | ΚV | 4-141 |
| 35 | 70 | 500 | 4 | YES | TTL,CMOS | INVERT W ENAB | 1050 | SN75437A | NE | 4-65 |
| 35 | 70 | 600 | 4 | YES | TTL,CMOS | INVERT W ENAB | 750 | SN75435 | NE | 4-59 |
| 35 | 70 | 1000 | 4 | YES | TTL,CMOS | INVERT W ENAB | 1050 | SN75438 | NE | 4-65 |
| 35 | 50 | 1250 | 4 | YES | TTL | INVERT | 500 | ULN2064 | NE | 4-163 |
| 35 | 50 | 1250 | 4 | YES | MOS | INVERT | 500 | ULN2066 | NE | 4-163 |
| 35 | 50 | 1250 | 4 | YES | TTL,CMOS | INVERT | 500 | ULN2068 | NE | 4-169 |
| 35 | 50 | 1250 | 4 | NO | TTL,CMOS | INVERT | 500 | ULN2074 | NE | 4-175 |
| 45 | 45 | 1000 | 4 | YES YES | TTL,CMOS | AND | 2000 300 | TPIC2404 SN75446 | KN D.P | 4-123 4-77 |
| 55 55 | 70 70 | 350 350 | 2 | YES | TTL,CMOS TTL,CMOS | NAND | 300 | SN75446 SN75447 | D.P | 4-77 |
| 55 | 70 | 350 | 2 | YES | TTL,CMOS | OR | 300 | SN75448 | D.P | 4-77 |
| 55 | 70 | 350 | 2 | YES | TTL,CMOS | NOR | 300 | SN75449 | D.P | 4-77 |
| 50 | 70 | 500 | 4 | YES | TTL,CMOS | INVERT W ENAB | 1050 | SN75436 | NE | 4-65 |
| 50 | 50 | 350 | 7 | YES | TTL,CMOS,PMOS | INVERT | 250 | ULN2001A | ł | 4-155 |
| 50 | 50 | 350 | 7 | YES | 25 V PMOS | INVERT | 250 | ULN2002A | | 4-155 |
| 50 | 50 | 350 | 7 | YES | TTL,CMOS | INVERT | 250 | ULN2003A | 1 | 4-155 |
| 50 | 50 | 350 | 7 | YES | 15 V MOS | INVERT | 250 | ULN2004A | 1 | 4-155 |
| 50 | 50 | 350 | 7 | YES | TTL | INVERT | 250 | ULN2005A | D,N | 4-155 |
| 50 | 50 | 1300 | 4 | YES | TTL,CMOS | INVERT W ENAB | 1500 | SN75439 | NE | 4-71 |
| 50 | 80 | 1500 | 4 | YES | TTL | INVERT | 500 | ULN2065 | NE | 4-163 |
| 50 | 80 | 1500 | 4 | YES | MOS | INVERT | 500 | ULN2067 | NE | 4-163 |
| 50 | 80 | 1500 | 4 | YES | TTL,5 V MOS | INVERT | 500 | ULN2069 | NE | 4-169 |
| 50 | 80 | 1500 | 4 | NO | TTL,5 V MOS | INVERT | 500 | ULN2075 | NE | 4-175 |

PERIPHERAL DRIVERS/ACTUATORS SELECTION GUIDE

General-Purpose Drivers and Actuators (Continued)

| SWITCHING VOLTAGE MAX (V) | OFF- STATE VOLTAGE MAX (V) | OUTPUT CURRENT (mA) | DRIVERS PER PACKAGE | OUTPUT CLAMP DIODES | INPUT CAPABILITY | FUNCTION | DELAY TIME TYP (ns) | TYPE | PKG | PAGE |
|---------------------------------|-------------------------------------|---------------------------|---------------------------|---------------------------|---------------------|----------------|------------------------------|----------|-------|-------|
| 55 | 70 | 300 | 2 | NO | TTL | AND . | 28 | SN75471 | D,P | 4-91 |
| 55 | 70 | 300 | 2 | NO | TTL | NAND | 38 | SN75472 | D,P | 4-91 |
| 55 | 70 | 300 | 2 | NO | TTL | OR | 28 | SN75473 | D,P | 4-91 |
| 55 | 70 | 300 | 2 | YES | TTL,CMOS | AND | 200 | SN75476 | D,P | 4-97 |
| 55 | 70 | 300 | 2 | YES | TTL,CMOS | NAND | 200 | SN75477 | D,P | 4-97 |
| 55 | 70 | 300 | 2 | YES | TTL,CMOS | OR | 200 | SN75478 | D,P | 4-97 |
| 55 | 70 | 300 | 2 | YES | TTL,CMOS | NOR | 200 | SN75479 | D,P | 4-97 |
| 60 | 60 | 100 | 4 | YES | TTL,CMOS,MOS | TELECOM RY DRV | 1000 | DS3680I | D,J,N | 4-3 |
| 60 | 60 | 1000 | 4 | YES | TTL,CMOS | INVERT | | TPIC2406 | KN | 4-129 |
| 60 | 100 | 350 | 7 | YES | TTL | INVERT | 250 | SN75465 | D,N | 4-83 |
| 60 | 100 | 350 | 7 | YES | TTL,CMOS,PMOS | INVERT | 250 | SN75466 | D,N | 4-83 |
| 60 | 100 | 350 | 7 | YES | 25 V PMOS | INVERT | 250 | SN75467 | D,N | 4-83 |
| 60 | 100 | 350 | 7 | YES | TTL,CMOS | INVERT | 250 | SN75468 | D,N | 4-83 |
| 60 | 100 | 350 | 7 | YES | 15 V MOS | INVERT | 250 | SN75469 | D,N | 4-83 |

Motor Drivers and Power Actuators

| SWITCHING VOLTAGE MAX (V) | OFF- STATE VOLTAGE MAX (V) | OUTPUT CURRENT (mA) | DRIVERS PER PACKAGE | OUTPUT CLAMP DIODES | INPUT CAPABILITY | FUNCTION | DELAY TIME TYP (ns) | TYPE | PKG | PAGE |
|---------------------------------|-------------------------------------|---------------------------|---------------------------|---------------------------|---------------------|---------------|------------------------------|----------|-----|-------|
| 36 | 36 | 600 | 4 | YES | TTL | HALF-H DRIVER | 600 | L293D | NE | 4-11 |
| 36 | 36 | 1000 | 4 | NO | TTL | HALF-H DRIVER | 600 | L293 | NE | 4-7 |
| 36 | 36 | 1000 | 4 | YES | TTL,CMOS | HALF-H DRIVER | 600 | SN754410 | NE | 4-103 |
| 36 | 36 | 1000 | 4 | NO | TTL,CMOS | HALF-H DRIVER | 600 | SN754411 | NE | 4-109 |
| 46 | 46 | 2000 | 2 | NO | TTL | FULL-H DRIVER | | L298 | ΚV | 4-15 |
| 46 | 46 | 2000 | 2 | NO | TTL | FULL-H DRIVER | | TPIC0298 | ΚV | 4-115 |

PERIPHERAL DRIVERS/ACTUATORS CROSS-REFERENCE GUIDE

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

| FAIRCHILD | SUGGESTED TI REPLACEMENT | PAGE NO. | MOTOROLA | SUGGESTED TI REPLACEMENT | PAGE NO. |
|-------------------------------|----------------------------------|-------------------------|-------------------------------|----------------------------------|-------------------------|
| μΑ75451 μΑ75452 | SN75451B SN75452B | 4-23 4-23 4-23 | ULN2003 ULN2004 | ULN2003A ULN2004A | 4-155 4-155 |
| μΑ75453 μΑ75454 | SN75453B SN75454B | 4-23 | ULN2064 ULN2065 | ULN2064 ULN2065 | 4-163 4-163 |
| μΑ75461 μΑ75462 | SN75461 SN75462 | 4-31 4-31 | ULN2066 ULN2067 ULN2068 | ULN2066 ULN2067 ULN2068 | 4-163 4-163 4-169 |
| MC1412 MC1413 | ULN2002A ULN2003A | 4-155 4-155 | ULN2069 | ULN2069 | 4-169 |
| μΑ3680 μΑ9665 | DS3680 ULN2001A | 4-3 4-155 | ULN2074 ULN2075 | ULN2074 ULN2075 | 4-175 4-175 |
| μΑ9666 μΑ9667 μΑ9668 | ULN2002A ULN2003A ULN2004A | 4-155 4-155 4-155 | NATIONAL | SUGGESTED TI REPLACEMENT | PAGE NO. |
| μΑ75471 μΑ75472 μΑ75473 | SN75471 SN75472 SN75473 | 4-91 4-91 4-91 | DS3611 DS3612 DS3613 | SN75471 SN75472 SN75473 | 4-91 4-91 4-91 |
| MOTOROLA | SUGGESTED TI REPLACEMENT | PAGE NO. | DS3658 DS3668 DS3680 | SN75437A SN75435 DS3680 | 4-65 4-59 4-3 |
| MC1411 MC1412 MC1413 | ULN2001A ULN2002A ULN2003A | 4-155 4-155 4-155 | DS75361 DS75365 | SN75372 SN75374 | 4-39 4-49 |
| MC1413T MC1416 | SN75468 ULN2004A | 4-83 4-155 | DS75451 DS75452 DS75453 | SN75451B SN75452B SN75453B | 4-23 4-23 4-23 |
| MC1471 MC1473 MC1474 | SN75476 SN75478 SN75479 | 4-97 4-97 4-97 | DS75454 DS75461 | SN75454B SN75461 | 4-23 4-31 |
| SN75451B SN75452B | SN75451B SN75452B | 4-23 4-23 | DS75462 DS75463 | SN75462 SN75463 | 4-31 4-31 |
| SN75453B SN75454B | SN75453B SN75454B | 4-23 4-23 | LM3611 LM3612 LM3613 | SN75471 SN75472 SN75473 | 4-91 4-91 4-91 |
| ULN2001 ULN2002 | ULN2001A ULN2002A | 4-155 4-155 | LM75453 | SN75453B | 4-23 |

PERIPHERAL DRIVERS/ACTUATORS CROSS-REFERENCE GUIDE

| RIFA | SUGGESTED TI | PAGE | SILICON | SUGGESTED TI | PAGE |
|-----------|-----------------------|----------------|--------------------|-----------------|-------------|
| | REPLACEMENT | NO. | GENERAL | REPLACEMENT | NO. |
| PBD352301 | ULN2001A | 4-155 | SG2023 | SN75468 | 4-83 |
| PBD352302 | ULN2004A | 4-155 | SG2024 | SN75469 | 4-83 |
| PBD352303 | ULN2003A | 4-155 | SG75451 | SN75451B | 4-23 |
| PBD352304 | ULN2002A | 4-155 | SG75451 | SN75452B | 4-23 |
| PBD352311 | SN75466 | 4-83 | SG75453 | SN75453B | 4-23 |
| PBD352312 | SN75469 | 4-83 | SG75454 | SN75454B | 4-23 |
| PBD352313 | SN75468 | 4-83 | SG75461 | SN75461 | 4-31 |
| PBD352314 | SN75467 | 4-83 | SG75461 SG75462 | SN75462 | 4-31 |
| | | | SG75463 | SN75463 | 4-31 |
| | SUGGESTED | PAGE | | | |
| SGS-ATES | TI REPLACEMENT | NO. | SG75473 | SN75473 | 4-91 |
| L201 | ULN2001A | 4-155 | | SUGGESTED | 2405 |
| L202 | ULN2001A | 4-155 | SPRAGUE | TI | PAGE NO. |
| L203 | ULN2003A | 4-155 | | REPLACEMENT | NO. |
| L204 | ULN2004A | 4-155 | UDN-2541 | SN75437A | 4-65 |
| L293 | L293 | 4-7 | UDN-3611 | SN75471 | 4-91 |
| L293 | SN754411 [†] | 4-109 | UDN-3612 | SN75472 | 4-91 |
| L293D | L293D | 4-11 | UDN-3613 | SN75473 | 4-91 |
| L293D | SN754410 [†] | 4-103 | UDN-5711 | SN75476 | 4-97 |
| L298 | L298 | 4-15 | UDN-5713 | SN75478 | 4-97 |
| ULN2001 | ULN2001A | 4-155 | UDN-5714 | SN75479 | 4-97 |
| ULN2002 | ULN2002A | 4-155 | UDN-5722 | SN75477 | 4-97 |
| ULN2003 | ULN2003A | 4-155 | ULN-2001 | ULN2001A | 4-155 |
| ULN2004 | ULN2004A | 4-155 | ULN-2002 | ULN2001A | 4-155 |
| ULN2064 | ULN2064 | 4-163 | ULN-2003 | ULN2003A | 4-155 |
| ULN2065 | ULN2065 | 4-163 | ULN-2004 | ULN2004A | 4-155 |
| ULN2066 | ULN2066 | 4-163 | ULN-2005 | ULN2005A | 4-155 |
| ULN2067 | ULN2067 | 4-163 | ULN-2021 | SN75466 | 4-83 |
| ULN2068 | ULN2068 | 4-169 | ULN-2022 | SN75467 | 4-83 |
| ULN2069 | ULN2069 | 4-169 | ULN-2023 | SN75468 | 4-83 |
| ULN2074 | ULN2074 | 4-175 | ULN-2024 | SN75469 | 4-83 |
| ULN2075 | ULN2075 | 4-175 | ULN-2025 | SN75465 | 4-83 |
| | SUGGESTED | | ULN-2064 | ULN2064 | 4-163 |
| SILICON | TI | PAGE | ULN-2065 | ULN2065 | 4-163 |
| GENERAL | REPLACEMENT | NO. | ULN-2066 | ULN2066 | 4-163 |
| SG2001 | ULN2001A | 4-155 | ULN-2067 | ULN2067 | 4-163 |
| SG2001 | ULN2001A ULN2002A | 4-155 4-155 | ULN-2068 | ULN2068 | 4-169 |
| SG2002 | ULN2003A | 4-155 | ULN-2069 | ULN2069 | 4-169 |
| SG2004 | ULN2003A | 4-155 | ULN-2074 | ULN2074 | 2-175 |
| | | | ULN-2075 | ULN2075 | 2-175 |
| SG2022 | SN75467 | 4-83 | l | | |

 $[\]ensuremath{^{\dagger}}\xspace \text{Consult}$ product data sheet for possible slight product differences.



PERIPHERAL DRIVERS/ACTUATORS CROSS-REFERENCE GUIDE

| UNITRODE | SUGGESTED TI REPLACEMENT | PAGE NO. | | |
|--------------|--------------------------------|--------------|---|--|
| L293 L293 | L293 SN754411 [†] | 4-7 4-109 | | |
| L293D | L293D | 4-11 | * | |
| L293D | SN754410 [†] | 4-103 | | |
| L298 | L298 | 4-15 | | |

[†]Consult product data sheet for possible slight product differences.



| General Information | 1 |
|--|---|
| | |
| Data Transmission and Control Circuits | 2 |
| | |
| Display Drivers | 3 |
| | |
| Peripheral Drivers/Power Actuators | 4 |
| | And description of the second |
| Mechanical Data | 5 |
| | |
| Explanation of Logic Symbols | 6 |

AM26LS31C QUADRUPLE DIFFERENTIAL LINE DRIVER

D2433, JANUARY 1979-REVISED MAY 1990

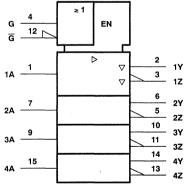
- Meets EIA Standard RS-422-A
- Operates From a Single 5-V Supply
- TTL Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output Enable Inputs

description

The AM26LS31C is a quadruple complementaryoutput line driver designed to meet the requirements of EIA Standard RS-422-A and Federal Standard 1020. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. Lowpower Schottky circuitry reduces power consumption without sacrificing speed.

The AM26LS31C is characterized for operation from 0°C to 70°C.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D, J, OR N PACKAGE (TOP VIEW)

| 1 | | 11 | ì |
|----------|---|----|-------------------------|
| 1A [| 1 | 16 |] v _{cc} |
| 1Y [| 2 | 15 |] 4A |
| 1Z [| 3 | 14 |] 4Y |
| ENABLE G | 4 | 13 |] 4Z |
| 2Z [| 5 | 12 |] ENABLE \overline{G} |
| 2Y [| 6 | 11 |] 3Z |
| 2A 🛚 | 7 | 10 |] 3Y |
| GND [| 8 | 9 |] 3A |
| | | | |

FUNCTION TABLE (EACH DRIVER)

| INPUT | ENA | BLES | OUTPUTS | | |
|-------|-----|------|---------|---|--|
| Α | G | G | Υ | Z | |
| Н | Н | Х | Н | L | |
| L | Н | Х | L | Н | |
| Н | Х | L | Н | L | |
| L | Х | L | L | Н | |
| X | L | Н | z | Z | |

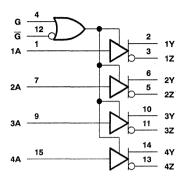
H = high level

L = low level

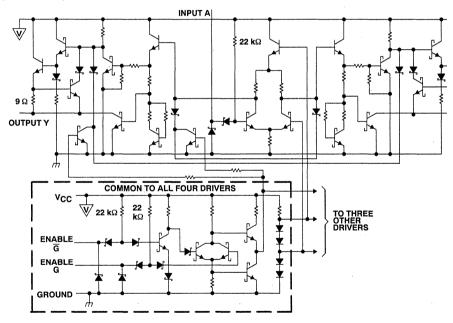
X = irrelevant

Z = high impedance (off)

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | 7 V |
|--|------------------------------|
| Input voltage | |
| Output off-state voltage | 5.5 V |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range | 0 to 70°C |
| Storage temperature range | – 65 to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | ge 260°C |

NOTE 1: All voltage values, except differential output voltage VOD, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | ٧ |
| High-level output current, IOH | | | - 20 | mA |
| Low-level output current, IOL | | | 20 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °Ç |

electrical characteristics over operating free-air temperature range (unless otherwise noted)

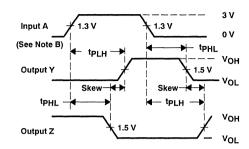
| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|---|---------------------------|---------------------------|------|------|--------|------|
| VIK | Input clamp voltage | V _{CC} = 4.75 V, | I _I = - 18 mA | | | 1.5 | ٧ |
| Voн | High-level output voltage | V _{CC} = 4.75 V, | I _{OH} = - 20 mA | 2.5 | | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = 4.75 V$ | I _{OL} = 20 mA | | | 0.5 | ٧ |
| loz | Off-state (high-impedance-state) output current | V _{CC} = 4.75 V | V _O = 0.5 V | | | - 20 | μΑ |
| | | | V _O = 2.5 V | | | 20 | |
| 11 | Input current at maximum input voltage | V _{CC} = 5.25 V, | V _I = 7 V | | | 0.1 | mA |
| ۱н | High-level input current | V _{CC} = 5.25 V, | V _I = 2.7 V | | | 20 | μΑ |
| I _I L | Low-level input current | V _{CC} = 5.25 V, | V _I = 0.4 V | | | - 0.36 | mA |
| los | Short-circuit output current [‡] | V _{CC} = 5.25 V | | - 30 | | 150 | mA |
| 1cc | Supply current | V _{CC} = 5.25 V, | All output disabled | | 32 | 80 | mA |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

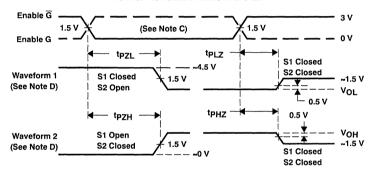
| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|-------------------------|------------------------|------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, | C _L = 30 pF, | See Figure 1, | S1 and S2 open | | | 00 | |
| | low-to-high-level output | | | | | 14 | 20 | ns |
| †PHL | Propagation delay time, | | | | | 14 | 20 | ns |
| | high-to-low-level output | | | | | | | |
| | Output-to-output skew | | | | | 1 | 6 | ns |
| ^t PZH | Output enable time to high level | C _L = 30 pF, | R _L = 75 Ω, | See Figure 1 | | 25 | 40 | ns |
| tPZL | Output enable time to low level | C _L = 30 pF, | R _L =180 Ω, | See Figure 1 | | 37 | 45 | ns |
| tPHZ | Output disable time from high level | C _L = 10 pF, | See Figure 1, | S1 and S2 closed | | 21 | 30 | ns |
| t _{PLZ} | Output disable time from low level | | | | | 23 | 35 | ns |

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

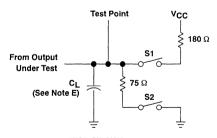


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

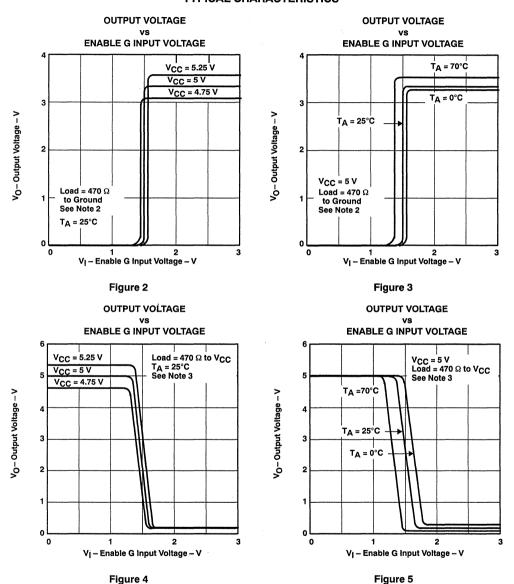
VOLTAGE WAVEFORMS



- **TEST CIRCUIT**
- NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_0 \sim 50 \Omega$, $t_f \leq 15$ ns, and $t_f \leq 6$ ns.
 - B. When measuring propagation delay times and skew, switches S1 and S2 are open.
 - C. Each enable is tested separately.
 - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. C_I includes probe and jig capacitance.

Figure 1. Switching Times

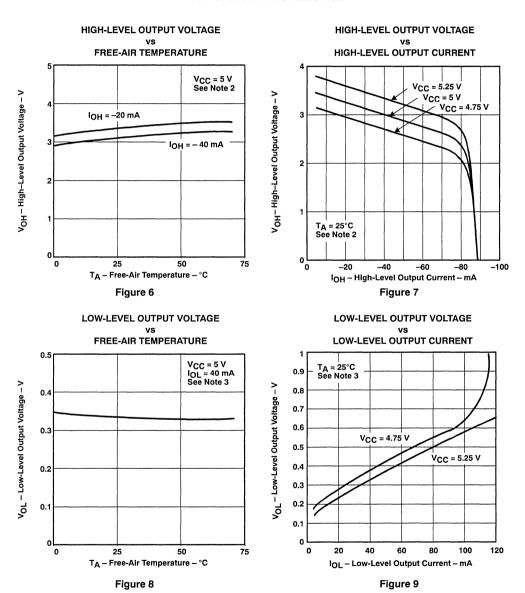




NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

3. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

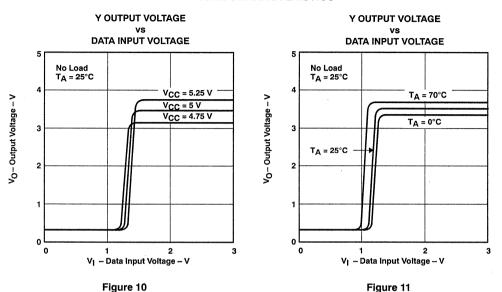




NOTES: 2. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

3. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.





AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM OUADRUPLE DIFFERENTIAL LINE RECEIVERS

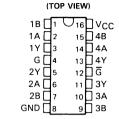
D2434, OCTOBER 1980-REVISED SEPTEMBER 1986

- AM26LS32A Meets EIA Standards RS-422-A and RS-423-A
- AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity
- AM26LS33A Has ±15-V Common-Mode Range With ±500 mV Sensitivity
- Input Hysteresis . . . 50 mV Typical
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- Complementary Output Enable Inputs
- Input Impedance . . . 12 kΩ Min
- Designed to Be Interchangeable With Advanced Micro Devices AM26LS32C and AM26LS33C

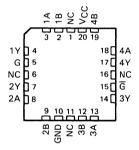
description

The AM26LS32A and AM26LS33A are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

AM26LS32AC, AM26LS33AC . . . D, J, OR N PACKAGE AM26LS32AM, AM26LS33AM . . . J PACKAGE



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

Compared to the AM26LS32C and the AM26LS33C, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and the AM26LS33AM are characterized for operation over the full military temperature range of -55°C to 125°C.

FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENA | BLES | ОИТРИТ |
|-----------------------------------|-----|------|--------|
| INPUT | G | G | OUIPUI |
| V > V | Н | X | Н |
| V _{ID} ≥ V _{TH} | х | L | Н |
| | Н | Х | ? |
| $V_{TL} \leq V_{ID} \leq V_{TH}$ | Х | L | ? |
| V V- | Н | Х | L |
| V _{ID} ≤ V _{TL} | X | L | L |
| X | L | Н | Z |

H = high level, L = low level, X = irrelevant Z = high impedance (off), ? = indeterminate

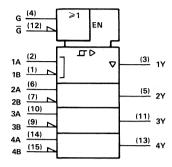


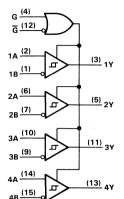
Copyright © 1986, Texas Instruments Incorporated

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

logic symbol†

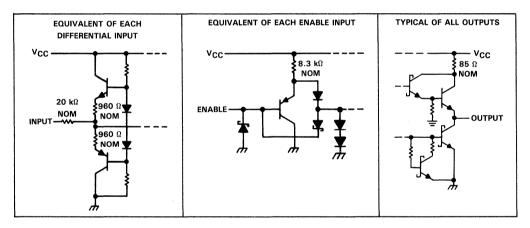
logic diagram (positive logic)





Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM OUADRUPLE DIFFERENTIAL LINE RECEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | AM26LS32AC AM26LS33AC | AM26LS32AM AM26LS33AM | UNIT | | |
|--|----------------|------------------------------|--------------------------|------|--|--|
| Supply voltage, V _{CC} (see Note 1) | | 7 | 7 | V | | |
| Input voltage, any differential input | | ± 25 | ± 25 | V | | |
| Differential input voltage (see Note 2) | | ± 25 | ± 25 | V | | |
| Continuous total power dissipation | | See Dissipation Rating Table | | | | |
| Operating free-air temperature range | | 0 to 70 | -55 to 125 | °C | | |
| Storage temperature range | | -65 to 150 | - 65 to 150 | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or N package | 260 | | °C | | |
| Case temperature for 60 seconds | FK package | | 260 | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | J package | 300 | 300 | °C | | |

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 - 2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | TA = 70°C | TA = 125°C |
|--------------|-----------------------|-----------------|--------------|--------------|
| | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (C-SUFFIX) | 1025 mW | 8.2 mW/°C | 656 mW | - |
| J (M-SUFFIX) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | - |

recommended operating conditions

| | | AM26LS32AC AM26LS32AM AM26LS33AC AM26LS33AM | | UNIT | | | | |
|--|------------------------|--|-----|------|------|-----|------|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, VCC | | 4.75 | 5 | 5.25 | 4.5 | 5 | 5.5 | V |
| High-level input voltage, VIH | | 2 | | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | | | 0.8 | V |
| O | AM26LS32AC, AM26LS32AM | | | ± 7 | | ± 7 | V | |
| Common-mode input voltage, V _{IC} | AM26LS33AC, AM26LS33AM | | | ± 15 | | | ±15 | V |
| High-level output current, IOH | | | | -440 | | | -440 | μΑ |
| Low-level output current, IOL | | | | 8 | | | 8 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | - 55 | | 125 | °C |

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|--------------------|---|---|---------------------------|------------------------|-------|------------------|-------|----------|
| V= | Differential input | Vo = Voumin | I _{OH} = -440 μA | AM26LS32A | | | 0.2 | V |
| VTH | high-threshold voltage | VO = VOHIIIII, | 10H = -440 μA | AM26LS33A | | | 0.5 | V |
| \/ - | Differential input | $V_0 = 0.45 V$ | lo: = 9 mA | AM26LS32A | -0.2‡ | | | V |
| ΛĹΓ | low-threshold voltage | VO = 0.45 V, | IOF - 9 IIIY | AM26LS33A | -0.5‡ | | | ٧ |
| V _{hys} | Hysteresis, V _{T+} - V _{T-} § | | | | | 50 | | mV |
| ViK | Enable input clamp voltage | V _{CC} = MIN, | I _I = -18 mA | | | | -1.5 | ٧ |
| Vall | High-level output voltage | V _{CC} = MIN, | $V_{ID} = 1 V$, | '32AC, '33AC | 2.7 | | | V |
| Vон | riigii-ievei output voitage | $V_{I(\overline{G})} = 0.8 \text{ V},$ | $I_{OH} = -440 \mu A$ | '32AM, '33AM | 2.5 | | | • |
| V | Law level cutnut voltage | V _{CC} = MIN, | $V_{ID} = -1 V$, | I _{OL} = 4 mA | | | 0.4 | V |
| VOL | VOL Low-level output voltage | $V_{I(\overline{G})} = 0.8 \text{ V}$ | | I _{OL} = 8 mA | , | | 0.45 | ٧ |
| la- | Off-state (high-impedance-state) | V _{CC} = MAX | | $V_0 = 2.4 \text{ V}$ | | | 20 | μΑ |
| loz | output current | ACC - MAX | | $V_0 = 0.4 V$ | | | - 20 | μΑ |
| 1. | Line input current | $V_{ } = 15 V,$ | Other input at -10 | V to 15 V | | | 1.2 | mA |
| 11 | Line input current | $V_{ } = -15 V$, | Other input at -15 | V to 10 V | | | - 1.7 | IIIA |
| ¹ I(EN) | Enable input current | V _I = 5.5 V | | | | | 100 | μΑ |
| ΉΗ | High-level enable current | V _I = 2.7 V | | | | | 20 | μΑ |
| lL. | Low-level enable current | V _I = 0.4 V | | | | | -0.36 | mA |
| rį | Input resistance | V _{IC} = -15 V to 15 V, One input to AC ground | | 12 | 15 | | kΩ | |
| los | Short-circuit output current¶ | V _{CC} = MAX | | | -15 | | -85 | mA |
| Icc | Supply current | V _{CC} = MAX, | All outputs disabled | | | 52 | 70 | mA |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C, and V_{IC} = 0.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C

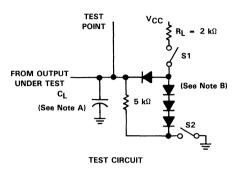
| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|--|--------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | C _i = 15 pF, See Figure 1 | | 20 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | CL = 15 pr, See Figure 1 | | 22 | 35 | ns |
| tPZH | Output enable time to high level | C _I = 15 pF, See Figure 1 | | 17 | 22 | ns |
| tPZL | Output enable time to low level | CL = 15 pr, See Figure 1 | | 20 | 25 | ns |
| tPHZ | Output disable time from high level | C _I = 5 pF, See Figure 1 | | 21 | 30 | ns |
| tPLZ | Output disable time from low level | CL = 5 pr, See Figure 1 | | 30 | 40 | ns |

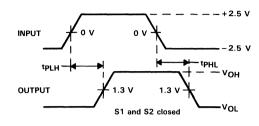
[‡]The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

 $^{^{\}S}$ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} . See Figures 10 and 11.

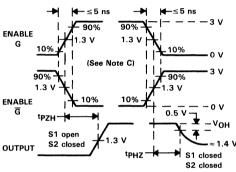
Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

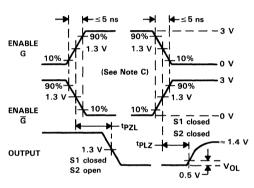
PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS FOR tPLH, tPHL





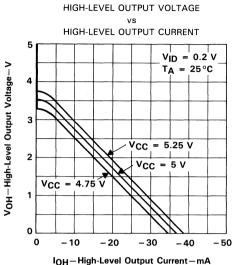
VOLTAGE WAVEFORMS FOR tPHZ, tPZH

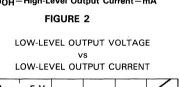
VOLTAGE WAVEFORMS FOR tPLZ, tPZL

NOTES: A. C_L includes probe and jig capacitance.

- B. All diodes are 1N3064 or equivalent.
- C. Enable G is tested with \overline{G} high; \overline{G} is tested with G low.

FIGURE 1





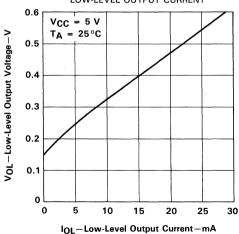
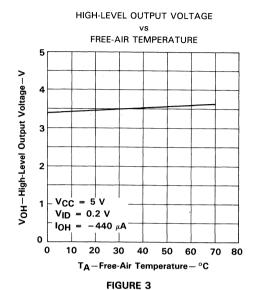


FIGURE 4



TOW-LEVEL OUTPUT VOLTAGE

VS

FREE-AIR TEMPERATURE

0.5

0.4

0.4

0.4

0.7

VCC = 5 V

VID = -0.2 V

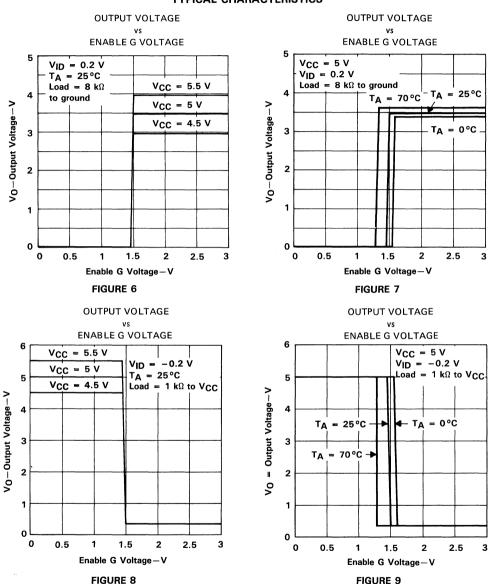
IOL = 8 mA

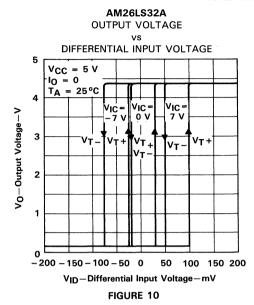
0

FIGURE 5

TA-Free-Air Temperature-°C

10 20 30 40 50 60 70 80





OUTPUT VOLTAGE DIFFERENTIAL INPUT VOLTAGE 5 $V_{CC} = 5 V$ $l_0 = 0$ $T_A = 25$ °C V_{IC}= Vcc= Vic -4 15 V - 15 V 0 V Vo-Output Voltage-V 3 Vτ ٧Ť ۷т – VT+ V_T+ 2 -200-150-100-50 0 100 150 200 50

VID-Differential Input Voltage-mV

FIGURE 11

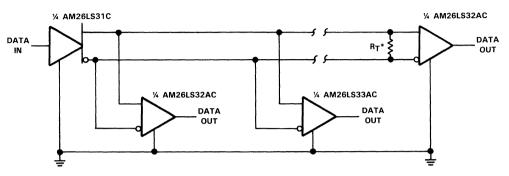
AM26LS33A

INPUT CURRENT INPUT VOLTAGE 3 2 -Input Current-mA 1 requirements of paragraph unshaded area shows -422-A and RS-423-A 0 of EIA Standards 61 1cc - 1 **VCC** -2 -3 -4 -25-20-15-10-5 0 5 10 15 20 25

V_I-Input Voltage-V FIGURE 12

AM26LS32AM, AM26LS33AM, AM26LS32AC, AM26LS33AC QUADRUPLE DIFFERENTIAL LINE RECEIVERS

APPLICATION INFORMATION



^{*}RT equals the characteristic impedance of the line.

FIGURE 13. CIRCUIT WITH MULTIPLE RECEIVERS

AM26S10C, AM26S11C QUADRUPLE BUS TRANSCEIVERS

9∏ 3B

D2298. JANUARY 1977-REVISED MAY 1990

- Schottky Circuitry for High Speed, Typical Propagation Delay Time . . . 12 ns
- Drivers Feature Open-Collector Outputs for Party-Line (Data Bus) Operation
- Driver Outputs Can Sink 100 mA at 0.8 V Maximum
- P-N-P Inputs for Minimal Input Loading
- Designed to Be Interchangeable With Advanced Micro Devices AM26S10 and AM26S11

(TOP VIEW) GND II 716 VCC 1B 15 AB 14 4R 1R 🗍 3 1D 13 4D 2D П 12 S 2R ∏6 11∏ 3D 2В Пл 10 3R

GND ∏8

AM26S10C, AM26S11C . . . D. J. OR N PACKAGE

description

The AM26S10 and AM26S11 are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use p-n-p transistors to reduce the input loading.

The driver of the AM26S10 is inverting; the driver of the AM26S11 is noninverting. Each device has two ground connections for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10C and AM26S11C are characterized for operation over the temperature range of $0\,^{\circ}$ C to $70\,^{\circ}$ C.

AM26S10 FUNCTION TABLE (TRANSMITTING)

| INPUTS | | OUTPUTS | | |
|--------|---|---------|---|--|
| S | D | В | R | |
| L | Н | L | Н | |
| -L | L | Н | L | |

AM26S11 FUNCTION TABLE (TRANSMITTING)

| INPUTS | | OUT | PUTS |
|--------|---|-----|------|
| S | D | В | R |
| L | Н | Н | L |
| L | L | L | н |

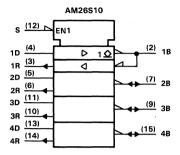
AM26S10 AND AM26S11 FUNCTION TABLE (RECEIVING)

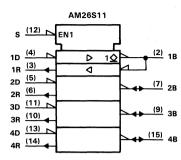
| | INPUTS | | OUTPUT |
|---|--------|---|--------|
| S | В | D | R |
| Н | Н | Х | L |
| Н | Ł | X | н |

H = high level, L = low level, X = irrelevant

AM26S10C, AM26S11C QUADRUPLE BUS TRANSCEIVERS

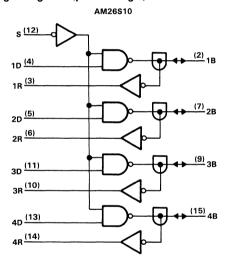
logic symbols†

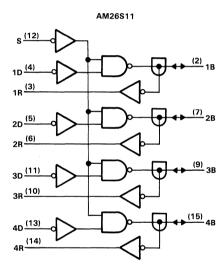




[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





schematic (each transceiver) 110 Ω NOM 2 kΩ NOM AM26S11 AM26S10 GND 2.7 kΩ NOM COMMON CIRCUITRY TO THREE OTHER DRIVERS TO ONE OTHER TO TWO RECEIVER RECEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range, VCC (see Note 1) | $-0.5\ V$ to $7\ V$ |
|--|--|
| Driver or strobe input voltage range | 0.5 V to 5.5 V |
| Bus voltage range, driver output off | 0.5 V to 5.25 V |
| Driver or strobe input current range | 30 mA to 5 mA |
| Driver output current | |
| Receiver output current | 30 mA |
| Continuous total power dissipation See Dis- | sipation Rating Table |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | . -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C |

NOTE 1: All voltage values are with respect to network ground terminals connected together.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mw |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | M | N NOM | MAX | UNIT |
|--|---|-----|-------|------|------|
| Supply voltage, V _{CC} | | 4.7 | 5 5 | 5.25 | V |
| High level input veltage V | D or S | | 2 | | v |
| High-level input voltage, VIH | В | 2.2 | 5 | | V |
| Low-level input voltage, V _{IL} | D or S | | | 0.8 | V |
| | В | | | 1.75 | |
| Receiver high-level output current, IOH | Receiver high-level output current, IOH | | | - 1 | mA |
| Low-level output current, IOL | Driver | | | 100 | ^ |
| | Receiver | | | 20 | mA |
| Operating free-air temperature, TA | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

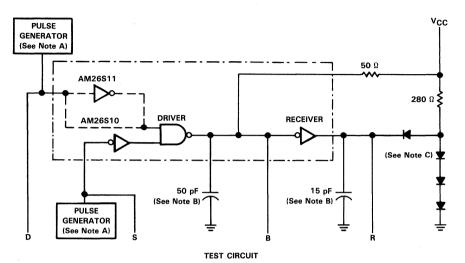
| | PARAMETER | | TES | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-----------------|---|-----------|---|-------------------------|--------------------------|----------|------------------|-------|---------------------------|
| V _{IK} | Input clamp voltage | D or S | $V_{CC} = 4.75 V,$ | I _J = -18 mA | | | | -1.2 | V |
| V _{OH} | High-level output voltage | R | $V_{CC} = 4.75 \text{ V},$ $I_{OH} = -1 \text{ mA}$ | V _{IH} = 2 V, | V _{IL} = 0.8 V, | 2.7 | 3.4 | | V |
| | | R | V 4.75.V | | I _{OL} = 20 mA | | | 0.5 | 5 5 V 7 B O O μA O O O μA |
| 1/ | Law lavel entent veltage | | $V_{CC} = 4.75 \text{ V},$ | | I _{OL} = 40 mA | | 0.33 | 0.5 | ., |
| V_{OL} | _ow-level output voltage | В | $V_{H} = 2 V,$ $V_{H} = 0.8 V$ | | I _{OL} = 70 mA | | 0.42 | 0.7 | V |
| | | | VIL = 0.8 V | | I _{OL} = 100 mA | 0.51 0.8 | | | |
| | | | V 2 V | $V_{CC} = 5.25 V$, | $V_0 = 0.8 V$ | | | - 50 | |
| IO(off) | Off-state output current | В | $V_{IH} = 2 V,$ $V_{IL} = 0.8 V$ | $V_{CC} = 5.25 V$, | $V_0 = 4.5 \text{ V}$ | | | 100 | μΑ |
| | | | VIL = 0.6 V | $V_{CC} = 0$, | $V_0 = 4.5 V$ | | | 100 | |
| 1 | High level input surrent | D | VCC = 5.25 V, | V: - 27V | | | | 30 | ^ |
| lН | High-level input current | S | vCC = 5.25 v, | V) = 2.7 V | | | | 20 | μΑ |
| ij | Input current at maximum input voltage | D or S | $V_{CC} = 5.25 V,$ | V ₁ = 5.5 V | | | | 100 | μΑ |
| | mpar vertage | D | | | | | | 0.54 | |
| ΙL | Low-level input current | S | $V_{CC} = 5.25 V,$ | $V_I = 0.4 V$ | | | | -0.36 | mA |
| los | Short-circuit output current [‡] | R | V _{CC} = 5.25 V | | | - 18 | | - 60 | mA |
| 1 | Complete | | $V_{CC} = 5.25 V_{r}$ | Strobe at 0 V, | No load, | | 45 | 70 | ^ |
| ICC | Supply current | | All driver output | s low | | | | 80 | mA |

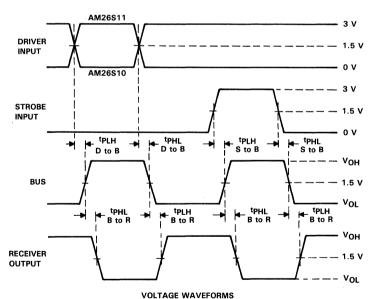
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | то | TEST | AM26S10 AM26S1 | | | 1 | UNIT | | |
|--|---|----------------------|--------------|----------------|-----|-----|-----|------|-----|-----|
| | | FROM TO CONDITIONS N | | MIN | TYP | MAX | MIN | TYP | MAX | ONT |
| tpLH Propagation delay time, low-to-high-level output | D | В | | | 10 | 15 | | 12 | 19 | |
| tpHL Propagation delay time, high-to-low-level output | | l ^D | | | 10 | 15 | | 12 | 19 | ns |
| tpLH Propagation delay time, low-to-high-level output | s | В | | | 14 | 18 | | 15 | 20 | |
| tphL Propagation delay time, high-to-low-level output |] | | C Fi 1 | | 13 | 18 | | 14 | 20 | ns |
| tpLH Propagation delay time, low-to-high-level output | В | R | See Figure 1 | | 10 | 15 | | 10 | 15 | |
| tpHL Propagation delay time, high-to-low-level output | | n | | | 10 | 15 | | 10 | 15 | ns |
| t _{TLH} Transition time, low-to-high-level output | | В | ! | 4 | 10 | | 4 | 10 | | |
| t _{THL} Transition time, high-to-low-level output | | | | 2 | 4 | | 2 | 4 | | ns |

 $^{^{\}dagger}$ All typical values are at T_A = 25 °C and V_{CC} = 5 V. ‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generators have the following characteristics: Z $_0$ = 50 Ω , t $_r$ = 10 \pm 5 ns.

- B. Includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

FIGURE 1



APPLICATION INFORMATION

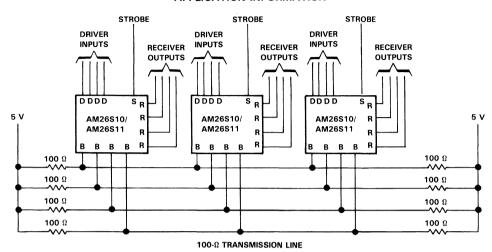


FIGURE 2. PARTY-LINE SYSTEM

D3058, NOVEMBER 1987-REVISED DECEMBER 1988

| ECL Control Inputs | D OR N PACKAGE (TOP VIEW) |
|--|------------------------------|
| 3-State Outputs | у Г. П. у |
| 10K ECL Input Compatible | V _{EE} U¹ |
| Package Options Include Plastic "Small | D1 ☐3 14 ☐ Ō1 |
| Outline" Package and Standard Plastic | D2 |
| 300-mil DIPs | D3 <u>□</u> 5 12 <u>□</u> 3 |
| Direct Replacement for National | $D4 \sqcup 6$ 11 $\sqcup Q4$ |
| Semiconductor DP8480 | Œ <u></u> 7 10 <u></u> |
| Contractor Di C-100 | GND [[8 9] GND |

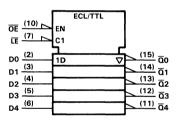
description

This circuit translates ECL input levels to TTL output levels and provides an inverting transparent latch. The 3-state outputs are designed to drive highly capacitive loads. All inputs operate at ECL levels.

If Latch Enable (\overline{LE}) is low, the latches are transparent and the \overline{Q} outputs follow the complement of the D inputs. If \overline{LE} is high, the outputs are latched. If output enable (\overline{OE}) is high, the outputs are in the high-impedance state, as they are during power up and power down.

The DP8480 is characterized for operation from 0°C to 75°C.

logic symbol†

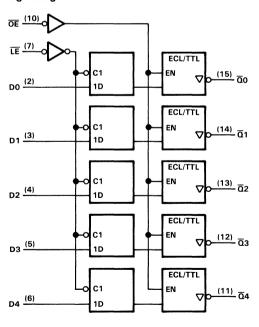


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH LATCH/TRANSLATOR)

| ŌĒ | ΙĒ | D | ā |
|----|----|---|----------------|
| Н | Х | Х | Z |
| L | L | L | Н |
| L | L | Н | L |
| L | н | X | a _o |

logic diagram





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC |
|--|
| Supply voltage, VEE8 V |
| Input voltage, VI 0 V to VEE |
| Output voltage, VO |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 75°C POWER RATING |
|---------|--------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 570 mW |
| N | 1150 mW | 9.2 mW/°C | 690 mW |

recommended operating conditions

| | | MIN | NOM MAX | UNIT |
|--|-----------------------|---------|-------------|------|
| Supply voltage, V _{CC} | | 4.5 | 5 5.5 | V |
| Supply voltage, VEE | | -4.68 - | -5.20 -5.72 | V |
| High level input valtage. V. | T _A = 0°C | -1145 | -840 | |
| High-level input voltage, V _{IH} (see Note 1) | T _A = 25°C | -1105 | -810 | m∨ |
| | T _A = 75°C | - 1045 | - 720 | |
| Low level input valtage Vo | T _A = 0°C | - 1870 | - 1490 | |
| Low-level input voltage, V _{IL} (see Note 1) | T _A = 25°C | - 1850 | - 1475 | m∨ |
| (see Note 1) | $T_A = 75$ °C | - 1830 | - 1450 | 1 |
| Pulse duration, LE low, tw (see Fig | 5 | | ns | |
| Setup time, data before $\overline{\text{LE}}$ [†] , t _{SU} (see Figure 1) | | 3 | | ns |
| Hold time, data after LEt, th (see Figure 1) | | 3 | | ns |
| Operating free-air temperature, TA | | | 75 | °C |

NOTE 1: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------|---|---------------------------------------|-------|------------------|------|------|
| ∨он | High-level output voltage | I _{OH} = -10 mA | VCC-2 | 2 | | ٧ |
| VOL | Low-level output voltage | I _{OL} = 12 mA | | 0.2 | 0.5 | ٧ |
| ΊΗ | High level input current | V _{IH} = V _{IH} max | | 75 | 350 | μΑ |
| կլ | Low-level input current | V _{IL} = V _{IL} min | | 50 | 85 | μΑ |
| IOHS | High-state short-circuit output current | V _{OHS} = 0, See Note 2 | - 70 | - 150 | | mA |
| lols | Low-state short-circuit output current | V _{OLS} = 2:5 V, See Note 2 | 70 | 150 | | mA |
| loz | High-impedance state output current | $V_0 = 0 \text{ to } 5 \text{ V}$ | | ± 1 | ±50 | μΑ |
| Icc | Supply current from V _{CC} | Outputs open, Inputs = VIL | | 16 | 35 | mA |
| ¹ EE | Supply current from VEE | Outputs open, Inputs = VIL | | - 30 | - 50 | mA |



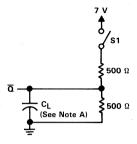
 $^{^{\}dagger}$ Typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = $25\,^{\circ}$ C. NOTE 2: During testing of I_{OHS} or I_{OLS}, only one output should be tested at a time and the current should be limited to a maximum of ±120 mA.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------|--|-----------------|-----|------------------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output from $\overline{\text{LE}}$ input | | 4 | 10 | 15 | ns |
| tPHL | Propagation delay time, high-to-low-level output from $\overline{\text{LE}}$ input | | 4 | 11 | 15 | ns |
| tPLH | Propagation delay time, low-to-high-level output from D input | $C_L = 50 pF$, | 3.5 | 10 | 15 | ns |
| tPHL | Propagation delay time, high-to-low-level output from D input | See Figure 1 | 3.5 | 11 | 15 | ns |
| t _{en} | Output enable time from OE input | | 6 | 12 | 25 | ns |
| tdis | Output disable time from OE input | | 4.5 | 8 | 22 | ns |

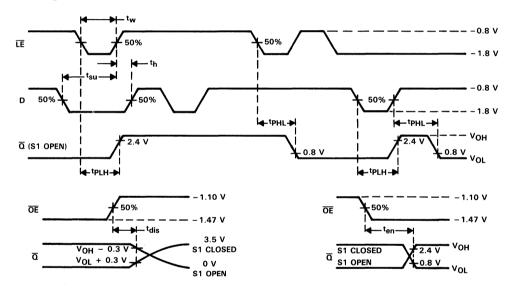
 $^{^{\}dagger}$ Typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25 °C, and with all channels switched simultaneously.

PARAMETER MEASUREMENT INFORMATION



OUTPUT LOAD CIRCUIT

NOTE A: C_L includes probe and jig capacitance.



NOTE B: ECL input rise times and fall time are 2 ns ± 0.2 ns from 20% to 80%.

FIGURE 1. SWITCHING CHARACTERISTICS

D3059, NOVEMBER 1987-REVISED AUGUST 1989

| ECL Control Inputs | D OR N PACKAGE |
|--|--------------------|
| 10K ECL Compatible | (TOP VIEW) |
| Propagation Delay 4 ns Typ | V _{EE} ∐¹ |
| Package Options Include Plastic "Small | Ō1 ☐3 14 ☐ D1 |
| Outline" Package and Standard Plastic | <u>0</u> 2 |
| 300-mil DIPs | <u>ā</u> 3 |
| Direct Replacement for National | Ō4 ☐6 11 ☐ D4 |
| Semiconductor DP8481 | OE ∐7 10 [☐ [Ē |
| Semiconductor Di 6461 | GND U8 9 ☐ GND |

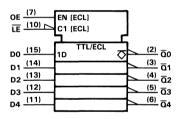
description

This circuit translates TTL input levels to ECL output levels and provides a 5-bit transparent latch. The outputs are gated by Output Enable (OE) and can be wire-OR connected. The Latch Enable (LE) and OE inputs are ECL.

If Latch Enable (\overline{LE}) is low, the latches are transparent and the \overline{Q} outputs follow the complement of the D inputs. If LE is high, the outputs are latched. If Output Enable (OE) is low, the outputs are forced to the low level.

The DP8481 is characterized for operation from 0°C to 75°C.

logic symbol†

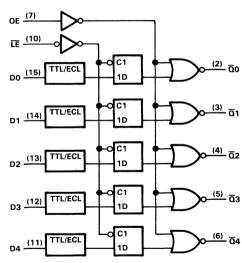


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH LATCH/TRANSLATOR)

| OE | LE | D | ā |
|----|----|---|----|
| Н | L | Н | L |
| Н | L | L | Н |
| н | н | Х | 00 |
| L | X | Х | L |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} |
|--|
| Supply voltage, VEE |
| Input voltage, V _I : OE or $\overline{\text{LE}}$ input |
| D inputs |
| Output current, IO |
| Continuous total dissipation |
| Operating temperature range, T _A 0°C to 75°C |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 75°C POWER RATING |
|---------|--------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 570 mW |
| N | 1150 mW | 9.2 mW/°C | 690 mW |

recommended operating conditions

| | | | | | MIN | NOM | MAX | UNIT |
|---------------------------------------|----------------------------|-----------------------|----------------|---|--------|-------|--------|------|
| Supply voltage, V _{CC} | | | | | | 5 | 5.5 | V |
| Supply voltage, V | EE | | : | | -4.68 | -5.20 | -5.72 | ٧ |
| High-level input v | oltage, V _{IH} (| TTL-level D inputs) | | | 2 | | | V |
| Low-level input v | oltage, V _{IL} (T | TL-level D inputs) | | | | | 0.8 | ٧ |
| High-level input v | oltage, V _{IH} | $T_A = 0$ °C | | | -1145 | | -840 | |
| (ECL-level OE and LE inputs) | | T _A = 25°C | | | - 1105 | | -810 | mV |
| (see Note 1) | | $T_A = 75$ °C | | | -1045 | | - 720 | |
| · · · · · · · · · · · · · · · · · · · | | $T_A = 0$ °C | | | - 1870 | | - 1490 | |
| | | T _A = 25°C | | | - 1850 | | - 1475 | mV |
| (see Note 1) | Note 1) . TA = 75°C | | | | - 1830 | | - 1450 | |
| Pulse duration, LE low, tw | | (see Figure 1) | | 5 | | | ns | |
| Setup time, t _{su} | Data before | <u>LE</u> ↑ | (see Figure 1) | | 5 | | | |
| | Data before | OE† (see Note 2) | (see Figure 1) | | 5.5 | | | ns |
| Hold time, data after LEt, th | | (see Figure 1) | | 1 | | | ns | |
| Operating free-air | temperature | . T _A | | | 0 | | 75 | °C |

- NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.
 - 2. This setup time applies when operating in the transparent mode (LE is low) and it is necessary that valid data be available at the output immediately after the outputs are enabled.

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST COND | DITIONS | MIN | TYP [†] MAX | UNIT |
|-----------|--|---------------------------|----------------------------|----------------------------------|--------|----------------------|------|
| VIK | Input clamp voltage | D0-D4 | I _I = -12 mA | $I_{\parallel} = -12 \text{ mA}$ | | -0.8 -1.2 | V |
| | High-level input Do | | V _I = 2.5 V | | | 1 40 | μΑ |
| ΊΗ | current | OE, LE | $V_1 = -0.8 \text{ V}$ | | | 200 | μΑ |
| 1 | Low-level input | D0-D4 | $V_{ } = 0.5 V$ | | | -50 -200 | ^ |
| ΊL | current | OE,LE | V _I = -1.8 V | | | 150 | μΑ |
| | Illah laval avana valena | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 0$ °C | - 1000 | -840 | |
| VOH | High-level output voltage | | $V_{EE} = -5.2 \text{ V},$ | T _A = 25 °C | -960 | -810 | mV |
| | (see Notes 1 and 3) | Ī | $V_{EE} = -5.2 \text{ V},$ | T _A = 75°C | - 900 | -720 | |
| | Critical high-level | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 0$ °C | - 1020 | | |
| VOHC | output voltage (see Notes 1 and 3) | | $V_{EE} = -5.2 \text{ V},$ | T _A = 25°C | - 980 | | mV |
| | | | $V_{EE} = -5.2 \text{ V},$ | T _A = 75°C | -920 | | |
| | Low-level output voltage (see Notes 1 and 3) | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 0$ °C | - 1870 | - 1665 | |
| VOL | | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 25$ °C | - 1850 | -1650 | mV |
| | | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 75$ °C | - 1830 | -1625 | |
| | Cuiti and law law at a second | | $V_{EE} = -5.2 \text{ V},$ | $T_A = 0$ °C | | -1645 | |
| VOLC | · | Critical low-level output | | T _A = 25°C | | -1630 | mV |
| | voltage (see Notes 1 and 3) | | $V_{EE} = -5.2 \text{ V},$ | T _A = 75°C | | - 1605 | |
| Icc | Supply current from VCC | | V _{CC} = 5.5 V | | | 20 | mA |
| IEE | Supply current from VEE | | $V_{EE} = -5.7 \text{ V}$ | | | - 90 | mA |

NOTES: 1. The algebraic convention, in which the least positive (most negative) value is designated one minimum, is used in this data sheet for logic levels only.

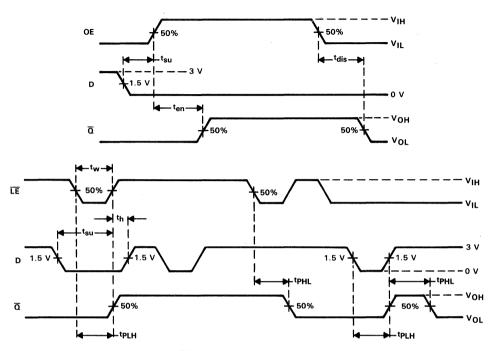
3. V_{OH} and V_{OL} are tested using the "outer-limit" values V_{IH} max and V_{IL} min. The "critical" values V_{OHC} and V_{OLC} are tested using the "inner-limit" values V_{IH} min and V_{IL} max. The latter values ensure the noise margins of 155 mV high and 125 mV low associated with 10K ECL.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------|--|---|-----|------------------|-----|------|
| tPLH | Propagation delay time, low-to-high level output from LE input | | 1.5 | 4 | 6 | ns |
| tPHL | Propagation delay time, high-to-low-level output from LE input | | 1.5 | 4 | 6 | ns |
| tPLH | Propagation delay time, low-to-high-level output from D input | $R_L = 50 \Omega \text{ to } -2 \text{ V},$ | 2.5 | 4 | 7.5 | ns |
| tPHL | Propagation delay time, high-to-low-level output from D input | See Figure 1 | 2.5 | 4 | 7.5 | ns |
| t _{en} | Output enable time from OE input | | 1 | 3 | 4 | ns |
| tdis | Output disable time from OE input | | 1 | 3 | 4 | ns |

 † Typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25 °C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: ECL input rise and fall times at OE and $\overline{\text{LE}}$ are 2 ns ± 0.2 ns from 20% to 80%. TTL input rise and fall times at D inputs are 3 ns maximum measured between 10% and 90%.

FIGURE 1. SWITCHING TIME WAVEFORMS

LT1030 QUAD LOW-POWER LINE DRIVER

D3297, APRIL 1989-REVISED JULY 1989

- Low Supply Voltage ... ±5 V to ±15 V
- Supply Current ... 500 μA Typ
- Zero Supply Current When Shut Down
- Outputs Can Be Driven ± 30 V
- Output Open When Off (3-State)
- 10-mA Output Drive
- Output of Several Devices Can Be Paralleled
- Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Std RS-232-C)
- Designed to Be Interchangeable With Linear Technology LT1030

description

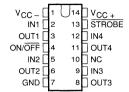
The LT1030 is an EIA-232 line driver that operates over a ± 5 -V to ± 15 -V supply voltage range on low supply current. The device can be shut down to zero supply current. Current-limiting fully protects the outputs from externally applied voltages of ± 30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply voltage requirements are minimized.

A major advantage of the LT1030 is the highimpedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The device can be used as an EIA-232 driver, micropower interface, or level translator, among others.

The LT1030 is characterized for operation from 0° C to 70° C.

LT1030 ... D OR N PACKAGE (TOP VIEW)



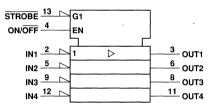
NC - No internal connection

AVAILABLE OPTIONS

| | PACKAGE | | | | |
|-------------|---------------|-------------|--|--|--|
| TA | SMALL OUTLINE | PLASTIC DIP | | | |
| | (D) | (N) | | | |
| 0°C to 70°C | LT1030CD | LT1030CN | | | |

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

pin descriptions

| PIN | | DESCRIPTION |
|-------------------|-------|---|
| NAME | NO | DESCRIPTION |
| GND | 7 | Ground pin. |
| IN1, IN2, | 2, 5, | Logic inputs. Operate properly on TTL or CMOS levels. Output valid from $V_1 = V_{CC-} + 2 V$ to 15 V. Connect to |
| IN3, IN4 | 9, 12 | 5 V when not used. |
| ON/OFF | 4 | Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5 V and 10 V. If V _{IL} |
| ON/OFF | 4 | is at or near 0.8 V, significant settling time may be required. |
| OUT1, OUT2, | 3, 6, | Line deliver autorite |
| OUT3, OUT 4 | 8, 11 | Line driver outputs. |
| STROBE | 13 | Forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately $2 k\Omega$ to GND. Leave open |
| STROBE | 13 | when not used. |
| V _{CC+} | 14 | Positive supply. |
| V _{CC} - | 1 | Negative supply. |

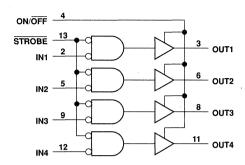
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LT1030 OUAD LOW-POWER LINE DRIVER

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range, V _{CC+} (see Note 1) |
|--|
| Supply voltage range, V _{CC} 0 V to -15 V |
| Input voltage range, logic inputs |
| Input voltage range, ON/OFF pin |
| Output voltage range (any output) |
| Duration of output short-circuit at (or below) 25°C (to ±30 V, see Note 2) unlimited |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range, T _A 0°C to 70°C |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values, except differential voltages, are with respect to the GND terminal.

The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Supply voltage, V _{CC+} | 5 | | 15 | ٧ |
| Supply voltage, V _{CC} | -5 | | -15 | V |
| High-level input voltage, VIH (see Note 3) | 2 | | 15 | V |
| Low-level input voltage, V _{IL} (see Note 3) | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

NOTE 3: These V_{IH} and V_{IL} specifications apply only for inputs IN1-IN4. For operating levels for ON/OFF, see Figure 2.

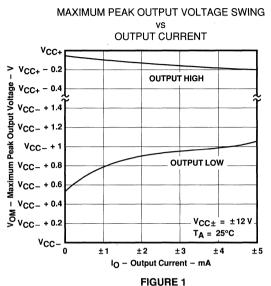
electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 5 \text{ V to } \pm 15 \text{ V (unless otherwise noted)}$

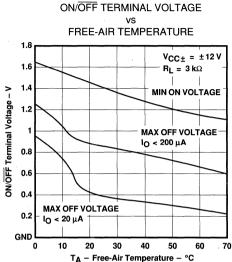
| | PARAMETER | TEST CONDITIONS | MIN TYP† MAX | UNIT |
|----------------------|--|--|--|------|
| V _{OM+} | Maximum positive peak output voltage swing | $I_{O} = -2 \text{ mA}, \qquad T_{A} = 25^{\circ}\text{C}$ | V _{CC+} - 0.3 V _{CC+} - 0.1 | V |
| V _{OM} - | Maximum negative peak output voltage swing | $I_0 = 2 \text{ mA}$. $I_A = 25 ^{\circ}\text{C}$ | | V |
| lн | High-level input current | $V_1 \ge 2 V$, $T_A = 25^{\circ}C$ | 2 20 | μА |
| [[]]L | Low-level input current | $V_1 \le 0.8 \text{V}, \qquad T_A = 25^{\circ}\text{C}$ | 10 20 | μА |
| łį | ON/OFF terminal current | $V_{l} = 0$ $V_{l} = 5 V$ | -0.1 -10 30 65 | μА |
| 10 | Output current | T _A ≈ 25°C | 5 12 | mA |
| loz | Off-state output current | $V_{O} = \pm 30 \text{ V}, T_{A} = 25^{\circ}\text{C}$ | ±2 ±100 | μА |
| lcc | Supply current (all outputs low) | $V_1 \ge at 2.4 V$, $I_0 = 0$ | 500 1000 | μΑ |
| I _{CC(off)} | Off-state supply current | ON/OFF at 0.4 V ON/OFF at 0.1 V | 10 10 150 | μА |

operating characteristics, $V_{CC\pm} = \pm 5 \text{ V to } \pm 15 \text{ V}$, $T_A = 25^{\circ}\text{C}$

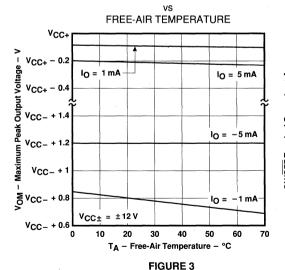
| PARAMETER | | TEST CONDITIONS | | | TYP† | MAX | UNIT |] |
|-----------|------------------|---------------------|------------------------|---|------|-----|------|---|
| SR | Driver slew rate | $R_L = 3 k\Omega$, | C _L = 51 pF | 4 | 15 | 30 | V/µs | 1 |

 $^{^{\}dagger}All$ typical values are at VCC± = ±12 V, TA = 25°C.





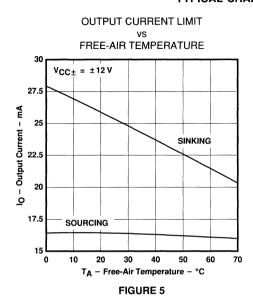
MAXIMUM PEAK OUTPUT VOLTAGE SWING

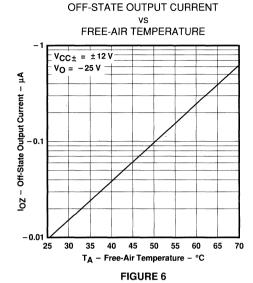


ON/OFF TERMINAL VOLTAGE 140 V_{CC±} = ±12 V TA = 25°C 120 ON/OFF Terminal Current - μΑ 100 80 60 40 20 0 -20 0 2.5 7.5 12.5

FIGURE 2

ON/OFF TERMINAL CURRENT





OFF-STATE SUPPLY CURRENT

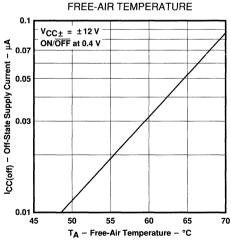
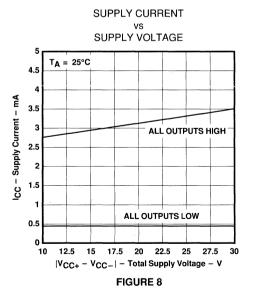
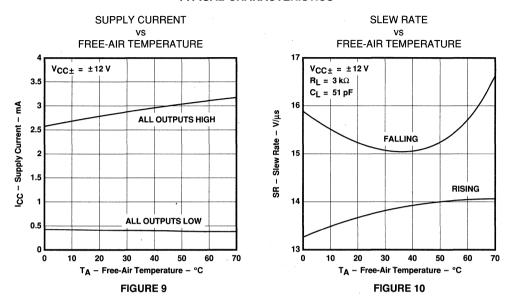


FIGURE 7





TYPICAL APPLICATION DATA

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V_{CC_+} to ground if the V_{CC_-} terminal is open-circuited or pulled above ground. If this is possible, connecting a diode from V_{CC_-} to ground will prevent the high-current state. Any low-cost diode can be used (see Figure 11).

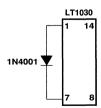


FIGURE 11. CONNECTING A DIODE FROM V_{CC-} TO GROUND



MAX232 DUAL EIA-232 DRIVER/RECEIVER

D3120, FEBRUARY 1989-REVISED JUNE 1989

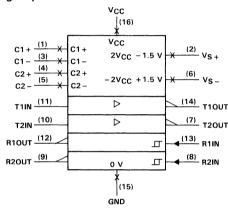
| Operates with Single 5-V Power Supply | D OR N PACKAGE |
|--|-----------------------------------|
| LinBiCMOS™ Process Technology | (TOP VIEW) |
| Two Drivers and Two Receivers | C1 + U1 U16 VCC VS + U2 15 GND |
| ● ±30-V Input Levels | C1 – 🗍 3 14 🗍 T10UT |
| Low Supply Current 8 mA Typ | C2 + |
| Meets ANSI/EIA-232-D-1986 Specifications (Revision of EIA Standard RS-232-C) | VS |
| Designed to be interested until Marriage | R2IN 🛛 8 9 🗍 R2OUT |

- Designed to be Interchangeable with Maxim MAX232
- Applications
 - EIA-232 Interface
 - Battery-Powered Systems
 - Terminals
 - Modems
 - Computers

description

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

logic symbol†



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Input supply voltage, VCC (see Note 1) | 0.3 V to 6 V |
|--|--|
| Positive output supply voltage, V _S + | |
| Negative output supply voltage, Vs | 0.3 V to -15 V |
| Input voltage range: Driver | 0.3 V to V _{CC} + 0.3 V |
| Receiver | ±30 V |
| Output voltage range: T10UT, T20UT | . V_{S-} - 0.3 V to V_{S+} + 0.3 V |
| R10UT, R20UT | 0.3 V to V _{CC} + 0.3 V |
| Short-circuit duration: V _{S+} | 30 s |
| V _S | 30 s |
| T10UT, T20UT | unlimited |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTE 1: All voltage values are with respect to network ground terminal.

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recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-----|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | V |
| High-level input voltage, VIH (T1IN, T2IN) | 2 | | | V |
| Low-level input voltage, V _{IL} (T1IN, T2IN) | | | 0.8 | V |
| Receiver input voltage, R1IN, R2IN | | | ±30 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| | PARAMATER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|--------------|--|-----|------------------|-----|------|
| | High-level output voltage | T10UT, T20UT | $R_L = 3 k\Omega$ to GND | 5 | 7 | | · V |
| Vон | nigh-level output voltage | R1OUT, R2OUT | IOH = -1 mA | 3.5 | | | V |
| V | Low-level output voltage [‡] | T10UT, T20UT | $R_L = 3 k\Omega$ to GND | | -7 | - 5 | V |
| VOL | Low-level output voltage | R10UT, R20UT | I _{OL} = 3.2 mA | | | 0.4 | • |
| V _{T+} | Receiver positive-going input threshold voltage | R1IN, R2IN | V _{CC} = 5 V, T _A = 25°C | | 1.7 | 2.4 | V |
| V _T _ | Receiver negative-going input threshold voltage | R1IN, R2IN | V _{CC} = 5 V, T _A = 25°C | 0.8 | 1.2 | | ٧ |
| V _{hys} | Input hysteresis | R1IN, R2IN | V _{CC} = 5 V | 0.2 | 0.5 | 1 | kΩ |
| rį | Receiver input resistance | R1IN, R2IN | V _{CC} = 5 V, T _A = 25°C | 3 | 5 | 7 | kΩ |
| ro | Output resistance | T10UT, T20UT | $V_{S+} = V_{S-} = 0, V_{O} = \pm 2 V$ | 300 | | | Ω |
| los§ | Short-circuit output current | T10UT, T20UT | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | | ±10 | | mA |
| lis | Short-circuit input current | T1IN, T2IN | V _I = 0 | | | 200 | μΑ |
| lcc | Supply current | | V _{CC} = 5.5 V, All outputs open, T _A = 25 °C | | 8 | 10 | mA |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|----------------------------------|--|-----|-----|-----|------|
| to | Receiver propagation delay time, | Soo Figure 2 | | 500 | | ns |
| ^t PLH(R) | low-to-high-level output | See Figure 2 | | 500 | | 110 |
| | Receiver propagation delay time, | See Figure 2 | | 500 | | |
| tPHL(R) | high-to-low-level output | See Figure 2 | | 500 | | ns |
| SR | Driver slew rate | $R_L = 3 k\Omega$ to 7 k Ω , See Figure 3 | | | 30 | V/μs |
| SR(tr) | Driver transition region | See Figure 4 | | 2 | | V/μs |
| on(tr) | slew rate | See Figure 4 | | 3 | | V/μS |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

[§]Not more than one output should be shorted at a time.

TYPICAL APPLICATION DATA

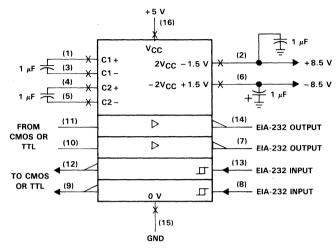
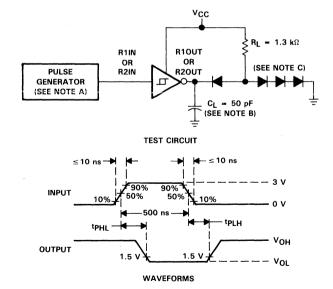


FIGURE 1. TYPICAL OPERATING CIRCUIT

PARAMETER MEASUREMENT INFORMATION



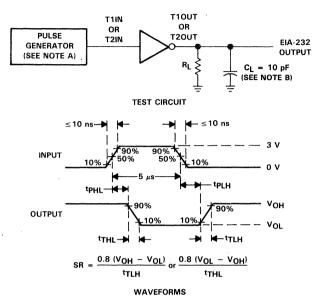
NOTES: A. The pulse generator has the following characteristics: $Z_{OUT} = 50 \Omega$, Duty Cycle $\leq 50\%$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

FIGURE 2. RECEIVER TEST CIRCUIT AND WAVEFORMS FOR tPHL AND tPLH MEASUREMENT

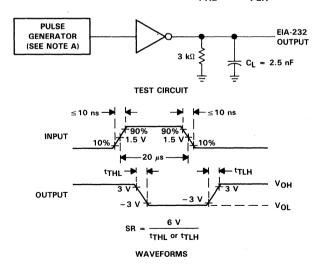


PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_{OUt} = 50 \ \Omega$, Duty Cycle $\leq 50\%$. B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER TEST CIRCUIT AND WAVEFORMS FOR tPHL AND tPLH MEASUREMENT (5-µs INPUT)



NOTE A: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω , Duty Cycle \leq 50%

FIGURE 4. TEST CIRCUIT AND WAVEFORMS FOR tTHL AND tTLH MEASUREMENT (20-µs INPUT)



MC3450, MC3452 Quadruple differential line receivers

D3006, FEBRUARY 1986-REVISED OCTOBER 1986

- Four Independent Receivers with Common Enable Input
- High Input Sensitivity . . . 25 mV Max
- High Input Impedance
- MC3450 has Three-State Outputs
- MC3452 has Open-Collector Outputs
- Glitch-Free Power-Up/Power-Down Operation

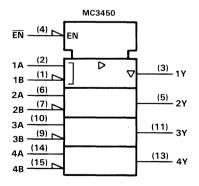
description

The MC3450 and MC3452 are quadruple differential line receivers designed for use in balanced and unbalanced digital data transmission. The MC3450 and MC3452 are the same except that the MC3450 has three-state ouputs whereas the MC3452 has open-collector outputs, which permit the wire-AND function with similar output devices. Three-state and open-collector outputs permit connection directly to a bus-organized system.

The MC3450 and MC3452 are designed for optimum performance when used with either the MC3453 quadruple differential line driver or SN75109A, SN75110A, and SN75112 dual differential drivers.

The MC3450 and MC3452 are characterized for operation from 0°C to 70°C.

logic symbols†



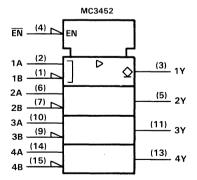
| D, J, OR N PACKAGE (TOP VIEW) | | | | | | |
|----------------------------------|-------------------|-------------------|--|--|--|--|
| 1B □ 1 | 1 U ₁₆ | □v _{cc+} | | | | |
| 1A 🔲 : | 2 15 | 4B | | | | |
| 1Y 🔲 | 3 14 |] 4A | | | | |
| EN [] | 1 13 |] 4Y | | | | |
| 2Y 🛚 🤋 | 5 12 | □vcc- | | | | |
| 2A 🗌 (| 5 11 |] 3Y | | | | |
| 2B 🔲 | 7 10 |] 3A | | | | |
| GND ∐8 | 3 9 |] 3B | | | | |

FUNCTION TABLE

| DIFFERENTIAL INPUTS | ENABLE | OUTPUT |
|---|--------|--------|
| A-B | EN | Υ |
| V _{ID} ≥ 25 mV | L | Н |
| $-25 \text{ mV} < \text{V}_{\text{JD}} < 25 \text{ mV}$ | L | ? |
| V _{ID} ≤ 25 mV | L | L |
| X | Н | Z |

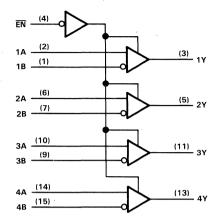
H = high level, L = low level, ? = indeterminate,

Z = impedance (off)

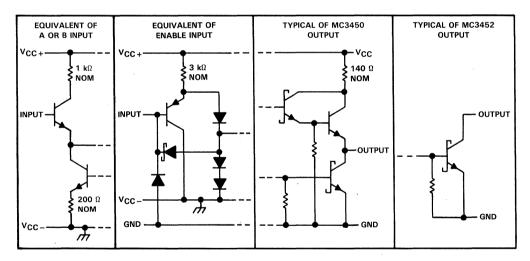


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC+ (see Note 1) 7 V Supply voltage, VCC- -7 V |
|---|
| |
| Differential input voltage (see Note 2) |
| Common-mode input voltage (see Note 3) |
| Enable input voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 4): |
| D package 950 mW |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

- 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. Common-mode input voltage is the average of the voltages at the A and B inputs.
- 4. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/ °C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C. In the J package, MC3450 and MC3452 chips are glass mounted.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-----------------|-----|-------|------|
| Supply voltage, V _{CC+} | 4.75 | 5 | 5.25 | V |
| Supply voltage, V _{CC} _ | -4.75 | - 5 | -5.25 | V |
| High-level enable input voltage, VIH | 2 | | | ٧ |
| Low-level enable input voltage, V _{IL} | | | 0.8 | ٧ |
| Low-level output current, IOL | | | - 16 | mA |
| Differential input voltage, V _{ID} (see Note 5) | -5 [†] | | 5 | V |
| Common-mode input voltage, V _{IC} (see Note 5) | -3† | | 3 | V |
| Input voltage range, any differential input to ground | -5 [†] | | 3 | ٧ |
| Operating free-air temperature, T _A | 0 | | 70 | °C |

[†] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

NOTE 5: The recommended combinations of input voltages fall within the shaded area of Figure 1.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES

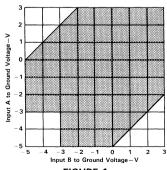


FIGURE 1



MC3450, MC3452 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

electrical characteristics over recommended operating free-air temperature range, VCC± = ±5.25 V (unless otherwise noted)

| | PARAMETER | | PARAMETER TEST CONDITIONS | | | MC3450 | | | MC3452 | | | |
|-------|---|----------|--|------|------------------|-------------------|-----|------------------|--------|------|--|--|
| | PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | UNIT | | |
| | | A inputs | $V_{ID} = -2 V$ | | 30 | 75 | | 30 | 75 | , | | |
| 1 | High-level | B inputs | $V_{ID} = -2 V$ | | 30 | 75 | | 30 | 75 | μΑ | | |
| l liH | input current | ĒN | V _{IH} = 2.4 V | | | 40 | | | 40 | μΑ | | |
| | | EM | V _{IH} = 5.25 V | ` | | 1 | | | 1 | mA | | |
| | Low-level | A inputs | $V_{ID} = 2 V$ | | | - 10 | | | - 10 | μΑ | | |
| Iμ | input current | | $V_{ID} = 2 V$ | | | - 10 | | | - 10 | μΑ | | |
| | input current | ĒN | $V_{IL} = 0.4 V$ | | | -1.6 | | | -1.6 | mA | | |
| Voн | High-level out voltage | tput | $V_{CC\pm} = \pm 4.75 \text{ V}, V_{ID} = 25 \text{ mV}$ $\overline{\text{EN}}$ at 0.8 V, $I_{OH} = -400$ $V_{IC} = -3 \text{ V}$ to 3 V | | | | | | | ٧ | | |
| loн | High-level out current | tput | $V_{CC\pm} = \pm 4.75 \text{ V}, V_{OH} = 5.25$ | V | | | | | 250 | μΑ | | |
| VOL | Low-level out voltage | put | $\frac{V_{CC\pm}}{EN}$ at 2 V, $\frac{V_{ID}}{I_{OL}} = 16$ mA $\frac{V_{IC}}{I_{OL}} = -3$ V to 3 V | | | 0.5 | | | 0.5 | ٧ | | |
| 1 | High-impedan | ce-state | $V_0 = 2.4 \text{ V}$ | | | 40 | | | | _ | | |
| loz | output curren | t | $V_0 = 0.4 \text{ V}$ | | | -40 | | | | μΑ | | |
| los | Short-circuit output curren | t‡ | $V_{ID} = 25 \text{ mV}, \qquad V_{O} = 0,$ $\overline{\text{EN}} \text{ at } 0.8 \text{ V}$ | - 18 | | ⁻ – 70 | | | | mA | | |
| Іссн+ | Supply currer V _{CC+} , outpu | | | | | 60 | | | 60 | mA | | |
| ICCH- | Supply currer | | | | | - 30 | | | -30 | m/A | | |

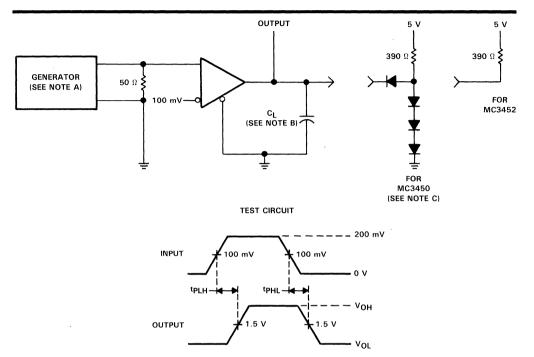
 $^{^{\}dagger}$ All typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25 °C. ‡ Not more one output should be shorted at a time.

switching characteristics, $VCC \pm = \pm 5 \text{ V}$, $TA = 25 ^{\circ}C$

| PARAMETER | FROM | то | TEST CONDITIONS | | MC3450 |) | | MC3452 | 2 | UNIT | | | |
|------------------|----------|----------|--------------------------------------|---------|------------------|--------------------------------------|-----|------------------|-----|------|----|----|----|
| PARAMETER | (INPUT) | (OUTPUT) | TEST CONDITIONS | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | UNII | | | |
| | A and B | V | C _L = 50 pF, See Figure 2 | | 17 | 25 | | | | | | | |
| ^t PLH | A and b | T T | C _L = 15 pF, See Figure 2 | | | | | 19 | 25 | ns | | | |
| + | A and B | | C _L = 50 pF, See Figure 2 | | 17 | 25 | | | | | | | |
| ^t PHL | A allu b | A allu b | A allu b | A and B | T . | C _L = 15 pF, See Figure 2 | | | | | 19 | 25 | ns |
| ^t PZH | ĒN | Υ | C _I = 50 pF, See Figure 2 | | | 21 | | | | ns | | | |
| tPZL | EN | Υ | CL = 50 pr, See Figure 2 | | | 27 | | | | lis | | | |
| ^t PHZ | ĒN | Υ | C 15 -5 C 5 2 | | | 18_ | | | | | | | |
| tPLZ | EN | Υ | $C_L = 15 \text{ pF}$, See Figure 3 | | | 29 | | | | ns | | | |
| tPLH | EN | Y | C _L = 15 pF, See Figure 4 | | | | | | 25 | ns | | | |
| ^t PHL | ĒN | Υ | C _L = 15 pF, See Figure 4 | | | | | | 25 | ns | | | |

 $^{^{\}dagger}$ All typical values are at VCC $_{+}~=$ 5 V, VCC $_{-}~=$ -5 V, TA = 25 °C.

MC3450, MC3452 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

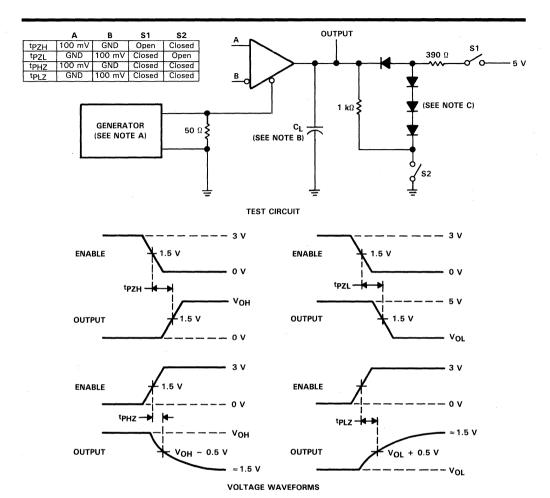


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns.

- B. CL includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

VOLTAGE WAVEFORMS

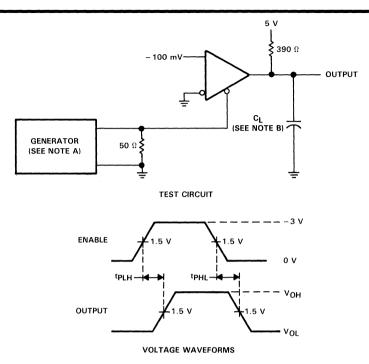
FIGURE 2. PROPAGATION DELAY TIMES



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, t_f \leq 6 ns.

- B. CL includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

FIGURE 3. MC3450 ENABLE AND DISABLE TIMES



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_f \leq$ 6 ns.

B. CL includes probe and jig capacitance.

FIGURE 4. MC3452 PROPAGATION DELAY TIMES FROM ENABLE

D3000, FEBRUARY 1986-REVISED JULY 1990

- Similar to a Dual Version of SN75110A Line Driver
- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Output Impedance
- High Common-Mode Output Voltage Range (-3 V to 10 V)
- Glitch-Free Power-Up/Power-Down Operation
- TTL Input Compatibility
- Common Enable Circuit
- Designed to be Interchangeable with Motorola MC3453

description

The MC3453 features four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This minimizes loading in party-line systems where a large number of drivers share the same line.

The driver outputs have a common-mode voltage range of -3 volts to 10 volts, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused outputs should be grounded.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 volts for high-logic-level input conditions and 0.8 volt for low-logic-level input conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

The MC3453 is characterized for operation from 0°C to 70°C.

D, J, OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

| 1A [| Ī | U ₁₆ | | VCC+ |
|----------|---|-----------------|--------|-------|
| 1 Y 🗀 | 2 | 15 | | 4A |
| 1z 🗆 | 3 | 14 | \Box | 4Y |
| 2Z [| 4 | 13 | | 4Z |
| 2Y 🛚 | 5 | 12 | | 3Z |
| ENABLE [| 6 | 11 | | 3Y |
| 2A 🗀 | 7 | 10 | | 3A |
| gnd [| 8 | 9 | | VCC - |

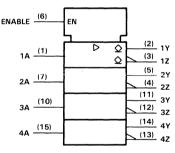
FUNCTION TABLE

| LOGIC | ENABLE INPUT | OUTPUT CURRENT | |
|-------|-----------------|-------------------|-----|
| INFO | INFO | Z | Υ |
| Н | Н | ON | OFF |
| L | н | OFF | ON |
| Н | L | OFF | OFF |
| L | L | OFF | OFF |

L = low logic level

H = high logic level

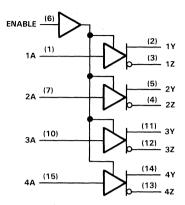
logic symbol†



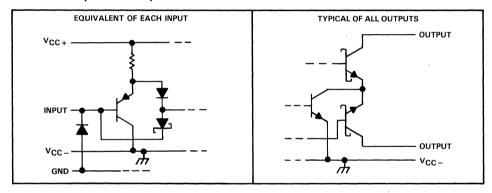
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) |
|---|
| Supply voltage, V _{CC} – |
| Input voltage (any input) |
| Output voltage range (any output) |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| D package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300 °C |

NOTES: 1. All voltage values are with respect to network ground terminal.

For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, derate
the J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2
mW/°C. In the J package the MC3453 is glass mounted.

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|--|-------|---|-------|-----|-------|------|
| Supply voltage, V _{CC+} | | | 4.75 | 5 | 5.25 | V |
| Supply voltage, V _{CC} - | | | -4.75 | -5 | -5.25 | V |
| High-level input voltage, VIH | | 2 | | 5.5 | ٧ | |
| Low-level input voltage, V _{IL} | | | 0 | | 0.8 | V |
| Common-mode output voltage range | Vocr+ | | 0 | | 10 | V |
| Common-mode output voltage range | Vocr- | | 0 | | -3 | V |
| Operating free-air temperature, TA | | | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 5.25 \text{ V}$, $V_{CC-} = -5.25 \text{ V}$ (unless otherwise noted)

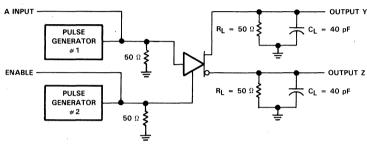
| | PARAMETER | 1 | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|---------------------------------------|-----------------------------------|------------------------------|-----------------------|-----|------------------|----------------------|------|
| VIK | Input clamp voltage | I _I = -12 mA | , and any | | | -0.9 | - 1.5 | V |
| | On state subsuit surrent | $V_{CC+} = 5.25 V$, | $V_{CC-} = -5.25 \text{ V}$ | | 11 | | 15 | |
| IO(on) | On-state output current | $V_{CC+} = 4.75 \text{ V},$ | $V_{CC-} = -4.75 \text{ V}$ | | 6.5 | 11 | 11 100 40 1 | mA |
| IO(off) | Off-state output current | $V_{CC+} = 4.75 V$ | $V_{CC-} = -4.75 \text{ V},$ | V _O = 10 V | | | 100 | μΑ |
| 1 | High-level input current | V ₁ = 2.4 V | | | | | 40 | μΑ |
| lіН | nigh-level input current | | | | | 1 | mA | |
| Ι _Ι Γ | Low-level input current | V _I = 0.4 V | | | | | -1.6 | mA |
| | Cumply current from Van | A inputs at 0.4 V | Enable at 2 V | | | 33 | 50 | mA |
| ICC+ | Supply current from V _{CC+} | A inputs at 0.4 v | Enable at 0.4 V | | | 33 | 50 | mA |
| 1 | Complete compant from Van | A innuts at 0.4 V | Enable at 2 V | | | -68 | - 90 | mA |
| ICC - | Supply current from V _{CC} - | A inputs at 0.4 V Enable at 0.4 V | | | -31 | -40 | IIIA | |

 $^{^\}dagger All$ typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, and T_A = 25 °C.

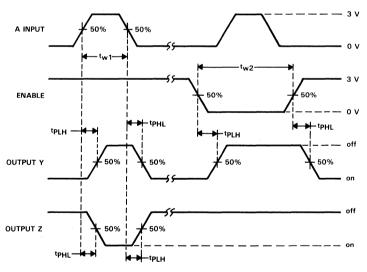
switching characteristics, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $R_L = 50$ Ω , $C_L = 40$ pF, $T_A = 25$ °C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|----------------|--------------------|-----|-----|-----|------|
| tpLH Propagation delay time, low-to-high-level output | Α | Y or Z | | | 9 | 15 | ns |
| tPHL Propagation delay time, high-to-low-level output | Α | Y or Z | See Figure 1 | | 7 | 15 | ns |
| tpLH Propagation delay time, low-to-high-level output | Enable | Y or Z | See rigure i | | 14 | 25 | ns |
| tpHL Propagation delay time, high-to-low-level output | Enable | Y or Z | , | | 15 | 25 | ns |

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{Q} = 50 \Omega$, $t_{r} = t_{f} = 10 \pm 5$ ns, $t_{W1} = 200$ ns, PRR ≤ 1 MHz, $t_{W2} = 1 \mu s$, PRR ≤ 500 kHz.

B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES



D2434, JUNE 1980-REVISED SEPTEMBER 1986

- Meets EIA Standards RS-422-A and RS423-A and Federal Standards 1020 and 1030
- 3-State, TTL-Compatible Outputs
- Fast Transition Times
- Operates from Single 5-V Supply
- Designed to be Interchangeable with Motorola MC3486

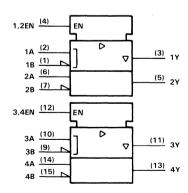
description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of EIA Standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

The MC3486 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

D, J OR N PACKAGE (TOP VIEW)

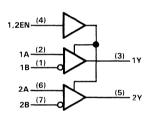
| 18 🏻 | 1 | U ₁₆ | □vcc |
|---------|---|-----------------|---------|
| 1 A 🔲 | 2 | 15 | ☐ 4B |
| 1 Y 🔲 | 3 | 14 |] 4A |
| 1,2EN 🔲 | 4 | 13 |] 4Y |
| 2Y 🗌 | 5 | 12 |] 3,4EN |
| 2A 🔲 | 6 | 11 |] 3Y |
| 2B 🗌 | 7 | 10 |] ЗА |
| GND 🔲 | 8 | 9 |] 3B |

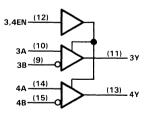
FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL INPUTS A-B | ENABLE | OUTPUT Y |
|---|--------|-------------|
| V _{ID} ≥ 0.2 V | Н | Н |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | Ξ | ? |
| $V_{ID} \leq -0.2 \text{ V}$ | Н | L |
| Irrelevant | L | Z |

H = high level, L = low level, Z = high-impedance (off), ? = indeterminate

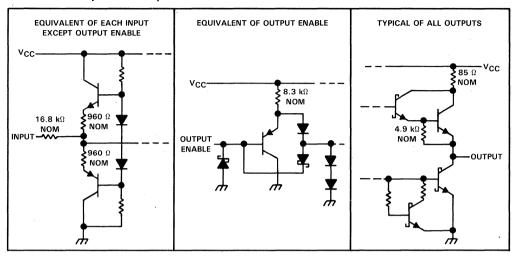
logic diagram (positive logic)







schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | . 8 V |
|--|-------|
| Input voltage, A or B inputs | ±15 V |
| Differential input voltage (see Note 2) | ±25 V |
| Enable input voltage | . 8 V |
| Low-level output current | 50 mA |
| Continuous total power dissipation See Dissipation Rating | Table |
| Operating free-air temperature range | 70°C |
| Storage temperature range65 °C to | 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300°C |

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V _{IC} | | ** | ± 7 | V |
| Differential input voltage, V _{ID} | | | ±6 | V |
| High-level enable input voltage, VIH | 2 | | | V |
| Low-level enable input voltage, V _{IL} | - | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |



electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITION: | S | MIN | MAX | UNIT |
|-----------------|---|--|-----------------------|-------------------|--------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 \text{ V}, I_0 = -0.4 \text{ m}$ | ıΑ | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 \text{ V}, I_0 = 8 \text{ mA}$ | | -0.2 [†] | | V |
| VIK | Enable-input clamp voltage | $I_I = -10 \text{ mA}$ | | | -1.5 | V |
| Vон | High-level output voltage | $V_{\text{ID}} = 0.4 \text{ V}, \qquad I_{\text{O}} = -0.4 \text{ mA},$ See Note 3 and Figure 1 | | 2.7 | | V |
| V _{OL} | Low-level output voltage | $V_{ID} = -0.4 \text{ V}, I_{O} = 8 \text{ mA},$ See Note 3 and Figure 1 | | | 0.5 | ٧ |
| lon | High-impedance-state output current | $V_{1L} = 0.8 \text{ V}, \qquad V_{1D} = -3 \text{ V}.$ | $V_0 = 2.7 \text{ V}$ | | 40 | μΑ |
| loz | riigii-iiripedance-state output current | $V_{1L} = 0.8 \text{ V}, \qquad V_{1D} = 3 \text{ V},$ | $V_0 = 0.5 V$ | | -40 | μΑ |
| | | | $V_1 = -10 \text{ V}$ | | - 3.25 | |
| Iв | Differential-input bias current | $V_{CC} = 0 \text{ V or } 5.25 \text{ V},$ | $V_1 = -3 V$ | | -1.5 | mA |
| שוי | Differential-input bias current | Other inputs at 0 V | V ₁ = 3 V | | 1.5 | """ |
| | | | $V_I = 10 \text{ V}$ | l | 3.25 | |
| lu. | High-level enable input current | $V_1 = 5.25 \text{ V}$ | | | 100 | μΑ |
| ήΗ | riigir-ievei enable input current | $V_1 = 2.7 \text{ V}$ | | 1 | 20 | μΑ |
| IIL | Low-level enable input current | $V_{I} = 0.5 V$ | | | - 100 | μΑ |
| los | Short-circuit output current | $V_{1D} = 3 V, V_{O} = 0,$ | See Note 4 | - 15 | - 100 | mA |
| lcc | Supply current | $V_{IL} = 0$ | | | 85 | mA |

[†]The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 3. Refer to EIA Standards RS-422-A and RS-423-A for exact conditions.

4. Only one output at a time should be shorted.

switching characteristics, VCC = 5 V, $TA = 25 ^{\circ}C$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|--|--------------------------------------|-----|-----|-----|------|
| tPHL | Propagation delay time, high-to-low-level output | C _I = 15 pF, See Figure 2 | | 28 | 35 | ns |
| tPLH | Propagation delay time, low-to-high-level output | CL = 15 pr, See Figure 2 | | 27 | 30 | ns |
| tPZH | Output enable time to high level | C _L = 15 pF, See Figure 3 | | 13 | 30 | ns |
| tPZL | Output enable time to low level | | | 20 | 30 | ns |
| tPHZ | Output disable time from high level | | | 26 | 35 | ns |
| tPLZ | Output disable time from low level | | | 27 | 35 | ns |

PARAMETER MEASUREMENT INFORMATION

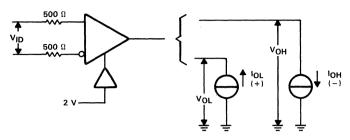


FIGURE 1. VOH, VOL

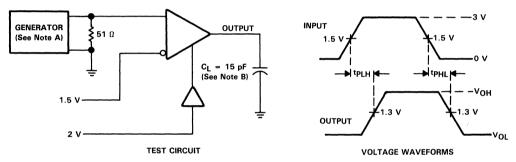
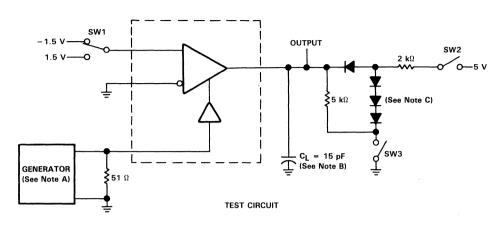


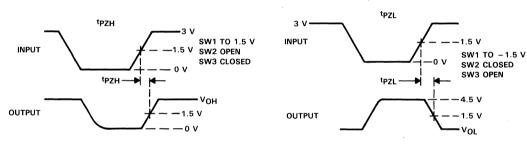
FIGURE 2. PROPAGATION DELAY TIMES

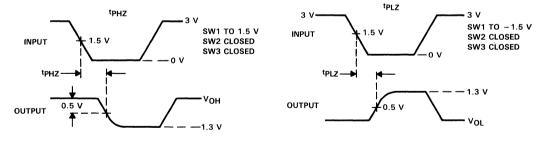
NOTES: A . The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \approx 50%, t_f \leq 6 ns.

B. Ci includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION







VOLTAGE WAVEFORMS

FIGURE 3. ENABLE AND DISABLE TIMES

NOTES: A . The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \approx 50%, $t_f \leq$ 6 ns.

- B. C_I includes probe and stray capacitance.
- C. All diodes are 1N916 or equivalent.



MC3487 QUADRUPLE DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

D2578, MAY 1980-REVISED SEPTEMBER 1986

| Meets EIA Standard RS-422-A and Federal Standard 1020 | D, J, OR N PACKAGE (TOP VIEW) |
|---|----------------------------------|
| 3-State, TTL-Compatible Outputs | 1A 1 16 VCC |
| Fast Transition Times | 1Y |
| High-Impedance Inputs | 1,2EN 🛮 4 13 🕽 4Z |
| Single 5-V Supply | 2Z |
| Power-Up and Power-Down Protection | 2A 🔲 7 10 🔲 3Y |
| Designed to Be Interchangeable with Motorola MC3487 | GND |

description

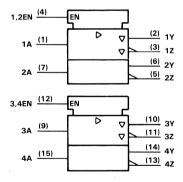
The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422-A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

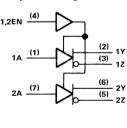
The MC3487 is characterized for operation from 0 °C to 70 °C.

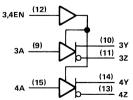
logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



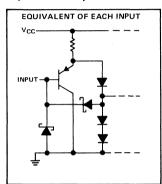


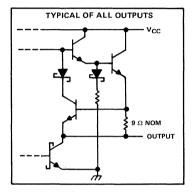
FUNCTION TABLE (EACH DRIVER)

| INPUT | OUTPUT | OUTPUTS | | | | |
|-------|--------|----------------|----------------|--|--|--|
| INPOT | ENABLE | Y | Z | | | |
| Н | Н | н . | L | | | |
| L | н | L | н | | | |
| × | L. | High-Impedance | High-Impedance | | | |

H = TTL high level L = TTL low level X = irrelevant

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N packages 260 °C |

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | 7 | MIN | MAX | UNIT | |
|-------------------|---|--------------------------------|--|-----|------|----|
| V _{IK} | Input clamp voltage | I ₁ = -18 mA | | | -1.5 | V |
| Voн | High-level output voltage | $V_{IL} = 0.8 V,$ | $V_{IH} = 2 V$, $I_{OH} = -20 \text{ mA}$ | 2.5 | | V |
| VoL | Low-level output voltage | $V_{IL} = 0.8 V,$ | $V_{IH} = 2 V$, $I_{OL} = 48 \text{ mA}$ | | 0.5 | V |
| V _{OD} | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | 2 | | V |
| Δ V _{OD} | Change in magnitude of differential output voltage [†] | $R_L = 100 \Omega$, | See Figure 1 | | ±0.4 | V |
| Voc | Common-mode output voltage [‡] | $R_L = 100 \Omega$, | See Figure 1 | | 3 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage [†] | $R_L = 100 \Omega$, | See Figure 1 | | ±0.4 | V |
| 1- | Output current with power off | V 0 | V _O = 6 V | | 100 | |
| Ю | Output current with power on | $V_{CC} = 0$ $V_{O} = -0.25 V$ | | | -100 | μΑ |
| lo- | High-impedance-state | Output enables | $V_0 = 2.7 V$ | | 100 | |
| loz | output current | at 0.8 V | V _O = 0.5 V | - | -100 | |
| lį | Input current at maximum input voltage | V _I = 5.5 V | | | 100 | μΑ |
| ΊΗ | High-level input current | V ₁ = 2.7 V | | | 50 | μΑ |
| IIL | Low-level input current | V _I = 0.5 V | | | -400 | μΑ |
| los | Short-circuit output current§ | V _I = 2 V | | -40 | -140 | mA |
| 1 | Cumbi current (all drivers) | Outputs disabled | Outputs disabled | | 105 | A |
| lcc | Supply current (all drivers) | Outputs enabled, No load | | | 85 | mA |

 $^{^{\}dagger}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

switching characteristics over recommended range of operating free-air temperature, VCC = 5 V

| | PARAMETER | TEST CONDITION | MIN | MAX | UNIT |
|------------------|--|--------------------------------------|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 2 | | 20 | ns |
| | Skew | 1 | | 6 | ns |
| tTD | Differential-output transition time | C _L = 15 pF, See Figure 3 | | 20 | ns |
| ^t PZH | Output enable time to high level | | | 30 | ns |
| tPZL | Output enable time to low level | G | | 30 | ns |
| tPHZ | Output disable time from high level | C _L = 50 pF, See Figure 4 | | 25 | ns |
| tPLZ | Output disable time from low level | | | 30 | ns |

PARAMETER MEASUREMENT INFORMATION

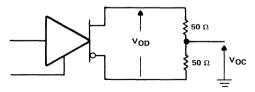


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



[‡]In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

§Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

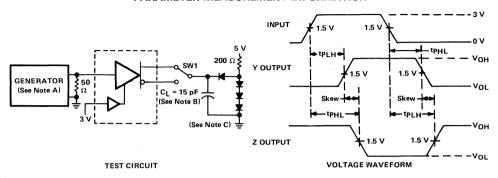


FIGURE 2. PROPAGATION DELAY TIMES

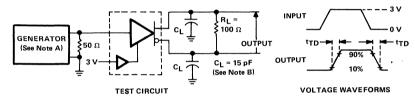
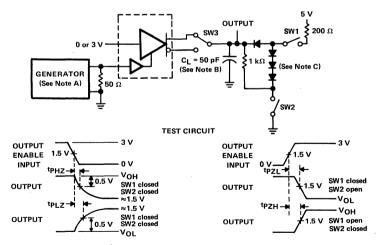


FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_0 = 50 \Omega$.
 - B. C_L includes probe and stray capacitance.
 - C. All diodes are 1N916 or 1N3064.



D3171, FEBRUARY 1989

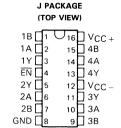
- Four Independent Receivers with Common Enable Input
- High Input Sensitivity . . . 25 mV Max
- High Input Impedance
- MC3550 has Three-State Outputs
- MC3552 has Open-Collector Outputs
- Glitch-Free Power-Up/Power-Down Operation
- Military-Temperature-Range Versions of MC3450 and MC3452

description

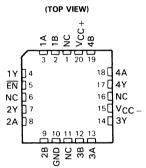
The MC3550 and MC3552 are quadruple differential line receivers designed for use in balanced and unbalanced digital data transmission. The two devices are the same except that the MC3550 has three-state outputs whereas the MC3552 has open-collector outputs, which permit the wire-AND function with similar output devices. Three-state and open-collector outputs permit direct connection to a bus-organized system.

The MC3550 and MC3552 are designed for optimum performance when used with either the MC3553 quadruple differential line driver or SN55109A, SN55110A, and SN55112 dual differential drivers.

The MC3550 and MC3552 are characterized for operation over the full military temperature range of -55 °C to 125 °C.



FK PACKAGE



NC-No internal connection

FUNCTION TABLE

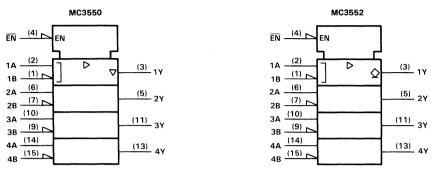
| DIFFERENTIAL INPUTS A-B | ENABLE EN | OUTPUT Y |
|----------------------------------|--------------|-------------|
| V _{ID} > 25 mV | L | Н |
| -25 mV < V _{ID} < 25 mV | L | ? |
| V _{ID} ≤ 25 mV | L | L |
| × | н | z |

H = high level, L = low level, ? = indeterminate,

Z = impedance (off)

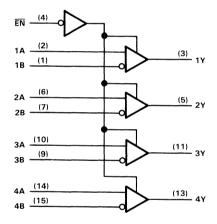
MC3550, MC3552 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

logic symbols†

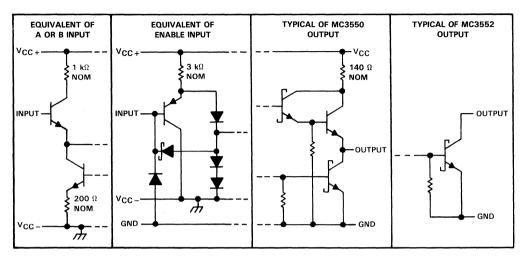


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC+ (see Note 1) | 7 V |
|---|--------------------------------|
| Supply voltage, VCC – | |
| Differential input voltage (see Note 2) | |
| Common-mode input voltage (see Note 3) | ±5 V |
| Enable input voltage | 5.5 V |
| | |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see | Note 4) 13/5 mW |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Operating free-air temperature range | |
| · · · · · · · · · · · · · · · · · · · | 55°C to 125°C |
| Operating free-air temperature range | 55°C to 125°C 65°C to 150°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

- 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. Common-mode input voltage is the average of the voltages at the A and B inputs.
- 4. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-----------------------|-----------------|-----|------|------|
| Cumply valtage Va- | T _A ≥ 25°C | 4.5 | 5 | 5.5 | V |
| Supply voltage, V _{CC+} | T _A < 25°C | 4.75 | 5 | 5.5 | ľ |
| Cumply valtage V | T _A ≥ 25°C | -4.5 | -5 | -5.5 | V |
| Supply voltage, V _{CC} - | T _A < 25°C | -4.75 | -5 | -5.5 | ľ |
| High-level enable input voltage, V _{IH} | | 2 | | | V |
| Low-level enable input voltage, VIL | | | | 0.8 | ٧ |
| Low-level output current, IOL | | | | -16 | mA |
| Differential input voltage, V _{ID} (see Note 5) | | 5† | | 5 | ٧ |
| Common-mode input voltage, V _{IC} (see Note 5) | | -3 [†] | | 3 | ٧ |
| Input voltage range, any differential input to ground | | -5 [†] | | 3 | V |
| Operating free-air temperature, TA | | - 55 | | 125 | °C |

[†] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

NOTE 5: The recommended combinations of input voltages fall within the shaded area of Figure 1.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES

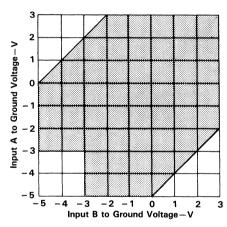


FIGURE 1

electrical characteristics over recommended operating free-air temperature range, VCC ± = MAX (unless otherwise noted)

| | PARAMETER | | IAMETER TEST CONDITIONS [†] | | | MC355 |) | MC3552 | | | UNIT |
|-------|--|----------|--|-------------------------|-----|------------------|------|--------|------|------|-------|
| | | | | | MIN | TYP [‡] | MAX | MIN | TYP‡ | MAX | 0.4.1 |
| | | A inputs | $V_{ID} = -2 V$ | | | 30 | 75 | | 30 | 75 | |
| l | High-level | B inputs | $V_{ID} = -2 V$ | | | 30 | 75 | | 30 | 75 | μΑ |
| чн | input current | ĒN | V _{IH} = 2.4 V | | | | 40 | | | 40 | μΑ |
| | | EN | $V_{IH} = V_{CC} + MA$ | X | | | 1 | | | 1 | mA |
| | Low-level | A inputs | $V_{ID} = 2 V$ | | | | - 10 | | | - 10 | ^ |
| IIL. | | B inputs | V _{ID} = 2 V | | | | - 10 | | | - 10 | μΑ |
| ł | input current | EN | $V_{IL} = 0.4 V$ | | | | 1.6 | | | -1.6 | mA |
| VOH | High-level output OH voltage | | $V_{CC\pm} = MIN$, \overline{EN} at 0.8 V, $V_{IC} = -3$ V to 3 | $I_{OH} = -400 \mu A$ | 2.4 | | | | | | V |
| Іон | High-level output current | | V _{CC±} = MIN, | $V_{OH} = V_{CC} + MAX$ | | | | | | 250 | μΑ |
| VOL | Low-level output voltage | | $V_{CC\pm} = MIN,$ \overline{EN} at 0.8 V, $V_{IC} = -3 \text{ V to } 3$ | | | | 0.5 | | | 0.5 | ٧ |
| | High-impedance | e-state | $V_0 = 2.4 \text{ V}$ | | | | 40 | | | | |
| loz | output current | | $V_0 = 0.4 \text{ V}$ | | | | -40 | | | | μΑ |
| los | Short-circuit output current | i | $V_{ID} = 25 \text{ mV},$ \overline{EN} at 0.8 V | V _O = 0, | -18 | | - 70 | | | | mA |
| ICCH+ | Supply current V _{CC+} , outputs | | A inputs at GND, | B inputs at 3 V, | | 3H 3H 6 | 60 | | | 60 | mA |
| Іссн- | Supply current VCC _ , outputs | | EN at 3 V | | | | - 30 | | | - 30 | mA |

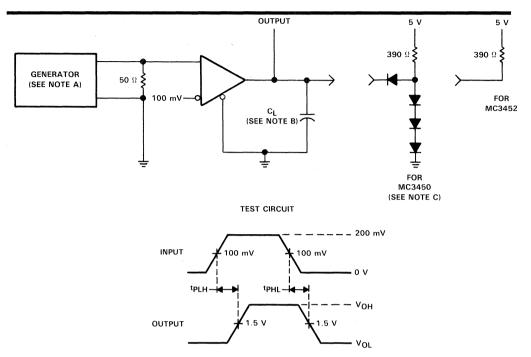
For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $VCC \pm = \pm 5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$

| PARAMETER | FROM | то | TEST CONDITIONS | MC3550 | | | MC3552 | | | | | |
|------------------|---------------|----------|--------------------------------------|---------|------|--------------------------------------|--------|-----|-----|------|----|----|
| TANAMETER | (INPUT) | (OUTPUT) | TEST CONDITIONS | MIN | TYP¶ | MAX | MIN | TYP | MAX | UNIT | | |
| tour | tpi H A and B | γ | C _L = 50 pF, See Figure 2 | | 17 | 25 | | | | | | |
| ^t PLH | A allu B | , r | C _L = 15 pF, See Figure 2 | | | | | 19 | 25 | ns | | |
| t _{PHL} | HL A and B Y | V | C _L = 50 pF, See Figure 2 | | 17 | 25 | | | | | | |
| PHL | | A and b | A and b | A and b | | C _L = 15 pF, See Figure 2 | | | | | 19 | 25 |
| ^t PZH | ĒN | Υ | C E0 = C. = Figure 2 | | | 21 | | | | | | |
| tPZL | ĒN | Y | C _L = 50 pF, See Figure 2 | | | 27 | | | | ns | | |
| ^t PHZ | ĒN | Y | C: _ 15 pc Coo Figure 2 | | | 18 | | | | | | |
| tPLZ | ĒN | Y | C _L = 15 pF, See Figure 3 | | | 29 | | | | ns | | |
| ^t PLH | EN | Y | C _L = 15 pF, See Figure 4 | | | | | | 25 | ns | | |
| [‡] PHL | ĒN | Y | C _L = 15 pF, See Figure 4 | | | | | | 25 | ns | | |

[¶] All typical values are at $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$.

 $^{^\}ddagger$ All typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25 °C. § Not more than one output should be shorted at a time,

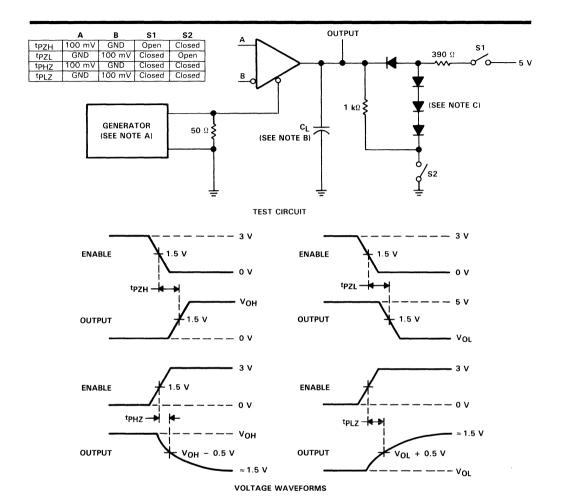


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.

- B. CL includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

VOLTAGE WAVEFORMS

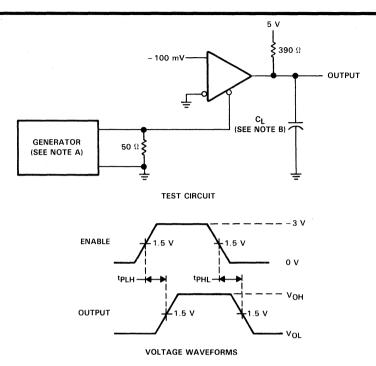
FIGURE 2. PROPAGATION DELAY TIMES



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_{\text{f}} \leq$ 6 ns.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

FIGURE 3. MC3550 ENABLE AND DISABLE TIMES



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_{f} \leq$ 6 ns. $t_{f} \leq$ 6 ns.

B. CL includes probe and jig capacitance.

FIGURE 4. MC3552 PROPAGATION DELAY TIMES FROM ENABLE

D3170, OCTOBER 1988

- Similar to a Dual Version of SN55110A Line Driver
- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Output Impedance
- High Common-Mode Output Voltage Range (-3 V to 10 V)
- Glitch-Free Power-Up/Power-Down Operation
- TTL Input Compatibility
- Common Enable Circuit
- Military-Temperature-Range Version of MC3453

description

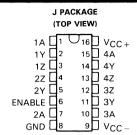
The MC3553 features four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This feature minimizes loading in partyline systems where a large number of drivers share the same line.

The driver outputs have a common-mode voltage range of -3 V to 10 V, allowing common-mode voltages on the line without affecting driver performance.

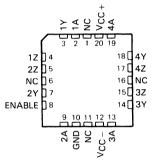
All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused outputs should be grounded.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests guarantee 400 mV of noise margin when interfaced with Series 54 TT.

The MC3553 is characterized for operation over the full military temperature range of -55 °C to 125 °C.



FK PACKAGE (TOP VIEW)



NC-No internal connection

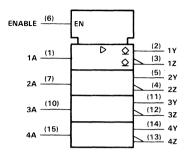
FUNCTION TABLE

| | LOGIC INPUT | ENABLE INPUT | OUTPUT CURRENT | |
|---|----------------|-----------------|-------------------|-----|
| | | | z | Υ |
| | Н | Н | ON | OFF |
| Ì | L | н | OFF | ON |
| | н | Ł | OFF | OFF |
| | L | L | OFF | OFF |

L = low logic level

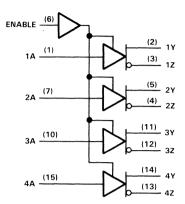
H = high logic level

logic symbol†

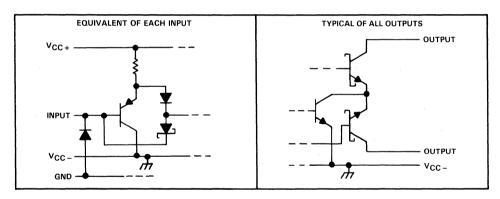


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) |
|--|
| Supply voltage, V _{CC} |
| Input voltage (any input) |
| Output voltage range (any output) |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) 1375 mW |
| Operating free-air temperature range |
| Storage temperature range |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/ °C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|------------------------|-------|-----|-------|------|
| Supply voltage, V _{CC+} | T _A ≥ 25°C | 4.5 | 5 | 5.5 | V |
| | T _A < 25°C | 4.75 | 5 | 5.5 | · · |
| Supply voltage, V _{CC} – | T _A ≥ 25°C | -4.5 | - 5 | - 5.5 | V |
| | T _A < 25 °C | -4.75 | - 5 | - 5.5 | v |
| High-level input voltage, VIH | | 2 | | 5.5 | V |
| Low-level input voltage, V _{IL} | | 0 | | 0.8 | V |
| Common mode output valtage range | Vocr+ | 0 | | 10 | V |
| Common-mode output voltage range | Vocr- | 0 | | -3 | V |
| Operating free-air temperature, TA | | | | 125 | °C |

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = MAX$, $V_{CC-} = -MAX$ (unless otherwise noted)

| | PARAMETER | PARAMETER TEST CONDITIONS [†] | | | TYP [‡] | MAX | UNIT |
|------------------|---|--|---------------------|--|------------------|-------|------|
| VIK | Input clamp voltage | lj = -12 mA | | | -0.9 | - 1.5 | V |
| | On state sutput surrent | $V_{CC+} = MAX, V_{CC}$ | CC - = MAX | | 11 | 15 | m ^ |
| (O(on) | On-state output current | $V_{CC+} = MIN, V_{CC-} = MIN$ | | | 11 | | mA |
| IO(off) | Off-state output current | $V_{CC+} = MIN$, $V_{CC-} = MIN$, $V_{O} = 10 \text{ V}$ | | | | 100 | μΑ |
| 1 | High-level input current | V _I = 2.4 V | | | | 40 | μΑ |
| ЧН | High-level input current | $V_I = V_{CC} + MAX$ | $V_I = V_{CC+} MAX$ | | | 1 | mA |
| I _I L | Low-level input current | V _I = 0.4 V | | | | - 1.6 | mA |
| laa | Supply current from V _{CC+} | A inputs at 0.4 V | Enable at 2 V | | 33 | 50 | mA |
| Icc+ | Subbly carrent from ACC+ | A inputs at 0.4 V | Enable at 0.4 V | | 33 | 50 | IIIA |
| lan | Icc - Supply current from Vcc - A inputs at 0.4 V | | Enable at 2 V | | - 68 | -90 | mA |
| Icc- | Supply current from V _{CC} – | Enable at 0.4 V | | | - 31 | - 40 | mA |

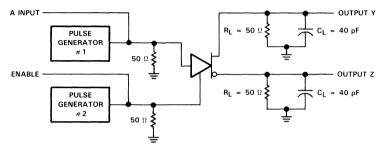
[†]For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

 $^{^{\}ddagger}$ All typical values are at $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, and $T_A = 25$ °C.

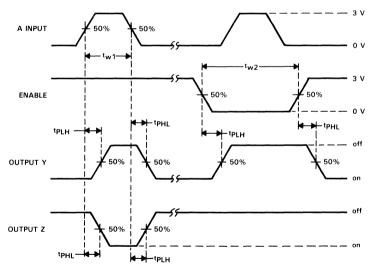
switching characteristics, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $R_L = 50$ Ω , $C_L = 40$ pF, $T_A = 25$ °C

| PARAMETER | | TO (OUTPUT) | TEST CONDITIONS | MIN | ТҮР | MAX | UNIT |
|---|--------|----------------|--------------------|-----|-----|-----|------|
| tpLH Propagation delay time, low-to-high-level output | Α | Y or Z | | | 9 | 15 | ns |
| tpHL Propagation delay time, high-to-low-level output | Α | Y or Z | See Figure 1 | | 7 | 15 | ns |
| tpLH Propagation delay time, low-to-high-level output | Enable | Y or Z | See Figure 1 | | 14 | 25 | ns |
| tpHL Propagation delay time, high-to-low-level output | Enable | Y or Z | | | 15 | 25 | ns |

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_0 \approx 50~\Omega$, $t_r = t_f = 10~\pm 5$ ns, $t_{W1} \leq 200$ ns, PRR ≤ 1 MHz, $t_{W2} \leq 1~\mu s$, PRR $\leq 500~kHz$.

B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES



N8T26 QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUTS

D2462, MAY 1978-REVISED SEPTEMBER 1986

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- Designed to Be Interchangeable with Signetics N8T26, also Called 8T26

description

The N8T26 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have 3-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of 200 μ A. This device is capable of high switching rates into high-capacitance loads and are suitable for driving long bus lines.

The N8T26 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (DRIVER)

| INP | UT | OUTPUT |
|-----|----|--------|
| DE | D | В |
| Н | L | н |
| Н | Н | L |
| L | X | Z |

FUNCTION TABLE (RECEIVER)

| IN | PUT | OUTPUT |
|----|-----|--------|
| RE | В | R |
| L | L | Н |
| L | Н | L |
| Н | X | z |

H = high level

L = low level

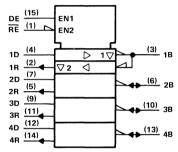
X = irrelevant

Z = high impedance

D, J, OR N PACKAGE (TOP VIEW)

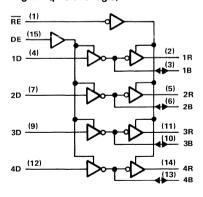
| RE [| U | 16 |] vcc |
|--------|---|----|-------|
| 1R 🔲 : | 2 | 15 |] DE |
| 18 🔲 3 | 3 | 14 |] 4R |
| 1D 🛮 4 | 1 | 13 |] 4B |
| 2R 🔲 | 5 | 12 |] 4D |
| 2В [[€ | 6 | 11 |] 3R |
| 2D 🗌 : | 7 | 10 |] 3B |
| GND [| 3 | 9 |] 3D |

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

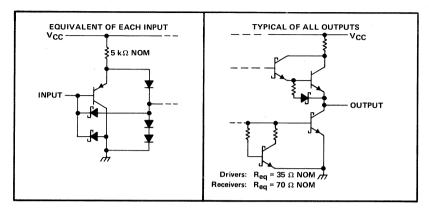
logic diagram (positive logic)





N8T26 QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUTS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|--------------|-------------|------|-----|------|------|
| Supply voltage, V _{CC} | | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | B, D, DE, RE | | 2 | | | V |
| Low-level input voltage, V _{IL} | B, D, DE, RE | | | | 0.85 | V |
| I Cab I and a standard of the | Driver, B | | | | - 10 | 4 |
| High-level output current, IOH | Receiver, R | Receiver, R | | | -2 | mA |
| Lour lovel output ourset Lo | Driver, B | | | | 40 | ^ |
| Low-level output current, IOL | Receiver, R | Receiver, R | | | 16 | mA |
| Operating free-air temperature, TA | | | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT |
|-----|---|-----------|---------------------------|--|------|------------------|-------|-------|
| VIK | Input clamp voltage | B,D,DE,RE | I _I = -5 mA | | | | - 1 | V |
| Vон | High-level output voltage | В | $V_{IH} = 2 V$, | $V_{IL} = 0.85 \text{ V}, I_{OH} = -10 \text{ mA}$ | 2.6 | 3.1 | | V |
| ¥0H | riigii-iever output voitage | R | $V_{IL} = 0.85 V$ | I _{OH} -2 mA | 2.6 | 3.1 | | • |
| VOL | Low-level output voltage | В | $V_{IH} = 2 V$, | $I_{OL} = 40 \text{ mA}$ | | | 0.5 | V |
| VOL | Low-level output voltage | R | $V_{IH} = 2 V$, | $V_{IL} = 0.85 \text{ V}, I_{OL} = 16 \text{ mA}$ | | | 0.5 | v |
| loz | Off-state (high-impedance | B,R | DE at 0.85 V | RE at 2 V, $V_0 = 2.6 \text{ V}$ | | | 100 | μΑ |
| 102 | state) output current | R | RE at 2 V, | $V_0 = 0.5 V$ | | | - 100 | μΛ |
| ΙΗ | High-level input current | D,DE,RE | V _I = 5.25 V | | | | 25 | μΑ |
| IIL | Low-level input current | B,D,DE,RE | V _I = 0.4 V | | | | - 200 | μΑ |
| los | Short-circuit output current [‡] | В | V _{CC} = 5.25 V | | - 50 | | - 150 | mA |
| 08 | Short circuit output current | R | VCC = 5.25 V | | - 30 | | - 75 | 111/4 |
| lcc | Supply current | | $V_{CC} = 5.25 \text{ V}$ | , No load | | | 87 | mA |

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------|-----|------------------------------|-----|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level output | В | R | $C_L \approx 30 \text{ pF},$ | | 8 | 18 | ns |
| tPHL Propagation delay time, high-to-low-level output | | | See Figure 1 | | 7 | 10 | ns |
| tpLH Propagation delay time, low-to-high-level output | | | $C_L = 300 \text{ pF},$ | | 14 | 20 | |
| tpHL Propagation delay time, high-to-low-level output | D | D B | See Figure 2 | | 12 | 20 | ns |
| tpLZ Output disable time from low level | RE | R | $C_L = 30 \text{ pF},$ | | 9 | 17 | ns |
| tpzL Output enable time to low level | ne ne | , n | See Figure 3 | | 15 | 30 | 115 |
| tpLZ Output disable time from low level | DE | В | $C_L = 300 \text{ pF},$ | | 20 | 43 | |
| tpzL Output enable time to low level | DE | В. | See Figure 4 | | 20 | 38 | ns |

 $^{^{\}dagger}AII$ typical values are at TA = 25 °C and VCC = 5 V. $^{\ddagger}Only$ one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

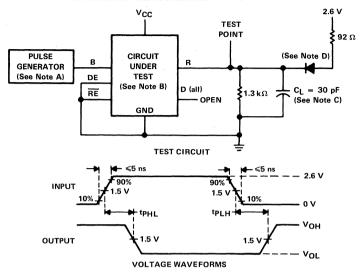


FIGURE 1. PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT

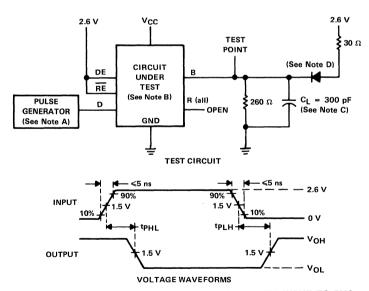


FIGURE 2. PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

- NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR \leq 10 MHz, duty cycle = 50%, $Z_0 \approx 50~\Omega$.
 - B. All inputs and outputs not shown are open.
 - C. C_L includes probe and jig capacitance.
 - D. All diodes are 1N916 or 1N3064.



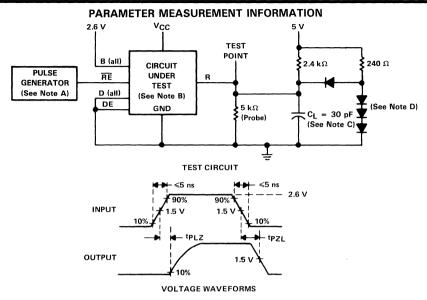


FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

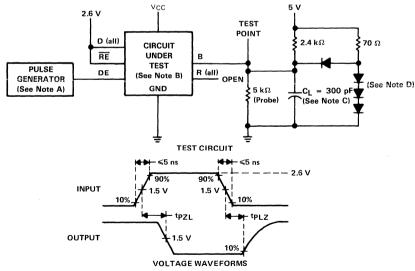


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

- NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR \leq 5 MHz, duty cycle = 50%, $Z_0 \approx 50~\Omega$.
 - B. All inputs and outputs not shown are open.
 - C. CL includes probe and jig capacitance.
 - D. All diodes are 1N916 or 1N3064.



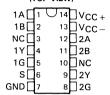
D2304, JANUARY 1977-REVISED MAY 1990

- High Speed
- Standard Supply Voltage
- Dual Channels
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Range of ±3 V
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- TTL Drive Capability
- High DC Noise Margin
- '107A and '107B Have Totem-Pole Outputs
- '108A and '108B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input for Power-Off Condition

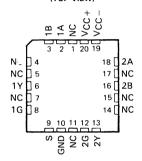
description

These circuits are TTL-compatible high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

SN55107A, SN55107B, SN55108A SN55108B . . . J PACKAGE SN75107A, SN75107B, SN75108A SN75108B . . . D, J, OR N PACKAGE (TOP VIEW)



SN55107A, SN55107B, SN55108A, SN55108B . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

The essential difference between the "A" and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:





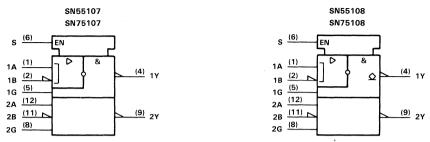
This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

The SN55107A, SN55107B, SN55108A, and SN55108B are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $\,^{\circ}$ C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0 $\,^{\circ}$ C to 70 $\,^{\circ}$ C.



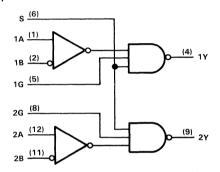
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logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

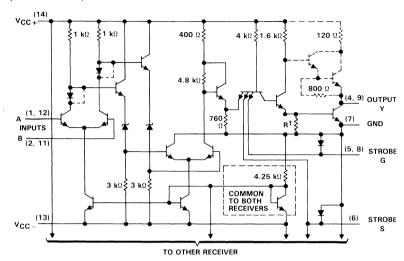


FUNCTION TABLE

| DIFFERENTIAL INPUTS | STROBES | | OUTPUT |
|--|---------|---|---------------|
| A-B | G | s | Υ |
| V _{ID} ≥ 25 mV | Х | X | Н |
| | Х | L | Н |
| $-25 \text{ mV} < V_{\text{ID}} < 25 \text{ mV}$ | L | X | Н |
| | Н | Н | Indeterminate |
| | X | L | Н |
| $V_{ID} \leq -25 \text{ mV}$ | L | Х | Н |
| | Н | Н | L |

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Pin numbers shown are for D, J, and N packages.

 $^{\dagger}\,R$ = 1 k Ω for '107A and '107B, 750 Ω for '108A and '108B.

NOTES: 1. Resistor values shown are nominal.

Components shown with dashed lines in the output circuitry are applicable to the '107A and '107B only. Diodes in series with the collectors of the differential input transistors are short circuited on '107A and '108A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 3) | 7 V |
|---|--------|
| Supply voltage, V _{CC} | -7 V |
| Differential input voltage (see Note 4) | ±6 V |
| Common mode input voltage (see Note 5) | +5 V |
| Strobe input voltage | 5.5 V |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 6): | |
| D package | 50 mW |
| FK or J package: Series 55 | 75 mW |
| J package: Series 75 | 25 mW |
| N package | 50 mW |
| Operating free-air temperature range: Series 55 | 125°C |
| Series 75 0°C to | o 70°C |
| Storage temperature range65°C to | |
| Case temperature for 60 seconds: FK package | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C |
| | |

- NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.
 - 4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
 - 5. Common-mode input voltage is the average of the voltages at the A and B inputs.
 - For operation above 25 °C free-air temperature, derate linearly at the following rates: 7.6 mW/ °C for the D package, 11.0 mW/ °C for the FK and J packages with series 55 chips, 8.2 mW/ °C for the J package with series 75 chips, and 9.2 mW/ °C for the N package.



SN55107A, SN55107B, SN55108A, SN55108B SN75107A, SN75107B, SN75108A, SN75108B DUAL LINE RECEIVERS

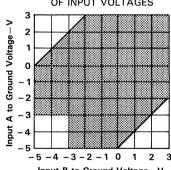
recommended operating conditions (see Note 7)

| | SN55107A, SN55107B SN55108A, SN55108B | | SN75107A, SN75107B SN75108A, SN75108B | | | UNIT | |
|---|--|-----|--|-----------------|-----|--------|----|
| <u> </u> | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V _{CC+} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | ٧ |
| Supply voltage, V _{CC} – | -4.5 | - 5 | -5.5 | -4.75 | - 5 | -5.25 | V |
| High-level input voltage between differential inputs, V _{IDH} (see Note 8) | 0.025 | | 5 | 0.025 | | 5 | ٧ |
| Low-level input voltage between differential inputs, VIDL (see Note 8) | -5† | | -0.025 | -5 [†] | | -0.025 | ٧ |
| Common-mode input voltage, V _{IC} (see Notes 8 and 9) | -3 [†] | | 3 | -3 [†] | | 3 | V |
| Input voltage, any differential input to ground (see Note 8) | -5 [†] | | 3 | -5 [†] | | 3 | V |
| High-level input voltage at strobe inputs, V _{IH(S)} | 2 | | 5.5 | 2 | | 5.5 | V |
| Low-level input voltage at strobe inputs, VIL(S) | 0 | | 0.8 | 0 | | 0.8 | V |
| Low-level output current, IOL | | | -16 | | | - 16 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

[†] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

- NOTES: 7. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3 V and 3 V.
 - 8. The recommended combinations of input voltages fall within the shaded area of the figure shown.
 - The common-mode voltage may be as low as -4 V provided that the more positive of the two inputs is not more negative than -3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIO | NS [†] | '107A, '107B MIN TYP [‡] MAX | '108A, '108B MIN TYP [‡] MAX | UNIT |
|-------|---|---|---|--|--|-------------|
| ΊΗ | High-level A input current B | V _{CC±} = MAX | V _{ID} = 5 V V _{ID} = -5 V | 30 75 30 75 | 30 75 30 75 | μΑ |
| IĮL | Low-level A input current B | V _{CC±} = MAX | V _{ID} = -5 V V _{ID} = 5 V | - 10 - 10 | - 10 - 10 | μΑ |
| ίιн | High-level input current into 1G or 2G | $V_{CC\pm} = MAX$, $V_{IH(S)} = 2.4 V$ $V_{CC\pm} = MAX$, $V_{IH(S)} = MAX$ | | 40 | 40 | μA mA |
| IIL | Low-level input current into 1G or 2G | $V_{CC\pm} = MAX$, $V_{IL(S)} = 0.4 V$ | | -1.6 | -1.6 | mA |
| ЧН | High-level input current into S | $V_{CC\pm} = MAX$, $V_{IH(S)} = 2.4 V$ $V_{CC\pm} = MAX$, $V_{IH(S)} = MAX$ | | 80 | 80 2 | μA mA |
| IIL | Low-level input current into S | $V_{CC\pm} = MAX, V_{IL(S)} = 0.4 V$ | | -3.2 | -3.2 | mA |
| Vон | High-level output voltage | $V_{CC\pm} = MIN, V_{IL(S)} = 0.8 \text{ V}$ $I_{OH} = -400 \mu\text{A}, V_{IC} = -3 \text{ V}$ to | | 2.4 | | > |
| VOL | Low-level output voltage | $V_{CC\pm} = MIN$, $V_{IH(S)} = 2 V$, $I_{OL} = 16 \text{ mA}$, $V_{IC} = -3 V \text{ to}$ | | 0.4 | 0.4 | ٧ |
| ЮН | High-level output current | $V_{CC\pm} = MIN, V_{OH} = MAX V$ | 'cc+ | | 250 | μΑ |
| los | Short-circuit output current§ | V _{CC±} = MAX | | -1870 | | mA |
| ICCH+ | Supply current from V _{CC+} , outputs high | $V_{CC\pm} = MAX, T_A = 25$ °C | | 18 30 | 18 30 | mA |
| l | Supply current from V _{CC} –, ouputs high | $V_{CC\pm} = MAX$, $T_A = 25$ °C | | -8.4 -15 | -8.4 -15 | mA |

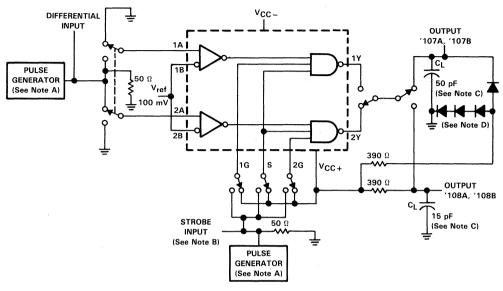
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC\pm} = \pm 5 \text{ V}$, $T_A = 25 \, ^{\circ}\text{C}$ (see Figure 1)

| PARAMETER TEST | | DADAMETER TECT CONDITIONS | | ′107A, ′107B | | | '108A, '108B | | |
|---------------------|---|------------------------------------|-----|--------------|-----|-----|--------------|-----|------|
| | | TEST CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| + | Propagation delay time, low-to-high-level | $R_L = 390 \Omega, C_L = 50 pF$ | | 17 | 25 | | | | ns |
| tPLH(D) | output, from differential inputs A and B | $R_L = 390 \Omega$, $C_L = 15 pF$ | | | | | 19 | 25 | 115 |
| * | Propagation delay time, high-to-low-level | $R_L = 390 \Omega, C_L = 50 pF$ | | 17 | 25 | | | | |
| ^t PHL(D) | output, from differential inputs A and B | $R_L = 390 \Omega$, $C_L = 15 pF$ | | | | | 19 | 25 | ns |
| +======= | Propagation delay time, low-to-high-level | $R_L = 390 \Omega$, $C_L = 50 pF$ | | 10 | 15 | | | | ns |
| ^t PLH(S) | output, from strobe input G or S | $R_L = 390 \Omega, C_L = 15 pF$ | | | | | 13 | 20 | 115 |
| +======= | Propagation delay time, high-to-low-level | $R_L = 390 \Omega$, $C_L = 50 pF$ | | 8 | 15 | | | | 200 |
| ^t PHL(S) | output, from strobe input G or S | $R_L = 390 \Omega, C_L = 15 pF$ | | | | | 13 | 20 | ns |

 $^{^\}ddagger$ All typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25 °C. 5 Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

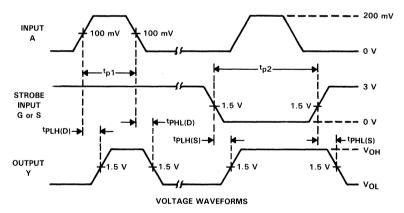


FIGURE 1. PROPAGATION DELAY TIMES

- NOTES: A. The pulse generators have the following characteristics: $Z_0 = 50 \Omega$, $t_f = 10 \pm 5 \text{ ns}$, $t_f = 10 \pm 5 \text{ ns}$, $t_{pd1} = 500 \text{ ns}$, PRR $\leq 1 \text{ MHz}$, $t_{pd2} = 1 \mu \text{s}$, PRR $\leq 500 \text{ kHz}$.
 - B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
 - C. C_L includes probe and jig capacitance.
 - D. All diodes are 1N916.



TYPICAL CHARACTERISTICS[†]

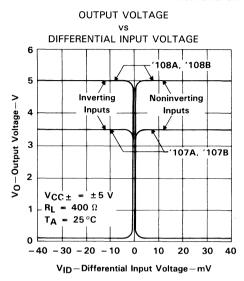


FIGURE 2

SUPPLY CURRENT, OUTPUTS HIGH vs

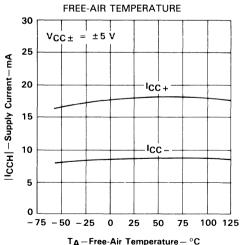


FIGURE 4

† Values below 0 °C and above 70 °C apply to SN55 Series only.



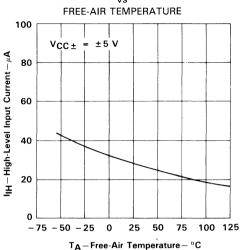
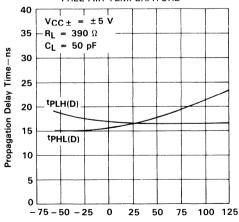


FIGURE 3

'107A, '107B PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS)

FREE-AIR TEMPERATURE



T_A—Free-Air Temperature— °C FIGURE 5



TYPICAL CHARACTERISTICS[†]

'108A, '108B
PROPAGATION DELAY TIME, LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)

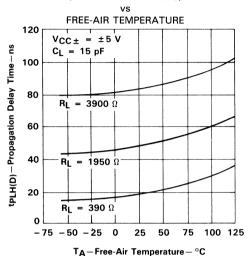
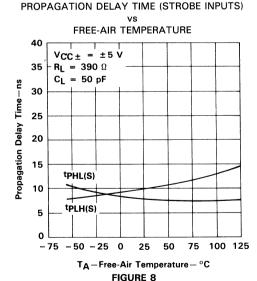
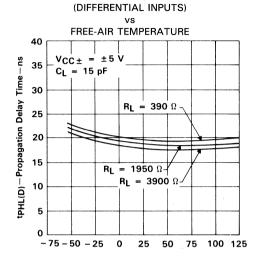


FIGURE 6 '107A, '107B



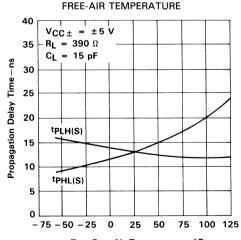
[†] Values below 0 °C and above 70 °C apply to SN55 Series only.

'108A, '108B PROPAGATION DELAY TIME, HIGH-TO-LOW LEVEL



T_A – Free-Air Temperature – °C FIGURE 7

'108A, '108B PROPAGATION DELAY TIME (STROBE INPUTS) vs



TA-Free-Air Temperature - °C



basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately $(30 + 1.3 \, \text{L})$ ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2I_{O(on)} \cdot R_{T}$$
.

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (RT) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

FIGURE 10

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.



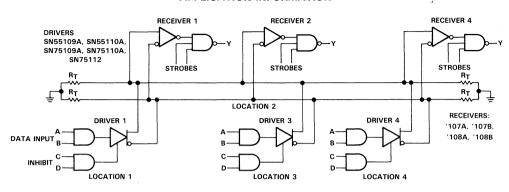


FIGURE 11

unbalanced or single-line systems

These dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of -3 V to 3 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

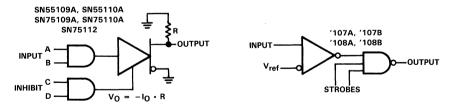
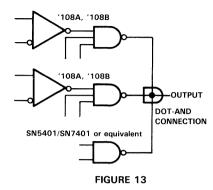


FIGURE 12



'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an opencollector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.



increasing common-mode input voltage range of receiver

The common-mode voltage range or CMVR is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ± 3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ± 10 V to ± 15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore reducing the versatility of the receiver.

The ability of the receiver to operate with approximately $\pm\,15\,\text{V}$ common-mode voltage at the inputs has been checked using the circuit shown in Figure 14. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately $\pm\,3\,\text{V}$ common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table A.

TABLE A

| Attenuator 1: | R1 = | $2 k\Omega$, $R2 = 0.5 k\Omega$ |
|---------------|------|---|
| Attenuator 2: | R1 = | $6 \text{ k}\Omega$, R2 = 1.5 k Ω |
| Attenuator 3: | R1 = | 12 k Ω , R2 = 3 k Ω |

Table B shows some of the typical switching results obtained under such conditions.

TABLE B. TYPICAL PROPAGATION DELAYS FOR RECEIVER WITH ATTENUATOR TEST CIRCUIT SHOWN IN FIGURE 14

| DEVICE | PARAMETERS | INPUT | TYPICAL |
|--------------|------------------|------------|---------|
| | | ATTENUATOR | (ns) |
| | | 1 | 20 |
| ′107A, ′107B | ^t PLH | 2 | 32 |
| | | 3 | 42 |
| | | 1 | 22 |
| | ^t PHL | 2 | 31 |
| | | 3 | 33 |
| | | 1 | 36 |
| | ^t PLH | 2 | 47 |
| '108A, '108B | | 3 | 57 |
| 1084, 1088 | | 1 | 29 |
| | t _{PHL} | 2 | 38 |
| | | 3 | 41 |



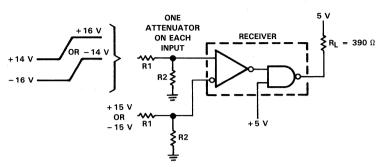


FIGURE 14. COMMON-MODE CIRCUIT FOR TESTING INPUT ATTENUATORS, WITH RESULTS SHOWN IN TABLE B

Two methods of terminating a transmission line to reduce reflections are:

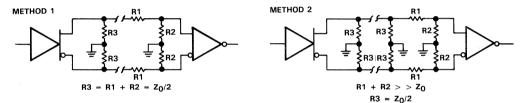
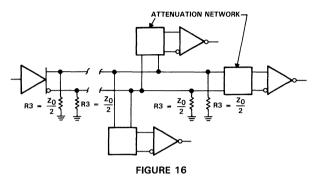


FIGURE 15

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

For party-line operation, method 2 should be used as follows:



To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table A.

furnace control using the SN75108A

The furnace control circuit in Figure 17 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically the operation of this control is as follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the "heat on" relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the "heat on" relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

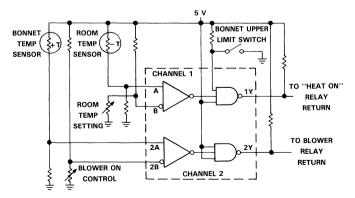
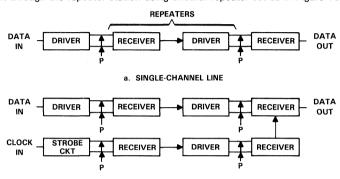


FIGURE 17. FURNACE CONTROL USING SN75108A



repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 18(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 18(b).



b. MULTICHANNEL LINE WITH STROBE

FIGURE 18. RECEIVER-DRIVER REPEATERS

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse width control.

As a differential comparator, a '107A or '108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 19. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

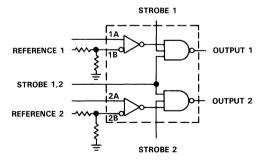
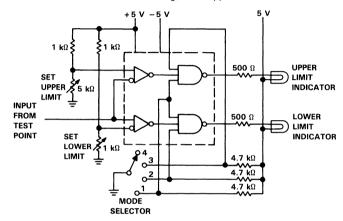


FIGURE 19. SN55107A SERIES RECEIVER AS A DUAL DIFFERENTIAL COMPARATOR



window detector

The window detector circuit in Figure 20 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time — such as detecting whether a voltage or signal has exceeded its limits or "window". Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the "upper and lower limits" test position is used.



MODE SELECTOR LEGEND

| POSITION | CONDITION |
|----------|---------------------------------|
| 1 | OFF |
| 2 | TEST FOR UPPER LIMIT |
| 3 | TEST FOR LOWER LIMIT |
| 4 | TEST FOR UPPER AND LOWER LIMITS |

FIGURE 20. WINDOW DETECTOR USING SN75108A

temperature controller with zero-voltage switching

The circuit in Figure 21 switches an electric resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately $100~\mu s$) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is AND'ed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

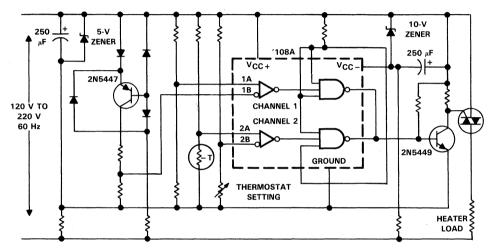


FIGURE 21. ZERO-VOLTAGE SWITCHING TEMPERATURE CONTROLLER

D2106, DECEMBER 1975-REVISED MAY 1990

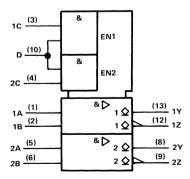
- Improved Stability over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range (-3 V to 10 V)
- TTL Input Compatibility
- Inhibitor Available for Driver Selection
- Glitch-Free During Power-Up/Down

| -55°C to 125°C J or FK PACKAGE | 0°C to 70°C J or N PACKAGE | OUTPUT FUNCTION |
|-----------------------------------|-------------------------------|-------------------------|
| SN55109A | SN75109A | 6-mA Current Switch |
| SN55110A | SN75110A | 12-mA Current Switch |
| | SN75112 | 27-mA Current Switch |

description

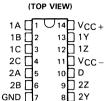
The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

logic symbol†

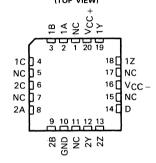


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IED Publication 617-12.

SN55109A, SN55110A, . . . J PACKAGE SN75109A, SN75110A, SN75112 . . . D, J, OR N PACKAGE

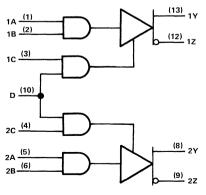


SN55109A, SN55110A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.



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description (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current is nominally 6 mA for the '109A, 12 mA for the '110A, and 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, IO(off), is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of $-3\,\mathrm{V}$ to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests assure 400 mV of noise margin when interfaced with Series 54/74 TTL.

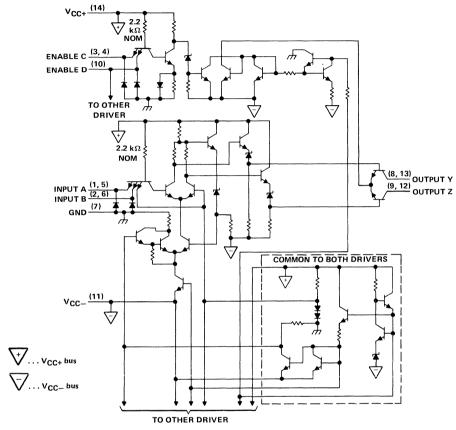
The SN55109A and SN55110A are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN75109A, SN75110A, and SN75112 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE (EACH DRIVER)

| | LOGIC INPUTS | | ENABLE INPUTS | | UTS [†] |
|---|-----------------|---|------------------|-----|------------------|
| Α | В | С | D | Υ | Z |
| Х | X | L | × | OFF | OFF |
| X | X | × | L | OFF | OFF |
| L | X | Н | Н | ON | OFF |
| X | L | Н | Н | ON | OFF |
| Н | н | Н | Н | OFF | ON |

H = high level, L = low level, X = irrelevant [†]When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for D, J, and N packages.

SN55109A, SN55110A SN75109A, SN75110A, SN75112 DUAL LINE DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| 1 | | SN55109A SN55110A | SN75109A SN75110A | SN75112 | UNIT | |
|---|-----------|------------------------------|----------------------|------------|------|--|
| V _{CC+} Supply voltage (see Note 1) | 7 | 7 | 7 | V | | |
| V _{CC} Supply voltage | | 7 | -7 | -7 | V | |
| V _I Input voltage | | | 5.5 | 5.5 | V | |
| Output voltage range | -5 to 12 | -5 to 12 | -5 to 12 | V | | |
| Continuous total power dissipation (see Note 2) | | See Dissipation Rating Table | | | | |
| Operating free-air temperature range | | - 55 to 125 | 0 to 70 | 0 to 70 | °C | |
| Storage temperature range | | -65 to 150 | -65 to 150 | -65 to 150 | °C | |
| Case temperature for 60 seconds: FK package | 260 | | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | | 300 | 300 | 300 | °C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D package | | 260 | 260 | °C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | N package | | 260 | 260 | | |

NOTES: 1. Voltage values are with respect to network ground terminal.

In the FK or J package, SN55109A and SN55110A chips are either silver glass or alloy mounted, and SN75109A, SN75110A, and SN75112 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | T _A = 70°C | T _A = 125°C |
|------------|-----------------------|-----------------|-----------------------|------------------------|
| PACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55 A) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75) | 1025 mW | 8.2 mW/°C | 656 mW | |
| N | 1150 mW | 9.2 mW/°C | 736 mW | - |

recommended operating conditions (see Note 3)

| | | SN55109A, SN55110A | | | SN75109A, SN75110A SN75112 | | | UNIT |
|--|----------------------|-----------------------|-----|-------|----------------------------------|-----|-------|------------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply Voltage V _{CC+} | T _A ≥ 0°C | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | |
| | T _A < 0°C | 4.75 | 5 | 5.5 | | | |] <u> </u> |
| Supply voltage V _{CC} – | T _A ≥ 0°C | -4.5 | - 5 | - 5.5 | -4.75 | - 5 | -5.25 | |
| Subbit Agustage ACC | T _A < 0°C | -4.75 | - 5 | -5.5 | | | | LĽ |
| Positive common-mode output voltage | | 0 | | 10 | 0 | | 10 | V |
| Negative common-mode output voltage | | 0 | | -3 | 0 | | -3 | V |
| High-level input voltage, VIH | | 2 | | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | | | 0.8 | V |
| Operating free-air temperature, TA | | - 55 | | 125 | 0 | | 70 | °C |

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS† | SN55109A, SN75109A | | SN55110A, SN75110A | | | SN75112 | | | UNIT | |
|--|---|-----------------------|--|-----------------------|------------------|-----------------------|------|------------------|---------|------|------------------|------|------|
| | | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| v _{IK} | Input clamp voltage | | $V_{CC\pm} = MIN$, $I_{\parallel} = -12 \text{ mA}$ | | -0.9 | 1.5 | | -0.9 | -1.5 | | -0.9 | -1.5 | ٧ |
| 1 | On-state output current | | $V_{CC\pm} = MAX, V_O = 10 V$ | | 6 | 7 | | 12 | 15 | | 27 | 36 | mA |
| ^I O(on) | On-state output current | | $V_{CC\pm} = MIN, V_O = -3 V$ | 3.5 | 6 | | 6.5 | 12 | | 18 | 27 | | mA |
| IO(off) | Off-state output current | | $V_{CC\pm} = MIN, V_O = 10 V$ | | | 100 | | | 100 | | | 100 | μА |
| 1. | Input current at maximum | A, B, or C inputs | V _{CC+} = MAX, V _I = 5.5 V | | | 1 | | | 1 | | | 1 | mA |
| 4 | input voltage | D input | VCC± = WAX, V = 5.5 V | | | 2 | | | 2 | | | 2 | IIIA |
| | High-level input current | A, B, or C inputs | V _{CC+} = MAX, V _I = 2.4 V | | | 40 | | | 40 | | | 40 | μА |
| ¹H | nign-level input current | D input | VCC ± = WAX, V ₁ = 2.4 V | | | 80 | | | 80 | | | 80 | μΑ |
| | Law lovel input ourrent | A, B, or C inputs | - MAY V - 0.4 V | | | -3 | | | -3 | | | ~ 3 | |
| l _{IL} | Low-level input current | D input | $V_{CC\pm} = MAX, V_i = 0.4 V$ | | | -6 | | | -6 | | | -6 | mA |
| I _{CC + (on)} | I _{CC+(on)} Supply current from V _{CC+} with driver enabled | | V _{CC±} = MAX, A and B inputs at 0.4 V, | | 18 | 30 | | 23 | 35 | | 25 | 40 | mA |
| I _{CC} – (on) Supply current from V _{CC} – with driver enabled | | C and D inputs at 2 V | | - 18 | - 30 | | - 34 | - 50 | | - 65 | - 100 | | |
| ICC + (off) | Supply current from V _{CC+} | with driver inhibited | V _{CC} = MAX, | | 18 | | | 21 | | | 30 | | mA |
| ICC - (off) | | | A, B, C, and D inputs at 0.4 V | | - 10 | | | - 17 | | | - 32 | | '''^ |

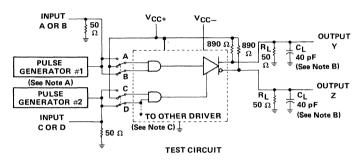
[†]For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions. ‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25 °C.

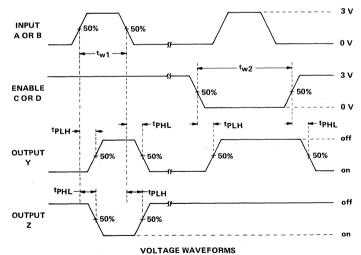
switching characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|-------------------------|-----|-----|-----|------|
| ^t PLH | A or B | A or B Y or Z | C _L = 40 pF, | | 9 | 15 | ns |
| tPHL | AOIB | | $R_L = 50 \Omega$, | | 9 | 15 | ns |
| tPLH . | C or D | Y or Z | See Figure 1 | | 16 | 25 | ns |
| tPHL telephone | | 1 01 2 | Joe rigule i | | 13 | 25 | ns |

[†]tpl H = Propagation delay time, low-to-high-level output.

PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generators have the following characteristics: $Z_0 = 50 \Omega$, $t_e = t_f = 10 \pm 5$ ns, $t_{W1} = 500$ ns, PRR ≤ 1 MHz, $t_{W2} = 1 \mu s$, PRR ≤ 500 kHz.

- B. C_L includes probe and jig capacitance.
- C. For simplicity, only one channel and the enable connections are shown.

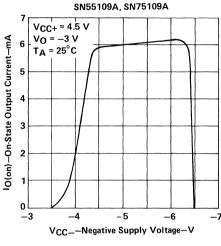
FIGURE 1. PROPAGATION DELAY TIMES

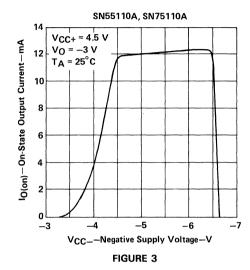


tpHL = Propagation delay time, high-to-low-level output.

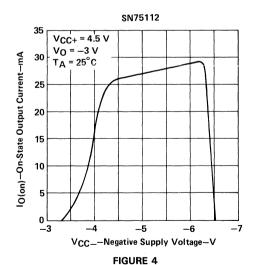
TYPICAL CHARACTERISTICS

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE





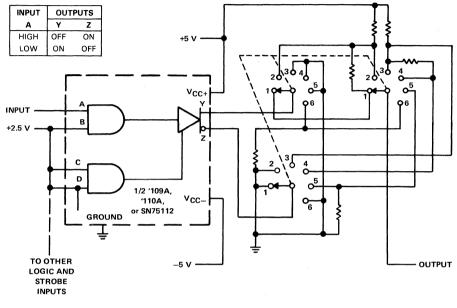






special pulse-control circuit

Figure 5 shows a circuit that may be used as a pulse generator output or in many other testing applications.



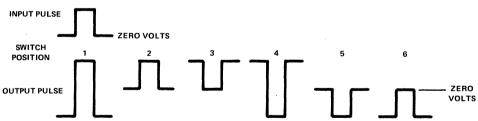


FIGURE 5. PULSE CONTROL CIRCUIT

2-110

SN55111, SN75111 QUADRUPLE LINE DRIVERS WITH COMMON ENABLES

D3000, FEBRUARY 1986-REVISED OCTOBER 1988

- Similar to a Dual Version of the SN55109A/SN75109A Line Driver
- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Output Impedance
- High Common-Mode Output Voltage Range (-3 V to 10 V)
- Glitch-Free Power-Up/Power-Down Operation
- TTL Input Compatibility
- Common Enable Circuit

description

The SN55111 and SN75111 feature four line drivers with a common enable input. When the enable input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the enable is low, all channel outputs are nonconductive (transistors biased to cutoff). This feature minimizes loading in party-line systems where a large number of drivers share the same line.

The driver outputs have a common-mode voltage range of -3 V to 10 V, allowing common-mode voltages on the line without affecting driver performance.

All outputs should be maintained within the recommended common-mode output voltage range to ensure that the channels do not interact with each other. To minimize power dissipation, all unused inputs should be grounded.

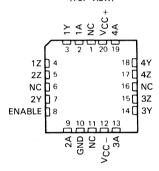
All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests guarantee 400 mV of noise margin when interfaced with Series 54/74 TTL.

The SN55111 is characterized for operation from $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN75111 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

SN55111 . . . J PACKAGE SN75111 . . . D, J, OR N PACKAGE (TOP VIEW)

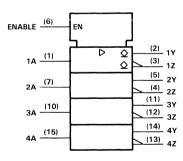
16□ VCC + 1A ∏1 1Y Π_2 15∏ 4A 1**Z** [3 14 T 4Y 2Z 🗆 4 13 T 4Z 2Y 🛚 5 12 3Z ENABLE 16 11 T 3Y 2A ∏7 10 T 3A GND 🛮 8 9 \ VCC -

SN55111 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol†



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

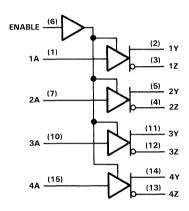
FUNCTION TABLE

| LOGIC | ENABLE | OUT | |
|-------|----------|-----|-----|
| INPUT | UT INPUT | z | Υ |
| Н | Н | ON | OFF |
| L | н | OFF | ON |
| н | L | OFF | OFF |
| L | L | OFF | OFF |

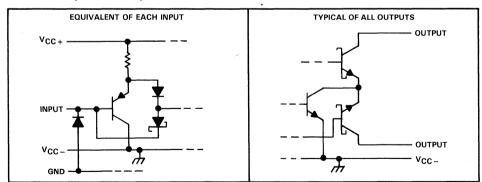
L = low logic level

H = high logic level

logic diagram (positive logic)



schematics of inputs and outputs



SN55111, SN75111 QUADRUPLE LINE DRIVERS WITH COMMON ENABLES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) |
|---|
| Supply voltage, VCC |
| Input voltage (any input) |
| Output voltage range (any output) |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN55111 |
| SN75111 |
| Storage temperature range65 °C to 150 °C |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds; J package |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | TA = 85°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------|---------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55111) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75111) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |

recommended operating conditions (see Note 2)

| | | SN55111 | | | | UNIT | | |
|--|-----------------------|---------|-----|-------|--------|------|-------|------|
| | | | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC+} | T _A ≥ 25°C | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| | T _A < 25°C | 4.75 | 5 | 5.5 | 4.75 | 5 | 5.25 | · · |
| Complementary V | T _A ≥ 25°C | -4.5 | - 5 | - 5.5 | - 4.75 | - 5 | -5.25 | V |
| Supply voltage, V _{CC} – | T _A < 25°C | -4.75 | -5 | -5.5 | -4.75 | ~ 5 | -5.25 | \ \ |
| High-level input voltage, VIH | | 2 | | 5.5 | 2 | | 5.5 | V |
| Low-level input voltage, V _{IL} | | 0 | | 0.8 | 0 | | 0.8 | V |
| Common mode autout valtere rooms | V _{OCR+} | 0 | | . 10 | 0 | | 10 | V |
| Common-mode output voltage range | V _{OCR} - | 0 | | -3 | 0 | | -3 | V |
| Operating free-air temperature, TA | | - 55 | | 125 | 0 | | 70 | °C |

NOTE 2: All unused outputs should be grounded.

SN55111, SN75111 QUADRUPLE LINE DRIVERS WITH COMMON ENABLES

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = MAX$, $V_{CC-} = MAX$ (unless otherwise noted)

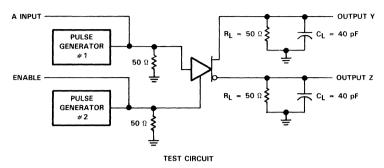
| | PARAMETER | TEST CO | MIN | TYP [‡] | MAX | UNIT | |
|---------|---------------------------------------|---------------------------|----------------------------|------------------|------|-------|------|
| VIK | Input clamp voltage | . I _I = -12 mA | | | -0.9 | - 1.5 | V |
| | On state cutnut current | $V_{CC+} = MAX,$ | V _{CC} = MAX | | 5.5 | 7 | m A |
| IO(on) | On-state output current | V _{CC+} = MIN, | V _{CC} = MIN | 3.5 | 5.5 | | mA |
| IO(off) | Off-state output current | V _{CC+} = MIN, | $V_{CC-} = MIN, V_O = 10V$ | | | 100 | μΑ |
| I | High-level input current | V _I = 2.4 V | | | | 40 | μΑ |
| lН | | $V_I = V_{CC} + MAX$ | | | | 1 | mA |
| Iμ | Low-level input current | V _I = 0.4 V | | | | -1.6 | mA |
| 1 | Supply current from V _{CC+} | A : | Enable at 2 V | | 28 | 40 | ^ |
| ICC+ | | A inputs at 0.4 V | Enable at 0.4 V | | 27 | 40 | mA |
| 1 | Supply current from V _{CC} - | A innute at 0.4 V | Enable at 2 V | | -43 | - 55 | mA |
| ICC - | | A inputs at 0.4 V | Enable at 0.4 V | | - 25 | - 35 | IIIA |

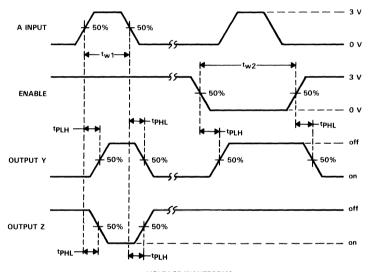
[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $R_L = 50 \Omega$, $C_L = 40 \text{ pF}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | ТҮР | MAX | UNIT |
|-----------|--|-----------------|----------------|--------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | Α | Y or Z | See Figure 1 | | 9 | 15 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Α | Y or Z | | | 7 | 15 | ns |
| tPLH | Propagation delay time, low-to-high-level output | Enable | Y or Z | | | 14 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Enable | Y or Z | | | 15 | 25 | ns |

 $^{^{\}ddagger}All$ typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, and T_A = 25 °C.





VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_0 \approx 50 \ \Omega$, $t_r = t_f = 10 \pm 5 \ ns$, $t_{W1} \le 200 \ ns$, PRR $\le 10 \ MHz$, $t_{W2} \le 1 \ \mu s$, PRR $\le 500 \ kHz$.

FIGURE 1. PROPAGATION DELAY TIMES

SN55113, SN75113 DUAL DIFFERENTIAL LINE DRIVERS

D1315, SEPTEMBER 1973--REVISED SEPTEMBER 1986

- Choice of Open-Collector, Open-Emitter, or 3-State Outputs
- High-Impedance Output State for Party-Line Applications
- Single-Ended or Differential AND/NAND Outputs
- Single 5-V Supply
- Dual Channel Operation
- Compatible With TTL
- Short-Circuit Protection
- High-Current Outputs
- Common and Individual Output Controls
- Clamp Diodes at Inputs and Outputs
- Easily Adaptable to SN55114 and SN75114 Applications
- Designed for Use With SN55115 and SN75115

description

The SN55113 and SN75113 dual differential line drivers with 3-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. Individual controls are provided for each output pair, as well as a common control for both output pairs. If any output is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

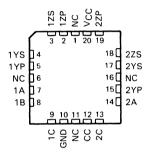
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

The SN55113 is characterized for operation over the full military temperature range of $-55\,^{\rm o}{\rm C}$ to 125 °C. The SN75113 is characterized for operation over the temperature range of 0 °C to 70 °C.

SN55113 . . . J PACKAGE SN75113 . . . D, J, OR N PACKAGE (TOP VIEW)

| 1ZP | Пī | U ₁₆ | □ vcc |
|-----|-------------|-----------------|-------|
| 1ZS | □2 | 15 | 2ZP |
| 1YS | Дз | 14 |] 2ZS |
| 1YP | []4 | 13 |] 2YS |
| 1 A | □ 5 | 12 | 2YP |
| 1B | □6 | 11 |] 2A |
| 1C | ď۶ | 10 | 2C |
| GND | \square 8 | 9 | Псс |

SN55113 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

| INF | OUTPUTS | | | | |
|--------|--------------------|----|----------------|-----|------|
| OUTPUT | UTPUT CONTROL DATA | | Α | AND | NAND |
| С | cc | AE | 3 [†] | Υ | Z |
| L | X | X | Х | Z | Z |
| Х | L | × | Х | z | Z |
| н | н | L. | Х | L | н |
| н | Н | × | L | L | н |
| н | н | н | Н | Н | L |

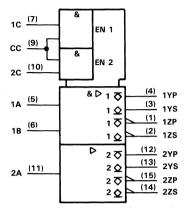
H = high level, L = low level, X = irrelevant,

Z = high impedance (off)



[†]B input and 4th line of function table are applicable only to driver number 1.

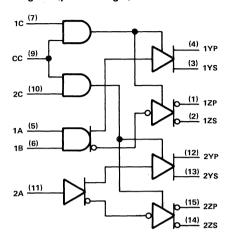
logic symbolt



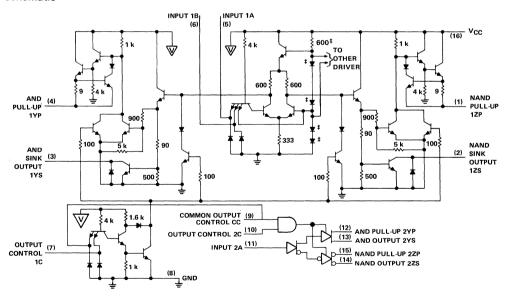
 $^{^\}dagger \text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematic



 $[\]bigvee$. . . V_{CC} bus

[‡]These components common to both drivers. Resistor values shown are nominal and in ohms.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|--|
| Off-state voltage applied to open-collector outputs |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range: SN55113 |
| SN75113 |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. In the J and FK packages, SN55113 chips are alloy mounted; SN75113 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55113) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75113) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |

recommended operating conditions

| | | SN55113 | | | SN75113 | | |
|------------------------------------|-----|---------|------|------|---------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | V |
| High-level output current, IOH | | | - 40 | | | -40 | mA |
| Low-level output current, IOL | | | 40 | | | 40 | mA |
| Operating free-air temperature, TA | -55 | | 125 | 0 | | 70 | °C |

SN55113, SN75113 **DUAL DIFFERENTIAL LINE DRIVERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | TEST CONDITION | uot | S | N55113 | | S | UNIT | | |
|-----------------|---|-------------------------|--------------------------|----------------------------------|-----|------------------|-------|-----|------------------|-------|-----------------|
| | FARAMETER | | TEST CONDITION | vo. | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNIT |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, | I _I = -12 mA | | | -0.9 | -1.5 | | -0.9 | - 1.5 | V |
| Voн | High-level output voltage | V _{CC} = MIN, | V _{IH} = 2 V, | I _{OH} = -10 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| VOH | riigii-level output voltage | V _{IL} = 0.8 V | | $I_{OH} = -40 \text{ mA}$ | 2 | 3.0 | | 2 | 3.0 | | V |
| VOL | Low-level output voltage | V _{CC} = MIN, | V _{IH} = 2 V, | | | 0.23 | 0.4 | | 0.23 | 0.4 | V |
| VOL | Low level output voltage | | $I_{OL} = 40 \text{ mA}$ | | | 0.23 | 0.4 | | 0.23 | 0.4 | ľ |
| Vok | Output clamp voltage | V _{CC} = MAX, | $I_0 = -40 \text{ mA}$ | | | -1.1 | - 1.5 | | -1.1 | - 1.5 | ٧ |
| | | | V _{OH} = 12 V | $T_A = 25$ °C | | 1 | 10 | | | | |
| lo. m | Off-state open-collector | V _{CC} = MAX | 0 | T _A = 125°C | | | 200 | | | | |
| IO(off) | output current | VCC - WAX | V _{OH} = 5.25 V | T _A = 25°C | | | | | 1 | 10 | μΑ |
| | | | | T _A = 70°C | | | | | | 20 | |
| loz | Off-state (high-impedance-state) output current | | T _A = 25°C, | $V_O = 0$ to V_{CC} | | | ±10 | | | ± 10 | |
| | | V _{CC} = MAX, | | V _O = 0 | | | - 150 | | | - 20 | - 20 ± 20 μA |
| | | Output controls | $T_A = MAX$ | V _O = 0.4 V | | | ±80 | | | ± 20 | |
| | | utput current at 0.8 V | IA - WAX | V _O = 2.4 V | | | ±80 | | | ± 20 | ± 20 |
| | | | | V _O = V _{CC} | | | 80 | | | 20 | |
| | Input current A, B, C | | ., | | | | 1 | | | 1 | |
| 11 | input voltage CC | V _{CC} = MAX, | V ₁ = 5.5 V | | | | 2 | | | 2 | mA |
| ΊΗ | High-level A, B, C | V _{CC} = MAX, | V 24 V | | | | 40 | | | 40 | |
| LIH. | input current CC | VCC = MAX, | V - 2.4 V | | | | 80 | | | 80 | μΑ |
| I _{IL} | Low-level A, B, C | V _{CC} = MAX, | V: - 0.4 V | | | | - 1.6 | | | -1.6 | ^ |
| 'lL | input current CC | VCC - MAX, | V - 0.4 V | | | | -3.2 | | | -3.2 | mA |
| los | Short-circuit | V _{CC} = MAX, | V _O = 0, | T _A = 25°C | -40 | - 90 | - 120 | -40 | - 90 | - 120 | mA |
| | output current§ | | | | | | | | | | |
| lcc | Supply current | All inputs at 0 V, | No load, | V _{CC} = MAX | | 47 | 65 | | 47 | 65 | mA |
| | (both drivers) | $T_A = 25$ °C | | V _{CC} = 7 V | | 65 | 85 | | 65 | 85 | |

[†]All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25 °C

| | PARAMETER | TEST CONDITIONS | SN55113 | | | SN75113 | | | UNIT |
|------------------|--|--------------------------------------|---------|-----|-----|---------|-----|-----|--------|
| | - ANAMETEN | TEST CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX |] ONIT |
| tPLH | Propagation delay time, low-to-high-level output | See Figure 1 | | 13 | 20 | ٠ | 13 | 30 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | 3ee rigule i | | 12 | 20 | | 12 | 30 | ns |
| ^t PZH | Output enable time to high level | R _L = 180 Ω, See Figure 2 | | 7 | 15 | | 7 | 20 | ns |
| ŤPZL | Output enable time to low level | $R_L = 250 \Omega$, See Figure 3 | | 14 | 30 | | 14 | 40 | ns |
| tPHZ | Output disable time from high level | $R_L = 180 \Omega$, See Figure 2 | | 10 | 20 | | 10 | 30 | ns |
| t _{PLZ} | Output disable time from low level | $R_L = 250 \Omega$, See Figure 3 | | 17 | 35 | | 17 | 35 | ns |

 $^{^{\}ddagger}$ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V. § Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

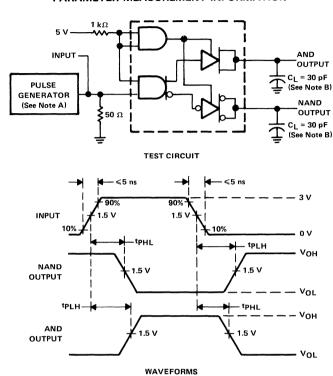
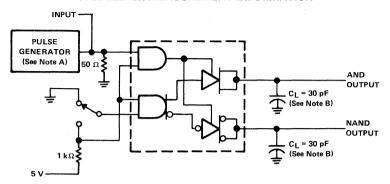


FIGURE 1. tpLH and tpHL

NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$.



TEST CIRCUIT

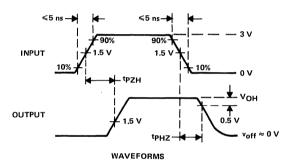
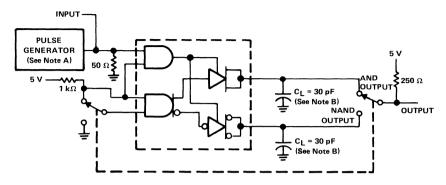


FIGURE 2. tPZH and tPHZ

NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \ \Omega$, PRR $\leq 500 \ kHz$, $t_W = 100 \ ns$.



TEST CIRCUIT

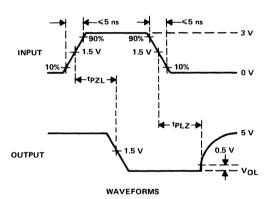
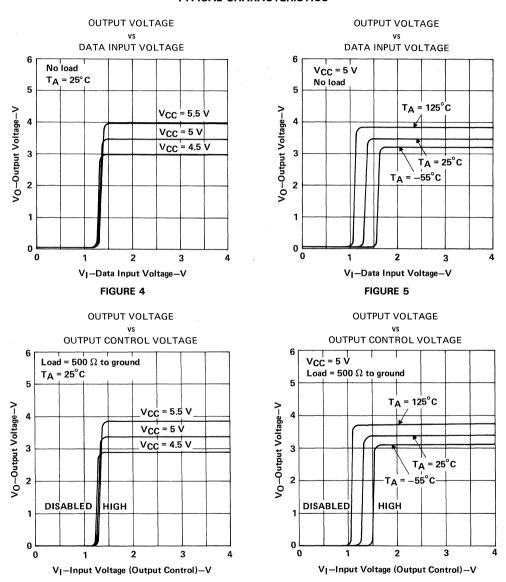


FIGURE 3. tpzL and tpLZ

NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$.

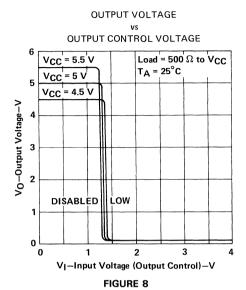


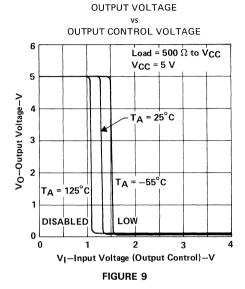
[†]Data for temperatures below 0 °C and above 70 °C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

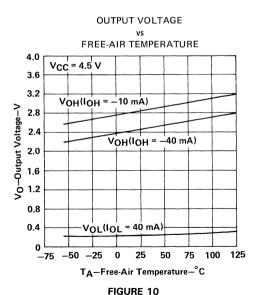
FIGURE 7

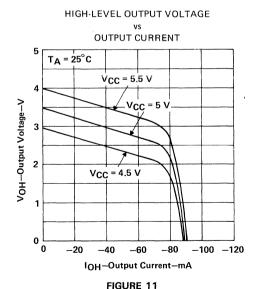


FIGURE 6

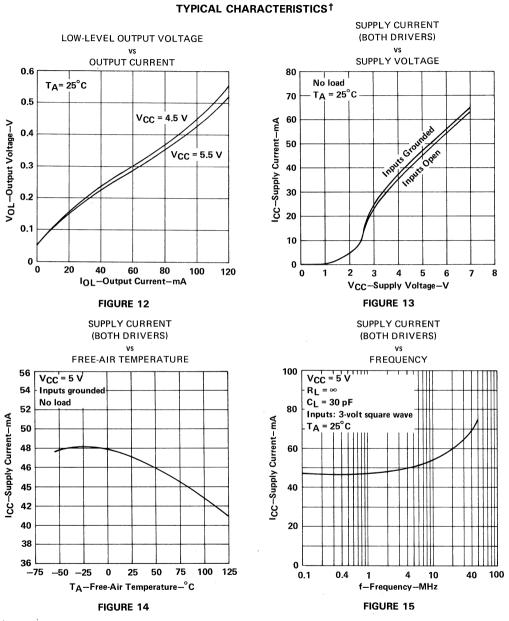






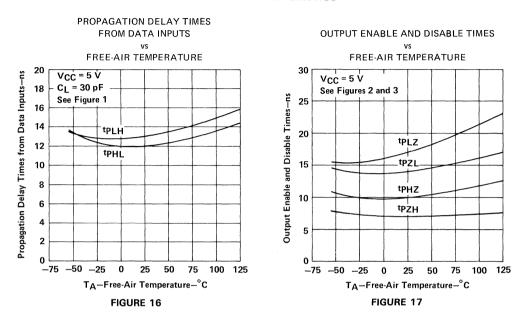


†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

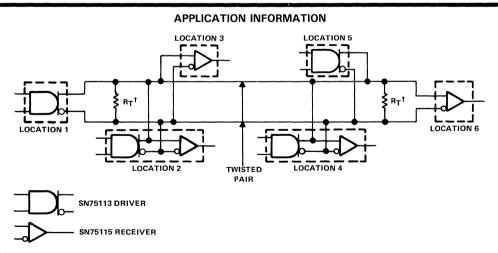


[†]Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.





†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.



[†]R_T = Z_O. A capacitor may be connected in series with R_T to reduce power dissipation.

FIGURE 18. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION



SN55114, SN75114 DUAL DIFFERENTIAL LINE DRIVERS

D1315, SEPTEMBER 1973-REVISED SEPTEMBER 1986

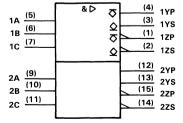
- Choice of Open-Collector, Open-Emitter, or Totem-Pole Outputs
- Single-Ended or Differential AND/NAND Outputs
- Single 5-V Supply
- Dual-Channel Operation
- TTL-Compatible
- Short-Circuit Protection
- High-Current Outputs
- Triple Inputs
- Clamp Diodes at Inputs and Outputs
- Designed for Use with SN55115 and SN75115 Differential Line Receivers
- Designed to Be Interchangeable with Fairchild 9614 Line Driver

description

The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with the high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL-compatible output levels, these devices may also be used as TTL expanders or phase splitters.

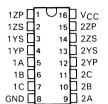
The SN55114 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN75114 is characterized for operation from 0 °C to 70 °C.

logic symbol†

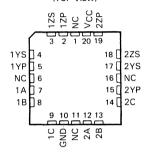


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN55114 . . . J PACKAGE SN75114 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



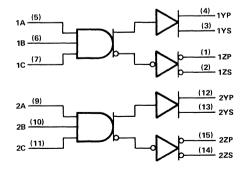
NC-No internal connection

FUNCTION TABLE

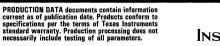
| | INPUTS | | | |
|--------------|------------|---------|---|---|
| Α | В | С | Υ | Z |
| Н | Н | Н | Н | L |
| ALL OTHER IN | РИТ СОМВІІ | NATIONS | L | Н |

H = high level, L = low level

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

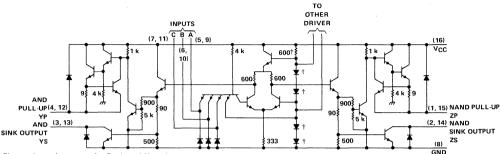




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SN55114, SN75114 DUAL DIFFERENTIAL LINE DRIVERS

schematic (each driver)



Pin numbers shown are for D, J, and N packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55114 | SN75114 | UNIT | | |
|--|------------------------------|------------|------|--|--|
| Supply voltage, V _{CC} (see Note 1) | 7 | 7 | V | | |
| Input voltage | 5.5 | 5.5 | V | | |
| Off-state voltage applied to open-collector outputs | 12 | 12 | V | | |
| Continuous total power dissipation (see Note 2) | See Dissipation Rating Table | | | | |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | °C | | |
| Storage temperature range | -65 to 150 | -65 to 150 | °C | | |
| Case temperature for 60 seconds: FK package | 260 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C | | |

- NOTES: 1. Voltage values are with respect to network ground terminal.
 - In the FK and J packages, SN55114 chips are either silver glass or alloy mounted. In the J package, SN75114 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | T _A = 70°C | T _A = 125°C |
|-------------|-----------------------|---------------------|-----------------------|------------------------|
| PACKAGE | POWER RATING | ABOVE $T_A = 25$ °C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°CC | 608 mW | |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55114) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75115) | 1025 mW | 8.2 mW/°C | 656 mw | _ |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN55114 | | | SN75114 | | | |
|--|-----|---------|-----|------|---------|------|------|--|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT | |
| Supply voltage, V _{CC1} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | |
| High-level input voltage, VIH | 2 | | | 2 | | | V | |
| Low-level input voltage, V _{IL} | | | 0.8 | | | 0.8 | V | |
| High-level output current, IOH | | | -40 | | | - 40 | mA | |
| Low-level output current, IOL | • | | 40 | | | 40 | mA | |
| Operating free-air temperature, TA | -55 | | 125 | 0 | | 70 | °C | |



[†]These components are common to both drivers. Resistor values shown are nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | DADAMETED | TEST CONDITIONS† | | | SN5511 | 4 | SN75114 | | | UNIT | | |
|---------|---|-----------------------|---------------------------|---|--------|------------------|---------|-----|------------------|-------|------|--|
| | PARAMETER | 16 | TEST CONDITIONS | | | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNII | |
| VIK | Input clamp voltage | $V_{CC} = MIN$, | $I_1 = -12 \text{ m/s}$ | \ | | -0.9 | - 1.5 | | -0.9 | -1.5 | V | |
| V | High-level output | $V_{CC} = MIN$, | $V_{IH} = 2 V$, | I _{OH} = -10 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V | |
| Vон | voltage | $V_{IL} = 0.8 V$, | | I _{OH} = -40 mA | 2 | 3 | | 2 | 3 | | v | |
| VOL | Low-level output | $V_{CC} = MIN$, | $V_{IH} = 2 V$, | | | 0.2 | 0.4 | | 0.2 | 0.45 | | |
| VOL | voltage | $V_{1L} = 0.8 V$, | $I_{OL} = 40 \text{ m/s}$ | ١ | | 0.2 | 0.4 | | 0.2 | 0.45 | | |
| Vau | Output clamp voltage $V_{CC} = 5 \text{ V}, I_{O} = 40 \text{ mA}, T_{A} = 2$ | | T _A = 25 °C | | 6.1 | 6.5 | | 6.1 | 6.5 | v | | |
| Voк | Output clamp voltage | $V_{CC} = MAX$ | $I_0 = -40 \text{ m}$ | A, $T_A = 25 ^{\circ}C$ | | - 1.1 | - 1.5 | | -1.1 | -1.5 | · | |
| | Off-state open-collector output current | | V _{OH} = 12 V | T _A = 25 °C | | 1 | 100 | | | | μΑ | |
| 10 | | | | | | | 200 | | | | | |
| IO(off) | | | Va 5 25 V | $V = \frac{T_A = 25 ^{\circ}\text{C}}{T_A = 70 ^{\circ}\text{C}}$ | | | | | 1 | 100 | | |
| | | | VOH = 5.25 | $T_A = 70 ^{\circ}C$ | | | | | | 200 | | |
| 11 | Input current at maximum input voltage | V _{CC} =MAX, | V _I = 5.5 V | | | | 1 | | | 1 | mA | |
| ۱н | High-level input current | V _{CC} = MAX | $, V_1 = 2.4 V$ | | | | 40 | | | 40 | μΑ | |
| IL | Low-level input current | $V_{CC} = MAX$ | $V_1 = 0.4 \ V$ | | | - 1.1 | - 1.6 | | - 1.1 | - 1.6 | mA | |
| los | Short-circuit | Voc - MAX | Vo =0 | T _A = 25 °C | -40 | - 90 | - 120 | -40 | _ 90 | -120 | mA | |
| 108 | output current§ | VCC = MAX, | VO0, | 1A-25 C | 40 | | 120 | 40 | 30 | 120 | | |
| loo | Supply current | All inputs at | O V, No load | i, V _{CC} =MAX | | 37 | 50 | | 37 | 50 | mA | |
| lcc | (both drivers) | $T_A = 25$ °C | | V _{CC} = 7 V | | 47 | 65 | | 47 | 70 | | |

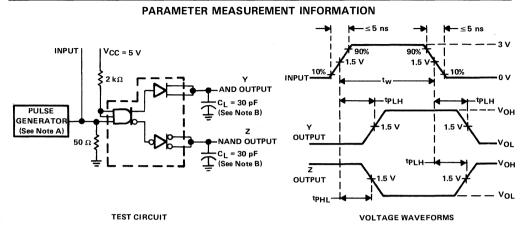
[†]All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | TEST | SN55114 | | | SN75114 | | | UNIT |
|-----------|--|----------------|---------|-----|-----|---------|-----|-----|------|
| | | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | ONIT |
| tPLH | Propagation delay time, low-to-high-level output | $C_L = 30 pF,$ | | 15 | 20 | | 15 | 30 | ns |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 1 | | 11 | 20 | | 11 | 30 | ns |

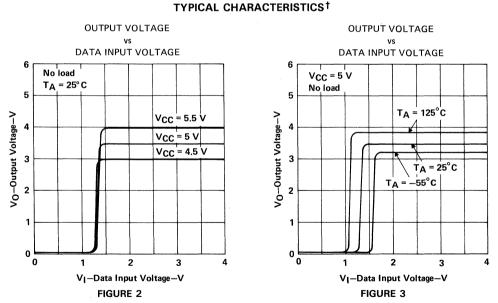
 $^{^{\}ddagger}AII$ typical values are at T_A = 25 °C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.

[§]Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.



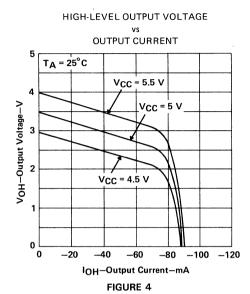
NOTES: A. The pulse generator has the following characteristics: $Z_0 = 500 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W \leq 100 \text{ ns}$. B. C_1 includes probe and jig capacitance.

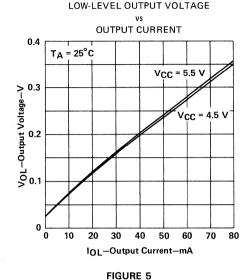
FIGURE 1. PROPAGATION DELAY TIMES



[†] Data for temperatures below 0 °C and above 70 °C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†





OUTPUT VOLTAGE



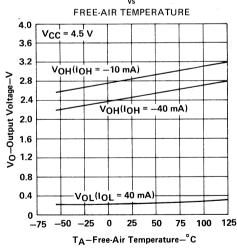


FIGURE 6

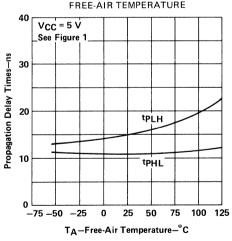
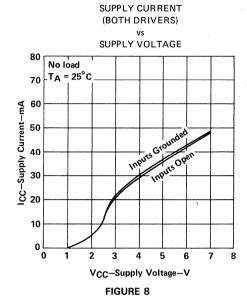


FIGURE 7

[†] Data for temperatures below 0 °C and above 70 °C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.



SUPPLY CURRENT (BOTH DRIVERS)

VS

FREE-AIR TEMPERATURE

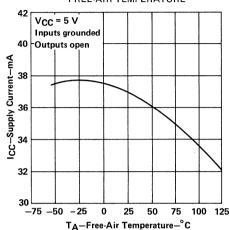
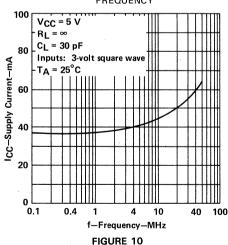


FIGURE 9

SUPPLY CURRENT (BOTH DRIVERS)

FREQUENCY



[†] Data for temperatures below 0 °C and above 70 °C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.



APPLICATION INFORMATION† 1/2 SN75114 DRIVER RT† TWISTED PAIR

 $^{\dagger}\,\text{R}_{T}\,=\,\text{Z}_{O}.$ A capacitor may be connected in series with R_{T} to reduce power dissipation.

FIGURE 11. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

SN55115, SN75115 DUAL DIFFERENTIAL LINE RECEIVERS

D1315, SEPTEMBER 1973-REVISED OCTOBER 1986

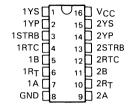
- Choice of Open-Collector or Active Pull-Up (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual-Channel Operation
- TTL Compatible
- ± 15 V Common-Mode Input Voltage Range
- Optional-Use Built-In 130-Ω Line-Terminating Resistor
- Individual Frequency Response Controls
- Individual Channel Strobes
- Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers
- Designed to Be Interchangeable With Fairchild 9615 Line Receivers

description

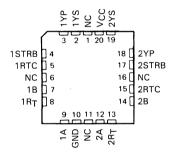
The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pull-up terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

The SN55115 is characterized for operation over the full military range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN75115 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

SN55115 . . . J PACKAGE SN75115 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55115 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

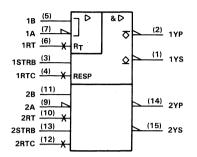
FUNCTION TABLE

| STROBE | DIFF INPUT | OUTPUT (YP AND YS TIED TOGETHER) |
|--------|---------------|-------------------------------------|
| L | Х | Н |
| н | L | н |
|] н | н | L |

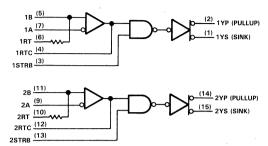
 $H = V_I \ge V_{IH}$ min or V_{ID} more positive than V_{TH} max $L = V_I \le V_{IL}$ max or V_{ID} more negative than V_{TL} max X = irrelevant

SN55115, SN75115 DUAL DIFFERENTIAL LINE RECEIVERS

logic symbol†

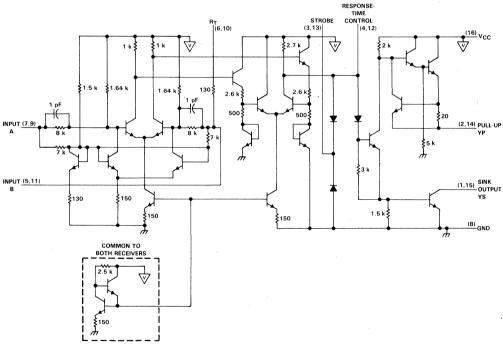


logic diagram (positive logic)



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each receiver)



Pin numbers shown are for D, J, and N packages. Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55115 | SN75115 | UNIT |
|--|------------------------------|------------|------|
| Supply voltage, V _{CC} (see Note 1) | 7 | 7 | V |
| Input voltage at A, B, and R _T inputs | ± 25 | ± 25 | V |
| Input voltage at strobe input | 5.5 | 5.5 | V |
| Off-state voltage applied to open-collector outputs | 14 | 14 | V |
| Continuous total power dissipation (see Note 2) | See Dissipation Rating Table | | |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C |

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 - 2. In the FK and J packages, SN55115 chips are either silver glass or alloy mounted and SN75115 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55115) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75115) | 1025 mW | 8.2 mW/°C | 656 mW | |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN55115 | | | SN75115 | | |
|--|------|---------|-----|------|---------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level (strobe) input voltage, VIH | 2.4 | | | 2.4 | | | V |
| Low-level (strobe) input voltage, VIL | | | 0.4 | | | 0.4 | V |
| High-level output current, IOH | | | -5 | | | -5 | mA |
| Low-level output current, IOL | | | 15 | | | 15 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

SN55115, SN75115 DUAL DIFFERENTIAL LINE RECEIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | t | | SN55115 | , | | SN75115 | | UNIT |
|-------------------|---|---|-----------------------------------|----------|------------------|------|-----------|------------------|-------|------|
| | PARAMETER | 1231 CONDITIONS | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNII |
| ∨ _{TH} § | Differential input high-threshold voltage | $V_{O} = 0.4 \text{ V}, I_{OL} = 15 \text{ mA},$ | V _{IC} = 0 | | | 500 | | | 500 | mV |
| V _{TL} § | Differential input low-threshold voltage | $V_0 = 2.4 \text{ V}, I_{OH} = -5 \text{ mA},$ | V _{IC} = 0 | - 500¶ | | | - 500¶ | | | mV |
| | Common-mode | | | +15 | + 24 | | +15 | + 24 | | ,, |
| VICR | input voltage range | $V_{ID} = \pm 1 \text{ V}$ | | to 15 | to ~ 19 | | to -15 | to 19 | | V |
| | | $V_{CC} = MIN, V_{ID} = -0.5 V,$ | T _A = MIN | 2.2 | | | 2.4 | | | v |
| v_{OH} | High-level output voltage | $V_{CC} = MIN, V_{ID} = -0.5 V,$ $I_{OH} = -5 \text{ mA}$ | $T_A = MIN$ $T_A = 25 ^{\circ}C$ | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | , | IOH = -5 IIIA | T _A = MAX | 2.4 | | | 2.4 | | | |
| V _{OL} | Low-level output voltage | $V_{CC} = MIN, V_{ID} = 0.5 V,$ $I_{OL} = 15 \text{ mA}$ | | | 0.22 | 0.4 | | 0.22 | 0.45 | ٧ |
| | | .,, ., | T _A = MIN | | | -0.9 | | | -0.9 | |
| IIL | Low-level input current | $V_{CC} = MAX$, $V_I = 0.4 V$, | T _A = 25°C | | -0.5 | -0.7 | | -0.5 | -0.7 | mA |
| | | Other input at 5.5 V | $T_A = MAX$ | | | -0.7 | | | -0.7 | |
| lau | High-level strobe current | $V_{CC} = MIN$, $V_{ID} = -0.5 V$, | = -0.5 V, T _A = 25°C | | | 2 | | | 5 | μА |
| ISH | riigiriever strobe current | V _{strobe} = 4.5 V | $T_A = MAX$ | | | 5 | | | 10 | μ^ |
| ^I SL | Low-level strobe current | $V_{CC} = MAX$, $V_{ID} = 0.5 V$, $V_{strobe} = 0.4 V$ | T _A = 25°C | | - 1.15 | -2.4 | | -1.15 | -2.4 | mA |
| I(RTC) | Response-time-control current | $V_{CC} = MAX$, $V_{ID} = 0.5 V$, $V_{RC} = 0$ | T _A ≈ 25°C | -1.2 | -3.4 | | - 1.2 | -3.4 | | mA |
| | , | $V_{CC} = MIN$, $V_{OH} = 12 V$, | $T_A = 25$ °C | | | 100 | | | | |
| la | Off-state open-collector | V _{ID} = -4.5 V | TA = MAX | | | 200 | | | | μΑ |
| IO(off) | output current | $V_{CC} = MIN$, $V_{OH} = 5.25 V$, | $T_A = 25$ °C | | | | | | 100 |] "^ |
| | | $V_{ID} = -4.75 \text{ V}$ | $T_A = MAX$ | | | | | | 200 | |
| R _T | Line-terminating resistance | V _{CC} = 5 V | T _A = 25°C | 77 | 130 | 167 | 74 | 130 | 179 | Ω |
| los | Short-circuit output current | $V_{CC} = MAX$, $V_{O} = 0$, $V_{ID} = -0.5 \text{ V}$ | T _A = 25°C | - 15 | - 40 | -80 | -14 | -40 | - 100 | mA |
| ¹ CC | Supply current (both receivers) | $V_{CC} = MAX$, $V_{ID} = 0.5 V$, $V_{IC} = 0$ | T _A = 25°C | | 32 | 50 | | 32 | 50 | mA |

[†] Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 30 \text{ pF}$, $T_A = 25 ^{\circ}\text{C}$

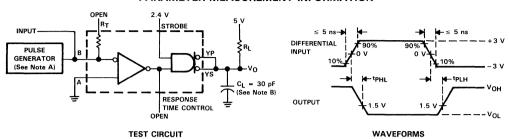
| PARAMETER | | TEST CONDITIONS | | SN55115 | | | SN75115 | | |
|------------------|--------------------------|--|-----|---------|-----|-----|---------|-----|------|
| | PANAIVIE I EN | TEST CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| tPLH | Propagation delay time, | $R_1 = 3.9 \text{ k}\Omega$, See Figure 1 | | -18 | 50 | | 18 | 75 | ns |
| io lo | low-to-high-level output | | 1 | | | | | | |
| tou | Propagation delay time, | $R_1 = 390 \Omega$, See Figure 1 | | 20 | 50 | | 20 | 75 | ns |
| ^t PHL | high-to-low-level output | NL = 390 12, See Figure 1 | | 20 | 30 | 20 | 75 | lis | |

 $^{^{\}ddagger}$ All typical values are at VCC = 5 V, TA = 25 °C, and V_{IC} = 0.

[§] Differential voltages are at the B input terminal with respect to the A input terminal.

The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

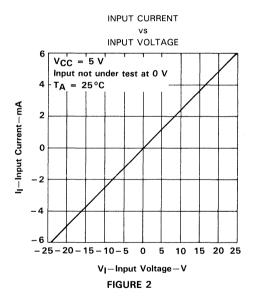
I Only one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one second.

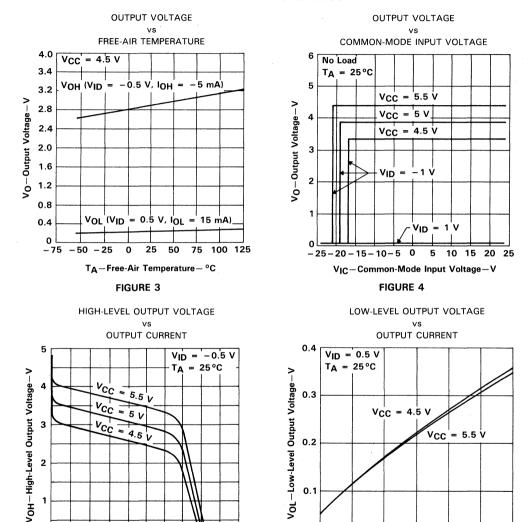


NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \,\Omega$, PRR $\leq 500 \,kHz$, $t_W \leq 100 \,ns$, duty cycle = 50%. B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS





0.1

0

0

10

15

IOL-Low-Level Output Current-mA

FIGURE 6

20

25

30



0 0

-20

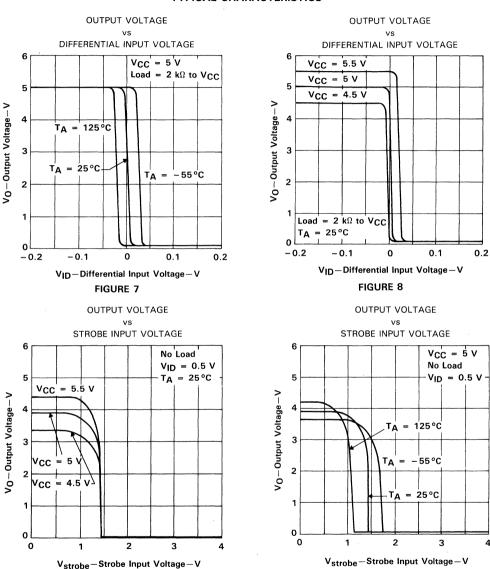
- 30

IOH-High-Level Output Current-mA

FIGURE 5

- 40

Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.



[†] Data for temperatures below 0 °C and above 70 °C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull up connected to the sink output.

FIGURE 9



FIGURE 10

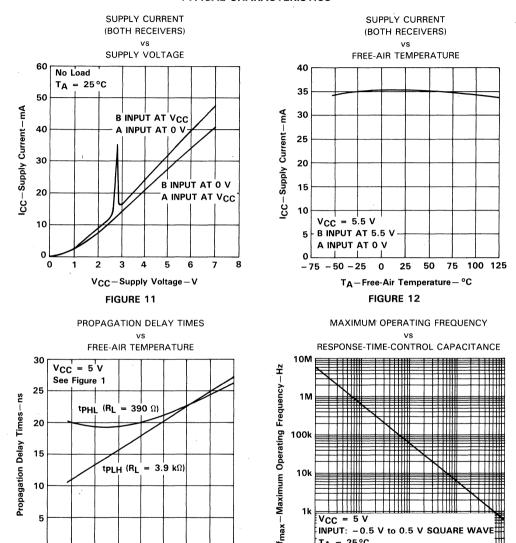


FIGURE 13 FIGURE 14 † Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

100 125

VCC = 5 V

TA = 25°C

0.01

100

0.001

INPUT: -0.5 V to 0.5 V SQUARE WA

0.1

Response-Time-Control Capacitance - µF

1

10



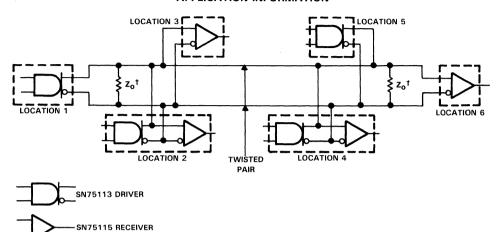
5

-75-50 -25

25 50 75

TA-Free-Air Temperature

APPLICATION INFORMATION



 $^{^{\}dagger}\text{A}$ capacitor may be connected in series with Z_{O} to reduce power dissipation.

FIGURE 15. BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

SN55116, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

D2143, MAY 1976-REVISED MAY 1990

Features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, SN75117) or Enable (SN75118, SN75119)
- Designed for Party-Line (Data-Bus)
 Applications
- Choice of Ceramic or Plastic Packages

Additional features of the SN55116/SN75116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

Additional features of the SN75117

 Driver Output Internally Connected to Receiver Input

The S¹ /5 18 is an SN75116 with 3-State Receiver Output Circuitry The SN75119 is an SN75117 with 3-State Receiver Output Circuitry

description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a 3-state differential line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver inputs and receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 3-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

The '116 and SN75118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver combined. The driver performs the dual input AND and NAND functions when enabled, or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package pins. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink pins together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and SN75118 features a differential-input circuit having a common-mode voltage range of \pm 15 V. An internal 130- Ω resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control pin allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the SN75118 has an output-enable for the 3-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the VCC and ground pins.

The SN75117 and SN75119 circuits provide the basic driver and receiver functions of the '116 and SN75118, but use a package that is only half as large. The SN75117 and SN75119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the SN75117 receiver has an output strobe while the SN75119 receiver has a 3-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency-response controls.

The SN55116 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to $125\,^{\circ}$ C; the SN75116, SN75117, SN75118, and SN75119 are characterized for operation from $0\,^{\circ}$ C to $70\,^{\circ}$ C.



SN55116, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

NC-No internal connection

| SN55116 J PACKAGE SN75116 D, J, OR N PACKAGE | SN75118 D, J, OR N PACKAGE (TOP VIEW) |
|---|---|
| TOP VIEW | DZP 1 16 VCC DZS 2 15 DB DYS 3 14 DA DYP 4 13 DE RA 5 12 RYP RT 6 11 RYS RB 7 10 RE GND 8 9 RTC |
| SN55116 FK PACKAGE (TOP VIEW) | SN75117 D, JG, OR P PACKAGE (TOP VIEW) |
| S | DI 1 8 VCC B 2 7 DE A 3 6 RY GND 4 5 RS |
| NC 6 | SN75119 D, JG, OR P PACKAGE (TOP VIEW) |
| # 9 10 11 12 13 # 9 20 E & | DI |

OUTPUTS

Α

H L

Z Z

SN75117, SN75119

FUNCTION TABLE

OF DRIVER

'116, SN75118 FUNCTION TABLE OF DRIVER

| ı | NPUT | ОUТ | PUTS | |
|----|------|-----|------|----|
| DE | DA | DB | DY | DZ |
| L | Х | Х | Z | Z |
| н | L | X | L | Н |
| н | Х | L | L | Н |
| Н | Н | Н | Н | L |

'116, SN75118 FUNCTION TABLE OF RECEIVER

| RS/RE | DIFF | OUTPUT RY | | | | |
|-------|-------|-----------|---------|--|--|--|
| NS/NE | INPUT | ′116 | SN75118 | | | |
| L | Х | Н | Z | | | |
| н | L | н | Н | | | |
| н | н | L | L | | | |

 $H = \text{high level (V}_I \geq \text{V}_{IH} \text{ min or V}_{ID} \text{ more positive than V}_{TH} \text{ max)}$

 $L = low level (V_I \le V_{IL} max or V_{ID} more negative than V_{TL} max)$

X = irrelevant

Z = high impedance (off)

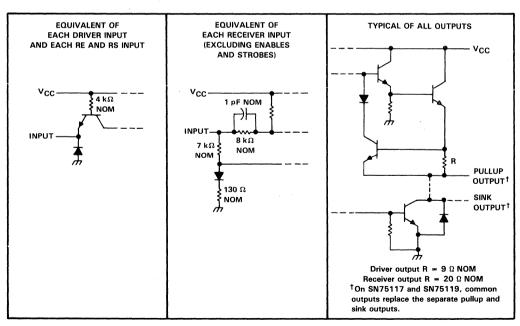
SN75117, SN75119 FUNCTION TABLE OF RECEIVER

LHLH

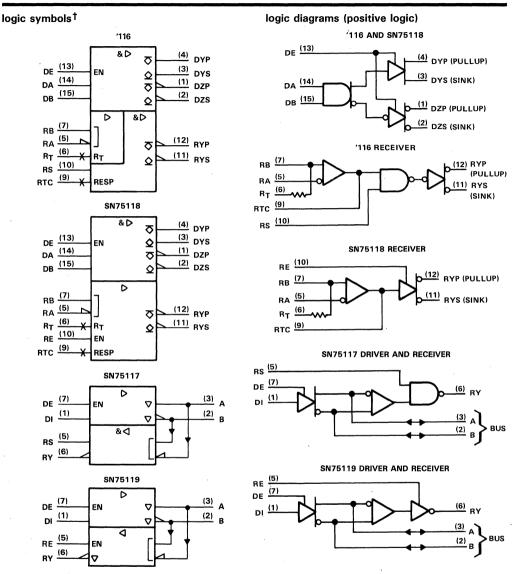
Х

| | INP | JTS | OUTPUT RY | | | | |
|---|-----|-------|-----------|---------|--|--|--|
| Α | В | RS/RE | SN75117 | SN75119 | | | |
| H | L | Н | Н | Н | | | |
| L | Н | Н | L | L | | | |
| X | Х | L | Н | Z | | | |

schematics of inputs and outputs



SN55116, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown for '116 and SN75118 are for J and N packages; those shown for SN75117 and SN75119 are for JG and P packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | ′116, SN75118 | SN75117, SN75119 | UNIT |
|---------------------------------|------------------------|------------------|---------------------|------|
| Supply voltage, VCC (see Not | e 1) | 7 | 7 | V |
| | DA, DB, DE, DI, RE, RS | 5.5 | 5.5 | |
| Input voltage, V _I | RA, RB, RT | ±25 | | 7 v |
| | A and B | | 0 to 6 | 1 |
| Off-state voltage applied to op | pen-collector outputs | 12 | | V |

| | SN55116 | SN75116 THRU SN75119 | UNIT |
|---|-------------|----------------------------|------|
| Continuous total power dissipation (see Note 2) | See Dissi | pation Rating Ta | ble |
| Operating free-air temperature range | - 55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J and JG packages | 300 | 300 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package | | 260 | °C |

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. In the FK and J packages, SN55116 chip is alloy mounted and SN75116 through SN75119 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|----------------|---------------------------------------|---|---------------------------------------|--|
| D (8 pin) | 725 mW | 5.8 mW/°C | 464 mW | _ |
| D (16 pin) | 950 mW | 7.6 mW/°C | 608 mW | - |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55116) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (all others) | 1025 mW | 8.2 mW/°C | 656 mW | _ |
| JG | 825 mW | 6.6 mW/°C | 528 mW | _ |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |
| Р | 1000 mW | 8.0 mW/°C | 640 mW | _ |

recommended operating conditions

| PARAMETER | | | SN5511 | 16 | SN75′ | | | UNIT | |
|--|---------------------|-----|--------|------|-------|-----|------|------|--|
| PARAMETER | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT | |
| Supply voltage, V _{CC} | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | ٧ | |
| High-level input voltage, VIH | All inputs except | 2 | | | 2 | | | ٧ | |
| Low-level input voltage, V _{IL} | differential inputs | | | 0.8 | | | 0.8 | ٧ | |
| High level autout august 1 | Drivers | | | - 40 | | | -40 | ^ | |
| High-level output current, IOH | Receivers | | | -5 | | | - 5 | mA | |
| 1 1 1 1 | Drivers | | | 40 | | | 40 | | |
| Low-level output current, IOL | Receivers | | | 15 | | | 15 | mA | |
| Description in the second | ′116, ′118 | | | ± 15 | | | ±15 | V | |
| Receiver input voltage, V _I | ′117, ′119 | 0 | | 6 | 0 | | 6 | V | |
| C | ′116, ′118 | | | ±15 | | | ±15 | ., | |
| Common mode receiver input voltage, VICR | ′117, ′119 | 0 | | 6 | 0 | | 6 | V | |
| Operating free-air temperature, TA | | -55 | | 125 | 0 | | 70 | °C | |

SN55116, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

| | PARAMETE | n | | TEST CONDITIONS T | | ′1′ | 16, SN7! | 5118 | SN75117, SN75119 | | | UNIT |
|------------------|------------------|----------------|--------------------------|--|---------------------------|-----|------------------|-------|------------------|------|-------|----------|
| | PARAMETE | in . | | TEST CONDITIONS | | MIN | TYP [‡] | MAX | MIN | TYP‡ | MAX | UNIT |
| V _{IK} | Input clamp v | oltage | V _{CC} = MIN, | I _I = -12 mA | | | -0.9 | -1.5 | | -0.9 | - 1.5 | V |
| | | | 1 | T 0500 (0NE5440) | I _{OH} = -10 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| Vон | High-level out | nut voltage | V 08 V | $T_A = 0$ °C to 70°C (SN75') | I _{OH} = -40 mA | 2 | 3 | | 2 | 3 | | V |
| ۷ОН | riigii-level out | put voltage | V ₁₁ = 2.0 V, | $T_A = -55$ °C to 125 °C | $I_{OH} = -10 \text{ mA}$ | 2 | | | 2 | | | • |
| | | | VIH - Z V | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ | | 1.8 | | | 1.8 | | | |
| VOL | Low-level out | nut voltage | V _{CC} = MIN, | $V_{IH} = 2 V$ | | | | 0.4 | | | 0.4 | v |
| VOL | LOW ICVCI OUL | put voitage | | I _{OL} = 40 mA | | | | | | | 0.7 | |
| Vok | Output clamp | voltage | $V_{CC} = MAX,$ | $I_0 = -40$ mA, DE at 0.8 V | | | | -1.5 | | | - 1.5 | V |
| | Off-state oper | n-collector | V _{CC} = MAX, | T _A = 25°C | | | 1 | -10 | | | | |
| IO(off) | output curren | | $V_{O} = 12 \text{ V}$ | | SN55116 | | | 200 | | | | μΑ |
| | output ourion | | 10 - 12 1 | TA = WAX | SN75′ | | | 20 | | | | |
| | | | V _{CC} = MAX, | $V_0 = 0$ to V_{CC} , DE at 0.8 | V, | | | ±10 | | | | |
| | Off-state | | $T_A = 25$ °C | | | | | ± 10 | | | | |
| loz | (high-impedan | ce-state) | V _{CC} = MAX, | | SN55116 | | | - 300 | | | | μΑ |
| | output curren | t | DE at 0.8 V, | $V_0 = 0.4 \text{ V to } V_{CC}$ | SN55116 | | | ±150 | | | | |
| | | | $T_A = MAX$ | $V_O = 0$ to V_{CC} | SN75′ | | | ± 20 | | | | |
| | Input current | | | | | | | | | | | |
| l _l | at maximum | | V _{CC} = MAX, | $V_{ } = 5.5 V$ | | | | 1 | | | 1 | mA |
| | input voltage | Driver or | | | | | | | | | | |
| ΊΗ | High-level | enable | V _{CC} = MAX, | V1 = 2 4 V | | | | 40 | | | 40 | μΑ |
| חוי | input current | input | | | | | | | | | | |
| I _I L | Low-level | , | VCC = MAX, | $V_1 = 0.4 \text{ V}$ | | | | -1.6 | | | - 1.6 | mA |
| -112 | input current | | 100 | ., | | | | | | | | |
| los | Short-circuit | _ | Vcc = MAX | $V_{O} = 0, T_{A} = 25 ^{\circ}\text{C}$ | | -40 | | - 120 | -40 | | - 120 | mA |
| .03 | output curren | t [§] | | | | | | | | | 0 | |
| lcc | Supply curren | t (driver | Vcc = MAX | $T_A = 25^{\circ}C$ | | | 42 | 60 | | 42 | 60 | mA |
| | and receiver of | combined) | - CC = 1,,,,,,,, | ·A 200 | | | -74 | | | 72 | | 11163 |

[†]All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 30 \text{ pF}$, $T_A = 25 ^{\circ}\text{C}$

driver section

| PARAMETER | TEST CONDITIONS | | | TYP | MAX | UNIT |
|---|----------------------|---------------|--|-----|-----|------|
| t _{PLH} Propagation delay time, low-to-high-level output | | Con Firmer 12 | | 14 | 30 | |
| t _{PHL} Propagation delay time, high-to-low-level output | • | See Figure 13 | | 12 | 30 | ns |
| tpZH Output enable time to high level | $R_L = 180 \Omega$, | See Figure 14 | | 8 | 20 | ns |
| tpZL Output enable time to low level | $R_L = 250 \Omega$, | See Figure 15 | | 17 | 40 | ns |
| t _{PHZ} Output disable time from high level | $R_L = 180 \Omega$, | See Figure 14 | | 16 | 30 | ns |
| tpLZ Output disable time from low level | $R_L = 250 \Omega$, | See Figure 15 | | 20 | 35 | ns |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C.

Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) receiver section

| | PARAMETER | | | TEGT CONDITION | -t | 1116 | s, SN75 | 118 | SN75117, SN75119 | | | |
|----------------|--------------------------------|---------|--------------------------------------|---|--|-----------|------------------|------|------------------|------------------|------|------|
| | PARAMETER | | | TEST CONDITIONS | S' | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNIT |
| | Differential input | | V _O = 0.4 V, | I _{OL} = 15 mA, | V _{CC} = MIN, V _{ICR} = 0, See Note 4 | | | 0.5 | | | 0.5 | v |
| VTH | high-threshold vo | itage § | See Note 3 | : | V _{CC} = 5 V, V _{ICR} = MAX, See Note 5 | , | | 1 | | | 1 | V |
| \/-· | Differential input | | V _O = 2.4 V, | I _{OH} = -5 mA, | V _{CC} = MIN, V _{ICR} = 0, See Note 4 | -0.5¶ | | | -0.5¶ | | | v |
| VTL | low-threshold vol | tage § | See Note 3 | | V _{CC} = 5 V, V _{ICR} = MAX, See Note 5 | ~ 1¶ | -19 | | -19 | | | V |
| | | | | | | 15 | | | 6 | | | |
| VI | Input voltage ran | ge# | V _{CC} = 5 V, | V _{ID} = -1 V or 1 V, | See Note 3 | to -15 | | | to O | | | V |
| ., | High-level output voltage | | I _{OH} = -5 mA, | V _{CC} = MIN, V _{ICR} = 0, | V _{ID} = -0.5 V, See Note 4 | 2.4 | | | 2.4 | | | V |
| Vон | High-level output | voitage | See Note 3 | V _{CC} = 5 V, V _{ICR} = MAX, | V _{ID} = -1 V, See Note 5 | 2.4 | | | 2.4 | | | ľ |
| | | | IOL = 15 mA, | V _{CC} = MIN, V _{ICR} = 0, | V _{ID} = 0.5 V, See Note 4 | | | 0.4 | | | 0.4 | v |
| VOL | Low-level output | voitage | See Note 3 | V _{CC} = 5 V, V _{ICR} = MAX, | V _{ID} = 1 V, See Note 5 | | | 0.4 | | _ | 0.4 | ľ |
| | | | V _{CC} = MAX, | $V_I = 0$, | Other input at 0 V | | -0.5 | -0.9 | | -0.5 | - 1 | |
| I(rec) | Receiver input cu | rrent | See Note 3 | V ₁ = 0.4 V, | Other input at 2.4 V | | -0.4 | -0.7 | | -0.4 | -0.8 | mA |
| | | | See Note 3 | $V_1 = 2.4 V,$ | Other input at 0.4 V | | 0.1 | 0.3 | | 0.1 | 0.4 | |
| l _l | Input current at maximum input | Strobe | $V_{CC} = MIN,$ $V_{strobe} = 4.5 V$ | $V_{\text{ID}} = -0.5 \text{ V},$ | ′116, SN75117 | | | 5 | | | 5 | μΑ |
| | voltage | Enable | V _{CC} = MAX, | V _I = 5.5 V | SN75118, SN75119 | | | 1 | | | 1 | mA |

[†]Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$, and $V_{IC} = 0$.

[§]Differential voltages are at the B input terminal with respect to the A input terminal. Neither receiver input of the SN75117 or SN75119 should be taken negative with respect to GND.

The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

[#]Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. Measurement of these characteristics on the SN75117 and SN75119 requires the driver to be disabled with the driver enable at 0.8 V.

^{4.} This applies with the less positive receiver input grounded. For SN55116, $V_{ID} = -1 \text{ V}$.

^{5.} For '116 and SN75118, this applies with the more positive receiver input at 15 V or the more negative receiver input at -15 V. For SN75117 and SN75119, this applies with the more positive receiver input at 6 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued) receiver section

| | PARAMETER | | | TEST CONDITION | uet | ′11 | 6, SN75 | 118 | SN75117, SN75119 | | | UNIT |
|----------------|---------------------------------------|-----------|---------------------------------------|--|-----------------------|------|---------|------|------------------|------------------|-------|------|
| | PANAIVIETEN | | | TEST CONDITION | 45 · | MIN | TYP‡ | MAX | MIN | TYP [‡] | MAX | ONIT |
| ΊΗ | High-level input current | Enable | V _{CC} = MAX, | V _I = 2.4 V | SN75118, SN75119 | | | 40 | | | 40 | μΑ |
| hL. | Low-level | Strobe | $V_{CC} = MAX,$ $V_{strobe} = 0.4 V,$ | V _{ID} = 0.5 V, See Note 4 | ′116, SN75117 | | | -2.4 | | | - 2.4 | mA |
| | input current | Enable | $V_{CC} = MAX,$ | $V_I = 0.4 V$ | SN75118, SN75119 | | | 1.6 | | | -1.6 | |
| I(RC) | Response-time-co | ntrol | V _{CC} = MAX, RC at 0 V, | V _{ID} = 0.5 V, See Note 4 | T _A = 25°C | -1.2 | | | | | | mA |
| | | | $V_{CC} = MAX,$ | $T_A = 25$ °C | | | 1 | 10 | | | | |
| IO(off | Off-state open-co output current | llector | $V_0 = 12 V$, | $T_A = MAX$ | SN55116 | | | 200 | | | | μΑ |
| | output current | | $V_{ID} = -1 V$ | IA = WAX | SN75 | | | 20 | | | | |
| | Off-state | | $V_{CC} = MAX$, | $T_A = 25$ °C | SN75118, SN75119 | | | ± 10 | | | ±10 | |
| loz | (high-impedance | state) | $V_O = 0$ to V_{CC} , | T MAY | SN75118 | | | ± 20 | | | | μΑ |
| | output current | | RE at 0.4 V | $T_A = MAX$ | SN75119 | | | | | | ± 20 | |
| R _T | Line-terminating r | esistance | V _{CC} = 5 V | | T _A = 25°C | 77 | | 167 | | | | Ω |
| los | Short-circuit output current§ | | $V_{CC} = MAX,$ $V_{ID} = -0.5 V,$ | V _O = 0, See Note 4 | T _A = 25°C | -15 | | -80 | - 15 | | -80 | mA |
| lcc | Supply current (d and receiver com | | V _{CC} = MAX, See Note 4 | V _{ID} = 0.5 V, | T _A = 25°C | | 42 | 60 | | 42 | 60 | mA |

SN55116, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC}=5$ V, $T_A=25$ °C, and $V_{IC}=0$. 5 Not more than one output should be shorted at a time.

NOTE 4: This applies with the less positive receiver input grounded. For SN55116, $V_{\mbox{ID}} = -1 \mbox{ V}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 30 \text{ pF}$, $T_A = 25 ^{\circ}\text{C}$

receiver section

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------------|--|------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-l | high-level output $R_1 = 400 \Omega$, See Figure 16 | | | 20 | 75 | ns |
| ^t PHL | Propagation delay time, high-to-low-l | evel output | NE = 400 12, See Figure 10 | | 17 | 75 | ns |
| ^t PZH | Output enable time to high level | SN75118 | $R_L = 480 \Omega$, See Figure 14 | | 9 | 20 | ns |
| tPZL | Output enable time to low level | and | $R_L = 250 \Omega$, See Figure 15 | | 16 | 35 | ns |
| tPHZ | Output disable time from high level | SN75119 | $R_L = 480 \Omega$, See Figure 14 | | 12 | 30 | ns |
| tPLZ | Output disable time from low level | only | $R_L = 250 \Omega$, See Figure 15 | | 17 | 35 | ns |

TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE vs DRIVER INPUT VOLTAGE

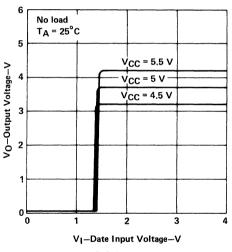


FIGURE 1

DRIVER OUTPUT VOLTAGE VS DRIVER INPUT VOLTAGE

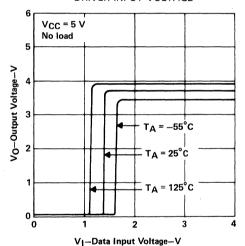


FIGURE 2

TYPICAL CHARACTERISTICS DRIVER HIGH-LEVEL OUTPUT VOLTAGE DRIVER LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT vs OUTPUT CURRENT 0.6 TA = 25°C $T_A = 25^{\circ}C$ VOH-High-Level Output Voltage-V 5 0.5 VOL-Low-Level Output Voltage-V V_{CC} = 4.5 V 4 0.4 V_{CC} = 5.5 V V_{CC} = 5.5 V V_{CC} = 5 V 3 CC = 4.5 V 0.3 2 0.2 0.1 -60 -100 -20 -40 -80 20 80 100 40 60 120 IOH-High-Level Output Current-mA IOL-Low-Level Output Current-mA FIGURE 3 FIGURE 4 DRIVER PROPAGATION DELAY TIMES DRIVER OUTPUT ENABLE AND DISABLE TIMES vs FREE-AIR TEMPERATURE[†] FREE-AIR TEMPERATURE[†] 20 30 Vcc = 5 V V_{CC} = 5 V C_L = 30 pF 18 See Note 6 See Figure 13 **Output Enable and Disable Times—ns** 25 16 Propagation Delay Times—ns **tPLH** 14 **tPLZ** 20 12 **tPZL tPHL tPHZ** 10 15 8 10 6 tPZH 4 5 2 25 50 100 125 _75 -50 -250 75 125 _75 <u>_</u>50 25 50 75 100

TA-Free-Air Temperature-°C

FIGURE 5

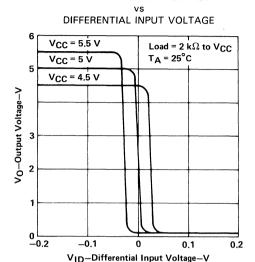


TA-Free-Air Temperature-°C

FIGURE 6

[†] Data for temperatures below 0 °C and above 70 °C are applicable to SN55116. NOTE 6: For tp_{ZH} and tp_{HZ}: $R_L = 180 \Omega$, see Figure 14. For tp_{ZH} and tp_{LZ}: $R_L = 250 \Omega$, see Figure 15.

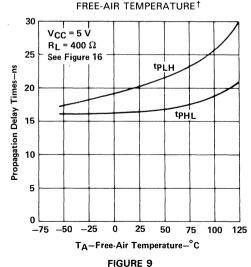
TYPICAL CHARACTERISTICS



RECEIVER OUTPUT VOLTAGE

RECEIVER PROPAGATION DELAY TIMES

FIGURE 7



RECEIVER OUTPUT VOLTAGE



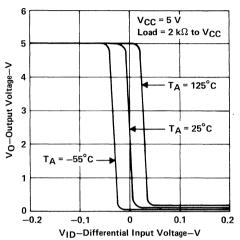
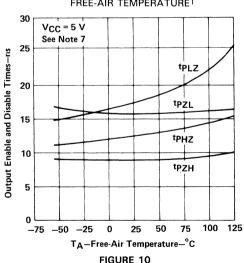


FIGURE 8

RECEIVER OUTPUT ENABLE AND DISABLE TIMES

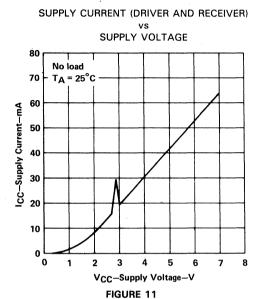
FREE-AIR TEMPERATURE[†]

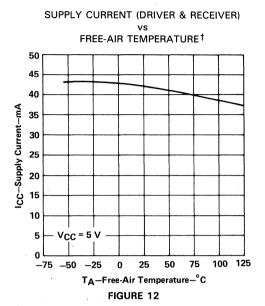


[†]Data for temperatures below 0 °C and above 70 °C are applicable to SN55116. NOTE 7: For tpzH and tpHz: $R_L = 480 \Omega$, see Figure 14. For tpzL and tpLz: $R_L = 250 \Omega$, see Figure 15.



TYPICAL CHARACTERISTICS





[†] Data for temperatures below 0°C and above 70°C are applicable to SN55116.

PARAMETER MEASUREMENT INFORMATION FROM OUTPUT TEST TEST FROM OUTPUT POINT POINT UNDER TEST UNDER TEST = 30 pF $C_1 = 30 pF$ (See Note B) (See Note B) LOAD CIRCUIT LOAD CIRCUIT - ≤5 ns 90% ≤5 ns 90% INPUT 1.5 \ 90% an% INPUT 1.5 t_{PHL} **→** tPLH 10% NAND 1.5 V OUTPUT OUTPUT tPLH-1.5 V AND 1.5 V OUTPUT VOL **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** FIGURE 13. tplH and tpHL (DRIVERS ONLY) FIGURE 14. tpzH and tpHZ TEST POINT $R_1 = 250 \Omega$ = **400** Ω FROM OUTPUT FROM OUTPUT UNDER TEST POINT UNDER TEST CL = 30 pF $C_1 = 30 pF$ (See Note C) (See Note B) (See Note B) LOAD CIRCUIT LOAD CIRCUIT 90% **4**—≤5 ns - **≤**5 ns INPUT 90% 90% B INPUT 50% 50% (See Note E) (See Note E) ^tPZL tPHL **4**−tPLH 0.5 V OUTPUT OUTPUT

- NOTES: A. Input pulses are supplied by generators having the following characteristics $Z_0 = 50 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$.
 - B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

FIGURE 15. tpzL and tpLZ

- C. All diodes are 1N3064 or equivalent.
- D. When testing the '116 and SN75118 receiver sections, the response-time control and the termination resistor pins are left open.

VOLTAGE WAVEFORMS
FIGURE 16. tpLH and tpHL (RECEIVERS ONLY)

E. For '116 and SN75118, V $_H=3$ V, V $_L=-3$ V, the A input is at 0 V. For SN75117 and SN75119, V $_H=3$ V, V $_L=0$, the A input is at 1.5 V.



D1334, SEPTEMBER 1973-REVISED SEPTEMBER 1986

- Designed for Digital Data Transmission over 50-Ω to 500-Ω Coaxial Cable, Strip Line, or Twisted Pair
- High-Speed
 t_{nd} = 20 ns Max at C_I = 15 pF
- TTL Compatible With Single 5-V Supply
- 2.4-V Output at IOH = -75 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receivers SN55122, SN75122
- Designed to Be Interchangeable With Signetics N8T13

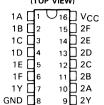
description

The SN55121 and SN75121 dual line drivers are designed for digital data transmission over lines having impedances from 50 to 500 ohms. They are also compatible with standard TTL logic and supply voltage levels.

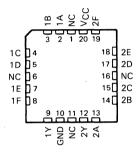
The low-impedance emitter-follower outputs of the SN55121 and SN75121 will drive terminated lines such as coaxial cable or twisted pairs. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 V. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55121 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN75121 is characterized for operation from 0 °C to 70 °C.

SN55121 . . . J PACKAGE SN75121 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55121 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

| | OUTPUT | | | | | |
|---|---------|---------|------|---------|----|---|
| A | В | С | D | Ε | F | Υ |
| Н | Н | Н | Н | Х | Х | Н |
| Χ | Х | Х | Х | Н | Н | н |
| Δ | II othe | r input | comb | ination | ıs | L |

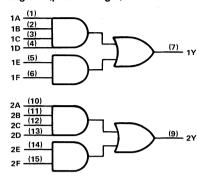
H = high level

L = low level

X = irrelevant

logic symbol† 1A (1) ≥1D 1B (2) 1C (3) (7) 1Y ℧ 1D (4) 1E (5) (6) (10) 2B 2C (12) (9) 2Y (13)2D 2E (14)

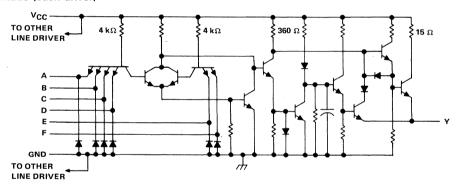
logic diagram (positive logic)



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

schematic (each driver)

2F (15)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55121 | SN75121 | UNIT |
|--|------------------------------|------------|------|
| Supply voltage, V _{CC} (see Note 1) | 6 | 6 | V |
| Input voltage | 6 | 6 | V . |
| Output voltage | 6 | 6 | V |
| Continuous total power dissipation (see Note 2) | See Dissipation Rating Table | | |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | 300 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C |

- NOTES: 1. All voltage values are with respect to both ground terminals connected together.
 - 2. In the FK and J packages, SN55121 chips are either silver glass or alloy mounted and SN75121 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55121) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75121) | 1025 mW | 8.2 mW/°C | 656 mW | _ |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN5512 | 1 | SN75121 | | | UNIT |
|------------------------------------|------|--------|------|---------|-----|------|------|
| • | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | V |
| High-level output current, IOH | | | - 75 | | | - 75 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| | PARAMETER | Т | EST CONDITIONS | | MIN | MAX | UNIT |
|--------------------|---|------------------------|----------------------------|----------------|-------|-------|------|
| VIK | Input clamp voltage | $V_{CC} = 5 V$, | I _I = -12 mA | | | - 1.5 | V |
| V _{(BR)I} | Input breakdown voltage | V _{CC} = 5 V, | i _j = 10 mA | | 5.5 | | V |
| Voн | High-level output voltage | $V_{IH} = 2 V$, | $I_{OH} = -75 \text{ mA},$ | See Note 3 | 2.4 | | V |
| lavi | High-level output current | $V_{CC} = 5 V$, | $V_{IH} = 4.5 V,$ | $V_{OH} = 2 V$ | - 100 | - 250 | mA |
| ЮН | High-level output current | $T_A = 25 ^{\circ}C$ | See Note 3 | | - 100 | - 250 | |
| lOL | Low-level output current | $V_{IL} = 0.8 V,$ | $V_{OL} = 0.4 V$, | See Note 3 | | -800 | μΑ |
| lO(off) | Off-state output current | $V_{CC} = 3 V$, | $V_0 = 3 V$ | | | 500 | μΑ |
| lн | High-level input current | $V_1 = 4.5 \text{ V}$ | | | | 40 | μΑ |
| IL | Low-level input current | V _I = 0.4 V | | | -0.1 | - 1.6 | mA |
| los | Short-circuit output current [†] | V _{CC} = 5 V, | T _A = 25 °C | | | - 30 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = 5.25 V$, | All inputs at 2 V, | Outputs open | - | 28 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 V_{r}$ | All inputs at 0.8 V, | Outputs open | | 60 | mA |

[†]Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------------------------|-----|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level output | $R_L = 37 \Omega$, $C_L = 15 pF$, | | 11 | 20 | |
| tpHL Propagation delay time, high-to-low-level output | See Figure 1 | | 8 | 20 | ns |
| tPLH Propagation delay time, low-to-high-level output | $R_L = 37 \Omega$, $C_L = 1000 pF$, | | 22 | 50 | |
| tPHL Propagation delay time, high-to-low-level output | See Figure 1 | | 20 | 50 | ns |

PARAMETER MEASUREMENT INFORMATION

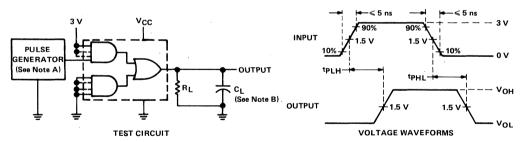
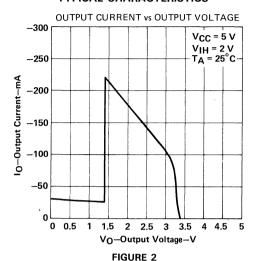


FIGURE 1. SWITCHING TIMES

NOTES: A. The pulse generators have the following characteristics: $Z_0 \approx 50 \ \Omega$, $t_W = 200 \ ns$, duty cycle $\leq 50\%$, PRR $\leq 500 \ kHz$. B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS



.....

APPLICATION INFORMATION

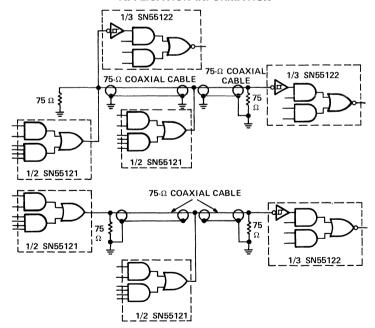


FIGURE 3. SINGLE-ENDED PARTY LINE CIRCUITS



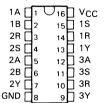
D1334, SEPTEMBER 1973-REVISED SEPTEMBER 1986

- Designed for Digital Data Transmission Over Coaxial Cable, Strip Line, or Twisted Pair
- Designed for Operation With 50- Ω to 500- Ω Transmission Lines
- TTL Compatible
- Single 5-V Supply
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation
 Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Fanout to 10 Series 54/74 Standard Loads
- Can Be Used With Dual Line-Drivers SN55121 and SN75121
- Interchangeable With Signetics N8T14

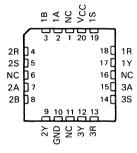
description

The SN55122 and SN75122 are triple line-receivers that are designed for digital data transmission over lines having impedances from 50 to 500 Ω . They are also compatible with standard TTL-logic and supply voltage levels.

SN55122 . . . J PACKAGE SN75122 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55122 . . . FK PACKAGE (TOP VIEW)



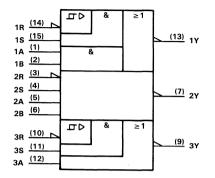
NC-No internal connection

The SN55122 and SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level voltage. The receiver can withstand a level of -0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

The SN55122 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The SN75122 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

SN55122, SN75122 TRIPLE LINE-RECEIVERS

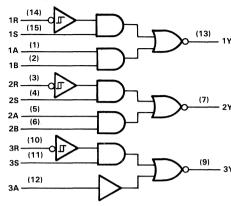
logic symbol[†]



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram



FUNCTION TABLE

| | INPL | | OUTPUT | |
|---|------|---|--------|---|
| Α | В‡ | R | S | Y |
| Н | Н | Х | Χ | L |
| Х | Х | L | Н | L |
| L | Х | Н | Х | н |
| L | Χ | X | L | н |
| x | L | Н | Х | н |
| Х | L | X | L | н |

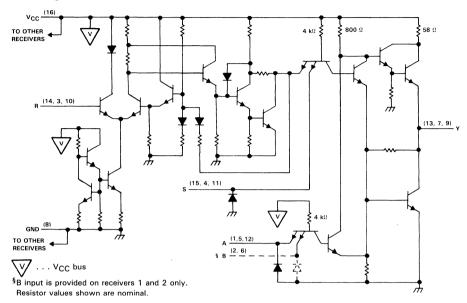
[‡]B input and last two lines of the function table are applicable to receivers 1 and 2 only.

H = high level

L = low level

X = irrelevant

schematic diagram (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage: R input |
| A, B, or S input |
| Output voltage |
| Output current |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range: SN55122 |
| SN75122 |
| Storage temperature range65°C to 150°C |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. In the FK and J packages, SN55122 chips are alloy mounted and in the J package, SN75122 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55122) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75122) | 1025 mW | 8.2 mW/°C | 656 mW | _ |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |



SN55122, SN75122 TRIPLE LINE-RECEIVERS

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|---------------|------|------|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | A, B, R, or S | 2 | | | V |
| Low-level input voltage, VIL | A, B, R, or S | | | 0.8 | V |
| High-level output current, IOH | | | -500 | | μΑ |
| Low-level output current, IOL | | | | 16 | mA |
| Operating free-air temperature, TA | SN55122 | - 55 | | 125 | °C |
| | SN75122 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature, VCC = 4.75 V to 5.25 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | S MI | N TYP [†] | MAX | UNIT | | |
|------------------------------|------------------------------|-----------------|---|------------------------------|-------|-------|-----|--|
| V _{hys} ‡ | Hysteresis | R | $V_{CC} = 5 \text{ V}, T_{A} = 25 ^{\circ}\text{C}$ | 0. | 3 0.6 | | V | |
| VIK | Input clamp voltage | A,B, or S | $V_{CC} = 5 \text{ V}, I_{I} = -12 \text{ mA}$ | | | -1.5 | ٧ | |
| V _{I(BR)} | Input breakdown voltage | A,B, or S | $V_{CC} = 5 \text{ V}, I_{I} = 10 \text{ mA}$ | 5. | 5 | | ٧ | |
| | | | $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, I_{O} | $_{\rm H} = -500 \ \mu A$ 2. | 6 | | | |
| | High-level output voltage | | $V_{I(A)} = 0, \qquad V_{I(B)} = 0, \qquad V_{I}$ | (S) = 2 V, | | | V | |
| ∨он | riigii-level output voltage | | $V_{I(R)} = 1.45 \text{ V (see Note 3),}$ | 2. | 6 | | • | |
| | | | $I_{OH} = -500 \mu A$ | | | | | |
| | | | $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, I_{O} | L = 16 mA | | 0.4 | | |
| VOI Low-level output voltage | | | $V_{I(A)} = 0, V_{I(B)} = 0, V_{I}$ | (S) = 2 V, | | | l v | |
| VOL | Low-level output voltage | | $V_{I(R)} = 1.45 \text{ V (see Note 4)},$ | | | 0.4 | \ | |
| | | | I _{OL} = 16 mA | | | | | |
| l | High-level input current | A,B, or S | V _I = 4.5 V | | | 40 | μΑ | |
| ΙН | riigii-ievei iliput culterit | R | V _I = 3.8 V | | | 170 | μΛ | |
| IJL | Low-level input current | A,B, or S | $V_1 = 0.4 \text{ V}, \qquad V_{1R} = 0.8 \text{ V}$ | -0. | 1 | - 1.6 | mA | |
| los§ | Short-circuit output curren | t | $V_{CC} = 5 \text{ V}, T_A = 25 \text{ °C}$ | -5 | 0 | -100 | mA | |
| Іссн | High-level supply current | | $V_{CC} = 5.25 \text{ V}$, All inputs at 0.8 $^{\circ}$ | V, Outputs open | | 72 | mA | |
| ICCL | Low-level supply current | | $V_{CC} = 5.25 \text{ V}$, All inputs at 2 V, (see Note 5) | Outputs open | | 100 | mA | |

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|------|
| tpLH Propagation delay time, low-to-high-level output from R input | See Figure 1 | | 20 | 30 | ns |
| tpHL Propagation delay time, high-to-low-level output from R input | See Figure 1 | | 20 | 30 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C. ‡ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage,

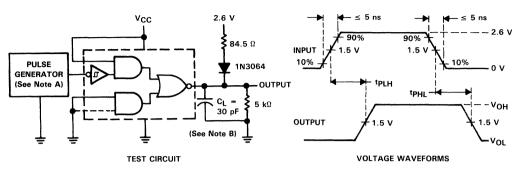
[§]Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTES: 3. The receiver input was high immediately before being reduced to 1.45 V.

^{4.} The receiver input was low immediately before being increased to 1.45 V.

^{5.} For SN55122, $V_{CC} = 5.5 \text{ V}$

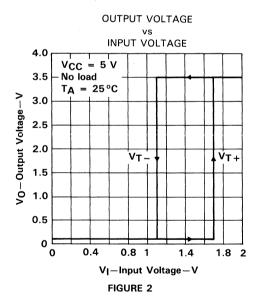
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_0 \approx 50 \ \Omega$, $t_W = 200 \ ns$, duty cycle = 50%, PRR = 500 kHz. B. C_1 includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

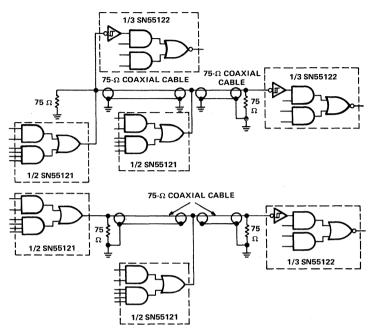
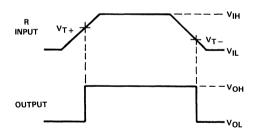


FIGURE 3. SINGLE-ENDED PARTY LINE CIRCUITS



The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring pulses.

FIGURE 4. PULSE SQUARING



D1663. SEPTEMBER 1973-REVISED SEPTEMBER 1986

- Single 5-V Supply
- High-Input-Impedance, High-Threshold Receivers
- Common Driver Strobe
- TTL-Compatible Driver and Strobe Inputs with Clamp Diodes
- High-Speed Operation
- 100-mA Open-Collector Driver Outputs
- Four Independent Channels
- TTL-Compatible Receiver Output

description

The SN55138 and SN75138 quad bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads of up to 100 mA open-collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

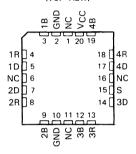
The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN75138 is characterized for operation from 0 °C to 70 °C.

SN55138 . . . J PACKAGE SN75138 . . . D, J, OR N PACKAGE (TOP VIEW)

> GND [1 ¹16∏∨cc 18 □ 15 14B 1RC 3 14 74R 1D [13 🗌 4D 4 2D 🗀 12 S 2R ∏ 6 11 3D 10 3R 2B [GND [9∏3B

SN55138 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE (TRANSMITTING)

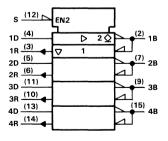
FUNCTION TABLE (RECEIVING)

| INPUTS | | OUT | PUTS |
|--------|---|-----|------|
| S | D | В | R |
| L | Н | L | Н |
| L | L | Н | L |

| INPUTS | OUTPUT |
|--------|--------|
| SBD | R |
| ннх | L |
| HLX | Н |

H = high level, L = low level, X = irrelevant

logic symbol†



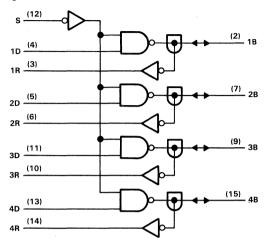
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.



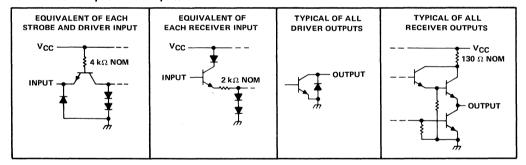
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logic diagram (positive logic)



Pin numbers showns are for D, J, and N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55138 | SN75138 | UNIT |
|--|-------------|---------------------|------|
| Supply voltage, VCC (see Note 1) | 7 | 7 | V |
| Input voltage | 5.5 | 5.5 | ٧ |
| Driver off-state output voltage | 7 | 7 | ٧ |
| Low-level output current into the driver output | 150 | 150 | mA |
| Continuous total power dissipation (see Note 2) | See Dissi | pation Rating Table |) |
| Operating free-air temperature range | - 55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | 300 | °C |

NOTES: 1. All voltage values are with respect to both ground terminals connected together.

2. In the FK and J packages, SN55138 chips are alloy mounted and SN75138 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55138) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75138) | 1025 mW | 8.2 mW/°C | 656 mW | - |
| N | 1150 mW | 9.2 mW/°C | 736 mW | |

recommended operating conditions

| | | SN55138 | | SN75138 | | | UNIT | | |
|---|------------------|---------|-----|---------|------|-----|------|------|--|
| | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT | |
| Supply voltage, V _{CC} | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | |
| High-level input voltage, V _{IH} | Driver or strobe | 2 | | | 2 | | | V | |
| | Receiver | 3.2 | | | 2.9 | | | | |
| I built a la V | Driver or strobe | | | 0.8 | | | 0.8 | v | |
| Low-level input voltage, V _{IL} | Receiver | | | 1.5 | | | 1.8 | | |
| High-level output current, IOH | Receiver output | | | -400 | | | -400 | μΑ | |
| | Driver output | | | 100 | | | 100 | T . | |
| Low-level output current, IOL | Receiver output | | | 16 | | | 16 | mA | |
| Operating free-air temperature, TA | | -55 | | 125 | 0 | | 70 | °C | |

SN55138, SN75138 **QUADRUPLE BUS TRANSCEIVERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN55138 | | | SN75138 | | | UNIT | |
|-----------------|--|-------------------------|---|--|-----|------|---------|-----|------------------|------|------|
| | I ANAMETER | | TEST CON | IDITIONS · | MIN | TYP‡ | MAX | MIN | TYP [‡] | MAX | UNIT |
| VIK | Input clamp voltage | Driver or strobe | V _{CC} = MIN, | I ₁ = -12 mA | | | -1.5 | | | -1.5 | > |
| V _{OH} | High-level output voltage | Receiver | $V_{CC} = MIN,$ $V_{IL(R)} = V_{IL} max,$ | ,-, | 2.4 | 3.5 | | 2.4 | 3.5 | | ٧ |
| VOL | Low-level | Driver | V_{CC} MIN, $V_{IL(S)} = 0.8 \text{ V},$ | $V_{IH(D)} = 2 V$, $I_{OL} = 100 \text{ mA}$ | | | 0.45 | | | 0.45 | v |
| VOL | output voltage | Receiver | $V_{CC} = MIN,$ $V_{IH(S)} = 2 V,$ | $V_{IH(R)} = V_{IH} min,$ $I_{OL} = 16 mA$ | | | 0.4 | | | 0.4 | • |
| lį | Input current at maximum input voltage | Driver or strobe | V _{CC} = MAX, | V _I = V _{CC} | | | 1 | | | 1 | mA |
| | High-level input current | Driver or strobe | $V_{CC} = MAX,$ | V _I = 2.4 V | | | 40 | | | 40 | |
| чн | | Receiver | $V_{CC} = 5 V$, $V_{I(S)} = 2 V$ | $V_{I(R)} = 4.5 V,$ | | 25 | 300 | | 25 | 300 | μΑ |
| | Low-level | Driver or strobe | $V_{CC} = MAX,$ | V _I = 0.4 V | | -1 | -1.6 | | -1 | -1.6 | mA |
| կլ | input current | Receiver | $V_{CC} = MAX,$ $V_{I(S)} = 2 V$ | $V_{I(R)} = 0.45 \text{ V},$ | | | - 50 | | | - 50 | μΑ |
| | Input current with power off | Receiver | V _{CC} = 0, | V _I = 4.5 V | | 1.1 | 1.5 | | 1.1 | 1.5 | mA |
| los | Short-circuit output current§ | Receiver | V _{CC} = MAX | | -20 | | - 55 | -18 | | - 55 | mA |
| | | All driver outputs low | $V_{CC} = MAX,$ $V_{I(S)} = 0.8 V$ | $V_{I(D)} = 2 V,$ | | 50 | 65 | | 50 | 65 | |
| lcc | Supply current | All driver outputs high | V _{CC} = MAX, V _{I(S)} = 2 V, Receiver outputs of | | | 42 | 55 | | 42 | 55 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | ТҮР | MAX | UNIT |
|-----------|-----------------|----------------|---|-----|-----|-----|------|
| tPLH | Driver | Driver | | | 15 | 24 | |
| tPHL | Driver | Driver | $C_L = 50 \text{ pF}, R_L = 50 \Omega,$ | | 14 | 24 | ns |
| tPLH | Caraba | Driver | See Figure 1 | | 18 | 28 | |
| tPHL | Strobe | trobe Driver | | | 22 | 32 | ns |
| tPLH | Receiver | Daneiue. | $C_L = 15 \text{ pF}, R_L = 400 \Omega,$ | | 7 | 15 | |
| tPHL | neceiver | Receiver | See Figure 2 | | 8 | 15 | ns |

[†]tpLH ≡ propagation delay time, low-to-high-level output

 $^{^{\}ddagger}All$ typical values are at V_{CC} = 5 V, T_A = 25 °C. $^{\$}Not$ more than one output should be shorted at a time.

tpHL ≡ propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION

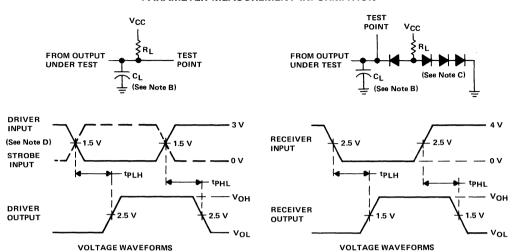
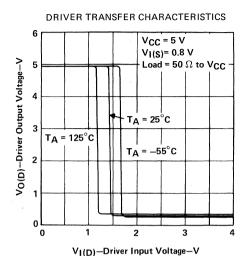


FIGURE 1. PROPAGATION DELAY TIMES FROM DATA AND STROBE INPUTS

FIGURE 2. PROPAGATION DELAY TIMES
FROM RECEIVER INPUT

- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_W = 100$ ns, PRR ≤ 1 MHz, $t_f \leq 10$ ns, $t_f \leq 10$ ns, $t_0 \approx 50 \ \Omega$.
 - B. CL includes probe and jig capacitance.
 - C. All diodes are 1N916 or 1N3064.
 - D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL CHARACTERISTICS†



2.....

FIGURE 3

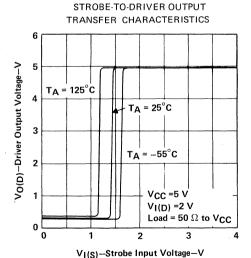
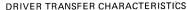
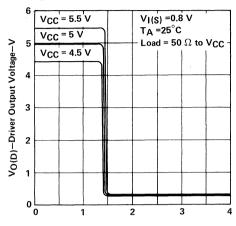


FIGURE 5

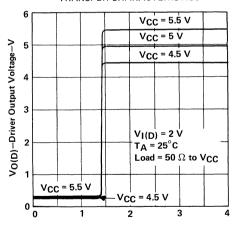




V_{I(D)}-Driver Input Voltage-V

FIGURE 4

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

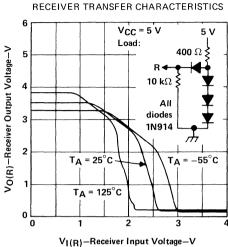


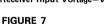
V_{I(S)}—Strobe Input Voltage—V

FIGURE 6

[†]Data for temperatures below 0 °C and above 70 °C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†





HIGH-LEVEL OUTPUT VOLTAGE

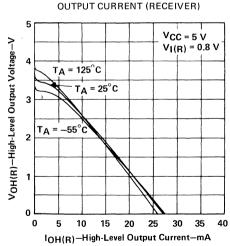


FIGURE 9

RECEIVER TRANSFER CHARACTERISTICS

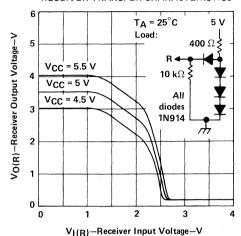


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE



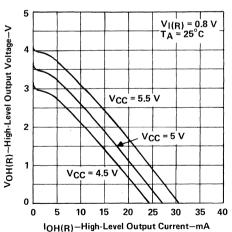


FIGURE 10

[†]Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.



TYPICAL CHARACTERISTICS[†]

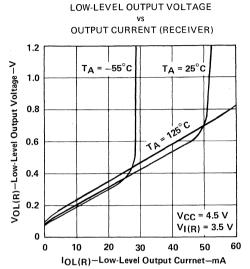


FIGURE 11

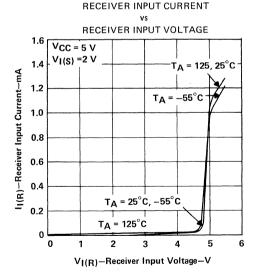


FIGURE 13

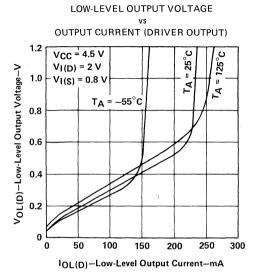
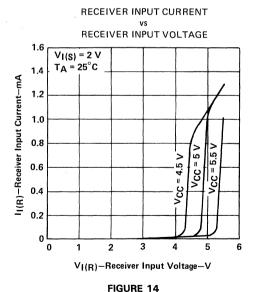


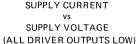
FIGURE 12

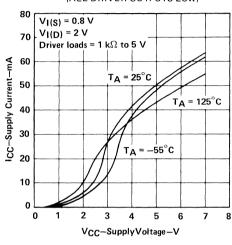


†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.



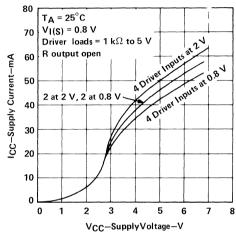
TYPICAL CHARACTERISTICS[†]





SUPPLY VOLTAGE T_A = 25°C

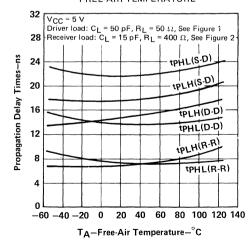
SUPPLY CURRENT



PROPAGATION DELAY TIMES

FIGURE 15

FREE-AIR TEMPERATURE



PROPAGATION DELAY TIMES

FIGURE 16

SUPPLY VOLTAGE

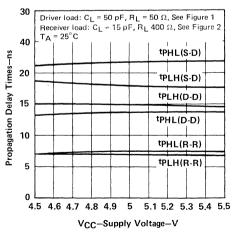


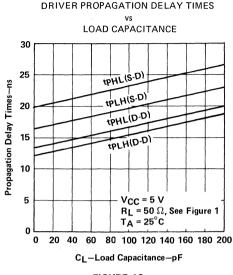
FIGURE 17

FIGURE 18

[†]Data for temperatures below 0 °C and above 70 °C is applicable to SN55138 circuits only.



TYPICAL CHARACTERISTICS



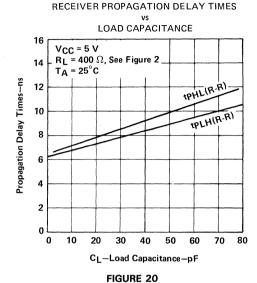


FIGURE 19

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APPLICATION INFORMATION

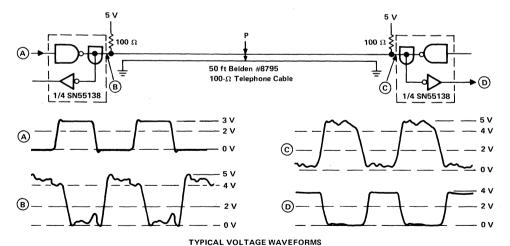


FIGURE 21. POINT-TO-POINT COMMUNICATION OVER 50 FEET OF TWISTED PAIR AT 5 MHz

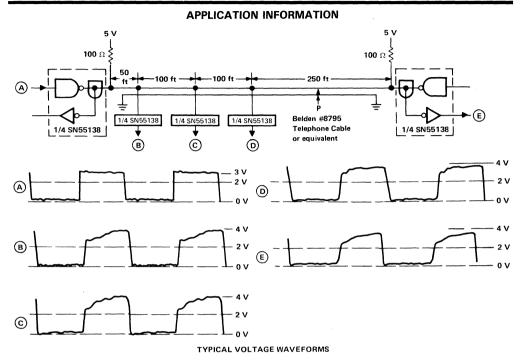


FIGURE 22. PARTY-LINE COMMUNICATION ON 500 FEET OF TWISTED PAIR AT 1 MHz

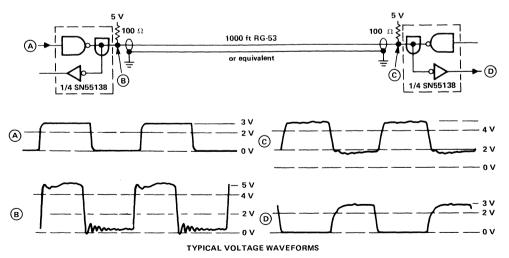


FIGURE 23. POINT-TO-POINT COMMUNICATION OVER 1000 FEET OF COAX AT 1 MHz



SN55157, SN75157 DUAL DIFFERENTIAL LINE RECEIVER

D2300, SEPTEMBER 1980-REVISED SEPTEMBER 1986

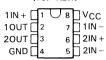
- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package
- Similar to uA9637AC except for Corner VCC and Ground Pin Positions

description

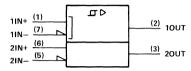
The SN75157 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and small outline package.

The SN55157 is characterized over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}.$ The SN75157 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}.$

SN55157 . . . JG PACKAGE SN75157 . . . D, JG, OR P PACKAGE (TOP VIEW)

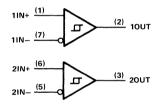


logic symbol†

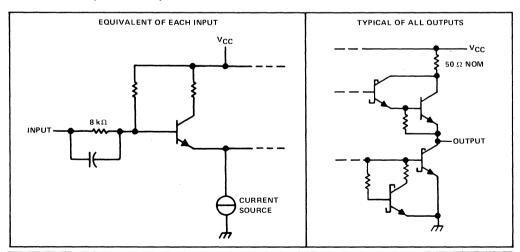


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1)0.5 V to 7 V |
|---|
| Input voltage |
| Differential input voltage (see Note 2) ±15 V |
| Output voltage (see Note 1) |
| Low-level output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| SN55157 JG package |
| SN75157 D package |
| JG package |
| P package |
| Operating free-air temperature range: SN55157 |
| SN75157 0°C to 70°C |
| Storage temperature range65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds JG package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds D or P package 260 °C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

3. For operation above 25 °C free-air temperature, derate the SN55157 JG package to 672 mW at 70 °C at the rate of 8.4 mW/ °C, the SN75157 JG package to 528 mW at 70 °C at the rate of 6.6 mW/°C, the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70 °C at the rate of 8.0 mW/°C. In the JG package, SN55157 chips are alloy mounted and SN75157 chips are glass mounted.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---------|------|-----|------|------|
| Supply voltage, VCC | | | | 5.25 | ٧ |
| Common-mode input voltage, V _{IC} | | | | ± 7 | ٧ |
| Operating free-air temperature, Τ _Δ | SN55157 | - 55 | 25 | 125 | °C |
| Operating mee-an temperature, 1A | SN75157 | 0 | 25 | 70 | ا ا |

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | TYP [†] ee Note | | UNIT |
|------------------|--|---|-------------------------|------|-----------------------------|-------|------|
| VT | Threshold voltage (V _{T+} and V _{T-}) | | | -0.2 | | 0.2 | v |
| VΤ | Threshold voltage (vT+ and vT-) | See Note 5 | | -0.4 | | 0.4 | \ \ |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | | | | 70 | | mV |
| Vон | High-level output voltage | $V_{ID} = 0.2 V,$ | $I_0 = -1 \text{ mA}$ | 2.5 | 3.5 | | ٧ |
| VOL | Low-level output voltage | $V_{ID} = -0.2 V$, | I _O = 20 mA | | 0.35 | 0.5 | ٧ |
| | Input current | $V_{CC} = 0 \text{ to } 5.5 \text{ V},$ | V _I = 10 V | | 1.1 | 3.25 | mA |
| l) | input current | See Note 6 | V _I = -10 V | | -1.6 | -3.25 | IIIA |
| los | Short-circuit output current [‡] | V _O = 0, | V _{ID} = 0.2 V | -40 | - 75 | - 100 | mA |
| Icc | Supply current | $V_{ID} = -0.5 V$, | No load | | 35 | 50 | mA |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

^{6.} The input not under test is grounded.



[‡]Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

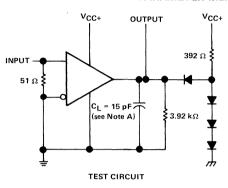
NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

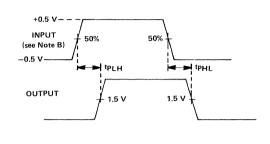
^{5.} The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------|--|--------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | C ₁ = 15 pF. See Figure 1 | | 15 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 1 | | 13 | 25 | ns |

PARAMETER MEASUREMENT INFORMATION





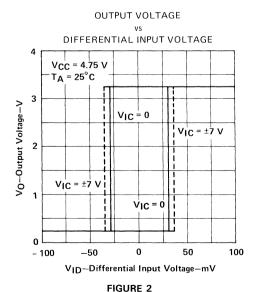
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS



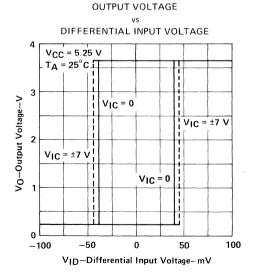
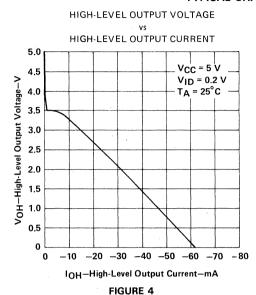
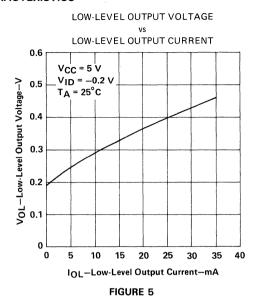
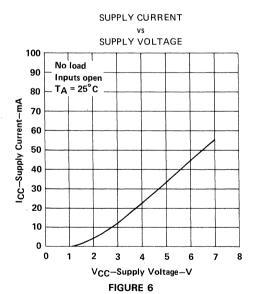


FIGURE 3

TYPICAL CHARACTERISTICS







TYPICAL APPLICATION DATA

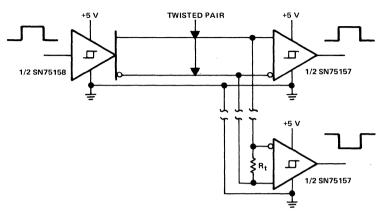


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

SN55158, SN75158 DUAL DIFFERENTIAL LINE DRIVERS

D2292, JANUARY 1977-REVISED SEPTEMBER 1986

Meets EIA Standard RS-422-A

• Single 5-V Supply

Balanced-Line Operation

TTL-Compatible

 High Output Impedance in Power-Off Condition

High-Current Active-Pullup Outputs

Short-Circuit Protection

Dual Channels

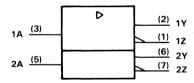
• Input Clamp Diodes

description

The SN55158 and SN75158 are dual complementary-output line drivers designed to satisfy the requirements set by the EIA Standard RS-422-A interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

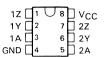
The SN55158 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN75158 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

logic symbol†

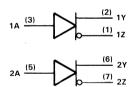


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN55158 . . . JG PACKAGE SN75158 . . . D, JG, OR P PACKAGE (TOP VIEW)

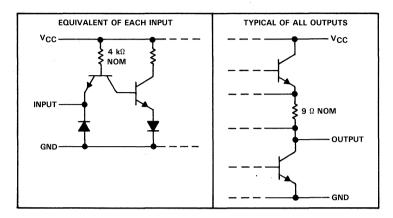


logic diagram (positive logic)



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|---|
| Input voltage |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range: SN55158 |
| SN75158 |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C |

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

2. In the JG package, SN55158 chips are alloy mounted and SN75158 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | TA = 70°C | T _A = 125°C |
|--------------|-----------------------|-----------------|--------------|------------------------|
| PACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 725 mW | 5.8 mW/°C | 464 mW | N/A |
| JG (SN55158) | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| JG (SN75158) | 825 mW | 6.6 mW/°C | 528 mW | N/A |
| Р | 1000 mW | 8.0 mW/°C | 640 mW | N/A |

recommended operating conditions

| | | SN55158 | | 5 | UNIT | | | |
|--|------|---------|-----|------|------|------|------|--|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNII | |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | ٧ | |
| High-level input voltage, VIH | 2 | | | 2 | | | ٧ | |
| Low-level input voltage, V _{IL} | | | 0.8 | | | 0.8 | V | |
| High-level output current, IOH | | | -40 | | | - 40 | mA | |
| Low-level output current, IOL | | | 40 | | | 40 | mA | |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C | |



electrical characteristics over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEC | T CONDI | NDITIONS† | | SN5515 | 58 | | SN7515 | 8 | UNIT |
|-------------------|--|---|----------------------|-------------------------|-----|------------------|-------------------|-----|------------------|-------------------|------|
| | PARAMETER | | TEST CONDITIONS† | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNII |
| VIK | Input clamp voltage | V _{CC} = MI | N, I _I = | – 12 mA | | -0.9 | -1.5 | | -0.9 | -1.5 | V |
| Vон | High-level output voltage | V _{CC} = MI V _{IH} = 2 V | | = 0.8 V, = -40 mA | 2 | 3.0 | | 2.4 | 3.0 | | V |
| V _{OL} | Low-level output voltage | $V_{CC} = MI$ $V_{IH} \approx 2 V$ | | = 0.8 V, = 40 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| VOD1 | Differential output voltage | V _{CC} = MA | XX, I _O = | = O | | 3.5 | 2V _{OD2} | | 3.5 | 2V _{OD2} | V |
| VOD2 | Differential output voltage | V _{CC} = MI | N | | 2 | 3.0 | | 2 | 3.0 | | V |
| Δ V _{OD} | Change in magnitude of differential output voltage § | V _{CC} = MI | N | $R_L = 100 \Omega$ | | ±0.02 | ±0.4 | | ± 0.02 | ±0.4 | V |
| Voc | Common-mode output voltage¶ | $V_{CC} = MA$ $V_{CC} = MI$ | | See Figure 1 | | 1.9 | 3 | | 1.8 1.5 | 3 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage § | V _{CC} = MI | • | | | ±0.01 | ±0.4 | | ±0.01 | ±0.4 | V |
| | | | $V_0 = 6$ | | | 0.1 | 100 | | 0.1 | 100 | |
| I _O | Output current with power off | $V_{CC} = 0$ | | | | -0.1 | - 100 | | -0.1 | - 100 | μΑ |
| | | | V ₀ = - | 0.25 to 6 V | | | ± 100 | | | ± 100 | |
| 11 | Input current at maximum input voltage | V _{CC} = MA | λX, V _j = | 5.5 V | | | 1 | | | 1 | mA |
| Iн | High-level input current | V _{CC} = MAX, V _I = 2.4 V | | | | 40 | | | 40 | μΑ | |
| I _I L | Low-level input current | V _{CC} = MAX, V _I = 0.4 V | | | - 1 | -1.6 | | - 1 | -1.6 | mA | |
| los | Short-circuit output current# | V _{CC} = MA | XX | | -40 | -90 | - 150 | -40 | - 90 | - 150 | mA |
| Icc | Supply current (both drivers) | V _{CC} = MA No load, | | ts grounded, = 25 °C | | 37 | 50 | | 37 | 50 | mA |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST | | N5515 | 8 | S | N75158 | 3 | UNIT |
|------------------|--|---------------|-----|-------|-----|----------|--------|-----|------|
| | PARAIVIETEN | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| tPLH | Propagation delay time, low-to-high-level output | See Figure 2, | | 16 | 25 | | 16 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Termination A | | 10 | 20 | | 10 | 20 | ns |
| tPLH | Propagation delay time, low-to-high-level output | See Figure 2, | | 13 | 20 | | 13 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Termination B | | 9 | 15 | | 9 | 15 | ns |
| ^t TLH | Transition time, low-to-high-level output | See Figure 2, | | 4 | 20 | | 4 | 20 | ns |
| tTHL | Transition time, high-to-low-level output | Termination A | | 4 | 20 | | 4 | 20 | ns |
| | Overshoot feater | See Figure 2, | | | 10 | | | 10 | % |
| | Overshoot factor | Termination C | | | 10 | <u> </u> | | 10 | 70 |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C except for V_{OC}, for which V_{CC} is as stated under test conditions.

 $^{^{\}S}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

[🖣] In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

[#]Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

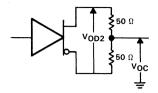
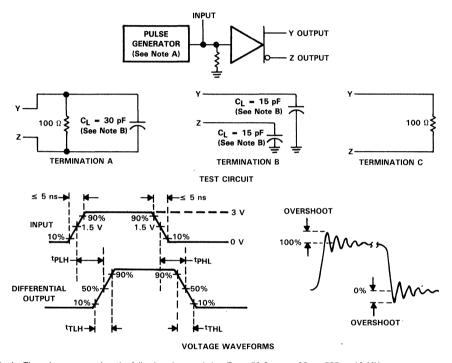
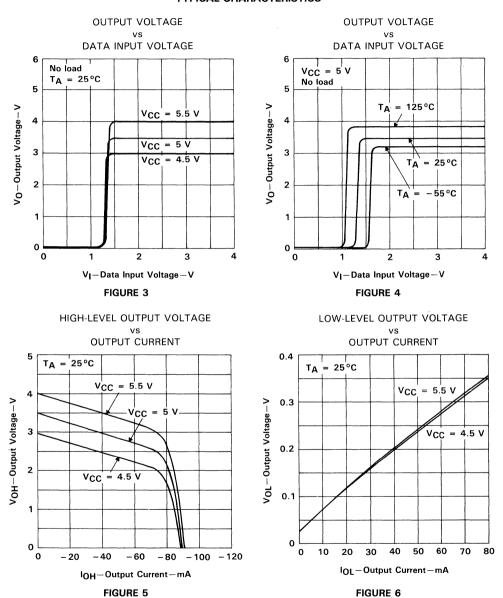


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



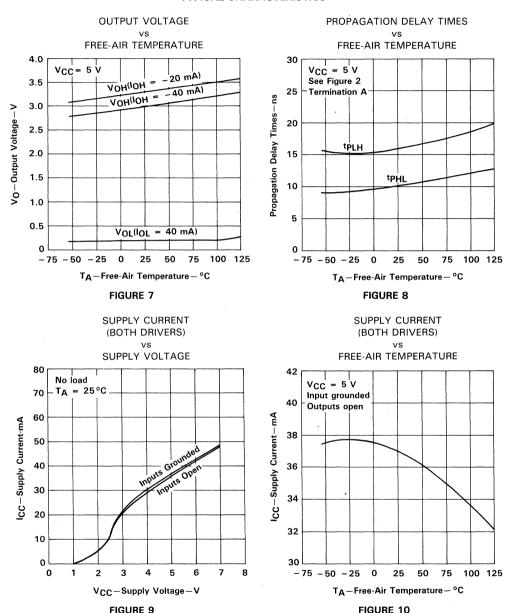
NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \ \Omega$, $t_W = 25 \ ns$, PRR $\leq 10 \ MHz$. B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES



[†]Data for temperatures below 0 °C and above 70 °C are applicable to SN55158 circuits only.





[†]Data for temperatures below 0 °C and above 70 °C are applicable to SN55158 circuits only.



TYPICAL CHARACTERISTICS

SUPPLY CURRENT (BOTH DRIVERS)

vs FREQUENCY

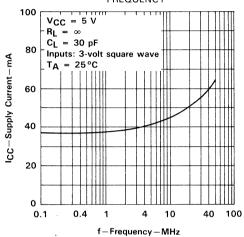


FIGURE 11

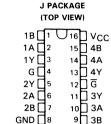
D3167, DECEMBER 1988

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . − 12 to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for AM26LS32

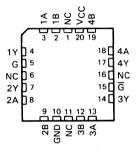
description

The SN55173 is a monolithic quadruple differential line receiver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers have an ORed pair of enables in common. Either G being high or G being low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of -12 to 12 V. The SN55173 is designed for optimum performance when used with the SN55172 or SN55174 quadruple differential line drivers.

The SN55173 is characterized for operation from -55 °C to 125 °C.

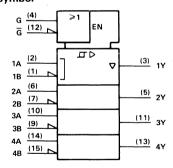


FK PACKAGE (TOP VIEW)



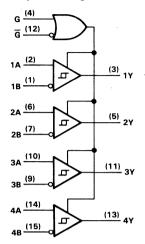
NC-No internal connection

logic symbol





logic diagram (positive logic)



FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENA | BLES | OUTPUT |
|----------------------------------|-----|------|--------|
| A-B | G | G | Υ |
| V- > 0.2 V | H | Х | Н |
| V _{ID} ≥ 0.2 V | × | L | Н |
| -0.2 V < V _{ID} < 0.2 V | Н | Х | ? |
| -0.2 V < VID < 0.2 V | × | L | ? |
| V 02V | Н | Х | L |
| V _{ID} ≤ -0.2 V | X | L | L |
| X | L | Н | Z |

H = high level

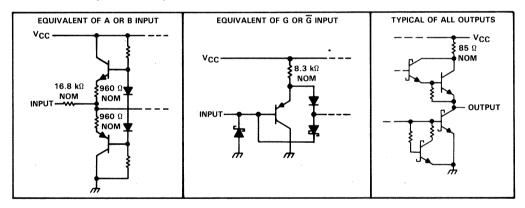
L = low level

X = irrelevant

? = indeterminate

Z = high-impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | ٧ |
|---|----|
| Input voltage, A or B inputs | ٧ |
| Differential input voltage (see Note 2) | ٧ |
| Enable input voltage | ٧ |
| Low-level output current | ۱A |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3) 1375 m | W |
| Operating free-air temperature range | °C |
| Storage temperature range | °C |
| Case temperature for 60-seconds: FK package | °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds | °C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

- 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | V |
| Common-mode input voltage, V _{IC} | | | ±12 | V |
| Differential input voltage, V _{ID} | | | ±12 | ٧ |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| High-level output current, IOH | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, T _A | - 55 | | 125 | °C |

SN55173 QUADRUPLE DIFFERENTIAL LINE RECEIVER

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONE | DITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|---|---------------------------|-------------------|------------------|-------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| V_{TL} | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | $I_0 = 16 \text{ mA}$ | -0.2 [‡] | | | > |
| V _{hys} | Hysteresis § | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | - 1.5 | ٧ |
| Voн | High-level output voltage | V _{ID} = 200 mV, | $I_{OH} = -400 \mu A$ | 2.5 | | | ٧ |
| V | Low level output voltage | ., | I _{OL} = 8 mA | | | 0.45 | V |
| VOL | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ | I _{OL} = 16 mA · | | | 0.5 | · • |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | | | | ± 20 | μΑ |
| 1. | Line input current | Other input at 0 V, | V _I = 12 V | | | 1 | mA |
| lı . | Line input current | See Note 4 | $V_I = -7 V$ | | | -0.8 | IIIA |
| ΙН | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| . I _{IL} | Low-level enable-input current | V _{IL} = 0.4 V | | | | -100 | μΑ |
| los | Short-circuit output current¶ | | | -15 | | -85 | mA |
| Icc | Supply current | Outputs disabled | | | | 70 | mA |

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|------|--|------------------------------|--------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V to}$ | 1.5 V, C _L = 15 pF, | | 20 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 1 | | | 22 | 35 | ns |
| tPZH | Output enable time to high level | C _L = 15 pF, | See Figure 2 | | 17 | 22 | ns |
| tPZL | Output enable time to low level | CL = 15 pF, | See Figure 3 | | 20 | 25 | ns |
| tPHZ | Output disable time from high level | C _L = 5 pF, | See Figure 2 | | 21 | 30 | ns |
| tPLZ | Output disable time from low level | C _L = 5 pF, | See Figure 3 | | 30 | 40 | ns |

[‡]The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} . See Figure 4.

Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

NOTE 4: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

PARAMETER MEASUREMENT INFORMATION

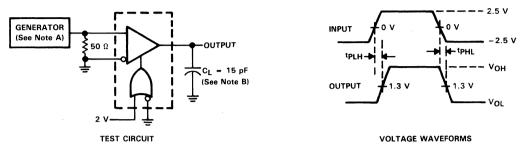


FIGURE 1. tPLH, tPHL

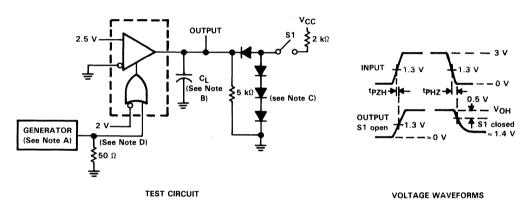


FIGURE 2. tpHZ, tpZH

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \le 6 \text{ ns}, t_f \le 6 \text{ ns}, Z_{out} = 50 \Omega.$
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N916 or equivalent.
 - D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

PARAMETER MEASUREMENT INFORMATION

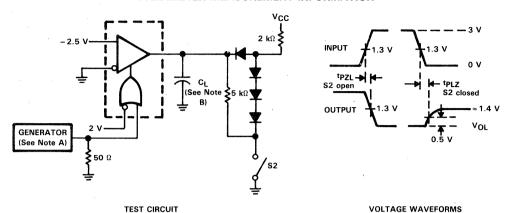
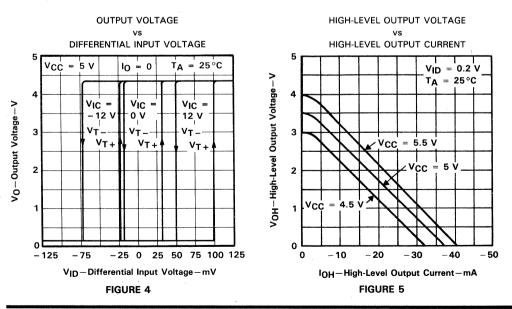


FIGURE 3. tpzl, tpLZ

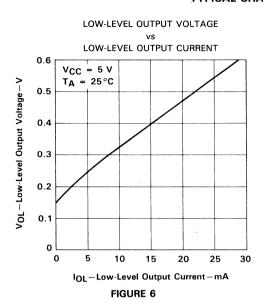
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{OUT} =$ 50 Ω .

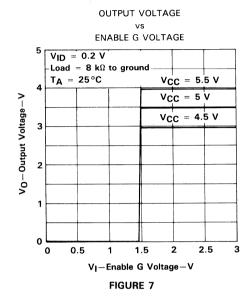
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

TYPICAL CHARACTERISTICS



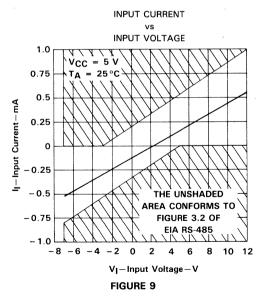
TYPICAL CHARACTERISTICS





OUTPUT VOLTAGE vs ENABLE G VOLTAGE 6 $V_{CC} = 5.5 V$ -0.2 V $V_{CC} = 5 V$ Load = $1 k\Omega$ to VCC 5 $V_{CC} = 4.5 V$ TA = 25°C Vo-Output Voltage-V 1 0 0 0.5 1.5 2 2.5 3 V_I-Enable G Voltage-V

FIGURE 8



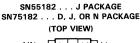
SN55182, SN75182 **DUAL DIFFERENTIAL LINE RECEIVERS**

D1292, OCTOBER 1972-REVISED SEPTEMBER 1986

- Single 5-V Supply
- **Differential Line Operation**
- **Dual Channels**
- TTL Compatibility
- ±15 V Common-Mode Input Voltage Range
- ± 15 V Differential Input Voltage Range
- Individual Channel Strobes
- **Built-In Optional Line-Termination Resistor**
- Individual Frequency Response Controls
- Designed for Use With Dual Differential **Drivers SN55183 and SN75183**
- Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A

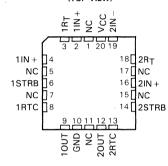
description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to





SN55182 . . . FK PACKAGE (TOP VIEW)



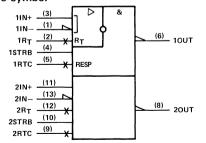
NC-No internal connection

provide immunity to differential noise spikes. The output goes to a high level when the inputs are opencircuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN75182 is characterized for operation from 0°C to 70°C.

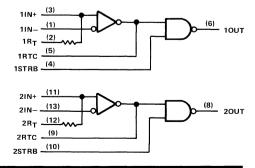
logic symbol †



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J and N packages.

logic diagram (positive logic)



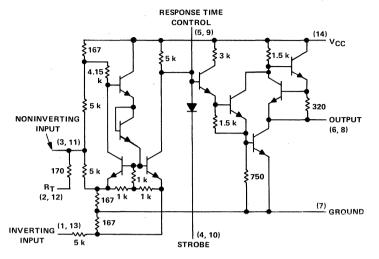
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SN55182, SN75182 DUAL DIFFERENTIAL LINE RECEIVERS

schematic (each receiver)



FUNCTION TABLE

| STROBE | DIFF INPUT | ОИТРИТ |
|--------|---------------|--------|
| L | Х | Н |
| н | Н | н |
| н | L | L |

- H = V_I ≥ V_{IH} min or V_{ID} more positive than V_{TH} max
- L = V_I ≤ V_{IL} max or V_{ID} more negative than V_{TL} max
- X = irrelevant

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55182 | SN75182 | UNIT |
|--|----------------------------|------------|------|
| Supply voltage, V _{CC1} (see Note 1) | 8 | 8 | ٧ |
| Common-mode input voltage | ± 20 | ± 20 | V |
| Differential input voltage (see Note 2) | ± 20 | ± 20 | . 🗸 |
| Strobe input voltage | 8 | 8 | ٧ |
| Output sink current | 50 | 50 | mA |
| Continuous total power dissipation (see Note 3) | See Dissipation Rating Tab | | |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | 300 | °C |

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
 - 2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
 - 3. In the FK and J packages, SN55182 chips are alloy mounted and SN75182 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|--------------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55182) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| 'J (SN75182) | 1025 mW | 8.2 mW/°C | 656 mW | - |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN55182 SN75182 | | | 2 | LIBUT | |
|--|------|-----------------|------|-----|-----|-------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| Common-mode input voltage, V _{IC} | | | ±15 | | | ±15 | V |
| High-level strobe input voltage, VIH(strobe) | 2.1 | | 5.5 | 2.1 | | 5.5 | V |
| Low-level strobe input voltage, VIL(strobe) | 0 | | 0.9 | 0 | | 0.9 | V |
| High-level output current, IOH | | | -400 | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | | | 16 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended ranges of VCC, VIC, and operating free-air temperature (unless otherwise noted)

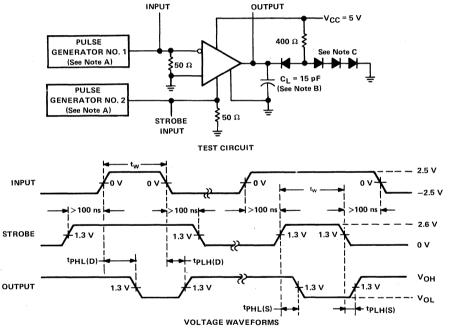
| | PARAMETER | | TEST CO | NDITIONS† | MIN | TYP [‡] | MAX | UNIT |
|-----------------|--|--|--|---|------|------------------|------------|------------|
| V | Differential innut bish th | unabald valtage | $V_{O} = 2.5 V,$ | $V_{IC} = -3 \text{ V to } 3 \text{ V}$ | | | 0.5 | V |
| Vтн | TH Differential input high-threshold voltage | | $I_{OH} = -400 \mu A$ | $V_{IC} = -15 \text{ V to } 15 \text{ V}$ | | | 1 | l ' |
| \/ | Differential input low-th | bold valtage | $V_0 = 0.4 V$, | $V_{IC} = -3 \text{ V to } 3 \text{ V}$ | | | -0.5 | V |
| VTL | Differential input low-th | resnoid voitage | $I_{OL} = 16 \text{ mA}$ | $V_{IC} = -15 \text{ V to } 15 \text{ V}$ | | | – 1 | L <u> </u> |
| | | | $V_{ID} = 1 V$, | $V_{strobe} = 2.1 V,$ | 2.5 | 4.2 | 5.5 | |
| Voн | High-level output voltag | Δ | $I_{OH} = -400 \mu A$ | | 2.0 | 7.2 | | l v |
| VOH | riigii-level output voltag | C | $V_{ID} = -1 V$, | $V_{\text{strobe}} = 0.4 \text{ V},$ | 2.5 | 4.2 | 5.5 | ' |
| | | | $I_{OH} = -400 \mu A$ $V_{ID} = -1 V,$ | | 2.5 | T.Z | | |
| VOL | Low-level output voltage | Low lovel output voltage | | $V_{strobe} = 2.1 V,$ | | 0.25 | 0.4 | l v |
| VOL | | | $I_{OL} = 16 \text{ mA}$ | | | | | |
| İ | Input current | | V _{IC} = 15 V | | | 3 | 4.2 | |
| | | Inverting input out current Noninverting input | $V_{IC} = 0$ | | | 0 | | mA |
| 41 | | | $V_{IC} = -15 V$ | | | -3 | -4.2 | |
| " | | | V _{IC} = 15 V | | | 5 | 7 |] |
| | | | $V_{IC} = 0$ | | | 1 | -1.4 | mA |
| | | | $V_{IC} = -15 \text{ V}$ | | | -7 | -9.8 | |
| ISH | High-level strobe curren | t | $V_{\text{strobe}} = 5.5 \text{ V}$ | | | | 5 | μΑ |
| I _{SL} | Low-level strobe current | İ . | V _{strobe} = 0 | | | - 1 | -1.4 | mA |
| rį | Input resistance | Inverting input | | | 3.6 | 5 | | kΩ |
| | input resistance | Noninverting input | | | 1.8 | 2.5 | | kΩ |
| RT | Line terminating resistance | | $T_A = 25 ^{\circ}C$ | | 120 | 170 | 250 | Ω |
| los | Short-circuit output current | | $V_{CC} = 5.5 V,$ | $V_0 = 0$ | -2.8 | -4.5 | -6.7 | mA |
| | | | $V_{IC} = 15 V$, | $V_{ID} = -1 V$ | | 4.2 | 6 | } |
| Icc | Supply current (average | per receiver) | $V_{IC} = 0,$ | $V_{ID} = -0.5 V$ | | 6.8 | 10.2 | mA |
| | | | $V_{IC} = -15 V$, | $V_{ID} = -1 V$ | | 9.4 | 14 | |

 $^{^{\}dagger}$ Unless otherwise noted, V_{strobe} ≥ 2.1 V or open. ‡ All typical values are at V_CC = 5 V, V_{IC} = 0, and T_A = 25 °C.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|--|-----|-----|-----|------|
| ^t PLH(D) | Propagation delay time, low-to-high-level output from differential input | | | 18 | 40 | ns |
| ^t PHL(D) | Propagation delay time, high-to-low-level output from differential input | R _L = 400 Ω, C _L = 15 pF, See Figure 1 | | 31 | 45 | ns |
| ^t PLH(S) | Propagation delay time, low-to-high-level output from strobe input | | | 9 | 30 | ns |
| ^t PHL(S) | Propagation delay time, high-to-low-level output from strobe input | | | 15 | 25 | ns |

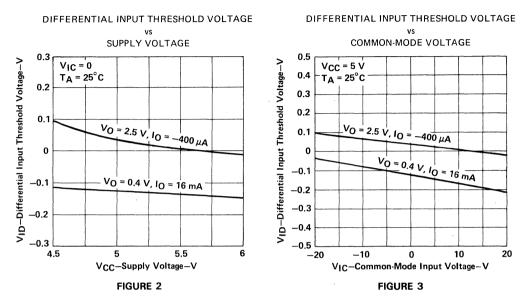
PARAMETER MEASUREMENT INFORMATION



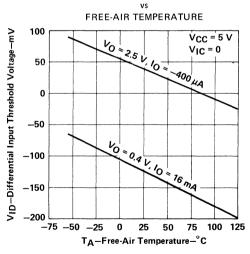
NOTES: A. The pulse generators have the following characteristics: $Z_0 = 50~\Omega$, $t_f \le 10~ns$, $t_f \le 10~ns$, $t_W = 0.5~\pm 0.1~\mu s$, PRR $\le 1~MHz$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

FIGURE 1. PROPAGATION DELAY TIMES

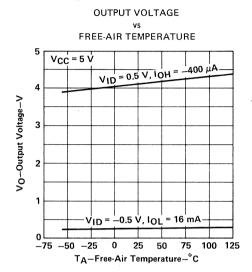


DIFFERENTIAL INPUT THRESHOLD VOLTAGE



[†]Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

FIGURE 4



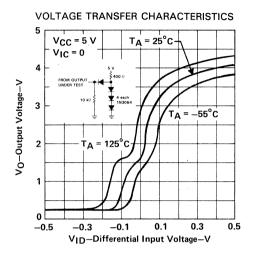


FIGURE 5

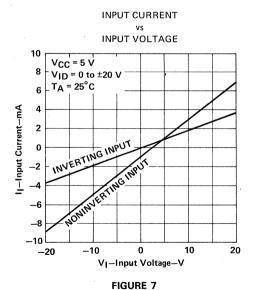
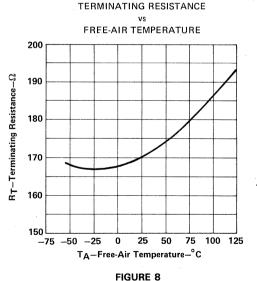
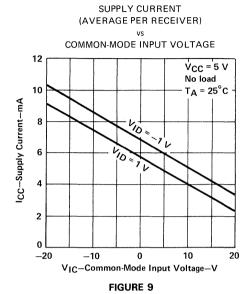


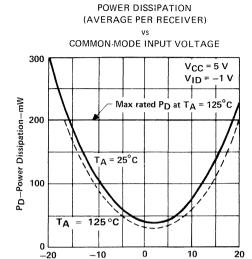
FIGURE 6



[†]Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.



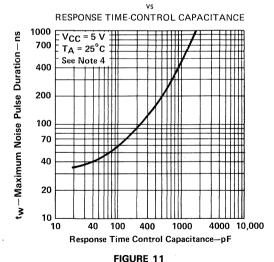


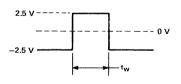


V_{IC}-Common-Mode Input Voltage-V

FIGURE 10

NOISE PULSE DURATION

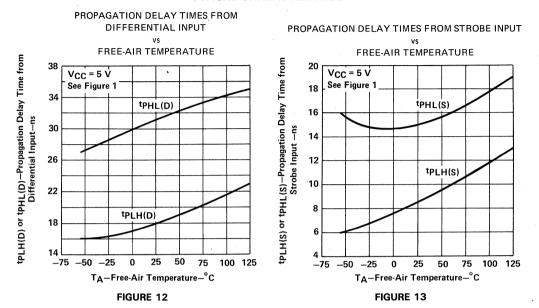




INPUT PULSE FOR FIGURE 11

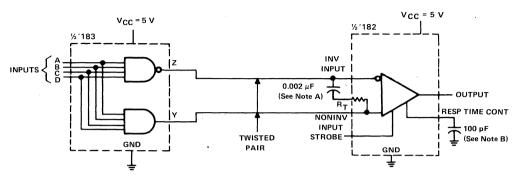
†Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only. NOTE 4: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differentially without the output changing from the low to high level.





[†]Data for temperatures below 0 °C and above 70 °C are applicable to SN55182 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let
$$f = 5$$
 MHz $C = 0.002 \, \mu F$
$$Z_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \, (5 \times 10^6) \, (0.002 \times 10^{-6})}$$
 $Z_C \approx 16 \, \Omega$

B. Use of a capacitor to control response time is optional.

FIGURE 14. TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE

SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

D1292, OCTOBER 1972-REVISED SEPTEMBER 1986

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830

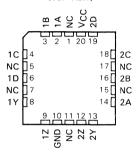
description

The SN55183 and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters, as the output stages are similar to TTL totem-pole outputs.

SN55183 . . . J PACKAGE SN75183 . . . D, J, OR N PACKAGE (TOP VIEW)

| | _ | | _ | |
|-------|---|-------------|---|-----|
| 1A [| 1 | U 14 | Ц | VCC |
| 1B [| 2 | 13 | | 2D |
| 1C 🗌 | 3 | 12 | D | 2C |
| 1D [| 4 | 11 | | 2B |
| 1 Y 🗌 | 5 | 10 | | 2A |
| 1Z [| 6 | 9 | | 2Y |
| GND 🗌 | 7 | 8 | | 2Z |

SN55183 . . . FK PACKAGE (TOP VIEW)

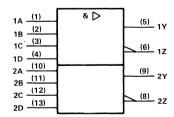


NC-No internal connection.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The SN75183 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

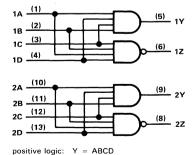
logic symbol†



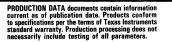
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

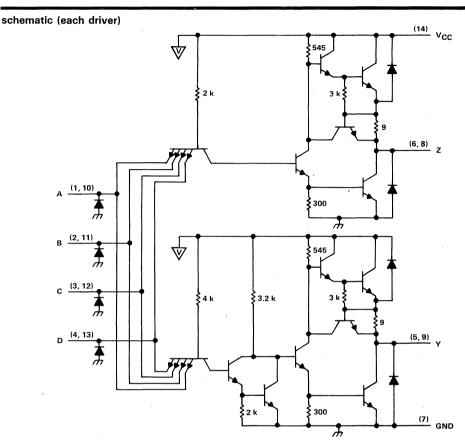


Z = ABCD





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Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55183 | SN75183 | UNIT | | |
|---|------------|-----------------------------|------|--|--|
| Supply voltage, V _{CC} (see Note 1) | 7 | 7 | V | | |
| Input voltage | 5.5 | 5.5 | V | | |
| Duration of output short-circuit (see Note 2) | 1 | 1 | s | | |
| Continuous total power dissipation (see Note 3) | See Dissip | See Dissipation Rating Tabl | | | |
| Operating free-air temperature range | -55 to 125 | 0 to 70 | °C | | |
| Storage temperature range | -65 to 150 | -65 to 150 | °C | | |
| Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C | | |
| Case temperature for 60 seconds: FK package | 260 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | 300 | °C | | |

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
 - 2. Not more than one output should be shorted to ground at a time.
 - 3. In the FK and J packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | T _A = 70°C | T _A = 125°C |
|-------------|-----------------------|---------------------|-----------------------|------------------------|
| TAORAGE | POWER RATING | ABOVE $T_A = 25$ °C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55183) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75183) | 1025 mW | 8.2 mW/°C | 656 mW | 2.000 |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN55183 | | | SN75183 | | |
|------------------------------------|-----|---------|-----|------|---------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | V |
| High-level output current, IOH | | | -40 | | | -40 | mA |
| Low-level output current, IOL | | | 40 | | | 40 | mA |
| Operating free-air temperature, TA | 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended ranges of VCC and operating free-air temperature (unless otherwise noted)

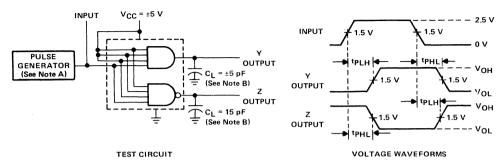
| PARAMETER | | | TEST | CONDITIONS | MIN | TYP† | MAX | UNIT |
|----------------|---|---------|--------------------------|----------------------------|-----|------|------|-------------|
| Vон | High-level output voltage | Y | V _{IH} = 2 V, | $I_{OH} = -0.8 \text{ mA}$ | 2.4 | | | V |
| *UH | Thigh level output veltage | (AND) | $V_{IH} = 2 V$, | $l_{OH} = -40 \text{ mA}$ | 1.8 | 3.3 | | • |
| Vol | Low-level output voltage | OUTPUT | $V_{IL} = 0.8 V$, | $I_{OL} = 32 \text{ mA}$ | | 0.2 | | v |
| VOL | Low-level output voltage | 001701 | $V_{JL} = 0.8 V$, | $I_{OL} = 40 \text{ mA}$ | | 0.22 | 0.4 | • |
| V | High-level output voltage | 7 | $V_{IL} = 0.8 V$, | $I_{OH} = -0.8 \text{ mA}$ | 2.4 | | | V |
| Voн | High-level output voltage | (NAND) | V _{IL} = 0.8 V, | I _{OH} = -40 mA | 1.8 | 3.3 | | |
| \/a. | I are larged and and relations | OUTPUT | $V_{IH} = 2 V$, | $I_{OL} = 32 \text{ mA}$ | | 0.2 | | > |
| VOL | Low-levael output voltage | OUIPUI | V _{IH} = 2 V, | I _{OL} = 40 mA | | 0.22 | 0.4 | · |
| Ιн | High-level input current | | V _{IH} = 2.4 V | a. | | | 120 | μΑ |
| I _I | I Input current at maximum input voltage | | V _{IH} = 5.5 V | | | | 2 | mA |
| IIL | I _{IL} Low-level input current | | V _{IL} = 0.4 V | | | | -4.8 | mA |
| los | IOS Short-circuit output current [‡] | | V _{CC} = 5 V, | T _A = 125°C | -40 | -100 | -120 | mA |
| loo | Supply current (average per | driver) | V _{CC} = 5 V, | All inputs at 5 V, | | 10 | 18 | mA |
| ICC | Supply current (average per driver) | | No load | | | 10 | 10 | |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

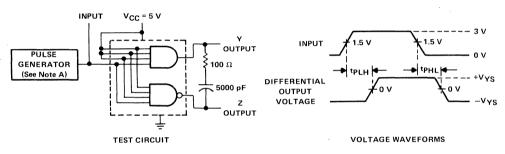
| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|------------------|---|---|----------------------------------|--|-----|-----|------|----|----|
| tPLH | Propagation delay time, low-to-high-level Y output | AND | | | 8 | 12 | ns | | |
| tPHL | Propagation delay time, high-to-low-level Y output | gates C _I = 15 pF, | | 12 | 18 | ns | | | |
| ^t PLH | Propagation delay time, low-to-high-level Z output | NAND | See Figure 1(a) | | 6 | 12 | ns | | |
| ^t PHL | Propagation delay time, high-to-low-level Z output | gates | | | 6 | 8 | ns | | |
| tPLH | Propagation delay time, low-to-high-level differential output | Y output with respect to Z output | · . | $z_{L} = 100 Ω$ Y output $z_{L} = 100 Ω$ | _ | | 9 | 16 | ns |
| tpHL | Propagation delay time high-to-low-level differential output | | with 5000 pF, See Figure 1(b) | | 8 | 16 | ns | | |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Not more than one output should be shorted to ground at a time and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION



(a) OUTPUTS Y AND Z

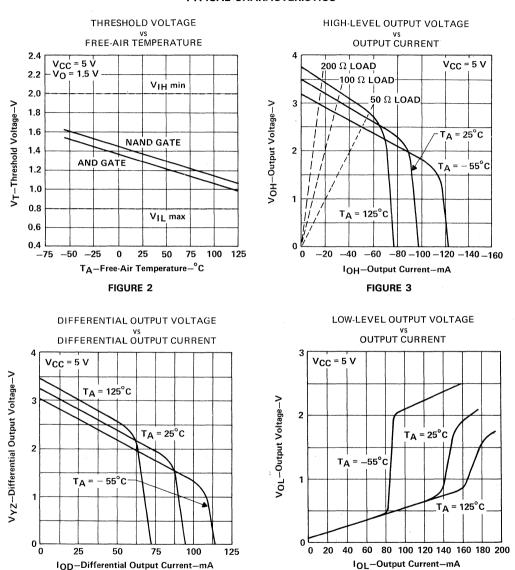


(b) DIFFERENTIAL OUTPUT

NOTES: A. The pulse generators have the following characteristics: $Z_0 = 50~\Omega$, $t_f \le 10~ns$, $t_f \le 10~ns$, $t_W = 0.5~\mu s$, PRR $\le 1~MHz$.

- B. C_L includes probe and jig capacitance.
- C. Waveforms are monitored on an oscilloscope with $R_{in} \geq 1 M\Omega$.

FIGURE 1. PROPAGATION DELAY TIMES



[†]Data for temperatures below 0 °C and above 70 °C are applicable to SN55183 circuits only.

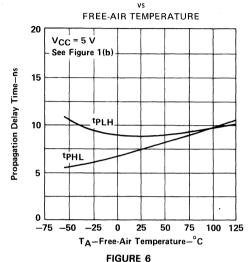
FIGURE 4



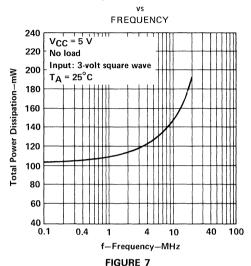
FIGURE 5

TYPICAL CHARACTERISTICS[†]



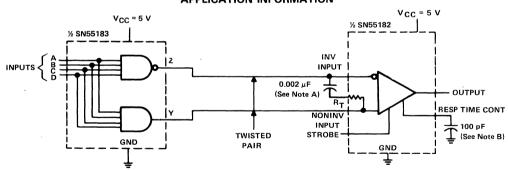


TOTAL POWER DISSIPATION (BOTH DRIVERS)



†Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let
$$f = 5$$
 MHz $C = 0.002 \mu F$
$$Z_C = \frac{1}{2\pi f C} = \frac{1}{2\pi (5 \times 10^6) (0.002 \times 10^{-6})}$$
 $Z_C \approx 16 \Omega$

B. Use of a capacitor to control response time is optional.

FIGURE 8. TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE



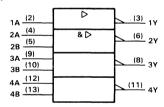
- Meets Specifications of EIA RS-232-C
- Designed to Be Interchangeable With Motorola MC1488
- Current-Limited Output: 10 mA Typ
- Power-Off Output Impedance: 300 Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible With Most TTL Circuits

description

The SN55188 and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with EIA Standard RS-232-C using a diode in series with each supply-voltage terminal as shown under typical applications.

The SN55188 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The SN75188 is characterized for operation from 0 °C to 70 °C.

logic symbol†



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (DRIVERS 2 THRU 4)

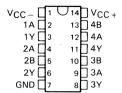
| Α | В | Υ |
|---|---|---|
| Н | Н | L |
| L | Х | Н |
| × | L | Н |

H = high level,

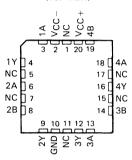
L = low level,

X = irrelevant

SN55188 . . . J PACKAGE SN75188 . . . D OR J PACKAGE (TOP VIEW)

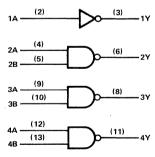


SN55188 . . . FK CHIP CARRIER PACKAGE (TOP VIEW)



NC-No internal connection

logic diagram (positive logic)



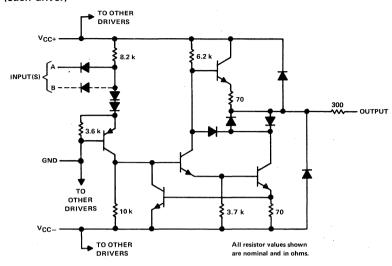
Positive logic

 $Y = \overline{A}$ (driver 1)

 $Y = \overline{AB} \text{ or } \overline{A} + \overline{B} \text{ (drivers 2 thru 4)}$

Pin numbers shown are for D and J packages.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55188 | SN75188 | UNIT | |
|--|-------------------|------------------------------|------------|------|--|
| Supply voltage V _{CC+} at (or below) 25 °C free-air temperature (se | ee Notes 1 and 2) | 15 | 15 | V | |
| Supply voltage V _{CC} at (or below) 25 °C free-air temperature (se | ee Notes 1 and 2) | 15 | 15 | V | |
| Input voltage range | | 15 to 7 | -15 to 7 | V | |
| Output voltage range | | -15 to 15 | -15 to 15 | V | |
| Continuous total power dissipation (see Note 2) | | See Dissipation Rating Table | | | |
| Operating free-air temperature range | | -55 to 125 | 0 to 70 | °C | |
| Storage temperature range | | -65 to 150 | -65 to 150 | °C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or N package | 260 | | °C | |
| Case temperature for 60 seconds | 260 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | J package | 300 | 300 |] | |

NOTES: 1. All voltage values are with respect to the network ground terminal.

For operation above 25 °C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the FK and J packages, SN55188 chips are alloy mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|-------------|---------------------------------------|--|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55188) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75188) | 1025 mW | 8.2 mW/°C | 656 mW | enema . |
| N | 1150 mW | 9.2 mW/°C | 736 mW | _ |

recommended operating conditions

| | | SN55188 | | | SN75188 | | | |
|------------------------------------|------|---------|------|-------|---------|------|------|--|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT | |
| Supply voltage, V _{CC+} | 7.5 | 9 | 15 | 7.5 | 9 | 15 | > | |
| Supply voltage, V _{CC} | -7.5 | -9 | - 15 | - 7.5 | -9 | - 15 | ٧ | |
| High-level input voltage, VIH | 1.9 | | | 1.9 | | | ٧ | |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | ٧ | |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C | |

electrical characteristics over operating free-air temperature range, $V_{CC+} = 9 \text{ V}$, $V_{CC-} = -9 \text{ V}$ (unless otherwise noted)

| | | | | SN | 15518 | В | SI | N75188 | 3 | |
|----------------|--|---|--|------|------------------|--------|-----|------------------|--------|---|
| | PARAMETER | TEST CONDIT | TIONS | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | UNIT |
| | | | | (Sc | e Not | e 3) | (S | ee Note | ∍ 3) | |
| Voн | High-level output voltage | V _{IL} = 0.8 V, | $V_{CC+} = 9 V$, $V_{CC-} = -9 V$ | 6 | 7 | | 6 | 7 | | V |
| VOH | Trigit-level output voltage | R _L = 3 kΩ | $V_{CC+} = 13.2 \text{ V},$ $V_{CC-} = -13.2 \text{ V}$ | 9 | 10.5 | | 9 | 10.5 | | |
| VOL | Low-level output voltage | V _{IH} = 1.9 V, | $V_{CC+} = 9 V$, $V_{CC-} = -9 V$ | | -7 | -6 | | - 7 | -6 | v |
| *OL | Low level desput voltage | R _L = 3 kΩ | $V_{CC+} = 13.2 \text{ V},$ $V_{CC-} = -13.2 \text{ V}$ | _ | 10.5 | - 9 | | - 10.5 | -9 | |
| ΊΗ | High-level input current | V _I = 5 V | | | | 10 | | | 10 | μΑ |
| կլ | Low-level input current | V _I = 0 | | | - 1 | ~1.6 | | - 1 | ~1.6 | mA |
| los(H) | Short-circuit output current at high level ‡ | V _I = 0.8 V, | V ₀ = 0 | -4.6 | -9 | - 13.5 | -6 | -9 | -12 | mA |
| los(L) | Short-circuit output current at low level [‡] | V _I = 1.9 V, | V ₀ = 0 | 4.6 | 9 | 13.5 | 6 | 9 | 12 | mA |
| r _o | Output resistance, power off | $V_{CC+} = 0,$ $V_{O} = -2 \text{ V to 2 V}$ | $V_{CC-} = 0$, | 300 | | | 300 | | | Ω |
| | , | $V_{CC+} = 9 V$, | All inputs at 1.9 V | | 15 | 20 | | 15 | 20 | |
| | | No load | All inputs at 0.8 V | | 4.5 | 6 | | 4.5 | 6 | |
| loo . | Supply current | $V_{CC+} = 12 V$, | All inputs at 1.9 V | | 19 | 25 | | 19 | 25 | mA |
| ICC+ | from V _{CC+} | No load | All inputs at 0.8 V | | 5.5 | 7 | | 5.5 | 7 | IIIA |
| | | $V_{CC+} = 15 V$, | All inputs at 1.9 V | | | 34 | | | 34 | |
| | | No load, T _A = 25°C | All inputs at 0.8 V | | | 12 | | | 12 | |
| | | $V_{CC-} = -9 V$, | All inputs at 1.9 V | | -13 | -17 | | -13 | - 17 | |
| | | No load | All inputs at 0.8 V | | | -0.5 | | _ | 0.015 | |
| 1 | Supply current | $V_{CC-} = -12 V$, | All inputs at 1.9 V | | -18 | - 23 | | 18 | - 23 | |
| ICC - | from ICC - | No load | All inputs at 0.8 V | | | -0.5 | | - | -0.015 | mA |
| | | $V_{CC-} = -15 V$, | All inputs at 1.9 V | | | - 34 | | | - 34 | |
| | | No load, T _A = 25°C | All inputs at 0.8 V | | | ~ 2.5 | | | - 2.5 | |
| PD | Total power dissipation | V _{CC+} = 9 V, No load | V _{CC} − = −9 V, | | | 333 | | | 333 | mW |
| טי | rotal power dissipation | $V_{CC+} = 12 V$, No load | $V_{CC-} = -12 V,$ | | ~ | 576 | | | 576 | *************************************** |

 $^{^{\}dagger}$ All typical values are at $T_A = 25 \,^{\circ}$ C.

NOTE 3: The algebraic convention in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if -6 V is a maximum, the typical value is a more negative voltage.



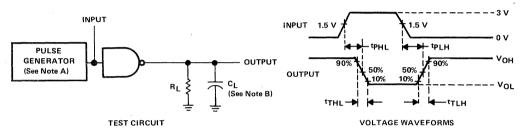
[‡]Not more than one output should be shorted at a time.

switching characteristics, $V_{CC+} = 9 \text{ V}$, $V_{CC-} = -9 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | TEST CO | ONDITIONS | MIN | TYP | MAX | UNIT |
|------|--|------------------------|-------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | , | | 220 | 350 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $R_L = 3 k\Omega$, | C _L = 15 pF, | | 100 | 175 | ns |
| tTLH | Transition time, low-to-high-level output [†] | See Figure 1 | | | 55 | 100 | ns |
| tTHL | Transition time, high-to-low-level output [†] | | | | 45 | 75 | ns |
| tTLH | Transition time, low-to-high-level output [‡] | $R_L = 3 k\Omega$ to 7 | $k\Omega$, $C_L = 2500 pF$, | | 2.5 | | μs |
| †THL | Transition time, high-to-low-level output [‡] | See Figure 1 | | | 3.0 | | μS |

[†]Measured between 10% and 90% points of output waveform.

PARAMETER MEASUREMENT INFORMATION



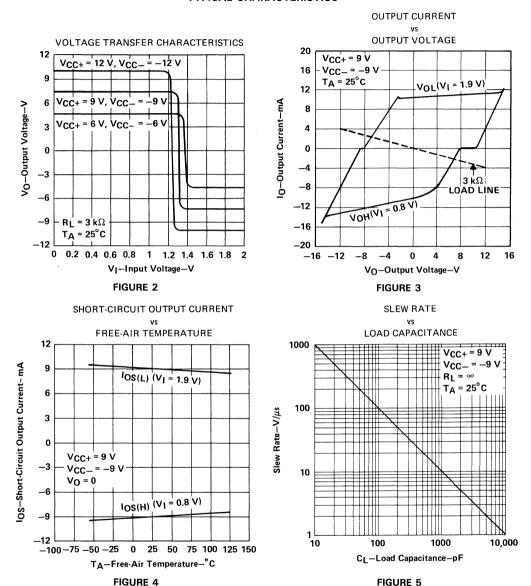
NOTES: A. The pulse generator has the following characteristics: $t_W = 0.5~\mu s$, PRR \leq 1 MHz, $Z_O = 50~\Omega$.

B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION AND TRANSITION TIMES

[‡]Measured between +3 V and -3 V points on the output waveform (EIA RS-232-C conditions)

TYPICAL CHARACTERISTICS[†]

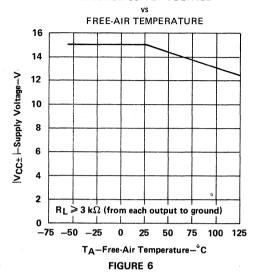


[†]Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.



THERMAL INFORMATION[†]

MAXIMUM SUPPLY VOLTAGE



[†]Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

APPLICATION INFORMATION

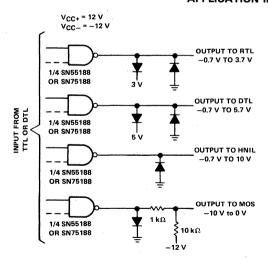


FIGURE 7. LOGIC TRANSLATOR APPLICATIONS

Diodes placed in series with the V_{CC+} and V_{CC}- leads will protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to \pm 15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

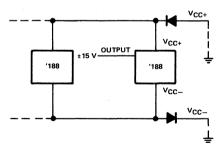


FIGURE 8. POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF EIA STANDARD RS-232-C

SN55189, SN55189A, SN75189, SN75189A **QUADRUPLE LINE RECEIVERS**

D1619, SEPTEMBER 1973-REVISED MAY 1990

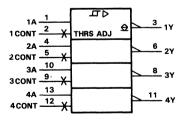
- Input Resistance . . . 3 k Ω to 7 k Ω
- Input Signal Range . . . ±30 V
- Operates from Single 5-V Supply
- **Built-In Input Hysteresis (Double Thresholds)**
- Response Control Provides: Input Threshold Shifting Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C
- Fully Interchangeable with Motorola MC1489, MC1489A

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

The SN55189 and SN55189A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN75189 and SN75189A are characterized for operation from 0°C to 70°C.

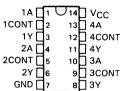
logic symbol†



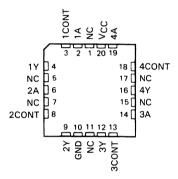
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN55189, SN55189A . . . J PACKAGE SN75189, SN75189A . . . D, J, OR N PACKAGE (TOP VIEW)

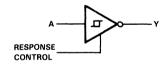


SN55189, SN55189A . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

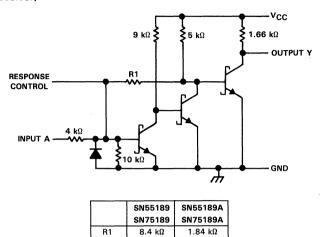
logic diagram (each receiver)





SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN55189 SN55189A | SN75189 SN75189A | UNIT |
|--|---------------------|---------------------|------|
| Supply voltage, V _{CC} (see Note 1) | 10 | 10 | V |
| Input voltage | ±30 | ±30 | V |
| Output current | 20 | 20 | mA |
| Continuous total power dissipation (see Note 2) | See Dissip | ation Rating Tal | ble |
| Operating temperature range | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | -65 to 150 | 65 to 150 | °C |
| Case temperature for 60 seconds: FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300 | 300 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | 260 | °C |

NOTES: 1. All voltage values are with respect to network ground terminals.

In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted and SN75189 and SN75189A chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | T _A = 70°C | T _A = 125°C |
|----------|-----------------------|-----------------|-----------------------|------------------------|
| PACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75) | 1025 mW | 8.2 mW/°C | 656 mW | . N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | . N/A |

SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

electrical characteristics over operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 1\%$, (unless otherwise noted)

| ı | PARAMETER FIGU | | т | TEST CONDITIONS† | | SN5518 SN55189 | | | N75189 N75189 | | UNIT |
|-----------------|-------------------|-----|----------------------|---|-------|-------------------|------|-------|------------------|------|-------|
| | | | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| | | | | T _A = 25°C | 1 | 1.3 | 1.5 | 1 | 1.3 | 1.5 | |
| | | | ′189 | TA = 0°C to 70°C | | | | 0.9 | | 1.6 | |
| V | Positive-going | 1 | | $T_A = -55$ °C to 125°C | 0.6 | | 1.9 | | | | V |
| V _{T+} | threshold voltage | 1 ' | | $T_A = 25$ °C | 1.75 | 1.9 | 2.25 | 1.75 | 1.9 | 2.25 |] |
| ļ | | | ′189A | $T_A = 0$ °C to 70°C | | | | 1.55 | | 2.25 | |
| | | | | $T_A = -55$ °C to 125 °C | 1.30 | | 2.65 | | | | |
| | Negative-going | | ′189, | $T_A = 25$ °C | 0.75 | 1.0 | 1.25 | 0.75 | 1.0 | 1.25 | |
| VT - | threshold voltage | 1 | 189A | $T_A = 0$ °C to 70 °C | | | | 0.65 | | 1.25 | V |
| | | | | $T_A = -55$ °C to 125 °C | 0.35 | | 1.6 | | | | |
| VOH | High-level | 1 | $V_1 = 0.7$ | $^{\prime}5 \text{ V}, \text{IOH} = -0.5 \text{ mA}$ | 2.6 | 4 | 5 | 2.6 | 4 | 5 | l v l |
| ТОП | output voltage | · | Input ope | en, $I_{OH} = -0.5 \text{ mA}$ | 2.6 | 4 | 5 | 2.6 | 4 | 5 | · · |
| VOL | Low-level | 1 | Vi = 3 \ | /, I _{OL} = 10 mA | | 0.2 | 0.45 | | 0.2 | 0.45 | v |
| · OL | output voltage | | | | | U.Z | | | | 0.40 | · |
| Ιн | High-level | 2 | $V_1 = 25$ | | 3.6 | | 8.3 | 3.6 | | 8.3 | mA |
| .111 | input current | _ | V _I = 3 \ | | 0.43 | | | 0.43 | | | |
| IIL | Low-level | 2 | $V_{1} = -2$ | | -3.6 | | -8.3 | -3.6 | | ~8.3 | mA |
| 'IL | input current | | $V_I = -3$ | 3 V | -0.43 | | | -0.43 | | | |
| los | Short-circuit | 3 | | | | -3 | | | -3 | | mA |
| .03 | output current | | | | | | | | | | |
| lcc | Supply current | 2 | V ₁ = 5 \ | /, Outputs open | | 20 | 26 | | 20 | 26 | mA |

[†] All characteristics are measured with the response control terminal open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|----------------|--|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | $C_L = 15 \text{ pF}, R_L = 3.9 \text{ k}\Omega$ | | 25 | 85 | ns |
| †PHL | Propagation delay time, high-to-low-level outut | _ | $C_L = 15 pF, R_L = 390 \Omega$ | | 25 | 50 | 115 |
| †TLH | Transition time, low-to-high-level output | 1 - | $C_L = 15 \text{ pF}, R_L = 3.9 \text{ k}\Omega$ | | 120 | 175 | ns |
| tTHL | Transition time, high-to-low-level output | | $C_L = 15 \text{ pF}, R_L = 390 \Omega$ | | 10 | 20 | 115 |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

PARAMETER MEASUREMENT INFORMATION[†]

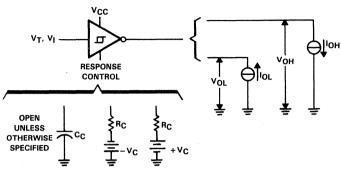
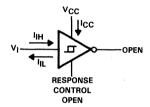


FIGURE 1. V_{T+}, V_{T-}, V_{OH}, V_{OL}



ICC is tested for all four receivers simultaneously

FIGURE 2. IIH, IIL, ICC

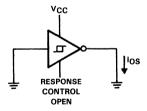
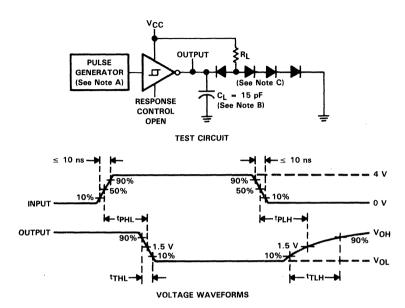


FIGURE 3. IOS

[†]Arrows indicate actual direction of current flow. Current into a terminal is a positive value.



NOTES: A. The pulse generator has the following characteristics: $Z_0 \approx 50 \ \Omega$, $t_w = 500 \ ns$.

- B. C_L includes probe and jig capacitances.C. All diodes are 1N3064 or equivalent.

FIGURE 4. SWITCHING TIMES

TYPICAL CHARACTERISTICS

SN55189, SN75189 OUTPUT VOLTAGE

VS

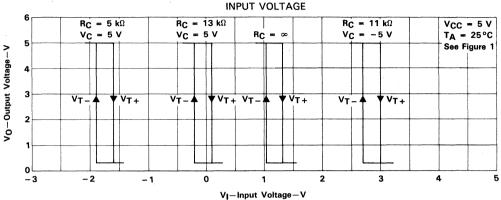


FIGURE 5

SN55189A, SN75189A OUTPUT VOLTAGE

vs

INPUT VOLTAGE

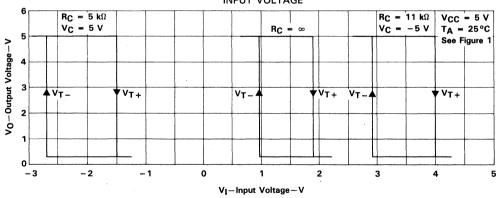
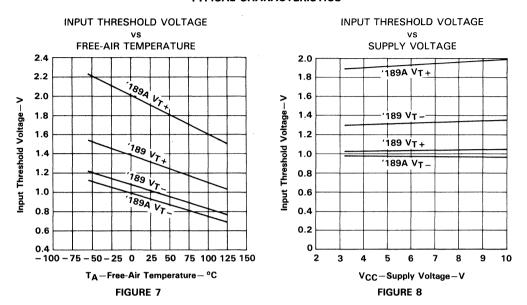
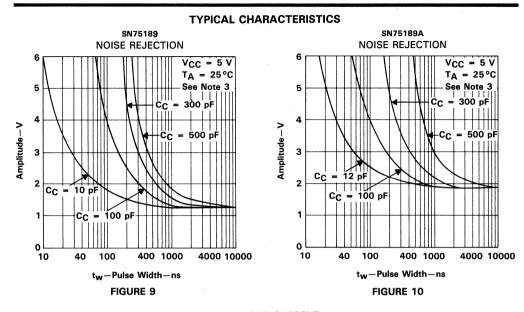


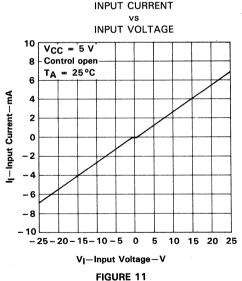
FIGURE 6

TYPICAL CHARACTERISTICS[†]



†Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.





NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

SN55ALS056. SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

D3275 APRII 1989

SUITABLE FOR IEEE STANDARD 896 APPLICATIONS[†]

- SN55ALS056 Is an Octal Transceiver
- SN55ALS057 Is a Quad Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 60 mW/Channel Max
- High-Impedance P-N-P Inputs
- BTL™ Logic Level 1-V Bus Swing Reduces **Power Consumption**
- Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines
- Power-Up/Down Protection (Glitch-Free)
- Open-Collector Driver Outputs Allow Wired-OR Connections

PRODUCTION DATA documents contain information

current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

description

The SN55ALS056 is an 8-channel, monolithic. high-speed, Advanced Low-Power Schottky device designed for 2-way data communication in a densely populated backplane. The SN55ALS057 is a 4-channel version with independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each driver (En). Both are compatible with Backplane Tranceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

SN55ALS056 . . . J OR W PACKAGE

| (7 | OP V | (IEW) |
|-------|------|---------|
| A1 [| 1 U | 20 B1 |
| A2 [| 2 | 19 B2 |
| аз [| 3 | 18 🗌 B3 |
| A4 🗌 | 4 | 17 B4 |
| vcc [| 5 | 16 GND |
| A5 [| 6 | 15 B5 |
| A6 🗆 | 7 | 14 🗌 B6 |
| A7 [| 8 | 13 🗀 B7 |
| A8 [| 9 | 12 B8 |
| cs [| 10 | 11∐T/Ř |

SN55ALS057 . . . J OR W PACKAGE (TOP VIEW)

| D1 [| ſī | U20 B1 |
|-------|----|---------|
| R1 🗌 | 2 | 19 E1 |
| D2 [| 3 | 18 B2 |
| R2 🗌 | 4 | 17 E2 |
| vcc [| 5 | 16 GNE |
| D3 [| 6 | 15🏻 B3 |
| R3 🗌 | 7 | 14 🗍 E3 |
| D4 🗌 | 8 | 13 🗍 B4 |
| R4 [| 9 | 12 E4 |
| TE [| 10 | 11 RE |

These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN55ALS056 and SN55ALS057 are characterized for operation from -55°C to 125°C.

† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range. BTL is a trademark of National Semiconductor Corporation.

SN55ALS056, SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

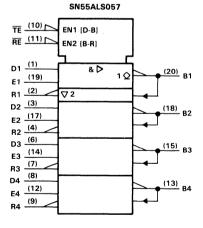
| | FK PACKAGE P VIEW) | SN55ALS057 FK PACKAGE (TOP VIEW) | | | | | |
|--------|-----------------------|---|---------|--|--|--|--|
| 3 2 | 1 20 19 | 2 2 1 2 4 A A A A A A A A A A A A A A A A A A | E 20 19 | | | | |
| R2 🕽 4 | 18 🛛 B2 | A4 🕽 4 | 18 🛛 B3 | | | | |
| Vcc D⁵ | 17 🛛 E2 | ∨cc þ ₅ | 17 🚺 B4 | | | | |
| D3 🕽 6 | 16 🛛 GND | A5 🕽 6 | 16 GND | | | | |
| R3 🗓 7 | 15 ☐ B 3 | A6 🕽 7 | 15 B5 | | | | |
| D4 🕽 8 | 14 🛛 E3 | A7 🕽 8 | 14 🛚 B6 | | | | |
| 9 10 | 11 12 13 | 9 10 11 | 12 13 | | | | |
| 1 3 개 | | 8 SS IR | 88 | | | | |

SN55ALS056, SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

logic symbols†

T/R (11) 3EN1 (A-B) 3EN2 (B-A) CS (10) G3 (20) B1 A1 (1) $\overline{\mathsf{D}}$ 10 **▽** 2 (1<u>9)</u> B2 A2 (2) A3 (3) (18) - вз (17) В4 (1<u>5)</u> B5 A5 (6) A6 (7) (14) В6 (<u>13)</u> B7 (<u>12)</u> B8 A8 —(9)

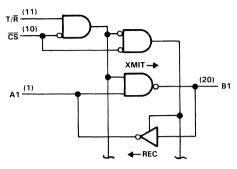
SN55ALS056



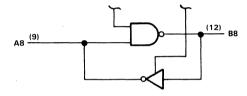
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

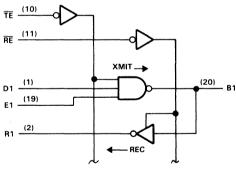
SN55ALS056



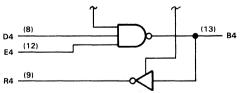
6 IDENTICAL CHANNELS NOT SHOWN



SN55ALS057



2 IDENTICAL CHANNELS NOT SHOWN



SN55ALS056 FUNCTION TABLE TRANSMIT/RECEIVE

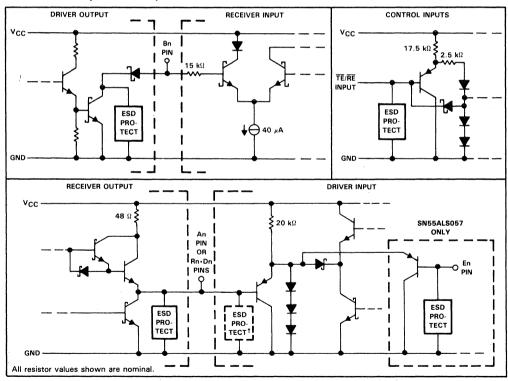
| CONT | ROLS | CHANNELS |
|------|------|-----------|
| CS | T/R | A↔B |
| L | Н | T (A → B) |
| L | L | R (B → A) |
| н | X | D |

SN55ALS057 FUNCTION TABLE TRANSMIT/RECEIVE

| C | ONTRO | LS | CHANNELS | | | |
|----|-------|----|----------|-----|--|--|
| TE | RE | En | D→B | B→R | | |
| L | L | L | D | R | | |
| L | L | н | Т | R | | |
| L | н | L | D | D - | | |
| L | н | Н | Т | D | | |
| н | L | Х | D | R | | |
| Н | Н | Х | D | D | | |

H = high-level, L = low-level, R = receive, T = transmit, D = disable, X = irrelevantDirection of data transmission is from An to Bn for the SN55ALS056 and from Dn to Bn for the SN55ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



[†]Additional ESD protection is on the SN55ALS057, which has separate receiver output and driver input pins.

SN55ALS056, SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | | | |
|--|--|--|--|
| Control input voltage | | | |
| Driver input voltage | | | |
| Driver output voltage | | | |
| Receiver input voltage | | | |
| Receiver output voltage | | | |
| Control input voltage | | | |
| (see Note 2) | | | |
| Operating free-air temperature range | | | |
| Storage temperature range65°C to 150°C | | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | | | |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|-----|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | V |
| High-level driver and control input voltage, VIH | 2 | | | V |
| Low-level driver and control input voltage, VIL | | | 0.8 | V |
| Bus termination voltage | 1.9 | | 2.1 | ٧ |
| Operating free-air temperature, TA | - 55 | | 125 | °C |

SN55ALS056, SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

SN55ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | ₹ | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|----------------------------|------------------|--|------|------------------|-------|------|
| ViK | Input clamp voltage at Ar | , T/R, or CS | $V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$ | | | - 1.5 | V |
| Vτ | Receiver input threshold a | at Bo | $V_{CC} = 5 \text{ V}, T_A = 25 \text{ °C}$ | 1.45 | | 1.65 | V |
| ٧, | | | $V_{CC} = 5 \text{ V}, T_A = -55 ^{\circ}\text{C to } 125 ^{\circ}\text{C}$ | 1.4 | | 1.7 | • |
| | | | V _{CC} = 4.5, Bn at 1.2 V, | | | | |
| Voн | High-level output voltage | at An | CS at 0.8 V, T/R at 0.8 V, | 2.4 | | | V |
| | | | $I_{OH} = -400 \mu A$ | | | | |
| | | | $V_{CC} = 4.5 \text{ V}$, Bn at 2 V, | | | | |
| | Low-level output voltage | An | CS at 0.8 V, T/R at 0.8 V, | | | 0.5 | |
| ., | | | T/\overline{R} at 0.8 V, $I_{OL} = 16 \text{ mA}$ | | | | v |
| VOL | | Bn | $V_{CC} = 4.5 \text{ V}, \text{ An at 2 V},$ | | | | v |
| | | | CS at 0.8 V, T/R at 2 V, | 0.75 | | 1.2 | |
| | | | See Figure 1 | | | | |
| | | An, T/R, or CS | $V_I = V_{CC} = 5.5 V$ | | | 40 | |
| ΊΗ | High-level input current | Bn | $V_{CC} = 5.5 \text{ V}, V_1 = 2 \text{ V},$ | 1 | | 100 | μΑ |
| | | DII | An at 0.8 V, T/R at 0.8 V | | | 100 | |
| I _I L | Low-level input current at | : An, T/R, or CS | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.4 \text{ V}$ | | | -400 | μΑ |
| | | | V _{CC} = 5.5 V, An at 0 V, | | | | |
| los | Short-circuit output curre | nt at An | Bn at 1.2 V, | -35 | | - 125 | μΑ |
| | | | T/R at 0.8 V | | | | |
| lcc | Supply current | | V _{CC} = 5.5 V | | | 85 | mA |
| C _{o(B} | Driver output capacitance | • | | | 4.5 | | pF |

SN55ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | 3 | TES | T CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|-------------------|---------------------------|--------------------------|------|------------------|-------|------|
| VIK | Input clamp voltage at Dr | , En, TE, or RE | $V_{CC} = 4.5 \text{ V},$ | I _I = -18 mA | | | -1.5 | ٧ |
| Vτ | V _T Receiver input threshold at Bn | | $V_{CC} = 5 V$, | T _A = 25°C | 1.45 | | 1.65 | V |
| ۷١ | neceiver input titrestiona a | IL DII | $V_{CC} = 5 V$, | $T_A = -55$ °C to 125 °C | 1.4 | | 1.7 | · · |
| Vou | High-level output voltage | at Rn | $V_{CC} = 4.5,$ | Bn at 1.2 V, | 2.4 | | | |
| VOH | | at mi | RE at 0.8 V, | $I_{OH} = -400 \mu A$ | 2.4 | | | ٧ |
| | | Rn | $V_{CC} = 4.5 V$, | Bn at 2 V, | | | 0.5 | |
| | | FWI | RE at 0.8 V, | I _{OL} = 16 mA | | | 0.5 | |
| VOL | Low-level output voltage | | $V_{CC} = 4.5 V$, | Dn at 2 V, | | | | V |
| | | Bn | En at 2 V, | TE at 0.8 V | 0.75 | | 1.2 | |
| | | | See Figure 1 | | | | | |
| | | Dn, En, TE, or RE | $V_I = V_{CC} = 5.5$ | | | 40 | | |
| 1 | High-level input current | | $V_{CC} = 5.5 V$, | $V_1 = 2 V$, | | | | μΑ |
| ΉΗ | riigii-level iliput current | Bn | Dn at 0.8 V, | En at 0.8 V, | | | 100 | μΑ |
| | | | TE at 0.8 V | | | | | |
| կլ | Low-level input current at | Dn, En, TE, or RE | $V_{CC} = 5.5 V$, | V _I = 0.4 V | | | -400 | μΑ |
| loo | Short-circuit output ourro | nt at Pa | $V_{CC} = 5.5 V,$ | Rn at 0 V, | - 35 | | -125 | |
| los | OS Short-circuit output current at Rn | | Bn at 1.2 V, | RE at 0.8 V | - 33 | | - 125 | μΑ |
| Icc | Supply current | | V _{CC} = 5.5 V | | | | 45 | mA |
| C _{o(B)} | Driver output capacitance | | | | | 4.5 | | pF |

 $^{^{\}dagger}All$ typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CON | DITIONS | TA [†] | MIN | ТҮР | мах | UNIT | | |
|------------------|---------------------------|-----------------|----------------|--------------------------------|--------------------|-----------------|---------------|------|-----|------|----|----|
| *m | Propagation delay time, | | | CS at 0.8 V, | T/R at 0.8 V, | 25 °C | | | 20 | | | |
| ^t PLH | low- to high-level output | Bn | An | $V_1 = 5 V$ | S1 closed, | Full range | | | 22 | ns | | |
| * | Propagation delay time, | BII | An | See Figure 4 | 51 Closed, | 25°C | | | 18 | 115 | | |
| tPHL | high- to low-level output | | | See rigure 4 | | Full range | | | 20 | | | |
| | Output disable time | | | Bn at 2 V, | T/R at 0.8 V, | 25 °C | | | 20 | | | |
| ^t PLZ | from low level | CS | | | S1 closed, | Full range | | | 22 | ns | | |
| | Output enable time | LS | An | V _L = 5 V, | 51 ciosea, | 25 °C | | | 13 | ns | | |
| tPZL | to low level | 1 | | See Figure 5 | | Full range | | | 14 | | | |
| | Output disable time | | | Bn at 0.8 V, | T/R at 0.8 V, | 25°C | | | 12 | | | |
| tPHZ | from high level | CS | | V _L = 0, S1 closed, | See Figure 5 | Full range | | | 13 | | | |
| | Output enable time | CS | I An 🛌 | An | All | Bn at 0.8 V, | T/R at 0.8 V, | 25°C | | | 14 | ns |
| ^t PZH | to high-level | ! | | S1 open, | See Figure 5 | Full range | | | 22 | | | |
| | Output disable time | | | CS at 0.8 V. | VC 0 V | 25°C | | | 17 | | | |
| ^t PLZ | from low level | T/R | | 1 | VC at 2 V, | Full range | | | 20 | | | |
| | Output enable time | 1 1/8 | An | V _L = 5 V, | S1 closed, | 25°C | | | 25 | ns | | |
| tPZL | to low level | | ĺ | See Figure 5 | | Full range | | | 40 | | | |
| | Output disable time | | | CS at 0.8 V, | V _L = 0 | 25 °C | | | 12 | | | |
| [‡] PHZ | from high level | T/R | | S1 closed, | See Figure 5 | Full range | | | 13 | | | |
| | Output enable time | 1 1/8 | An | CS at 0.8 V, | S1 open, | 25°C | | | 15 | ns | | |
| ^t PZH | to high level | 1 | | See Figure 5 | | Full range | | | 22 | | | |
| | Receiver noise rejection | - P- | An | | S1 closed, | 25°C | 4 | | | | | |
| tw(NR) | pulse duration | Bn | or Rn | See Figure 6 | | Full range | 2 | | | ns | | |

driver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CON | DITIONS | TA [†] | MIN | TYP‡ | мах | UNIT | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|---------------------------|--|--------------------|-----------------------|--------------------------|-----------------|-----|------|-----|------|-----|-----|------------|--------------------|------|-----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|--|------|--|--|----|-----|
| + | Propagation delay time, | | | | | 25°C | | | 10 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ^t PLH | low- to high-level output | An | Bn | CS at 0.8 V, | T/\overline{R} at 2 V, | Full range | | | 40 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Propagation delay time, | An | Bn | V _L = 2 V, | See Figure 2 | 25°C | | | 12 | ns | | | | | | | | | | | | | | | | | | | | | | | | | |
| tPHL | high- to low-level output | | | | | Full range | | | 15 | l | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Propagation delay time, | CS Bn | | | | 25°C | | | 18 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| tPLH | low- to high-level output | | An and T/R at 2 V, | $V_L = 2 V$, | Full range | | | 30 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Propagation delay time, | LS | , bn | ы | ы | Dn i | DΠ | ы | ы | DII | DII | DII | DII | See Figure 2 25 °C | 25°C | | | 20 | ns | | | | | | | | | | | | | | | | |
| tPHL | high- to low-level output | | | | | Full range | | | 22 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Propagation delay time, | | | | 25°C | | | 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| tPLH | low- to high-level output | T/R | D., | CS at 0.8 V, | $V_L = 2 V$, | Full range | | | 37 | l | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Propagation delay time, | 1/ | Bn | Bn | Bu | gn | Bn | Bn | Bn | Bn | Bn | Bn | Bn | Bn | ы | DII | Bn | Bn | Bn | Bn | Bn | Bn | Bn | Bn | Bu | Bu | Bn | Bn | See Figure 3 | | 25°C | | | 18 | .ns |
| tPHL | high- to low-level output | İ | | | | | | | | | | | Full range | | | 21 | 1 | | | | | | | | | | | | | | | | | | |
| | Transition time, | | | | | 25°C | 1 | 3 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| tTLH | low- to high-level output | ۸., | D= | CS at 0.8 V, | T/\overline{R} at 2 V, | Full range | 1 | | 33 |] | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Transition time, |] An | An Bn | V _L = 2 V, | See Figure 2 | 25°C | 1 | 3 | 10 | ns | | | | | | | | | | | | | | | | | | | | | | | | | |
| tTHL | high- to low-level output | | | | | Full range | 1 | | 13 | | | | | | | | | | | | | | | | | | | | | | | | | | |

[†]Full range is -55°C to 125°C.



 $^{^{\}ddagger}$ Typical values are at $V_{CC} = 5$.

SN55ALS056, SN55ALS057 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CO | ONDITIONS | TA [†] | MIN | MAX | UNIT | |
|---------------------|---------------------------|-----------------|----------------|-----------------------|-----------------------------|-----------------|------------|-----|------|----|
| • | Propagation delay time, | | | RE at 0.8 V. | TE at 2 V, | 25°C | | 20 | | |
| ^t PLH | low- to high-level output | Bn | Rn | $V_1 = 5 V$ | S1 closed, | Full range | | 22 | ns | |
| | Propagation delay time, | DII | nii | See Figure 4 | ST closed, | 25°C | | 18 | IIS | |
| tPHL | high- to low-level output | | | See Figure 4 | | Full range | | 20 | 1 | |
| Output disable time | | | D 0.1/ | ŦĒ . 0.1/ | 25°C | | 15 | | | |
| tPLZ. | from low level | RE | n- 1 | . | Bn at 2 V, | TE at 2 V, | Full range | | 17 | |
| | Output enable time | HE | | - | V _L = 5 V, | S1 closed, | 25°C | | 13 | ns |
| tPZL | to low level | } | | See Figure 5 | | Full range | | 14 | 1 | |
| | Output disable time | | | Bn at 0.8 V, TE | at 2 V, V _L = 0, | 25°C | | 12 | | |
| ^t PHZ | from high level | RE | ο. | S1 closed, | See Figure 5 | Full range | | 13 | | |
| | Output enable time | HE | Rn | Bn at 0.8 V, | TE at 2 V, | 25°C | | 14 | ns | |
| ^t PZH | to high-level | | | S1 closed, | See Figure 5 | Full range | | 15 | l | |
| | Receiver noise rejection | _ | | V _L = 5 V, | S1 closed, | 25°C | 4 | | | |
| tw(NR) | pulse duration | Bn | Rn | See Figure 6 | | Full range | 2 | | ns | |

driver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CO | ONDITIONS | TA [†] | MIN TY | P‡ | MAX | UNIT | |
|------------------|---------------------------|-----------------|----------------|-----------------------|-----------------|-----------------|------------|----|-----|------|--|
| | Propagation delay time, | | | | | 25°C | | | 10 | | |
| tPLH | low- to high-level output | Dn | Bn | TE at 0.8 V, | RE at 2 V, | Full range | | | 27 | | |
| | Propagation delay time, | or En | DII | V _L = 2 V, | See Figure 2 | 25°C | | | 12 | ns | |
| tPHL | high- to low-level output | | | | | Full range | | | 15 | | |
| | Propagation delay time, | | | | | 25°C | | | 10 | | |
| ^t PLH | low- to high-level output | | | Dn, En, RE at 2 | $V, V_L = 2 V,$ | Full range | | | 27 | | |
| | Propagation delay time, | TE | Bn | See Figure 2 | | 25°C | | | 17 | ns | |
| tPHL | high- to low-level output | | | | | Full range | | | 19 | | |
| | Transition time, | | | | | 25°C | 1 / | 3 | 8 | | |
| tTLH | low- to high-level output | Dn | ο- | RE at 2 V, | $V_L = 2 V$ | Full range | 1 | | 33 | | |
| | Transition time, | or En | Bn | See Figure 2 | | 25°C | 1 | 3 | 10 | ns | |
| [‡] THL | high- to low-level output | | | | | | Full range | 1 | | 13 | |

 $^{^{\}ddagger}$ Typical values are at $V_{CC} = 5 \text{ V}.$

driver plus receiver

| | PARAMETER FROM (INPUT) (| | TO (OUTPUT) | TEST CONDITIONS | TA [†] | MIN MAX | UNIT |
|------------------|---------------------------|------|----------------|---------------------------|-----------------|---------|------|
| | Propagation delay time, | | | RE at 0.8 V, TE at 0.8 V, | 25°C | 25 | |
| ^t PLH | low- to high-level output | - Dn | Rn | | Full range | 35 | ns |
| | Propagation delay time, | υn | - Di | | 25°C | 25 | |
| tPHL | high- to low-level output | | | (Both loads are used) | Full range | 35 | |

[†]Full range is -55°C to 125°C.

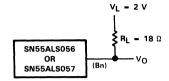
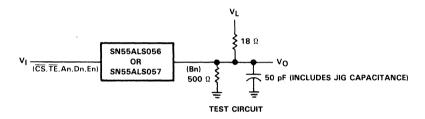
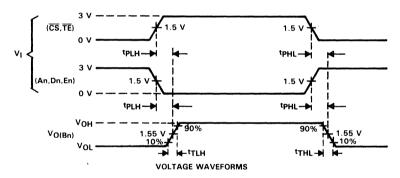


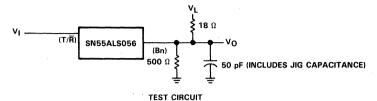
FIGURE 1. TEST CIRCUIT FOR DRIVER LOW-LEVEL OUTPUT VOLTAGE

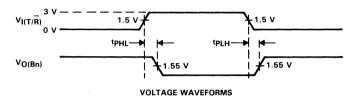




NOTE: $t_f = t_f \le 5$ ns from 10% to 90%.

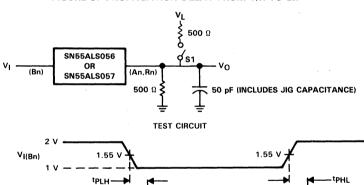
FIGURE 2. DRIVER PROPAGATION DELAY TIMES





NOTE: $t_r = t_f \le 5$ ns from 10% to 90%.

FIGURE 3. PROPAGATION DELAY FROM T/R TO Bn

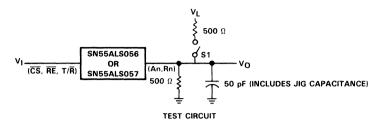


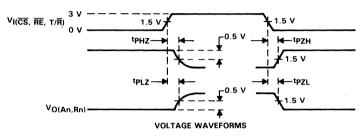
VOLTAGE WAVEFORMS

NOTE: $t_f = t_f \le 10 \text{ ns from } 10\% \text{ to } 90\%$.

VO(An,Rn)

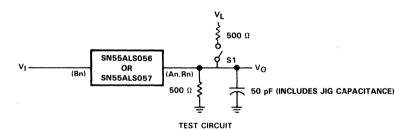
FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

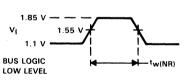


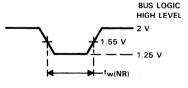


NOTE: $t_r = t_f \le 5$ ns from 10% to 90%.

FIGURE 5. PROPAGATION DELAY FROM CS OR T/R TO An OR FROM RE TO Rn







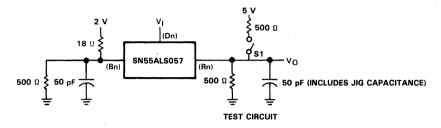
tw is increased until the output voltage fall just reaches 2.0 V. tw is increased until the output voltage rise just reaches 0.8 V.

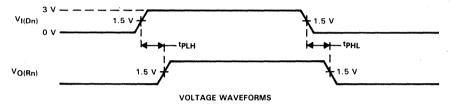
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \le 2$ ns from 10% to 90%.

FIGURE 6. RECEIVER NOISE IMMUNITY







NOTE: $t_r = t_f \le 5$ ns from 10% to 90%.

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

D2299 FERRUARY 1986-REVISED OCTOBER 1989

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN55ALS130 and SN75ALS130)
- Minimum Output Voltage of 3.11 V at IOH = −60 mA
- Fault Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current Limit Circuit Minimizes Power Dissipation During a Fault Condition
- Advanced Low-Power Schottky Circuitry
- Dual Common Enable
- Individual Fault Flags
- Designed to Be an Improved Replacement for the MC3481

description

The SN55ALS126 and SN75ALS126 quadruple line drivers are designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at $I_{OH} = -59.3$ mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN55ALS126 and SN75ALS126 are compatible with standard TTL logic and supply voltages.

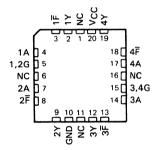
The SN55ALS126 and SN75ALS126 employ the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low

SN55ALS126, SN75ALS126...J PACKAGE SN75ALS126...D OR N PACKAGE

(TOP VIEW)

| 1Y [|]1 | U 16 | П | VCC |
|--------|----|------|---|------|
| 1F [|]2 | 15 | | 4Y |
| 1A [|]3 | 14 | р | 4Ē |
| 1,2G [|]4 | 13 | Д | 4A |
| 2A [|]5 | 12 | | 3,4G |
| 2F [|]6 | 11 | | 3A |
| 2Y [|]7 | 10 | Д | 3Ē |
| GND [|]8 | 9 | | 3Y |

SN55ALS126 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

| INP | UTS | OUTPUTS | | | |
|-----|-----|---------|---|--|--|
| G | Α | Υ | F | | |
| L | Х | L | Н | | |
| н | H | н | Н | | |
| Н | Н | s | L | | |

H = high level, L = low level, X = irrelevant, S = shorted to ground

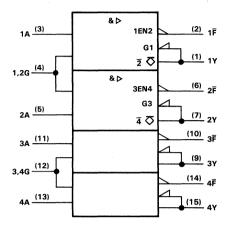
The SN55ALS126 and SN75ALS126 can drive a $50-\Omega$ load as required in the IBM GA22-6974-3 specification or a $90-\Omega$ load as used in many I/O systems. Optimum performance can be achieved when the devices are used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN55ALS126 is characterized for operation from $-55\,^{\circ}$ C to 125 $^{\circ}$ C, and the SN75ALS126 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

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Texas V Instruments

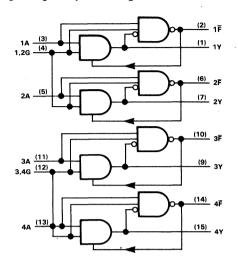
logic symbol†



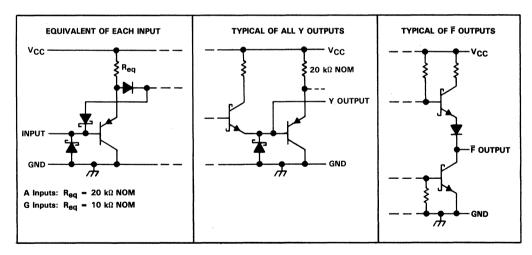
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC |
|---|
| Input voltage |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN55ALS126 55°C to 125°C |
| SN75ALS126 0 °C to 70 °C |
| Storage temperature range65°C to 150°C |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | TA - 70°C | TA = 125°C |
|----------------|-----------------------|-----------------|--------------|--------------|
| PACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55ALS126) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75ALS126) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |

recommended operating conditions

| | SI | SN55ALS126 SN75ALS126 | | 26 | UNIT | | |
|------------------------------------|------|-----------------------|-------|-----------------|------|--------|-----------|
| | MIN | NOM | MAX | MAX MIN NOM MAX | | MAX | ן ייייי ך |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.95 | 4.5 | 5 | 5.95 | ٧ |
| High-level input voltage, VIH | 2 | | | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | ٧ |
| High-level output current, IOH | | | -59.3 | | | - 59.3 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

SN55ALS126, SN75ALS126 QUADRUPLE LINE DRIVERS

electrical characteristics over recommended operating free-air temperature range

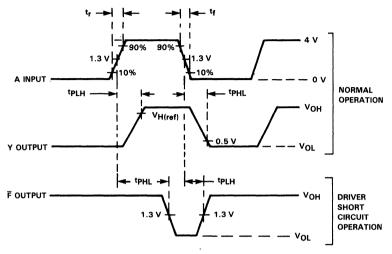
| PARAMETER | | | TEST CONDITIONS | MIN | MAX | UNIT | |
|-----------------|---------------------------|--------|--|---|-----------------|-------|--|
| VIK | input clamp voltage | A,G | $V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$ | | - 1.5 | ٧ | |
| | | Υ | $V_{CC} = 4.5 \text{ V}, I_{OH} = -59.3 \text{ mA}$ $V_{IH} = 2 \text{ V}$ | 3.11 | | | |
| Vон | High-level output voltage | Υ | $V_{CC} = 5.25 \text{ V}, I_{OH} = -41 \text{ mA}$ $V_{IH} = 2 \text{ V}$ | 3.9 | | ٧ | |
| | | F | $V_{CC} = 4.5 \text{ V}, I_{OH} = -400 \mu\text{A}$ $V_{IH} = 2 \text{ V}$ | 2.5 | | | |
| | | Υ | $V_{CC} = 5.5 \text{ V}, I_{OL} = -240 \mu\text{A},$ $V_{IL} = 0.8 \text{ V}$ | | 0.15 | | |
| VOL | Low-level output voltage | Υ | $V_{CC} = 5.95 \text{ V}, I_{OL} = -1 \text{ mA},$ $V_{IL} = 0.8 \text{ V}$ | | 0.15 | ٧ | |
| | | F | $V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}, \text{Y at 0 V}$ | | 0.5 | | |
| IO(off) | Off-state output current | Υ | $V_{CC} = 4.5 \text{ V}, V_{1} = 0, \qquad V_{O} = 3.11 \text{ V}$ | | 100 | μΑ | |
| ·O(011) | On state output current | Υ | $V_{CC} = 0$, $V_{I} = 0$, $V_{O} = 3.11 V$ | | 200 | μ | |
| 1. | Input current | Α | V _{CC} = 4.5 V, V _I = 5.5 V | | 100 | μΑ | |
| · I | input current | G | | | 400 | | |
| Ιн | High-level input current | A G | $V_{CC} = 4.5 \text{ V}, V_{I} = 2.7 \text{ V}$ | | 20 80 | μΑ | |
| I _{IL} | Low-level input current | A G | V _{CC} = 5.95 V, V _I = 0.4 V | | - 250 - 1000 | μΑ | |
| | | Υ | $V_{CC} = 5.5 \text{ V}, V_{O} = 0, \qquad V_{IH} = 2.7 \text{ V}$ | | -5 | | |
| los | Short-circuit output | | F | V _{CC} = 5.5 V, V _O = 0 | -15 | - 100 | |
| | | Υ | $V_{CC} = 5.95 \text{ V}, V_{O} = 0, V_{IH} = 2.7 \text{ V}$ | | -5 | mA | |
| | | F | $V_{CC} = 5.95 \text{ V}, V_{O} = 0$ | - 15 | -110 | | |
| | Supply current, all | | V _{CC} = 5.5 V, No load, V _{IH} = 2.7 V | | 25 | 4 | |
| ІССН | outputs high | | $V_{CC} = 5.95 \text{ V}$, No load, $V_{IH} = 2.7 \text{ V}$ | | 27 | mA | |
| 1 | Supply current, | | V _{CC} = 5.5 V, No load, V _{IL} = 0.4 V | | 45 | mA | |
| ICCL | Y outputs low | | V _{CC} = 5.95 V, No load, V _{IL} = 0.4 V | | 47 | IIIA | |

switching characteristics over recommended operating free-air temperature range

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|----------|----|--|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | | V _{CC} = 4.5 V to 5.5 V, | | 30 | ns |
| [†] PHL | Propagation delay time, high-to-low-level output | A | Y | $R_L = 50 \Omega$, $C_L = 50 pF$ $V_{H(ref)} = 3.11 V^{\dagger}$, | , | 28 | ns |
| tPLH tPHL | Ratio of propagation delay times | | | See Figures 1 and 2 | 0.3 | 3 | |
| [†] PLH | Propagation delay time, low-to-high-level output | A | Υ | $V_{CC} = 5.25 \text{ V to } 5.95 \text{ V},$ $R_L = 90 \Omega,$ $C_L = 50 \text{ pF}$ | , | 34 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | <u> </u> | ľ | V _{H(ref)} = 3.9 V See Figures 1 and 2 | | 34 | ns |
| ^t PLH | Propagation delay time, low-to-high-level output | _ A | F | $V_{CC} = 5 \text{ V},$ $R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$ | | 45 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | 7 ^ | 「 | See Figures 1 and 2 | | 75 | ns |

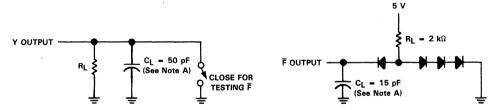
 $^{^{\}dagger}$ For SN55ALS126 at $T_{A}~=~-5\,\!\!\!/5\,^{\circ}\text{C},~V_{\mbox{H(ref)}}~=~2.5~\mbox{V}.$





NOTE: The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} \approx$ 50 t_{o

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN55ALS126 and SN75ALS126)
- Minimum Output Voltage of 3.11 V at IOH = -60 mA
- Fault-Flag Circuit Output Signals Driver **Output Fault**
- **Fault-Detection Current Limit Circuit** Minimizes Power Dissipation During a Fault Condition
- Advanced Low-Power Schottky Circuitry
- Common Enable and Common Fault Flag
- Designed to be an Improved Replacement for the MC3485

description

The SN55ALS130 and SN75ALS130 quadruple line drivers are designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at IOH = -59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN55ALS130 and SN75ALS130 are compatible with standard TTL logic and supply voltages.

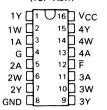
The SN55ALS130 and SN75ALS130 employ the IMPACT™ process to achieve fast switching speeds and low power dissipation. Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN55ALS130 and SN75ALS130 can drive a $50-\Omega$ load as required in the IBM GA22-6974-3 specification or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the devices are used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

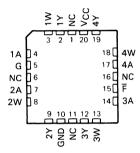
The SN55ALS130 is characterized for operation from -55°C to 125°C. The SN75ALS130 is characterized for operation from 0°C to 70°C.

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SN55ALS130 . . . J PACKAGE SN75ALS130 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55ALS130 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

FUNCTION TABLE

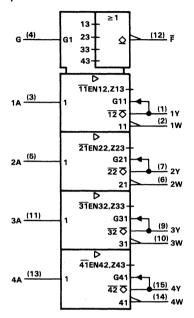
| INP | JTS | OUTPUTS | | | | |
|----------------|-----|---------|---|---|--|--|
| G [†] | Α | Y | F | w | | |
| L | Х | L | Н | Н | | |
| X | L | L | H | Н | | |
| Н | Н | н | Н | L | | |
| Н | Н | s | L | Н | | |

H = high level, L = low level, X = irrelevant, S = shorted to around

TG and F are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

SN55ALS130, SN75ALS130 QUADRUPLE LINE DRIVERS

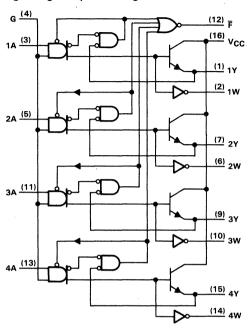
logic symbol†



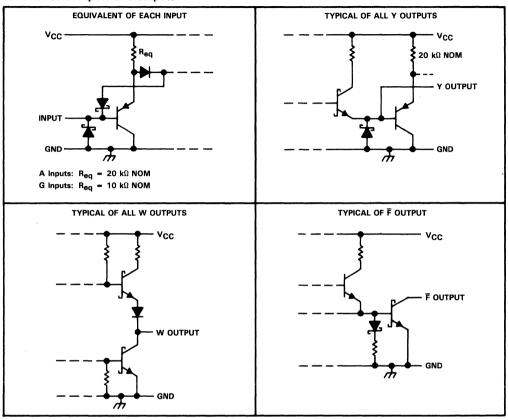
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC |
|---|
| Input voltage |
| Continuous total dissipation |
| Operating free-air temperature range: SN55ALS130 |
| SN75ALS130 |
| Storage temperature range65 °C to 150 °C |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package 300 °C |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | TA = 70°C | TA = 125°C |
|----------------|-----------------------|-----------------|--------------|--------------|
| PACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55ALS130) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75ALS130) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |

recommended operating conditions

| | SN | SN55ALS130 | | | SN75ALS130 | | |
|--|-----|---------------------|-------|-----|------------|-------|----|
| | MIN | MIN NOM MAX MIN NOM | | MAX | UNIT | | |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.95 | 4.5 | 5 | 5.95 | V |
| High-level input voltage, VIH | 2 | | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | | | 0.8 | V |
| High-level output current, IOH | | | -59.3 | | | -59.3 | mA |
| Operating free-air temperature, TA | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---------|---------------------------|-----|--|-------------------------|------|------------------|-------|
| VIK | Input clamp voltage | A,G | $V_{CC} = 4.5 \text{ V}, I_{I} = -18 \text{ mA}$ | | | - 1.5 | V |
| | | Υ | $V_{CC} = 4.5 \text{ V}, I_{OH} = -59.3 \text{ mA},$ | V _{IH} = 2 V | 3.11 | | |
| Vон | High-level output voltage | Υ | $V_{CC} = 5.25 \text{ V}, I_{OH} = -41 \text{ mA},$ | V _{IH} = 2 V | 3.9 | | V |
| | | W | $V_{CC} = 4.5 \text{ V}, I_{OH} = -400 \mu\text{A},$ | V _{IH} = 2 V | 2.5 | | |
| | | Υ | $V_{CC} = 5.5 \text{ V}, I_{OL} = -240 \mu\text{A},$ | V _{IL} = 0.8 V | | 0.15 | |
| V/ | | Y | $V_{CC} = 5.95 \text{ V}, I_{OL} = -1 \text{ mA},$ | V _{IL} = 0.8 V | | 0.15 | v |
| VOL | Low-level output voltage | F | V _{CC} = 4.5 V, I _{OL} = 8 mA, | Y at 0 V | | 0.5 | · |
| | | W | V _{CC} = 4.5 V, I _{OL} = 8 mA | | | 0.5 | |
| 1 | 044 | Υ | $V_{CC} = 4.5 \text{ V}, V_{IL} = 0,$ | $V_0 = 3.11 \text{ V}$ | | 100 | μΑ |
| IO(off) | Off-state output current | Υ | $V_{CC} = 0$, $V_{IL} = 0$, | $V_0 = 3.11 \text{ V}$ | | 200 | μΑ |
| loн | High-level output current | F | $V_{CC} = 5.95 \text{ V}, V_{OH} = 5.95 \text{ V}$ | | | 100 | μΑ |
| 1. | l | Α | V _{CC} = 4.5 V, V _{IH} = 5.5 ∀ | | | 100 | μА |
| ų | Input current | G | VCC = 4.5 V, VIH = 5.5 V | | | 400 | μΑ |
| 1 | High-level input current | Α | V _{CC} = 4.5 V, V _{IH} = 2.7 V | | | 20 | μΑ |
| ΊΗ | mign-level input current | G | VCC = 4.5 V, VIH = 2.7 V | | | 80 | μΑ |
| 1 | Low-level input current | Α | V _{CC} = 5.95 V, V _{II} = 0.4 V | | | 250 | μΑ |
| IIL | Low-level input current | G | VCC = 5.95 V, VIL = 0.4 V | | | - 1000 | μΑ |
| | | Υ, | $V_{CC} = 5.5 \text{ V}, V_{O} = 0,$ | $V_{IH} = 2.7 V$ | | – 5 | |
| 100 | Short-circuit output | W | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | | - 15 | - 100 | mA |
| los | Short-circuit output | Υ | $V_{CC} = 5.95 \text{ V}, V_{O} = 0,$ | $V_{IH} = 2.7 V$ | | – 5 | 111/4 |
| | | W | $V_{CC} = 5.95 \text{ V}, V_{O} = 0$ | | - 15 | - 110 | |
| laau | Supply current, all | | V _{CC} = 5.5 V, No load, | $V_{IH} = 2.7 V$ | | 30 | mA |
| ІССН | outputs high | | V _{CC} = 5.95 V, No load, | $V_{IH} = 2.7 V$ | | 32 | IIIA |
| loor | Supply current, | | V _{CC} = 5.5 V, No load, | V _{IL} = 0.4 V | | 45 | mA |
| ICCL | Y outputs low | | V _{CC} = 5.95 V, No load, | $V_{IL} = 0.4 V$ | | 47 | |

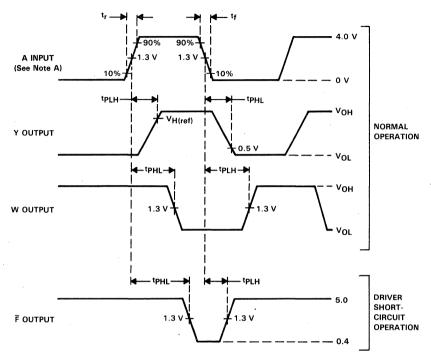
switching characteristics over recommended operating free-air temperature range

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|------|-----|---|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | | V _{CC} = 4.5 V to 5.5 V, | | 30 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | A | Υ . | $R_L = 50 \Omega$, $C_L = 50 pF$, $V_{H(ref)} = 3.11 V^{\dagger}$, Input $f = 1 MHz$, | | 28 | ns |
| tPLH tPHL | Ratio of propagation delay times | | | See Figures 1 and 2 | 0.3 | 3 | |
| [†] PLH | Propagation delay time, low-to-high-level output | A | Y | $V_{CC} = 5.25 \text{ V to } 5.95 \text{ V},$ $R_L = 90 \Omega,$ $C_L = 50 \text{ pF},$ | | 34 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output |] ^ | ľ | V _{H(ref)} = 3.9 V, Input f = 5 MHz, See Figures 1 and 2 | | 34 | ns |
| ^t PLH | Propagation delay time, low-to-high-level output | A | w | $V_{CC} = 5 \text{ V}, \qquad R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$ | | 34 | ns |
| tPHL | Propagation delay time, high-to-low-level output | A | l w | See Figures 1 and 2 | | 21 | ns |
| tPLH | Propagation delay time, low-to-high-level output | A | Ē | $V_{CC} = 5 \text{ V}, \qquad R_{L} = 2 \text{ k}\Omega,$ $C_{L} = 15 \text{ pF},$ | | 45 | ns |
| [†] PHL . | Propagation delay time, high-to-low-level output |] ^ | | See Figures 1 and 2 | | 75 | ns |

 $^{^{\}dagger}$ For SN55ALS130 at $T_{A}~=~-55\,^{o}\text{C},~V_{\mbox{H(ref)}}~=~2.5~\mbox{V}.$



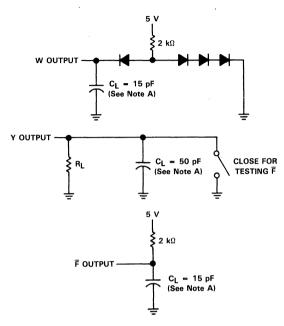
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, t_f \leq 6 ns, t_f \leq 6 ns, Z_{out} \approx 50 Ω .

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS



D3276, APRIL 1989

SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

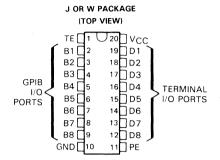
- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 56 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 550 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

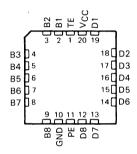
The SN55ALS160 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky designed for two-way communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passivepullup outputs when Pullup Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places these ports in the highimpedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when VCC = 0. When combined with the SN55ALS161 management bus transceiver, the device provides the complete 16-wire interface for the IEEE 488 bus.

The SN55ALS160 is characterized for operation from -55 °C to 125 °C.



FK PACKAGE (TOP VIEW)



FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

| II | INPUTS OUTPUT | | | | ŧΝ |
|----|---------------|----|----------------|--|----|
| D | TE | PE | В | | В |
| Н | Н | Н | Н | | L |
| L | Н | X | L | | Н |
| н | Х | L | Z [†] | | Х |
| Х | L | Х | Ζ [†] | | |

| Ħ | NPUT | OUTPUT | |
|---|------|--------|---|
| В | TE | PE | D |
| L | L | Х | L |
| Н | L | Х | Н |
| х | Н | X | Z |
| | | | |

H = high level, L = low level, X = irrelevant,

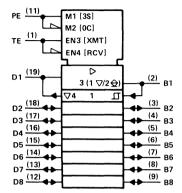
Z = high-impedance state.

[†] This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

[†]The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

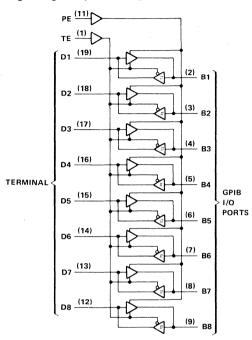


logic symbol†

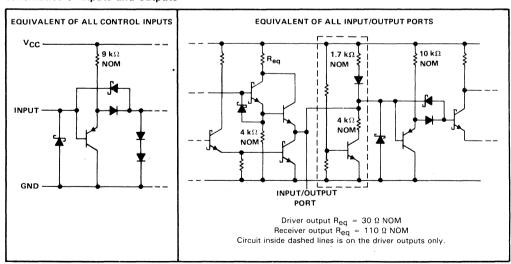


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | . 7 V |
|--|-------|
| Input voltage | 5.5 V |
| Low-level driver output current | 0 mA |
| Low-level output current | 0 mA |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): 1375 | 5 mW |
| Operating free-air temperature range | 25°C |
| Storage temperature range – 65 °C to 1 | 50°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package 3 | |
| Case temperature for 60 seconds: FK package | 60°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT | | |
|------------------------------------|---|------|-----|------|------|--|--|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V | | |
| | TE and PE at $T_A = -55$ °C to 125°C | 2 | | | | | |
| High-level input voltage, VIH | Bus and terminal at $T_A = 25$ °C or 125 °C | 2 | | | V | | |
| | Bus and terminal at $T_A = -55$ °C | 2.1 | | | | | |
| , | TE and PE at $T_A = -55$ °C to 125 °C | | | 0.8 | | | |
| Low-level input voltage, VIL | Bus and terminal at T _A = 25 °C or -55 °C | | | 0.8 | V | | |
| | Bus and terminal at T _A = 125 °C | | | 0.7 | | | |
| High level cutout surrent law | Bus ports with pullups active (V _{CC} = 5 V) | | | -5.2 | mA | | |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ | | |
| Low lovel output ourrent les | Bus ports | | | 48 | A | | |
| Low-level output current, IOL | Terminal ports | | | 16 | mA | | |
| Operating free-air temperature, TA | | - 55 | | 125 | °C | | |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------|--|-----------|----------------------------|---|------|------------------|-------|--------|
| VIK. | Input clamp voltage | | $V_{CC} = 4.75 V$, | $I_I = -18 \text{ mA}$ | - | -0.8 | - 1.5 | V |
| | Huetorosia | | $V_{CC} = 5 V$, | T _A = 25°C | 0.4 | 0.55 | | |
| V_{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | $V_{CC} = 5 V$, | T _A = 125°C | 0.25 | | | V |
| | (v + - v -) | | $V_{CC} = 5 V$, | | 0.4 | | | |
| | High-level | Terminal | $V_{CC} = 4.75 V$, | $I_{OH} = -800 \mu\text{A}$, TE at 0.8 V | 2.7 | 3.5 | | |
| Voн | output voltage | Bus | $V_{CC} = 5 V$, | $I_{OH} = -5.2 \text{ mA}$, PE and TE at 2 V | 2.5 | 3.3 | | V |
| | output voltage | bus | $V_{CC} = 4.75 V$, | $I_{OH} = -5.2 \text{ mA}$, PE and TE at 2 V | 2.2 | | | |
| | | Terminal | $V_{CC} = 4.75 V$, | $I_{OL} = 16 \text{ mA}, \text{TE at } 0.8 \text{ V}$ | | 0.3 | 0.5 | |
| VOL | Low-level | | $V_{CC} = 4.75 V,$ | I _{OL} = 48 mA, | | 0.35 | 0.5 | |
| VOL | output voltage | Bus | TE at 2 V, | $T_A = 25$ °C or 125 °C | | 0.35 | 0.5 | V |
| | output voltage | bus | $V_{CC} = 4.75 V_{r}$ | I _{OL} = 48 mA, | | 0.35 | 0.55 | |
| | • | | TE at 2 V, | $T_A = -55$ °C | | 0.35 | 0.55 | |
| 1. | Input current at | | | | | | | |
| Ц | maximum input | Terminal | $V_{CC} = 5.25 V$, | $V_I = 5.5 V$ | | 0.2 | 100 | μΑ |
| | voltage | | | | | | | |
| Luci | High-level | | $V_{CC} = 5.25 \text{ V},$ | V: - 2.7.V | | 0.1 | 20 | μΑ |
| ΊΗ | input current | Terminal, | vCC = 5.25 v, | V = 2.7 V | | 0. ! | 20 | μΑ |
| 1 | Low-level | PE, or TE | $V_{CC} = 5.25 \text{ V},$ | V: - 0 F V | | 30 | - 100 | μΑ |
| IIL | input current | | VCC = 5.25 V, | V = 0.5 V | | 30 | - 100 | μΑ |
| Viou | Voltage at bus port | | $V_{CC} = 5 V$, | $I_{I(bus)} = 0$ | 2.5 | 3.0 | 3.7 | V |
| VIO(bus) | voltage at bus port | | Driver disabled | $I_{I(bus)} = -12 \text{ mA}$ | | | - 1.5 | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | |
| | | | | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | |
| | Current into | Power on | $V_{CC} = 5 V$, | $V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$ | | | 2.5 | mA |
| II/O(bus) | bus port | 100001011 | Driver disabled | VI(bus) = 2.5 V to 5.7 V | | | -3.2 | 1117-1 |
| | bus port | | | $V_{I(bus)} = 3.7 \text{ V to 5 V}$ | 0 | | 2.5 | |
| | | | | $V_{I(bus)} = 5 V \text{ to } 5.5 V$ | 0.7 | | 2.5 | |
| | | Power off | $V_{CC} = 0$, | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | 40 | μΑ |
| loo | Short-circuit | Terminal | V _{CC} = 5.25 V | | - 15 | - 35 | - 75 | mA |
| los | output current | Bus | VCC = 5.25 V | | - 25 | - 50 | - 125 | 111/4 |
| lcc | Supply current | | $V_{CC} = 5.25 V,$ | Terminal outputs low and enabled | | 42 | 56 | mA |
| 100 | Juppiy Current | | No load | Bus outputs low and enabled | | 52 | 85 | 111/4 |
| Cu | Bus-port capacitance | | $V_{CC} = 5 V to 0$ | $V_{1/O} = 0 \text{ to } 2 \text{ V}, f = 1 \text{ MHz}$ | | 30 | | pF |

 $^{^{\}dagger}AII$ typical values are at $V_{CC}~=~5$ V, $T_{A}~=~25\,^{\circ}C.$

switching characteristics at VCC = 4.75 V, 5 V, and 5.25 V and CL = 50 pF (unless otherwise noted)

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | TA [†] | MIN | TYP‡ | MAX | UNIT | 1 |
|------------------|---------------------------|-----------------|----------------|-----------------|-----------------|-----|-------|------|------|----|
| | Propagation delay time, | | | | 25°C | | 10 | 17 | | 1 |
| ^t PLH | low- to high-level output | Terminal | Bus | C Fi 1 | Full range | | | 20 | | 1 |
| | Propagation delay time, | i erminai | Bus | See Figure 1 | 25°C | | 10 | 14 | ns | 1 |
| ^t PHL | high- to low-level output | | | | Full range | | | 16 | | |
| | Propagation delay time, | | | | 25 °C | | 8 | 15 | | 1 |
| tPLH | low- to high-level output | Bus | Terminal | C 5: 2 | Full range | | | 18 | | 1 |
| | Propagation delay time, | Bus | i erminai | See Figure 2 | 25 °C | | 8 | 15 | ns | ١ |
| tPHL | high- to low-level output | | | | Full range | | | 18 | | - |
| | Output enable time | | | | 25 °C | | 24 | 30 | | 7 |
| tPZH | to high level | | | | Full range | | | 41 | | ١ |
| | Output disable time | 1 | | | 25 °C | | 9 | 14 | | |
| tPHZ | from high level | TE | Bus | C Fi 2 | Full range | | | 16 | | |
| | Output enable time | 1 1 5 | Bus | See Figure 3 | 25 °C | | 16 | 28 | ns | |
| tPZL | to low level | | | | Full range | | | 34 | | |
| | Output disable time | | | | | | 25 °C | | 12 | 19 |
| tPLZ | from low level | | | | Full range | | | 24 | | ١ |
| | Output enable time | | | | 25 °C | | 24 | 36 | | ٦ |
| tPZH | to high level | | | | Full range | | | . 50 | | |
| | Output disable time | 1 | | } | 25 °C | | 10 | 18 | | |
| tPHZ | from high level * | TE | Terminal | C 5: 4 | Full range | | | 23 | | Ì |
| | Output enable time | 1 15 | i erminai | See Figure 4 | 25 °C | | 15 | 26 | ns | ١ |
| tPZL | to low level | | | | Full range | | | 30 | | |
| | Output disable time | 1 | | , | 25°C | | 15 | 24 | | 1 |
| tPLZ | from low level | | | | Full range | | | 31 | | 1 |
| | Output pullup | | | | 25°C | | 16 | 24 | | 1 |
| ten | enable time | Dr. | 5 . | 05 | Full range | | | 25 | | |
| | Output pullup | PE | Bus | See Figure 5 | 25 °C | | 9 | 16 | ns | 1 |
| ^t dis | disable time | | | | Full range | | | 20 | | ļ |

 $^{^{\}dagger}$ Full range is $-55\,^{\circ}$ C to $125\,^{\circ}$ C.

[‡]All typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION

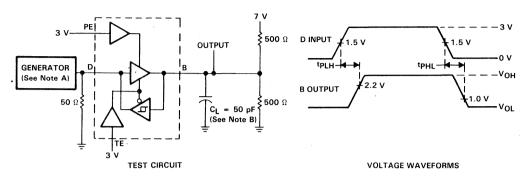


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

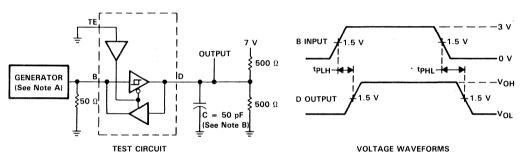


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

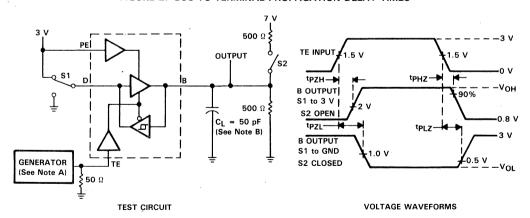


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \le 5 \text{ ns}, Z_0 = 50 \Omega.$

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

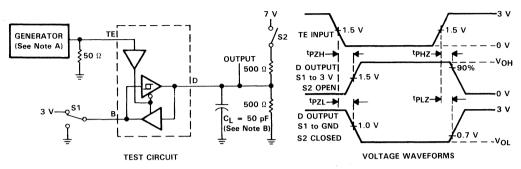


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

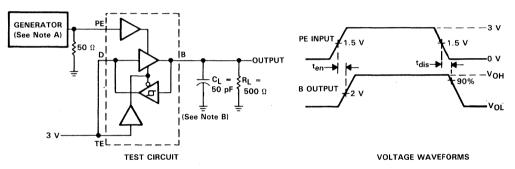


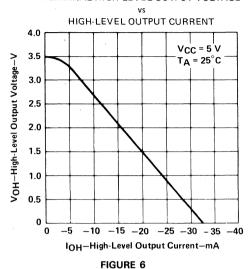
FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 5 ns, $t_O =$ 50 Ω .

B. C_I includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE



TERMINAL LOW-LEVEL OUTPUT VOLTAGE

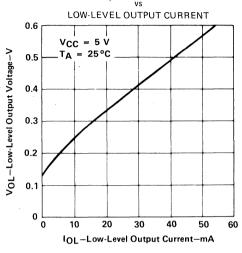


FIGURE 7

TERMINAL OUTPUT VOLTAGE

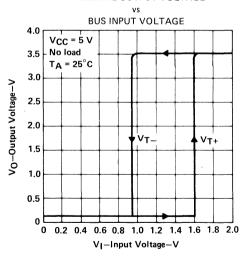
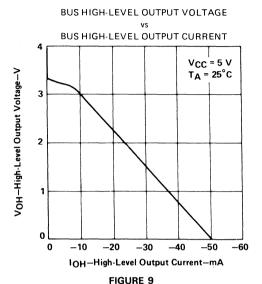
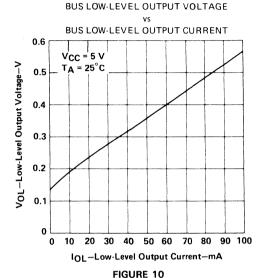


FIGURE 8

TYPICAL CHARACTERISTICS





TERMINAL INPUT VOLTAGE

VS

TERMINAL INPUT VOLTAGE

VS

VS

TERMINAL INPUT VOLTAGE

VS

TA = 5°C

No load

TA = 25°C

2

BUS OUTPUT VOLTAGE

BUS CURRENT BUS VOLTAGE V_{CC} = 5 V = 25°C 1/O(bus)-Bus Current-mA -2 -3 THE UNSHADED -5 AREA CONFORMS TO PARAGRAPH 3.5.3 OF -6 EE STANDARD 488-1978 -2 -1 VI/O(bus)-Bus Voltage-V

FIGURE 11

V_I-Input Voltage-V

1.2 1.3 1.4

0

1.0



1.5 1.6

1.7

D3277, APRIL 1989

SUITABLE FOR IEEE STANDARD 488-1978 (GPIB) APPLICATIONS[†]

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low Power Schottky Circuitry
- Low Power Dissipation . . . 59 mW Max per Channel
- Fast Propagation Times . . . 25 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 550 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN55ALS161 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN55ALS160 octal bus transceiver, the SN55ALS161 provides the complete 16-wire interface for the IEEE 488 bus. [†]

The SN55ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when

(TOP VIEW) 720 VCC TE REN 19 REN IFC [3 18 TIFC NDAC 14 17 NDAC GPIR NRFD[16 NRFD TERMINAL I/O DAVE 15 DAV I/O PORTS PORTS EOI 14 EOL ATN T8 13 ATN SRQ 19 12 SRQ GND [11 DC FK PACKAGE (TOP VIEW) S E E S NDAC 18 IFC NRFD 1 5 17 NDAC DAV 16 NRFD EOL 15 DAV ATN þв 14 EOI

J OR W PACKAGE

CHANNEL IDENTIFICATION TABLE

| NAME | IDENTITY | CLASS |
|------|--------------------|--------------|
| DC | Direction Control | Control |
| TE | Talk Enable | Control |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | Management |
| IFC | Interface Clear | ivianagement |
| EOI | End or Identify | |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | Transfer |

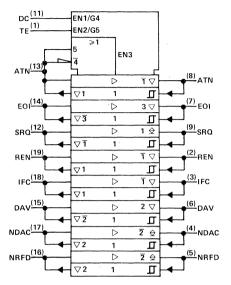
V_{CC} = 0. The drivers are designed to handle loads up to 48-mA sink current. Each receiver features p-n-p transistor inputs for high input impedance and a hysteresis of 250 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN55ALS161 is characterized for operation from -55°C to 125°C.

[†] The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

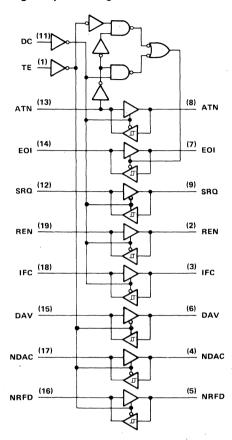


logic symbol†



- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- □ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

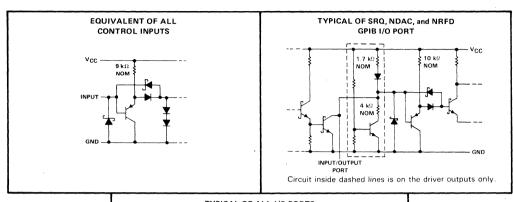
| CONTROLS | | | BUS-MANAGEMENT CHANNELS | | | | | DATA-TRANSFER CHANNELS | | | | |
|----------|----|------------------|-------------------------|--------------------|-----|-----|-----|------------------------|--------------------|------|--|--|
| DC | TE | ATN [†] | ATN [†] | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD | | |
| | | | | (Controlled by DC) | | | | | (Controlled by TE) | | | |
| Н | Н | Н | R | т | R | R | Т | т т | R | R | | |
| Н | Н | L | l " | | n | n | R | l ' | n | n. | | |
| L | L | Н | _ | R | т | т | R | R | , ₊ | т | | |
| L | L | L |] ' | n | | , | T |] | ' | • | | |
| Н | L | X | R | T | R | R | R | R | Т | Т | | |
| L | Н | X | T | R | Т | T | Т | Т | R | R | | |

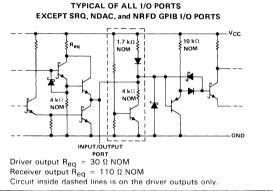
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data reception is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Low-level driver output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) 1375 mW |
| Operating free-air temperature range |
| Storage temperature range |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate to 275 mW at 125 °C at the rate of 11.0 mW/ °C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---|------|-----|------|------|
| Supply voltage, VCC | | 4.75 | 5 | 5.25 | V |
| | TE and DC at $T_A = -55$ °C to 125°C | 2 | | | |
| High-level input voltage, VIH | Bus and terminal at TA = 25 °C or 125 °C | 2 | | | V |
| | Bus and terminal at T _A = −55 °C | 2.1 | | | |
| | TE and DC at $T_A = -55$ °C to 125°C | | | 8.0 | |
| Low-level input voltage, V _{IL} | Bus and terminal at TA = 25 °C or -55 °C | | | 0.8 | V |
| | Bus and terminal at T _A = 125°C | 0 | | 0.7 | |
| High-level output current, IOH | Bus ports with pullups active (V _{CC} = 5 V) | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| Low level output ourrent lev | Bus ports | | | 48 | mA |
| Low-level output current, IOL | Terminal ports | | | 16 | IIIA |
| Operating free-air temperature, TA | | -55 | | 125 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | TES | T CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------------|---|-----------|---|---|-------------|------------------|-------|----------|
| V _{IK} | Input clamp voltage | | $V_{CC} = 4.75 \text{ V},$ | l _l = -18 mA | | -0.8 | - 1.5 | ٧ |
| | | | $V_{CC} = 5 V$, | T _A = 25°C | 0.4 | 0.55 | | |
| V_{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | $V_{CC} = 5 V$, | $T_A = 125$ °C | 0.25 | | | V |
| | | | $V_{CC} = 5 V,$ $V_{CC} = 5 V,$ | $T_A = -55$ °C | 0.4 | | | |
| | | Terminal | $V_{CC} = 4.75 \text{ V},$ | $I_{OH} = -800 \mu A$ | 2.7 | 3.5 | | |
| V _{OH} ‡ | High-level output voltage | Bus | $V_{CC} = 5 \text{ V}, \qquad I_{OH} = -5.2 \text{ mA}$ | | 2.5 | 3.3 | | V |
| | | bus | $V_{CC} = 4.75 V$, | I _{OH} = -5.2 mA | 2.2 | | | |
| | | Terminal | $V_{CC} = 4.75 V,$ | | | 0.3 | 0.5 | |
| VOL | Low-level output voltage | | $V_{CC} = 4.75 V,$ | $I_{OL} = 48 \text{ mA},$ | | 0.35 | 0.5 | v |
| VOL. | Low-level output voltage | Bus | | $T_A = 25$ °C or 125 °C | | | 0.0 | , |
| | | | $V_{CC} = 4.75 \text{ V, I}_{1}$ | $O = 48 \text{ mA}, T_A = -55 ^{\circ}\text{C}$ | | 0.35 | 0.55 | |
| l _i | Input current at Terminal | | $V_{CC} = 5.25 V_{c}$ | $V_1 = 5.5 \text{ V}$ | | 0.2 | 100 | μΑ |
| '1 | maximum input voltage | | 100 0.20 17 | | | | | μ |
| ΉΗ | High-level | Terminal | V _{CC} = 5.25 V, | $V_1 = 2.7 \text{ V}$ | | 0.1 | 20 | μΑ |
| | input current | | | -1 | | | | <u></u> |
| IIL. | Low-level | control | V _{CC} = 5.25 V, | $V_1 = 0.5 V$ | | - 30 | - 100 | μΑ |
| | input current | inputs | | | L | | | ļ |
| V _{I/O(bus)} | Voltage at bus port | | $V_{CC} = 5 V$, | I _{I(bus)} = 0 | 2.5 | 3.0 | 3.7 | v |
| 1,0,000, | | | Driver disabled | $I_{I(bus)} = -12 \text{ mA}$ | | | -1.5 | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | | | | |
| | | | | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | |
| | | Power on | V _{CC} = 5 V, | V _{I(bus)} = 2.5 V to 3.7 V | | | 2.5 | mA |
| I/O(bus) | Current into bus port | | Driver disabled | | <u> </u> | | -3.2 | |
| | | | | $V_{\text{I(bus)}} = 3.7 \text{ V to 5 V}$ | 0 | | 2.5 | |
| | | | | V _{I(bus)} = 5 V to 5.5 V | 0.7 | | 2.5 | ļ |
| | | Power off | VCC = 0 | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | 40 | μA |
| los‡ | Short-circuit Terminal | | V _{CC} = 5.25 V | | -15 | - 35 | | mA |
| | output current | Bus | | | - 25 | | -125 | <u> </u> |
| lcc | Supply, current | | | No load, TE and DC low | | 55 | 90 | mA |
| C _{i/o(bus)} | Bus-port capacitance | | $V_{CC} = 5 \text{ V to 0},$ | C 4 MILE | | 30 | | pF |
| | | | $V_{I/O} = 0$ to 2 V, | T = I MHz | L | | | L |

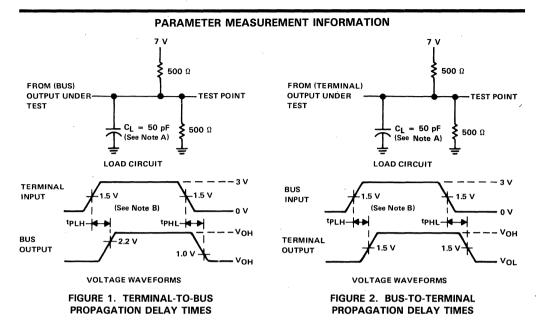
 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH and IOS apply for three-state outputs only.



switching characteristics at $V_{CC} = 4.75 \text{ V}$, 5 V, and 5.25 V and $C_L = 50 \text{ pF}$ (unless otherwise noted)

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | TA [†] | MIN | TYP [‡] | MAX | UNIT |
|------------------|---------------------------|-----------------|-------------------------------|-----------------|-----------------|-----|------------------|-----|------|
| | Propagation delay time, | | Bus | | 25°C | | 10 | 17 | |
| ^t PLH | low- to high-level output | T | (Except | C 5' 1 | Full range | | | 20 | ns |
| | Propagation delay time, | Terminal | SRQ, NDAC, | See Figure 1 | 25°C | | 10 | 14 | |
| tPHL | high- to low-level output | 1 | and NRFD) | | Full range | | | 16 | |
| | Propagation delay time | | Bus | | 25°C | | | 25 | |
| ^t PLH | low- to high-level output | Tamainal | | Can Firmura 2 | Full range | | | 30 | |
| | Propagation delay time, | Terminal | NRFD, SRQ, NDAC | See Figure 2 | 25°C | | 10 | 14 | ns |
| tPHL | high- to low-level output | 1 | NDAC | | Full range | | | 16 | ĺ |
| | Propagation delay time, | | | | 25°C | | 10 | 15 | |
| ^t PLH | low- to high-level output | D | T | S | Full range | | | 18 | |
| | Propagation delay time, | Bus | Terminal | See Figure 2 | 25°C | | 10 | 15 | ns |
| ^t PHL | high- to low-level output | | | | Full range | | | 18 | ĺ |
| | Output enable time | | | | 25°C | | 20 | 30 | |
| ^t PZH | to high level | j . | | } | Full range | | | 41 | |
| | Output disable time | | Bus (ATN, REN, IFC, and | | 25°C | | 8 | 14 | |
| ^t PHZ | from high level | TE | | 0 = 0 | Full range | | | 16 | ĺ |
| ^t PZL | Output enable time | or DC | | See Figure 3 | 25°C | | 16 | 28 | ns |
| | to low level | | DAV) | | Full range | | | 34 | ĺ |
| | Output disable time | | | ŀ | 25°C | | 10 | 19 | ĺ |
| tPLZ | from low level | j | | | Full range | | | 24 | ĺ |
| | Output enable time | | | | 25°C | | 24 | 30 | |
| ^t PZH | to high level | | | 1 | Full range | | | 48 | |
| | Output disable time | 1 | | | 25°C | | 13 | 19 | |
| tPHZ | from high level | TE | Bus | | Full range | | | 25 | ĺ |
| | Output enable time | or DC | (EOI) | See Figure 3 | 25°C | | 21 | 35 | ns |
| ^t PZL | to low level | 1 | | | Full range | | | 43 | |
| | Output disable time | 1 | | | 25°C | | 13 | 20 | ĺ |
| ^t PLZ | from low level | 1 | | Ì | Full range | | | 27 | Í |
| | Output enable time | | | | 25°C | | 24 | 36 | |
| ^t PZH | to high level | 1 | | | Full range | | | 50 | |
| | Output disable time | 1 | , | | 25°C | | 12 | 20 | |
| tPHZ | HZ from high level TE | Car Figure 1 | Full range | | | 33 | | | |
| | Output enable time | or DC | Terminal | See Figure 4 | 25°C | | 20 | 34 | ns |
| tPZL | to low level | | | | Full range | | | 41 | |
| | Output disable time | 1 | | | 25°C | | 13 | 24 | |
| ^t PLZ | LZ from low level | | Full range | | | 35 | l | | |

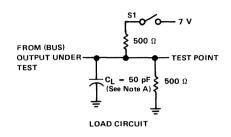
 $^{^{\}dagger}$ Full range is $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. ‡ All typical values are at V_{CC} = 5 V.

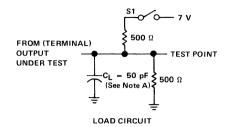


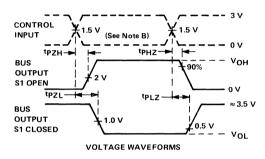
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_0 = 50 \Omega$.

PARAMETER MEASUREMENT INFORMATION







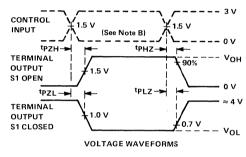


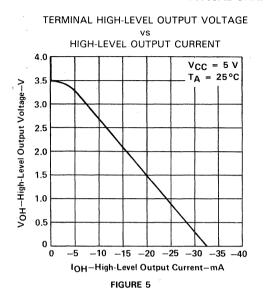
FIGURE 3. BUS ENABLE AND DISABLE TIMES

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_I includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50~\Omega$.

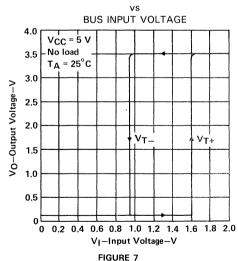
TYPICAL CHARACTERISTICS



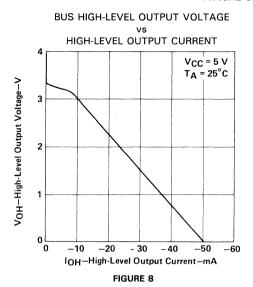
TERMINAL LOW-LEVEL OUTPUT VOLTAGE LOW-LEVEL OUTPUT CURRENT 0.6 Vcc = 5 V $T_A = 25^{\circ}C$ VOL-Low-Level Output Voltage-V 0.5 0.4 0.3 0.2 0.1 0 10 30 40 50 60 IOL-Low-Level Output Current-mA

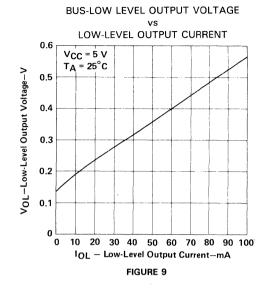
FIGURE 6

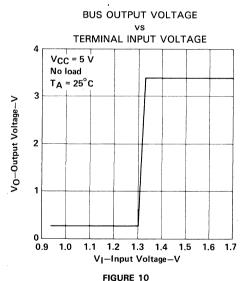
TERMINAL OUTPUT VOLTAGE

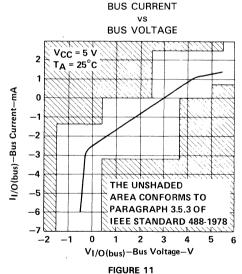


TYPICAL CHARACTERISTICS









D2904, JULY 1985-REVISED JUNE 1986

- Meets EIA Standard RS-422-A
- High-Speed, Low-Power ALS Design
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output Enable Inputs
- Improved Replacement for the AM26LS31

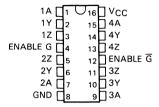
description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

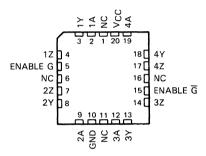
High-impedance inputs maintain input currents low, less than 1 μA for a high level and less than 100 μA for a low level. Complementary control inputs, G and \overline{G} , allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver. The SN55ALS192 is also capable of data rates in excess of 20 megabits per second and designed to operate with the SN55ALS193; however, it may be limited to a lower bit rate based on the temperature. Reference should be made to the Dissipation Rating Table and Figure 15.

The SN55ALS192 is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN75ALS192 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

SN55ALS192 . . . J PACKAGE SN75ALS192 . . . D, J, OR N PACKAGE (TOP VIEW)



SN55ASL192 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection

FUNCTION TABLE (EACH DRIVER)

| INPUT | ENA | BLES | OUT | PUTS | ; |
|-------|-----|------|-----|------|---|
| Α | G | G | Y | Z | |
| Н | Н | Х | Н | L | |
| L | Н | X | L | Н | |
| Н | × | L | н | L | |
| L | Х | L | L | Н | |
| Х | . L | Н | Z | Z | |

H = high level, L = low level,

Z = high impedance (off),

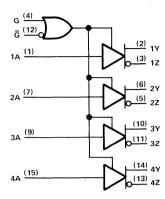
X = irrelevant



logic symbol†

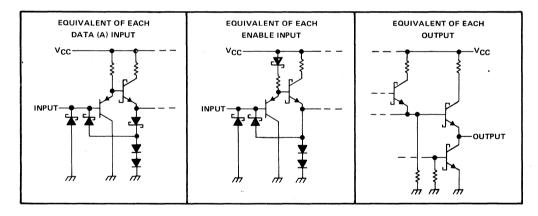
(4) ΕN (12)G (<u>2)</u> 1Y 1A (1) (3) V 1Z (6) 2Y (7) 2A (5) 2Z (10) 3A (9) 31 (11) 3Z (14)4A (15) (13)

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

schematics of inputs and outputs



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55ALS192 | SN75ALS192 | UNIT |
|--|----------------|------------|------------|-------|
| Supply voltage, V _{CC} (see Note 1) | | 7 | 7 | V |
| Input voltage, V _I | | 7 | 7 | V |
| Output off-state voltage | | 6 | 6 | V |
| | D package | | 950 | |
| Continuous total dissipation at (or below) | FK package | 1375 | | mW |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) | J package | 1375 | 1025 | 1 mvv |
| | N package | | 1150 |]` |
| Operating free-air temperature range | | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds | FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | J package | 300 | 300 |] ' |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or N package | | 260 | °C |

- NOTES: 1. All voltage values except differential output voltage VOD are with respect to network ground terminal.
 - For operation above 25 °C free-air temperature, refer to the Dissipation Rating Table. In the J package, SN55ALS192 chips
 are either alloy or silver glass mounted and SN75ALS192 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|----------------------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | |
| FK or J (SN55ALS912) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75ALS192) | 1025 mW | 8.2 mW/°C | 656 mW | |
| N | 1150 mW | 9.2 mW/°C | 736 mW | |

recommended operating conditions

| | SN | 155ALS1 | 92 | SN75ALS192 | | | UNIT |
|------------------------------------|------|---------|-----|------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNII |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | ٧ |
| High level input voltage, VIH | 2 | | | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | ٧ |
| High-level output current, IOH | | | -20 | | | - 20 | mA |
| Low-level output current, IOL | | | 20 | | | 20 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST C | ONDITIONS† | SN | 55ALS1 | 92 | SN | 75ALS | 192 | UNIT |
|-------------------|--|-----------------------------------|---------------------------|-------------------|------------------|-------|-------------------|------------------|-------|------|
| | PARAIVIETER | TEST CO | JINDITIONS . | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNIT |
| VIK | Input clamp voltage | V _{CC} = MIN, | I _I = -18 mA | | | -1.5 | | | - 1.5 | V |
| VOH | High-level output voltage | V _{CC} = MIN, | $I_{OH} = -20 \text{ mA}$ | 2.4 | | | 2.5 | | | V |
| VOL | Low-level output voltage | V _{CC} = MIN, | IOL = 20 mA | | | 0.5 | | | 0.5 | V |
| ٧o | Output voltage | $V_{CC} = MAX$, | 10 = 0 | 0 | | 6 | 0 | | 6 | V |
| VOD1 | Differential output voltage | V _{CC} = MIN, | 10 = 0 | 1.5 | | 6 | 1.5 | | 6 | V |
| Wonal | Differential output voltage | $R_{\rm I} = 100 \Omega_{\rm c}$ | See Figure 1 | ½ V _{OD} | 1 | | ½ V _{OE} |)1 | | |
| 1.0021 | | nt = 100 ss, | Jee rigule 1 | 2 | | | 2 | | | V |
| Δ VOD | Change in magnitude of differential output voltage § | | | | | ±0.2 | | | ±0.2 | v |
| Voc | Common-mode output voltage¶ | $R_L = 100 \Omega$, | See Figure 1 | | | ± 3 | | | ± 3 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | | | ±0.2 | V |
| 1- | Output gurrant with namer off |)/== O | V _O = 6 V | | | 100 | | | 100 | |
| 10 | Output current with power off | VCC = 0 | $V_0 = -0.25 \text{ V}$ | | | - 100 | | | - 100 | μΑ |
| lo- | Off-state (high-impedance | V _{CC} = MAX | $V_0 = 0.5 \text{ V}$ | | | 20 | | | - 20 | μΑ |
| loz | state) output current | ACC - MAX | $V_0 = 2.5 V$ | | | 20 | | | 20 | μΑ |
| lı | Input current at maximum input voltage | $V_{CC} = MAX,$ | V _I = 7 V | | | 0.1 | | | 0.1 | mA |
| ΉΗ | High-level input current | $V_{CC} = MAX$, | $V_{1} = 2.7 V$ | | | 20 | | | 20 | μΑ |
| կը ՜ | Low-level input current | $V_{CC} = MAX$, | $V_I = 0.4 V$ | | | -0.2 | | | -0.2 | mA |
| los | Short-circuit output current# | V _{CC} = MAX | | - 30 | | - 150 | - 30 | | - 150 | mA |
| ICC | Supply current (all drivers) | $V_{CC} = MAX,$ | All outputs disabled | | 26 | 45 | | 26 | 45 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$ (see Figure 2)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------|--|--|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | | 6 | 13 | ns |
| tPHL | Propagation delay time, high-to-low-level output | 0 20 5 61 1 62 | | 9 | 14 | ns |
| | Output-to-output skew | C _L = 30 pF, S1 and S2 open | | 3 | 6 | ns |
| tPZH | Output enable time to high level | $R_L = 75 \Omega$ | | 11 | 15 | ns |
| tPZL | Output enable time to low level | $R_L = 180 \Omega$ | | 16 | 20 | ns |
| tPHZ | Output disable time from high level | C 10 - F C1 1 C2 - 1 1 | | 8 | 15 | ns |
| tpi z | Output disable time from low level | $C_L = 10 \text{ pF}, S1 \text{ and } S2 \text{ closed}$ | | 18 | 20 | ns |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C.

 $^{^{\}S}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level

In EIA Standard RS-422A, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, VOS. *Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

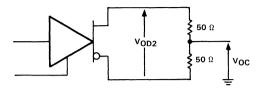
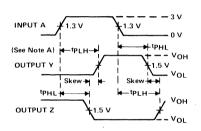
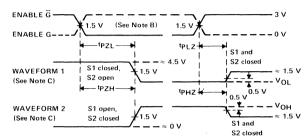


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

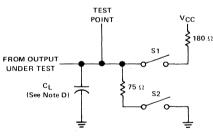




PROPAGATION DELAY TIMES AND SKEW

ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

- NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
 - B. Each enable is tested separately.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. C_L includes probe and jig capacitance.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_0 \approx 50 \Omega$, $t_f \leq 15 \text{ ns}$, and $t_f \leq 6 \text{ ns}$.

FIGURE 2. SWITCHING TIMES



TYPICAL CHARACTERISTICS Y OUTPUT VOLTAGE Y OUTPUT VOLTAGE DATA INPUT VOLTAGE DATA INPUT VOLTAGE 5.0 5.0 Vcc = 5 V No Load Outputs Enabled 4.5 Outputs Enabled $T_A = 25^{\circ}C$ No Load 4.0 4.0 Vcc = 5.5 V TA = 125°C V₀-Output Voltage-V Vo-Output Voltage-V V_{CC} = 5 V 3.5 3.5 V_{CC} = 4.5 V 3.0 3.0 25°C 2.5 2.5 o°Ċ TA = 70°C 2.0 2.0 -55°C 1.5 1.5 1.0 1.0 0.5 0.5 0 [0 [0.5 3.0 1.0 3.0 0.5 3.5 V_I-Data Input Voltage-V VI-Data Input Voltage-V FIGURE 3 FIGURE 4 Y OUTPUT VOLTAGE Y OUTPUT VOLTAGE ENABLE G INPUT VOLTAGE ENABLE G INPUT VOLTAGE 4.0 5.0 Vcc = 5.5 V V_{CC} = 5 V 4.5 3.5 $V_1 = 2 V$ V_{CC} = 5 V $R_I = 470 \Omega$ to Ground 4.0 VO-Output Voltage-V 3.0 See Note 3 Vo-Output Voltage-V V_CC = 4.5 V 3.5 Τ_Δ = 125°C 2.5 3.0 TA = 25°C 2.0 2.5 о°С TA = 70°C 2.0 1.5 - 55 °C 1.5 1.0 ν_ι = 2 ν $R_{I_{-}}$ = 470 Ω to Ground 1.0 0.5 See Note 3 0.5 $T_A = 25^{\circ}C$

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

3.0

0

1.0

1.5

FIGURE 6

V_I-Enable G Input Voltage-V

2.0

2.5

3.0



0

0

0.5

1.0

1.5

V_I-Enable G Input Voltage-V

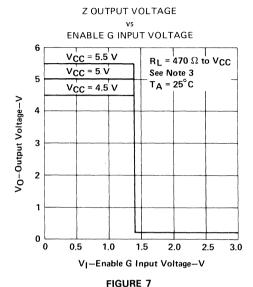
FIGURE 5

2.0

2.5

Z OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS



ENABLE G INPUT VOLTAGE 6 Vcc = 5 V $R_I = 470 \Omega$ 5 to VCC See Note 4 Vo-Output Voltage-V 4 $T_{\Delta} = 125$ °C TA = 70°C TA = 25°C 3 $T_A = 0$ °C $T_{\Delta} = -55^{\circ}C$ 2 1

riddile 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

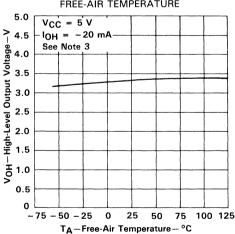


FIGURE 8
HIGH-LEVEL OUTPUT VOLTAGE

1.5

V_I-Enable G Input Voltage-V

2.0

2.5

3.0

1.0

0

0.5

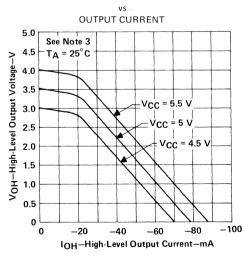


FIGURE 9

FIGURE 10

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

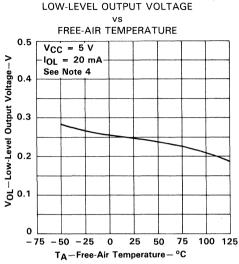
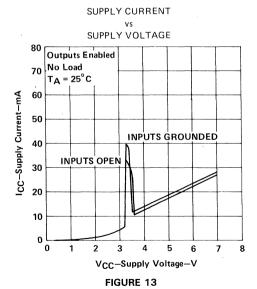


FIGURE 11



LOW-LEVEL OUTPUT VOLTAGE

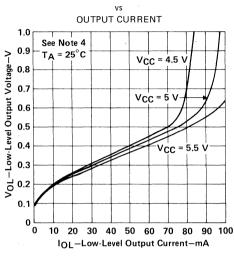
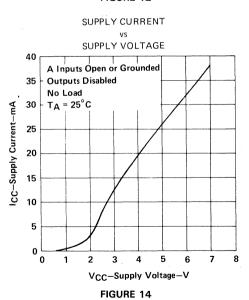


FIGURE 12



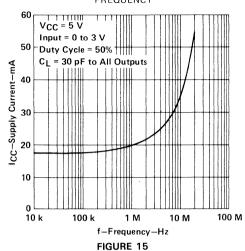
NOTE 4: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.



TYPICAL CHARACTERISTICS

SUPPLY CURRENT

FREQUENCY



D2917, OCTOBER 1985-REVISED OCTOBER 1988

- Meets EIA Standard RS-422-A
- High-Speed ALS Design
- 3-State TTL-Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Two Pairs of Drivers Independently Enabled
- Designed as a Replacement for the MC3487 with Improvements: ICC 50% Lower, Switching Speed 30% Faster, Full-Temperature-Range Version

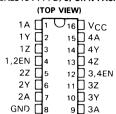
description

These quadruple complementary-output line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of EIA Standard RS-422-A and are compatible with 3-state TTL circuits. Advanced Low-Power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns and enable/disable times are typically less than 16 ns.

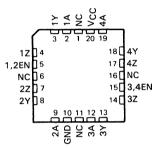
High-impedance inputs keep input currents low, less than 1 μ A for a high level and less than 100 μ A for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 10 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

The SN55ALS194 is characterized for operation from $-55\,^{\circ}$ C to $125\,^{\circ}$ C. The SN75ALS194 is characterized for operation from $0\,^{\circ}$ C to $70\,^{\circ}$ C.

SN55ALS194 . . . J PACKAGE SN75ALS194 . . . D, J, OR N PACKAGE



SN55ALS194 . . . FK PACKAGE (TOP VIEW)



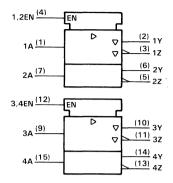
NC-No internal connection

FUNCTION TABLE (EACH DRIVER)

| INPUT | OUTPUT | OUTI | PUTS |
|--------|--------|----------------|----------------|
| ENABLE | | Y | Z |
| Н | Н | Н | L |
| L | [н | L | н - |
| X | L | High-Impedance | High-Impedance |

H = TTL high level, L = TTL low level, X = irrelevant

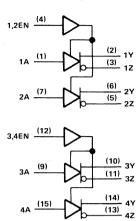
logic symbol†



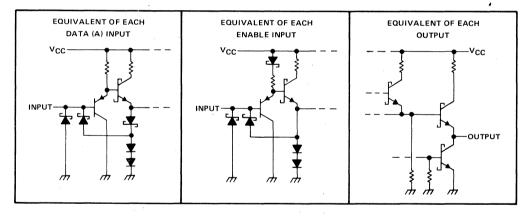
 $^{^\}dagger \text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage, V ₁ |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN55ALS19455°C to 125° |
| SN75ALS194 0°C to 70° |
| Storage temperature range65°C to 150° |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260° |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J. package |

NOTE 1; All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C | DERATING FACTOR | TA = 70°C | TA = 125°C |
|----------------|-----------------------|-----------------|--------------|--------------|
| FACRAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 ·mW/ °C | 880 mW | 275 mW |
| J (SN55ALS194) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75ALS194) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |

recommended operating conditions

| | | SN55ALS194 | | SN75ALS194 | | | UNIT | |
|---|--|------------|-----|------------|------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | ONIT |
| Supply voltage, V _{CC} | - | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V _{IH} | All inputs, T _A = 25 °C | 2 | | | 2 | | | v |
| | A inputs, $T_A = Full range$ | 2 | | | 2 | | | |
| | EN inputs, T _A = Full range | 2.1 | | | 2 | | MAX | |
| Low-level input voltage, V _{IL} | | | | 0.8 | | | 8.0 | V |
| High-level output current, IOH | | | | - 20 | | | - 20 | mA |
| Law law law at a second as a second as | $T_A = 25 ^{\circ}C$ | | | 48 | | | 48 | ^ |
| Low-level output current, IOL | T _A = Full range | | | 20 | | | 48 | mA |
| Operating free-air temperature, TA | | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST (| TEST CONDITIONS | | | TYP | MAX | UNIT |
|-------------------|--|--|--------------------|--------------------------|-------------------|-----|-------------|------------|
| V _{IK} | Input clamp voltage | V _{CC} = MIN, | I ₁ = - | 18 mA | | | -1.5 | ٧ |
| V _{OH} | High-level output voltage | V _{CC} = MIN, I _{OH} = -20 mA | | SN55ALS194 SN75ALS194 | 2.4 | | | ٧ |
| VOL | Low-level output voltage | V _{CC} = MIN, | IOL = | MAX | | | 0.5 | V |
| VO | Output voltage | 10 = 0 | | | 0 | | 6 | V |
| V _{OD1} | Differential output voltage | 10 = 0 | | | 2 | | 6 | . V |
| V _{OD2} | Differential output voltage | | | | ½ V _{OI} | 01 | | ٧ |
| Δ V _{OD} | Change in magnitude of differential output voltage ‡ | $R_{l} = 100 \Omega$ | See Figure 1 | | | | ±0.4 | ٧ |
| Voc | Common-mode output voltage | 7 | | | | | ± 3 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage [‡] | | | | | | ±0.4 | ٧ |
| 10 | Output current with power off | V _{CC} = 0 | V ₀ = | 6 V -0.25 V | | | 100 -100 | μΑ |
| loz | High-impedance state output current | V _{CC} = MAX, Output enables | V ₀ = | 2.7 V | | | 100 | μΑ |
| | riigii iripedance state output current | at 0.8 V | V ₀ = | $V_0 = 0.5 V$ | | | - 100 | |
| 4 | Input current at maximum input voltage | V _{CC} = MAX, | V _I = ! | 5.5 V | | | 100 | μΑ |
| ΊΗ | High-level input current | V _{CC} = MAX, | V _I = : | 2.7 V | | | 50 | μΑ |
| IIL | Low-level input current | V _{CC} = MAX, | V ₁ = (| 0.5 V | | | - 200 | μΑ |
| los | Short-circuit output current§ | V _{CC} = MAX, | V ₁ = 3 | 2 V | - 40 | | - 140 | mA |
| lcc | Supply current (all drivers) | V _{CC} = MAX, | All ou | tputs disabled | | 26 | 45 | mA |

switching characteristics, VCC = 5 V, TA = 25 °C

| | PARAMETER | | SN55ALS194 | | SN75ALS194 | | | UNIT | |
|------------------|--|---|------------|-----|------------|-----|-----|------|-----|
| İ | PARAMETER | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | ONT |
| tPLH | Propagation delay time, low-to-high-level output | C 15 E | | 6 | 13 | | 6 | 13 | ns |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 2 | | 9 | 14 | | 9 | 14 | ns |
| | Output-to-output skew | | | 3.5 | 6 | | 3.5 | 6 | ns |
| · | Differential-output transition time | $C_{L} = 15 pF$, | | 8 | 14 | | 8 | 14 | ns |
| tTD | Differential-output transition time | See Figure 3 | | | 14 | | | 14 | 113 |
| ^t PZH | Output enable time to high level | | | 9 | 12 | | 9 | 12 | ns |
| tPZL | Output enable time to low level | $C_L = 15 pF$, | | 12 | 20 | | 12 | 20 | ns |
| tPHZ | Output disable time from high level | See Figure 4 | | 9 | 15 | | 9 | 14 | ns |
| tPLZ | Output disable time from low level | | | 12 | 15 | | 12 | 15 | ns |

[†] All typical values are at V_{CC} = 5 V, T_A = 25 °C. $^{\ddagger}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A |
|----------------------|------------------------------------|
| v _o | V _{oa} , V _{ob} |
| V _{OD1} | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ |
| Δ V _{OD} | $ V_t - \overline{V}_t $ |
| Voc | V _{os} |
| ΔIVOCI | Vos - Vos |
| los | I _{sa} l, I _{sb} |
| In | lyal, lyhl |

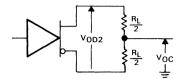


FIGURE 1. DRIVER VOD AND VOC

PARAMETER MEASUREMENT INFORMATION

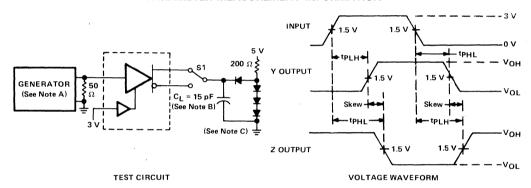


FIGURE 2. PROPAGATION DELAY TIMES

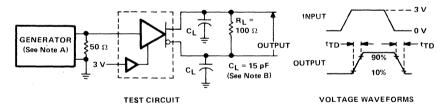
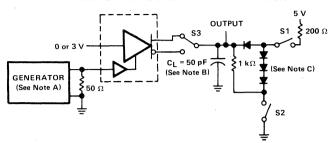


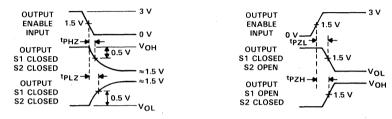
FIGURE 3. DIFFERENTIAL-OUTPUT TRANSITION TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle $\le 50\%$, $Z_0 \approx 50~\Omega$.
 - B. C_L includes probe and stray capacitance.
 - C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

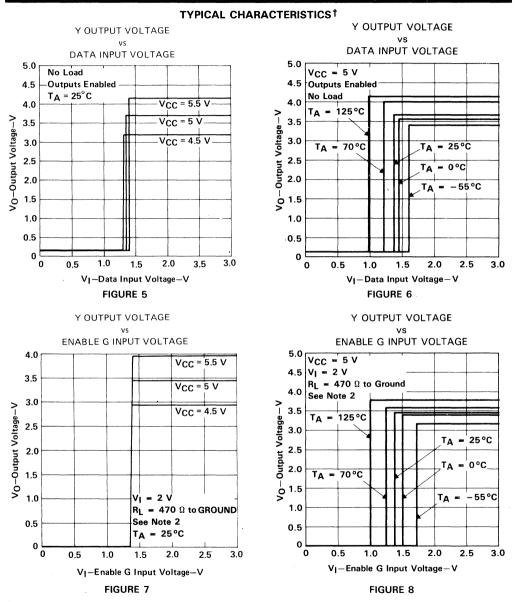


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ cycle \leq 50%, $Z_0 \approx$ 50 Ω .

- B. C_L includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

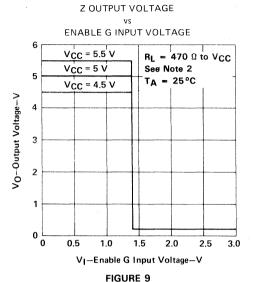
FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

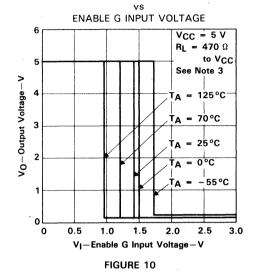


†Data for temperatures below 0°C and above 70°C are applicable to SN55ALS194 circuits only.

NOTE 2: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

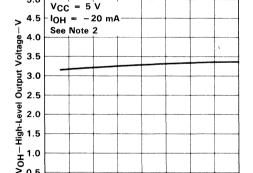






Z OUTPUT VOLTAGE

HIGH-LEVEL OUTPUT VOLTAGE FREE-AIR TEMPERATURE



HIGH-LEVEL OUTPUT VOLTAGE

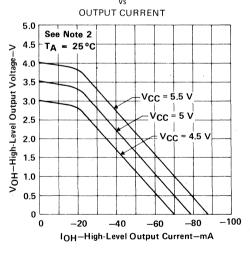


FIGURE 11

25 50

TA-Free-Air Temperature - °C

FIGURE 12

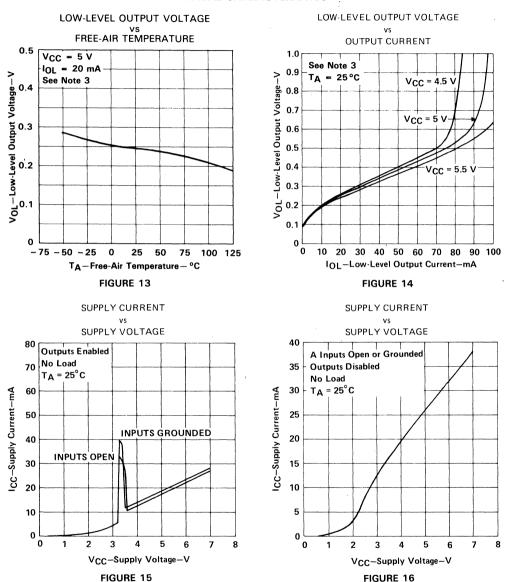
†Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only. NOTES: 2. The A input is connected to VCC during the testing of the Y outputs and to ground during the testing of the Z outputs. 3. The A input is connected to ground during the testing of the Y outputs and to VCC during the testing of the Z outputs.

75 100 125

5.0

0.5

-75 -50 -25



[†] Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTE 3: The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT



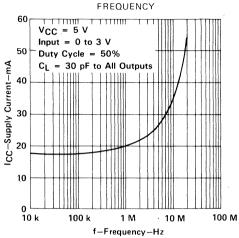


FIGURE 17

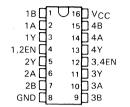
D2928, JUNE 1986-REVISED JUNE 1990

- Meets EIA Standards RS-422-A and RS-423-A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- -7 V to 7 V Common-Mode Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

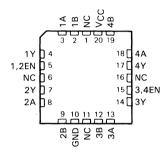
description

The SN55ALS195 and SN75ALS195 are monolithic quadruple line receivers with 3-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of EIA Standards RS-422-A and RS-423-A. The 3-state outputs permit direct connection to a busorganized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

SN55ALS195, SN75ALS195 . . . J PACKAGE (TOP VIEW)



SN55ALS195 . . . FK PACKAGE (TOP VIEW)

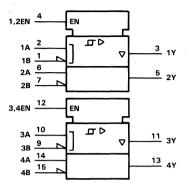


NC-No internal connection

The devices are optimized for balanced multipoint bus transmission at rates up to 20M b/s. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of \pm 200 mV over a common-mode input voltage range of \pm 7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

The SN55ALS195 is characterized for operation from $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The SN75ALS195 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

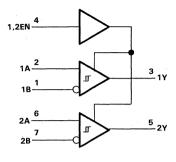
logic symbol[†].

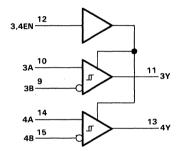


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J package.

logic diagram





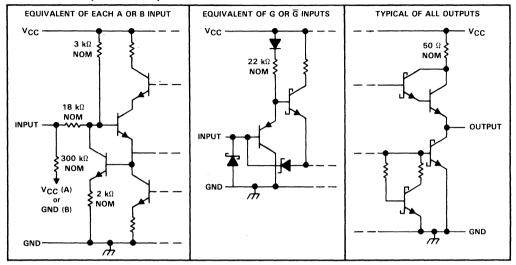
FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL INPUTS A-B | ENABLE | OUTPUT Y |
|---|--------|-------------|
| V _{ID} ≥ 0.2 V | Н | Н |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | Н | ? |
| V _{ID} ≤ -0.2 V | Н | L |
| X | L | Z |

H = high level, L = low level, X = irrelevant,

? = indeterminate, and Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage, A or B inputs, V _I |
| Differential input voltage (see Note 2) |
| Enable input voltage |
| Low-level output current 50 mA |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN55ALS195 |
| SN75ALS195 0°C to 70°C |
| Storage temperature range |
| Case temperature for 60 seconds: FK package |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300 °C |

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | TA = 125°C POWER RATING |
|----------------|---------------------------------------|---------------------------------|---------------------------|----------------------------|
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN55ALS195) | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J (SN75ALS195) | 1025 mW | 8.2 mW/°C | 656 mW | N/A |



^{2.} Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

recommended operating conditions

| | SN | SN55ALS195 | | SN75ALS195 | | | |
|--|------|------------|------|------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.5 | . 5 | 5.5 | 4.75 | . 5 | 5.25 | V |
| Common-mode input voltage, V _{IC} | | | ±7 | | | ±7 | ٧ |
| Differential input voltage, VID | | | ±12 | | | ±12 | V |
| High-level input voltage, VIH | _ 2 | | | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | V |
| High-level output current, IOH | | | -400 | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | | | 16 | mA |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST (| CONDITIONS [†] | MIN | TYP‡ | MAX | UNIT |
|------------------|-------------------------------------|--|--|---------|-------|-------|------|
| V _{T+} | Positive-going threshold voltage | | | | | 200 | mV |
| V _T _ | Negative-going threshold voltage | | | - 200 § | | | mV |
| V _{hys} | Hysteresis¶ | | | | 120 | | mV |
| VIK | Enable-input clamp voltage | V _{CC} = MIN, | I _I = -18 mA | | | -1.5 | V |
| Vон | High-level output voltage | V_{CC} MIN, $I_{OH} = -400 \mu A$, | V _{ID} = 200 mV, See Figure 1 | 2.5 | 3.6 | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = MIN$ $V_{ID} = -200 \text{ mV},$ | I _{OL} = 8 mA | | | 0.45 | V |
| VOL | Low level output voltage | See Figure 1 | I _{OL} = 16 mA | | | 0.5 | ľ |
| | High-impedance state output current | $V_{CC} = MAX,$ $V_{ID} = -3 V,$ | $V_{IL} = 0.8 \text{ V},$ $V_{O} = 2.7 \text{ V}$ | | | 20 | |
| loz | | $V_{CC} = MAX,$ $V_{IO} = 3 V,$ | V _{IL} = 0.8 V, V _O = 0.5 V | | | -20 | μΑ |
| 1. | Line input current | Other input at 0 V, | $V_{CC} = MIN, V_I = 15 V$ | | 0.7 | 1.2 | mA |
| 11 | | See Note 3 | $V_{CC} = MAX, V_I = -15 V$ | | - 1.0 | - 1.7 | |
| ۱н | High-level enable-input current | V _{CC} = MAX | V _{IH} = 2.7 V | | | 20 | μΑ |
| | | | V _{IH} = 5.25 V | | | 100 | |
| իւ | Low-level enable-input current | V _{CC} = MAX, | V _{IL} = 0.4 V | 10 | | - 100 | μA |
| | Input resistance | | | 12 | 18 | | kΩ |
| los | Short-circuit output current | $V_{CC} = MAX,$ $V_{O} = 0,$ | V _{ID} = 3 V, See Note 4 | -15 | -78 | -130 | mA |
| Icc | Supply current | $V_{CC} = MAX,$ | Outputs disabled | | 22 | 35 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

[§]The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

Hysteresis is the difference between the positive-going input threshold voltage, V_{T +}, and the negative-going input threshold voltage, V_{T -}. NOTES: 3. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

^{4.} Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|---|--------------------------------|-----------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low- to high-level output | $V_{ID} = 0 V \text{ to } 3 V$ | $C_L = 15 pF$, | | 15 | 22 | ns |
| tPHL | Propagation delay time, high- to low-level output | See Figure 2 | | | 15 | 22 | ns |
| tPZH | Output enable time to high level | C _I = 15 pF, | See Figure 3 | | 13 | 25 | |
| tPZL | Output enable time to low level | C[= 15 pr, | See Figure 3 | | 10 | 25 | ns |
| tPHZ | Output disable time from high level | C 15 = 5 | See Figure 3 | | 19 | 25 | |
| tPLZ | Output disable time from low level | CL = 15 pF, | See rigure S | | 17 | 22 | ns |

PARAMETER MEASUREMENT INFORMATION

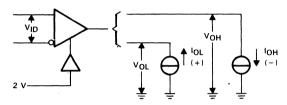
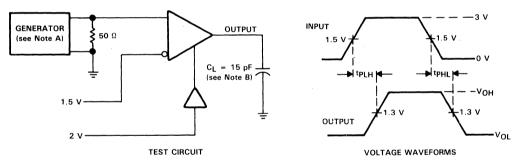


FIGURE 1. VOH, VOL

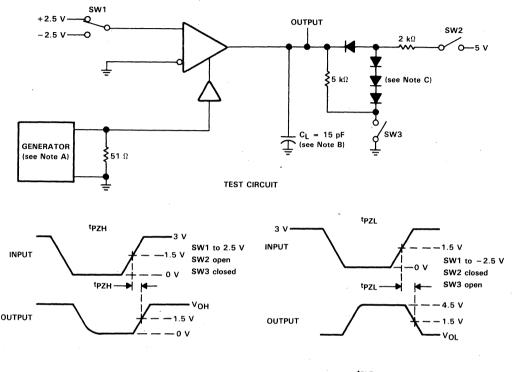


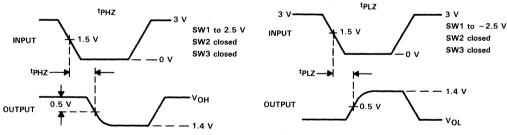
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{OUT} = 50 Ω , t_f \leq 6 ns, t_f \leq 6 ns.

B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION





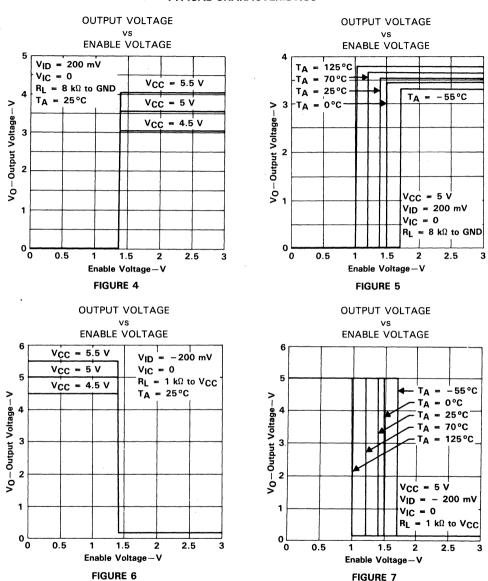
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} = 50 \Omega t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

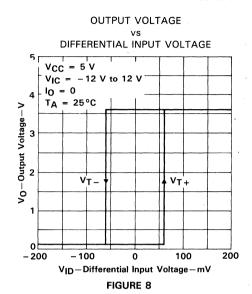
FIGURE 3. ENABLE AND DISABLE TIMES

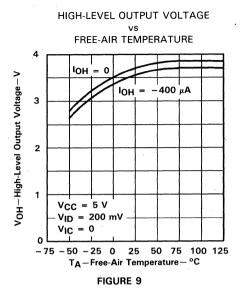


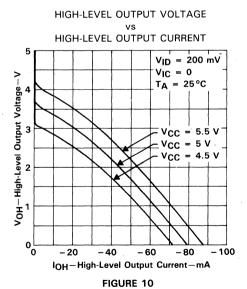


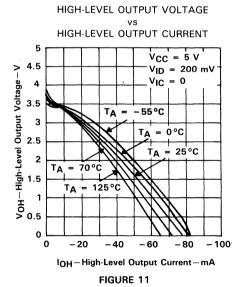
[†]Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.











[†]Data for temperatures below 0 °C and above 70 °C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.



LOW-LEVEL OUTPUT VOLTAGE

FREE-AIR TEMPERATURE 0.40 $V_{CC} = 5 V$ $V_{ID} = -200 \text{ mV}$ 0.35 Vol. - Low-Level Output Voltage - V $V_{IC} = 0$ 0.30 0.25 IO = 8 mA 0.20 0.15 $I_0 = 0$ 0.10 0.05 0

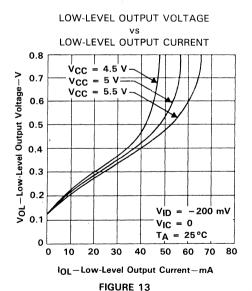
TA-Free-Air Temperature - °C

25 50 75

100 125

FIGURE 12

-75 -50 -25 0

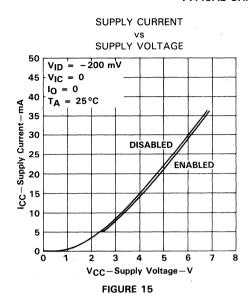


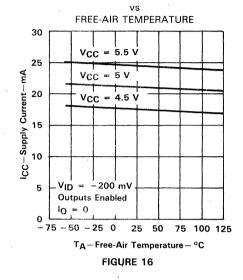
LOW-LEVEL OUTPUT VOLTAGE LOW-LEVEL OUTPUT CURRENT 0.8 VCC = 5 V $V_{ID} = -200 \text{ mA}$ > 0.7 $V_{IC} = 0$ VOL-Low-Level Output Voltage-0.6 = 70°C 0.5 125°C 0°C 0.4 -55°C 0.3 = 25°C 0.1 0 0 30 40 50 70 IOL-Low-Level Output Current-mA

FIGURE 14

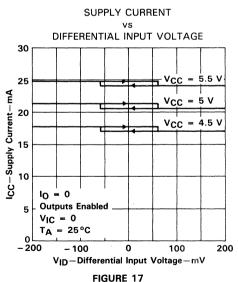
[†]Data for temperatures below 0 °C and above 70 °C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

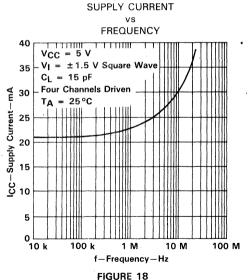






SUPPLY CURRENT

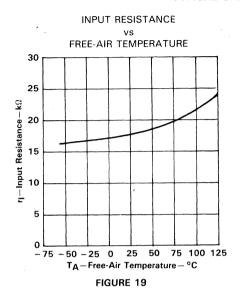


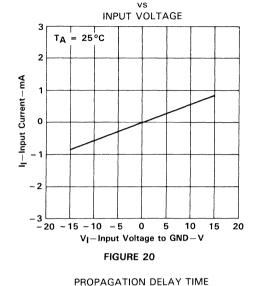


[†]Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

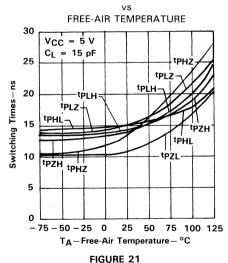
INPUT CURRENT

TYPICAL CHARACTERISTICS[†]





SWITCHING CHARACTERISTICS



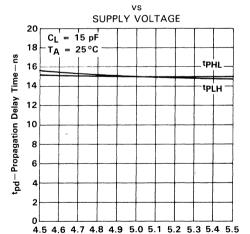


FIGURE 22

V_{CC}-Supply Voltage-V

†Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.



D3407, JANUARY 1990

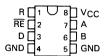
- **Bidirectional Transceiver**
- Designed for Multipoint Transmission in Noisy Environments Such as Automotive Applications
- 3-State Driver and Receiver Outputs
- **Individual Driver and Receiver Enables**
- Wide Positive and Negative Input/Output **Bus Voltage Ranges**
- Driver Output Capability. . . ± 10 mA Max
- Thermal Shutdown Protection
- **Driver Positive and Negative Current** Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for noisy environments, where a lowimpedance termination to ground is required.

The SN65076B and SN75076B combine a differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The receiver has an active-low enable. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

D OR P PACKAGE (TOP VIEW)



FUNCTION TABLE (DRIVER)

| INPUT | OUTPUTS | | | |
|-------|-------------------------------|--|--|--|
| D | A B | | | |
| Н | H L | | | |
| L | L [†] H [†] | | | |

[†]These levels assume that the open-collector outputs (A) and the open-emitter outputs (B) are connected to a pullup and pulldown resistor, respectively.

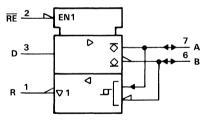
FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|---|--------------|-------------|
| V _{ID} ≥ 0.2 V | L | L |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | L | ? |
| $V_{\text{ID}} \leq -0.2 \text{ V}$ | L | н |
| × | н | z |

H = high level, L = low level, ? = indeterminate,

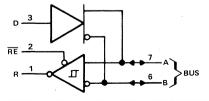
X = irrelevant, Z = high impedance (off)

logic symbol†

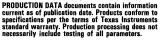


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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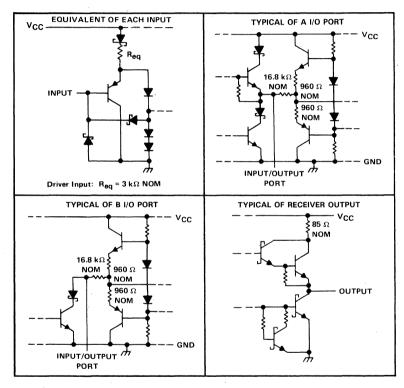




description (continued)

The driver is designed to handle loads up to 10 mA of sink and source current. The driver features positive-and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150 °C in the P package and 170 °C in the D package. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of \pm 200 mV, and a typical input hysteresis of 50 mV.

The SN65076B is characterized for operation from $-40\,^{\circ}\text{C}$ to $105\,^{\circ}\text{C}$ and the SN75076B is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.



NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 105°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | 261 mW |
| Р | 1100 mW | 8.8 mW/°C | 702 mW | 396 mW |

recommended operating conditions

| | | | М | N TYP | MAX | UNIT |
|---|--------------|--------------------|-----|-------|-------|------|
| Supply voltage, V _{CC} | | | 4.7 | 5 5 | 5.25 | V |
| Voltage at any bus terminal (separat | alv or commo | a model. Vi or Via | | | 12 | V |
| Voltage at any bus terminar (separat | ery or commo | Tillode, VI of VIC | | | - 7 | |
| High-level input voltage, VIH | | D and RE | | 2 | | V |
| Low-level input voltage, V _{IL} | | D and RE | | | 0.8 | ٧ |
| Differential input voltage, VID (see N | ote 2) | | | | ±12 | V |
| High-level output current, IOH | | Driver (A) | | | - 10 | mA |
| High-level output current, IOH | | Receiver | | | - 400 | μΑ |
| Low-level output current, I _{OL} | | Driver (B) | | | 10 | mA |
| | | Receiver | | | 8 | IIIA |
| Operating free-air temperature, TA | SN65076B | | | 10 | 105 | °C |
| | SN75076B | | | 0 | 70 | |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CO | NDITIONS | MIN | TYP [†] MAX | UNIT |
|------------------|---------------------------------|-------------------------|----------------------------|-----|----------------------|------|
| VIK | Input clamp voltage | I _I = -18 mA | | | -1.5 | V |
| Vo | Output voltage | V _I = 2 V, | I _O = 0 | 0 | 6 | V |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | 6 | V |
| V _{OD2} | Differential output voltage | See Figure 1 | | 1.5 | 5 | V |
| 1. | Output current V _I = | | V _O = 12 V | | 1 | |
| ِ ان | | V _I = 0.8 V | $\dot{V}_0 = -7 \text{ V}$ | | -0.8 | mA |
| ΊΗ | High-level input current | V _I = 2.4 V | | | 20 | μΑ |
| ΊL | Low-level input current | V _I = 0.4 V | | | - 400 | μΑ |
| | , | V ₀ = -7 V | | | -250 | |
| 1 | Chiitt | V ₀ = 0 | | | - 150 | 1 |
| los | Short-circuit output current | $V_O = V_{CC}$ | | | 250 | mA |
| | · | V _O = 12 V | | | 250 | |
| lcc | Supply current (total package) | No load | | | 30 | mA |

 $^{^{\}dagger}AII$ typical values are at VCC $\,=\,5$ V and $T_{\mbox{\scriptsize A}}\,=\,25\,^{\mbox{\scriptsize o}}C.$

driver switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------|-----------------|-----|-----|-----|------|
| ton | Differential-output turn-on time | 0 5 | | 60 | 90 | ns |
| toff | Differential-output turn-off time | See Figure 3 | | 75 | 110 | ns |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|---|---|-------------------------|-------|------------------|-----------|------|
| VTH | Differential-input high-threshold voitage | $V_0 = 2.7 V$ | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | I _O = 8 mA | -0.2‡ | | | V |
| V _{hys} | Hysteresis § | • | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _J = -18 mA | | | | -1.5 | V |
| Vон | High-level output voltage | V _{ID} = -200 mV, See Figure 2 | $I_{OH} = -400 \mu A$, | 2.7 | | | V |
| VOL | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ See Figure 2 | I _{OL} = 8 mA, | | | 0.45 | V |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4$ | V | | | ± 20 | μΑ |
| lj. | Line input current | Other input = 0 V, See Note 3 | | | | 1 -0.8 | mA |
| Iн | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| I _I L | Low-level enable-input current | V _{IL} = 0.4 V | | | | -100 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | | | -15 | | - 85 | mA |
| ICC | Supply current (total package) | No load | | | | 30 | mA |

 $^{^{\}dagger}$ AII typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

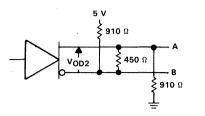
receiver switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|--|----------------------------|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = 0 \text{ to } 3$ | Ι, | | 21 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $C_L = 15 pF$, | See Figure 4 | | 23 | 35 | ns |
| tPZH | Output enable time to high level | $C_1 = 15 pF$ | See Figure 5 | | 10 | 20 | ns |
| tPZL | Output enable time to low level | CL = 15 pr, | See rigure 5 | | 12 | 20 | ns |
| tPHZ | Output disable time from high level | C. 15 F | Con Figure F | | 20 | 35 | ns |
| tPLZ | Output disable time from low level | $C_L = 15 pF,$ | See Figure 5 | | 17 | 25 | ns |

[‡]The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTE 3: This applies for both power on and power off.

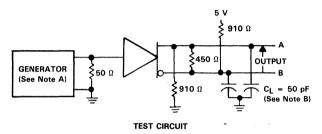
PARAMETER MEASUREMENT INFORMATION



V_{ID} V_{OH} V_{OH} V_{OH} V_{OH} V_{OH}

FIGURE 1. DRIVER VOD2

FIGURE 2. RECEIVER VOH AND VOL



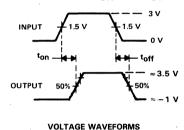
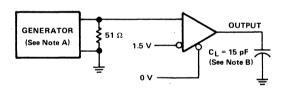
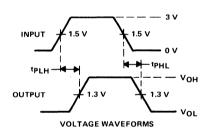


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY TIMES





TEST CIRCUIT

FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 500 kHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{Out} =$ 50 Ω .

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION **2** kΩ C_L = 15 pF **1N916 OR EQUIVALENT** (See Note B) GENERATOR **50** Ω (See Note A) **TEST CIRCUIT** - 3 V INPUT INPUT S1 to 1.5 V S1 to -1.5 V 0 V S2 open S2 closed S3 open S3 closed tPZH → | tPZL---۷он ≈4.5 V OUTPUT OUTPUT VOL - 3.A S1 to 1.5 V S1 to -1.5 V INPUT INPUT S2 closed S2 closed S3 closed S3 closed tPHZ tPLZ-۷он OUTPUT OUTPUT ≈1.3 V · VOL **VOLTAGE WAVEFORMS**

FIGURE 5. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 500 kHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} =$ 50 Ω .

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT CURRENT 5 V_{ID} = 0.2 V $T_{\Delta} = 25^{\circ}C$

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

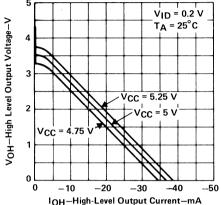


FIGURE 6

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

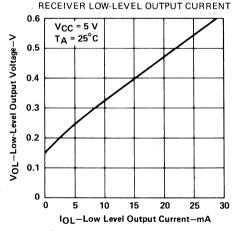


FIGURE 8

RECEIVER HIGH-LEVEL OUTPUT FREE-AIR TEMPERATURE

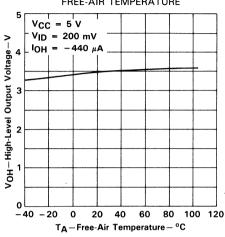


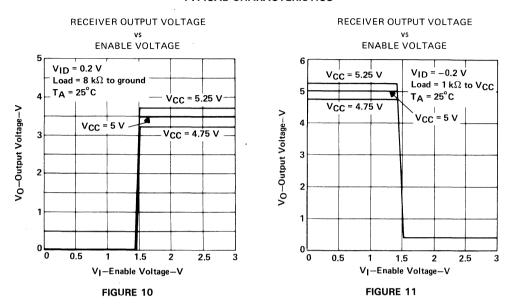
FIGURE 7

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs

FREE-AIR TEMPERATURE $V_{CC} = 5 V$ $V_{ID} = -200 \text{ mV}$ Vol -- Low-Level Output Voltage-- V 0.5 IOL = 8 mA 0.4 0.3 0.2 0.1 -40 - 2040 60 100 120 T_A-Free-Air Temperature - °C

FIGURE 9

TYPICAL CHARACTERISTICS



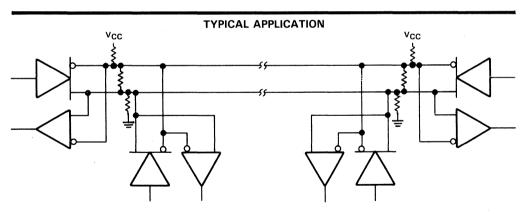


FIGURE 12. TYPICAL APPLICATION CIRCUIT

SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

D2619, JULY 1985-REVISED SEPTEMBER 1989

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

D, JG, OR P PACKAGE (TOP VIEW)



FUNCTION TABLE (DRIVER)

| INPUT | ENABLE | OUTPUTS | |
|-------|--------|---------|---|
| D | DE | Α | В |
| Н | Н | Н | L |
| L | н | L | н |
| × | L | z | Z |

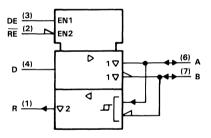
FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|----------------------------------|--------------|-------------|
| V _{ID} ≥ 0.2 V | L | н |
| -0.2 V < V _{ID} < 0.2 V | L | ? |
| V _{ID} ≤ -0.2 V | L | L |
| × | н | z |

H = high level, L = low level, ? = indeterminate,

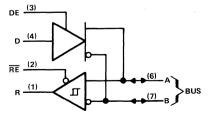
X = irrelevant, Z = high impedance (off)

logic symbol†



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Texas Instruments

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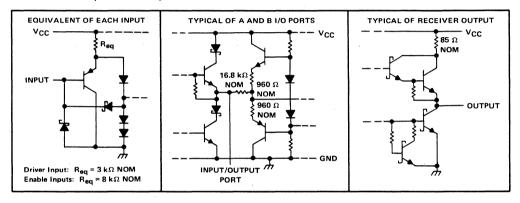
SN65176B, SN75176B DIFFERENTIAL BUS TRANSCEIVERS

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positiveand negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150 °C. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of ± 200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from -40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|---|------|
| Voltage at any bus terminal | 5 V |
| Enable input voltage | .5 V |
| Continuous total power dissipation (see Note 2) See Dissipation Rating T | able |
| Operating free-air temperature range: SN65176B | 5°C |
| SN75176B | 0°C |
| Storage temperature range65 °C to 150 | 0°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: D or P package 26 | 0°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 30 | 0°C |

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

2. In the JG package, the chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 105°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | 261 mW |
| JG | 825 mW | 6.6 mW/°C | 528 mW | 297 mW |
| Р | 1100 mW | 8.8 mW/°C | 702 mW | 396 mW |

recommended operating conditions

| | | | MII | N TYP | MAX | UNIT |
|--|--------------|--------------------|-----|-------|------|------|
| Supply voltage, V _{CC} | | | 4.7 | 5 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common mode), V _I or V _{IC} | | | | 12 | V | |
| Voltage at any bus terriman (separat | ery or commo | Thioder, VI or VIC | | | - 7 | |
| High-level input voltage, VIH | | D, DE, and RE | | 2 | | V |
| Low-level input voltage, VIL | | D, DE, and RE | | | 0.8 | V |
| Differential input voltage, VID (see N | lote 3) | | | | ± 12 | V |
| High-level output current, IOH | | Driver | | | - 60 | mA |
| High-level output current, IOH | Receiver | | | | -400 | μΑ |
| Low-level output current, I _{OL} Driver Receiver | | Driver | | | 60 | mA |
| | | | | 8 |] " | |
| Operating free-air temperature, TA | SN65176B | | -4 |) | 105 | °C |
| | SN75176B | | |) | 70 | |

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP [‡] | MAX | UNIT | |
|-------------------|---|---|--|-------------------|------------------|------------|-------|--|
| VIK | Input clamp voltage | I _I = -18 mA | | | | - 1.5 | V | |
| Vo | Output voltage | I _O = 0 | | 0 | | 6 | V | |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 6 | ٧ | |
| | | $R_L = 100 \Omega$, | See Figure 1 | ½ V _{OD} | 1 | | | |
| VOD2 | Differential output voltage | | | 2 | | | V | |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V | |
| V _{OD3} | Differential output voltage | See Note 4 | | 1.5 | | 5 | V | |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | | | | ±0.2 | V | |
| Vос | Common-mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | + 3 - 1 | V | |
| Δ V _{OC} | Change in magnitude of common-mode output voltage § | | | | | ±0.2 | ٧ | |
| 10 | Output current | Output disabled, See Note 5 | $V_0 = 12 \text{ V}$ $V_0 = -7 \text{ V}$ | | | 1 -0.8 | mA | |
| ΊΗ | High-level input current | V _I = 2.4 V | <u> </u> | 1 | | 20 | μΑ | |
| ΊL | Low-level input current | V _I = 0.4 V | | | | -400 | μΑ | |
| | · | $V_0 = -7 \text{ V}$ | | | | - 250 | | |
| | Short-circuit output current | V _O = 0 | | | | - 150 | 1.1 | |
| los | | $V_O = V_{CC}$ | | | | 250 | mA | |
| | <u> </u> | V _O = 12 V | | | | 250 | 1 | |
| | Supply current (total package) | N. t | Outputs enabled | | 42 | 55 | T | |
| ICC | | No load | Outputs disabled | T | 26 | 35 | mA mA | |

[†] The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs. [‡] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25 ^{\circ}\text{C}$.

NOTES: 4. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

driver switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|----------------------|--------------|-----|-----|-----|------|
| tDD | Differential-output delay time | $R_L = 54 \Omega$, | See Figure 3 | | 15 | 22 | ns |
| ^t TD | Differential-output transition time | | | | 20 | 30 | ns |
| tPZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 85 | 120 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 40 | 60 | ns |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | 150 | 250 | ns |
| ^t PLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | 20 | 30 | ns |

 $[\]Delta$ I/V_{OD}| and Δ |V_{OC}| are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

^{5.} This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|-------------------------------------|--|
| v _o | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | V _o | Vo |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| VOD3 | | V _t (Test Termination Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | V _{os} | V _{os} |
| Δ V _{OC} | V _{os} − V̄ _{os} | V _{os} − V̄ _{os} |
| los | Isal, Isbl | |
| lo | I _{xa} , I _{xb} | l _{ia} , l _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CON | DITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|--|----------------------------------|-------|------------------|-----------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | I _O = 8 mA | -0.2‡ | | | V |
| V _{hys} | Hysteresis § | | • | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _j = -18 mA | | | | -1.5 | V |
| Voн | High-level output voltage | V _{ID} = -200 mV, See Figure 2 | $I_{OH} = -400 \mu A$, | 2.7 | | | ٧ |
| VOL | Low-level output voltage | V _{ID} = -200 mV, See Figure 2 | I _{OL} = 8 mA, | | | 0.45 | V |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4$ | V | | | ± 20 | μΑ |
| l _i | Line input current | Other input = 0 V, See Note 6 | ' | | | 1 -0.8 | mA |
| ΊΗ | High-level enable-input current | $V_{IH} = 2.7 V$ | | | | 20 | μА |
| IIL | Low-level enable-input current | $V_{IL} = 0.4 \text{ V}$ | | | | - 100 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | | | -15 | | - 85 | mA |
| lcc | Supply current (total package) | No load | Outputs enabled Outputs disabled | | 42 26 | 55 35 | mA |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

receiver switching characteristics, VCC = 5 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = 0 \text{ to } 3 \text{ V},$ | | 21 | 35 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 6 | | 23 | 35 | ns |
| ^t PZH | Output enable time to high level | C _I = 15 pF, See Figure 7 | | 10 | 20 | ns |
| tPZL | Output enable time to low level | CL = 15 pr, See Figure 7 | | 12 | 20 | ns |
| ^t PHZ | Output disable time from high level | C _I = 15 pF, See Figure 7 | | 20 | 35 | ns |
| ^t PLZ | Output disable time from low level | C _L = 15 pF, See Figure 7 | | 17 | 25 | ns |

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

 $^{^{\}S}$ Hysteresis is the difference between the positive-going input threshold voltage, V_{T-} , and the negative-going input threshold voltage, V_{T-} . See Figure 4.

NOTE 6: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

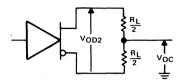


FIGURE 1. DRIVER VOD AND VOC

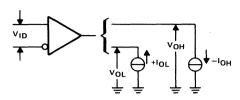
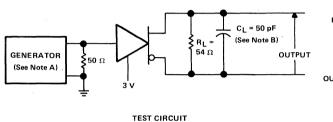


FIGURE 2. RECEIVER VOH AND VOL



OUTPUT 50% 1.5 V 1.5 V 0 V

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

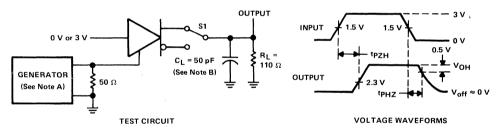


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

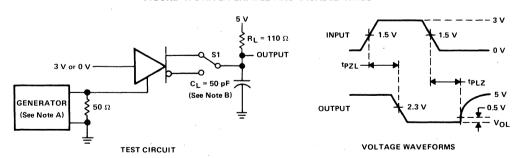


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $z_{out} =$ 50 Ω .

B. C_L includes probe and jig capacitance.



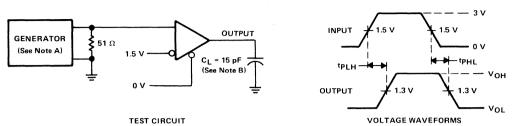


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

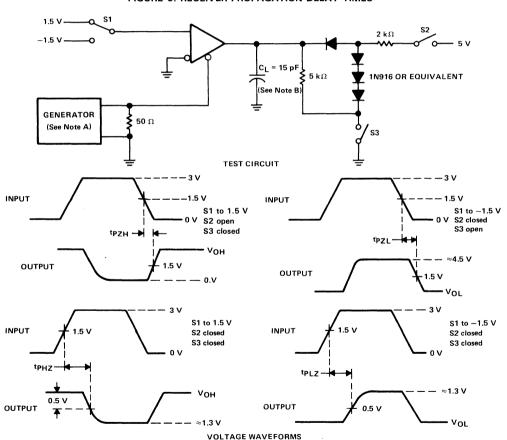


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

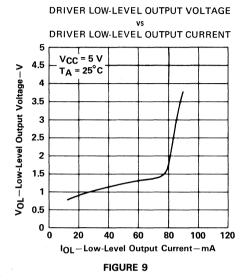
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} =$ 50 Ω .

B. C_L includes probe and jig capacitance.



DRIVER HIGH-LEVEL OUTPUT VOLTAGE DRIVER HIGH-LEVEL OUTPUT CURRENT 5 V_{CC} = 5 V VOH-High-Level Output Voltage-V 4.5 $T_A = 25^{\circ}C$ 3.5 3 2.5 2 1.5 1 0.5 0 0 -40 -60 -80 -100 IOH-High-Level Output Current-mA

FIGURE 8



DRIVER DIFFERENTIAL OUTPUT VOLTAGE

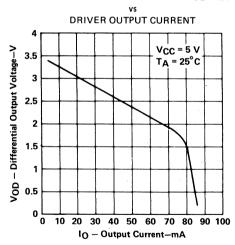


FIGURE 10

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

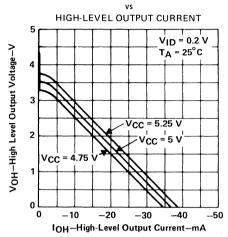


FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs

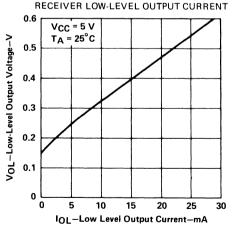


FIGURE 13

RECEIVER HIGH-LEVEL OUTPUT vs

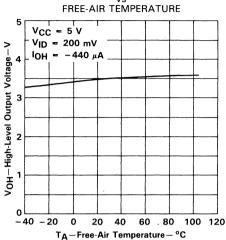


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

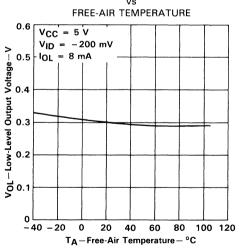
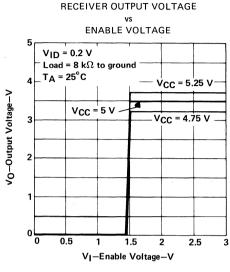


FIGURE 14



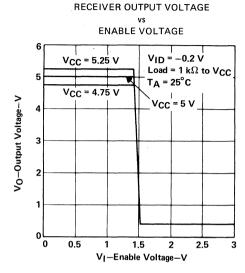


FIGURE 15

FIGURE 16

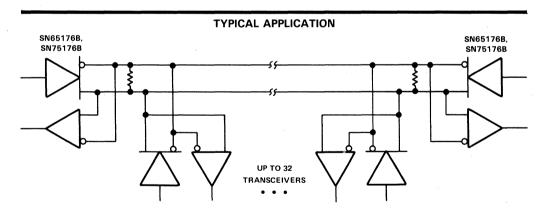


FIGURE 17. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D3042, AUGUST 1987-REVISED MAY 1990

- Meets EIA Standards RS-422A and RS-485, CCITT Recommendations V.11 and X.27, and ISO 8482:1987(E)
- Designed and Tested for Data Rates up to 35 MBaud
- SN65ALS176 Operating Temperature 40°C to 85°C
- Three Skew Limits Available:

'ALS176...10 ns 'ALS176A...7.5 ns 'ALS176B...5 ns

- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 30 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

description

The SN65ALS176 and SN75ALS176 series Differential Bus Transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

D OR P PACKAGE (TOP VIEW)

| - 1 | | ТТ | | Ì |
|-----|---|--------|---|-----------------------|
| R[| 1 | \cup | 8 |] v _{cc} |
| RE[| 2 | | 7 | V _{CC}]в |
| DE[| 3 | | 6 |] A |
| ΡŪ | 4 | | 5 | GND |
| | | | | |

FUNCTION TABLE (DRIVER)

| INPUT | ENABLE | OUTI | OUTPUTS | |
|-------|--------|------|---------|--|
| D | DE | Α | В | |
| Н | Н | Н | L | |
| L | Н | L | Н | |
| X | L | Z | Z | |

FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS A-B | ENABLE RE | OUTPUT R |
|-----------------------------------|--------------|-------------|
| V _{ID} ≥ 0.2 V | L | Н |
| - 0.2 V < V _{ID} < 0.2 V | L | ? |
| V _{ID} ≤ − 0.2 V | L | L |
| X | H | Z |

H = high level, L = low level, ? = indeterminate,

X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

| | t _{pmax} – t _{pmin} | PACKAGE | | | |
|-------|---------------------------------------|------------------------|--------------------|--|--|
| TA | ^t sk(1) [‡] | SMALL OUTLINE (D) † | PLASTIC DIP (P) | | |
| 0°C | 10 | SN75ALS176D | SN75ALS176P | | |
| to | 7.5 | SN75ALS176AD | SN75ALS176AP | | |
| 70°C | 5 | SN75ALS176BD | SN75ALS176BP | | |
| -40°C | | | | | |
| to | 10 | SN65ALS176D | SN65ALS176P | | |
| 85°C | | | | | |

† The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75ALS176DR).

† t_{Sk(1)} is the greater of 1) the difference between the maximum and

The SN65ALS176 and SN75ALS176 series combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{\rm CC} = 0$. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from -40° C to 85° C and the SN75ALS176 series is characterized for operation from 0° C to 70° C.

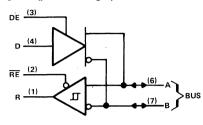


^{*} t_{Sk(1)} is the greater of 1) the difference between the maximum and minimum specified values of tp_LH of (tp_DH), and 2) the difference between the maximum and minimum specified values of tp_HL (or tp_DL). This is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device.

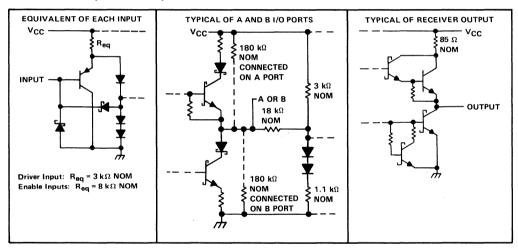
logic symbol[†]

DE (3) EN1 EN2 (6) A (7) B

logic diagram (positive logic)



schematics of inputs and outputs



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | 7 V |
|---|--------------------------------|
| Voltage at any bus terminal | – 10 V to 15 V |
| Enable input voltage | 5.5 V |
| Continuous total power dissipation | . See Dissipation Rating Table |
| Operating free-air temperature range, T _A : SN65ALS176 | 40°C to 85°C |
| SN75ALS176 Series | 0°C to 70°C |
| Storage temperature range | – 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | 520 mW |

recommended operating conditions

| | | MIN | TYP | MAX | UNIT |
|--|---------------|------|-----|-------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | ٧ |
| Voltage at any bus terminal (separately or common mode), V _I or V _{IC} | | | | 12 | v |
| | | | | -7 | v |
| High-level input voltage, VIH | D, DE, and RE | 2 | | | V |
| Low-level input voltage, V _{IL} | D, DE, and RE | | | 0.8 | V |
| Differential input voltage, V _{ID} (see Note 2) | | | | ±12 | ٧ |
| High level output ourrent leve | Driver | | | - 60 | mA |
| High-level output current, IOH | Receiver | | | - 400 | μΑ |
| Low lovel output output la | Driver | | | 60 | mA |
| Low-level output current, IOL | Receiver | | | 8 | MA |
| Operating free-air temperature, TA | SN65ALS176 | - 40 | | 85 | 00 |
| | SN75ALS176 | 0 | | 70 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CO | NDITIONS† | MIN | TYP [‡] | MAX | UNIT |
|-------------------|--|--|-----------------------|----------------------|------------------|----------|------|
| VIK | Input clamp voltage | I _I = – 18 mA | | | | - 1.5 | V |
| Vo | Output voltage | IO = 0 | | 0 | | 6 | V |
| Vop1 | Differential output voltage | I _O = 0 | | 1.5 | | 6 | V |
| | | $R_{\rm I} = 100 \Omega$ | See Figure 1 | 1/2 V _{OD1} | | | |
| VOD2 | Differential output voltage | 11[= 100 sz, | Jee rigule r | 2 | | | V |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V |
| V _{OD3} | Differential output voltage | V _{test} = - 7 V to 12 V | /, See Figure 2 | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage § | | | | | ± 0.2 | ٧ |
| Voc | Common-mode output voltage | R_L = 54 Ω or 100 Ω , See Figure 1 | | | | 3 - 1 | V |
| Δ Voc | Change in magnitude of common-mode output voltage§ | _ | | | | ± 0.2 | ٧ |
| lo | | Output disabled, | V _O = 12 V | | | 1 | |
| .0 | Output current | See Note 3 | V _O = -7 V | | | - 0.8 | mA |
| ΊН | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| l _I L | Low-level input current | V _I = 0.4 V | | | | - 400 | μΑ |
| | | V _O = ~ 6 V | SN65ALS176 | | | 050 | |
| | | V _O = -7 V | SN75ALS176 | | | -250 | |
| loo | Short-circuit output current ¶ | V _O = 0 | All | | | - 150 | |
| los | Short-circuit output current " | VO = VCC | All | | | | mA |
| | | V _O = 8 V | SN65ALS176 | | 250 | | l |
| | | V _O = 12 V | SN75ALS176 | | | | |
| | Supply ourrent | No load | Outputs enabled | | 23 | 30 | |
| ICC | Supply current | INO IOAU | Outputs disabled | | 19 | 26 | mA |

The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V and T_A = 25°C.

[§] $\Delta \mid V_{OD} \mid$ and $\Delta \mid V_{OC} \mid$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

[¶] Duration of the short circuit should not exceed one second.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

| PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|-------------------------------------|---|-----|------------------|-----|------|
| tDD | Differential output delay time | | | | 15 | ns |
| tsk(p) | Pulse skew (tDDL - tDDH) | $R_L = 54 \Omega$, $C_L = 50 pF$, See Figure 3 | | 0 | 2 | ns |
| ^t TD | Differential output transition time | | | 8 | | ns |
| ^t PZH | Output enable time to high level | $R_L = 110 \Omega$, $C_L = 50 pF$, See Figure 4 | | | 80 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, $C_L = 50 pF$, See Figure 5 | | | 30 | ns |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, $C_L = 50 pF$, See Figure 4 | | | 50 | ns |
| tpi z | Output disable time from low level | $R_I = 110 \Omega$, $C_I = 50 pF$, See Figure 5 | | | 30 | ns |

SN75ALS176, SN75ALS176A, SN75ALS176B

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|--------------------|---------------------------------------|----------|----------------------|-------------------------|--------------|------|-----|------|----|
| | | 'ALS176 | | | | 3 | 8 | 13 | |
| tDD | Differential output delay time | 'ALS176A | | | | 4 | 7 | 11.5 | ns |
| | • | 'ALS176B | $R_L = 54 \Omega$, | C _L = 50 pF, | See Figure 3 | 5 | 8 | 10 | |
| t _{sk(p)} | Pulse skew (tDDL - tDDH) | |] | | | | 0 | 2 | ns |
| tTD | Differential output transition time | | 1 | | | | 8 | | ns |
| tPZH | tPZH Output enable time to high level | | $R_L = 110 \Omega$, | C _L = 50 pF, | See Figure 4 | | 23 | 50 | ns |
| tpZL | Output enable time to low level | | $R_L = 110 \Omega$, | C _L = 50 pF, | See Figure 5 | | 14 | 20 | ns |
| tPHZ | Output disable time from high level | | $R_L = 110 \Omega$, | C _L = 50 pF, | See Figure 4 | | 20 | 35 | ns |
| t _{PLZ} | Output disable time from low level | | $R_L = 110 \Omega$, | C _L = 50 pF, | See Figure 5 | | 8 | 17 | ns |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|---|--|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| VOD1 | Vo | Vo |
| VOD2 | V _t (R _L = 100 Ω) | V _t (R _L = 54 Ω) |
| l Vods l | | V _t (Test Termination Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ \nabla_t - \overline{\nabla}_t $ |
| Voc | Vos | Vos |
| ΔIVoci | $ V_{os} - \overline{V}_{os} $ | $ V_{OS} - \overline{V}_{OS} $ |
| los | sa , sb | |
| 10 | xa , xb | l _{ia} , l _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CO | NDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|---|-----------------------------|-------|------|-------|------|
| VTH | Differential-input high-threshold voltage | V _O = 2.7 V, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | V _O = 0.5 V, | IO = 8 mA | - 0.2 | | | ٧ |
| V _{hys} | Hysteresis [§] | | | | 60 | | mV |
| VIK | Enable-input clamp voltage | I _I = - 18 mA | | | | - 1.5 | ٧ |
| Vон | High-level output voltage | V _{ID} = - 200 mV, See Figure 6 | I _{OH} = – 400 μA, | 2.7 | | | ٧ |
| VOL | Low-level output voltage | V _{ID} = - 200 mV, See Figure 6 | I _{OL} = 8 mA, | | | 0.45 | ٧ |
| loz | High-impedance-state output current | V _O = 0.4 V to 2.4 V | / | | | ±20 | μΑ |
| 1. | Line input ourrent | Other input = 0 V, | V _I = 12 V | | | 1 | A |
| 11 | Line input current | See Note 4 | V _I = 7 V | | | - 0.8 | mA |
| ΊΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μА |
| IL | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| ri | Input resistance | | | 12 | 20 | | kΩ |
| los | Short-circuit output current | V _{ID} = 200 mV, | VO = 0 | - 15 | | - 85 | mA |
| 1 | | | Outputs enabled | | 23 | 30 | |
| Icc | Supply current | No load | Outputs disabled | | 19 | 26 | mA |

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

| | PARAMETER | 7 | EST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--------------------|-------------------------------------|-------------------------|---|-----|------|-----|------|
| tpd | Propagation time | V:= 1 E V +o | 1.5 V, C _I = 15 pF, See Figure 7 | | | 25 | ns |
| t _{sk(p)} | Pulse skew (tpHL - tpLH) | VID = - 1.5 V to | 1.5 V, CL = 15 pr, See Figure 7 | | 0 | 2 | ns |
| ^t PZH | Output enable time to high level | | | | 11 | 18 | ns |
| ^t PZL | Output enable time to low level | C _I = 15 pF. | See Figure 8 | | 11 | 18 | ns |
| ^t PHZ | Output disable time from high level | - OL = 15 μι, | Gee rigure o | | | 50 | ns |
| t _{PLZ} | Output disable time from low level | Ī | | | | 30 | ns |

SN75ALS176, SN75ALS176A, SN75ALS176B

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|---|------|------|-----|------|
| | 'ALS176 'ALS176A 'ALS176B VID = -1.5 V to 1.5 V, | 'ALS176 | | 9 | 14 | 19 | |
| ^t pd | | 'ALS176A | V _{ID} = -1.5 V to 1.5 V, C _I = 15 pF, See Figure 7 | 10.5 | 14 | 18 | ns |
| | | V D = - 1.5 V to 1.5 V, CL = 15 μr, See Figure 7 | 11.5 | 13 | 16.5 | | |
| t _{sk(p)} | Pulse skew (tpHL - tpLH) |) | | | 0 | 2 | ns |
| ^t PZH | | | | | 7 | 14 | ns |
| tPZL | Output enable time to low lev | el | C _I = 15 pF, See Figure 8 | | 20 | 35 | ns |
| ^t PHZ | Output disable time from high level | | OE = 15 pr., See rigule 6 | | 20 | 35 | ns |
| ^t PLZ | Output disable time from low | level | | | 8 | 17 | ns |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

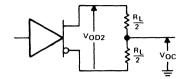


FIGURE 1. DRIVER VOD AND VOC

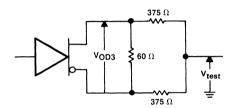
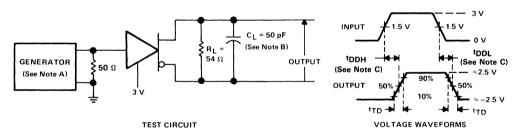


FIGURE 2. DRIVER V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{r} \leq$ 7 ns, $t_{r} \leq$ 8 ns, t_{r}

- B. CL includes probe and jig capacitance.
- C. tDD = tDDH or tDDL

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

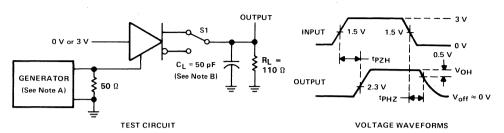


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

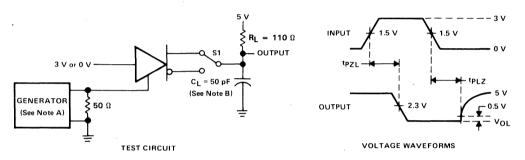


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 7 ns, $t_f \le$ 8 ns, $t_f \le$ 8 ns, $t_f \le$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, t_f

B. CL includes probe and jig capacitance.

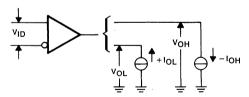


FIGURE 6. RECEIVER VOH AND VOL

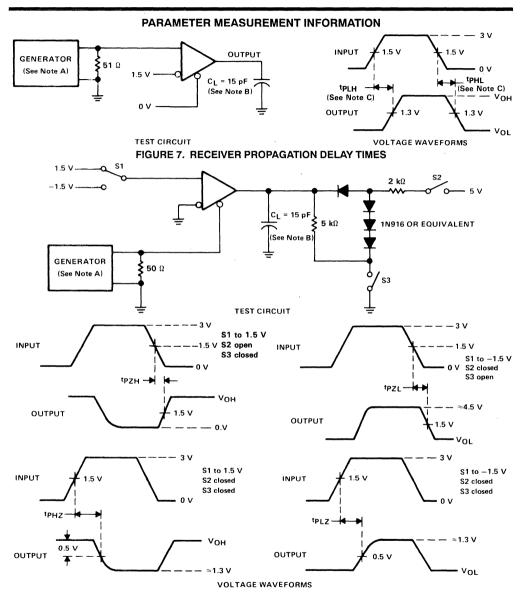


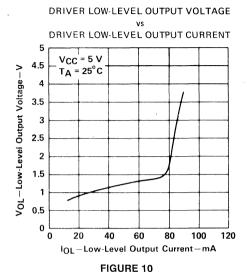
FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f
 - B. C_L includes probe and jig capacitance.
 - C. tpd = tpLH or tpHL



DRIVER HIGH-LEVEL OUTPUT VOLTAGE DRIVER HIGH-LEVEL OUTPUT CURRENT 5 VCC = 5 V VOH-High-Level Output Voltage-V 4.5 $T_A = 25^{\circ}C$ 4 3.5 3 2.5 2 1.5 1 0.5 0 -60 -80 --100 -120 IOH - High-Level Output Current - mA

FIGURE 9



DRIVER DIFFERENTIAL OUTPUT VOLTAGE

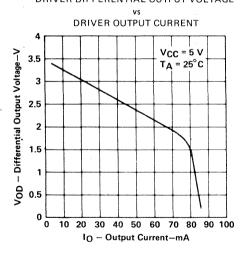
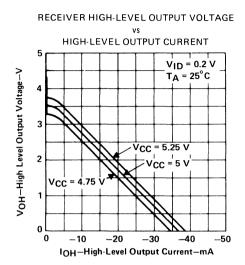


FIGURE 11

 $V_{CC} = 5 V$

TYPICAL CHARACTERISTICS



V_{ID} = 200 mV OH = -440 μA

RECEIVER HIGH-LEVEL OUTPUT vs FREE-AIR TEMPERATURE

FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

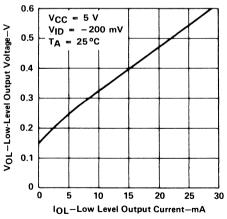


FIGURE 14

FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

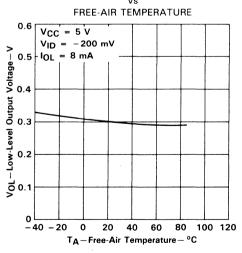
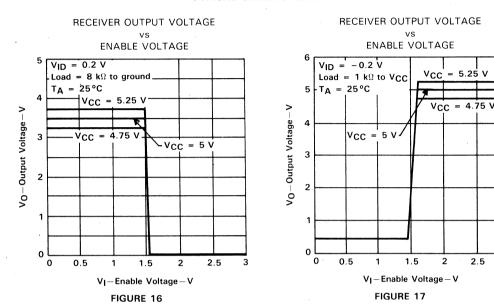


FIGURE 15



APPLICATION INFORMATION

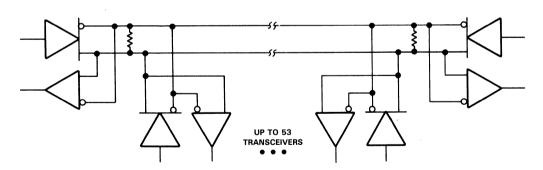


FIGURE 18. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.



D3043, AUGUST 1987 - REVISED DECEMBER 1989

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew between Devices . . . € ns Max
- Low Supply Current Requirements 30 mA Max
- Individual Driver and Receiver I/O pins with Dual V_{CC} and Dual GND
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

description

The SN65ALS180 and SN75ALS180 Differential Driver and Receiver Pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer

D OR N PACKAGE (TOP VIEW)

| NC [[| 1 | U14 | Vcc |
|-------|---|-----|-----|
| R☐ | 2 | 13 | VCC |
| RE 🗌 | 3 | 12 | Α |
| DE 🗍 | 4 | 11 | В |
| D□ | 5 | 10 | Z |
| GND 🗌 | 6 | 9 | Υ |
| GND 🗌 | 7 | 8 | NC |

NC-No internal connection

FUNCTION TABLE (DRIVER)

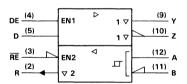
| INPUT | ENABLE | OUTPUTS | | |
|-------|--------|---------|---|--|
| D | DE | Y | Z | |
| Н | Н | Н | L | |
| L | Н | L | Н | |
| X | L | z | Z | |

FUNCTION TABLE (RECEIVER)

| ENABLE | OUTPUT |
|--------|--------|
| RE | R |
| L | Н |
| L | ? |
| L | L |
| Н | z |
| | |

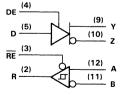
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

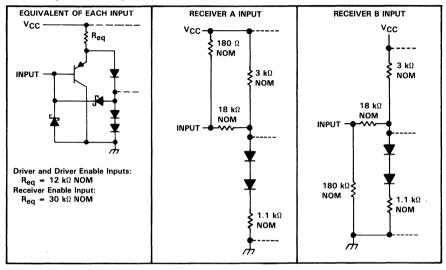


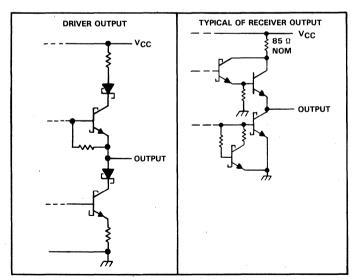
Texas Instruments

minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from -40° C to 85°C and the SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|---|
| Voltage at any bus terminal |
| Enable input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA: SN65ALS180 |
| SN75ALS180 0°C to 70°C |
| Storage temperature range –65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE T _A ≤ 25°C POWER RATING | | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING | |
|--|---------|--|---------------------------------------|---------------------------------------|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW | |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW | |

recommended operating conditions

| | | | MIN | TYP | MAX | UNIT |
|--|---------------|---------------|-----|-----|----------|-------|
| Supply voltage, VCC | | | | | 5.25 | V |
| Voltage at any bus terminal (separately or common mode), VI or VIC | | | | | 12 -7 | ٧ |
| High-level input voltage, VIH | D, DE, and RE | | 2 | | | ٧ |
| Low-level input voltage, VIL | D, DE, and RE | D, DE, and RE | | | 0.8 | ٧ |
| Differential input voltage, VID (see Note 2 | 2) | | | | ±12 | V |
| High-level output current, IOH | Driver | Driver | | | -60 | mA |
| riigii-ievei oatput carrent, iOH | Receiver | Receiver | | | -400 | μΑ |
| Low-level output current, IOI | Driver | Driver | | | 60 | mA |
| cow-level output current, IOE | Receiver | Receiver | | | 8 | III/A |
| Operating free-air temperature, TA | | SN65ALS180 | -40 | | 85 | °C |
| Operating nee-all temperature, 14 | | SN75ALS180 | 0 | | 70 | |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating freeair temperature (unless otherwise noted)

| | PARAMETER | TEST CON | OITIONS [†] | MIN | TYP‡ | MAX | UNIT |
|-------------------|---|---|-----------------------|----------------------|------|----------|-------|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| VO | Output voltage | I _O = 0 | | 0 | | 6 | V |
| VOD1 | Differential output voltage | IO = 0 | | 1.5 | | 6 | ٧ |
| | | $R_{I} = 100 \Omega$ | See Figure 1 | 1/2 V _{OD1} | | | |
| VOD2 | Differential output voltage | | | 2 | | | V |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | ٧ |
| V _{OD3} | Differential output voltage | $V_{test} = -7 V \text{ to } 12 V,$ | See Figure 2 | 1.5 | | 5 | ٧ |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | | | | ±0.2 | ٧ |
| Voc | Common-mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | +3 -1 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | ٧ |
| lo | Output current | Output disabled, | V _O = 12 V | | | 1 | mA |
| ,O | Culput current | See Note 3 | $V_0 = -7 \text{ V}$ | | | -0.8 | III/A |
| lн | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| ηL | Low-level input current | $V_1 = 0.4 \text{ V}$ | | | | -400 | μΑ |
| | | $V_0 = -7 V$ | SN75ALS180 | | | -250 | |
| | | $V_0 = -6 V$ | SN65ALS180 | | | -250 | |
| loo | Short-circuit output current¶ | $V_O = 0$ | All | | | -150 | mA |
| los | Short-circuit output current | $\Lambda^{O} = \Lambda^{CC}$ | All | | | | mA |
| | | V _O = 8 V | SN65ALS180 | | | 250 | |
| | | V _O = 12 V | SN75ALS180 | | | | |
| loo | Supply current | No load | Outputs enabled | | 23 | 30 | mA |
| ICC | Cuppiy Culterit | 140 loau | Outputs disabled | | 19 | 26 | 111/4 |

[†] The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | TEST CO | NDITIONS | MIN | TYP‡ | MAX | UNIT |
|------------------|-------------------------------------|--|--------------|-----|------|-----|------|
| t _{DD} | Differential-output delay time | | | 3 | 8 | 13 | ns |
| | Skew (tDDH-tDDL) | $R_L = 54 \Omega$, $C_L = 50 pF$, See Figure 3 | | | 1 | 6 | ns |
| tTD | Differential output transition time | See Figure S | | 3 | 8 | 13 | ns |
| t _{PZH} | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 23 | 50 | ns |
| tpzL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 19 | 24 | ns |
| ^t PHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | 8 | 13 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | 8 | 13 | ns |

[‡] All typical values are at V_{CC} = 5 V and T_A = 25°C.

^{§ ∆ |} V_{OD} | and ∆ | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

 $[\]P$ Duration of the short circuit should not exceed one second.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--|--|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | Vo | Vo |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test Termination Measurement 2) |
| V _{test} | | V _{tst} |
| Δ V _{OD} | $ V_t - \widetilde{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | V _{os} | V _{os} |
| Δ V _{OC} | $\mid V_{OS} - \overline{V}_{OS} \mid$ | $\mid V_{OS} - \overrightarrow{V}_{OS} \mid$ |
| los | I _{sa} , I _{sb} | |
| 10 | I _{xa} , I _{xb} | lia, lib |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CO | ONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|--|-------------------------|-------|------|------|-------|
| VTH | Differential-input high-threshold voltage | V _O = 2.7 V, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_{O} = 0.5 V$, | $I_O = 8 \text{ mA}$ | -0.2‡ | | | ٧ |
| V _{hys} | Hysteresis [§] | | | | 60 | | mV |
| VIK | Enable-input clamp voltage | $I_{\parallel} = -18 \text{ mA}$ | | | | -1.5 | V |
| V _{OH} | High-level output voltage | V _{ID} = 200 mV, See Figure 6 | $I_{OH} = -400 \mu A$ | 2.7 | | | ٧ |
| V _{OL} | Low-level output voltage | V _{ID} = -200 mV, See Figure 6 | I _{OL} = 8 mA, | | | 0.45 | ٧ |
| loz | High-impedance-state output current | $V_O = 0.4 \text{ V to } 2.4 \text{ V}$ | γ | | | ±20 | μΑ |
| 1. | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA |
| 11 | Line input current | See Note 4 | $V_I = -7 V$ | | | -0.8 | 111/5 |
| ΊΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| IIL | Low-level enable-input current | V _{IL} = 0.4 V | | | | -100 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | $V_{ID} = 200 \text{ mV},$ | V _O = 0 | -15 | | -85 | mA |
| laa | Cupply ourrent | No load | Outputs enabled | | 23 | 30 | mA |
| lcc | Supply current | No load | Outputs disabled | | 19 | 26 | 11174 |

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|--|--|---------------|-----|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | O F: 7 | 9 | 14 | 19 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ $C_{I} = 15 \text{ pF}$ | See Figure 7, | 9 | 14 | 19 | ns |
| | Skew (tpLH - tpHL) | OL = 13 bi | | | 2 | 6 | ns |
| ^t PZH | Output enable time to high level | | | | 7 | 1.4 | ns |
| tPZL - | Output enable time to low level | C _I = 15 pF, | See Figure 8 | | 7 | 14 | ns |
| tPHZ | Output disable time from high level | OL = 13 pr, | See rigule o | | 20 | 35 | ns |
| †PLZ | Output disable time from low level | | | | 8 | 17 | ns |

 $[\]dagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

PARAMETER MEASUREMENT INFORMATION

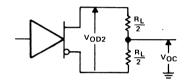


FIGURE 1. DRIVER VOD AND VOC

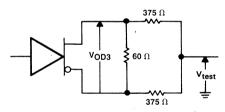


FIGURE 2. DRIVER VOD3

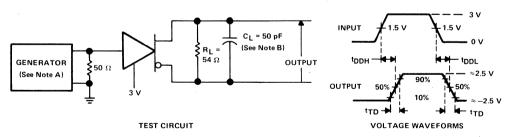


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{T} \leq$ 6 ns, $t_{T} \leq$ 6 ns, $Z_{out} = 50 \Omega$.

B. CL includes probe and jig capacitance.



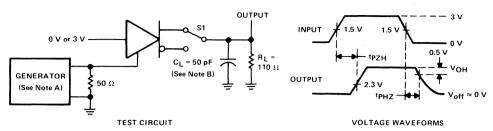


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

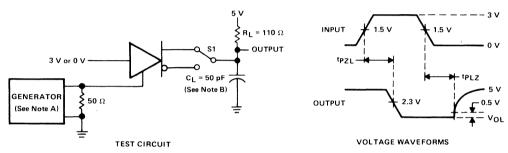


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_{out} = 50 Ω .

B. C_L includes probe and jig capacitance.

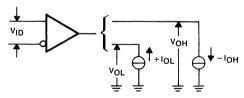


FIGURE 6. RECEIVER VOH AND VOL

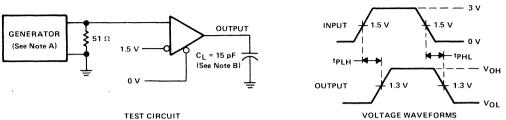


FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

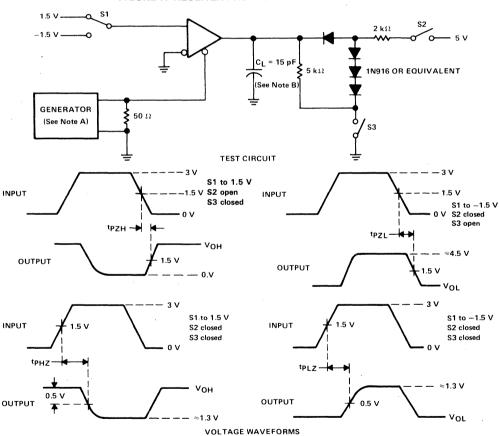


FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

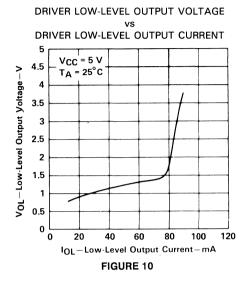
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{f} \leq$ 7 ns, $t_{f} \leq$ 8 ns, $t_{f} \leq$ 8 ns, $t_{f} \leq$ 9 ns, t_{f}

B. CL includes probe and jig capacitance.

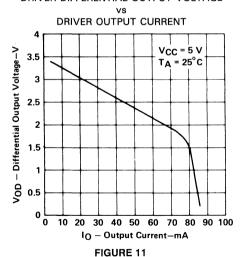


DRIVER HIGH-LEVEL OUTPUT VOLTAGE vs DRIVER HIGH-LEVEL OUTPUT CURRENT V_{CC} = 5 V VOH -- High-Level Output Voltage -- V 4.5 $T_A = 25^{\circ}C$ 4 3.5 3 2.5 2 1.5 1 0.5 0 -20 -40 -60 -80 -100 -120 IOH-High-Level Output Current-mA

FIGURE 9



DRIVER DIFFERENTIAL OUTPUT VOLTAGE



RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

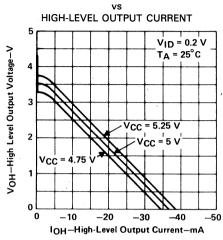


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

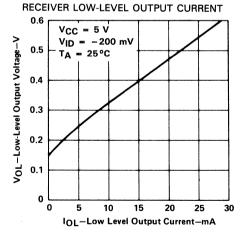


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT



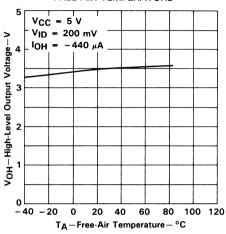


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

FREE-AIR TEMPERATURE

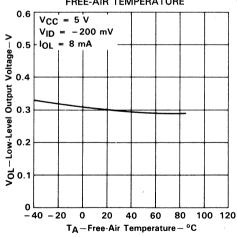
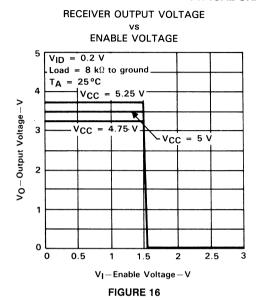


FIGURE 15



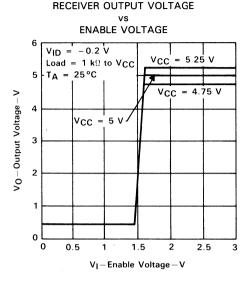
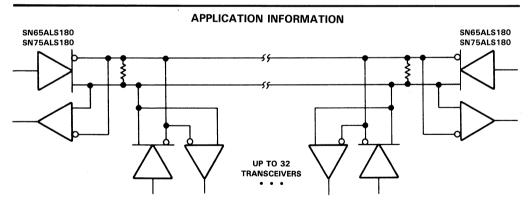


FIGURE 17



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18. TYPICAL APPLICATION CIRCUIT



SN65C185, SN75C185 LOW-POWER MULTIPLE DRIVERS AND RECEIVERS

D3325, AUGUST 1989 ~ REVISED JULY 1990

- Meets Standard EIA-232-D (Revision of RS-232-C)
- Single Chip With Easy Interface Between **UART and Serial Port Connector**
- Less than 8-mW Power Consumption
- Wide Driver Supply Voltage . . . 4.5 V to 13.2 V
- **Driver Output Slew Rate Limited to** 30 V/us Max
- Receiver Input Hysteresis ... 800 mV Typ
- **Push-Pull Receiver Outputs**
- On-Chip Receiver 1-us Noise Filter
- ESD Protection Exceeds 1000 V Per MIL-STD-883C, Method 3015

description

The SN65C185 and SN75C185 are low-power BIMOS devices containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The SN65C185 and SN75C185 will typically replace one SN75188 and two SN75189 devices. These devices have been designed to conform to Standards ANSI/EIA-232-D-1986, which supersedes RS-232-C. The three drivers and five receivers of the SN65C185 and SN75C185 are similar to those of the SN75C188 quadruple drivers and SN75C189A quadruple receivers. respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/us and the receivers have filters that reject input noise pulses that are shorter than 1 us. Both these features eliminate the need for external components.

The SN65C185 and SN75C185 have been designed using low-power techniques in a BI-MOS technology. In most applications the receivers contained in these devices will interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C185 and SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

(TOP VIEW) ا ∏ مم∨ J20 \ V_{CC} 19 RY1 RA2 □3 18 RY2 RA3 🛚 4 17 RY3 DY1 [15] 16 DA1 DY2 ∏6 15 DA2 14 RY4

13 DA3

12 RY5

11 T GND

RA4 7

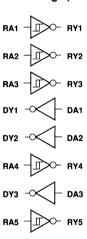
DY3 | 8

RA5 ∏9

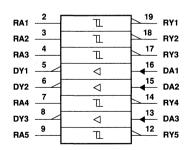
V SS 🗌 10

DW OR N PACKAGE

logic diagram (positive logic)



logic symbol[†]



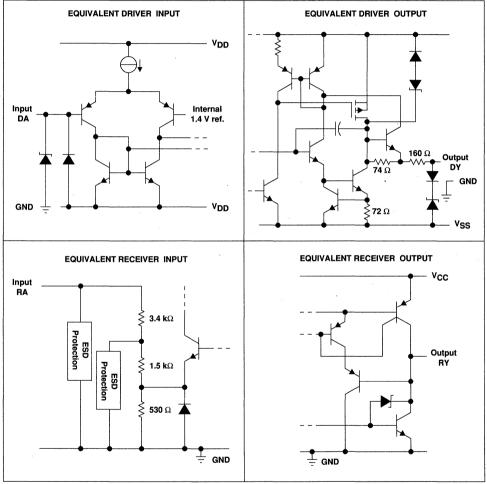
[†]This symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-122.



description (continued)

The SN65C185 is characterized for operation from -40°C to 85°C. The SN75C185 is characterized for operation from 0°C to 70°C.

equivalent schematics of inputs and outputs



SN65C185, SN75C185 LOW-POWER MULTIPLE DRIVERS AND RECEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{DD} (see Note 1) | |
|--|--|
| Supply voltage, V _{SS} | |
| Supply voltage, V _{CC} | 7 V |
| Input voltage range, Driver | V _{SS} to V _{DD} |
| Receiver | |
| Output voltage range, Driver | V _{SS} – 6 V to V _{DD} + 6 V |
| Receiver | $-0.3 \text{ V to V}_{CC} + 0.3 \text{ V}$ |
| Continuous total dissipation | . See Dissipation Rating Table |
| Operating free-air temperature range, TA: SN65C185 | 40°C to 85°C |
| SN75C185 | 0°C to 70°C |
| Storage temperature range | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | |

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 585 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|----------|-----------------|------|-----------------|-------|
| Supply voltage, V _{DD} | | 4.5 | 12 | 13.2 | V |
| Supply voltage, V _{SS} | | - 4.5 | - 12 | - 13.2 | V |
| Supply voltage, V _{CC} | | 4.5 | 5 | 6 | V |
| Input voltage, V _I (see Note 2) | Driver | V _{SS} | + 2 | V _{DD} | V |
| | Receiver | - 25 | | 25 | V |
| High-level input voltage, VIH | Driver | 2 | | | V |
| Low-level input voltage, VIL | Driver | | | 0.8 | \ \ \ |
| High-level output current, IOH | Receiver | | | -1 | mA |
| Low-level output current, IOL | Heceiver | | | 3.2 | mA |
| Operating free-air temperature, T _A | SN65C185 | - 40 | | 85 | °C |
| perating free-air temperature, 1A | SN75C185 | C | | 70 | 1 |

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

SN65C185, SN75C185 LOW-POWER MULTIPLE DRIVERS AND RECEIVERS

SUPPLY CURRENTS

| | PARAMETER | TEST (| TEST CONDITIONS | | | MAX | UNIT |
|-----|-------------------------------------|----------------------------|---|--|---------|-------|------|
| Inn | Supply current from V _{DD} | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | 115 | 200 | μА |
| IDD | Зарру санентноги УДД | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | 115 | 200 | μΑ |
| loo | Supply current from V _{SS} | No load, | $V_{DD} = 5 V$, $V_{SS} = -5 V$ | | − 115 ° | - 200 | μА |
| ISS | Supply content nom vSS | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | - 115 | - 200 | μΛ |
| lcc | Supply current from V _{CC} | No load, | $V_{DD} = 5 V$, $V_{SS} = -5 V$ | | | 750 | μΑ |
| 100 | Supply carrent non vee | All inputs at 0 or 5 V | $V_{DD} = 12 V$, $V_{SS} = -12 V$ | | | 750 | μΛ |

DRIVER SECTION

driver electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

| | PARAMETER | TEST CO | ONDITIONS | MIN | TYP [†] | MAX | UNIT |
|--------------------|-----------------------------|--|------------------------------------|-------|------------------|--------|------|
| VOH | High-level output voltage | $V_{IL} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega,$ | $V_{DD} = 5 V$, $V_{SS} = -5 V$ | 4 | . 4.5 | | v |
| TOH | riigir iever output voitage | See Figure 1 | $V_{DD} = 12 V$, $V_{SS} = -12 V$ | 10 | 10.8 | | • |
| V _{OL} | Low-level output voltage | $V_{IH} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega,$ | $V_{DD} = 5 V$, $V_{SS} = -5 V$ | | - 4.4 | - 4 | V |
| VOL | (see Note 2) | See Figure 1 | $V_{DD} = 12 V$, $V_{SS} = -12 V$ | | -10.7 | - 10 | |
| ΙΗ | High-level input current | V _I = 5 V, See Figure : | 2 | | | 1 | μΑ |
| I _{IL} | Low-level input current | V _I = 0, See Figure : | 2 | | | - 1 | μΑ |
| I _{OS(H)} | High-level short circuit | $V_1 = 0.8 V$, $V_0 = 0 \text{or} V$ | $V_O = V_{SS}$ | - 4.5 | - 12 | - 19.5 | mA |
| 10S(H) | output current (see Note 3) | See Figure 1 | | - 4.5 | - 12 | - 13.3 | "" |
| loous | Low-level short circuit | $V_1 = 2 V$, $V_0 = 0 \text{ or } V$ | $V_O = V_{DD}$, | 4.5 | 12 | 19.5 | mA |
| los(L) | output current (see Note 3) | See Figure 1 | | 4.5 | 12 | 13.3 | 111/ |
| r_ | Output resistance | $V_{DD} = V_{SS} = V_{CC} = 0$ | $V_{O} = -2 V \text{ to } 2 V,$ | 300 | 400 | | Ω |
| ro | Output resistance | See Note 4 | | 300 | 400 | | 52 |

[†]All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

3. Not more than one output should be shorted at one time.

4. Test conditions are those specified by EIA-232-D.

driver switching characteristics, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10%, T_A = 25°C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|------|-----|-----|------|
| * | Propagation delay time, | | | 1.2 | 3 | |
| ^t PLH | low-to-high-level output (see Note 5) | | | 1.2 | 3 | μs |
| + | Propagation delay time, | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 15 pF$, | | 2.5 | 3.5 | |
| ^t PHL | high-to-low-level output (see Note 5) | See Figure 3 | | 2.5 | 3.5 | μs |
| tTLH | Transition time, low-to-high-level output | | 0.53 | 2 | 3.2 | μs |
| tTHL | Transition time, high-to-low-level output | | 0.53 | 2 | 3.2 | μs |
| tTLH | Transition time, low-to-high-level output (see Note 6) | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 2500 pF$, | | 1.0 | 3 | μs |
| tTHL | Transition time, high-to-low-level output (see Note 6) | See Figure 3 | | 1.0 | 3 | μs |
| SR | Output slew rate (see Note 6) | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 15 pF$, | 4 | 10 | 30 | V/vo |
| | Output siew rate (see Note 6) | See Figure 3 | - | 10 | 30 | V/µs |

NOTES: 5. tpHI and tpI H include the additional time due to on-chip slew rate and is measured at the 50% points.

6. Measured between 3-V and -3-V points of output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

RECEIVER SECTION

receiver electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = -12V, V_{CC} = 5 V ± 10% (unless otherwise noted)

| | PARAMETER | TEST C | ONDITIONS | MIN | TYP [†] | MAX | UNIT |
|--------------------|--|--------------------------------------|-----------------------------|--------|------------------|-------|------|
| V _{T+} | Positive-going threshold voltage | See Figure 5 | | 1.6 | 2.1 | 2.55 | ٧ |
| V _T _ | Negative-going threshold voltage | See Figure 5 | | 0.65 | 1 | 1.25 | ٧ |
| V _{hys} | Input hysteresis (see Note 7) | | | 600 | 1000 | | mV |
| | | $V_1 = 0.75 \text{ V}, I_{OH} = -20$ | μA, See Figure 5 and Note 8 | 3.5 | | | |
| Va Llia | High-level output voltage | $V_1 = 0.75 V$, | V _{CC} = 4.5 V | 2.8 | 4.4 | | v |
| VOH | riigii-level output voltage | I _{OH} = -1 mA, | V _{CC} = 5 V | 3.8 | 4.9 | | ľ |
| | | See Figure 5 | V _{CC} = 5.5 V | 4.3 | 5.4 | | |
| VOL | Low-level output voltage | $V_1 = 3 V$, $I_{OL} = 3.2 r$ | nA, See Figure 5 | | 0.17 | 0.4 | V |
| l | High lovel input ourrent | V _I = 3 V | | 0.43 | 0.55 | 1 | mA |
| ΊΗ | High-level input current | V _I = 25 V | | 3.6 | 4.6 | 8.3 | IIIA |
| 1 | Low-level input current | V _I = -3 V | | - 0.43 | - 0.55 | - 1 | m 1 |
| ۱۱L | Low-level input current | V _I = -25 V | | - 3.6 | - 5.0 | - 8.3 | mA |
| I _{OS(H)} | Short-circuit output current at high-level | $V_{I} = 0.75, V_{O} = 0,$ | See Figure 4 | | - 8 | - 15 | mA |
| l _{OS(L)} | Short-circuit output current at low-level | $V_I = V_{CC}, V_O = V_{CC},$ | See Figure 4 | | 13 | 25 | μΑ |

 † All typical values are at $T_A = 25^{\circ}$ C.

NOTES: 7. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

8. If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs will remain in the high state.

receiver switching characteristics, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10%, T_A = 25°C (unless otherwise noted)

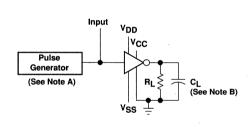
| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------------|---|---------------------|-----------------|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | _ | | 3 | 4 | μs |
| tPHL | Propagation delay time, high-to-low-level output | $R_L = 5 k\Omega$, | $C_L = 50 pF$, | | 3 | 4 | μs |
| tTLH | Transition time, low-to-high-level output | See Figure 6 | | | 300 | 450 | ns |
| tTHL | Transition time, high-to-low-level output | | | | 100 | 300 | ns |
| | Pulse duration of longest pulse rejected as noise | $R_L = 5 k\Omega$, | $C_L = 50 pF$, | | | 4 | |
| ^t w(N) | (see Note 9) | See Figure 6 | | ' | | 4 | μs |

NOTE 9: The intent of this specification is that any input pulse of less than 1 μs will have no effect on the output, and any pulse duration of greater than 4 μs will cause the output to change state twice. Reaction to a pulse duration between 1 μs and 4 μs is uncertain.

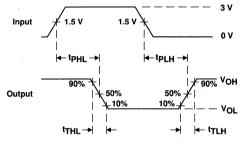
$$\begin{array}{c} V_{DD} \\ V_{CC} \\ V_{I} \\ \hline \end{array} \begin{array}{c} V_{CC} \\ V_{O} \\ \hline \end{array} \begin{array}{c} V_{CS} \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array} \begin{array}{c}$$

Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, I_{OS(H)}, and I_{OS(L)}

Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



(a) DRIVER TEST CIRCUIT



(b) DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, PRR = 20 kHz, $Z_0 = 50 \Omega$, $t_r = t_f < 50 ns$. B. CL includes probe and jig capacitance.

Figure 3. Driver Propagation and Transition Times

Figure 4. Receiver Test Circuit for I_{OS}(H) and I_{OS}(L)

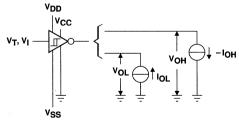
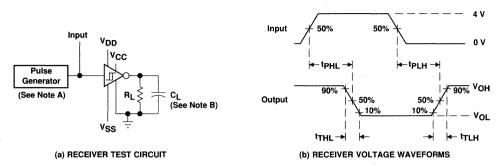


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, PRR = 20 kHz, $Z_0 = 50 \Omega$, $t_f = t_f < 50 ns$. B. C_1 includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

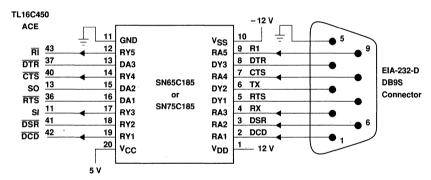


Figure 7. Typical Connection

SN65C188, SN75C188 QUADRUPLE LOW-POWER LINE DRIVER

D3075, JANUARY 1988-REVISED MAY 1990

- BiMOS Technology With TTL and CMOS Compatibility
- Meets Standard EIA-232-D (Revision of RS-232-C)
- Very Low Quiescent Current: 95 μA Typ
 VCC+ = ±12 V
- Current-Limited Output: 10 mA Typ
- CMOS- and TTL-Compatible Inputs
- On-Chip Slew Rate Limited to 30 V/μs max
- Flexible Supply Voltage Range
- Characterized at V_{CC} ± of ± 4.5 V and ± 15 V
- Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88
- ESD Protection Exceeds 2000 V Per MIL-Std-883C Method 3015

(TOP VIEW) VCC - 1 1 14 VCC + 1A 2 13 4B 1Y 3 12 4A 2A 4 11 4Y 2B 5 10 3B 2Y 6 9 3A

D. DB. OR N PACKAGE

FUNCTION TABLES DRIVER 1 DRIVERS 2 THRU 4

A Y

GND [

| ļ | Α | В | Υ |
|---|---|---|---|
| | Н | Н | L |
| | L | X | н |
| | Х | L | н |

□3Y

H = High Level L = Low Level X = Don't Care

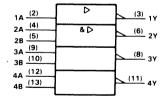
description

The SN65C188 and SN75C188 are monolithic, low-power, quadruple line drivers that interface data terminal equipment with data communications equipment. These devices are designed to conform to Standard ANSI/EIA-232-D-1986, which supercedes RS-232-C.

An external diode in series with each supply-voltage terminal is needed to protect the SN65C188 and SN75C188 under certain fault conditions to comply with EIA-232-D (refer to Application Information).

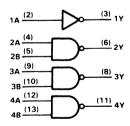
The SN65C188 is characterized for operation from $-40\,^{\circ}$ C to 85 $^{\circ}$ C. The SN75C188 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

logic symbol†



 $^\dagger \text{This}$ symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



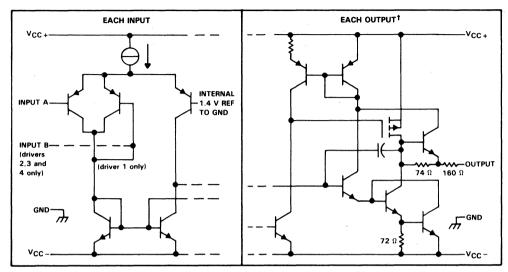
positive logic $Y = \overline{A} \text{ (driver 1)}$ $Y = \overline{AB} \text{ or } \overline{A} + \overline{B} \text{ (drivers 2 thru 4)}$

s contain information
Products conform to
I Texas
of Texas Instruments
of processing does not
all parameters.

INSTRUMENTS

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schematics of inputs and outputs



[†]All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC+ (see Note 1) 15 V |
|--|
| Supply voltage, VCC - (see Note 1) |
| Input voltage range, V _I V _{CC} – to V _{CC} + |
| Output voltage range, VO |
| Continuous total power dissipation |
| Operating free-air temperature range, TA: SN65C18840°C to 85°C |
| SN75C188 |
| Storage temperature range |
| Lead temperature 1, 6 mm (1/16 in.) from case for 10 seconds |

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| DB | 525 mW | 4.2 mW/°C | 273 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | N | IIN I | NOM | MAX | UNIT |
|--|----------|-----|---------|-----|-------------------|------|
| | | 4.5 | 12 | 15 | V | |
| Supply voltage, V _{CC} – | | | 1.5 | -12 | - 15 | V. |
| Input voltage, V _I | | Vo | C - + 2 | | V _{CC} + | V |
| High-level input voltage, VIH | | | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | | | 0.8 | ٧ |
| Operating free-air temperature, TA | SN65C188 | - | 40 | | 85 | °C |
| | SN75C188 | | 0 | | 70 | -0 |

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = -12 V (unless otherwise noted)

| | PARAMETER | TEST CONDITIO | NS | MIN | TYP [†] | MAX | UNIT |
|--------|--|--|--|------|------------------|--------|------|
| | Himb lavel systems well- | $V_{II} = 0.8 \text{ V}, R_{I} = 3 \text{ k}\Omega$ | $V_{CC+} = 5 V,$ $V_{CC-} = -5 V$ | 4 | | | V |
| Vон | High-level output voltage | VIL = 0.8 V, RL = 3 KM | $V_{CC+} = 12 V,$ $V_{CC-} = -12 V$ | 10 | | | ľ |
| Voi | Low-level output voltage | $V_{IH} = 2 \text{ V}, R_{L} = 3 \text{ k}\Omega$ | $V_{CC+} = 5 V$, $V_{CC-} = -5 V$ | | | -4 | V |
| VOL | (see Note 2) | THE EXTENSION OF THE STATE OF T | $V_{CC+} = 12 V,$ $V_{CC-} = -12 V$ | | | -10 | |
| ΊΗ | High-level input current | V _I = 5 V | | | | 10 | μΑ |
| IIL. | Low-level input current | V _I = 0 | | | | - 10 | μΑ |
| los(H) | Short-circuit output current at high level ‡ | $V_{I} = 0.8 \text{ V}, V_{O} = 0 \text{ or } V_{CC} -$ | | -5.5 | - 10 | - 19.5 | mA |
| los(L) | Short-circuit output current at low level [‡] | $V_1 = 2 V, V_0 = 0 \text{ or } V_{CC+}$ | | 5.5 | 10 | 19.5 | mA |
| ro | Output resistance, power off | $V_{CC+} = 0, V_{CC-} = 0, V_{O} =$ | -2 V to 2 V | 300 | | | Ω |
| laa. | Supply gurrent from Vac | $V_{CC+} = 5 \text{ V}, V_{CC-} = -5 \text{ V},$ No load | All inputs at 2 V or 0.8 V | | 90 | 160 | |
| ICC+ | Supply current from V _{CC+} | $V_{CC+} = 12 \text{ V}, V_{CC-} = -12 \text{ V}$ No load | All inputs at 2 V or 0.8 V | | 95 | 160 | μΑ |
| laa | Supply ourrant from Vac | $V_{CC+} = 5 \text{ V, } V_{CC-} = -5 \text{V,}$ No load | All inputs at 2 V or 0.8 V | | - 90 | - 160 | μА |
| ICC- | Supply current from V _{CC} – | $V_{CC+} = 12 \text{ V}, V_{CC-} = -12 \text{ V}$ No load | All inputs at 2 V or 0.8 V | | -95 | -160 | μΑ |

 $^{^{\}dagger}All$ typical values are at T_A = 25 °C. $^{\ddagger}Not$ more than one output should be shorted at one time.

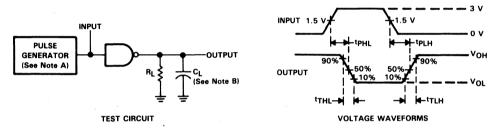
NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if a -4 V is a maximum, the typical value is a more negative voltage.

switching characteristics, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -12 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|--|------|-----|-----|------|
| tPLH | Propagation delay time, low-to-high level output [†] | $R_L = 3 k\Omega$, $C_L = 15 pF$, | | | 3 | μS |
| tPHL | Propagation delay time, high-to-low level output [†] | See Figure 1 | | | 3.5 | μS |
| tTLH | Transition time, low-to-high-level output [‡] | | 0.53 | | 3.2 | μS |
| tTHL | Transition time, high-to-low-level output [‡] | | 0.53 | | 3.2 | μs |
| [†] TLH | Transition time, low-to-high-level output§ | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 2500 pF$, | | 1.5 | 3 | μS |
| ^t THL | Transition time, high-to-low-level output§ | See Figure 1 | | 1.5 | 3 | μS |
| SR | Output slew rate [§] | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 15 pF$ | 6 | 15 | 30 | V/μs |

[†]Measured at the 50% level.

PARAMETER MEASUREMENT INFORMATION



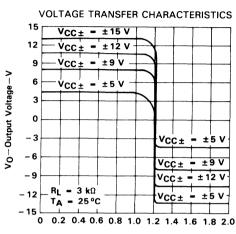
NOTES: A. The pulse generator has the following characteristics: $t_W = 25~\mu s$, PRR = 20~kHz, $Z_O = 50~\Omega$, $t_T = t_f \le 50~ns$. B. C_L includes probe and jig capacitance.

FIGURE 1. PROPAGATION AND TRANSITION TIMES

[‡]Measured between the 10% and 90% points on the output waveform.

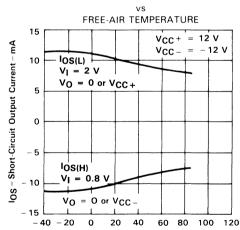
[§]Measured between the 3 V and −3 V points on the output waveform (EIA-232-D conditions), all unused inputs tied either high or low.

TYPICAL CHARACTERISTICS



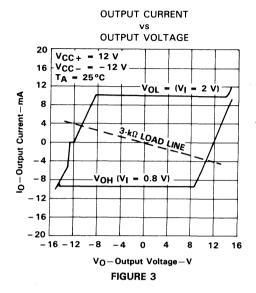
V_I-Input Voltage – V FIGURE 2

SHORT-CIRCUIT OUTPUT CURRENT

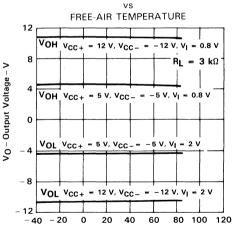


TA - Free-Air Temperature - °C

FIGURE 4



OUTPUT VOLTAGE



T_A – Free-Air Temperature – °C
FIGURE 5

TYPICAL CHARACTERISTICS

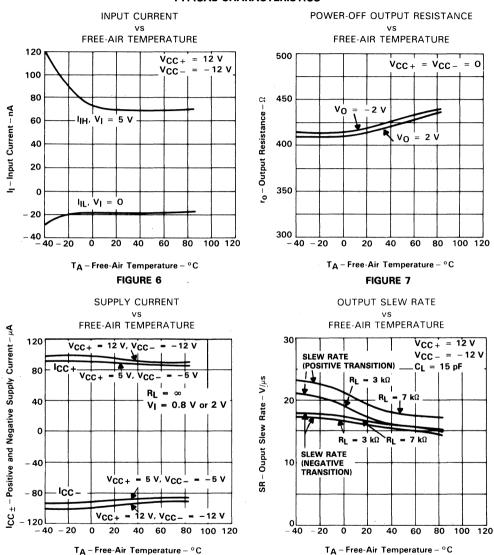


FIGURE 8

FIGURE 9

VS

†THL

tTLH

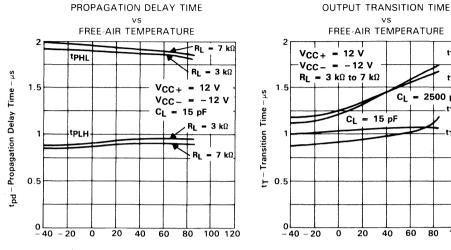
tTHL-

TLH-

100 120

= 2500 pF

TYPICAL CHARACTERISTICS



TA - Free-Air Temperature - °C

FIGURE 10

TA - Free-Air Temperature - °C

60

FIGURE 11

APPLICATION INFORMATION

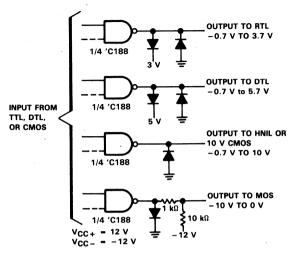
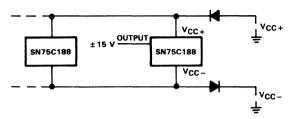


FIGURE 12. LOGIC TRANSLATOR APPLICATIONS

APPLICATION INFORMATION



NOTE: External diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75C188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

FIGURE 13. POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF STANDARD EIA-232-D

SN65C1154, SN75C1154 OUADRUPLE LOW-POWER DRIVERS/RECEIVERS

D3230, DECEMBER 1988-REVISED MAY 1990

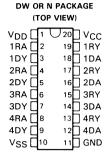
- Meets Standard EIA-232-D (Revision of RS-232-C)
- Very Low Power Consumption . . . 5 mW Typ
- Wide Driver Supply Voltage . . . ± 4.5 V to + 15 V
- Driver Output Slew Rate Limited to 30 V/μs
 Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1-μs Noise Filter
- ESD Protection Exceeds 2000 V Per MIL-Std-833C Method 3015

description

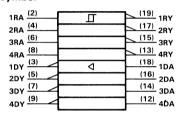
The SN65C1154 and SN75C1154 are lowpower BI-MOS devices containing 4 independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuitterminating equipment (DCE). This device has been designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/µs and the receivers have filters that reject input noise pulses of shorter than 1 μ s. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1154 is characterized for operation from -40°C to 85°C. The SN75C1154 is characterized for operation from 0°C to 70°C.



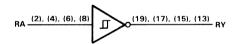
logic symbol†



 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

typical of each receiver

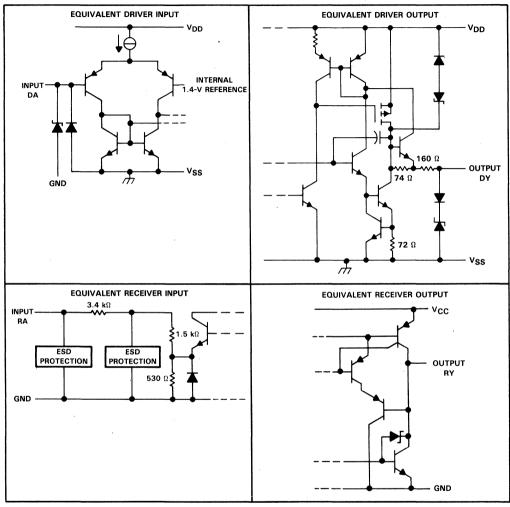


typical of each driver





schematics of inputs and outputs



All resistor values shown are nominal.

SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VDD (see Note 1) |
|--|
| Supply voltage, VSS |
| Supply voltage, VCC |
| Input voltage range: Driver |
| Receiver |
| Output voltage range: Driver (VSS - 6 V) to (VDD + 6 V) |
| Receiver |
| Continuous total power dissipation |
| Operating free-air temperature range: SN65C115440°C to 85°C |
| SN75C1154 |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 585 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|--|--------------------|---|-------------------------|------------|
| Supply voltage, V _{DD} | | 4.5 | 12 | 15 | V |
| Supply voltage, VSS | | -4.5 | - 12 | - 15 | ٧ |
| Supply voltage, VCC | | 4.5 | 5 | 6 | ٧ |
| nput voltage, V _I | Driver | V _{SS} +2 | | V_{DD} | ν . |
| input voltage, vj | Driver Receiver Itage, VIL urrent, IOH Receiver Receiver Priver Receiver Receiver | | | ±25 | . v |
| High-level input voltage, VIH | Deliver | 2 | | 5 6 VDD ± 25 0.8 -1 3.2 | V |
| Low-level input voltage, VIL | ver | | | 0.8 | ľ |
| High-level output current, IOH | Panalysis | | 1.5 12 15 1.5 -12 -15 1.5 5 6 1.2 V _{DD} ±25 2 0.8 -1 3.2 | mA | |
| Low-level output current, IOL | Neceiver | | _ | 3.2 | mA |
| Operating free-air temperature, TA | SN65C1154 | -40 | | 85 | °C |
| | SN75C1154 | 0 | | 70 | 1 " |

SN65C1154, SN75C1154 QUADRUPLE LOW-POWER DRIVERS/RECEIVERS

driver section

electrical characteristics over operating free-air temperature range, $V_{DD} = 12 \text{ V}$, $V_{SS} = -12 \text{ V}$, $V_{CC} = 5 \text{ V} \pm 10\%$ (unless otherwise noted)

| | PARAMETER | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|------|-----------------------------|--|---|-----|--------|--------|------|
| Vall | High level and a decidence | $V_{IL} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega,$ | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | 4 | 4.5 | | ٧ |
| Vон | High-level output voltage | See Figure 1 | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | 10 | 10.8 | | V |
| Vai | Low-level output voltage | $V_{IH} = 2 V$, $R_L = 3 k\Omega$, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | -4.4 | -4 | V |
| VOL | (See Note 2) | See Figure 1 | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | - 10.7 | - 10 | V |
| ΊΗ | High-level input current | V _I = 5 V, See Figure 2 | | | | 1 | μΑ |
| ΊL | Low-level input current | V _I = 0, See Figure 2 | | | | - 1 | μΑ |
| lagu | High-level short circuit | V: = 0.8 V Vo = 0.0r Voo | $V_{I} = 0.8 \text{ V}, V_{O} = 0 \text{ or } V_{SS}, \text{ See Figure 1}$ | | | 19.5 | mA |
| losh | output current [‡] | V = 0.8 V, V() = 0 81 VSS, | | | | - 13.5 | |
| loo | Low-level short circuit | $V_1 = 2 V$, $V_0 = 0$ or V_{DD} , S | oo Eiguro 1 | 7.5 | 12 | 19.5 | mA |
| IOSL | output current [‡] | V = 2 V, VO = 0 0 VDD, 3 | ee riguie i | 7.5 | 12 | 13.5 | |
| loo | Supply current from VDD | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | 115 | 250 | μΑ |
| IDD | Supply culterit from VDD | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | 115 | 250 | μ. |
| laa | Cumply ourrent from Va- | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | -115 | - 250 | ^ |
| ISS | Supply current from VSS | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | -115 | - 250 | μΑ |
| ro | Output resistance | $V_{DD} = V_{SS} = V_{CC} = 0, V_{O}$ | = -2 V to 2 V, See Note 3 | 300 | 400 | | Ω |

 $^{^{\}dagger}$ All typical values are at $T_A = 25$ °C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

3. Test conditions are those specified by EIA-232-D.

switching characteristics at $T_A = 25$ °C, $V_{DD} = 12$ V, $V_{SS} = -12$ V, $V_{CC} = 5$ V $\pm 10\%$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|------|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high level output § | $R_1 = 3 \text{ to } 7 \text{ k}\Omega$ | | 1.2 | 3 | μS |
| tPHL | Propagation delay time, high-to-low level output § | $C_{l} = 3 \text{ to } 7 \text{ ku},$ $C_{l} = 15 \text{ pF},$ | | 2.5 | 3.5 | μs |
| tTLH | Transition time, low-to-high level output | See Figure 3 | 0.53 | 2 | 3.2 | μs |
| tTHL | Transition time, high-to-low level output | See Figure 3 | 0.53 | 2 | 3.2 | μS |
| tTLH | Transition time, low-to-high level output# | $R_L = 3 \text{ to } 7 \text{ k}\Omega,$ $C_1 = 2500 \text{ pF},$ | | 1 | 2 | μs |
| tTHL | Transition time, high-to-low level output# | See Figure 3 | | 1 | 2 | μs |
| SR | Output slew rate | $R_L=3$ to 7 k Ω , $C_L=150$ pF, See Figure 3 | 4 | 10 | 30 | V/μs |

[§]tpHL and tpLH include the additional time due to on-chip slew rate and are measured at the 50% points.

[‡]Not more than one output should be shorted at one time.

Measured between 10% and 90% points of output waveform.

[#]Measured between 3 V and -3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

receiver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10% (unless otherwise noted)

| | PARAMETER | TEST CO | INDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|--|---|----------|------------------|---|------|
| V _{T+} | Positive-going threshold voltage | See Figure 5 | | 1.7 | 2.1 | 2.55 | ٧ |
| V _T - | Negative-going threshold voltage | See Figure 5 | | | 1 | 1.25 | ٧ |
| V _{hys} | Input hysteresis [‡] | | | 600 | 1000 | | mV |
| | | $V_1 = 0.75 \text{ V}, I_{OH} = -20 \mu \text{A}$ | | 3.5 | | | |
| Vон | High-level output voltage | See Figure 5 | $V_{CC} = 4.5 V$ | 2.8 | 4.4 | | v |
| VOH | | | V _{CC} = 5 V | 3.8 | 4.9 | | |
| | | | V _{CC} = 5.5 V | 4.3 | 5.4 | | |
| VOL | Low-level output voltage | $V_1 = 3 \text{ V}, I_{OL} = 3.2 \text{ mA}, Sec$ | Figure 5 | 0.17 0.4 | | | |
| lu. | High-level input current | V _I = 25 V | | 3.6 | 4.6 | 8.3 | |
| ΊΗ | nigh-level input current | V _I = 3 V | | 0.43 | 0.55 | 1 | mA |
| L. | | $V_1 = -25 \text{ V}$ | | -3.6 | - 5 | 2.1 2.55 1 1.25 2000 4.4 4.9 5.4 .17 0.4 4.6 8.3 .55 1 -5 -8.3 .55 -1 -8 -15 13 25 400 600 | IIIA |
| IIL | Low-level input current | V _I = -3 V | | -0.43 | -0.55 | | |
| losн | Short-circuit output at high level | V _I = 0.75 V, V _O = 0, See Fi | $V_{I} = 0.75 \text{ V}, V_{O} = 0, \text{ See Figure 4}$ | | -8 | - 15 | mA |
| losL | Short-circuit output current at low level | V _I = V _{CC} , V _O = V _{CC} , See Figure 4 | | | 13 | 25 | mA |
| loo | Cumply ourrent from Van | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | 400 | 600 | ^ |
| Icc | Supply current from V _{CC} | All inputs at 0 or 5 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | 400 | 600 | μΑ |

 $^{^{\}dagger}$ All typical values are at T_A = 25 °C.

switching characteristics at TA = $25\,^{\circ}$ C, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10% (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------|--|---|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high level output | | | 3 | 4 | μS |
| tPHL | Propagation delay time, high-to-low level output | $C_L = 50 \text{ pF}, R_L = 5 \text{ k}\Omega,$ | | 3 | 4 | μS |
| tTLH | Transition time, low-to-high level output§ | See Figure 6 | | 300 | 450 | ns |
| tTHL | Transition time, high-to-low level output§ | | | 100 | 300 | ns |
| tw(N) | Duration of longest pulse rejected as noise | $C_L = 50 \text{ pF}, R_L = 5 \text{ k}\Omega$ | 1 | | 4 | μS |

Measured between 10% and 90% points of output waveforms.

[‡]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{W(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{W(N)}$.

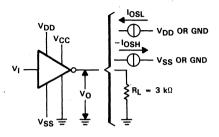


FIGURE 1. DRIVER TEST CIRCUIT, VOH, VOL, IOSL, IOSH

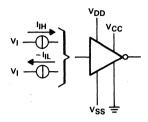
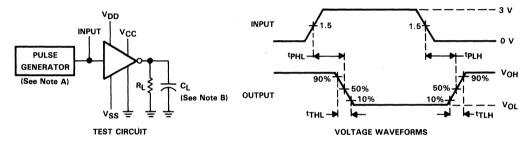


FIGURE 2. DRIVER TEST CIRCUIT, IIL, IIH



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, PRR = 20 kHz, $Z_O = 50 \Omega$, $t_f = t_f < 50 ns$. B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER PROPAGATION AND TRANSITION TIMES

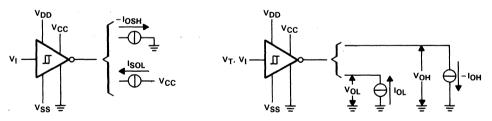
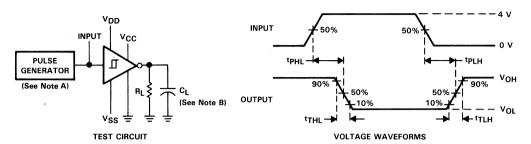


FIGURE 4. RECEIVER TEST CIRCUIT, IOSH, IOSL FIGURE 5. RECEIVER TEST CIRCUIT, V_T, V_{OL}, V_{OH}



NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, PRR = 20 kHz, $Z_0 = 50 \Omega$, $t_r = t_f < 50 ns$. B. C_L includes probe and jig capacitance.

FIGURE 6. RECEIVER PROPAGATION AND TRANSITION TIMES

D3425, MAY 1990

- Meets Standard EIA-232-D (Revision of RS-232-C)
- Very Low Power Consumption . . . 5 mW
 Tvp
- Wide Driver Supply Voltage . . . ±4.5 V to +15 V
- Driver Output Slew Rate Limited to 30 V/μs Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1-μs Noise Filter
- Functionally Interchangeable with Motorola MC145406
- ESD Protection Exceeds 2000 V Per MIL-Std-883C Method 3015

description

The SN65C1406 and SN75C1406 are lowpower BI-MOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to Standards ANSI/EIA-232-D-1986 (which supersedes RS-232-C). The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 $V/\mu s$ and the receivers have filters that reject input noise pulses of shorter than 1 μ s. Both these features eliminate the need for external components.

The SN65C1406 and SN75C1406 have been designed using low-power techniques in a BI-MOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from -40°C to 85°C. The SN75C1406 is characterized for operation from 0°C to 70°C.

| | N PACKAGE P VIEW) |
|--------------------|----------------------|
| V _{DD} □1 | U16 VCC |
| 1RA 🛮 2 | 15 1RY |
| 1DY 🛮 3 | 14 🗍 1DA |
| 2RA 🛮 4 | 13 2RY |
| 2DY 🛮 5 | 12 2DA |
| 3RA | 11 3RY |
| 3DY 🛮 7 | 10 ☐ 3DA |
| Vss ∏8 | 9 GND |

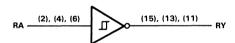
logic symbol†

| 1RA 4 13 1RY 2RA 4 11 2RY | |
|---------------------------|---|
| 6 - 11 | |
| 3RA 3RY | Y |
| 1DY 1DA | |
| 2DY 5 12 2DA 3DY 7 10 3DA | |

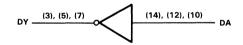
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

typical of each receiver

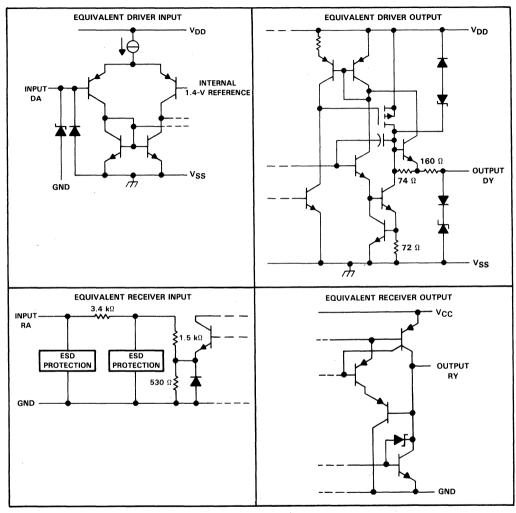


typical of each driver





schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VDD (see Note 1) |
|--|
| Supply voltage, VSS |
| Supply voltage, VCC |
| Input voltage range: Driver |
| Receiver |
| Output voltage range: Driver (VSS - 6 V) to (VDD + 6 V) |
| Receiver |
| Continuous total power dissipation |
| Operating free-air temperature range: SN65C140640°C to 85°C |
| SN75C1406 |
| Storage temperature range |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-----------|---------------------|-----|-----------------|------|
| Supply voltage, V _{DD} | | 4.5 | 12 | 15 | V |
| Supply voltage, VSS | | -4.5 | -12 | - 15 | V |
| Supply voltage, V _{CC} | | 4.5 | 5 | 6 | V |
| Innut valtage V | Driver | V _{SS} + 2 | | V _{DD} | V |
| Input voltage, V _I | Receiver | | | ± 25 | ľ |
| High-level input voltage, VIH | Driver | 2 | | | V |
| Low-level input voltage, V _{IL} | Driver | | | 0.8 | · |
| High-level output current, IOH | Dessituat | | | - 1 | mA |
| Low-level output current, IOL | Receiver | | | 3.2 | mA |
| Oncerting free air termenture T | SN65C1406 | -40 | | 85 | °C |
| Operating free-air temperature, TA | SN75C1406 | 0 | | 70 | ٦ |

SN65C1406, SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

driver section

electrical characteristics over operating free-air temperature range, VDD = 12 V, VSS = -12 V, $VCC = 5 V \pm 10\%$ (unless otherwise noted)

| | PARAMETER | TEST CO | INDITIONS | MIN | TYP [†] | MAX | UNIT |
|------|-----------------------------|--|---|-----|------------------|-------|--------|
| V/0 | High-level output voltage | $V_{IL} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega,$ | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | 4 | 4.5 | | V |
| Уон | riigii-ievei output voitage | See Figure 1 | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | 10 | 10.8 | | · · |
| VOL | Low-level output voltage | $V_{IH} = 2 V$, $R_L = 3 k\Omega$, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | -4.4 | - 4 | ٧ |
| VOL | (See Note 2) | See Figure 1 | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | - 10.7 | - 10 | |
| ΙН | High-level input current | V _I = 5 V, See Figure 2 | | | | 1 | μΑ |
| IIL | Low-level input current | V _I = 0, See Figure 2 | | | | - 1 | μΑ |
| losh | High-level short circuit | Vi = 0.8 V. Vo = 0 or Vcc | $V_1 = 0.8 \text{ V}, V_0 = 0 \text{ or VSS}, \text{ See Figure 1}$ | | ~ 12 | _195 | mA |
| 102H | output current [‡] | V = 0.0 V, V() = 0.01 VSS, | See Figure 1 | 7.5 | | 10.5 | 1111/2 |
| IOSL | Low-level short circuit | $V_1 = 2 V, V_0 = 0 \text{ or } V_{DD}, S$ | ee Figure 1 | 7.5 | 12 | 19.5 | · mA |
| -USL | output current [‡] | 1 = 2 1, 10 = 8 8, 1 _{DD} , 8 | | 7.0 | | 10.0 | 1117 |
| Inn | Supply current from VDD | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | 115 | 250 | μΑ |
| IDD | Supply culterit from VDD | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | 115 | 250 | μΛ |
| laa | Supply current from Vss | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | - 115 | - 250 | μΑ |
| Iss | Supply culterit from VSS | All inputs at 2 V or 0.8 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | -115 | - 250 | μΑ |
| ro | Output resistance | $V_{DD} = V_{SS} = V_{CC} = 0, V_{O}$ | = -2 V to 2 V, See Note 3 | 300 | 400 | | Ω |

 $^{^{\}dagger}$ All typical values are at $T_A = 25 \,^{\circ}$ C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

3. Test conditions are those specified by EIA-232-D.

switching characteristics at $T_A = 25$ °C, $V_{DD} = 12$ V, $V_{SS} = -12$ V, $V_{CC} = 5$ V $\pm 10\%$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|------|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high level output § | B: 2 to 7 to | | 1.2 | 3 | μS |
| tPHL | Propagation delay time, high-to-low level output § | $R_L = 3 \text{ to } 7 \text{ k}\Omega$, $C_1 = 15 \text{ pF}$, | | 2.5 | 3.5 | μS |
| †TLH | Transition time, low-to-high level output¶ | See Figure 3 | 0.53 | 2 | 3.2 | μs |
| tTHL | Transition time, high-to-low level output | See Figure 3 | 0.53 | 2 | 3.2 | μS |
| tTLH | Transition time, low-to-high level output# | $R_L = 3 \text{ to } 7 \text{ k}\Omega$ | | 1 | 2 | μS |
| tTHL | Transition time, high-to-low level output# | C _L = 2500 pF, See Figure 3 | | 1 | 2 | μS |
| SR | Output slew rate | R _L = 3 to 7 kΩ, C _L = 150 pF, See Figure 3 | 4 | 10 | 30 | V/μs |

[§]tpHi and tpi H include the additional time due to on-chip slew rate and are measured at the 50% points.

[‡]Not more than one output should be shorted at one time.

Measured between 10% and 90% points of output waveform.

[#]Measured between 3 V and −3 V points of output waveform (EIA-232-D conditions) with all unused inputs tied either high or low.

receiver section

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10% (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|-------------------------------------|---|--|-------|------------------|------|----------|
| V _{T+} | Positive-going threshold voltage | See Figure 5 | See Figure 5 | | 2.1 | 2.55 | v |
| VT- | Negative-going threshold voltage | See Figure 5 | | 0.65 | 1 | 1.25 | ٧ |
| V _{hys} | Input hysteresis.‡ | | | 600 | 1000 | | mV |
| | | $V_1 = 0.75 \text{ V}, I_{OH} = -20 \mu \text{A}$ | , See Figure 5 and Note 4 | 3.5 | | | |
| V | High-level output voltage | V: = 0.75 V lov = 1 mA | $V_{CC} = 4.5 V$ | 2.8 | 4.4 | | v |
| Vон | nigh-level output voltage | | V _{CC} = 5 V | 3.8 | 4.9 | | v |
| | | | V _{CC} = 5.5 V | 4.3 | 5.4 | | |
| VOL | Low-level output voltage | $V_{I} = 3 \text{ V, I}_{OL} = 3.2 \text{ mA, See}$ | V _I = 3 V, I _{OL} = 3.2 mA, See Figure 5 | | 0.17 | 0.4 | ٧ |
| | High-level input current | V _I = 25 V | $V_1 = 25 \text{ V}$ | | 4.6 | 8.3 | |
| ΉΗ | nigri-level input current | V _I = 3 V | | 0.43 | 0.55 | 1 | mA |
| | Lave lavel facet access | $V_{ } = -25 \text{ V}$ | | -3.6 | - 5 | -8.3 | IIIA |
| l IIL | Low-level input current | $V_I = -3 V$ | | -0.43 | -0.55 | - 1 | |
| losh | Short-circuit output at high level | V _I = 0.75 V, V _O = 0, See Figure 4 | | | -8 | - 15 | mA |
| | Short-circuit output | $V_1 = V_{CC}, V_0 = V_{CC}, See Figure 4$ | | | 13 | . 25 | mA |
| IOSL | current at low level | | | | 13 | . 25 | IIIA |
| [₁ | Cumply assessed from Va- | No load, | $V_{DD} = 5 \text{ V}, V_{SS} = -5 \text{ V}$ | | 320 | 450 | |
| Icc | Supply current from V _{CC} | All inputs at 0 or 5 V | $V_{DD} = 12 \text{ V}, V_{SS} = -12 \text{ V}$ | | 320 | 450 | μΑ |

[†]All typical values are at T_A = 25 °C.

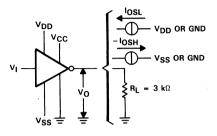
switching characteristics at $T_A = 25$ °C, $V_{DD} = 12$ V, $V_{SS} = -12$ V, $V_{CC} = 5$ V $\pm 10\%$ (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------|--|---|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high level output | | | 3 | 4 | μS |
| tPHL | Propagation delay time, high-to-low level output | $C_L = 50 \text{ pF}, R_L = 5 \text{ k}\Omega,$ | | 3 | 4 | μS |
| tTLH | Transition time, low-to-high level output§ | See Figure 6 | | 300 | 450 | ns |
| tTHL | Transition time, high-to-low level output§ | | | 100 | 300 | ns |
| tw(N) | Duration of longest pulse rejected as noise | $C_L = 50 \text{ pF}, R_L = 5 \text{ k}\Omega$ | 1 | | 4 | μs |

[§]Measured between 10% and 90% points of output waveforms.

[†]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

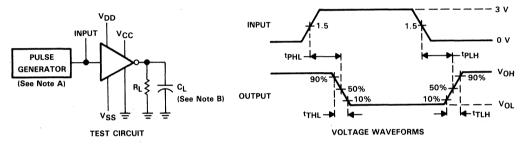
The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{W(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{W(N)}$.



Vcc

FIGURE 1. DRIVER TEST CIRCUIT, VOH, VOL, IOSL, IOSH

FIGURE 2. DRIVER TEST CIRCUIT, IIL, IIH



NOTES: A. The pulse generator has the following characteristics: $t_W = 25~\mu s$, PRR = 20 kHz, $Z_0 = 50~\Omega$, $t_r = t_f < 50~ns$. B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER PROPAGATION AND TRANSITION TIMES

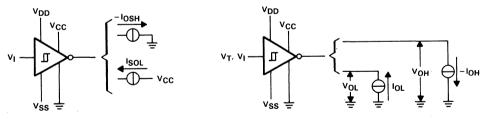
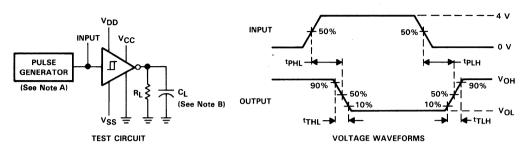


FIGURE 5. RECEIVER TEST CIRCUIT, VT, VOL, VOH FIGURE 4. RECEIVER TEST CIRCUIT, IOSH, IOSL



NOTES: A. The pulse generator has the following characteristics: $t_W = 25~\mu s$, PRR = 20 kHz, $Z_0 = 50~\Omega$, $t_f = t_f < 50~ns$. B. C_L includes probe and jig capacitance.

FIGURE 6. RECEIVER PROPAGATION AND TRANSITION TIMES

SN75061 DRIVER/RECEIVER PAIR WITH SQUELCH

D2959, JANUARY 1987-REVISED JULY 1990

| • | IEEE 802.3 1BASE5 Driver and Receiver | N PACKAGE | | |
|---|---|--------------------------------------|------------------------------------|--|
| • | On-Chip Receiver Squelch with Adjustable Threshold | (TOP \ | VIEW) | |
| • | Adjustable Squelch Delay | DRO + ☐ 2 DRO – ☐ 3 | 15 DATEN 14 DRI | |
| • | Direct TTL-Level Squelch Output | SQDLAJ 4 | 13 DLEN | |
| • | Squelch Circuit Allows for External Noise Filtering | RXI + ☐ 5 RXI – ☐ 6 SQTHAJ ☐ 7 | 12 ☐ RXO 11 ☐ SQO 10 ☐ SQDLI | |
| • | Two Driver-Enable Options | GND ☐8 | 9 SQRXO | |

- On-Chip Start-of-Idle Detection and Disable
- Driver Provides 2 V Minimum into a 50-Ω Differential Load to Allow for Use with Doubly-Terminated Lines and Multipoint Architectures
- On-Chip Driver Slew-Rate Control for Very Closely Matched Output Rise and Fall Times

| | PIN | |
|--------|--------|---|
| NAME | NUMBER | DESCRIPTION |
| DATEN | 15 | Driver Data Enable. When low, places driver outputs in an active state. When high, the driver outputs |
| | | are in a high-impedance state if DLEN is also high. |
| DLEN | 13 | Driver Delay Enable. When this signal is low and DATEN is high, the driver outputs are active for a |
| | | period of time set by DRDLAJ after a positive-going transition on DRI. If there is no active data on DRI, |
| | | the outputs are in a high-impedance state. |
| DRDLAJ | 1 | Driver Delay Adjust is a connection for the external R-C combination that determines the duration of |
| | | the driver output active state after a positive transition on DRI when DLEN is low and DATEN is high. |
| DRI | 14 | Driver Data Input |
| DRO+ | 2 | Noninverting Driver Output |
| DRO - | 3 | Inverting Driver Output |
| GND | 8 | Ground. Common for all voltages |
| RXI+ | 5 | Noninverting Receiver Input |
| RXI – | 6 | Inverting Receiver Input |
| RXO | 12 | Main Receiver Output |
| SQDLAJ | 4 | Squelch Delay Adjust is a connection for an external R-C combination that determines the duration |
| | | of the receiver unsquelch after a negative-going transition on SQDLI. |
| SQDLI | 10 | Squelch Delay Input is the input to the one-shot that controls the duration of the receiver unsquelch |
| | | period. The main receiver output remains unsquelched as long as SQDLI is held high. Timing of the |
| | | unsquelch period begins on the high-to-low transition of SQDLI. |
| sqo | 11 | Squelch Output is high while the receiver is squelched. |
| SQRXO | 9 | Squelch Receiver Output is high only when the differential receiver input exceeds the threshold set |
| | | by SQTHAJ. |
| SQTHAJ | 7 | Squelch Receiver Threshold Adjust. The voltage at this input determines the threshold of the squelch |
| | | receiver in a ratio of -2, SQTHAJ to threshold. If left open, the squelch receiver threshold defaults |
| | | to -600 mV. |
| Vcc | 16 | Supply voltage input |

FUNCTION TABLES

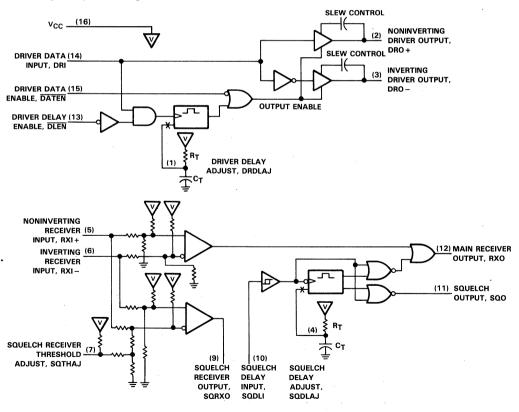
| | | DRIV | ER . | |
|-----|-------|------|----------------|-------|
| | PUTS | | | |
| DRI | DATEN | DLEN | DRO+ | DRO – |
| L | L | × | L | Н |
| н | L | X | Н | L |
| х | н | Н | z | Z |
| Н | н | L | H [†] | L† |
| L | н | L | L‡ | H‡ |

| RECEIVER [§] | | | | | | | |
|-----------------------|------|--------|---------|-----|--|--|--|
| CONDITION | INP | UTS | OUTPUTS | | | | |
| CONDITION | RXI+ | `RXI – | RXO | sqo | | | |
| No active signal ¶ | X | Х | Н | Н | | | |
| Active signal¶ | L. | Н | L | L | | | |
| Active signal | Н | L | н | L | | | |

[†]This condition is valid during the time period set by Driver Delay Adjust following a rising transition on Driver In. Following this, if no subsequent positive transition occurs on Driver In, the outputs will go to the high impedance state.

†This condition is valid if it occurs within the enable time set by Driver Delay Adjust after a rising transition on Driver In. Otherwise the outputs will be in the high-impedance state.

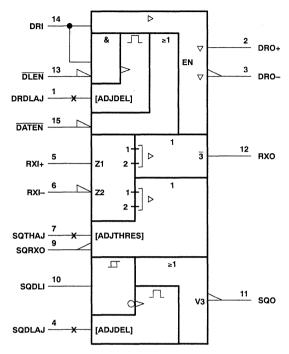
logic diagram (positive logic)



[§]Pins 9 and 10 are tied together.

[¶]An active signal is one that has an amplitude greater than the threshold level set by Squelch Threshold Adjust.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN75061 is a single-channel driver/receiver pair designed for use in IEEE 802.3, 1BASE5 applications as well as other general data communications circuits. The SN75061 offers the system designer both a driver and a receiver that are easily configured for use with a variety of controllers and data encoder/decoders.

The receiver features a full analog squelch circuit with an adjustable threshold and a programmable squelch delay. Internal nodes of the squelch circuitry are brought out to external connections to allow for the insertion of noise filtering circuitry of the designer's choice.

As with the receiver, the driver offers the user a variety of implementation options. Driver enabling may be controlled directly by an external logic input, or by use of an on-chip one-shot that is retriggered as long as data is being sent to the driver. The driver will then automatically go to the high-impedance state when end-of-packet occurs. The driver features internal slew-rate control for optimal matching of rise and fall times allowing for reduction of driver-induced jitter.

receiver

The SN75061 receiver implements full analog squelch functions by integrating both a separate, parallel squelch receiver with an externally programmable threshold, and a programmable one-shot. The output of the squelch receiver and the input to the high-level dc-triggered one-shot are brought out to external connections. These pins can be shorted for direct implementation, or used for the insertion of noise-filtering



SN75061 DRIVER/RECEIVER PAIR WITH SQUELCH

circuitry of the implementer's design. The receiver one-shot can be effectively bypassed by applying a high logic level to Squelch Delay In. The squelch threshold may be set externally by applying an external voltage set to a level that is -2 times the desired threshold voltage. If Squelch Threshold Adjust is left open, the squelch receiver will default to its internal preset value of -600 mV. The receiver also outputs a high logic "squelch" signal when there is no active data present at the receiver inputs. When no data is present on the transmission line, the receiver output assumes a high level. The "unsquelch" duration is set externally with an R-C combination at Squelch Delay Adjust.

driver

The driver offers the user a variety of implementation options. Driver enabling may be controlled directly by an active-low external logic input on Data Enable, or by use of another on-chip one-shot that retriggers with positive-going transitions on the driver input line. If no positive transition occurs within the pulse duration set by an external R-C combination, the one-shot times out and the driver is automatically put into a high-impedance state. When operating in the defay-enable mode, the 2-bit-time high-level start-ofidle pulse prescribed by IEEE 802.3 1BASE5 causes the one-shot to time out and automatically place the driver outputs in the high-impedance state. This delay time is also adjustable for use in other applications. The driver implements an output slew-rate control that is internally set for nominally 40 mV/ns. (This is roughly a 100-ns peak-to-peak differential transition time.) The driver outputs are capable of driving a $50-\Omega$ differential load with a minimum output level of 2 V. Short-circuit output current is greater than 100 mA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} |
|---|
| Input voltage (any logic input) |
| Receiver differential input voltage |
| Receiver input voltage |
| Driver output voltage |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) 1150 mW |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: For operation above 25 °C free-air temperature, derate to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----------|-------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | ٧ |
| Driver high-level input voltage, VIH | 2 | | | ٧ |
| Driver low-level input voltage, V _{IL} | | | 0.8 | V |
| Driver high-level output current, IOH | | | - 150 | mA |
| Driver low-level output current, IOL | | | 150 | mA |
| Receiver common-mode input voltage, V _{IC} (see Note 2) | -2.5 | | 5 | V |
| External timing resistance, Rext | 5 | | 260 | kΩ |
| External timing capacitance, Cext | · N | o restric | tion | |
| Operating free-air temperature, TA | 0 | | 70 | °C |

NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage VIC and threshold levels VTH and VTI.

electrical characteristics over recommended operating free-air and supply voltage range (unless otherwise noted)

driver

| PARAMETER | | TEST (| CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---------------------------------------|-----------------------------|---|-------|------------------|-------|------|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| 1/ | Differential autout valence | $R_L = 50 \Omega$ | | 2 | 2.4 | 3.3 | V |
| VOD | Differential-output voltage | $R_L = 115 \Omega$ | | | | 3.65 | V |
| 4)/ | Change in differential-output voltage | | | | | 50 | mV |
| ΔV _{OD} | for a change in logic input state | | | | | 50 | IIIV |
| ΊΗ | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| IIL | Low-level input current | V _I = 0.5 V | | | - | - 35 | μΑ |
| los | Short-circuit output current | $V_0 = 0 \text{ or } 6 V$, | $V_1 = 0.8 \text{ V or } 2.5 \text{ V}$ | ± 100 | | ± 300 | mA |
| 1 | High impedance output gurrent | V _{CC} = 5.25 V | V _{OC} = 10 V | | | 100 | |
| loz | High-impedance output current | VCC = 5.25 V | $V_{OC} = 0$ | | | - 100 | μΑ |

receiver

| | PARAMETER | | TEST C | ONDITIONS | MIN | TYP [†] | MAX | UNIT |
|---------------------|--|--|---|--|-------|------------------|-------|------|
| VIK | Input clamp voltage, squelch | delay | I _I = -18 mA | | | | -1.5 | V |
| VTH | Differential-input high-thresh | old voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 50 | mV |
| V _{TL} | Differential-input low-threshovoltage (see Note 2) | ild | V _O = 0.5 V, | I _O = 16 mA | - 50 | | | mV |
| V _{hys} | Hysteresis (V _{TH} - V _{TL}) | | | | | 50 | | mV |
| VIC | Common-mode input voltage | | | | | | 5 | V |
| | | RXO | $V_{CC} = 4.75 V$, | $I_{OH} = -400 \mu A$, | 2.7 | | | |
| 1/ | High lavel and water and | SQO | SQDLAJ at 0.8 V | | 2.7 | 3.5 | | V |
| Vон | High-level output voltage | SQRXO | $V_{CC} = 4.75 \text{ V},$ $V_{ID(RXI)} = -0.7 \text{ V},$ | I _{OH} = -20 μA, SQDLAJ open | 2.7 | 4.65 | | V |
| | Low-level output voltage | RXO $V_{CC} = 4.75 \text{ V},$ SQDLAJ at 2 V | Voc = 4.75.V | I _{OL} = 8 mA | | | 0.45 | |
| V _{OL} | | | I _{OL} = 16 mA | | | 0.5 | ĺ | |
| | | SQO | SQDEAS at 2 V | I _{OL} = 8 mA | | 0.35 | 0.5 | V |
| | | SQRXO | $V_{CC} = 4.75 V$, | I _{OL} = 8 mA | | | 0.45 | |
| | | SUNAU | $V_{ID(RXI)} = 50 \text{ mV}$ | I _{OL} = 16 mA | | | 0.5 | ĺ |
| lіН | High-level input current | SQDLI | V _I = 2.4 V | | | | 20 | μΑ |
| ΙΙL | Low-level input current | SUDLI | $V_{ } = 0.5 V$ | | | | - 35 | μΑ |
| | | RXO | Vcc = 5.25 V. V | V= - 0 | - 15 | | -85 | |
| los | Short-circuit output current | SQO | | ν0 = 0 | - 15 | | - 100 | mA |
| | | SQRXO | $V_{CC} = 5 V$, | V _O = 0 | -0.8 | - 1 | -1.2 | ĺ |
| rı | Input resistance | | | | | 10 | | kΩ |
| | Squelch preset | | V _{CC} = 5 V, | VIC = 1.5 V to 3.5 V | - 525 | -600 | -675 | mV |
| V _{TL(sq)} | | | SQTHAJ OPEN, | $V_{IC} = -2.5 \text{ V to } 1.5 \text{ V}$ or 3.5 V to 5 V | - 500 | | - 700 | mV |
| | Ratio of Squelch Threshold A input voltage to actual squel threshold voltage | | SQTHAJ at 200 mV | to 4 V | -1.9 | | -2.1 | |

driver and receiver

| ICC Supply current No loads | ¹ CC | Supply current | V _{CC} = 5.25 V, | Driver outputs disabled, | 70 | mA |
|-----------------------------|-----------------|----------------|---------------------------|--------------------------|----|----|
|-----------------------------|-----------------|----------------|---------------------------|--------------------------|----|----|

 $^{^{\}dagger}\,\text{All}$ typical values are at VCC = 5 V, TA = 25 °C.

NOTE 2: The algebraic convention, in which the less-positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{TH} and V_{TL} .



switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

driver

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---|-----|-----|-----|-------|
| SR | Differential-output slew rate | $V_0 = -2 \text{ V to } 2 \text{ V},$ $R_L = 100 \Omega \text{ (differential)}, See Figure 1$ | 28 | 40 | 52 | mV/ns |
| ^t DD | Differential-output delay time (tDD+ and tDD-) | $C_1 = 15 \text{ pF},$ $R_L = 100 \Omega \text{ (differential)}, See Figure 2$ | | | 160 | ns |
| t _{DD+} -t _{DD-} | Differential-output delay time difference | $R_L = 100 \Omega$ (differential), See Figure 2 | | | 5 | ns |
| ^t PHZ | Disable time from DATEN | | | | 220 | ns |
| tPLZ | Disable time from DATEN | | | _ | 300 | ns |
| ^t PZH | Enable time from DATEN | See Figures 3, 4, and 5 | | | 220 | ns |
| tPZL | Enable time from DATEN | | | | 290 | ns |
| ^t PZH | Enable time from DLEN | Ţ | | | 250 | ns |
| ^t w(en) | Enable duration time (with DLEN low) | C_{ext} = 100 pF, R_{ext} = 62 k Ω , See Figure 6 | 2 | 2.5 | 3 | μS |

receiver

| PARAMETER | | TEST CON | MIN | TYP | MAX | UNIT | |
|---------------------|--|---|--|-----|-----|------|----|
| t _{en(RX)} | Receiver enable time | Squelch off, | See Figure 7 | | 117 | | ns |
| tPLH | Propagation delay time, low-to-high-level output | Squelch off, | See Figure 8 | | 20 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Squelch off, | See Figure 8 | | 22 | 35 | ns |
| | Unsquelch duration time | C _{ext} = 50 pF, See Figure 9 | $R_{\text{ext}} = 51 \text{ k}\Omega,$ | 1 | 1.2 | 1.45 | μS |
| tunsq | onsqueion duration time | C _{ext} = 15 pF, See Figure 9 | $R_{\text{ext}} = 6.8 \text{ k}\Omega$, | | | 180 | ns |

PARAMETER MEASUREMENT INFORMATION

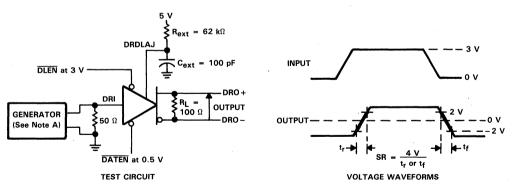


FIGURE 1. DRIVER SLEW RATE MEASUREMENTS

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, Duty Cycle \leq 50%, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{OUT} =$ 50 Ω .



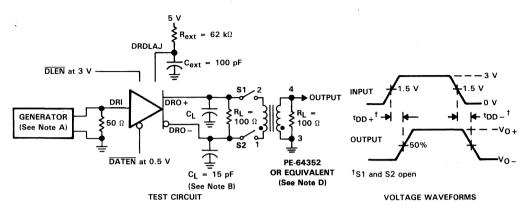


FIGURE 2. DRIVER DIFFERENTIAL DELAY TIMES

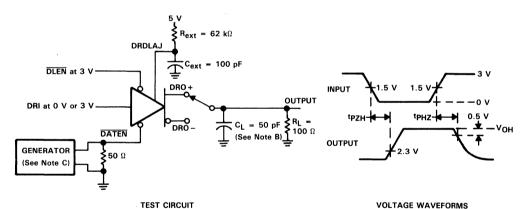


FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, Duty Cycle \leq 50%, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} =$ 50 Ω .
 - B. C_L includes probe and jig capacitance.
 - C. The input pulse is supplied by a generator having the following characteristics: PRR \leq 500 kHz, Duty Cycle \leq 50%, $t_f \leq$ 6 ns, $t_f \leq$ 6ns, $t_{QUt} =$ 50 Ω .
 - D. When measuring differential-output delay time difference, switches S1 and S2 are closed. (Isolation transformer from Pulse Engineering P/N PE-64352).

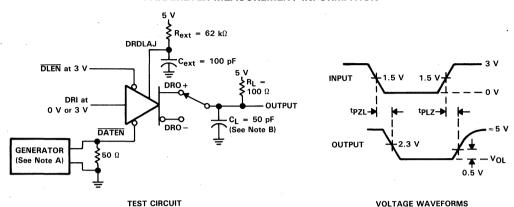


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

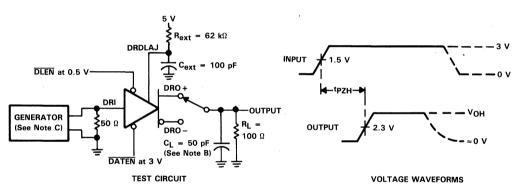


FIGURE 5. ENABLE TIMES FROM DELAY ENABLE

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 200 kHz, Duty Cycle \leq 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $z_{out} =$ 50 Ω .
 - B. C_L includes probe and jig capacitance.
 - C. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, Duty Cycle \leq 50%, $t_{\rm f} \leq$ 6 ns, $t_{\rm f} \leq$ 6 ns, $z_{\rm out} =$ 50 Ω .

PARAMETER MEASUREMENT INFORMATION

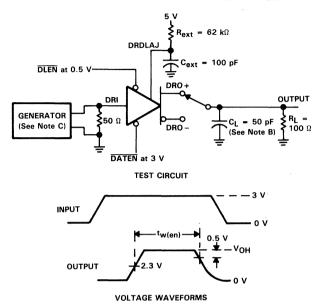


FIGURE 6. ENABLE DURATION TIME WITH DELAY ENABLE LOW

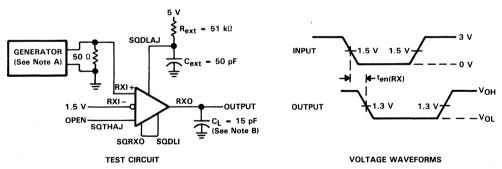


FIGURE 7. RECEIVER ENABLE (UNSQUELCH) TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 500 kHz, Duty Cycle \leq 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{OUT} =$ 50 Ω .

- B. C_L includes probe and jig capacitance.
- C. The input pulse is supplied by a generator having the following characteristics: PRR \leq 200 kHz, Duty Cycle \leq 50%, $t_{\rm f} \leq$ 6 ns, $t_{\rm f} \leq$ 6 ns, $t_{\rm cut} =$ 50 Ω .

PARAMETER MEASUREMENT INFORMATION

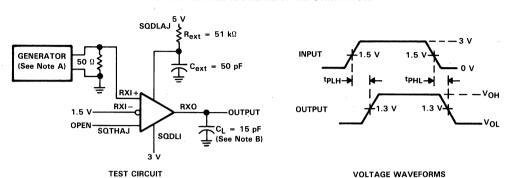


FIGURE 8. RECEIVER PROPAGATION DELAY TIMES

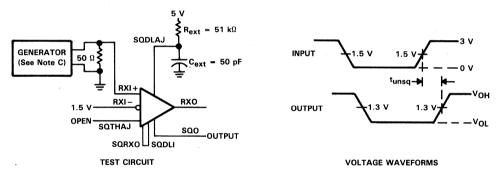


FIGURE 9. UNSQUELCH DURATION TIME

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, Duty Cycle \leq 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{OUT} =$ 50 Ω .
 - B. C_L includes probe and jig capacitance.
 - C. The input pulse is supplied by a generator having the following characteristics: PRR \leq 100 kHz, Duty Cycle \leq 50%, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{Out} =$ 50 Ω .

- Meets IBM System 360 Input/Output Interface Specifications
- Operates from Single 5-V Supply
- TTL Compatible
- 3.11-V Output at IOH = -59.3 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receiver SN75124
- Designed to Be Interchangeable With Signetics N8T23

description

The SN75123 dual line driver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN75123 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN75123 is characterized for operation from 0 °C to 70 °C.

D, J, OR N PACKAGE (TOP VIEW)

| 1 A | Пī | U ₁₆ | □vcc |
|-----|-------------|-----------------|------|
| 1B | \square^2 | 15 |] 2F |
| 1C | Ωз | 14 | ☐ 2E |
| 1D | Д4 | 13 |] 2D |
| 1E | □ 5 | 12 |] 2C |
| 1F | □ 6 | 11 | ☐ 2B |
| 1 Y | Q٦ | 10 |] 2A |
| GND | П8 | 9 | 2Y |

FUNCTION TABLE

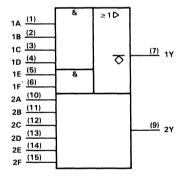
| | | INPL | JTS | OUTPUT | | |
|-----------------|-----|------|------|--------|---|---|
| Α | В | С | D | E | F | Υ |
| Н | Н | Н | Н | Х | Х | н |
| х | Χ | Х | Χ | Н | н | н |
| All other input | | | | | | L |
| ı | 100 | nbin | atio | ns | | _ |

H = high level

L = low level

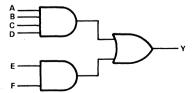
X = irrelevant

logic symbol†



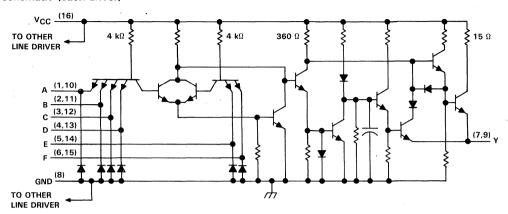
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



Texas V Instruments Copyright @ 1986, Texas Instruments Incorporated

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Output voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| D package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C, the
J package to 656 mW at 70°C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.
In the J package, SN75123 chips are glass mounted.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, VCC | 4.75 | - 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.8 | ٧ |
| High-level output current, IOH | | | -100 | `mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics, VCC = 4.75 V to 5.25 V, TA = 0 °C to 70 °C (unless otherwise noted)

| | PARAMETER | | TEST CONDITION | S | MIN | MAX | UNIT |
|--------------------|---|------------------------------|-------------------------|------------------------|-------|-------|------|
| VIK | Input clamp voltage | $V_{CC} = 5 V$, | I _I = -12 mA | | | -1.5 | V |
| V _{(BR)I} | Input breakdown voltage | $V_{CC} = 5 V$, | l _l = 10 mA | | 5.5 | | V |
| Vall | High-level output voltage | $V_{CC} = 5 V$, | V _{IH} = 2 V, | T _A = 25°C | 3.11 | | V |
| Vон | night-level output voltage | $I_{OH} = -59.3 \text{ mA},$ | See Note 3, | $T_A = 0$ °C to 70 °C | 2.9 | | · · |
| lou | High-level output current | $V_{CC} = 5 V$, | $V_{IH} = 4.5 V,$ | V _{OH} = 2 V, | - 100 | - 250 | mA |
| Іон | riigii-iever output current | $T_A = 25 ^{\circ}C$ | See Note 3 | | 100 | - 250 | IIIA |
| VOL | Low-level output voltage | $V_{IL} = 0.8 V,$ | $I_{OL} = -240 \mu A$ | See Note 3 | | 0.15 | V |
| IO(off) | Off-state output current | $V_{CC} = 0$, | V _O = 3 V | | | . 40 | μΑ |
| ΊΗ | High-level input current | $V_{J} = 4.5 \text{ V}$ | | | | 40 | μΑ |
| ΊL | Low-level input current | V _I = 0.4 V | | | -0.1 | - 1.6 | mA |
| los | Short-circuit output current [†] | $V_{CC} = 5 V$, | T _A = 25 °C | | | - 30 | mA |
| loou | Supply current, outputs high | $V_{CC} = 5.25 \text{ V},$ | All inputs at 2 V | | | 28 | m A |
| Іссн | Supply current, outputs high | Outputs open | | | | 26 | mA |
| lace | Supply current, outputs low | $V_{CC} = 5.25 \text{ V},$ | All inputs at 0.8 | V, | | 60 | mA |
| CCL | Supply current, outputs low | Outputs open | | | | | mA |

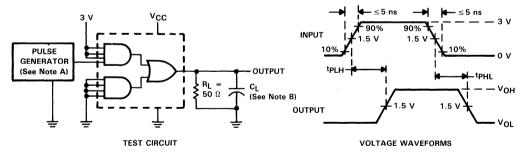
[†]Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------------------|-----|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level output | $R_L = 50 \Omega$, $C_L = 15 pF$, | | 12 | 20 | |
| tpHL Propagation delay time, high-to-low-level output | See Figure 1 | | 12 | 20 | ns |
| tpLH Propagation delay time, low-to-high-level output | $R_L = 50 \Omega$, $C_L = 100 pF$, | | 20 | 35 | |
| tpHL Propagation delay time, high-to-low-level output | See Figure 1 | | 15 | 25 | ns |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_0 \approx 50 \ \Omega$; $t_W = 200 \ ns$, duty cycle = 50%.

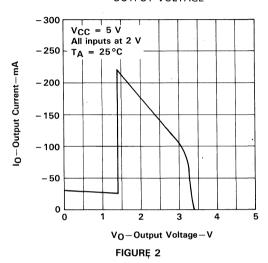
B. C_L Includes probe and jig capacitance.

FIGURE 1. SN75123 SWITCHING TIMES



TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs
OUTPUT VOLTAGE



APPLICATION INFORMATION

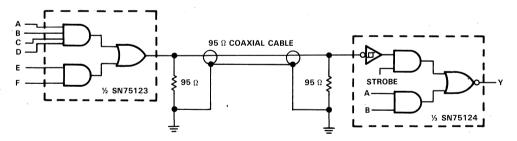


FIGURE 3. UNBALANCED LINE COMMUNICATION USING '123 AND '124

- Meets IBM System 360 Input/Output Interface Specifications
- Operates from Single 5-V Supply
- TTL Compatible
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Designed for Use with Dual Line Driver SN75123
- Designed to Be Interchangeable with Signetics N8T24

description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

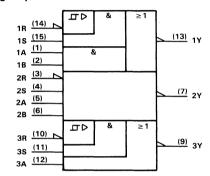
The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of -0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, will hold the output low. The third receiver has only an A input that, if high, will hold the output low.

The SN75124 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

D, J, OR N PACKAGE (TOP VIEW)

| 1A | of 1 | π | Jı | 6 | | ٧٥ | С |
|-----|--------|---|----|---|---|-----|---|
| 1B | d: | 2 | 1 | 5 | | 18 | ; |
| 2R | | 3 | 1 | 4 | | 1 F | |
| 2S | П | 1 | 1 | 3 | | 1 | • |
| 2A | D: | 5 | 1 | 2 | | 34 | |
| 2B | Пe | 3 | 1 | 1 | | 38 | , |
| 2Y | \Box | 7 | 1 | 0 | | 3F | 1 |
| GND | Ц | 3 | | 9 | ם | 3 | • |
| | | | | | | | |

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

| | INP | UTS | | OUTPUT |
|---|-----|-----|---|--------|
| Α | В‡ | R | S | Υ |
| Н | Н | X | Х | L |
| X | Х | L | Н | L |
| L | Х | H | Х | н |
| L | Χ | Х | L | н |
| Х | L | • н | Х | н |
| Х | L | Х | L | Н |

[‡]B input and last two lines of the function table are applicable to receivers 1 and 2 only.

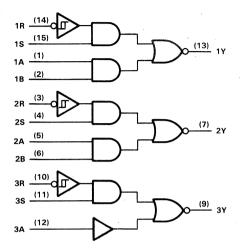
AVAILABLE OPTIONS

| | | PACKAGE | |
|---------|---------------|-------------|-------------|
| T_{A} | SMALL OUTLINE | CERAMIC DIP | PLASTIC DIP |
| | (D) | (J) | (N) |
| 0°C | | | |
| to | SN75124D | SN75124J | SN75124N |
| 70°C | | | l |

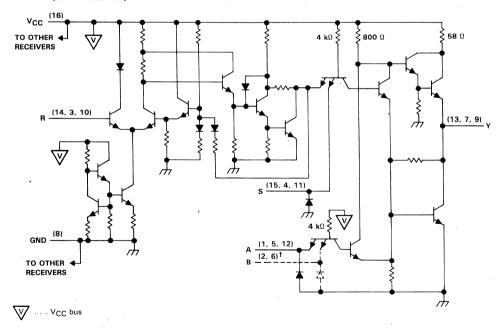
The D package is available taped and reeled. Add the suffix R to the device type (i.e., ${\sf SN75124DR}$).

TEXAS INSTRUMENTS

logic diagram (positive logic)



schematic (each receiver)



[†]B input is provided on receivers 1 and 2 only. Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | V |
|---|----|
| Input voltage: R input with VCC applied | ٧ |
| R input with VCC not applied | ٧ |
| A, B, or S input | ٧ |
| Output voltage | ٧ |
| Output current | Α |
| Continuous total dissipation See Dissipation Rating Tab | le |
| Operating free-air temperature range | Ċ |
| Storage temperature range | Ċ |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 'n |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260° | 'C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | N | VIIN | NOM | MAX | UNIT | |
|---|---------------------|---|------|-----|------|------|--|
| Supply voltage, V _{CC} | Supply voltage, VCC | | .75 | 5 | 5.25 | V | |
| High level input voltage V | A, B, or S | | 2 | | | ,, | |
| | R | | 1.7 | | |] | |
| High-level input voltage, V _{IH} Low-level input voltage, V _{IL} High-level output current, I _{OH} Low-level output current, I _{OL} | A, B, or S | | | | 0.8 | V | |
| | R | | | | 0.7 | 1 ° | |
| High-level output current, IOH | | | | | -800 | μΑ | |
| Low-level output current, IOL | | | | | 16 | mA | |
| Operating free-air temperature, T | A | | 0 | | 70 | °C | |

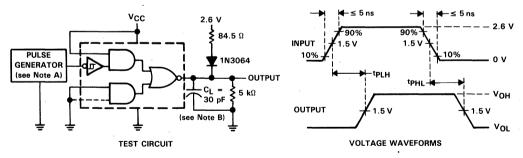
electrical characteristics, VCC = 4.75 V to 5.25 V, TA = 0 °C to 70 °C (unless otherwise noted)

| PARAMETER | | | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|------------------|---|-------------------------|------|-----|-------|--------|
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | R | $V_{CC} = 5 V$, | T _A = 25°C | 0.2 | 0.5 | | V |
| V _{IK} | Input clamp voltage | A,B, or S | $V_{CC} = 5 V$ | I _I = -12 mA | | | - 1.5 | ٧ |
| V _{(BR)I} | Input breakdown voltage | A,B, or S | V _{CC} = 5 V, | I _I = 10 mA | 5.5 | | | V |
| Vон | Higḥ-level output voltage | | $V_{IH} = V_{IH} min,$ $I_{OH} = -800 \mu A,$ | | 2.6 | | | V |
| VOL | Low-level output voltage | | $V_{IH} = V_{IH} min,$ $I_{OL} = 16 mA,$ | | | | 0.4 | V |
| t. | Input current at | | V _I = 7 V | | | | 5 | mA |
| " | I _I maximum input voltage | | V _I = 6 V, | V _{CC} = 0 | | | 5 | I IIIA |
| T | High lavel in the summer | A,B, or S | V _I = 4.5 V | | | | . 40 | ^ |
| lн | High-level input current | R | V _I = 3.11 V | | | | 1.70 | μΑ |
| ИL | Low-level input current | A,B, or S | $V_{ } = 0.4 V_{, }$ | V _{IR} = 0.8 V | -0.1 | | -1.6 | mA |
| los | Short-circuit output curren | t [†] | V _{CC} = 5 V, | T _A = 25 °C | - 50 | | - 100 | mA |
| | | All inputs = 0.8 | V | | | 72 | mA | |
| lcc | Supply current | | All inputs = 2 V | | | | 100 | |

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level output from R input | Saa Fiauma 1 | | 20 | 30 | |
| tpHL Propagation delay time, high-to-low-level output from R input | See Figure 1 | | 20 | 30 | ns |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50~\Omega$, PRR $\leq 5~MHz$, duty cycle = 50%.

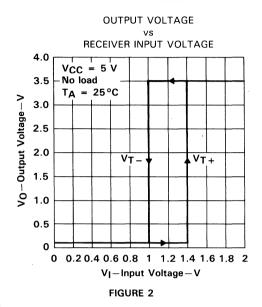
B. C_L includes probe and jig capacitance.

FIGURE 1. SN75124 SWITCHING TIMES

 $^{^{\}dagger}$ Typical value is at V_{CC} = 5 V, T_A = 25 °C. ‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

TYPICAL CHARACTERISTICS



TYPICAL APPLICATION DATA

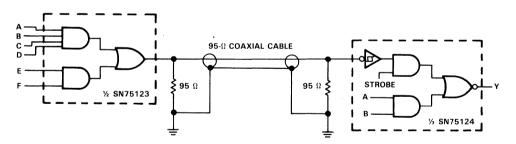


FIGURE 3. UNBALANCED LINE COMMUNICATION USING SN75123 AND SN75124

SN75125, SN75127 SEVEN-CHANNEL LINE RECEIVERS

D2239, JANUARY 1977-REVISED SEPTEMBER 1986

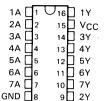
- Meets IBM 360/370 I/O Specification
- Input Resistance . . . 7 k Ω to 20 k Ω
- Output Compatible with TTL
- Schottky-Clamped Transistors
- Operates from Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on SN75127

description

The SN75125 and SN75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky-clamped transistors allow for low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

The SN75125 and SN75127 are characterized for operation from 0°C to 70°C.

SN75125 . . . D, J, OR N PACKAGE (TOP VIEW)



SN75127 . . . D, J, OR N PACKAGE

| (TOP VIEW) | | | | | | |
|------------|----------------|---------------------------------|--|--|--|--|
| 1A [| T | U ₁₆ V _{CC} | | | | |
| 2A [| 2 | 15 1Y | | | | |
| 3A [| 3 | 14 🗌 2Y | | | | |
| 4A [|]4 | 13 🗍 3Y | | | | |
| 5A [| 5 | 12 🗍 4Y | | | | |
| 6A [| 6 | 11 🗍 5Y | | | | |
| 7A [| 7 | 10 🗍 6Y | | | | |
| J DNF | 1 ₈ | 9 T 7Y | | | | |

logic symbols†

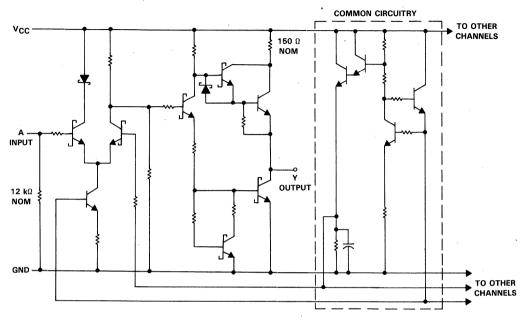
| | SN75125 | |
|----------------------------|---------|---------|
| 1A (1) | ٥ | (16) 1Y |
| 2A (2) | | (9) 2Y |
| 1A (1) 2A (2) 3A (3) | | (14) 3Y |
| 4A (4) 5A (5) 6A (6) | | (13) 4Y |
| 5A (5) | | (12) 5Y |
| 6A (6) | | (11) 6Y |
| 7A (7) | | (10) 7Y |
| | | |

| | SN75127 | |
|------------------------|---------|--------------------|
| 1A (1) | D | (15) 1Y |
| 1A (1) 2A (2) 3A | | (14) 2Y |
| 441 | | (13) (13) |
| 4A (4) (5) | | (12) 4Y (11) EV |
| 5A (5) 6A (6) | | (10) |
| 6A (7) | | (9) 7V |
| /A | | |

....

[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publicaiton 617-12.

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage range: SN75125 |
| SN75127 |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. In the J package, SN75125 and SN75127 chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25$ °C | DERATING FACTOR | T _A = 70°C |
|---------|------------------|-----------------|-----------------------|
| FACKAGE | POWER RATING | ABOVE TA = 25°C | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J . | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | A | MIN | NOM | MAX | UNIT |
|------------------------------------|---|-----|-----|------|------|
| Supply voltage, V _{CC} | | 4.5 | 5 | 5.5 | V |
| High-level input voltage, VIH | | 1.7 | | | V |
| Low-level input voltage, VIL | | | | 0.7 | V |
| High-level output current, IOH | | | | -0.4 | mA |
| Low-level output current, IOL | | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

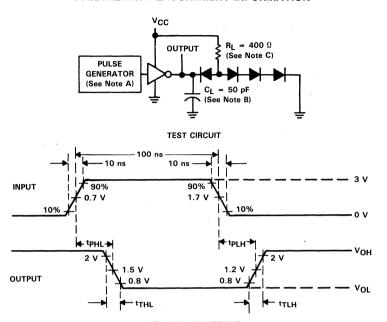
| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----|---|--|------|------------------|------|------|
| Voн | High-level output voltage | $V_{CC} = 4.5 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = -0.4 \text{ mA}$ | 2.4 | 3.1 | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = 4.5 \text{ V}, V_{IH} = 1.7 \text{ V}, I_{OL} = 16 \text{ mA}$ | | 0.4 | 0.5 | V |
| ЧН | High-level input current | $V_{CC} = 5.5 \text{ V}, V_{I} = 3.11 \text{ V}$ | | 0.3 | 0.42 | mA |
| Iμ | Low-level input current | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.15 \text{ V}$ | | | 30 | μΑ |
| los | Short-circuit output current [‡] | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | - 18 | | - 60 | mA |
| ri | Input resistance | $V_{CC} = 4.5 \text{ V}, 0 \text{ V}, \text{ or open},$ $\Delta V_{I} = 0.15 \text{ V to } 4.15 \text{ V}$ | 7 | | 20 | kΩ |
| | Cl. | $V_{CC} = 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA},$ All inputs at 0.7 V | | 15 | 25 | mA |
| lcc | Supply current | $V_{CC} = 5.5 \text{ V}, I_{OL} = 16 \text{ mA},$ All inputs at 4 V | | 28 | 47 | mA |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level output | | 7 | 14 | 25 | ns |
| tPHL Propagation delay time, high-to-low-level output | | 10 | 18 | 30 | ns |
| TPLH Ratio of propagation delay times | $R_L = 400 \Omega$, $C_L = 50 pF$, See Figure 1 | 0.5 | 0.8 | 1.3 | |
| t _{TLH} Transition time, low-to-high-level output | | 1 | 7 | 12 | ns |
| t _{THL} Transition time, high-to-low-level output | 7 | 1 | 3 | 12 | ns |

 $^{^\}dagger AII$ typical values are at VCC $\,=\,5$ V, $T_A\,=\,25\,^\circ C.$ $^\ddagger Not more than one output should be shorted at a time.$

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_0 \approx 50~\Omega$, PRR $\leq 5~MHz$. B. C_L includes probe and jig capacitance. C. All diodes are 1N3064 or equivalent.

FIGURE 1

TYPICAL CHARACTERISTICS

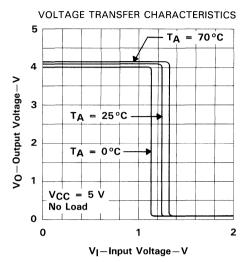
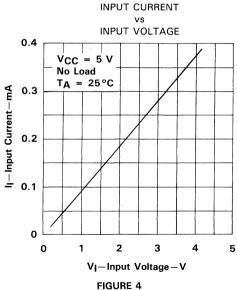


FIGURE 2



 $V_{CC} = 5.5 V$ $V_{CC} = 5 V$ 4 VCC = 4.5 V VO-Output Voltage-V 3 2

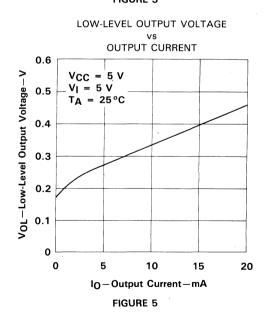
No Load TA = 25°C

0

0

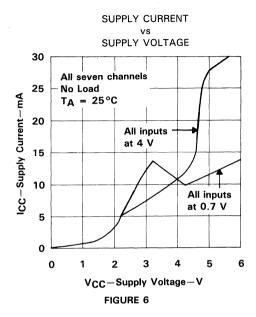
VOLTAGE TRANSFER CHARACTERISTICS

1 V_I-Input Voltage-V FIGURE 3



2

TYPICAL CHARACTERISTICS



D3405, FEBRUARY 1990

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN55ALS126 and SN75ALS126)
- Minimum Output Voltage of 3.11 V at IOH = -60 mA
- Fault-Flag Circuit Output Signals Driver Output Fault
- **Fault-Detection Current-Limit Circuit Minimizes** Power Dissipation During a Fault Condition
- **Dual Common Enable**
- Individual Fault Flags
- Designed to Replace the MC3481

description

The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at IOH = -59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75126 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

D. J. OR N PACKAGE (TOP VIEW)

| 1 Y [| Ī | U16 VCC |
|--------|---|----------|
| 1F [| 2 | 15 🗌 4Y |
| 1A 🗆 | 3 | 14 🗖 4 🖡 |
| 1,2G [| 4 | 13 🗌 4A |
| 2A 🗌 | 5 | 12 3,4G |
| 2F 🗌 | 6 | 11 🗌 3A |
| 2Y 🗌 | 7 | 10∏ 3F |
| GND [| 8 | 9 🗆 3Y |

FUNCTION TABLE

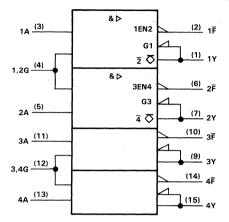
| INP | UTS | OUT | PUTS |
|-----|-----|-----|------|
| G | Α | Y | F |
| L | Х | L | Н |
| Н | Н | н | Н |
| Н | Н | s | L |

H = high level, L = low level, X = irrelevant, S = shorted to around

The SN75126 can drive a 50- Ω load as required in the IBM GA22-6974-3 specification or a 90- Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

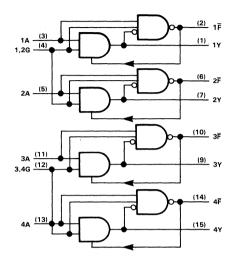
The SN75126 is characterized for operation from 0°C to 70°C.

logic symbol†

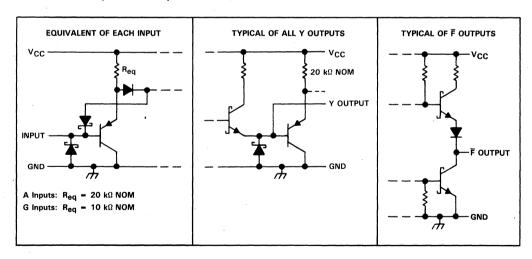


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC |
|--|
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package 300 °C |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-----|-----|-------|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.95 | V |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| High-level output current, IOH | | | -59.3 | mA |
| Operating free-air temperature, T _A | 0 | | 70 | °C |

SN75126 QUADRUPLE LINE DRIVER

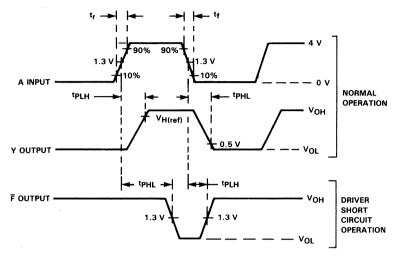
electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------|----------------------|-----|---|------------------------------|-------------------------|------|-------|--------|
| VIK | Input clamp voltage | A,G | $V_{CC} = 4.5 V,$ | I _j = -18 mA | | | - 1.5 | V |
| | High-level output | Y | $V_{CC} = 4.5 V,$ | $I_{OH} = -59.3 \text{ mA},$ | V _{IH} = 2 V | 3.11 | | |
| Vон | • | Υ | $V_{CC} = 5.25 \text{ V},$ | $I_{OH} = -41 \text{ mA},$ | V _{IH} = 2 V | 3.9 | | V |
| | voltage | F | $V_{CC} = 4.5 V,$ | $I_{OH} = -400 \mu A$ | V _{IH} = 2 V | 2.5 | | |
| | | Y | $V_{CC} = 5.5 V$, | $I_{OL} = -240 \mu A$ | V _{IL} = 0.8 V | | 0.15 | |
| \/-· | Low-level output | Υ | $V_{CC} = 5.95 V$, | $I_{OL} = -1 \text{ mA},$ | $V_{IL} = 0.8 V$ | | 0.15 | v |
| VOL | VOL voltage | F | $V_{CC} = 4.5 \text{ V},$ $V_{IH} = 2 \text{ V}$ | I _{OL} = 8 mA, | Y at 0 V, | | 0.5 | V |
| | Off-state output | Υ | $V_{CC} = 4.5 \text{ V},$ | V _I = 0, | V _O = 3.11 V | | 100 | μΑ |
| IO(off) | current | Y | $V_{CC} = 0$, | V ₁ = 0, | V _O = 3.11 V | | 200 | μΑ |
| | Input current | Α | V _{CC} = 4.5 V, | V: - 5 5 V | | | 100 | μΑ |
| 11 | input current | G | VCC = 4.5 V, | VI = 5.5 V | | | 200 | μΑ |
| 1 | High-level input | Α | $V_{CC} = 4.5 \text{ V},$ | V ₁ = 2.7.V | | | 20 | μΑ |
| ΙΗ | current | G | VCC = 4.5 V, | V = 2.7·V | | | 40 | μΛ |
| I _{IL} | Low-level input | Α | $V_{CC} = 5.95 \text{ V},$ | V1 - 0.4 V | | | - 250 | μΑ |
| 'IL | current | G | VCC = 3.33 V, | V = 0.4 V | | | - 500 | μ |
| | | Υ | $V_{CC} = 5.5 V,$ | | $V_{IH} = 2.7 V$ | | - 5 | |
| loo | Short-circuit output | F | $V_{CC} = 5.5 V,$ | $V_0 = 0$ | | - 15 | - 100 | mA |
| los | current | Υ | $V_{CC} = 5.95 V$, | $V_0 = 0$, | $V_{IH} = 2.7 V$ | | - 5 | 1111/4 |
| | | F | $V_{CC} = 5.95 V$, | $V_0 = 0$ | | - 15 | - 110 | |
| loou | Supply current, | | $V_{CC} = 5.5 V,$ | No load, | V _{IH} = 2 V | | 70 | mA |
| Іссн | all outputs high | | $V_{CC} = 5.95 V$, | No load, | V _{IH} = 2 V | | 80 | 1114 |
| loci | Supply current, | | $V_{CC} = 5.5 V,$ | No load, | $V_{IL} = 0.8 V$ | | 55 | mA |
| ICCL | Y outputs low | | $V_{CC} = 5.95 V$, | No load, | $V_{IL} = 0.8 V$ | | 70 ' | |

switching characteristics at $T_A = 25$ °C

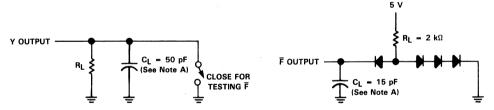
| PARAMETER | | FROM | то | TEST CONDITIONS | MIN . | MAX | UNIT |
|--------------|---|----------|----|---|-------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | | V _{CC} = 4.5 V to 5.5 V, | | 40 | ns |
| tPHL | Propagation delay time, high-to-low-level output | A | Y | $R_L = 50 \Omega$, $C_L = 50 pF$, $V_{H(ref)} = 3.11 V$, | | 37 | ns |
| tPLH tPHL | Ratio of propagation delay times | | | See Figures 1 and 2 | 0.3 | 3 | |
| tPLH | Propagation delay time, low-to-high-level output | А | _ | $V_{CC} = 5.25 \text{ V to } 5.95 \text{ V},$ $R_L = 90 \Omega,$ $C_L = 50 \text{ pF},$ | | 45 | ns |
| tPHL | Propagation delay time, high-to-low-level output | ` | ' | V _{H(ref)} = 3.9 V See Figures 1 and 2 | | 45 | ns |
| tPLH | Propagation delay time, low-to-high-level output | A | F | $V_{CC} = 5 \text{ V},$ $R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$ | | 60 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | | See Figures 1 and 2 | | 100 | ns |

PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{r} \leq$ 7 ns, $t_{r} \leq$ 8 ns, $t_{r} \leq$ 9 ns, t_{r}

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



NOTE A: CL includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

SN75128, SN75129 EIGHT-CHANNEL LINE RECEIVERS

D2305 JANUARY 1977-REVISED SEPTEMBER 1986

| Meets IBM 360/370 I/O Specification | DW, J, OR N PACKAGE |
|--|----------------------------------|
| • Input Resistance 7 k Ω to 20 k Ω | (TOP VIEW) |
| Output Compatible With TTL | 1S/1S* ☐ 1 |
| Schottky-Clamped Transistors | 2A 🛚 3 18 🖸 2Y |
| Operates From a Single 5-Volt Supply | 3A |
| High Speed Low Propagation Delay | 5A 🛮 6 15 🗒 5Y |
| Ratio Specification tpLH/tTHL | 6A 🛮 7 14 🗎 6Y 7A 🗒 8 13 🖯 7Y |
| Common Strobe for Each Group of Four Receivers | 8A |

^{*}S and \$\overline{S}\$ for SN75128 and SN75129, respectively

description

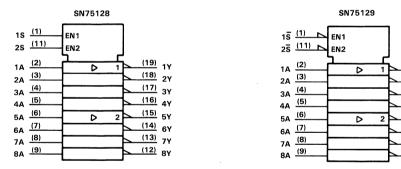
SN75128 . . . Active-High Strobes

SN75129 . . . Active-Low Strobes

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



(19)

(18)

(17)

(16)

(15)

(14) 6Y

(12)

(13) 7Y

37

logic diagrams (positive logic) SN75128 SN75129 (<u>18)</u> 2Y (<u>17)</u> 3Y 2S (11) 25 (11) (14) 6Y (<u>14)</u> 6Y (<u>13)</u> 7Y schematic (each driver) 150 Ω NOM INPUT OUTPUT **17 k**Ω NOM **12 k**Ω NOM SN75129 GND INPUT ONE OF TWO COMMON CIRCUITRY TO THREE OTHER TO SEVEN CHANNELS OTHER CHANNELS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| A input voltage range |
| Strobe input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | | DERATING FACTOR ABOVE TA = 25°C | |
|---------|---------|---------------------------------|--------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MI | N NOM | MAX | UNIT |
|--|---|----|-------|------|------|
| Supply voltage, V _{CC} | | 4. | 5 5 | 5.5 | V |
| High level in the college Ave. | A | 1. | 7 | | V |
| High-level input voltage, VIH | S | | 2 | | 1 ° |
| Low-level input voltage, V _{IL} | A | | | 0.7 | |
| | S | | | 0.7 |] |
| High-level output current, IOH | | | | -0.4 | mA |
| Low-level output current, IOL | | | | 16 | mA |
| Operating free-air temperature, TA | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----|--|----------------------|---|--|------|------------------|-------|------|
| VoH | High-level output v | oltage | | $V_{CC} = 4.5 \text{ V}, V_{IL} = 0.7 \text{ V}, I_{OH} = -0.4 \text{ mA}$ | 2.4 | 3.1 | | V |
| VOL | Low-level output vo | oltage | | $V_{CC} = 4.5 \text{ V}, V_{IH} = 1.7 \text{ V}, I_{OL} = 16 \text{ mA}$ | | 0.4 | 0.5 | V |
| VIK | Input clamp voltage |) | s | $V_{CC} = 4.5 \text{ V}, \text{ I}_{I} = -18 \text{ mA}$ | | | - 1.5 | V |
| Α Α | | Α | $V_{CC} = 5.5 \text{ V}, V_{\parallel} = 3.11 \text{ V}$ | | 0.3 | 0.42 | mA | |
| ΉΗ | I _{IH} High-level input current | | S | $V_{CC} = 5.5 \text{ V}, V_{I} = 2.7 \text{ V}$ | | | 20 | μΑ |
| 1 | lu low-level input current 🛏 | | Α | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.15 \text{ V}$ | | | 30 | μΑ |
| 'IL | | | S | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.4 \text{ V}$ | | | -0.4 | mA |
| los | Short-circuit output | current [‡] | | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | - 18 | | - 60 | mA |
| rj | Input resistance | | | $V_{CC} = 4.5 \text{ V}$, 0, or open; $\Delta V_{I} = 0.15 \text{ V}$ to 4.15 V | 7 | | 20 | kΩ |
| | SN751 | | 28 | V _{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 0.7 V | | 19 | 31 | |
| 1 | Supply current | SN751 | 29 | V _{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 0.7 V | | 19 | 31 | mA |
| Icc | Supply current | SN751 | 28 | V _{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 4 V | | 32 | 53 | IIIA |
| | SN751. | 29 | V _{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 4 V | | 32 | 53 | | |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

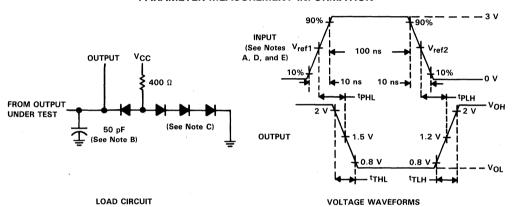


[‡]Not more than one output should be shorted at a time.

switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | | TEST CONDITIONS | SN75128 | | | SN75129 | | | UNIT |
|--|-----|------------------------|---------|-----|-----|---------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | וואוט |
| tpLH Propagation delay time, low-to-high-level output | A | | 7 | 14 | 25 | 7 | 14 | 25 | ns |
| tpHL Propagation delay time, high-to-low-level output | 7 ^ | | 10 | 18 | 30 | 10 | 18 | 30 | ns |
| tpLH Propagation delay time, low-to-high-level output | S | $R_{l} = 400 \Omega$ | | 26 | 40 | | 20 | 35 | ns |
| tphl Propagation delay time, high-to-low-level output | 7 3 | $C_1 = 50 \text{ pF},$ | | 22 | 35 | | 16 | 30 | ns |
| TPLH to the transfer of the tr | Α | See Figure 1 | 0.5 | 0.8 | 1.3 | 0.5 | 0.8 | 1.3 | |
| t _{TLH} Transition time, low-to-high-level output | 1 | 1 | 7 | 12 | 1 | 7 | 12 | ns | |
| t _{THL} Transition time, high-to-low-level output | | 1 | 3 | 12 | 1 | 3 | 12 | ns | |

PARAMETER MEASUREMENT INFORMATION



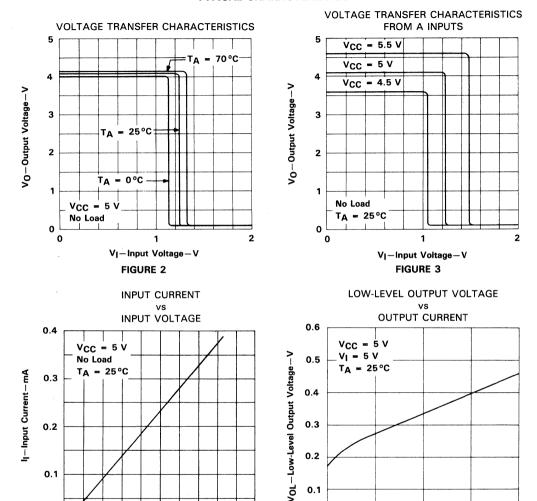
NOTES: A. Input pulses are supplied by a generator having the following characteristics: $Z_0 = 50 \Omega$, PRR $\leq 5 \text{ MHz}$.

- B. Includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. The strobe inputs of SN75129 are in-phase with the output.
- E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

FIGURE 1

TYPICAL CHARACTERISTICS

ŕ





0

0

1

2

V_I-Input Voltage-V

FIGURE 4

3

4

0

0

5

10

IO-Output Current-mA

FIGURE 5

15

20

SN75130 QUADRUPLE LINE DRIVER

D3406, FEBRUARY 1990

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also see SN75ALS130)
- Minimum Output Voltage of 3.11 V at IOH = −60 mA
- Fault-Flag Circuit Output Signals Driver Output Fault
- Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition
- Common Enable and Common Fault Flag
- Designed to Be an Improved Replacement for the MC3485

description

The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at $I_{OH} = -59.3$ mA) over the recommended ranges of supply voltage (4.5 V to 5.5 V) and temperature (0 °C to 70 °C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75130 is compatible with standard TTL logic and supply voltages.

D, J, OR N PACKAGE (TOP VIEW)

| 1Y | Пī | U 16 | □ vcc |
|-----|-------------|-------------|-------|
| 1W | \square^2 | 15 |] 4Y |
| 1A | \square 3 | 14 |] 4W |
| G | \Box 4 | 13 |] 4A |
| 2A | □ 5 | 12 | ΡĒ |
| 2W | □ 6 | 11 |] 3A |
| 2Y | ٦, | 10 | ⊒ зw |
| GND | 8 | 9 | □ 3Y |
| | | | |

FUNCTION TABLE

| INP | JTS | OUTPUTS | | | | | |
|-----|------------------|---------|---|---|--|--|--|
| G† | G [†] A | | F | w | | | |
| L | Х | L | Н | Н | | | |
| x | L | L | Н | Н | | | |
| Н | Н | н | Н | L | | | |
| н | Н | s | L | н | | | |

H = high level, L = low level, X = irrelevant, S = shorted to around

[†]G and F are common to the four drivers. If any of the four Y outputs is shorted, the Fault-Flag will respond.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

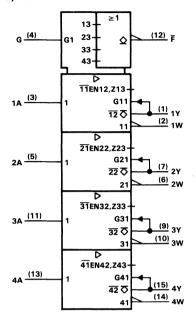
The SN75130 can drive a $50-\Omega$ load as required in the IBM GA22-6974-3 specification or a $90-\Omega$ load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75125, SN75127, SN75128, or SN75129 line receivers.

The SN75130 is characterized for operation from 0°C to 70°C.

IMPACT is a trademark of Texas Instruments Incorporated

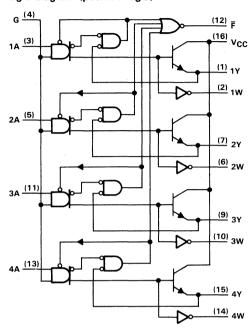
SN75130 QUADRUPLE LINE DRIVER

logic symbol†

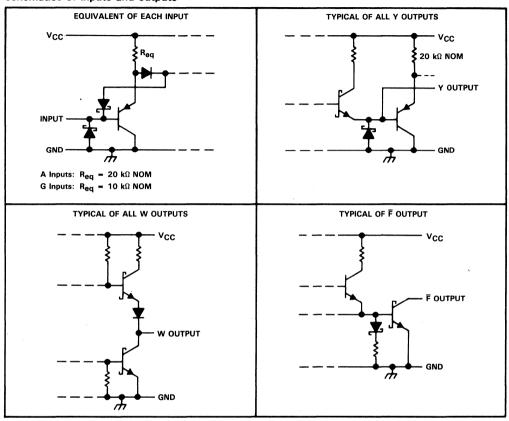


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC | | | | | . 7 V | |
|--|----|----|----|------|--------|--|
| Input voltage | | | | | | |
| Continuous total dissipation at (or below): D package | | | | 95 | 0 mW | |
| J package | | | | 102 | 25 mW | |
| N package | ٠. | | | 115 | 60 mW | |
| Operating free-air temperature range, TA | | | ٥٥ | C to | 70°C | |
| Storage temperature range | | 65 | °C | to | 150°C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | | ٠. | | | 260°C | |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: I nackage | | | | | 300 °C | |

NOTE 1: For operation above 15 °C free-air temperature, derate D package to 608 mW at 70 °C at the rate of 7.6 mW/°C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|-----|-----|-------|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.95 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | V |
| High-level output current, IOH | | | -59.3 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

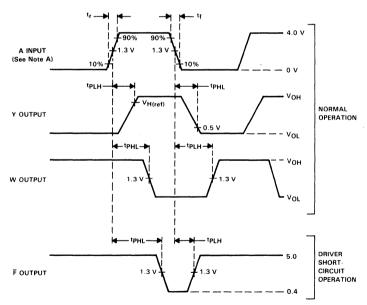
electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT | |
|-----------------|---------------------------|-----|---|------------------------|------|-------|-------|--|
| VIK | Input clamp voltage | A,G | I _I = -18 mA | | | - 1.5 | V | |
| V _{OH} | High-level output voltage | Υ | $V_{CC} = 4.5 \text{ V}, I_{OH} = -59.3 \text{ mA},$ | V _{IH} = 2 V | 3.11 | | | |
| | | Υ | $V_{CC} = 5.25 \text{ V}, I_{OH} = -41 \text{ mA},$ | V _{IH} = 2 V | 3.9 | | V | |
| | | W | $V_{CC} = 4.5 \text{ V}, I_{OH} = -400 \mu\text{A},$ | V _{IH} = 2 V | 2.5 | | | |
| | | Υ | $V_{CC} = 5.5 \text{ V}, I_{OL} = -240 \mu\text{A},$ | $V_{IL} = 0.8 V$ | | 0.15 | | |
| \/a. | Low-level output voltage | Υ | $V_{CC} = 5.95 \text{ V}, I_{OL} = -1 \text{ mA},$ | $V_{IL} = 0.8 V$ | | 0.15 | V | |
| VOL | Low-level output voltage | F | $V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA},$ | Y at 0 V | | 0.5 | V | |
| | | W | $V_{CC} = 4.5 \text{ V}, I_{OL} = 8 \text{ mA}$ | | | 0.5 | | |
| 1 | Off-state output current | Υ | $V_{CC} = 4.5 \text{ V}, V_{IL} = 0,$ | $V_0 = 3.11 \text{ V}$ | | 100 | μΑ | |
| IO(off) | On-state output current | Υ | $V_{CC} = 0$, $V_{IL} = 0$, | $V_0 = 3.11 \text{ V}$ | | 200 | μА | |
| Іон | High-level output current | F | $V_{CC} = 5.95 \text{ V}, V_{OH} = 5.95 \text{ V}$ | | | 100 | μΑ | |
| 1. | Input current | Α | V _{CC} = 4.5 V, V _{IH} = 5.5 V | | | 100 | μΑ | |
| łį . | | G | vCC = 4.9 v, vIH = 5.5 v | | | 400 | | |
| 1 | High-level input current | Α | V _{CC} = 4.5 V, V _{IH} = 2.7 V | | | 20 | μΑ | |
| ЧH | High-level input current | G | VCC = 4.5 V, VIH = 2.7 V | | | 80 | μΑ | |
| la. | Low-level input current | Α | VCC = 5.95 V, V _{II} = 0.4 V | | | 250 | μΑ | |
| ᆜ | Low-level input current | G | VCC = 5.95 V, V L = 0,4 V | | | -1000 | μΑ | |
| | | Υ | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | | | -5 | | |
| laa | Short-circuit output | W | vCC = 9:9 v' vO = 0 | | -15 | - 100 | mA | |
| los | | Υ | $V_{CC} = 5.95 \text{ V}, V_{O} = 0 \text{ V}$ | | | -5 | IIIA | |
| | | W | VCC = 5.95 V, VO = 0V | | - 15 | - 110 | | |
| loou | Supply current, all | | $V_{CC} = 5.5 \text{ V}, V_{I} = 2 \text{ V}$ | | | 75 | mA | |
| Іссн | outputs, high | | $V_{CC} = 5.95 \text{ V}, V_{I} = 2 \text{ V}$ | | 85 | ША | | |
| | Supply current, | | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.8 \text{ V}$ | | | 55 | - m A | |
| ICCL | Y outputs low | | $V_{CC} = 5.95 \text{ V}, V_{I} = 0.8 \text{ V}$ | | 70 | mA | | |

switching characteristics over recommended operating free-air temperature range

| | PARAMETER | FROM | TO | TEST CONDITIONS | MIN | MAX | UNIT | |
|------------------|---|------|-----|---|---|-----|------|----|
| ^t PLH | Propagation delay time, low-to-high-level output | | A Y | $ \begin{array}{c} V_{CC} = 4.5 \; \text{V to } 5.5 \; \text{V}, \\ R_L = 50 \; \Omega, \qquad C_L = 50 \; \text{pF}, \\ V_{H(ref)} = 3.11 \; \text{V}, \text{Input } f = 1 \; \text{MHz}, \\ \text{See Figures 1 and 2} \end{array} $ | | 40 | ris | |
| tPHL | Propagation delay time, high-to-low-level output | A | | | | 37 | ns | |
| tPLH tPHL | Ratio of propagation delay times | | | | 0.3 | 3 | | |
| tPLH | Propagation delay time, low-to-high-level output | A | Y | $\begin{array}{llllllllllllllllllllllllllllllllllll$ | 1 | 45 | ns | |
| tPHL | Propagation delay time, high-to-low-level output |] ^ | | | | 45 | ns | |
| ^t PLH | Propagation delay time, low-to-high-level output | | A W | 1 30 | $V_{CC} = 5 \text{ V},$ $R_L = 2 \text{ k}\Omega,$ $C_L = 15 \text{ pF},$ | | 45 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | | See Figures 1 and 2 | | 28 | ns | |
| ^t PLH | Propagation delay time, low-to-high-level output | A | Ē | $V_{CC}=5$ V, $R_L=2$ $k\Omega$, $C_L=15$ pF, See Figures 1 and 2 | | 60 | ns | |
| tPHL | Propagation delay time, high-to-low-level output | | | | | 100 | ns | |

PARAMETER MEASUREMENT INFORMATION

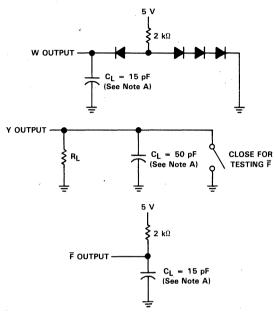


NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $t_{out} = 50 \Omega$.

FIGURE 1. INPUT AND OUTPUT VOLTAGE WAVEFORMS



PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and stray capacitance.

FIGURE 2. SWITCHING CHARACTERISTICS LOAD CIRCUITS

SN75136 QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUTS

D2291, JANUARY 1977-REVISED SEPTEMBER 1986

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- Driver Has 40-mA Current Sink Capability
- Designed to Be Functionally Interchangeable with Signetics N8T26, also Called 8T26

description

The SN75136 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have 3-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of $200~\mu A$.

The SN75136 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (DRIVER)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| D | DE | В |
| L | Н | Н |
| Н | Н | L |
| Х | L | z |

FUNCTION TABLE (RECEIVER)

| INF | UTS | OUTPUT |
|-----|-----|--------|
| В | RE | R |
| L | L | Н |
| н | L | L |
| x | Н | z |

H = high level

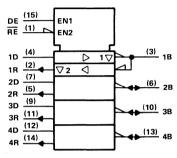
L = low level

X = irrelevant

Z = high impedance

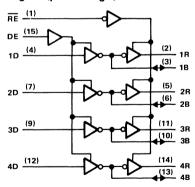
D, J, OR N PACKAGE (TOP VIEW) RE 1 716 VCC 15 DE 1R Γ 14 T 4R 1B [13 4B 1D [12 4D 2R [5 11 🛚 3R 2B ∏6 2D 10 T 3B ⊓ зb GND ∏8 9

logic symbol†

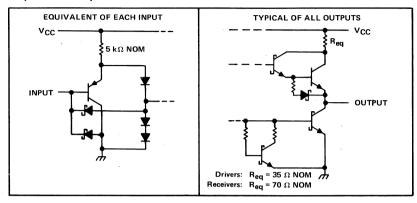


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schématics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | _ | DERATING FACTOR | |
|---------|--------------|---------------------|--------------|
| | POWER RATING | ABOVE $T_A = 25$ °C | POWER RATING |
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|--------------|------|------|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | B, D, DE, RE | 2 | | | ٧ |
| Low-level input voltage, VIL | B, D, DE, RE | | | 0.85 | ٧ |
| High-level output current, IOH | Driver, B | | - 10 | | mA |
| High-level output current, IOH | Receiver, R | | | -2 | IIIA |
| Laur laval autout aurent la | Driver, B | | | 40 | mA |
| Low-level output current, IOL | Receiver, R | | | 16 | IIIA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT |
|-----|---|-----------|----------------------------|--|------|------------------|------|------|
| VIK | Input clamp voltage | B,D,DE,RE | $I_1 = -5 \text{ mA}$ | | | | - 1 | V |
| Va | High-level output voltage | В | V _{IH} = 2 V, | $V_{IL} = 0.85 \text{ V}, I_{OH} = -10 \text{ mA}$ | 2.6 | 3.1 | | V |
| Vон | High-level output voltage | R | $V_{IL} = 0.85 \text{ V},$ | $I_{OH} = -2 \text{ mA}$ | 2.6 | 3.1 | | V |
| VOI | Low-level output voltage | В | $V_{IH} = 2 V$, | I _{OL} = 40 mA | | | 0.5 | V |
| VOL | | R | $V_{IH} = 2 V$, | $V_{IL} = 0.85 \text{ V}, I_{OL} = 16 \text{ mA}$ | | | 0.5 | 1 |
| lo- | Off-state (high-impedance | B,R | DE at 0.85 V, | \overline{RE} at 2 V, $V_0 = 2.6 \text{ V}$ | | | 100 | ^ |
| loz | state) output current | R | RE at 2 V, | $V_0 = 0.5 V$ | | | -100 | μΑ |
| ΊΗ | High-level input current | D,DE,RE | $V_1 = 5.25 \text{ V}$ | | | | 25 | μΑ |
| IIL | Low-level input current | B,D,DE,RE | V _I = 0.4 V | | | | -200 | μΑ |
| 1 | Short-circuit output current [‡] | В | V E 2E V | | - 50 | | -150 | mA |
| los | Short-circuit output current | R | V _{CC} = 5.25 V | | - 30 | | - 75 | IIIA |
| Icc | Supply current | | $V_{CC} = 5.25 V$, | No load | | | 87 | mA |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

| | PARAMETER | | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|-----|------|--------------------------------------|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | В | R | C _L = 30 pF, See Figure 1 | | 8 | 18 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | " | CL = 30 pr, See Figure 1 | | 7 | 14 | 115 |
| ^t PLH | Propagation delay time, low-to-high-level output | D | В | C _L = 300 pF,See Figure 2 | | 11 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | " | CL = 300 pr, see rigure 2 | | 16 | 24 | 113 |
| tPLZ | Output disable time from low level | RE | R | C _I = 30 pF, See Figure 3 | | 16 | 24 | ns |
| tPZL | Output enable time to low level | 111 | l '` | CL = 30 pr, See rigure 3 | | 15 | 30 | 113 |
| tPLZ | Output disable time from low level | DF | В | C _L = 300 pF,See Figure 4 | | 9 | 24 | ns |
| tPZL | Output enable time to low level | DE | " | CL = 500 pi ,See Figure 4 | | 31 | 38 | 113 |

 $^{^\}dagger All$ typical values are at T $_A=25\,^\circ C$ and V $_{CC}=5$ V. $^\ddagger Only$ one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION 2.6 V Vcc TEST POINT ≸92Ω PULSE CIRCUIT (See Note D) В R GENERATOR UNDER (See Note A) DE TEST (See Note B) D (all) $C_1 = 30 pF$ RE 1.3 kΩ (See Note C) OPEN GND **TEST CIRCUIT** - ≤5 ns ≤5 ns 90% 90% INPUT 1.5 \ 10% tpH1 OUTPUT 1.5 V VOL **VOLTAGE WAVEFORMS**

FIGURE 1. PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT

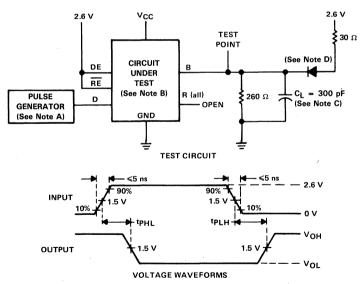


FIGURE 2. PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

- NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR \leq 10 MHz, duty cycle = 50%, $Z_0 \approx$ 50 Ω .
 - B. All inputs and outputs not shown are open.
 - C. C_L includes probe and jig capacitance.
 - D. All diodes are 1N916 or 1N3064.



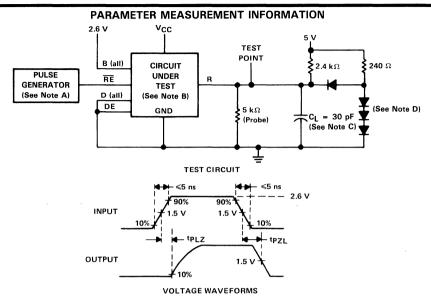


FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

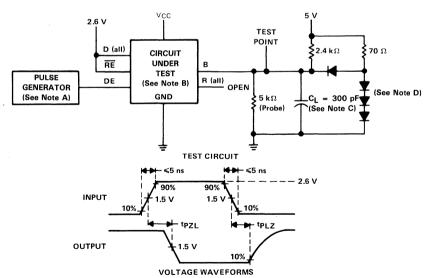


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

- NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR \leq 5 MHz, duty cycle = 50%, Z₀ \approx 50 Ω .
 - B. All inputs and outputs now shown are open.
 - $\text{C. } \text{C}_{\text{L}}$ includes probe and jig capacitance.
 - D. All diodes are 1N916 or 1N3064.



- Single 5-V Supply
- ± 100 mV Sensitivity
- For Application As: Single-Ended Line Receiver Gated Oscillator Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications
- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

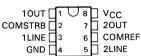
description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.5 V, making it possible to optimize noise immunity for a given system design. Due to their low input current (less than $100 \, \mu A$), they are ideally suited for party-line (bus-organized) systems.

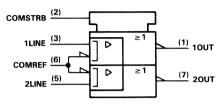
The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected.

The SN75140 and SN75141 are characterized for operation from 0°C to 70°C.

D, JG, OR P PACKAGE (TOP VIEW)

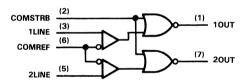


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

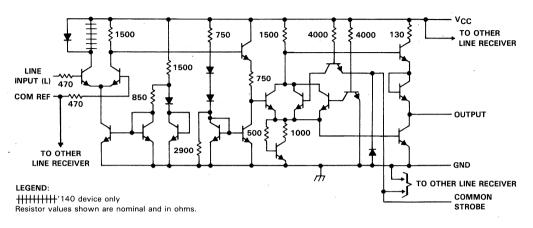


FUNCTION TABLE (EACH RECEIVER)

| LINE INPUT | STROBE | OUTPUT |
|----------------------------------|--------|--------|
| \leq V _{ref} - 100 mV | L | Н |
| ≥ V _{ref} + 100 mV | X | L |
| × | н · | L |

H=high level, L=low level, X=irrelevant

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Reference input voltage, V _{ref} |
| Line input voltage range with respect to ground |
| Line input voltage with respect to V _{ref} ±5 V |
| Strobe input voltage |
| Continuous total power dissipation |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C |

NOTE 1: Unless otherwise specified, voltage values are with respect to network terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------------------------|-----|-----------------------|------|
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | ٧ |
| Reference input voltage, V _{ref} | 1.5 | | 3.5 | ٧ |
| High-level line input voltage, VIH(L) | V _{ref} + 0.1 | , | V _{CC} - 1 | ٧ |
| Low-level line input voltage, VIL(L) | 0 | | V _{ref} -0.1 | ٧ |
| High-level strobe input voltage, VIH(S) | 2 | | 5.5 | ٧ |
| Low-level strobe input voltage, V _{IL(S)} | 0 | | 0.8 | ٧ |



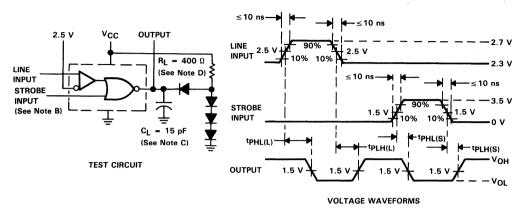
electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|---------------------|-----------------------------|---------------------|---|------|------------------|------|------|
| V _{IK} (S) | Strobe input clamp vo | Itage | I _I (S) = -12 mA | | | -1.5 | V |
| Voн | High-level output volta | ige | $V_{IL(L)} = V_{ref} - 100 \text{ mV}, V_{IL(S)} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}$ | 2.4 | | V | |
| VOL | Low-level output volta | ae | $V_{IH(L)} = V_{ref} + 100 \text{ mV}, V_{IL(S)} = 0.8 \text{ V},$ $I_{OL} = 16 \text{ mA}$ | | | 0.4 | v |
| - OL | , | | $V_{IL(L)} = V_{ref} - 100 \text{ mV}, V_{IH(S)} = 2 \text{ V},$ $I_{OL} = 16 \text{ mA}$ | | | 0.4 | |
| | Strobe input current | Strobe | | I | | 1 | |
| l _l (S) | at maximum input voltage | Com strb | $V_{I(S)} = 5.5 \text{ V}$ | | | 2 | mA |
| | | Strobe | $V_{I(S)} = 2.4 \text{ V}$ | | | 40 | |
| | High-level | Com strb | - 1(0) | | | 80 |] |
| lн | · · | Line input | $V_{I(L)} = 3.5 \text{ V}, V_{ref} = 1.5 \text{ V}$ | | 35 | 100 | μΑ |
| | input current | Reference | V 0 V 2 E V | | 35 | 100 | |
| | | Com ref | $V_{I(L)} = 0, V_{ref} = 3.5 V$ | | 200 | | |
| | | Strobe | $V_{ (S)} = 0.4 \text{ V}$ | | | -1.6 | mA |
| | Low-level | Com strb | VI(S) - 0.4 V | | | -3.2 | IIIA |
| IIL | | Line input | $V_{I(L)} = 0, V_{ref} = 1.5 V$ | | | - 10 | |
| | input current | Reference | 15 V V - 0 | | | - 10 | μΑ |
| | | Com ref | $V_{I(L)} = 1.5 \text{ V}, V_{ref} = 0$ | | | - 20 | |
| los | Short-circuit output cu | ırrent [‡] | V _{CC} = 5.5 V | - 18 | | - 55 | mA |
| Іссн | Supply current, output | t high | $V_{I(S)} = 0, V_{I(L)} = V_{ref} - 100 \text{ mV}$ | | 18 | 30 | mA |
| ICCL | Supply current, output | low | $V_{I(S)} = 0, V_{I(L)} = V_{ref} + 100 \text{ mV}$ | | 20 | 35 | mA |

 $^{^{\}dagger}$ All typical values are at VCC $\,=\,5$ V, $T_{A}\,=\,25\,^{\circ}C.$ ‡ Only one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $V_{ref} = 2.5 \text{ V}$, $T_A = 25 ^{\circ}C$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------|-------------------------------------|--|-----|-----|-----|-------|
| + | Propagation delay time, low-to- | | | 22 | 35 | |
| tPLH(L) | high-level output from line input | | | | | ns |
| | Propagation delay time, high-to- | | | 22 | 30 | 115 |
| tPHL(L) | low-level output from line input | $C_L = 15$ pF, $R_L = 400 \Omega$, See Figure 1 | | 22 | 30 | İ |
| | Propagation delay time, low-to- | | | 12 | 22 | |
| tPLH(S) | high-level output from strobe input | | | 12 | 22 | ns |
| | Propagation delay time, high-to- | | | 8 | 15 | 1 115 |
| tPHL(S) | low-level output from strobe input | | | | 15 | |

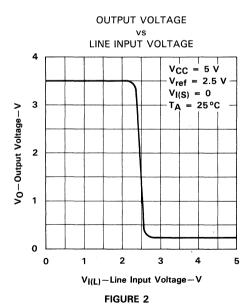


NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z₀ = 50 Ω .

- B. Unused strobes are to be grounded.
- C. C_L includes probe and jig capacitance.
- D. All diodes are 1N3064.

FIGURE 1

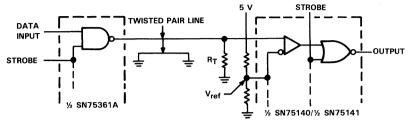
TYPICAL CHARACTERISTICS



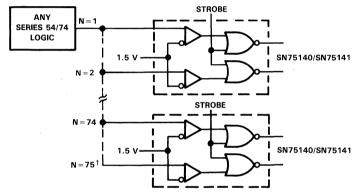


APPLICATION INFORMATION

line receiver

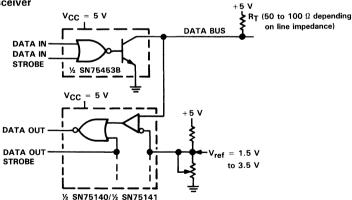


high fan-out from standard TTL gate



†Although most Series 54/74 circuits have a 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

dual bus transceiver

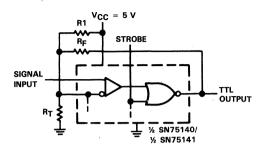


Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package and only one power supply is required (+5 V). Data In and Data Out terminals are TTL compatible.

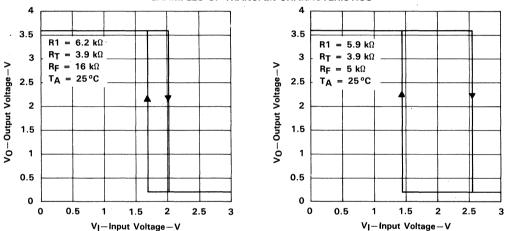


APPLICATION INFORMATION

schmitt trigger



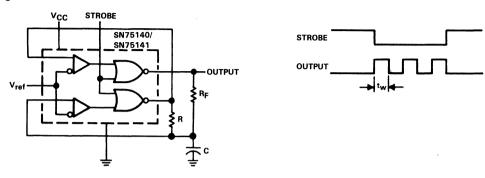
EXAMPLES OF TRANSFER CHARACTERISTICS



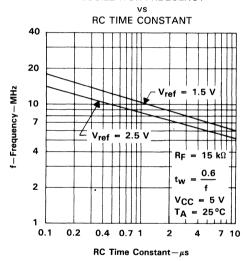
Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

APPLICATION INFORMATION

gated oscillator



OSCILLATOR FREQUENCY



SN75146 DUAL DIFFERENTIAL LINE RECEIVER

D2609, FEBRUARY 1986

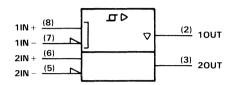
- Meets EIA Standards RS-422-A and RS-423-A
- Meets EIA Standards RS-232 and CCITT V.28 with External Components
- Meets Federal Standards 1020 and 1030
- Built-in 5-MHz Low-Pass Filter
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- 8-Pin Dual-In-Line Package
- Pinout Compatible with the μA9637 and μA9639

description

The SN75146 is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A. The receiver is designed to have a constant impedance with input voltages of ± 3 volts to ± 25 volts allowing it to meet the requirements of EIA standard RS-232-C and CCITT recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kilohertz, and has a built-in 5-megahertz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-volt power supply and is supplied in both the 8-pin dual-in-line and small outline packages.

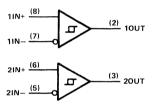
The SN75146 is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

logic symbol[†]

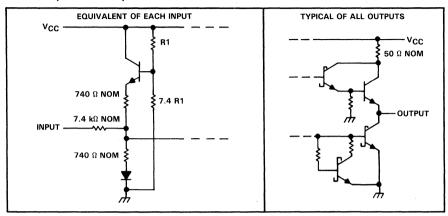


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) Input voltage | ±25 V |
|---|-------------|
| Output voltage (see Note 1) | |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note | |
| D package | 725 mW |
| JG package | 825 mW |
| P package | 1000 mW |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P pac | kage 260°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C, the D package to 464 mW at 70°C at the rate of 5.8 mW/°C, and the P package to 640 mW at 70°C at the rate of 8 mW/°C. The SN75146 chips are glass mounted in the JG package.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | ٧ |
| Common-mode input voltage, V _{IC} | | | ± 7 | V |
| Operating free-air temperature, TA | 0 | 25 | 70 | °C |



electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | | TYP [†] | MAX | UNIT |
|------------------|---|---|---|-------------------|------------------|-------|--------|
| ., | Thursday of the second Manager | | | -0.2 [‡] | | 0.2 | |
| V⊤ | Threshold voltage (V_{T+} and V_{T-}) | See Note 4 | | -0.4‡ | | 0.4 |] ' |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | | | 70 | | | mV |
| VIB | Input bias voltage | I _I = 0 | | 2 | | 2.4 | V |
| νон | High-level output voltage | $V_{ID} = 0.2 V,$ | I _O = -1 mA | 2.5 | 3.5 | | V |
| VOL | Low-level output voltage | $V_{ID} = -0.2 V$, | $I_0 = 20 \text{ mA}$ | | 0.35 | 0.5 | \ \ |
| r. | Input resistance | See Note 5. | $V_1 = 3 \text{ V to } 25 \text{ V or}$ | 6 | 7.8 | 9.5 | kΩ |
| rį | | Oce Note 5, | $V_1 = -3 \text{ V to } -25 \text{ V}$ | | | 3.5 | K45 |
| | Input current | $V_{CC} = 0 \text{ to } 5.5 \text{ V},$ | V _I = 10 V | | 1.1 | 3.25 | mA |
| 11 | input current | See Note 6 | $V_1 = -10 \text{ V}$ | | -1.6 | -3.25 |] '''^ |
| los | Short-circuit output current§ | V _O = 0, | V _{ID} = 0.2 V | - 40 | - 75 | 100 | mA |
| Icc | Supply current | $V_{ID} = -0.5 V$, | No load | | 35 | 50 | mA |

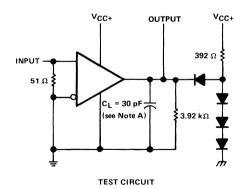
[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

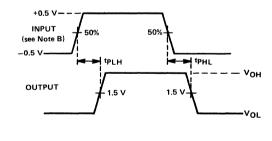
NOTES: 4. The expanded threshold parameter is tested with a 500- Ω resistor in series with each input.

switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | | TEST CONDITION | | TYP | MAX | UNIT |
|-----------|--|--------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | C _I = 30 pF, See Figure 1 | 100 | 150 | 300 | ns |
| tPHL | Propagation delay time, high-to-low-level output | CL = 30 pr., See rigure i | 100 | 150 | 300 | ns |

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORM

NOTES: A. C_I includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES



[‡]The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

[§] Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

^{5.} r_i is defined by $\Delta V_i/\Delta l_i$.

^{6.} The input not under test is grounded.

TYPICAL CHARACTERISTICS

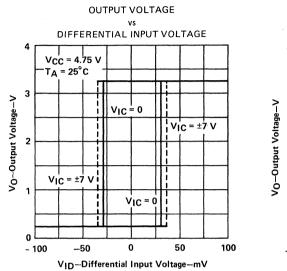
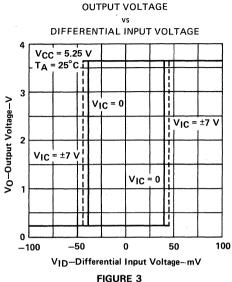
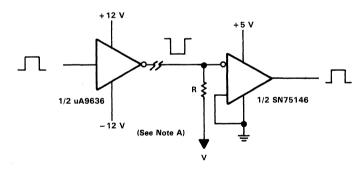


FIGURE 2



TYPICAL APPLICATION DATA



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of RS-232-C and CCITT V.28 and guarantee open-circuit-input failsafe operation, R and V are selected to satisfy the following equations:

$$V = -1.1 - 3.3 \frac{R}{r_i}$$
 volts

$$3 \ k\Omega \ \leq \ \frac{R(r_i)}{R \ + \ r_i} \ \leq \ 7 \ k\Omega$$

FIGURE 4. RS-232-C SYSTEM APPLICATIONS



TYPICAL APPLICATION DATA

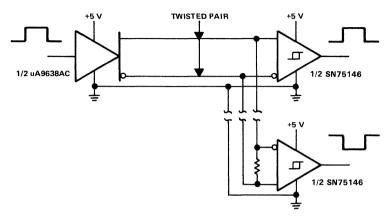


FIGURE 5. RS-422-A SYSTEM APPLICATIONS

- Satisfies Requirement of EIA Standard RS-232-C
- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage Between -25 V and 25 V
- 2-μs Max Transition Time Through the 3 V to -3 V Transition Region Under Full 2500-pF Load
- Inputs Compatible With Most TTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate Can Be Controlled With an External Capacitor at the Output
- Standard Supply Voltages . . . ± 12 V

description

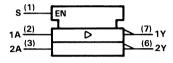
The SN75150 is a monolithic dual line driver designed to satisify the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and – 12-V power supplies.

The SN75150 is characterized for operation from 0° C to 70° C.

D, JG, OR P PACKAGE (TOP VIEW)

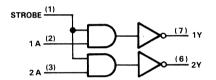
| S∐1 | U 8 | VCC+ |
|--------|-----|---------|
| 1A 🛮 2 | 7 |] 1Y |
| 2A 🛮 3 | 6 |] 2Y |
| GND ☐4 | 5 |] Vcc – |

logic symbol†



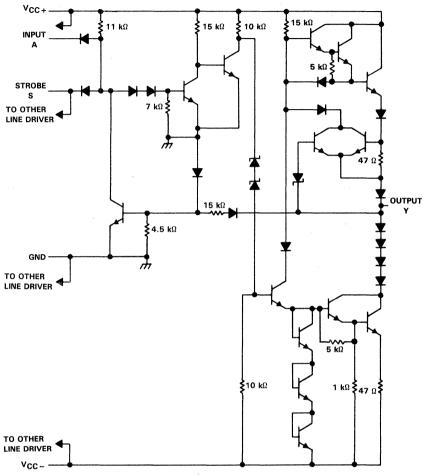
 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram (positive logic)





schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) |
|---|
| Supply voltage, VCC |
| Input voltage |
| Applied output voltage |
| Continuous total power dissipation |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| | PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---|---------|---------------------------------------|---------------------------------|---------------------------|
| 1 | D | 725 mW | 5.8 mW/°C | 464 mW |
| | JG | 825 mW | 6.6 mW/°C | 528 mW |
| | Р | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|--------|------|-------|------|
| Supply voltage, V _{CC+} | 10.8 | 12 | 13.2 | V |
| Supply voltage, V _{CC} - | - 10.8 | - 12 | -13.2 | V |
| High-level input voltage, V _{IH} | 2 | | 5.5 | V |
| Low-level input voltage, VIL | 0 | | 0.8 | ٧ |
| Applied output voltage, VO | | | ±15 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75150 DUAL LINE DRIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | | MIN | TYP [†] | MAX | UNIT |
|-------|--|---|------------------------------|-------------------------|-----|------------------|-------|------|
| Vон | High-level output voltage | $V_{CC+} = 10.8 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | | | 5 | 8 | | ٧ |
| VOL | Low-level output voltage (see Note 2) | $V_{CC+} = 10.8 \text{ V},$ $V_{IH} = 2 \text{ V},$ | $V_{CC-} = -10.8 \text{ V},$ | | | -8 | -5 | ٧ |
| lan | High-level input current | $V_{CC+} = 13.2 \text{ V},$ $V_{CC-} = -13.2 \text{ V},$ | | Data input | | 1 | 10 | μΑ |
| IH | riigh-level iliput culterit | $V_{L} = 2.4 \text{ V}$ | | Strobe input | | 2 | 20 | μΑ |
| 1 | Low level input ourrent | V _{CC+} = 13.2 V, | | Data input | | 1 | - 1.6 | A |
| IIL. | Low-level input current | $V_{CC-} = -13.2 \text{ V},$ $V_{I} = 0.4 \text{ V}$ | | Strobe input | | -2 | -3.2 | mA |
| | Short-circuit output current [‡] | $V_{CC+} = 13.2 \text{ V},$ | | $V_0 = 25 \text{ V}$ | | 2 | 8 | |
| 1 | | | | $V_0 = -25 \text{ V}$ | | -3 | -8 | |
| los | | $V_{CC-} = -13.2 \text{ V}$ | $V_0 = 0, V_1 = 3 V$ | | 10 | 15 | 30 | mA |
| i | | | Vo : | = 0, V _I = 0 | -10 | -15 | - 30 | |
| Іссн+ | Supply current from V _{CC+} , high-level output | V _{CC+} = 13.2 V, | | | | 10 | 22 | ^ |
| Іссн- | Supply current from V _{CC} , high-level output | $V_I = 0,$ $T_A = 25$ °C | nL = | = 3 kΩ, | | - 1 | - 10 | mA |
| ICCL+ | Supply current from V _{CC+} , low-level output | V _{CC+} = 13.2 V, | | _ = -13.2 V, = 3 kΩ, | | 8 | 17 | ^ |
| ICCL- | Supply current from V _{CC} -, low-level output | $V_I = 3 V,$ R_L $T_A = 25 ^{\circ}C$ | | - 3 KW, | | -9 | - 20 | mA |

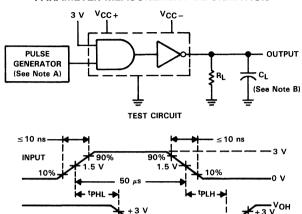
 $^{^{\}dagger}$ All typical values are at VCC $_{+}\,$ = 12 V, VCC $_{-}\,$ = $\,-$ 12 V, TA = 25 °C.

switching characteristics, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -12 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$ (see Figure 1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|---|-----|-----|-----|------|
| tTLH | Transition time, low-to-high-level output | C _L = 2500 pF, | 0.2 | 1.4 | 2 | μs |
| tTHL | Transition time, high-to-low-level output | $R_L = 3 k\Omega \text{ to } 7 k\Omega$ | 0.2 | 1.5 | 2 | μS |
| tTLH | Transition time, low-to-high-level output | C _L = 15 pF, | | 40 | | ns |
| tTHL | Transition time, high-to-low-level output | $R_L = 7 k\Omega$ | | 20 | | ns |
| tPLH | Propagation delay time, low-to-high-level output | C _L = 15 pF, | | 60 | | ns |
| tpHI | Propagation delay time, high-to-low-level output | $R_1 = 7 k\Omega$ | | 45 | | ns |

[‡] Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when -5 V is the maximum, the typical value is a more negative voltage.



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle \leq 50%, Z $_{0}$ \approx 50 $\Omega.$

tTHL -

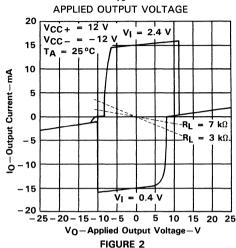
B. C_L includes probe and jig capacitance.

OUTPUT

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT



APPLICATION INFORMATION

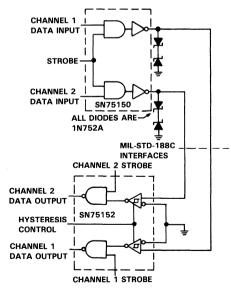


FIGURE 3. DUAL-CHANNEL SINGLE-ENDED INTERFACE CIRCUIT MEETING MIL-STD-188C, PARAGRAPH 7.2.



SN75151, SN75153 QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

D2453, DECEMBER 1978-REVISED OCTOBER 1986

- Meets FIA Standard RS-422-A
- High-Impedance Output State for Party-Line Operation
- High Output Impedance in Power-Off Condition
- Low Input Current to Minimize Loading
- Single 5-V Supply
- 40-mA Sink- and Source-Current Capability
- High-Speed Schottky Circuitry
- Low Power Requirements

description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the SN75151 provides an additional enable input for each driver. The output circuits have active pull-up and pull-down and are capable of sinking or sourcing 40 milliamperes.

The SN75151 and SN75153 meet all requirements of EIA Standard RS-422-A and Federal Standard 1020. They are characterized for operation from 0°C to 70°C.

SN75151 DW, J, OR N PACKAGE (TOP VIEW)

| 1A [| 1 | U 20 | □vco |
|-------|----|-------------|------|
| 1Y 🗌 | 2 | 19 |] 4A |
| 1Z [| 3 | 18 |] 4Y |
| 1C [| 14 | 17 |] 4Z |
| cc [| 5 | 16 |] 4C |
| 2C [| 6 | 15 | s |
| 2Z [| 7 | 14 |] 3C |
| 2Y [| 8 | 13 |] 3Z |
| 2A [| 9 | 12 |] 3Y |
| GND [| 10 | 11 | ПзΑ |

SN75153 J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

| 1 A [| 1 | U ₁₆ | □∨cc |
|-------|----|-----------------|------|
| 1 Y [| 2 | 15 |] 4A |
| 1Z [|]3 | 14 |] 4Y |
| cc[|]4 | 13 |] 4Z |
| 2Z [|]5 | 12 |] s |
| 2Y [|]6 | 11 |] 3Z |
| 2A [| 7 | 10 | □ 3Y |
| GND [| 8 | 9 |] 3A |
| | | | |

FUNCTION TABLES

SN75151

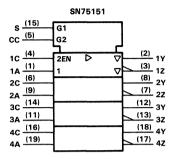
| INPUTS | | | | OUTPUTS | |
|--------|--------|--------|------|----------|---|
| ENABLE | ENABLE | STROBE | DATA | v | 7 |
| cc | С | S | Α | ' | |
| L | Х | X | Х | Z | Z |
| x | L | X | X | z | Z |
| н | Н | L | X | , L | Н |
| н | Н | X | L | L | H |
| Н | Н | Н | Н | Н | L |

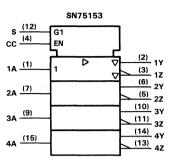
SN75153

| INPUTS | | | OUTPUTS | | |
|--------|--------|------|---------|---|--|
| ENABLE | STROBE | DATA | Υ | z | |
| CC | S | Α | | | |
| L | X | Х | Z | Z | |
| Н | L | X | L | Н | |
| Н | × | L | L | Н | |
| Н | н | Н | Н | L | |

SN75151, SN75153 QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

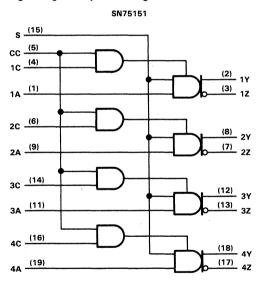
logic symbols†

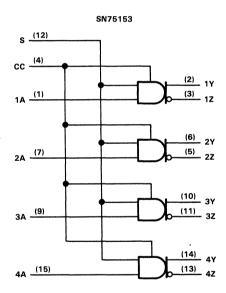


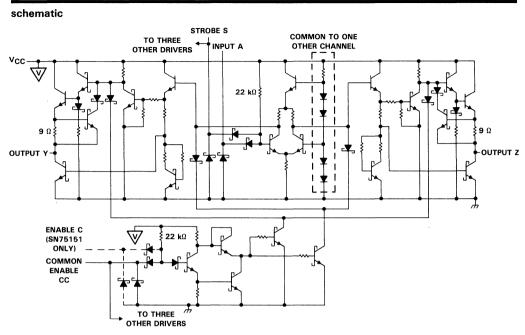


[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)







All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| DW package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package 260°C |

- NOTES: 1. All voltage values, except differential output voltage $V_{\mbox{\scriptsize OD}}$, are with respect to network ground terminal.
 - For operation above 25 °C free-air temperature, derate the DW package at the rate of 9 mW/°C, the J package at the rate
 of 8.2 mW/°C, and the N package at the rate of 9.2 mW/°C. In the J package, the chips are glass mounted.

SN75151, SN75153 QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Common-mode output voltage, VOC | -0.25 | | 6 | V |
| High-level output current, IOH | | | -40 | mA |
| Low-level output current, IOL | | | 40 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CO | NDITIONS† | MIN | TYP [‡] | MAX | UNIT | |
|-------------------|---|------------------------------|--------------------------------|----------|------------------|-------------------|------------|--|
| V _{IK} | Input clamp voltage | V _{CC} = MIN, | CC, S | | | - 2 | I V I | |
| VIK | input clamp voltage | $I_1 = -12 \text{ mA}$ | All others | | -0.9 | - 1.5 |] <u> </u> | |
| | | V _{CC} = MIN, | I _{OH} = -20 mA | 2.5 | | | | |
| Vон | High-level output voltage | $V_{IL} = MAX$, | | - | | | \ \ | |
| | <u> </u> | V _{IH} = 2 V | I _{OH} = -40 mA | 2.4 | | | | |
| VOL | Low-level output voltage | $V_{CC} = MIN,$ | $V_{IL} = MAX$, | ļ | | 0.5 | l v | |
| | | V _{IH} = 2 V, | I _{OL} = 40 mA | | | | | |
| VOD1 | Differential output voltage | $V_{CC} = MAX,$ | 10 = 0 | <u> </u> | 3.4 | 2V _{OD2} | V | |
| V _{OD2} | Differential output voltage | V _{CC} = MIN | | 2 | 2.8 | | V | |
| Δ V _{OD} | Change in magnitude of | V _{CC} = MIN | | | ±0.01 | ± 0.4 | V | |
| 414001 | differential output voltage§ | AGC = 141114 | B. 400.0 | | ±0.01 | 10.4 | l * | |
| 1/ | Common-mode output voltage | V _{CC} = MAX | $R_L = 100 \Omega$, | Ī | 1.8 | 3 | V | |
| voc | | V _{CC} = MIN | See Figure 1 | | 1.6 | 3 | | |
| 411/221 | Change in magnitude of common-mode output voltage § | V _{CC} = MIN or MAX | | . 0.00 | ±0.02 | ±0.4 | V | |
| ∆ Voc | | | | | ±0.02 | | ° | |
| | Off-state (high-impedance- | V _{CC} = MAX, | V _O = 0.5 V | | | - 20 | | |
| loz | state) output current | Enable at 0.8 V | $V_0 = 2.5 \text{ V}$ | | | 20 | μA | |
| | state) output current | Lilable at 0.5 V | $V_0 = V_{CC}$ | | | 20 |] | |
| | Output current with power off | V _{CC} = 0 | V _O = 6 V | | 0.1 | 100 | μΑ | |
| Ю | | | $V_0 = -0.25 \text{ V}$ | | -0.1 | - 100 | | |
| | | | $V_0 = -0.25 \text{ V to 6 V}$ | | | ± 100 | | |
| lį | Input current at maximum input voltage | V _{CC} = MAX, | V _I = 5.5 V | l | | 0.1 | mA | |
| '1 | | | | | | 0.1 | ,,,, | |
| hн | High-level input current | $V_{CC} = MAX$, | C('151), A | | | 20 | μА | |
| 1111 | Thigh lover impart current | V _I = 2.4 V | CC, S | 1 | | 80 | , | |
| IIL. | Low-level input current | V _{CC} = MAX, | C ('151), A | L | | -0.36 | mA. | |
| | • | V _I = 0.4 V | CC,S | ļ | | -1.6 | | |
| los | Short-circuit output current# | V _{CC} = MAX | | - 50 | - 90 | | mA | |
| lcc | Supply current (both drivers) | $V_{CC} = MAX,$ | Outputs disabled | | 30 | | mA . | |
| 100 | Cappiy Carront (both drivers) | No load | Outputs enabled | | 60 | 80 | | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{*} All typical values are at T_A = 25 °C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.

 $^{^{\}S}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

[¶]In EIA Standard RS-422-A, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, VOS.

[#]Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, VCC = 5 V, TA = 0 °C to 70 °C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|--|-----|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $C_L = 30 \text{ pF}, R_L = 100 \Omega, \text{ See Figure 2},$ | | 15 | 30 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Termination A | | 15 | 30 | ns |
| tPLH | Propagation delay time, low-to-high-level output | C 20 pE Son Figure 2 Termination B | | 13 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 30 pF, See Figure 2, Termination B | | 13 | 25 | ns |
| ^t TLH | Transition time, low-to-high-level output | $C_L = 30 \text{ pF}, R_L = 100 \Omega, \text{ See Figure 2},$ | | 12 | 20 | ns |
| [†] THL | Transition time, high-to-low-level output | Termination A | | 12 | 20 | ns |
| tPZH | Outut enable time to high level | $C_L = 30 \text{ pF}, R_L = 60 \Omega, \text{ See Figure 3}$ | | 18 | 35 | ns |
| tPZL | Output enable time to low level | $C_L = 30 \text{ pF}, R_L = 111 \Omega, \text{ See Figure 4}$ | | 20 | 35 | ns |
| tPHZ | Output disable time from high level | $C_L = 30 \text{ pF}, R_L = 60 \Omega, See Figure 3$ | | 19 | 30 | ns |
| tPLZ | Output disable time from low level | $C_L = 30 \text{ pF}, R_L = 111 \Omega, \text{ See Figure 4}$ | | 13 | 30 | ns |
| | Overshoot factor | $R_L = 100 \Omega$, See Figure 2, Termination C | | | 10 | % |

[†]All typical values are at $T_A = 25$ °C.

PARAMETER MEASUREMENT INFORMATION

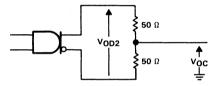
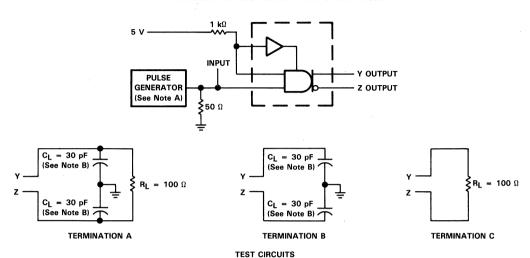
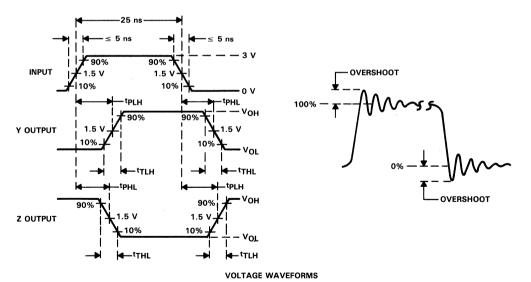


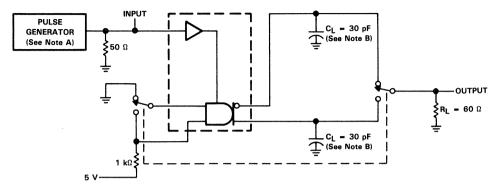
FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES





NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω , PRR \leq 10 MHz. B. C_L includes probe and jig capacitance.

FIGURE 2. tplH, tpHL, tTLH, tTHL, AND OVERSHOOT FACTOR



TEST CIRCUIT

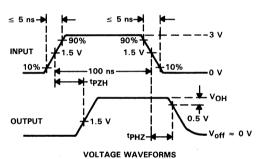
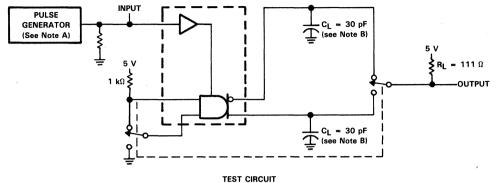


FIGURE 3. tPZH AND tPHZ

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω , PRR \leq 500 kHz.

B. C_L includes probe and jig capacitance.



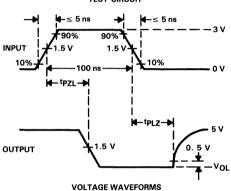


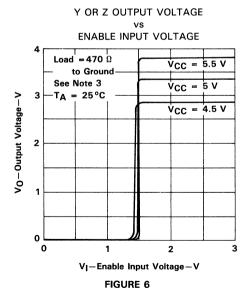
FIGURE 4. tpzL AND tpLZ

NOTES: A. The pulse generators have the following characteristics: $Z_{OUt} = 50 \ \Omega$, PRR $\leq 500 \ kHz$. B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE vs DATA INPUT VOLTAGE 5 No Load TA = 25°C V_{CC} = 5.5 V V_{CC} = 5 V Vo-Output Voltage-V V_{CC} = 4.5 V 3 2 1 0 3 0 V_I-Data Input Voltage-V

FIGURE 5



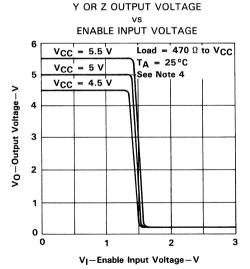
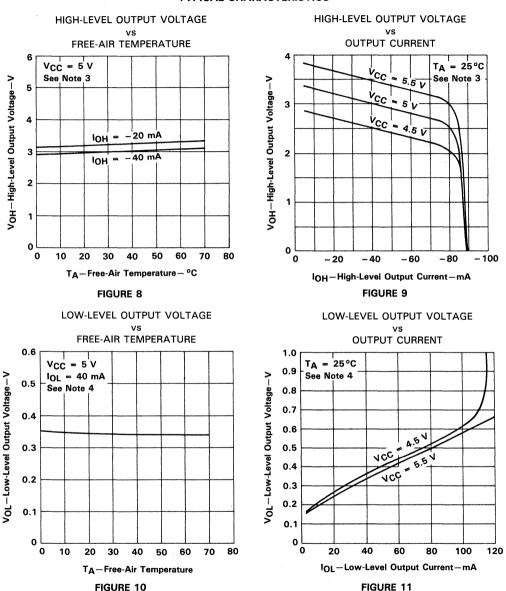


FIGURE 7

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

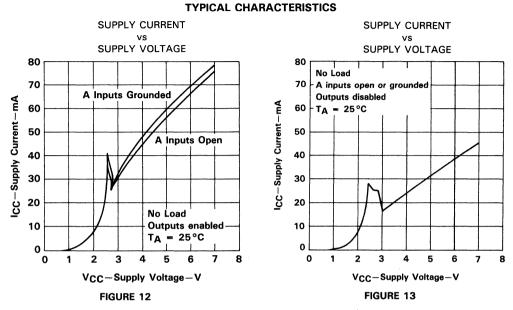
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS



NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.



NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs. 4. The A input is connected to ground during the testing of the Y outputs and to VCC during the testing of the Z inputs.

SN75154 QUADRUPLE LINE RECEIVER

D899, NOVEMBER 1970-REVISED MAY 1990

- Satisfies Requirements of EIA Standard RS-232-C
- Input Resistance . . . 3 $k\Omega$ to 7 $k\Omega$ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible With TTL
- Output With Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

D, J, OR N PACKAGE (TOP VIEW)

| 3T 1 16 VCC | 2 |
|----------------|----|
| | |
| 2T 2 15 VCC | :1 |
| 1T 🛛 3 14 🗍 4T | |
| 1A 🛮 4 13 🗒 1Y | |
| 2A 🛛 5 12 🗍 2Y | |
| 3A 🛛 6 11 🔲 3Y | |
| 4A 🛛 7 10 🔲 4Y | |
| GND 8 9 R1† | |

[†]For function of R1, see schematic

description

The SN75154 is a monolithic Low-Power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

The SN75154 is characterized for operation from 0°C to 70°C.

SN75154 QUADRUPLE LINE RECEIVER

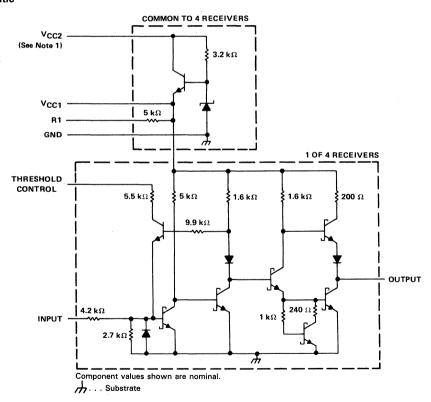
1A (4) (13) 17 (12) 27 (14) (10) 47

1A (4) (13) 1V 1T (3) 2A (5) (12) 2V 3A (6) (11) 3V 3T (1) (10) (10)

logic diagram

4T (14)

schematic



NOTE 1: When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1}. When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Normal supply voltage, VCC1 (see Note 2) | . 7 V |
|--|-------|
| Alternate supply voltage, VCC2 | 14 V |
| Input voltage | ±25 V |
| Continuous total power dissipation See Dissipation Rating | Table |
| Operating free-air temperature range | 70°C |
| Storage temperature range65°C to 1 | 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C |

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Normal supply voltage, V _{CC1} | 4.5 | 5 | 5.5 | V |
| Alternate supply voltage, V _{CC2} | 10.8 | 12 | 13.2 | V |
| High-level input voltage, VIH (see Note 3) | 3 | | 15 | V |
| Low-level input voltage, V _{IL} (see Note 3) | - 15 | | -3 | V |
| High-level output current, IOH | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

NOTES: 2. Voltage values are with respect to network ground terminal.

3. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

SN75154 QUADRUPLE LINE RECEIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

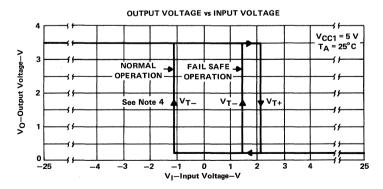
| | PARAMETE | R | TEST FIGURE | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|----------------------|---|---------------------|---|--|------|------|------|------|
| \/ | Positive-going | Normal operation | 1 | | 0.8 | 2.2 | 3 | v |
| V _{T+} | threshold voltage | Fail-safe operation | l ' | | 0.8 | 2.2 | 3 | v |
| V _T _ | Negative-going | Normal operation | 1 | | -3 | -1.1 | 0 | V |
| v 1 - | threshold voltage | Fail-safe operation | ' | | 0.8 | 1.4 | 3 | |
| \/ı | Hysteresis (V _{T+} - V _{T-}) | Normal operation | 1 | | 0.8 | 3.3 | 6 | V |
| V_{hys} | 11/2/6/62/2 (A + - A -1 | Fail-safe operation |] ' | | 0 | 0.8 | 2.2 | , |
| Voн | High-level output voltage | | 1 | I _{OH} = -400 μA | 2.4 | 3.5 | | V |
| VOL | Low-level output voltage | | 1 | I _{OL} = 16 mA | | 0.29 | 0.4 | V |
| | | | | $\Delta V_{\parallel} = -25 \text{ V to } -14 \text{ V}$ | 3 | 5 | 7 | |
| | | | 2 | $\Delta V_{I} = -14 \text{ V to } -3 \text{ V}$ | 3 | 5 | 7 | |
| rį | Input resistance | | | $\Delta V_{I} = -3 \text{ V to 3 V}$ | 3 | 6 | 8 | kΩ |
| | | | $\Delta V_{\parallel} = 3 \text{ V to } 14 \text{ V}$ | 3 | 5 | 7 | | |
| | | | | $\Delta V_{\parallel} = 14 \text{ V to } 25 \text{ V}$ | 3 | 5 | 7 | |
| V _{I(open)} | open) Open-circuit input voltage | | 3 | I _I = 0 | 0 | 0.2 | 2 | V |
| los | Short-circuit output current [†] | | 4 | $V_{CC1} = 5.5 \text{ V}, V_{I} = -5 \text{ V}$ | - 10 | - 20 | - 40 | mA |
| ICC1 | Supply current from V _{CC1} | | 5 | $V_{CC1} = 5.5 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | | 20 | 35 | mA |
| ICC2 | Supply current from VCC: | 2 |] | $V_{CC2} = 13.2 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | | 23 | 40 | |

 $[\]ensuremath{^{\dagger}}\xspace\ensuremath{\text{Not}}$ more than one output should be shorted at a time.

switching characteristics, $V_{CC1} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$, $N = 10 \,^{\circ}$

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN T | YP MAX | UNIT | |
|-----------|--|----------------|-------------------------|---|--------|------|----|
| tPLH | Propagation delay time, low-to-high-level output | | | | 11 | ns | |
| tPHL | Propagation delay time, high-to-low-level output | 6 | 6 | $C_{l} = 50 \text{ pF}, R_{l} = 390 \Omega$ | | 8 | ns |
| tTLH | Transition time, low-to-high-level output | | CL = 50 pr, NL = 590 tr | | 7 | ns | |
| tTHL | Transition time, high-to-low-level output | | | | 2.2 | ns | |

TYPICAL CHARACTERISTICS



NOTE 4: For normal operation, the threshold controls are connected to V_{CC1}. For fail-safe operation, the threshold controls are open.

 $^{^{\}ddagger}$ All typical values are at $V_{CC1} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

d-c test circuits†

TEST TABLE

| TEST | MEASURE | А | Т | Υ | V _{CC1} (PIN 15) | V _{CC2} (PIN 16) |
|--|-----------------|--------|--------|-----|------------------------------|------------------------------|
| Open-circuit input | V _{OH} | Open | Open | ЮН | 4.5 V | Open |
| (fail safe) | V _{OH} | Open | Open | 10H | Open | 10.8 V |
| V _{T+} min, | V _{OH} | 0.8 V | Open | ЮН | 5.5 V | Open |
| V _T min (fail safe) | Voн | 0.8 V | Open | Іон | Open | 13.2 V |
| V _{T+} min (normal) | VoH | Note A | Pin 15 | Іон | 5.5 V and T | Open |
| V + IIIII (IIOIIIIai) | VoH | Note A | Pin 15 | IОН | T | 13.2 V |
| V _{IL} max, | VoH | -3 V | Pin 15 | ІОН | 5.5 V and T | Open |
| V _{T —} min (normal) | V _{OH} | -3 V | Pin 15 | lон | Т | 13.2 V |
| VIH min, VT + max, | VOL | 3 V | Open | lOL | 4.5 V | Open |
| V _T _ max (fail safe) | VOL | 3 V | Open | lOL | Open | 10.8 V |
| V _{IH} min, V _{T+} max | VOL | 3 V | Pin 15 | lOL | 4.5 V and T | Open |
| (normal) | VOL | 3 V | Pin 15 | lOL | Т | 10.8 V |
| V _{T _} max (normal) | VOL | Note B | Pin 15 | lOL | 5.5 V and T | Open |
| V _ max (normal) | V _{OL} | Note B | Pin 15 | loL | T | 13.2 V |

NOTES: A. Momentarily apply -5 V, then 0.8 V.

B. Momentarily apply 5 V, then ground.

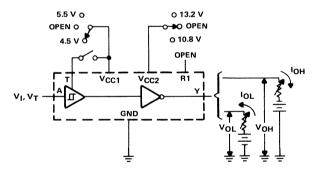
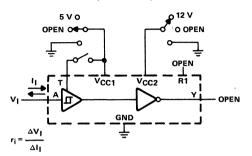


FIGURE 1. VIH, VIL, VT+, VT-, VOH, VOL

[†]Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

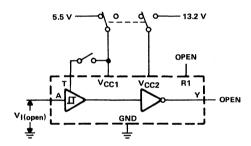
d-c test circuits† (continued)



TEST TABLE

| т | VCC1 (PIN 15) | V _{CC2} (PIN 16) |
|--------|------------------|------------------------------|
| Open | 5 V | Open |
| Open | GND | Open |
| Open | Open | Open |
| Pin 15 | T and 5 V | Open |
| GND | GND | Open |
| Open | Open | 12 V |
| Open | Open | GND |
| Pin 15 | Т | 12 V |
| Pin 15 | Т | GND |
| Pin 15 | T | Open |

FIGURE 2. ri



TEST TABLE

| Т | VCC1 (PIN 15) | V _{CC2} (PIN 16) |
|--------|------------------|------------------------------|
| Open | 5.5 V | Open |
| Pin 15 | 5.5 V | Open |
| Open | Open | 13.2 V |
| Pin 15 | Т | 13.2 V |

FIGURE 3. VI(open)

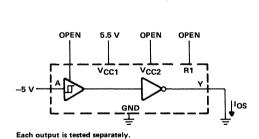
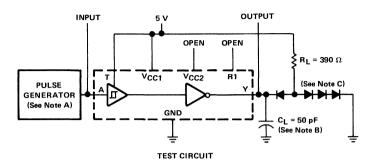


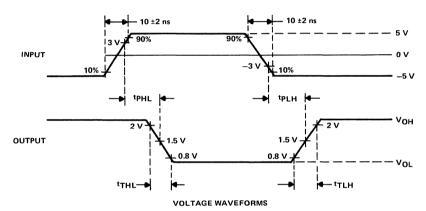
FIGURE 5. ICC

All four line receivers are tested simultaneously.

FIGURE 4. IOS

[†]Arrows indicate actual direction of current flow. Current into a terminal is a positive value.





NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \ \Omega$, $t_W \le 200 \ ns$, duty cycle $\le 20\%$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.

FIGURE 6. SWITCHING TIMES

D2951, JULY 1986-REVISED AUGUST 1989

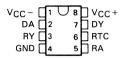
- Meets EIA Standard RS-232-C
- 10-mA Current Limited Output
- Wide Range of Supply
 Voltage . . . VCC = 4.5 V to 15 V
- Low Power . . . 130 mW
- Built-In 5-V Regulator
- Response Control Provides: Input Threshold Shifting Input Noise Filtering
- Power-Off Output Resistance . . . 300 Ω Typ
- Driver Input TTL Compatible

description

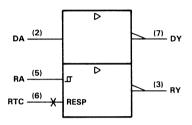
The SN75155 is a monolithic line driver and receiver that is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232-C. A Response Control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

The SN75155 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

D, JG, OR P PACKAGE (TOP VIEW)

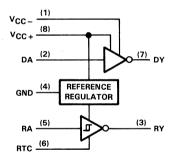


logic symbol†

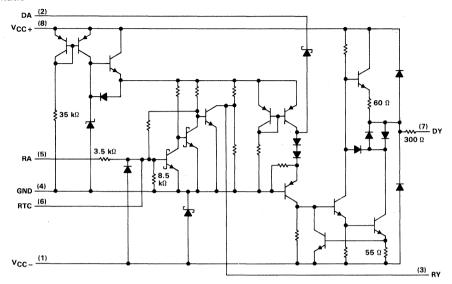


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram



schematic



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC + (see Note 1) |
|---|
| Supply voltage, VCC (see Note 1) |
| Input voltage range: Driver15 V to 15 V |
| Receiver |
| Output voltage range (Driver) |
| |
| Continuous total power dissipation See Dissipation Rating Table |
| Continuous total power dissipation |
| |
| Operating free-air temperature range |

OTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE [†] | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|----------------------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| JG | 825 mW | 6.6 mW/°C | 528 mW |
| Р | 1000 mW | 8.0 mW/°C | 640 mW |

 $^{\dagger}\mbox{In}$ the JG package, SN75155 chips are glass mounted.



recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC+} | 4.5 | 12 | 15 | ٧ |
| Supply voltage, V _{CC} _ | -4.5 | -12 | - 15 | V |
| Input voltage, driver, V _{I(D)} | | | ±15 | V |
| Input voltage, receiver, V _{I(R)} | - 25 | | 25 | V |
| High-level input voltage, driver, VIH | . 2 | | | V |
| Low-level input voltage, driver, VIL | | | 0.8 | V |
| Response control current | | | ±5.5 | mA |
| Output current, receiver, IO(R) | | | 24 | mA |
| Operating free-air temperature, Тд | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

| | PARAMETERS | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-------|---------------------------|-------------------|---------------------|-----------------------------|-----|------------------|-------|------|
| | | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$, | $V_{I(D)} = 2 V$ | | 6.3 | 8.1 | |
| ICCH+ | High-level supply current | $V_{CC+} = 9 V$, | $V_{CC-} = -9 V$, | $V_{I(R)} = 2.3 V,$ | | 9.1 | 11.9 | mA |
| | | $V_{CC+} = 12 V,$ | $V_{CC-} = -12 V$, | Output open | | 10.4 | 14 | |
| | | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$, | $V_{I(D)} = 0.8 V,$ | | 2.5 | 3.4 | |
| ICCL+ | Low-level supply current | $V_{CC+} = 9 V$ | $V_{CC-} = -9 V$ | $V_{I(R)} = 0.6 V,$ | | 3.7 | 5.1 | mA |
| | | $V_{CC+} = 12 V$ | $V_{CC-} = -12 V$, | Output open | | 4.1 | 5.6 | |
| Inn | Supply current | $V_{CC+} = 5 V$, | $V_{CC-} = 0$, | $V_{1(R)} = 2.3 \text{ V},$ | | 4.8 | 6.4 | mA |
| ICC+ | Supply current | $V_{CC+} = 9 V$, | $V_{CC-} = 0$, | $V_{I(D)} = 0$ | | 6.7 | 9.1 | IIIA |
| | | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$, | $V_{I(D)} = 2 V,$ | | -2.4 | - 3.1 | |
| ICCH- | High-level supply current | $V_{CC+} = 9 V$ | $V_{CC-} = -9 V$, | $V_{I(R)} = 2.3 V,$ | | -3.9 | -4.9 | mA |
| | | $V_{CC+} = 12 V,$ | $V_{CC-} = -12 V$, | Output open | | -4.8 | - 6.1 | |
| | | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$, | $V'_{I(D)} = 0.8 V,$ | | -0.2 | -0.35 | |
| ICCL- | Low-level supply current | $V_{CC+} = 9 V$, | $V_{CC-} = -9 V$, | $V_{I(R)} = 0.6 V$ | - | -0.25 | -0.4 | mA |
| | | $V_{CC+} = 12 V,$ | $V_{CC-} = -12 V$, | Output open | - | -0.27 | -0.45 | |

 $^{^{\}dagger}AII$ typical values are at $T_{\mbox{\scriptsize A}}~=~25\,^{\circ}\mbox{\scriptsize C}.$

SN75155 LINE DRIVER AND RECEIVER

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -12 \text{ V}$ (unless otherwise noted)

driver section

| | PARAMETER TEST CONDITIONS | | | | | TYP [†] | MAX | UNIT |
|------|---------------------------------------|-------------------------|--------------------|---|-----|------------------|--------|------|
| | | | , | $V_{CC+} = 5 \text{ V}, V_{CC-} = -5 \text{ V}$ | 3.2 | 3.7 | | |
| ∨он | High-level output voltage | $V_{IL} = 0.8 V,$ | $R_L = 3 k\Omega$ | $V_{CC+} = 9 \text{ V}, V_{CC-} = -9 \text{ V}$ | 6.5 | 7.2 | | V |
| | | | | $V_{CC+} = 12 \text{ V}, V_{CC-} = -12 \text{ V}$ | 8.9 | 9.8 | | |
| | Lave Lavel autout valtage | | | $V_{CC+} = 5 \text{ V}, V_{CC-} = -5 \text{ V}$ | | -3.6 | -3.2 | |
| VOL | Low-Level output voltage (see Note 2) | V _{IH} = 2 V, | $R_L = 3 k\Omega$ | $V_{CC+} = 9 \text{ V}, V_{CC-} = -9 \text{ V}$ | | - 7.1 | -6.4 | V |
| | | | | $V_{CC+} = 12 \text{ V}, V_{CC-} = -12 \text{ V}$ | | - 9.7 | -8.8 | |
| ЧН | High-level input current | V _I = 7 V | | | | | . 5 | μΑ |
| IL | Low-level input current | V _I = 0 | | | | -0.73 | -1.2 | mA |
| loou | High-level short-circuit | V _I = 0.8 V, | Va = 0 | | - 7 | - 12 | _ 14 5 | mA |
| losh | output current | V1 = 0.8 V, | VO = 0 | | _, | - 12 | - 14.5 | IIIA |
| loo | Low-level short-circuit | V _I = 2 V, | V _O = 0 | | 6.5 | 11.5 | 15 | mA |
| IOSL | output current | V1 - 2 V, | VO = 0 | | 0.5 | 11.5 | 15 | IIIA |
| P.o | Output resistance | V _O = -2 V t | - 2 V | | | 300 | | Ω |
| RO | with power off | VU2 V I | .U Z V | | | 300 | | ** |

receiver section (see Figure 1)

| | PARAMETER | | TEST CONDITIONS | S | MIN | TYP [†] | MAX | UNIT |
|------------------|-------------------------------------|----------------------------|--------------------|---------------------------|-------|------------------|-------|----------------|
| V _{T+} | Positive-going threshold voltage | | | | 1.2 | 1.9 | 2.3 | V |
| V _T _ | Negative-going threshold voltage | | | | 0.6 | 0.95 | 1.2 | ٧ |
| V _{hys} | Hysteresis | | | | 0.6 | | | ٧ |
| | | $V_1 = 0.6 V$, | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$ | 3.7 | 4.1 | 4.5 | |
| | High-level output voltage | I _{OH} = 10 μA | $V_{CC+} = 12 V$, | $V_{CC-} = -12 \text{ V}$ | 4.4 | 4.7 | 5.2 | l _v |
| VOH | | $V_1 = 0.6 V$, | $V_{CC+} = 5 V$, | $V_{CC-} = -5 V$ | 3.1 | 3.4 | 3.8 | |
| | | I _{OH} = 0.4 mA | $V_{CC+} = 12 V,$ | $V_{CC-} = -12 V$ | 3.6 | 4 | 4.5 | |
| VOL | Low-level output voltage | V _I = 2.3 V, IC |)L = 24 mA | | | 0.2 | 0.3 | V |
| | High level innut access | V _I = 25 V | | | 3.6 | 6.7 | 10 | mA |
| ΙΗ | High-level input current | V _I = 3 V | | | 0.43 | 0.67 | 1 | mA |
| 1 | $V_{\rm I} = -25 \text{ V}$ | | | | -3.6 | -6.7 | -10 | mA |
| l IIL | Low-level input current | V _I = -3 V | | | -0.43 | -0.67 | - 1 | mA |
| los | Short-circuit output current | V _I = 0.6 V | | | | -2.8 | - 3.7 | mA |

 $^{^{\}dagger}$ All typical values are at $T_{A} = 25 \,^{\circ}$ C.

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only, e.g., if -8.8 V is the maximum, the typical value is a more negative value.

switching characteristics over recommended operating free-air temperature range, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $C_L = 50 \text{ pF}$ (unless otherwise noted)

driver section (see Figure 2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|--|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $R_1 = 3 k\Omega$ | | 250 | 480 | |
| tPHL | Propagation delay time high-to-low-level output | ur = 2 km | | 80 | 150 | ns |
| | Output rise time | $R_L = 3 k\Omega$ | | 67 | 180 | ns |
| ۱۲ | | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 2500 pF$ | | 2.4 | 3 | μS |
| tf | Output fall time | $R_L = 3 k\Omega$ | | 48 | 160 | ns |
| | Output rail time | $R_L = 3 k\Omega$ to $7 k\Omega$, $C_L = 2500 pF$ | | 1.9 | 3 | μS |

receiver section (see Figure 3)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|----------------|--|------------------------|-----|------------------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | R _I = 400 Ω | | 175 | 245 | |
| tPHL | Propagation delay time, high-to-low-level output | nL = 400 12 | | 37 | 100 | ns |
| t _r | Output rise time | $R_L = 400 \Omega$ | | 255 | 360 | ns |
| tf | Output fall time | $R_L = 400 \Omega$ | | 23 | 50 | ns |

[†]All typical values are at $T_A = 25$ °C.

PARAMETER MEASUREMENT INFORMATION

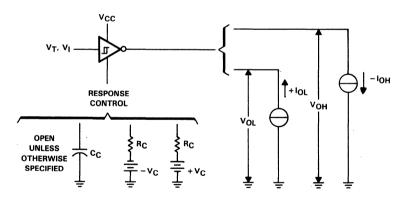
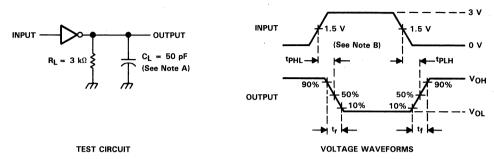


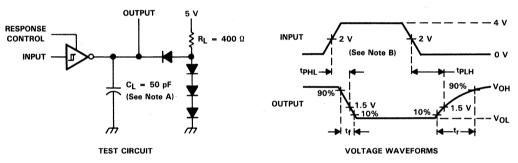
FIGURE 1. RECEIVER SECTION TEST CIRCUIT (V_{T+} , V_{T-} , V_{OH} , V_{OL})



NOTES: A. C_L includes probe and jig capacitance.

B. The input waveform is supplied by a generator with the following characteristics: $Z_{OUt} \approx 50 \, \Omega$, $t_W = 1 \, \mu s$, $t_f \leq 10 \, ns$, $t_f \leq 10 \, ns$.

FIGURE 2. DRIVER SECTION SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

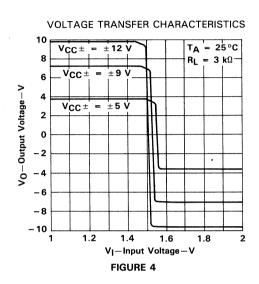


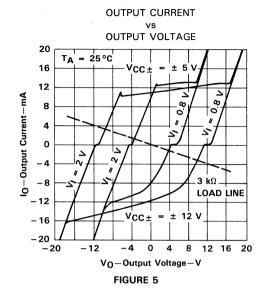
NOTES: A. C_I includes probe and jig capacitance.

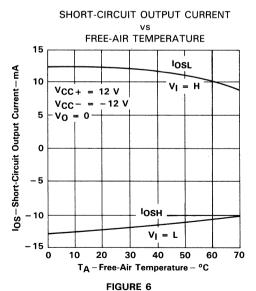
B. The input waveform is supplied by a generator with the following characteristics: $Z_{OUI} \approx 50 \,\Omega$, $t_W = 1 \,\mu s$, $t_f \le 10 \,ns$, $t_f \le 10 \,ns$.

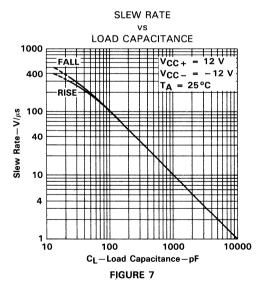
FIGURE 3. RECEIVER SECTION SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS (DRIVER)









TYPICAL CHARACTERISTICS (RECEIVER)

OUTPUT VOLTAGE vs INPUT VOLTAGE

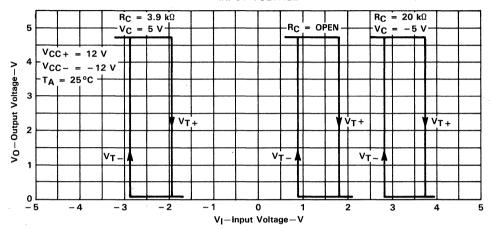


FIGURE 8

OUTPUT VOLTAGE vs

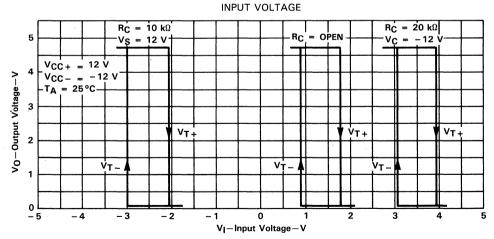
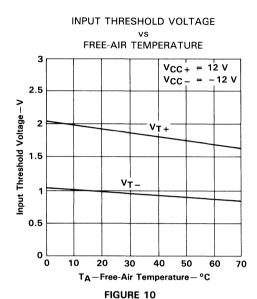


FIGURE 9



TYPICAL CHARACTERISTICS (RECEIVER)



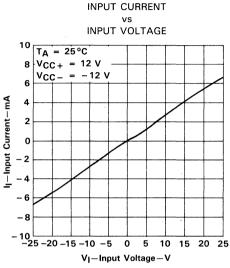
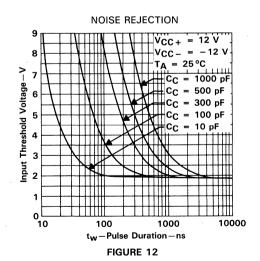


FIGURE 11



SN75159 DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

D2325, JANUARY 1977-REVISED SEPTEMBER 1986

- Meets EIA Standard RS-422-A
- Single 5-V Supply
- Balanced Line Operation
- TTL-Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

(TOP VIEW) 714] VCC NC T1 1Z [13 2Z 12 2Y 1Y [3 1A | 4 11 2B 1B ∏ 5 10∏ 2A 1EN ∏6 9∏ 2EN GND [8∏ NC

D. J. OR N PACKAGE

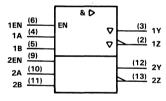
NC-No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†

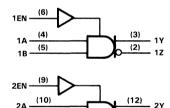


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

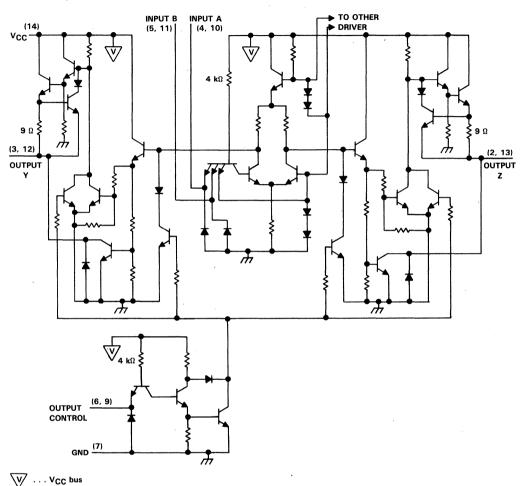
(11)

2В



(13)

schematic (each driver)



Resistor values shown are nominal.

| absolute maximum ratings over operating free-air temperature range (unless otherwise noted) |
|--|
| Supply voltage, VCC (see Note 1) |
| Input voltage |
| Off-state voltage applied to open-collector outputs |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| D package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C |
| NOTES: 1. All voltage values except differential output voltage V _{OD} are with respect to the network ground terminal. V _{OD} is at the Y |

output with respect to the Z output.

2. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/°C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C. In the J package, SN75159 chips are glass mounted.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | V |
| High-level output voltage, IOH | | | -40 | mA |
| Low-level output current, IOL | | | 40 | mA |
| Operating free-air temperature, TA | | 1 | 70 | °C. |

SN75159 **DUAL DIFFERENTIAL LINE DRIVER** WITH 3-STATE OUTPUTS

electrical characteristics over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|---|-------------------------------------|------------------------|-----|------------------|-------------------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 V$, | I _I = -12 mA | | | -0.9 | - 1.5 | V |
| Vон | High-level output voltage | $V_{CC} = 4.75 \text{ V},$ $V_{IH} = 2 \text{ V},$ | $I_{OH} = -40 \text{ mA}$ | | 2.4 | 3.0 | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = 4.75 \text{ V},$ $V_{IH} = 2 \text{ V},$ | | | | 0.25 | 0.4 | ٧ |
| Voк | Output clamp voltage | $V_{CC} = 5.25 \text{ V},$ | $I_0 = -40 \text{ mA}$ | | | -1.1 | - 1.5 | V |
| Vo | Output voltage | $V_{CC} = 4.75 \text{ V to}$ | $5.25 \text{ V}, \text{ I}_{0} = 0$ | | 0 | | 6 | ٧ |
| V _{OD1} | Differential output voltage | $V_{CC} = 5.25 V,$ | I _O = 0 | , | | , 3.5 | 2V _{OD2} | ٧ |
| V _{OD2} | Differential output voltage | $V_{CC} = 4.75 \text{ V}$ | | | 2 | 3.0 | | V |
| Δ V _{OD} | Change in magnitude of differential output voltage [‡] | V _{CC} = 4.75 V | | | | ±0.02 | ±0.4 | ٧ |
| v _{oc} | Common-mode output voltage§ | $V_{CC} = 5.25 \text{ V}$ $V_{CC} = 4.75 \text{ V}$ | $R_L = 100 \Omega$, | See Figure 1 | | 1.8 | 3 | > |
| Δ V _{OC} | Change in magnitude of common-mode output voltage [‡] | V _{CC} = 4.75 V to 5.25 V | | | | ±0.01 | ±0.4 | ٧ |
| | | | V _O = 6 V | | | 0.1 | 100 | |
| lo | Output current with power off | $V_{CC} = 0$ | $V_0 = -0.25 \text{ V}$ | | | -0.1 | -100 | μΑ |
| | | | $V_0 = -0.25 \text{ V}$ | o 6 V | | | ± 100 | |
| | | | $T_A = 25$ °C, | $V_0 = 0$ to V_{CC} | | | ±10 | |
| | Off state (high impedance | $V_{CC} = 5.25 V,$ | | V ₀ = 0 | | | - 20 | |
| loz | Off-state (high impedance- state) output current | Output controls | T _A = 70°C | V _O = 0.4 V | | | ± 20 | μΑ |
| | state/ output current | at 0.8 V | 1A = 70 °C | V _O = 2.4 V | | | ± 20 | |
| | | | | $V_O = V_{CC}$ | | | 20 | |
| l _l | Input current at maximum input voltage | V _{CC} = 5.25 V, | V _I = 5.5 V | | | | 1 | mA |
| Ιн | High-level input current | V _{CC} = 5.25 V, | | | | | 40 | μΑ |
| IIL | Low-level input current | $V_{CC} = 5.25 V$, | V _I = 0.4 V | | | - 1 | -1.6 | mA |
| los | Short-circuit output current | $V_{CC} = 5.25 \text{ V}$ | | | -40 | - 90 | - 150 | mA |
| ¹cc | Supply current (both drivers) | $VCC = 5.25 \text{ V},$ $T_A = 25 ^{\circ}C$ | Inputs grounded, | No load, | | 47 | 65 | mA |

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25$ °C except for V_{OC} , for which V_{CC} is as stated under test conditions. $^{\ddagger}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

In EIA Standard RS-422-A, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, VOS. Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over operating free-air temperature range, VCC = 5 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|--|--|-----|------------------|-----|------|
| tpLH Propagation delay time, low-to-high-level output | $C_L = 30 \text{ pF}, R_L = 100 \Omega, \text{ See Figure 2},$ | | 16 | 25 | ns |
| tPHL Propagation delay time, high-to-low-level output | Termination A | | 11 | 20 | ns |
| tPLH Propagation delay time, low-to-high-level output | 0 15 5 0 5 0 7 | | 13 | 20 | ns |
| tphL Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 2, Termination B | | 9 | 15 | ns |
| tTLH Transition time, low-to-high-level output | $C_L = 30 \text{ pF}, R_L = 100 \Omega, \text{ See Figure 2},$ | | 4 | 20 | ns |
| t _{THL} Transition time, high-to-low-level output | Termination A | | 4 | 20 | ns |
| tPZH Output enable time to high level | $C_L = 30 \text{ pF}, R_L = 180 \Omega, \text{ See Figure 3}$ | | 7 | 20 | ns |
| tpzL Output enable time to low level | $C_L = 30 \text{ pF}, R_L = 250 \Omega, \text{ See Figure 4}$ | | 14 | 40 | ns |
| tpHZ Output disable time from high level | $C_L = 30 \text{ pF}, R_L = 180 \Omega, \text{ See Figure 3}$ | | 10 | 30 | ns |
| tpLZ Output disable time from low level | $C_L = 30 \text{ pF}, R_L = 250 \Omega, \text{ See Figure 4}$ | | 17 | 35 | ns |
| Overshoot factor | $R_L = 100 \Omega$, See Figure 2, Termination C | | | 10 | % |

 $^{^{\}dagger}$ All typical values are at $T_A = 25 \,^{\circ}$ C.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A |
|----------------------|-------------------------------------|
| v _o | V _{oa} , V _{ob} |
| VOD1 | Vo |
| V _{OD2} | V _t |
| Δ V _{OD} | $ V_t - \overline{V}_t $ |
| Voc | Vos |
| ΔIVOC | $ V_{os} - \overline{V}_{os} $ |
| los . | I _{sa} , I _{sb} |
| 10 | I _{xa} , I _{xb} |

PARAMETER MEASUREMENT INFORMATION

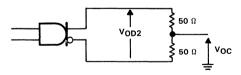
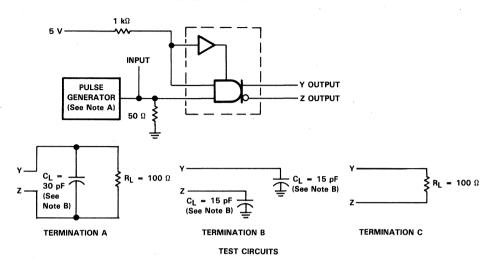
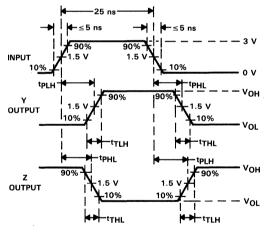
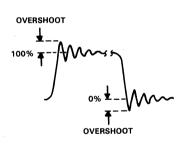


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES







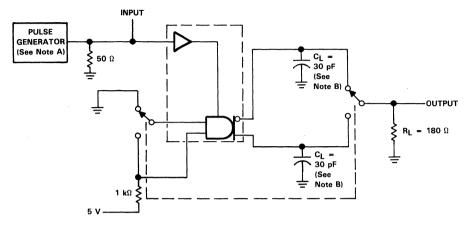
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_{out} = 50 \Omega$, PRR $\leq 10 MHz$.

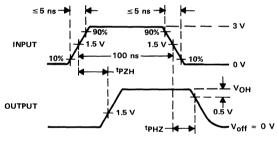
B. C_L includes probe and jig capacitance.

FIGURE 2. tplH, tpHL, tTLH, tTHL, AND OVERSHOOT FACTOR





TEST CIRCUIT

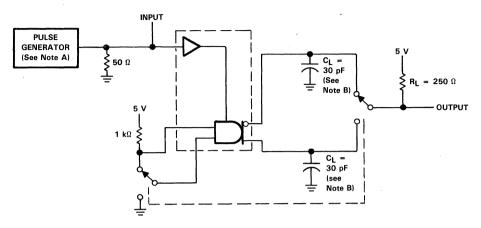


VOLTAGE WAVEFORMS

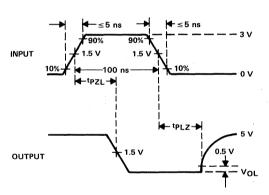
NOTES: A. The pulse generator has the following characteristics: Z $_{out}$ = 50 Ω , PRR \leq 500 kHz.

B. C_L includes probe and jig capacitance.

FIGURE 3. tPZH AND tPHZ



TEST CIRCUIT

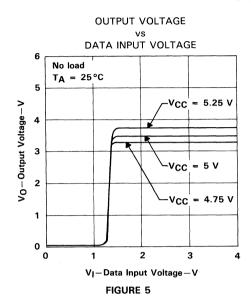


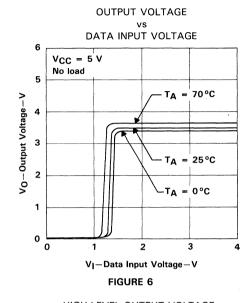
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω , PRR \leq 500 kHz. C. C_L includes probe and jig capacitance.

FIGURE 4. tPZL AND tPLZ

TYPICAL CHARACTERISTICS





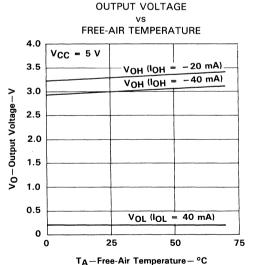
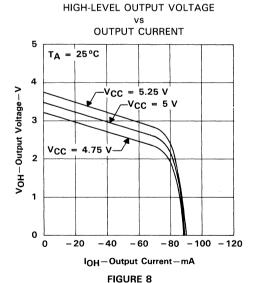
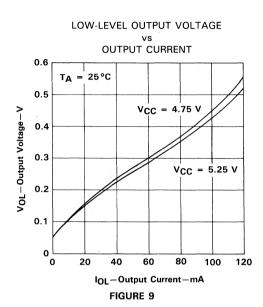


FIGURE 7



TYPICAL CHARACTERISTICS



SUPPLY CURRENT (BOTH DRIVERS)

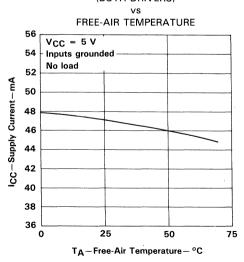
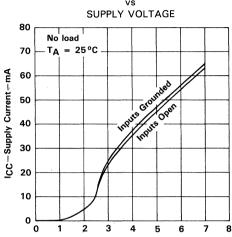


FIGURE 11

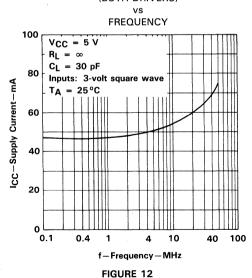
SUPPLY CURRENT (BOTH DRIVERS) vs



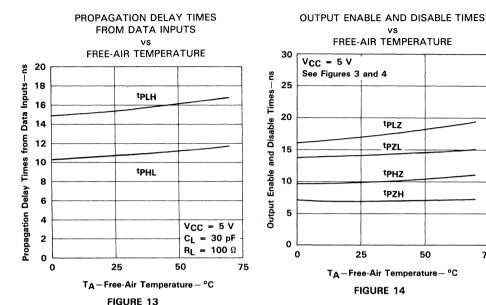
SUPPLY CURRENT
(BOTH DRIVERS)

VCC-Supply Voltage-V

FIGURE 10



TYPICAL CHARACTERISTICS



75

D2525, OCTOBER 1985

MEETS IEEE STANDARD 488-1978 (GPIB)

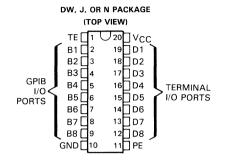
- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (VCC = 0)

description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, highspeed, low-power Schottky device designed for two-way data communications over singleended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power-up and powerdown are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.



FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

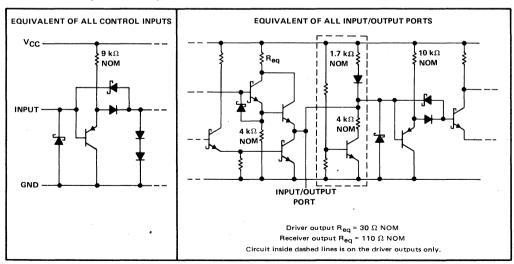
| INPUTS | | OUTPUT | II | NPUT | s | OUTPUT | |
|--------|----|--------|----------------|------|----|--------|---|
| D | TE | PE | В | В | TE | PE | D |
| Н | Н | Н | Н | L | L | Х | L |
| L | Н | X | L | Н | L | Χ | н |
| Н | X | L | Z [†] | Х | Н | Х | Z |
| Х | Ł | X | Z [†] | | | | |

H = high level, L = low level, X = irrelevant, Z = High-impedance

[†] This is the high-impedance state of a normal 3-state output modified by the internal resistors to VCC and ground.

logic diagram (positive logic) logic symbol[†] M1 [3S] M2 [0C] TE (1) EN3 [XMT] D1 (19) EN4 [RCV] D1 (19) ⁽²⁾_ B1 (2) B1 3 (1 ▽/2 숙 D2 (18) D2 (18) (<u>3)</u> B2 (3) D3 (17) (4) D3 (17) (16)(5) B4 (6) B5 D5 (15) (<u>4)</u> B3 (7) (14)D6 B6 D4 (16) (8) В7 (<u>5)</u> B4 (9) TERMINAL D5 (15) GPIB 1/0 [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and (6) - B5 PORTS IEC Publication 617-12. ∇ Designates 3-state outputs. D6 (14) ◆ Designates passive-pullup outputs. (7<u>)</u> B6 D7 (13) (8) - B7 (12) DΩ (9)

schematics of inputs and outputs



SN75160B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | V |
|---|-----|
| Input voltage | V |
| Low-level driver output current | nΑ |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Tal | ble |
| Operating free-air temperature range | °C |
| Storage temperature range | °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package 300 | °C |
| Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260 | °C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. In the J package, SN75160B chips are alloy mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|--------------------------------|-----|-----|------|------|
| Supply voltage, V _{CC} | | | 5 5 | 5.25 | V |
| High-level input voltage, VIH | | | 2 | | V |
| Low-level input voltage, VIL | | , | | 0.8 | V |
| High lovel autout automat I | Bus ports with pull-ups active | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| Low-level output current, IOL | Bus ports . | | | 48 | A |
| | Terminal ports | | | 16 | mA · |
| Operating free-air temperature, TA | | (|) | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT | |
|-------------------------------------|--|-----------|--|--|------|------------------|-------|-------|--|
| V _{IK} Input clamp voltage | | | I _I = -18 mA | | | -0.8 | -1.5 | V | |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus . | | | 0.4 | 0.65 | | V | |
| Voн | High-level | Terminal | $I_{OH} = -800 \mu A$, | TE at 0.8 V | 2.7 | 3.5 | | V | |
| | output voltage | Bus | $I_{OH} = -5.2 \text{ mA},$ | PE and TE at 2 V | 2.5 | 3.3 | | | |
| VOL | Low-level | Terminal | | | | 0.3 | 0.5 | V | |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA},$ | TE at 2 V | | 0.35 | 0.5 | ľ | |
| lį | Input current at maximum input voltage | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ | |
| lН | High-level input current | Terminal | V _I = 2.7 V | | | 0.1 | 20 | μΑ | |
| ЦL | Low-level input current | Terminal | V _I = 0.5 V | | | - 10 | - 100 | μΑ | |
| V | Voltage at bus port | | Driver disabled | $I_{l(bus)} = 0$ | 2.5 | 3.0 | 3.7 | V | |
| V _{I/O(bus)} | voitage at bus port | | | $I_{I(bus)} = -12 \text{ mA}$ | | | -1.5 | \ \ \ | |
| | Current into bus port | Power on | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | | |
| | | | Driver disabled | $V_{l(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | | |
| I _I /O(bus) | | | | V _{I(bus)} = 2.5 V to 3.7 V | | | +2.5 | mA | |
| 'I/O(bus) | | | | V _{I(bus)} = 3.7 V to 5 V | 0 | | 2.5 | | |
| | | | | $V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$ | 0.7 | | 2.5 | i | |
| | | Power off | V _{CC} = 0, | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | -40 | μΑ | |
| | Short-circuit | Terminal | 100 07 | (I(Dus) o to Ele t | - 15 | - 35 | - 75 | P | |
| los | output current | Bus | | | - 25 | - 50 | -125 | mA | |
| lcc | Supply current | | | Receivers low and enabled | | 70 | 90 | mA | |
| | | | No load | Drivers low and enabled | | 85 | 110 | | |
| C _{i/o(bus)} | (bus) Bus-port capacitance | | $V_{CC} = 5 \text{ V to 0},$ f = 1 MHz | $CC = 5 \text{ V to 0}, V_{I/O} = 0 \text{ to 2 V},$ = 1 MHz | | 30 | | pF . | |

 $^{^{\}dagger}\text{All typical values are at V}_{CC}~=~5$ V, $T_{A}~=~25\,^{o}\text{C}.$

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25 ^{\circ}\text{C}$ (unless otherwise noted)

| | PARAMETER | FROM | TO | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|----------|----------|-------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | | C ₁ = 30 pF, | | 14 | 20 | |
| tPHL | Propagation delay time, high-to-low-level output | Terminal | Bus | See Figure 1 | | 14 | 20 | ns |
| tPLH | Propagation delay time, low-to-high-level output | Bus | | C ₁ = 30 pF, | | 10 | 20 | |
| tPHL | Propagation delay time, high-to-low-level output | | Terminal | See Figure 2 | | 15 | 22 | ns |
| tPZH | Output enable time to high level | | Bus | See Figure 3 | | 25 | 35 | |
| tPHZ | Output disable time from high level | TE | | | | 13 | 22 | |
| tPZL | Output enable time to low level | 15 | | | | 22 | 35. | ns |
| tPLZ | Output disable time from low level | | | | | 22 | 32 | 1 |
| tPZH | Output enable time to high level | | 7 | | | 20 | 30 | |
| tPHZ | Output disable time from high level | TE | T | See Figure 4 | | 12 | 20 | |
| tPZL | Output enable time to low level | I E | Terminal | | | 23 | 32 | ns |
| tPLZ | Output disable time from low level | 1 | | | | 19 | 30 | |
| t _{en} | Output pull-up enable time | PE | Bus | See Figure 5 | | 15 | 22 | ns |
| tdis | Output pull-up disable time |] , PE | | | | 13 | 20 | |

PARAMETER MEASUREMENT INFORMATION

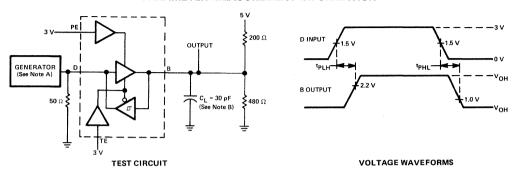


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

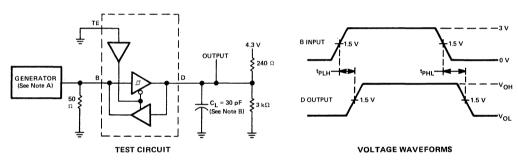


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

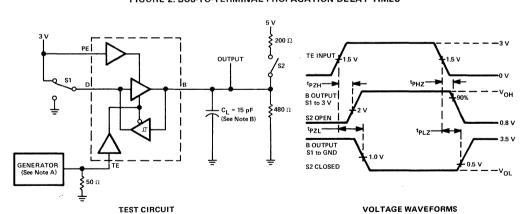


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, $t_f \le ns$, $Z_0 = 50 \Omega$.

B. CL includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

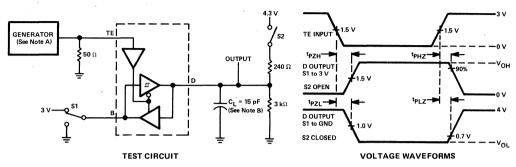


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

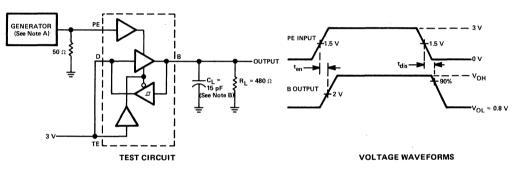
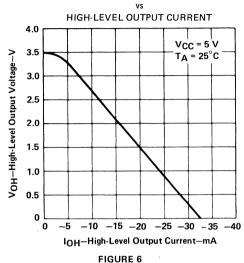


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

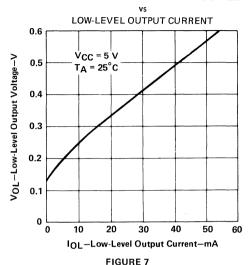
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ ns, $Z_0 =$ 50 Ω .

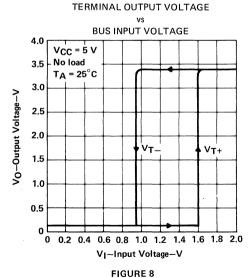
B. C_L includes probe and jig capacitance.

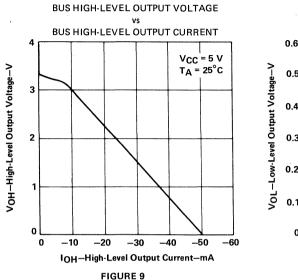


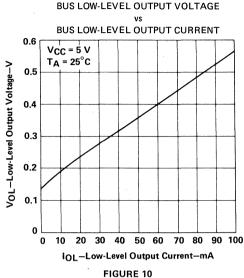


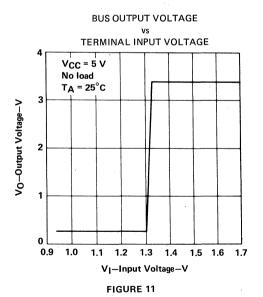
TERMINAL LOW-LEVEL OUTPUT VOLTAGE

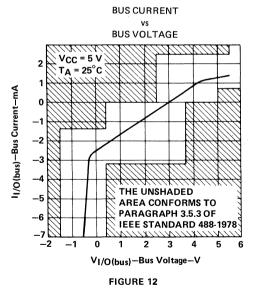












SN75161B, SN75162B OCTAL GENERAL PURPOSE INTERFACE BUS TRANSCEIVERS

D2618, OCTOBER 1980-REVISED OCTOBER 1985

MEETS IEEE STANDARD 488-1978 (GPIB)

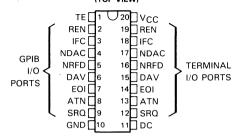
- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multi-Controllers
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)

description

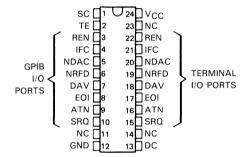
The SN75161B and SN75162B eight-channel general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75161B and SN75162B each features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power up/down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during VCC power-up and power-down. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

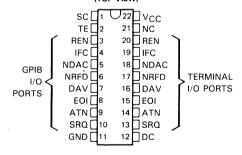
SN75161B . . . DW, J, OR N PACKAGE (TOP VIEW)



SN75162B . . . DW PACKAGE (TOP VIEW)



SN75162B . . . N PACKAGE (TOP VIEW)



NC-No internal connection

description (continued)

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage VCC is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

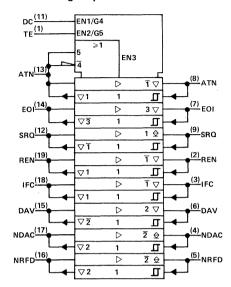
The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

| NAME | IDENTITY | CLASS |
|------|--------------------------------|------------|
| DC | Direction Control | |
| TE | Talk Enable | Control |
| sc | System Control (SN75162B only) | |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | |
| IFC | Interface Clear | Management |
| EOI | End or Identify | |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | ransier |

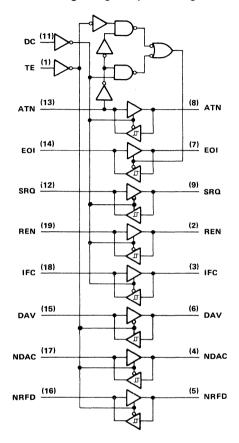
SN75161B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SN75161B logic symbol[†]

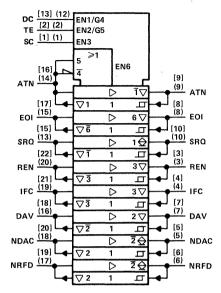


[†] This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.

SN75161B logic diagram (positive logic)



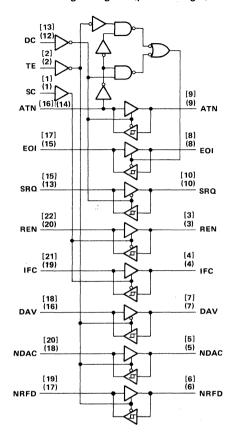
SN75162B logic symbol[†]



 $^{^{\}dagger}$ This symbol is in accordance with IEEE Std 91-1984 and IEC publication 617-12.

✓designates 3-state output, **♦**designates passive-pullup outputs.

SN75162B logic diagram (positive logic)



^[] Denotes pin numbers for DW package.

^() Denotes pin numbers for N package.

SN75161B RECEIVE/TRANSMIT FUNCTION TABLE

| (| CONTROLS BU | | | JS-MANA | S-MANAGEMENT CHANNELS | | | | DATA-TRANSFER CHANNE | | | |
|----|-------------|------------------|------------------|--------------------|-----------------------|-----|-----|---------|----------------------|----------|--|--|
| DC | TE | ATN [†] | ATN [†] | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD | | |
| | | | | (Controlled by DC) | | | | (Co | ntrolled b | y TE) | | |
| Н | Н | Н | | т | R | R | Т | _ | R | В. | | |
| Н | Н | L | R | ' | п | n | R | • • ' _ | n | R | | |
| L | L | Н | - | R | т | т | R | R | т | т | | |
| L | L | L | ' ' | n | n i | 1 | Т | n, | <u>'</u> | <u>'</u> | | |
| Н | L | Х | R | Т | R | R | R | R | Т | Т | | |
| L | Н | X | Т | R | Т | T | T | Т | R | R | | |

SN75162B RECEIVE/TRANSMIT FUNCTION TABLE

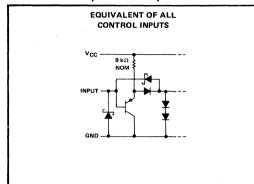
| CONTROLS | | | В | BUS-MANAGEMENT CHANNELS | | | | DATA-TRANSFER CHANNELS | | | | | | |
|----------|----|----|------|-------------------------|----------|-----------|-----------|------------------------|-----|-------------|------|---|---|--|
| sc | DC | TE | ATN† | ATN† | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD | | | |
| | | | | (Controlle | d by DC) | (Controll | ed by SC) | | (Co | ntrolled by | TE) | | | |
| | Н | Н | Н | | Τ | | | T | т. | R | R | | | |
| | Н | Н | L | R T | | | R | 1 | n | n | | | | |
| | L | L | Н | т - | R | | | R | R | т | т | | | |
| | L | L | L | | n | n | n | ' '' | | | • Т | n | 1 | |
| | H | L | Х | R | Т | | | R | R | Т | T | | | |
| | L | Н | Х | Т | R | | | T | T | R | R | | | |
| I | | | | | | Т | Т | | | | | | | |
| L | | | | | | R | R | | | | | | | |

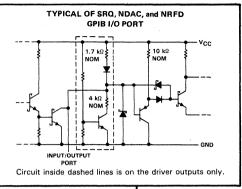
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

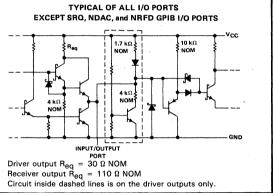
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†] ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Low-level driver output current |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Tab |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package 300° |
| Lead temperature 1.6 mm (1/16) inch from the case for 10 seconds: DW or N package 260° |

NOTES 1. All voltage values are with respect to network ground terminal.

2. In the J package, SN75161B chips are alloy mounted.



SN75161B, SN75162B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|-------------|---------------------------------------|---------------------------------|---------------------------|
| DW (20 Pin) | 1125 mW | 9.0 mW/°C | 720 mW |
| DW (24 Pin) | 1350 mW | 10.8 mW/°C | 864 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW |
| N (20 Pin) | 1150 mW | 9.2 mW/°C | 736 mW |
| N (22 Pin) | 1700 mW | 13.6 mW/°C | 1088 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|--------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, VIL | | | | 0.8 | V |
| High level and an annual level | Bus ports with 3-state outputs | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| 1 | Bus ports | | | 48 | |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST C | ONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------------|---|-----------------|--|---|------|------------------|----------------|------|
| VIK | Input clamp voltage | | I _I = -18 mA | | | -0.8 | -1.5 | V |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | | | 0.4 | 0.65 | | V |
| V _{OH} ‡ | High-level | Terminal | $I_{OH} = -800 \mu$ | A | 2.7 | 3.5 | | V |
| vOH. | output voltage | Bus | $I_{OH} = -5.2 \text{ m}$ | A | 2.5 | 3.3 | | · · |
| V | Low-level | Terminal | IOL = 16 mA | | | 0.3, | 0.5 | > |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA}$ | | | 0.35 | 0.5 | V |
| lı . | Input current at | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ |
| <u>'</u> | maximum input voltage | | <u>'</u> | | | | | |
| ΉΗ | High-level input current | Terminal and | V _I = 2.7 V | | | 0.1 | 20 | μΑ |
| I _{IL} | Low-level | control | V _I = 0.5 V | | | - 10 | -100 | μΑ |
| 'IL | input current | inputs | V ₁ 0.0 V | | | | | μ, , |
| V _{I/O(bus)} | Voltage at bus port | | Driver disabled | I _{I(bus)} = 0 | 2.5 | 3.0 | 3.7 | v |
| • 1/O(bus) | | | Diritor diodolog | $I_{I(bus)} = -12 \text{ mA}$ | | | - 1.5 | · |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | | | | |
| | | Power on | Driver disabled | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | |
| I _{I/O(bus)} | Current into bus port | | | V _{I(bus)} = 2.5 V to 3.7 V | | | + 2.5 - 3.2 | mA |
| | | | | V _{I(bus)} = 3.7 V to 5 V | 0 | | 2.5 | |
| | | | 1 | V _{I(bus)} = 5 V to 5.5 V | 0.7 | | 2.5 | |
| | | Power off | $V_{CC} = 0$, | V _{I(bus)} = 0 to 2.5 V | | | - 40 | μΑ |
| 1 | Short-circuit | Terminal | | | - 15 | - 35 | - 75 | ^ |
| los | output current | Bus | | | -25 | - 50 | -125 | mA |
| lcc | Supply current | | No load, | TE, DC, and SC low | | | 110 | mA |
| C _{i/o(bus)} | Bus-port capacitance | | $V_{CC} = 5 \text{ V to}$ $V_{I/O} = 0 \text{ to } 2$ | | | 30 | | pF . |

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. † VOH applies for 3-state outputs only.



switching characteristics, VCC = 5 V, CL = 15 pF, TA = 25 °C (unless otherwise noted)

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|----------|----------------------------|---|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | Terminal | Bus | C _L = 30 pF, | | 14 | 20 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | Terminal | Dus | See Figure 1 | | 14 | 20 | |
| tPLH | Propagation delay time, low-to-high-level output | Terminal | Bus (SRQ, NDAC NRFD) | C _L = 30 pF, See Figure 1 | | 29 | 35 | ns |
| ^t PLH | Propagation delay time, low-to-high-level output | Pug | Torminal | C _L = 30 pF, | | 10 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | bus | Bus Terminal | | | 15 | 22 | 115 |
| tPZH | Output enable time to high level | TE, DC, | BUS | | | | 60 | |
| ^t PHZ | Output disable time from high level | or | (ATTN, EOI, | See Figure 3 | | | 45 | ns |
| tPZL | Output enable time to low level | SC | REN, IFC, | occ rigure o | | | 60 | 113 |
| tPLZ | Output disable time from low level | 30 | and DAV) | | | | 55 | 1 |
| tPZH | Output enable time to high level | TE, DC, | | | | | 55 | |
| tPHZ | Output disable time from high level | i i | Terminal | See Figure 4 | | | 50 | ns |
| †PZL | Output enable time to low level | or SC | Tomman | 555guio 4 | | | 45 | 113 |
| tPLZ | Output disable time from low level | 30 | | | | | 55 | |

PARAMETER MEASUREMENT INFORMATION

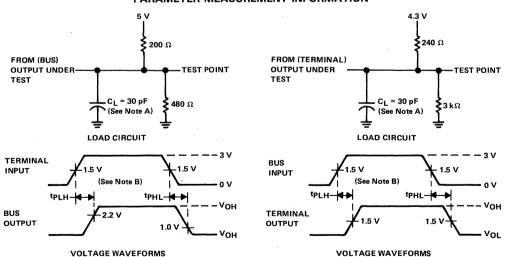


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. CL includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_0 = 50 \Omega$.



PARAMETER MEASUREMENT INFORMATION

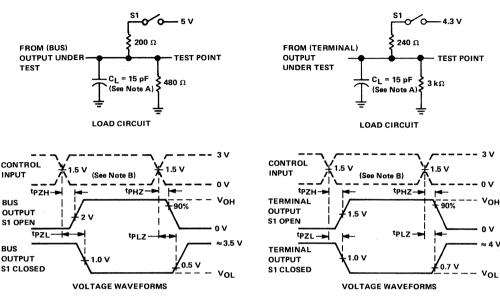


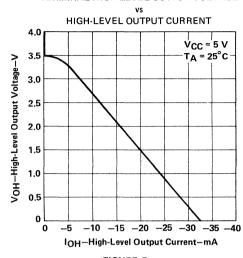
FIGURE 3. BUS ENABLE AND DISABLE TIMES

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{O} = 50 \Omega$.

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE



TERMINAL LOW-LEVEL OUTPUT VOLTAGE

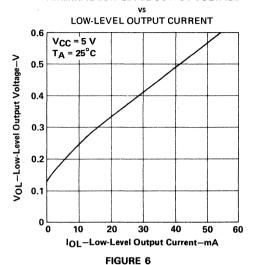
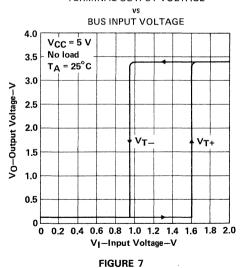
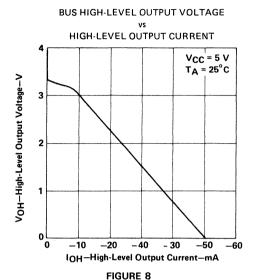


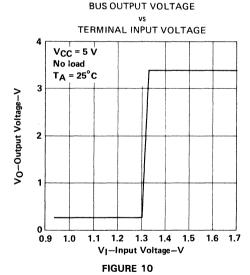
FIGURE 5

TERMINAL OUTPUT VOLTAGE

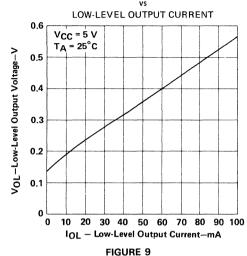


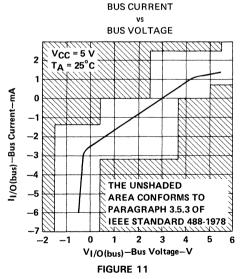


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BUS-LOW LEVEL OUTPUT VOLTAGE





SN75163B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2611, OCTOBER 1985

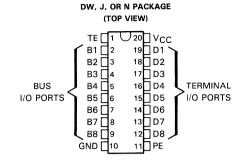
- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed Low-Power Schottky Circuitry
- Low Power Dissipation . . . 66 mW Max Per Channel
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (VCC=0)

description

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state modes. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 mV of hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$.

The SN75163B is characterized for operation from 0°C to 70°C.



FUNCTION TABLES

EACH DRIVER INPUTS OUTPUT

R

н

L

z

L

7

PE

Н

L

н

D TE

н н

L H H

н х

х

| EAGIT HEGETYETT | | | | | | | | | | |
|-----------------|-----|-------|--------|---|--|--|--|--|--|--|
| | - 1 | NPUTS | OUTPUT | | | | | | | |
| 1 | В | TE | PE | D | | | | | | |
| ı | L | L | Χ | L | | | | | | |
| ı | Н | L | Х | н | | | | | | |
| i | Х | Н | X | z | | | | | | |

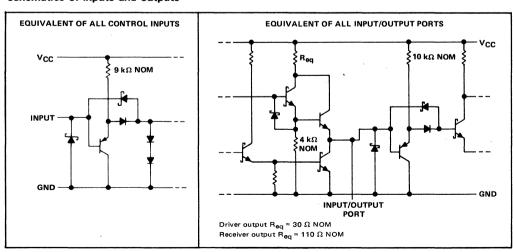
EACH DECEIVED

H = high level, L = low level, X = irrelevant, Z = high-impedance state

SN75163B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

logic symbol† logic diagram (positive logic) M1 [3S] M2 [0C] EN3 [XMT] D1 (19) EN4 [RCV] (2)_ B1 D1 (19) (<u>2)</u> B1 D2 (18) 3 (1 ▽/2 △) (<u>3)</u> B2 D2 (18) (<u>3)</u> B2 (<u>4)</u> B3 D3 (17) D3 <u>(17)</u> D4 (16) (5) B4 D5 (15) (6) · B5 D6 (14) (7) D4 (16) В6 D7 (13) (8) В7 (5) B4 TERMINAL D5 (15) BUS [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and (<u>6)</u> B5 IEC Publication 617-12. ∇ Designates 3-state outputs. D6 (14) ◆ Designates open-collector outputs. (7<u>)</u> B6 D7 (13) (<u>8)</u> B7

schematics of inputs and outputs



(12)

(9)

SN75163B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Low-level driver output current |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. In the J package, SN75163B chips are alloy mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT | |
|--|-------------------------------|------|---|------|------|--|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V | |
| High-level input voltage, VIH | | 2 | | | V | |
| Low-level input voltage, VIL | | | | 0.8 | V | |
| High-level output current, IOH | Bus ports with pullups active | | | 10 | mA | |
| | Terminal ports | | | -800 | μΑ | |
| I am tamel automate automate I am | Bus ports | | | 48 | ^ | |
| Low-level output current, IOL | Terminal ports | | | 16 | ⊢ mA | |
| Operating free-air temperature range, TA | | 0 | *************************************** | 70 | °C | |

SN75163B OCTAL GENERAL PURPOSE INTERFACE BUS TRANSCEIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT |
|-----------------------|--|----------|-----------------------------|--|------|------------------|-------|------|
| VIK | Input clamp voltage | | l ₁ = -18 mA | | | -0.8 | - 1.5 | ٧ |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) [‡] | Bus | | | 0.4 | 0.65 | | V |
| Voн | High level | Terminal | $I_{OH} = -800 \mu A$ | TE at 0.8 V | 2.7 | 3.5 | | V |
| VOH | output voltage | Bus | $I_{OH} = -10 \text{ mA},$ | PE and TE at 2 V | 2.5 | 3.3 | | V |
| VoL | Low-level | Terminal | IOL = 16 mA, | TE at 0.8 V | | 0.3 | 0.5 | V |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA},$ | PE and TE at 2 V | | 0.4 | 0.5 | · · |
| 1 | High-level output current | Bus | $V_0 = 5.5 V$, | PE at 0.8 V, | | | 100 | |
| Іон | (open-collector mode) | bus | D and TE at 2 V | D and TE at 2 V | | | 100 | μΑ |
| 1 | Off-state output current | D | PE at 2 V, | V _O = 2.7 V | | | 20 | _ |
| loz | (3-state mode) | Bus | TE at 0.8 V | V _O = 0.4 V | | | - 20 | μΑ |
| 1. | Input current at | Terminal | V _I = 5.5 V | | | 0.2 | 100 | |
| Ч | maximum input voltage | remina | V = 5.5 V | | | 0.2 | 100 | μΑ |
| 1 | High-level | T | V 27V | | | 0.1 | 20 | _ |
| ΉΗ | input current | Terminal | $V_1 = 2.7 V$ | - | | 0.1 | 20 | μΑ |
| 1 | Low-level | T | V _I = 0.5 V | | | - 10 | - 100 | |
| lir. | input current | Terminal | V = 0.5 V | | | - 10 | - 100 | μΑ |
| 1 | Short-circuit | Terminal | | | -15 | -35 | -75 | mA |
| los | output current | Bus | | | - 25 | - 50 | -125 | mA |
| loo | Supply ourrant | | No load | Receivers low and enabled | | | 80 | mA |
| Icc | Supply current | | INU IUAU | Drivers low and enabled | | | 100 | IIIA |
| Cuin | D | | V _{CC} = 5 V or 0, | $V_{I/O} = 0 \text{ to } 2 \text{ V},$ | | 30 | | nE. |
| C _{i/o(bus)} | Bus-port capacitance | | f = 1 MHz | | 30 | | | pF |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5, T_{A} = 25 $^{\circ}$ C.

switching characteristics, VCC = 5 V, CL = 15 pF, TA = 25 °C (unless otherwise noted)

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|----------|----------|-------------------------|---------|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | _ ` | | C _L = 30 pF, | | 14 | 20 | |
| ^t PHL | Propagation delay time, high-to-low-level output | Terminal | Bus | See Figure 1 | | 14 | 20 | ns |
| tPLH | Propagation delay time, low-to-high-level output | Bus | Terminal | C _I = 30 pF, | | 10 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | bus | Terminai | See Figure 2 | | 15 | 22 | ns |
| tPZH | Output enable time to high level | | Bus | | | 25 | 35 | |
| tPHZ | Output disable time from high level | TE | | See Figure 3 | 1 | 13 | 22 | ns |
| tPZL | Output enable time to low level | 1 '5 | bus | See Figure 3 | | 22 | 35 | IIS |
| tPLZ | Output disable time from low level | 1 | | | | 22 | 32 | |
| tPZH | Output enable time to high level | | | | | 20 | 30 | |
| tPHZ | Output disable time from high level | TE | Tamainal | Can Figure 4 | ŀ | 12 | 20 | |
| tPZL | Output enable time to low level | 1 15 | Terminal | See Figure 4 | 1 | 23 | 32 | ns |
| tPLZ | Output disable time from low level | 1 | | | | 19 | 30 | |
| t _{en} | Output pull-up enable time | PE | Tamainal | C Fi E | | 15 | 22 | |
| t _{dis} | Output pull-up disable time |] | Terminal | See Figure 5 | <u></u> | 13 | 20 | ns |

[‡]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

PARAMETER MEASUREMENT INFORMATION

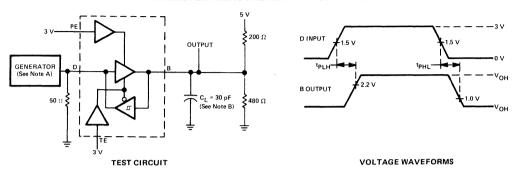


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

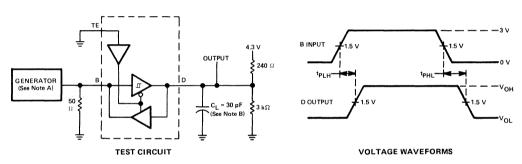


FIGURE 2, BUS-TO-TERMINAL PROPAGATION DELAY TIMES

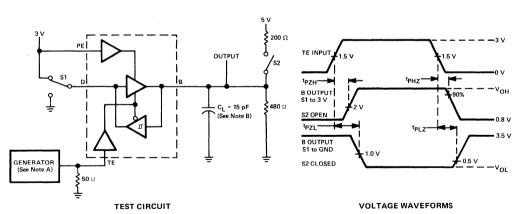


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ ns, $Z_0 =$ 50 Ω .

B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

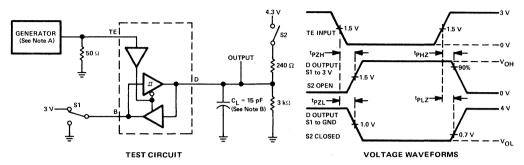


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

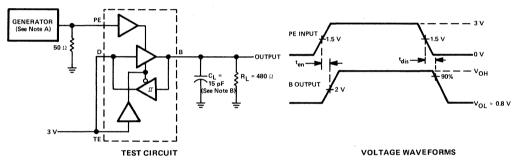
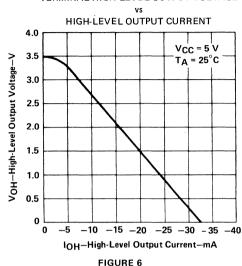


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

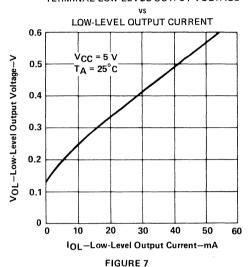
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ ns, $Z_0 =$ 50 Ω .

B. C_L includes probe and jig capacitance.

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE



TERMINAL LOW-LEVEL OUTPUT VOLTAGE



TERMINAL OUTPUT VOLTAGE

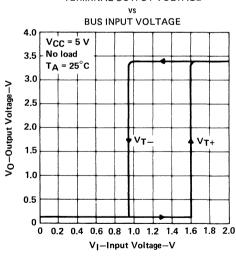
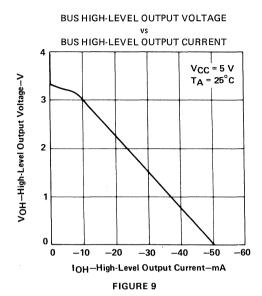
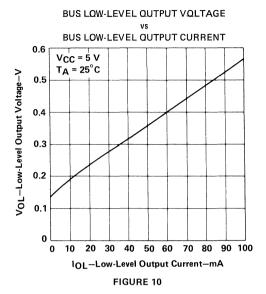


FIGURE 8





BUS OUTPUT VOLTAGE VS TERMINAL INPUT VOLTAGE VCC = 5 V No load TA = 25°C 2 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 V1-Input Voltage -V

FIGURE 11

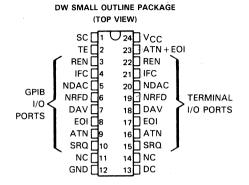
D2908, OCTOBER 1985

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- ATN + EOI (OR Function) Output to Simplify Board Layout
- Designed to Implement Control Bus Interface for Multi-Controllers
- Low-Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device is Powered Down (VCC = 0)

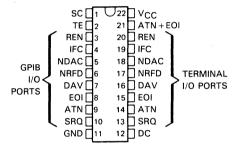
description

The SN75164B eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75164B provides the complete 16-wire interface for the IEEE 488 bus.

The SN75164B features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75164B is identical to the SN75162B with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.



N DUAL-IN-LINE PACKAGE (TOP VIEW)



NC-No internal connection.

CHANNEL IDENTIFICATION TABLE

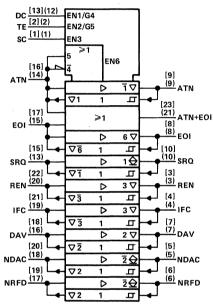
| NAME | IDENTITY | CLASS |
|-----------|--------------------|------------|
| DC | Direction Control | |
| TE | Talk Enable | Control |
| SC | System Control | |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | Management |
| IFC | Interface Clear | |
| EOI | End or Identify | |
| ATN + EOI | ATN logical OR EOI | Logic |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | 110113161 |

Texas Instruments

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

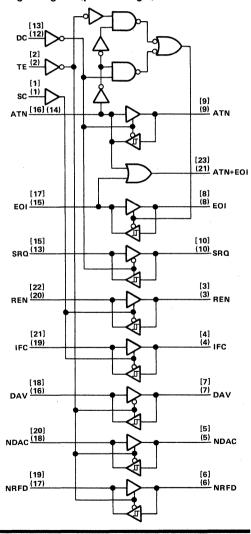
The SN75164B is manufactured in a 22-pin dual-in-line and 24-pin Small Outline package. The SN75164B is characterized for operation from 0° C to 70° C.

logic symbol†



¹This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



^[] Denotes pin numbers for DW package.
() Denotes pin numbers for N package.

SN75164B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

RECEIVE/TRANSMIT FUNCTION TABLE

| CONTROLS BUS-MANAG | | | | GEMENT CHANNELS | | | DATA-TRANSFER CHANNELS | | | | |
|--------------------|----|----|------------------|------------------|----------|------------|------------------------|-----|-----|-------------|------|
| SC | DC | TE | ATN [†] | ATN [†] | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD |
| | | | | (Controlle | d by DC) | (Controlle | d by SC) | | (Co | ntrolled by | TE) |
| | Н | Н | Н | R | + | | | Т | т | - | R |
| | Н | Н | L | · · | ' | | | R | , | R | n |
| | L | L | Н | 7 | R | | | R | R | т | т |
| | L | L | L | · . | n | | | Т | n | | ' |
| | Н | L | Х | R | T | | | R | R | Т | T |
| | L | Н | Х | Т | R | | | Т | Т | R | R |
| Н | | | | | | T | Т | | | | |
| L | | | | | | R | R | | | | |

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

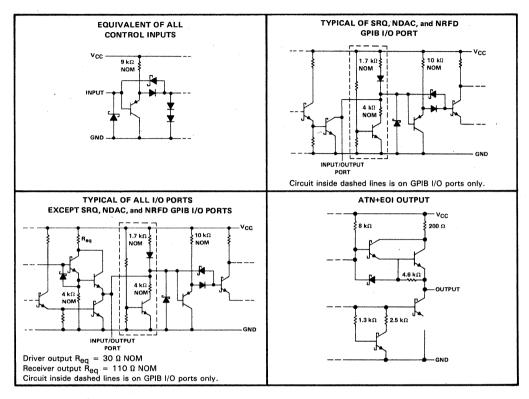
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†] ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

| INPL | JTS | OUTPUT |
|------|-----|-----------|
| ATN | EOI | ATN + EOI |
| Н | Х | Н |
| X | H | н |
| L | L | L |

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|---|
| Input voltage |
| Low-level driver output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| DW package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package 260°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

For operation above 25 °C free-air temperature, derate the DW package at the rate of 10.8 mW/°C, the N package at the rate of 13.6 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|--------------------------------|------|-----|-------|------|
| Supply voltage, V _{CC1} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, VIL | | | | 0.8 | V |
| | Bus ports with 3-state outputs | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | - 800 |] |
| | ATN + EOI | | | -400 | μΑ |
| | Bus ports | | | 48 | |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| | ATN + EOI | | | 4 | |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST COM | NDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|---------------------------------------|--|----------|-------------|-------|---------------|
| VIK | Input clamp voltage | | l _l = −18 mA | | | | -1.5 | V |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | | | 0.4 | | | V |
| | | Terminal | I _{OH} = -800 μA | | 2.7 | | | |
| VoH [‡] | High-level output voltage | Bus | I _{OH} = -5.2 mA | | 2.5 | | | V |
| | | ATN + EOI | I _{OH} = -400 μA | | 2.7 | | | 1 |
| | | Terminal | I _{OL} = 16 mA | | | | 0.5 | |
| VOL | Low-level output voltage | Bus | I _{OL} = 48 mA | | | | 0.5 | V |
| | | ATN + EOI | IOL = 4 mA | | | | 0.4 | |
| 1. | Input current at | Terminal § | V _I = 5.5 V | | | | 100 | μΑ |
| lį. | maximum input voltage | ATN, EOI | V _I = 5.5 V | | | | 200 | μΑ |
| | | Terminal, | V _I = 2.7 V | | | | 20 | |
| Ιн | High-level input current | control | V1 - 2.7 V | | <u> </u> | | | μΑ |
| | | ATN, EOI | V ₁ = 2.7 V | | | | 40 | |
| | | Terminal, | V _I = 0.5 V | | ŀ | | - 100 | Ī |
| IIL | Low-level input current | control | · | | <u> </u> | | | μΑ |
| **** | | ATN, EOI | $V_1 = 0.5 V$ | | | | - 500 | |
| V _{I/O(bus)} | Voltage at bus port | | Driver disabled | li(bus) = 0 | 2.5 | | 3.7 | l v |
| - I/O(bus/ | | | Dilver disabled | II(bus) = -12 mA | | | - 1.5 | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | - 1.3 | | | |
| | | | | $V_{l(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | |
| II/O(bus) | Current into bus port | Power on | Driver disabled | $V_{l(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$ | | | +2.5 | mA |
| ·I/O(bus) | Sarrent into Bas port | | 211101 01002100 | | ļ | | -3.2 | 1 |
| | | | | $V_{I(bus)} = 3.7 \text{ V to 5 V}$ $V_{I(bus)} = 5 \text{ V to 5.5 V}$ | 0 | | 2.5 | 1 |
| | | | | | 0.7 | | 2.5 | |
| | | Power off | V _{CC} = 0, | $V_{l(bus)} = 0 V to 2.5 V$ | | | -40 | μΑ |
| | | Terminal | | | - 15 | | - 75 | - |
| los | Short-circuit output current | Bus | | | -25 | | -125 | mA |
| | | ATN + EOI | | | -10 | | - 100 | |
| ICC | Supply current | *************************************** | No load, | TE, DC, and SC low | | | 120 | mA |
| C _{i/o(bus)} | Bus-port capacitance | | V _{CC} = 5 V to 0 V, | | 30 | | | pF |
| 1/0(003) | | | $V_{I/O} = 0 \text{ to } 2 \text{ V}$ | , f = 1 MHz | | | | <u> L</u> |

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies for three-state outputs only. § Except ATN and EOI terminal pins.



SN75164B OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25 \,^{\circ}\text{C}$ (unless otherwise noted)

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------|---|------------------------------------|----------------------------|---|-----|-----|-----|------|--|
| ^t PLH | Propagation delay time, low-to-high-level output | Terminal | Bus | C _L = 30 pF, | | 14 | 20 | ns | |
| ^t PHL | Propagation delay time, high-to-low-level output | Tommina | Jus | See Figure 1 | | 14 | 20 | | |
| ^t PLH | Propagation delay time, low-to-high-level output | Terminal | Bus (SRQ, NDAC NRFD) | C _L = 30 pF, See Figure 1 | | 29 | 35 | ns | |
| tPLH | Propagation delay time low-to-high-level output | Bus | Terminal | C _L = 30 pF, | | 10 | 20 | ns | |
| tPHL | Propagation delay time, high-to-low-level output | bus | , | See Figure 2 | | 15 | 22 | 115 | |
| ^t PLH | Propagation delay time, low-to-high-level output | Terminal ATN or Terminal EOI | ATN + EOI | See Figure 3 | | 14 | | ns | |
| tPHL | Propagation delay time, high-to-low-level output | Terminal ATN or Terminal EOI | ATN+EOI | See Figure 3 | | 14 | | ns | |
| tPZH | Output enable time to high level | TE, DC, | BUS | | | | 60 | | |
| ^t PHZ | Output disable time from high level | or | (ATTN, EOI, | See Figure 4 | | | 45 | ns | |
| ^t PZL | Output enable time to low level | sc sc | REN, IFC, | oco i iguio 4 | L | | 60 |] | |
| tPLZ | Output disable time from low level | | and DAV) | | | | 55 | | |
| ^t PZH | Output enable time to high level | TE, DC, | | | | | 55 |] | |
| tPHZ | Output disable time from high level | or | Terminal | See Figure 5 | L | | 50 | ns | |
| tPZL | Output enable time to low level | sc | | | | | 45 | | |
| ^t PLZ | Output disable time from low level | | | | 1 | | 55 | | |

PARAMETER MEASUREMENT INFORMATION 5 V 4.3 V 240 Ω **200** Ω FROM (BUS) FROM (TERMINAL) **OUTPUT UNDER TEST POINT** OUTPUT UNDER TEST POINT TEST TEST C_L = 30 pF C_L = 30 pF **480** Ω (See Note A) (See Note A) LOAD CIRCUIT LOAD CIRCUIT - - 3 V - 3 V TERMINAL BUS INPUT 1.5 V INPUT (See Note B) (See Note B) nν tPHL-₩ tPLH-^tPHL-₩-> Vон Vон BUS 2.2 V TERMINAL OUTPUT OUTPUT 1 5 V 15 V 1.0 V VOL νон VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS FIGURE 1. TERMINAL-TO-BUS FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES PROPAGATION DELAY TIMES TEST POINT Vcc TERMINAL 1.5 V ATN+EOI 0 V $2 k\Omega$ tPLH--tPHL-ATN+EOI FROM VOL ATN+EOI c_{L} **VOLTAGE WAVEFORMS** (See Note C) (See Note A)

FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_I includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns,
- $t_f \leq 6 \text{ ns, } Z_{OUT} = 50 \ \Omega.$ C. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

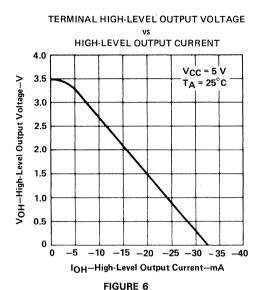
PARAMETER MEASUREMENT INFORMATION 200 Ω 240 O FROM (BUS) FROM (TERMINAL) OUTPUT UNDER **TEST POINT** OUTPUT TEST POINT TEST UNDER TEST C_L = 15 pF C_L = 15 pF 480 Ω $3 k\Omega$ (See Note A) (See Note A LOAD CIRCUIT LOAD CIRCUIT CONTROL CONTROL (See Note B) INPUT INPUT (See Note B) tPZHtPZHtPHZ-> tPHZ-> TERMINAL ۷он νон BUS 90% 90% OUTPUT OUTPUT 1.5 V S1 OPEN S1 OPEN nν 0 V tPZL tPLZtPLZtPZL-> ≈ 3.5 V BUS TERMINAL OUTPUT OUTPUT 0.5 V 0.7 V S1 CLOSED S1 CLOSED VOL VOL **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS**

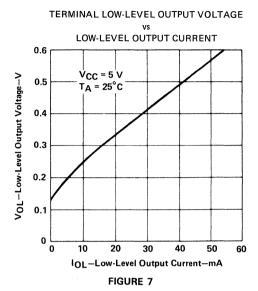
FIGURE 4. BUS ENABLE AND DISABLE TIMES

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \Omega$.





TERMINAL OUTPUT VOLTAGE

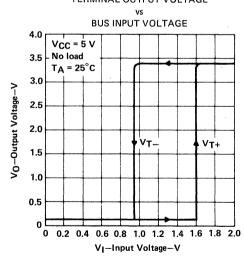
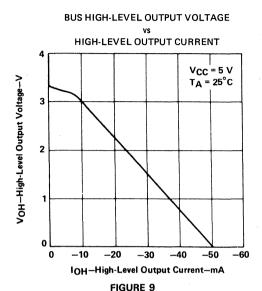
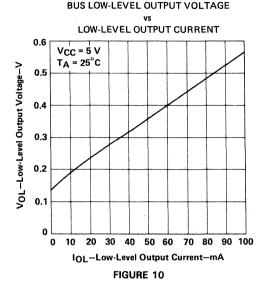
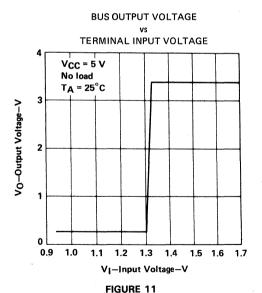


FIGURE 8







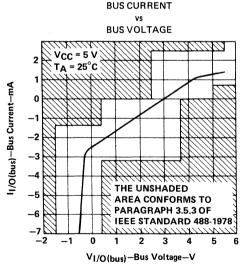


FIGURE 12

SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

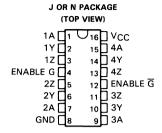
D2596, OCTOBER 1980-REVISED APRIL 1988

Meets EIA Standards RS-422-A and RS-485

- Meets CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range of -7 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Operates from Single 5-V Supply
- Low Power Requirements
- Functionally Interchangeable with AM26LS31

description

The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.



DW PACKAGE (TOP VIEW)

| 1A 🔲 1 | U 20 | □vcc |
|----------------|------|-----------|
| 1Y 🔲 2 | 19 |]4A |
| NC □3 | 18 |]4Y |
| 1Z []4 | 17 | NC |
| ENABLE G 5 | 16 | 4Z |
| 2Z []6 | 15 |]ENABLE G |
| NC □7 | 14 |] 3Z |
| 2Y 🛮 8 | 13 |]NC |
| 2A 🛮 9 | 12 |]3Y |
| GND []1 | 0 11 |]3A |

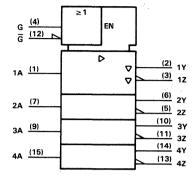
NC-No internal connection

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150 °C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

logic symbol†



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

FUNCTION TABLE (EACH DRIVER)

| | INPUT | ENA | BLES | OUTPUTS | | |
|---|-------|-----|------|---------|-----|--|
| | Α | G | G | Υ | , Z | |
| | H | Н | Х | Н | L | |
| | L | Н | х | L | н | |
| | н | Х | L | Н | L | |
| | L | х | L | L | Н | |
| 1 | Х | L | Н | Z | Z | |

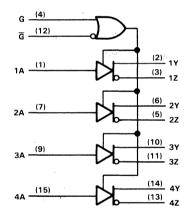
H = high level

L = low level

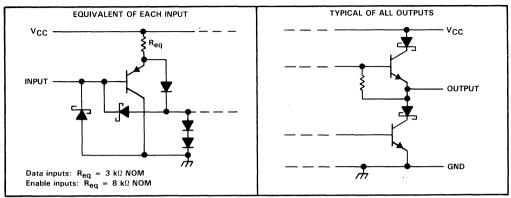
X = irrelevant

Z = high impedance (off)

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

| Supply voltage, VCC | . 7 V | |
|---|-------|--|
| Input voltage | 5.5 V | |
| Continuous total dissipation See Dissipation Rating | Table | |
| Operating free-air temperature range | 70°C | |
| Storage temperature range65°C to 1 | 50°C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package | 300°C | |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: DW or N package 2 | 260°C | |

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|----------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Common-mode output voltage, VOC | | | -7 to 12 | V |
| High-level output current, IOH | | | - 60 | mA |
| Low-level output current, IOL | | | 60 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75172 QUADRUPLE DIFFERENTIAL LINE DRIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CON | DITIONS | MIN | TYP [†] | MAX | UNIT | |
|-------------------|---|---|---------------------------------------|--------------------|------------------|-------|------|--|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V | |
| ٧o | Output voltage | I _O = 0 | | 0 | | 6 | ٧ | |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 6 | V | |
| VOD2 | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | ½ V _{OD1} | | | V | |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V | |
| V _{OD3} | Differential output voltage | See Note 2 | | 1.5 | | 5 | V | |
| Δ V _{OD} | Change in magnitude of differential output voltage [‡] | | | | | ±0.2 | ٧ | |
| Voc | Common-mode output voltage§ | $R_L = 54 \Omega \text{ or } 100 \text{ s}$ | | | +3 -1 | ٧ | | |
| Δ V _{OC} | Change in magnitude of common-mode output voltage [‡] | | | | | ±0.2 | ٧ | |
| 10 | Output current with power off | $V_{CC} = 0$, | $V_0 = -7 \text{ V to } 12 \text{ V}$ | | | ±100 | μΑ | |
| loz | High-impedance-state output current | $V_0 = -7 \text{ V to } 12$ | V | | | ±100 | μΑ | |
| ЧН | High-level input current | V _I = 2.7 V | | | | 20 | μΑ | |
| ΊL | Low-level input current | V _I = 0.5 V | | | | - 360 | μΑ | |
| | | $V_0 = -7 V$ | , | | | - 180 | | |
| los | Short-circuit output current | Vo = Vcc | | | | 180 | mA | |
| | | V _O = 12 V | | | | 500 | | |
| 1 | Supply surrent (all drivers) | No load | Outputs enabled | | 38 | 60 | | |
| ₁ CC | Supply current (all drivers) | INO IORO | Outputs disabled | | 18 | 40 | mA | |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|------------------------------------|-----------------------------------|
| ٧o | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | V _o | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| 12/1 | | V _t (Test Termination) |
| VOD3 | | Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| V _{OC} | Vos | V _{os} |
| Δ V _{OC} | Vos-Vos | V _{os} -V _{os} |
| los | I _{sa} , I _{sb} | |
| Io | I _{xa} , I _{xb} | lia, lib |

[‡] ∆|V_{OD}| and ∆|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

[§] In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}. NOTE 2: See EIA Standard RS-485 Figure 3-5, Test Termination Measurement 2.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | | TYP | MAX | UNIT |
|------------------|-------------------------------------|----------------------|--------------|--|-----|-----|------|
| tDD | Differential-output delay time | $R_1 = 54 \Omega$. | See Figure 2 | | 45 | 65 | ns |
| tTD | Differential-output transition time | n[= 54 11, | See rigure 2 | | 80 | 120 | ns |
| ^t PZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 3 | | 80 | 120 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 4 | | 45 | 80 | ns |
| ^t PHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 3 | | 78 | 115 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 4 | | 18 | 30 | ns |

PARAMETER MEASUREMENT INFORMATION

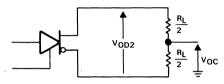


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

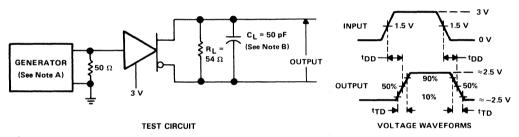


FIGURE 2. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_0 = 50$ Ω .

B. C_L includes probe and stray capacitance.

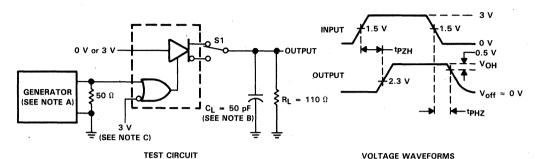


FIGURE 3. tPZH AND tPHZ

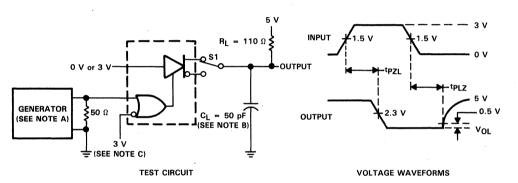
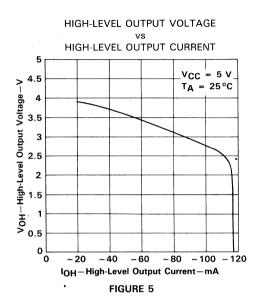
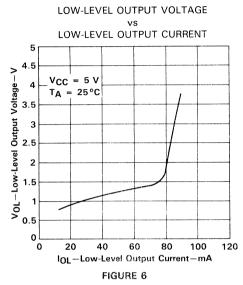


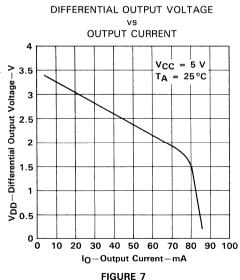
FIGURE 4. tpzL AND tpLZ

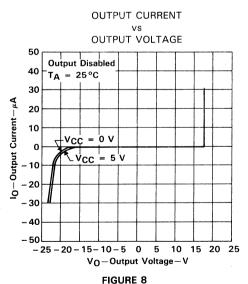
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $t_f \le 5$ ns

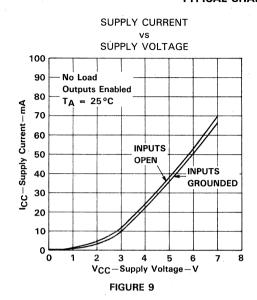
- B. C₁ include probe and jig capacitance.
- C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

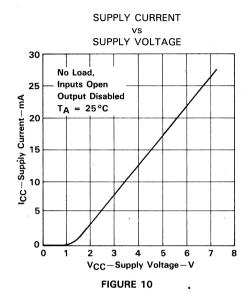




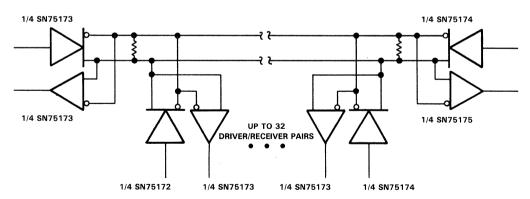








TYPICAL APPLICATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11



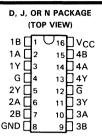
D2600, OCTOBER 1980-REVISED JULY 1990

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . − 12 to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-V Supply
- Low Power Requirements
- Plug-In Replacement for AM26LS32

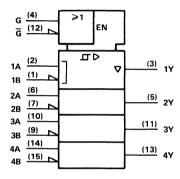
description

The SN75173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of - 12 to 12 V. Fail safe design ensures that if the inputs are open circuited, the outputs will always be high. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN75173 is characterized for operation from 0 °C to 70 °C.

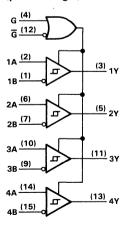


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Texas V

FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENA | BLES | OUTPUT |
|----------------------------------|-----|------|--------|
| A-B | G | G | Υ |
| V _{ID} ≥ 0.2 V | Н | Х | Н |
| VID ≥ 0.2 V | Х | L | н |
| -0.2 V < V _{ID} < 0.2 V | Н | Х | ? |
| -0.2 V < VID < 0.2 V | X | L | ? |
| V _{ID} ≤ -0.2 V | Н | X | L |
| V _{ID} ≤ -0.2 V | Х | L | L |
| X | L | Н | Z |

H = high level

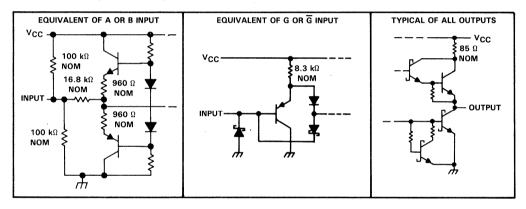
L = low level

X = irrelevant

? = indeterminate

Z = high impedance (off)

schematics of inputs and outputs



| absolute maximum ratings over operating free-air temperature range (unless otherwise noted) |
|--|
| Supply voltage, VCC (see Note 1) |
| Input voltage, A or B inputs |
| Differential input voltage (see Note 2) |
| Enable input voltage |
| Low-level output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| D package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |
| NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal. |
| 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input. |
| 3. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/°C, the |

J package to 656 mW at 70 °C at the rate of 8.2 mW/ °C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/ °C.

recommended operating conditions

In the J package, SN75173 chips are glass mounted.

| | | MIN | NOM | MAX | UNIT |
|---|---|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | ٧ |
| Common-mode input voltage, V _{IC} | : | | | ±12 | ٧ |
| Differential input voltage, V _{ID} | | | | ±12 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| High-level output current, IOH | | | | -400 | μΑ |
| Low-level output current, IOL | | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

SN75173 OUADRUPLE DIFFERENTIAL LINE RECEIVER

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|---|---|--------------------------|-------------------|------------------|-------|------|
| V _{TH} | Differential-input high-threshold voltage | $V_0 = 2.7 V$ | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$, | I _O = 16 mA | -0.2 [‡] | | | V |
| V _{hys} | Hysteresis [§] | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | - 1.5 | V |
| Voн | High-level output voltage | V _{ID} = 200 mV, | $I_{OH} = -400 \mu A$ | 2.7 | | | V |
| VOL | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ | I _{OL} = 8 mA | | | 0.45 | V |
| *UL , | | VID - 200 IIIV, | $I_{OL} = 16 \text{ mA}$ | | | 0.5 | Ľ |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | | | | ±20 | μΑ |
| h | Line input current | Other input at 0 V, | V _I = 12 V | | | 1 | mA |
| <u> </u> | Ene input current | See Note 4 | V _I = -7 V | | | -0.8 | '''^ |
| ЧН | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| 1 _L | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| r _i | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current¶ | | | - 15 | | -85 | mA |
| Icc | Supply current | Outputs disabled | | | | 70 | mA |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

NOTE 4: Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

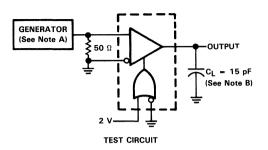
switching characteristics, VCC = 5 V, TA = 25 °C

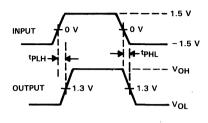
| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V, } C_L = 15 \text{ pF,}$ | | | 20 | 35 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | See Figure 1 | | | 22 | 35 | ns |
| tPZH | Output enable time to high level | C _L = 15 pF, | See Figure 2 | | 17 | 22 | ns |
| tPZL | Output enable time to low level | C _L = 15 pF, | See Figure 3 | | 20 | 25 | ns |
| tPHZ | Output disable time from high level | $C_L = 5 pF$, | See Figure 2 | | 21 | 30 | ns |
| tPLZ | Output disable time from low level | $C_L = 5 pF$, | See Figure 3 | | 30 | 40 | ns |

[‡]The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

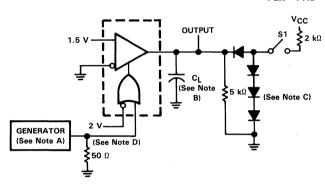
Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

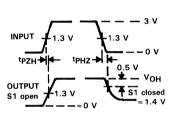




VOLTAGE WAVEFORMS

FIGURE 1. tPLH, tPHL





TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 2. tpHZ, tpZH

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{OUT} =$ 50 Ω .
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N916 or equivalent.
 - D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

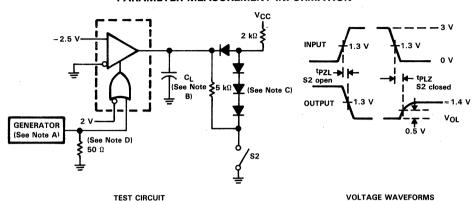


FIGURE 3. tPZL, tPLZ

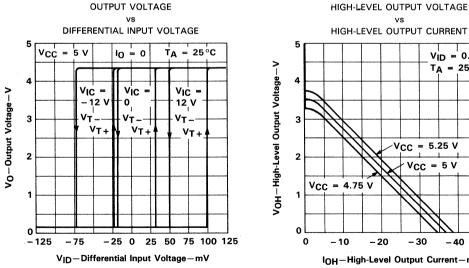
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \le 6 \text{ ns}, t_f \le 6 \text{ ns}, Z_{out} = 50 \Omega.$

B. CL includes probe and jig capacitance.

FIGURE 4

- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

TYPICAL CHARACTERISTICS



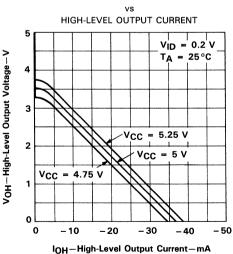
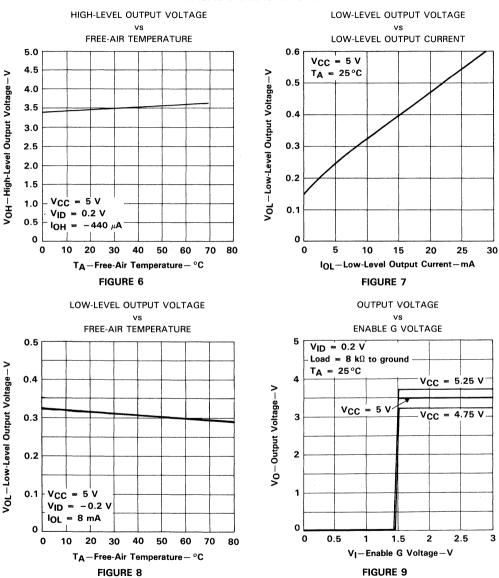
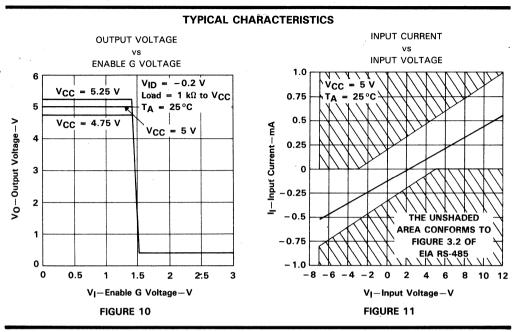
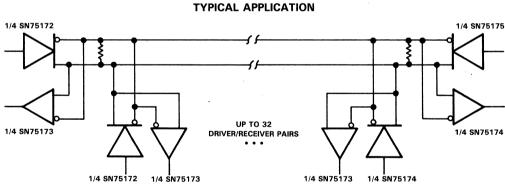


FIGURE 5







NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D2601, OCTOBER 1980-REVISED MAY 1988

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range of -7 V to 12 V
- Active-High Enable
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Operates from Single 5-V Supply
- Low Power Requirements
- Functionally Interchangeable with MC3487

description

The SN75174 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negativecurrent limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150 °C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

| INPUT | ENABLE | OUTP | UTS |
|-------|--------|------|-----|
| INPUT | ENABLE | Υ | Z |
| Н | н | Н | L |
| L | н | L | Н |
| X | L | Z | Z |

H = TTL high level, L = TTL low level,

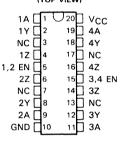
X = irrelevant,

Z = High impedance (off)

J OR N PACKAGE (TOP VIEW)

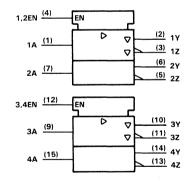
| 1A | □1 | U_{16} | | VCC |
|-------|----------|----------|--------|-------|
| 1Y | 2 | 15 | | 4A |
| 1Z | □3 | 14 | | 4Y |
| 1,2EN | □4 | 13 | | 4Z |
| 2Z | □5 | 12 | \Box | 3,4EN |
| 2Y | □6 | 11 | | 3Z |
| 2A | \Box 7 | 10 | | 3Y |
| GND | Πa | a | П | 3A |

DW PACKAGE (TOP VIEW)



NC-No internal connection

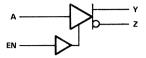
logic symbol†



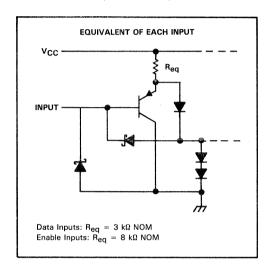
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

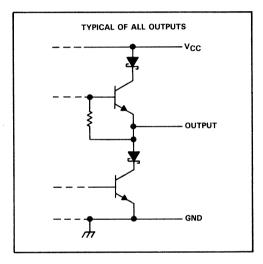


logic diagram, each driver (positive logic)



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package 260 °C |

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|----------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-Level input voltage, V _{IL} | | | 0.8 | V |
| Common-mode output voltage, VOC | | | -7 to 12 | V |
| High-level output curent, IOH | | | -60 | mA |
| Low-level output current, IOL | | | 60 | mA |
| Operating free-air temperature, T _A | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONI | DITIONS | MIN | TYP [†] | MAX | UNIT | |
|-------------------|---|--|---------------------------------------|-------------------|------------------|------------|------|--|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V | |
| Vон | High-level output voltage | V _{IH} = 2 V, I _{OH} = -33 mA | V _{IL} = 0.8 V, | | 3.7 | | ٧ | |
| VoL | Low-level output voltage | V _{IH} = 2 V, I _{OL} = 33 mA | V _{IL} = 0.8 V, | | 1.1 | | ٧ | |
| Vo | Output voltage | 10 = 0 | | 0 | | 6 | V | |
| V _{OD1} | Differential output voltage | 10 = 0 | | 1.5 | | 6 | V | |
| V _{OD2} | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | ½ V _{OI} | D1 | | ٧ | |
| . 002. | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V | |
| V _{OD3} | Differential output voltage | See Note 2 | | 1.5 | | 5 | V | |
| Δ V _{OD} | Change in magnitude of differential output voltage [‡] | | | | | ±0.2 | ٧ | |
| Voc | Common mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | + 3 – 1 | V | |
| 4 Voc | Change in magnitude of common mode output voltage [‡] | | | | | ±0.2 | V | |
| 10 | Output current with power off | V _{CC} = 0, | $V_0 = -7 \text{ V to } 12 \text{ V}$ | 1 | | ±100 | μΑ | |
| loz | High-impedance-state output current | $V_0 = -7 \text{ V to } 12 \text{ V}$ | | | | ±100 | μΑ | |
| ΊΗ | High-level input current | V _I = 2.7 V | | | | 20 | μΑ | |
| lir. | Low-level input current | V ₁ = 0.5 V | | | | -360 | μΑ | |
| | | $V_0 = -7 V$ | | | | -250 | | |
| los | Short-circuit output current | Vo = Vcc | | | | 180 | mA | |
| | * | V _O = 12 V | | | | 500 | 1 | |
| | | No load | Outputs enabled | | 38 | 60 | mA | |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C.

^{*}Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|----------------------|--------------|-----|-----|-----|------|
| tDD | Differential-output delay time | $R_1 = 54 \Omega$ | See Figure 2 | | 45 | 65 | ns |
| tTD | Differential-output transition time | 1" = 54 11, | See rigule 2 | | 80 | 120 | ns |
| tPZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 3 | | 80 | 120 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 4 | | 55 | 80 | ns |
| tPHZ | Outut disable time from high level | $R_L = 110 \Omega$, | See Figure 3 | | 75 | 115 | ns |
| ^t PLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 4 | | 18 | 30 | ns |

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|-----------------------------------|--|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | . V _o | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| VOD3 | | V _t (Test Termination Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | Vos | V _{os} |
| Δ V _{OC} | Vos - Vos | V _{os} − V̄ _{os} |
| los | I _{sa} , I _{sb} | |
| 10 | I _{xa} , I _{xb} | l _{ia} , l _{ib} |

PARAMETER MEASUREMENT INFORMATION

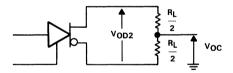
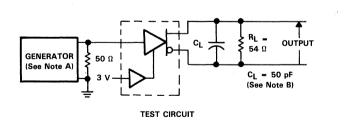
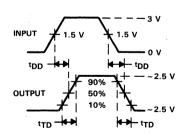


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES





VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_0 = 50$ Ω .
 - B. C_L includes probe and stray capacitance.

FIGURE 2. DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



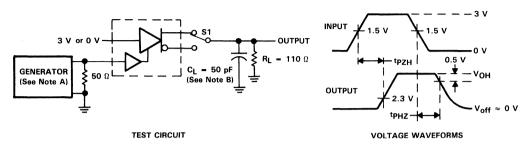


FIGURE 3. tpzH AND tpHZ

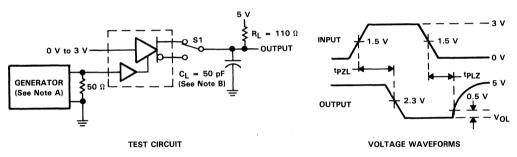
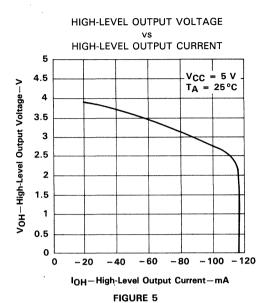
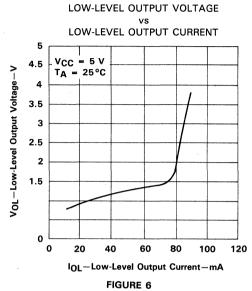
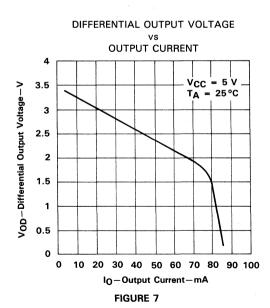


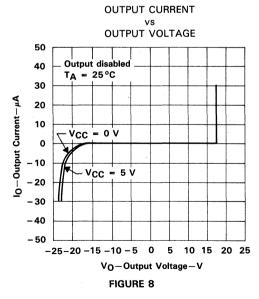
FIGURE 4. tpzi AND tpLZ

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_{\rm f} \leq 5~{\rm ns},~{\rm Z_O} = 50~\Omega.$ B. C_L includes probe and stray capacitance.

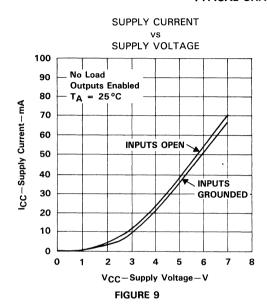


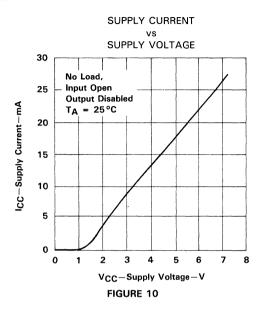




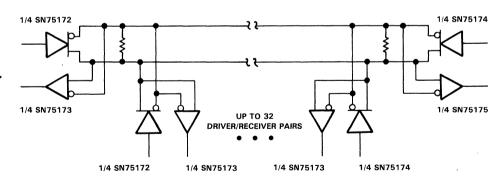








TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11



D2602, OCTOBER 1980-REVISED SEPTEMBER 1989

10 3A

7 3B

- Meets EIA Standards RS-422-A, RS-423-A, and RS-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common Mode Input Voltage Range
 12 V to 12 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-V Supply
- Low Power Requirements
- Plug-in Replacement for MC3486

description

The SN75175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A, RS-423-A, and RS-485 and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of ± 12 V. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

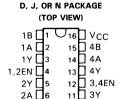
The SN75175 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL INPUTS A — B | ENABLE | OUTPUT Y |
|---|--------|-------------|
| V _{ID} ≥ 0.2 V | Н | Н |
| $-0.2 \text{ V} < \text{V}_{\text{1D}} < 0.2 \text{ V}$ | Н | ? |
| V _{ID} ≥ -0.2 V | Н | L |
| X | L | Z |

H = high level, L = low level, ? = indeterminate,

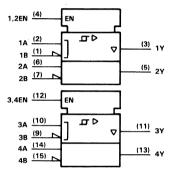
X = irrelevant, Z = high impedance (off)



2B 🗖 7

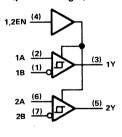
GND Π

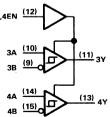
logic symbol†



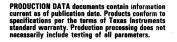
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



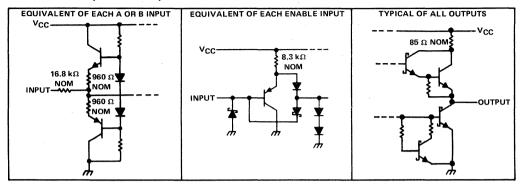


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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Input voltage, A or B inputs |
|---|
| Enable input voltage |
| Low-level output current |
| · |
| 0 di |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| D package |
| J package |
| N Package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package $\dots -260^{\circ}\text{C}$ |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

3. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/°C, the J package to 656 mW at 70 °C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C. In the J package, SN75175 chips are glass mounted.

recommended operating conditions

| | ٨ | ΛIN | NOM | MAX | UNIT |
|---|----|-----|-----|------|------|
| Supply voltage, VCC | 4. | .75 | 5 | 5.25 | ٧ |
| Common-mode input voltage, VIC | | | | ±12 | V |
| Differential input voltage, V _{ID} | | | | ±12 | V |
| High-level enable input voltage, VIH | | 2 | | | V |
| Low-level enable input voltage, V _{IL} | | | | 0.8 | ٧ |
| High-level output current, IOH | | | | -400 | μА |
| Low-level output current, I _{OL} | | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|---|---|-------------------------|-------------------|------------------|-------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 \text{ V}, \qquad I_0 = -0.4 \text{ mA}$ | 1 | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_{O} = 0.5 \text{ V}, \qquad I_{O} = 16 \text{ mA}$ | | -0.2 [‡] | | | V |
| V _{hys} | Hysteresis [§] | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | - 1.5 | V |
| Voн | High-level output voltage | $V_{ID} = 200 \text{ mV}, I_{OH} = -400 \mu$ | A, See Figure 1 | 2.7 | | | V |
| VOL | Low-level output voltage | V _{ID} = -200 mV, See Figure 1 | I _{OL} = 8 mA | | | 0.45 | V |
| - 01 | | TID TOO MIT, GOOD TIGGING T | I _{OL} = 16 mA | | | 0.5 | |
| loz | High-impedance-state output current | V _O = 0.4 V to 2.4 V | , | | | ± 20 | μΑ |
| 4. | Line input current | Other input at 0 V, | V _I = 12 V | | | 1 | mA |
| 11 | Line input current | See Note 4 | $V_{I} = -7 V$ | | | -0.8 | IIIA |
| ΉΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| IIL. | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| ri | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | | | - 15 | | - 85 | mA |
| lcc | Supply current | Outputs disabled | | | | 70 | mA |

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | | TYP | MAX | UNIT |
|------------------|--|-------------------------|----------------|--|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | C _I = 15 pF, | See Figure 2 | | 22 | 35 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | CL = 15 pr, | See Figure 2 | | 25 | 35 | ns |
| tPZH | Output enable time to high level | $C_{l} = 15 pF_{r}$ | See Figure 3 | | 13 | 30 | ns |
| tPZL | Output enable time to low level | С[— 15 рг, | See Figure 5 , | | . 19 | 30 | ns |
| tPHZ | Output disable time from high level | $C_1 = 15 pF$ | See Figure 3 | | 26 | 35 | ns |
| ^t PLZ | Output disable time from low level | С[= 15 рг, | See Figure 3 | | 25 | 35 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The algebraic convention, in which the less postitive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_T_. See Figure 4.

Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. NOTE 4: Refer to EIA standards RS-422-A, RS-423-A, and RS-485 for exact conditions.

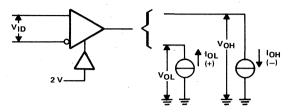


FIGURE 1. VOH, VOL

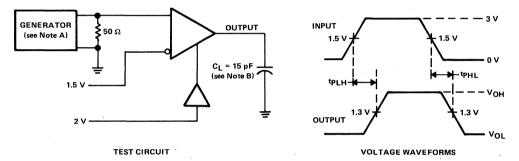
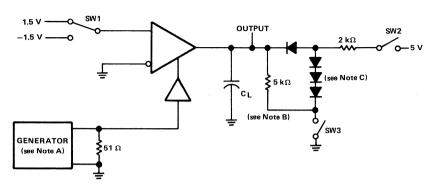


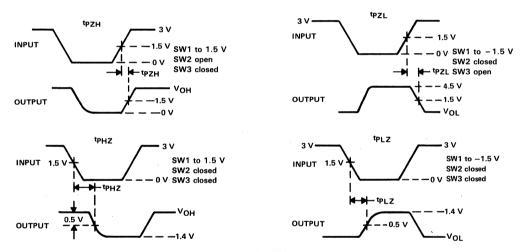
FIGURE 2. PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_{\text{f}} \leq$ 6 ns, $t_{\text{f}} \leq$ 6 ns, $t_{\text{out}} =$ 50 Ω .

B. CL includes probe and stray capacitance.



TEST CIRCUIT

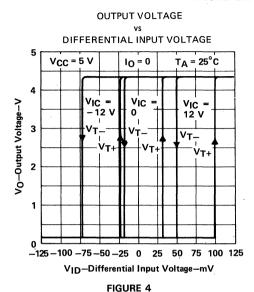


VOLTAGE WAVEFORMS

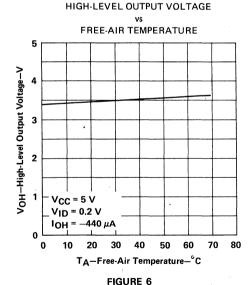
FIGURE 3. ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_f \leq 6$ ns, $t_{r} \leq 6 \text{ ns, } Z_{OUT} = 50 \ \Omega.$ B. CL includes probe and stray capacitance.

- C. All diodes are 1N916 or equivalent.







HIGH-LEVEL OUTPUT VOLTAGE
vs

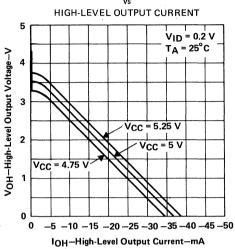


FIGURE 5

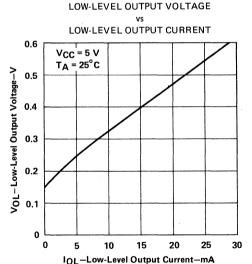


FIGURE 7

LOW-LEVEL OUTPUT VOLTAGE OUTPUT VOLTAGE FREE-AIR TEMPERATURE **ENABLE VOLTAGE** 0.5 5 V_{CC} = 5 V $V_{ID} = 0.2 V$ $V_{ID} = -0.2 V$ Load = 8 $k\Omega$ to ground Vol -Low-Level Output Voltage-V IOL = 8 mA $T_A = 25^{\circ}C$ V_{CC} = 5.25 V Vo-Output Voltage-V Vcc = 5 V V_{CC} = 4.75 V 3 0.3 0.2 1 0 0 0 10 20 30 40 50 60 70 80 0 0.5 1 1.5 2 3 2.5 TA-Free-Air Temperature-°C V_I-Enable Voltage-V FIGURE 8 FIGURE 9 **OUTPUT VOLTAGE** SUPPLY CURRENT (ALL RECEIVERS) **ENABLE VOLTAGE** SUPPLY VOLTAGE 6 100 VID = -0.2 V V_{CC} = 5.25 V No load Load = 1 k Ω to VCC Inputs open 90

TYPICAL CHARACTERISTICS

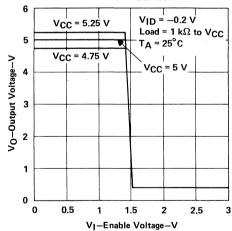
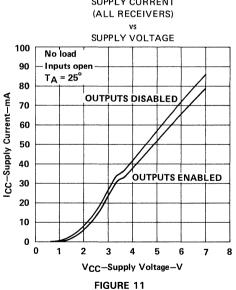


FIGURE 10



INPUT CURRENT **INPUT VOLTAGE** 0.75 $T_A = 25^{\circ}C$ 0.5 I|-Input Current-mA 0.25 -0.25 THE UNSHADED -0.5 AREA CONFORMS TO FIGURE 3.2 OF -0.75 EIA RS-485 -2 8 10 12

FIGURE 12

V_I-Input Voltage-V

TYPICAL APPLICATION 1/4 SN75172 UP TO 32 DRIVER/RECEIVER PAIRS 1/4 SN75173 1/4 SN75173 1/4 SN75174 FIGURE 13

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

D2619, JUNE 1984-REVISED AUGUST 1989

- Bidirectional Transceiver
- Meets EIA Standards RS-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability. . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27.

The SN75176A combines a 3-state differential line driver and a differential-input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or VCC = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

D OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (DRIVER)

| INPUT | ENABLE | OUTPUTS | | |
|-------|--------|---------|---|--|
| D | DE | Α | В | |
| Н | Н | Н | L | |
| L | н | L | н | |
| / x | L | z | Z | |

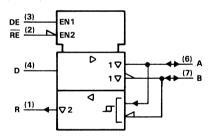
FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|--|--------------|-------------|
| V _{ID} ≥ 0.2 V | L | Н |
| $-0.2 \text{ V} < \text{V}_{1D} < 0.2 \text{ V}$ | L | ? |
| V _{ID} ≤ -0.2 V | L | L |
| × | н | z |

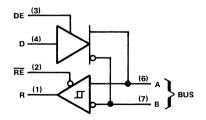
H = high level, L = low level, ? = indeterminate,

X = irrelevant, Z = high impedance (off)

logic symbol



logic diagram (positive logic)



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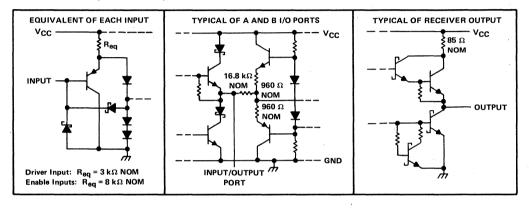


description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positiveand negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150 °C. The receiver features a minimum input impedance of 12 k Ω , input sensitivity of \pm 200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|---|-----------|
| Voltage at any bus terminal | / to 15 V |
| Enable input voltage | 5.5 V |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): | |
| D package | 725 mW |
| P package | 000 mW |
| Operating free-air temperature range | to 70°C |
| Storage temperature range65°C 1 | to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260°C |

- NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
 - 2. For operation above 25 °C free-air temperature, derate the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C and derate the P package to 640 mW at 70 °C at the rate of 8.0 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common-mode), V _I or V _{IC} | | -7 | | 12 | V |
| High-level input voltage, VIH | D, DE, and RE | 2 | | | V |
| Low-level input voltage, V _{IL} | D, DE, and RE | | | 0.8 | V |
| Differential input voltage, V _{ID} (see Note 3) | | | | ±12 | V |
| High lavel autout average I | . Driver | | | - 60 | mA |
| High-level output current, IOH | Receiver | | | -400 | μΑ |
| Nove local systems are seen at 1- | Driver | | | 60 | |
| Low-level output current, IOL | Receiver | | | 8 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|---|--|-----|------------------|--------------------|----------|
| V _{IK} | Input clamp voltage | I _I = -18 mA | | | | -1.5 | ٧ |
| Vон | High-level output voltage | $V_{IH} = 2 V$, $I_{OH} = -33 \text{ mA}$ | V _{IL} = 0.8 V, | | 3.7 | | V |
| VOL | Low-level output voltage | V _{IH} = 2 V, I _{OL} = 33 mA | V _{IL} = 0.8 V, | | 1.1 | | V |
| V _{OD1} | Differential output voltage | I _O = 0 | | | | 2 V _{OD2} | ٧ |
| V _{OD2} | Differential output voltage | $R_{L} = 100 \Omega,$ $R_{L} = 54 \Omega,$ | See Figure 1 See Figure 1 | 1.5 | 2.7 2.4 | | V |
| Δ V _{OD} | Change in magnitude of differential output voltage [‡] | | | | | ±0.2 | V |
| Voc | Common-mode output voltage§ | $R_L = 54 \Omega \text{ or } 100 \Omega$ | See Figure 1 | | | 3 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage [‡] | | | | | ±0.2 | V |
| lo | Output current | Output disabled, See Note 4 | V ₀ = 12 V V ₀ = -7 V | | | 1 -0.8 | mA |
| ΊΗ | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| IIL | Low-level input current | V _I = 0.4 V | | | | -400 | μΑ |
| | 31 | $V_0 = -7 V$ | | | | -250 | |
| los | Short-circuit output current | $V_0 = V_{CC}$ | | | | 250 | mA |
| | | V _O = 12 V | | | | 500 | <u> </u> |
| Icc | Supply current (total package) | No load | Outputs enabled | | 35 | 50 | mA |
| | | L | Outputs disabled | | 26 | 40 | <u> </u> |

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_{A} = 25 ^{\circ}\text{C}$.

driver switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|-------------------------------------|----------------------|------------------------|-----|-----|-----|------|
| t _{DD} | Differential-output delay time | B 60.0 | L = 60 Ω, See Figure 3 | | 40 | 60 | ns |
| tTD | Differential-output transition time |] nL = 60 12, | | | 65 | 95 | ns |
| tPZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 55 | 90 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 30 | 50 | ns |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | 85 | 130 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | 20 | 40 | ns |

 $^{^{\}ddagger}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

[§]In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}. NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDIT | TEST CONDITIONS | | TYP [†] | MAX | UNIT |
|-----------------------------------|---|---|-------------------------|-------------------|------------------|------|------|
| V⊤H | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | 10 = 8 mA | -0.2 [‡] | | | V |
| V _{T+} - V _{T-} | Hysteresis [§] | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| Voн | High-level output voltage | $V_{ID} = -200 \text{ mV},$ See Figure 2 | $IOH = -400 \mu A$, | 2.7 | | | V |
| V _{OL} | Low-level output voltage | V _{ID} = -200 mV, See Figure 2 | I _{OL} = 8 mA, | | | 0.45 | V |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | V | | | ± 20 | μΑ |
| l _l | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA |
| " | Ene input current | See Note 4 | $V_I = -7 V$ | | | -0.8 | "" |
| ΊΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| ll. | Low-level enable-input current | V _{IL} = 0.4 V | | | | -100 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | | | - 15 | | -85 | mA |
| laa. | Supply current (total package) | No. lead | Outputs enabled | | 35 | 50 | |
| lcc | | No load | Outputs disabled | | 26 | 40 | mA |

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

receiver switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ | | | 21 | 35 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | $C_L = 15 pF$, | See Figure 6 | | 23 | 35 | ns |
| ^t PZH | Output enable time to high level | C _L = 15 pF, | See Figure 7 | | 10 | 30 | ns |
| tPZL | Output enable time to low level | | | | 12 | 30 | ns |
| tPHZ | Output disable time from high level | $C_1 = 15 pF$, | See Figure 7 | | 20 | 35 | ns |
| tPLZ | Output disable time from low level | С[– 15 рг, | See Figure 7 | | 17 | 35 | ns |

[‡]The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} , and the negative-going input threshold voltage, V_{T-} . See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

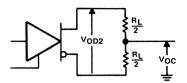


FIGURE 1. DRIVER VOD AND VOC

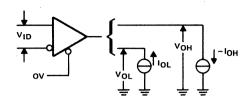


FIGURE 2. RECEIVER VOH AND VOI

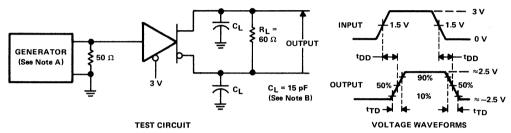


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

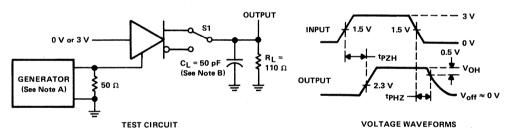


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

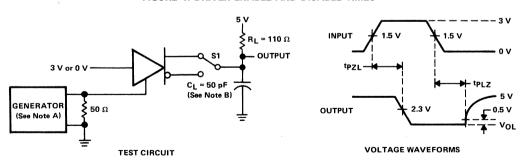


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_f \le 6$ ns, $t_f \le 6$ ns, $Z_{out} = 50 \Omega$.

B. C_I includes probe and jig capacitance.



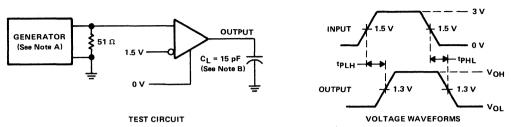


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

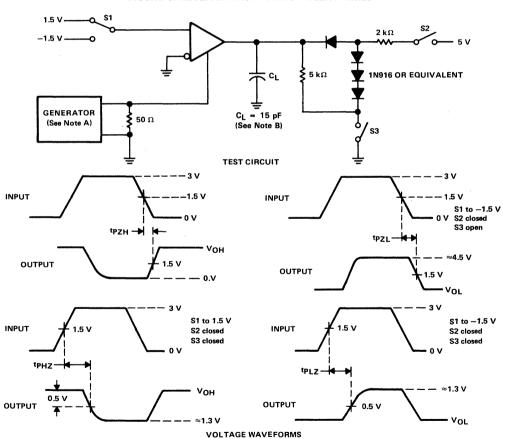


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_f \le 6$ ns, $t_f \le 6$ ns, $Z_{OUT} = 50 \Omega$.

B. CL includes probe and jig capacitance.



TYPICAL CHARACTERISTICS

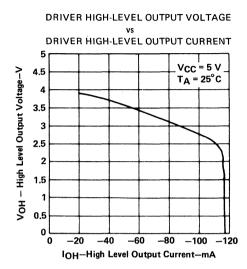


FIGURE 8

DRIVER DIFFERENTIAL OUTPUT VOLTAGE

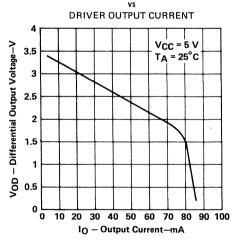


FIGURE 10

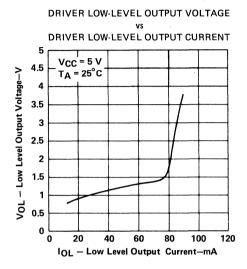


FIGURE 9

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

vs

RECEIVER LOW-LEVEL OUTPUT CURRENT

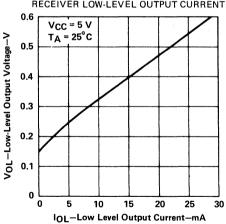
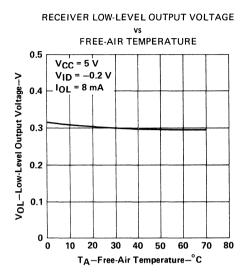


FIGURE 11

TYPICAL CHARACTERISTICS



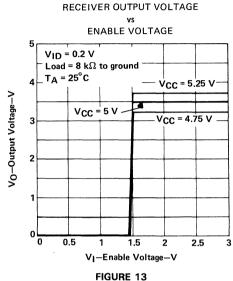
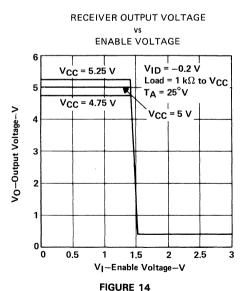


FIGURE 12



TYPICAL APPLICATION SN75176A SN75176A UP TO 32 TRANSCEIVERS

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

SN75177B, SN75178B DIFFERENTIAL BUS REPEATERS

D2606, JULY 1985-REVISED JANUARY 1990

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X 27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . 7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN75177B and SN75178B differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177B and SN75178B are identical except for the complementary enable inputs, which allow the devices to be used in pairs for bidirectional communication.

SN75177B . . . D, JG, OR P PACKAGE (TOP VIEW)



SN75178B . . . JG OR P PACKAGE (TOP VIEW)



SN75177B FUNCTION TABLE

| DIFFERENTIAL INPUTS | ENABLE | OUTPUTS | | rs |
|---|--------|---------|---|----|
| A-B | EN | T | Υ | Z |
| $V_{ID} \ge 0.2 V$ | Н | Н | Н | L |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | Н | ? | ? | ? |
| $V_{ID} \leq 0.2 V$ | Н | L | L | Н |
| X | L | z | Z | Z |

SN75178B FUNCTION TABLE

| DIFFERENTIAL INPUTS | ENABLE | OUTPUTS | | гs |
|---|--------|---------|---|----|
| AB | EN | Т | Υ | Z |
| V _{ID} ≥ 0.2 V | L | Н | Н | L |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | L | ? | ? | ? |
| $V_{ID} \leq 0.2 V$ | L | L | L | Н |
| X | н | Z | Z | Z |

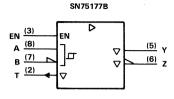
H = high level, L = low level, ? = indeterminate,

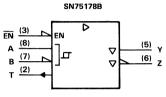
X = irrelevant, Z = impedance (off)

The SN75177B and SN75178B feature positive- and negative-current limiting 3-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of -7 V to 12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150 °C. The driver is designed to drive current loads up to 60 mA maximum.

The SN75177B and SN75178B are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176B bus transceiver.

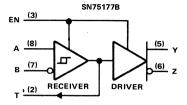
logic symbols†

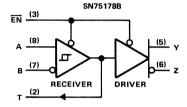




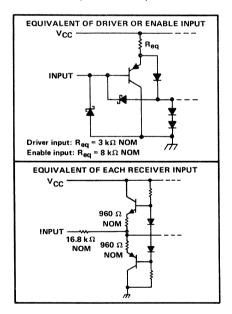
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

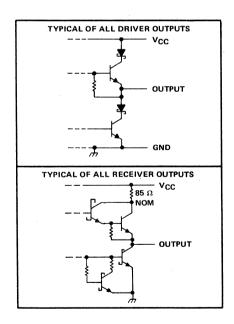
logic diagrams (positive logic)





scnematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Voltage range at any bus terminal |
| Differential input voltage (see Note 2) |
| Enable input voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| D package |
| JG package 825 mW |
| P package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

- 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. For operation above 25 °C free-air temperature, derate the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70 °C at the rate of 6.6 mW/°C and the P package to 640 mW at 70 °C at the rate of 8.0 mW/°C. In the JG package, SN75177B and SN75178B chips are glass mounted.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|----------|-----------------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | EN or EN | 2 | | | V |
| Low-level linput voltage, VIL | EN or EN | | | 0.8 | V |
| Common-mode input voltage, V _{IC} | | -7 [†] | | 12 | V |
| Differential input voltage, VID | | | | ±12 | V |
| I the board of the second of t | Driver | | | - 60 | mA |
| High-level output current, IOH | Receiver | | | -400 | μΑ |
| 1 | Driver | | | 60 | 4 |
| Low-level output current, IOL | Receiver | | | 8 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

[†]The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|--|------------------------|---------------------------------------|-------------------|------------------|---------|------|
| VIK | Input clamp voltage | I _I = -18 r | mA | | | -1.5 | ٧ |
| Vo | Output voltage | I ₀ = 0 | | 0 | | 6 | ٧ |
| VOD1 | Differential output voltage | I ₀ = 0 | | 1.5 | | 6 | V |
| | | B 100 | Ω, See Figure 1 | ½V _{OD1} | | | V |
| V _{OD2} | Differential output voltage | HL = 100 | u, See Figure 1 | 2 | | | V |
| | | $R_L = 54 \Omega$ | , See Figure 1 | 1.5 | 2.5 | 5 | ٧ |
| V _{OD3} | Differential output voltage | See Note 4 | • | 1.5 | | 5 | V |
| 41171 | Change in magnitude of | | | | | ±0.2 | V |
| Δ V _{OD} | differential output voltage [‡] | $R_L = 54 \Omega$ | or 100 Ω , | | | ±0.2 | V |
| Voc | Common-mode output voltage | See Figure | 1 | | | 3 -1 | ٧ |
| A I V = -1 | Change in magnitude of | | | | | ±0.2 | V |
| Δ Voc | common-mode output voltage [‡] | | | | | ±0.2 | V |
| Ю | Output current | $V_{CC} = 0$, | $V_0 = -7 \text{ V to } 12 \text{ V}$ | | | ±100 | μΑ |
| loz | High-impedance-stage output current | V _O = -7 | V to 12 V | | | ± 100 | μΑ |
| ΊΗ | High-level input current | V _I = 2.4 \ | 1 | | | 20 | μΑ |
| IL | Low-level input current | V _I = 0.4 \ | / | | | -400 | μΑ |
| | | V ₀ = -7 | V | | | - 250 | |
| los | Short-circuit output current | VO = VCC | ; | | | 250 | mA |
| | | V _O = 12 \ | / | | | 250 | |
| laa | Supply current (total package) | No load | Outputs enabled | | 57 | 70 | mA |
| ICC | Supply current (total package) | No load | Outputs disabled | | 26 | 35 | IIIA |

driver switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST CON | DITIONS | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|----------------------|--------------|-----|-----|-----|------|
| tDD | Differential-output delay time | D E4.0 | Con Figure 2 | | 15 | 22 | ns |
| tTD | Differential-output transition time | $R_L = 54 \Omega$, | See Figure 3 | | 20 | 30 | ns |
| tPZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 85 | 120 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 40 | 60 | ns |
| ^t PHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | 150 | 250 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | 20 | 30 | ns |

[†]All typical values are at $V_{CC}=5$ V and $T_A=25$ °C. $^{\ddagger}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

NOTE 4: See EIA Standard RS-485 from Figure 3.5, Test Termination Measurement 2.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--|--|
| v _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| VOD1 | V _o | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test termination Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | V _{os} | V _{os} |
| Δ Voc | V _{os} - V _{os} | $ V_{os} - \overline{V}_{os} $ |
| los | I _{sa} , I _{sb} | |
| lo | li _{xa} l, li _{xb} l | l _{ia} , l _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CON | DITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|-------------------------------|--------------------------|-------------------|------------------|-------|------|
| Vтн | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | I _O = 8 mA | -0.2 [‡] | | | V |
| V _{hys} | Hysteresis § | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | I _I = ~18 mA | | | | - 1.5 | V |
| | High lovel autous valtage | $V_{ID} = 200 \text{ mV},$ | $I_{OH} = -400 \mu A$ | 2.7 | | | V |
| Vон | High-level output voltage | See Figure 2 | | 2.7 | | | L v |
| \/-· | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ | $I_{OL} = 8 \text{ mA},$ | | | 0.45 | V |
| VOL | Low-level output voltage | See Figure 2 | |] | | 0.45 | |
| l | High impodence state cutout current | V- 04V-24V | | | 2 | 20 | ^ |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4$ | V | | | -400 | μΑ |
| I. | Line innut aurent | Other input at 0 V, | V _I = 12 V | | | 1 | mA |
| l) | Line input current | See Note 5 | V _I = -7 V | | | -0.8 | IIIA |
| ΊН | High-level enable-input current | V _{IH} = 2.7 V | | 1 | | 20 | μΑ |
| l _{IL} | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 200 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | | | -15 | | -85 | mA |
| 1 | Comply coment (total peakers) | Ne lead | Outputs enabled | | 57 | 70 | A |
| CC | Supply current (total package) | No load | Outputs disabled | | 26 | 35 | mA |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

receiver switching characteristics, VCC = 5 V, TA = 25°C

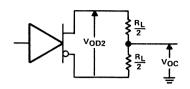
| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------|--|---------------------------|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V}$ | to 1.5 V, | | 19 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $C_L = 15 pF$, | See Figure 6 | | 30 | 40 | ns |
| tPZH | Output enable time to high level | $C_{i} = 15 pF$ | See Figure 7 | | 10 | 20 | ns |
| tPZL | Output enable time to low level | C[= 15 pr, | See Figure 7 | | 12 | 20 | ns |
| tPHZ | Output disable time from high level | $C_1 = 15 pF$, | See Figure 8 | | 25 | 35 | ns |
| tPLZ | Output disable time from low level | CL = 15 pr, | See rigure 6 | | 17 | 25 | ns |



[‡]The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 12.

NOTE 5: Refer to EIA Standard RS-422 for exact conditions.



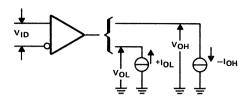


FIGURE 1. DRIVER VOD AND VOC

FIGURE 2. RECEIVER VOH AND VOL

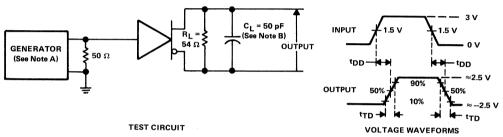


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

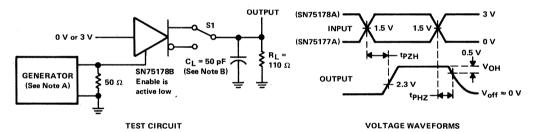


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES (tpzh, tphz)

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.

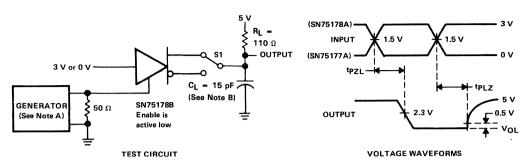


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES (tpzl, tplz)

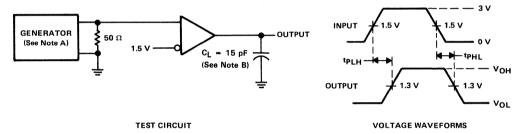
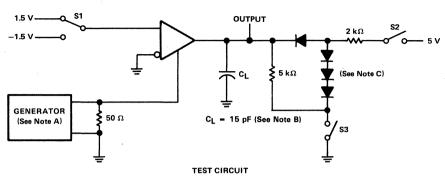
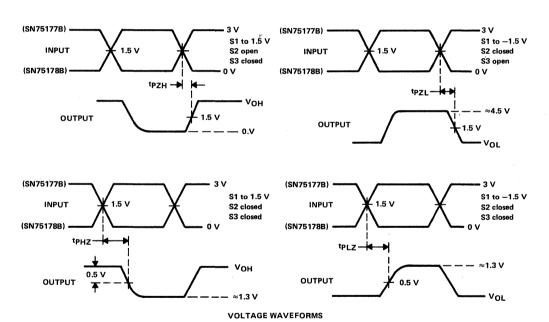


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{OUT} =$ 50 Ω .

B. C₁ includes probe and jig capacitance.





NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \approx 50%, $t_f = t_f = 6$ ns, $Z_0 = 50 \Omega$.

- B. CL includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.

FIGURE 7. RECEIVER ENABLE AND DISABLE TIMES



TYPICAL CHARACTERISTICS



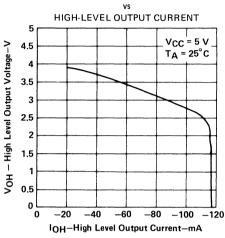


FIGURE 8

DRIVER DIFFERENTIAL OUTPUT VOLTAGE

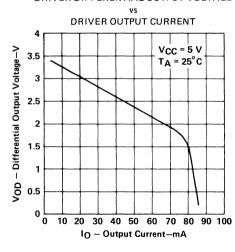


FIGURE 10

DRIVER LOW-LEVEL OUTPUT VOLTAGE

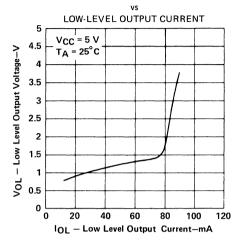


FIGURE 9

RECEIVER OUTPUT VOLTAGE

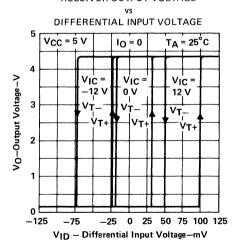


FIGURE 11

TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

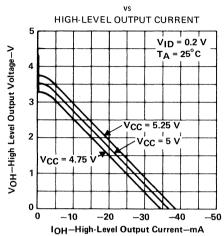


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

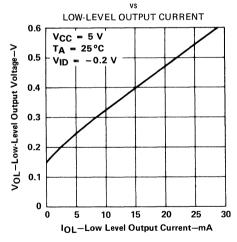


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

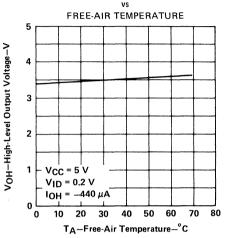


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

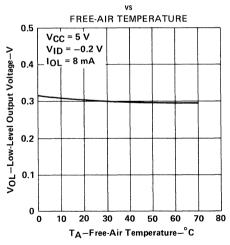
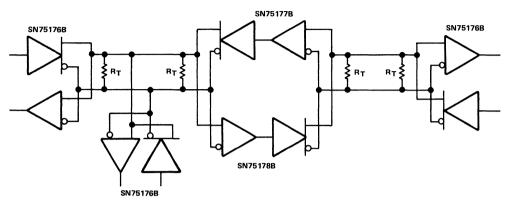


FIGURE 15

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 16. TYPICAL APPLICATION CIRCUIT

D2845, OCTOBER 1985-REVISED AUGUST 1989

- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- Bus Voltage Range . . . −7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN75179B driver and bus receiver circuit is a monolithic integrated device designed for balanced transmission line applications and meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver outputs provide limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of $\pm\,200$ mV over a common-mode input voltage range of -12 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately $150\,^{\circ}\text{C}$. The device is designed to drive current loads of up to 60 mA maximum.

The SN75179B is characterized for operation from 0° C to 70° C.

D, JG, OR P PACKAGE (TOP VIEW)

| Vcc □1 | U 8 | | ١ |
|--------|------------|------|---|
| R □ 2 | 7 |] E | 3 |
| D 🛮 3 | 6 | [] z | • |
| GND 4 | 5 | ו 🛚 | ′ |

FUNCTION TABLE (DRIVER)

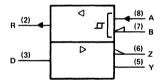
| INPUT | OUTPUTS |
|-------|---------|
| D | ΥZ |
| . Н | H L |
| L | LH |

FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS | OUTPUT |
|----------------------------------|--------|
| A — B | R |
| V _{ID} ≥ 0.2 V | н |
| -0.2 V < V _{ID} < 0.2 V | 7 |
| $V_{ID} \leq -0.2 V$ | L |

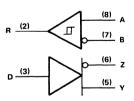
H = high level, L = low level, ? = indeterminate

logic symbol†



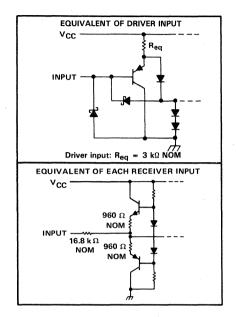
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

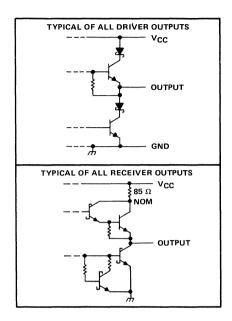
logic diagram





schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) 7 V Voltage at any bus terminal -10 V to 15 V Differential input voltage (see Note 2) ±25 V |
|--|
| Continuous total dissipation at (or below 25 °C free-air temperature (see Note 3): |
| D package |
| JG package 825 mW |
| P package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C |

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 - 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 - 3. For operation above 25 °C free-air temperature, derate the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70 °C at the rate of 6.6 mW/°C and the P package to 640 mW at 70 °C at the rate of 8.0 mW/°C.. In the JG package SN75179B, chips are glass mounted.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|----------|-----------------|-----|------|------|
| Supply voltage, VCC | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | Driver | 2 | | | V |
| Low-level input voltage, V _{IL} | Driver | | | 0.8 | V |
| Common-mode input voltage, V _{IC} | | -7 [†] | | 12 | V |
| Differential input voltage, V _{ID} | | | | ±12 | V |
| High-level output current, IOH | Driver | | | -60 | mA |
| riigii-level output current, IOH | Receiver | | | -400 | μΑ |
| Low-level output current, IOI | Driver | | | 60 | ^ |
| cow-level output current, IOL | Receiver | | | 8 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

[†] The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for commonmode input voltage and threshold voltage.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CON | DITIONS | MIN | TYP [‡] | MAX | UNIT |
|-------------------|--|--|---|-------------------|------------------|--------------|------|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| V _O | Output voltage | I _O = 0 | | 0 | | 6 | V |
| V _{OD1} | Differential output voltage | IO = 0 | | 1.5 | | 6 | V |
| Vod2 | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | ½V _{OD1} | | | · V |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V |
| VOD3 | Differential output voltage | See Note 4 | | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage § | | | | | ±0.2 | ٧ |
| Voc | Common-mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | + 3 1 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage § | | | | | ±0.2 | ٧ |
| Ю | Output current | $V_{CC} = 0$, | $V_0 = -7 \text{ V to } 12 \text{ V}$ | | | ± 100 | μΑ |
| ΙΗ | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| IIL | Low-level input current | V _I = 0.4 V | *************************************** | | | - 200 | μΑ |
| los | Short-circuit output current | $V_O = -7 \text{ V}$ $V_O = V_{CC} \text{ or } 12 \text{ V}$ | | | | - 250 250 | mA |
| lcc | Supply current (total package) | No load | | | 57 | 70 | mA |

driver switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | | TEST CONDITIONS | | | TYP | MAX | UNIT |
|-----------------|-------------------------------------|---------------------|--------------|--|-----|-----|------|
| t _{DD} | Differential-output delay time | $R_1 = 54 \Omega$. | Soo Figure 2 | | 15 | 22 | ns |
| tTD | Differential-output transition time | $H_L = 54 \Omega$, | See Figure 3 | | 20 | 30 | ns |



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C. § Δ |V_{QD}| and Δ |V_{QC}| are the changes in magnitude of V_{QD} and V_{QC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 4: See EIA Standard RS-485, Figure 3.5, Test Termination Measurement 2.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|-------------------------------------|--|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| VOD1 | Vo | V _o |
| VOD2 | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test termination Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| V _{OC} | V _{os} | V _{os} |
| Δ VOC | $ V_{os} - \overline{V}_{os} $ | $ V_{os} - \overline{V}_{os} $ |
| los | Isal, Isb | |
| ю | I _{xa} , I _{xb} | l _{ia} , l _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

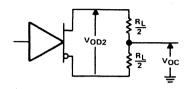
| PARAMETER | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT |
|------------------|---|---|-------------------------------|-------|------------------|----------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$, | I _O = 8 mA | -0.2‡ | | | V |
| V _{hys} | Hysteresis [§] | | | | 50 | | mV |
| Vон | High-level output voltage | V _{ID} = 200 mV, See Figure 2 | $I_{OH} = -400 \mu\text{A},$ | 2.7 | | | ٧ |
| V _{OL} | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ See Figure 2 | I _{OL} = 8 mA, | | | 0.45 | V |
| t _l | Line input current | Other input at 0 V, See Note 5 | $V_{i} = 12 V$ $V_{i} = -7 V$ | | | 1 0.8 | mA |
| rį | Input resistance | | | 12 | | | kΩ |
| ios | Short-circuit output current | | | -15 | | -85 | mA |
| Icc | Supply current (total package) | No load | | | 57 | 70 | mA |

receiver switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ | | 19 | 35 | ns |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, See Figure 4 | | 30 | 40 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for commonmode input voltage and threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTE 5: Refer to EIA Standard RS-422-A for exact conditions.



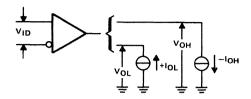


FIGURE 1. DRIVER VOD AND VOC

FIGURE 2. RECEIVER VOH AND VOL

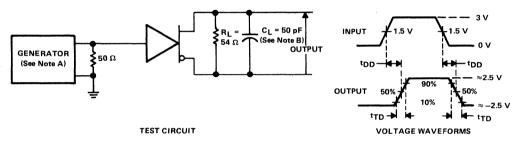


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

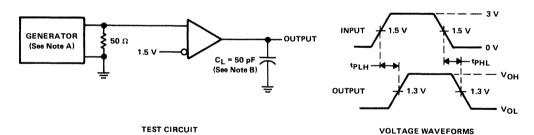


FIGURE 4. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \ \Omega$.

B. CL includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

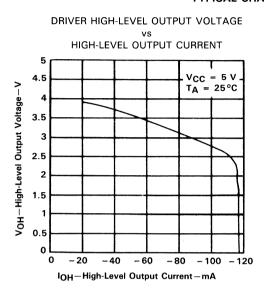
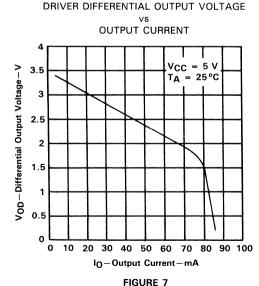
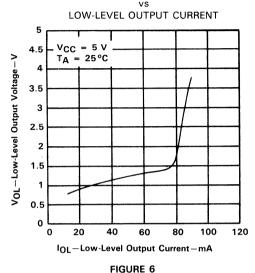


FIGURE 5



DRIVER LOW-LEVEL OUTPUT VOLTAGE



RECEIVER OUTPUT VOLTAGE DIFFERENTIAL INPUT VOLTAGE

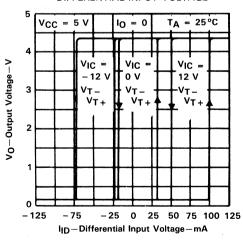


FIGURE 8



TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE HIGH-LEVEL OUTPUT CURRENT 5 $V_{ID} = 0.2 V$ $T_A = 25$ °C 3 = 5.25 V= 5 V

FIGURE 9

VOH-High-Level Output Voltage-V 0 - 10 - 20 - 30 -40 - 50 IOH-High-Level Output Current-mA

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

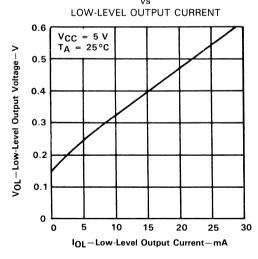


FIGURE 11

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

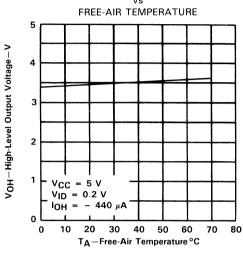


FIGURE 10

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

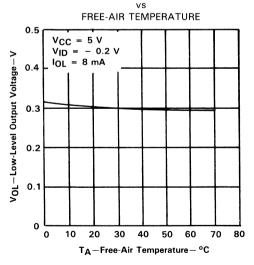


FIGURE 12

D3389, FEBRUARY 1990

- Meets Standards RS-232-C, EIA-232-D, and CCITT V.28
- Four Independent Drivers and Receivers
- Loopback Mode Functionally Self-Tests
 Drivers and Receivers Without
 Disconnection From Line
- Driver Slew Rate Limited to 30 V/µs Max
- Built-in Receiver 1-us Noise Filter
- Internal Thermal Overload Protection
- EIA-232-D Inputs and Outputs Withstand ± 30V
- Low Supply Current . . . 2.5 mA Typ
- ESD Protection Exceeds 2000 V Per MIL-STD-833C Method 3015

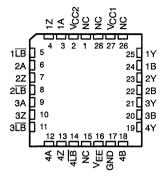
description

The SN75186 is a low-power bipolar device containing four driver/receiver pairs designed to interface data terminal equipment (DCE). Additionally, the SN75186 has a loopback mode that may be used by a data communication system to perform a functional self test on each driver/receiver pair, removing the need to locally disconnect cables and install a loopback connector. Flexibility of control is ensured by each driver/receiver pair having its own loopback control input. The SN75186 is designed to conform to standards RS-232-C, its revision ANSI/EIA-232-D-1986, and CCITT V.28.

The maximum slew rate is limited to 30 V/ μ s at the driver outputs and drives a capacitive load of 2500 pF at 20 kBaud. The receivers have input filters that disregard input noise pulses shorter than 1 μ s. The SN75186 is a robust device capable of withstanding \pm 30 V at driver outputs and at receiver inputs whether powered or unpowered. This device has an internal ESD protection rated at 2 kV to prevent functional failures.

The SN75186 is characterized for operation from 0°C to 70°C.

FN PACKAGE (TOP VIEW)



NC - No internal connection

FUNCTION TABLE (EACH RECEIVER)

| LOOPBACK | INP | UTS | OUTPUT |
|----------|------------------|-----|--------|
| LB | A B [†] | | Z |
| Н | Х | Н | L |
| н | Х | L | н |
| L | L | Х | L |
| L | Н | Х | Н |

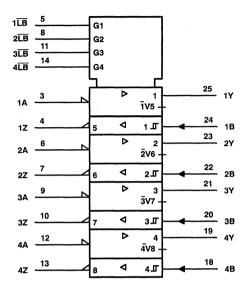
FUNCTION TABLE (EACH DRIVER)

| LOOPBACK LB | INPUT A | OUTPUT Y [†] | | | |
|----------------|------------|--------------------------|--|--|--|
| Н | Н | L | | | |
| н | L | н | | | |
| L | Х | L | | | |

[†] Voltages are RS-232-C, EIA-232-D, and V.28 levels

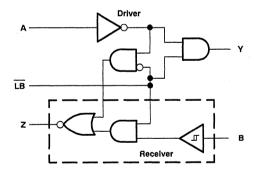
H = high level, L = low level, X = irrelevant

logic symbol†

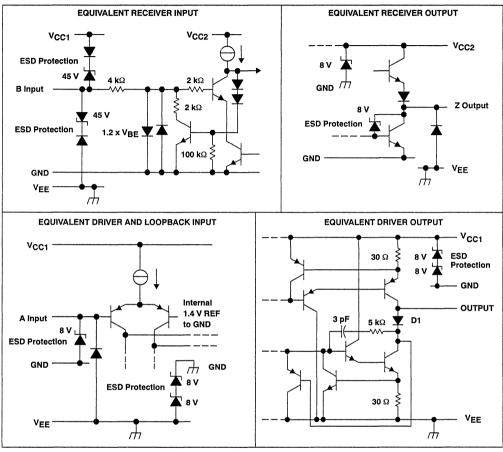


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram, each driver/receiver pair (positive logic)



schematics of inputs and outputs



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC1} (see Note 1) | 15 V |
|--|---|
| Supply voltage, V _{CC2} | |
| Supply voltage, VEE | – 15 V |
| Receiver input voltage range | – 30 V to 30 V |
| Driver input voltage range | (V _{EE} + 2 V) to V _{CC1} V |
| Loopback input voltage range | 0 V to 7 V |
| Driver output voltage range | |
| Continuous total power dissipation at (or below) 25°C free-air | |
| temperature (see Note 2) | 1400 mW |
| Operating free-air temperature range, T _A | 0°C to 70°C |
| Storage temperature range | – 65°C to 150°C |
| Case temperature for 10 seconds | 260°C |

NOTES: 1. All voltages are with respect to the network ground terminal.

2. For operation above 25°C free-air temperature, derate linearly to 896 mW at 70°C at the rate of 11.2 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---------------------|-------|-----|------------------|------|
| Supply voltage, V _{CC1} | | 10.8 | 12 | 13.2 | ٧ |
| Supply voltage, V _{CC2} | | 4.5 | 5 | 5.5 | ٧ |
| Supply voltage, VEE | | -10.8 | -12 | -13.2 | ٧ |
| Input voltage, V _I | Driver and loopback | 0 | | V _{CC2} | ٧ |
| Input voltage, V _I (see Note 3) | Receiver | | | ± 30 | ٧ |
| High-level input voltage, VIH | Driver and loopback | 2 | | | V |
| Low-level input voltage, VIL | Driver and loopback | | | 0.8 | V |
| Output voltage, VO, powered on or off | Driver | | | ± 30 | V |
| High-level output current, IOH | Receiver | | | -4 | mA |
| Low-level output current, IOL | Receiver | | | 4 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

NOTE 3: If all receiver inputs are held at ± 30V, the thermal dissipation limit of the package may be exceeded. The thermal shutdown may not protect the device, as this dissipation occurs in the receiver input resistors.

DRIVER SECTION

driver electrical characteristics over full recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | NS | MIN | TYP† | MAX | UNIT |
|-----------------|--|-------------------------|--------------------------|-------------------------|------|------|------|------|
| Vон | High-level output voltage | $R_L = 3 k\Omega$, | V _{IL} = 0.8 V, | See Figure 1 | 7 | | | V |
| VOL | Low-level output voltage [‡] | $R_L = 3 k\Omega$, | V _{IH} = 2 V, | See Figure 1 | | | -7 | ٧ |
| VOH(LB) | High-level output voltage in loopback modeद | $R_L = 3 k\Omega$, | LB at 0.8 V, | V _{IL} = 0.8 V | | | -7 | ٧ |
| ΊΗ | High-level input current (driver and loopback inputs)# | V _I = 5 V, | See Figure 2 | | | | 100 | μА |
| I _{IL} | Low-level input current (driver and loopback inputs)# | V _I = 0, | See Figure 2 | | | , | 100 | μΑ |
| los(H) | High-level short-circuit output current | V _I = 0.8 V, | V _O = 0, | | - 10 | - 20 | - 35 | mA |
| | | See Note 4 a | | | | | | |
| los(L) | Low-level short-circuit output current | V _i = 2 V, | $V_O = 0$, | | 10 | 20 | 35 | mA |
| 108(L) | 2011 lever short enealt eatput earront | See Note 4 and Figure 1 | | | | | 7777 | |
| ICC1 | Supply current from V _{CC1} | No load | | | | 2.5 | 4 | mA |
| ICC1(LB) | Supply current from V _{CC1} with loopback on | No load, | LB at 0.8 V | | | | 10 | mA |
| IEE | Supply current from VEE | No load | | | | -2.5 | -4 | mA |
| IEE(LB) | Supply current from VEE with loopback on | No load, | LB at 0.8 V | | | | -10 | mA |
| ICC2 | Supply current from V _{CC2} | No load, | V _I = 0, | See Note 6 | | -10 | -100 | μΑ |
| | | No load, | LB at 0.8 V, | V _I = 0, | | | | |
| ICC2(LB) | Supply current from V _{CC2} with loopback on | See Note 6 | | | | - 10 | 100 | μА |
| ro | Output resistance | VCC1 = VEE | | 0.3 | | 5 | | kΩ |
| 1.0 | | $V_0 = -2 V to$ | 2 V, | See Note 5 | 0.0 | | | |

[†] All typical values are at $T_A = 25$ °C.

- 5. Test conditions are those specified by EIA-232-D.
- Without a load and V_I = 0, the worst case conditions, V_{CC2} pin sources a small current originating from V_{CC1} giving I_{CC2} supply current a negative sign. When a receiver has an output load, V_{CC2} sinks static and dynamic supply currents to meet load requirements.

[‡] The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

[§] This is the most positive level that the driver output will rise to when the device is in the loopback mode and the driver input is at a low level.

The loopback mode should be entered only when the driver output is in the low (marking) state.

[#] Unused driver inputs should be tied to 0 V or VCC2; unused loopback inputs should be tied to VCC2.

NOTES: 4. Minimum I_{OS(H)} and I_{OS(L)} are specified at V_O = 0 as this more accurately describes the output current needed to dynamically drive capacitive lines. A minimum of ±10 mA is sufficient to drive 2500 pF in parallel with 3 kΩ at a slew rate of 4 V/μs (in accordance with EIA-232-D and V.28).

driver switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDI | TIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|--|-------------------------|-----|-----|-----|------|
| t _{PLH} | Propagation delay time, low-to-high level output | $R_L = 3 k\Omega$ to $7 k\Omega$, | C _L = 15 pF, | | 0.6 | 5 | μs |
| tPHL. | Propagation delay time, high-to-low-level output | See Figure 3 | | | 0.8 | 5 | μS |
| ^t skew | tpLH -tpHL | $R_L = 3 k\Omega$ to 7 kΩ, $C_L = 15 pF$ to 2500 pF | | 0.2 | 1 | μs | |
| SR | Output slew rate | R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF | | 4 | | 30 | V/µs |
| ^t pd(ILB) | Propagation delay time going into loopback mode‡ | R_L = 3 kΩ to 7 kΩ, See Figure 7 | See Note 7, | | 3 | 50 | μs |
| ^t pd(OLB) | Propagation delay time going out of loopback mode§ | $R_L = 3 k\Omega$ to 7 kΩ, See Figure 7 | See Note 7, | | 3 | 50 | μs |
| ^t pd(LB) | Propagation delay time in loopback mode [¶] | $R_L = 3 k\Omega$ to 7 kΩ, See Figure 8 | See Note 7, | | 3 | 15 | μS |
| t _{skew} | Skew time in loopback mode | $R_L = 3 k\Omega$ to $7 k\Omega$, | See Note 7 | | 4 | 10 | μs |

[†] All typical values are at TA = 25°C.

[†] This is the delay between entering the loopback mode and when the data on the receiver output becomes valid.

[§] This is the worst-case (rising or falling edges) total propagation delay between driver input and receiver output when in the loopback mode.

This is the magnitude of the difference between the propagation delay time of the rising and falling edges of tpd(LB).

NOTE 7: Skew time is the magnitude of the difference between the propagation delay time of the rising and falling edges of tpd(LB).

RECEIVER SECTION

receiver electrical characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDI | TEST CONDITIONS | | TYP [†] | MAX | UNIT |
|------------------|--|---|--------------------------|-----|------------------|-----|------|
| V _{T+} | Positive-going threshold voltage | See Figure 5 | | 1.3 | 2 | 2.5 | V |
| V _T _ | Negative-going threshold voltage | See Figure 5 | | 0.5 | 1 | 1.7 | V |
| V _{hys} | Input hysteresis (VT+ - VT-) | | | 0.5 | 1 | 1.5 | V |
| 1/ | High Issuel and and and and and | $V_1 = -3 \text{ V or inputs open,}$ | ΙΟΗ = -20 μΑ | 3.5 | | | ., |
| VOH | High-level output voltage | See Note 8 and Figure 5, | I _{OH} = – 4 mA | 2.4 | | | ٧ |
| VOL | Low-level output voltage | I _{OL} = 4 mA, See Figure 5 | V _J = 3 V, | | | 0.4 | ٧ |
| los(H) | Short-circuit output current at high-level | V _{OH} = 0, | See Figure 4 | | 20 | -60 | mA |
| los(L) | Short-circuit output current at low-level | VOL = VCC2, | See Figure 4 | Ī | 20 | 60 | mA |
| rin | Input resistance | V _I ≤ 25 V | V _I ≤ 25 V | | | | 1.0 |
| .111 | input resistance | V _I = 3 V to 25 V | | | | 7 | kΩ |

NOTE 8: If the inputs are left unconnected, the receiver interprets this as a low input and the receiver outputs will remain in the high state.

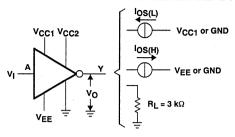
receiver switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------------|--|--------------------------------------|-----|------|-----|------|
| tPLH | Propagation delay time, low-to-high level output | 0 5: 0 | | 2 | 6 | μs |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 6 | | 2 | 6 | μs |
| tTLH | Transition time, low-to-high level output [‡] | C _L = 50 pF, See Figure 6 | | 200 | 300 | ns |
| tTHL | Transition time, high-to-low level output [‡] | | | 50 | 300 | ns |
| tskew | tplH - tpHL | | | 0.1 | 1 | μS |
| t _{wN} | Maximum pulse duration assumed to be noise§ | Pulse amplitude = 5 V | 1 | 2 | 4 | μS |

[†] All typical values are at T_A = 25°C.

[‡] Transition times are measured between 10% and 90% points on output waveform.

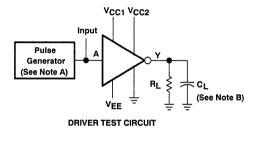
[§] The receiver will ignore any positive- or negative-going pulse whose duration is less than the minimum value of t_W and accept any positive- or negative-going pulse whose duration is greater than the maximum value of t_W.



V_I V_{EE} V_{CC2}

Figure 1. Driver Test Circuit, V_{OH}, V_{OL}, I_{OS(L)}, I_{OS(H)}

Figure 2. Driver and Loopback Test Circuit, I_{IL}, I_{IH}



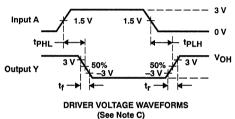
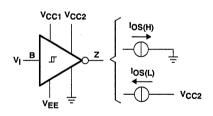


Figure 3. Driver Propagation Time and Slew Rate



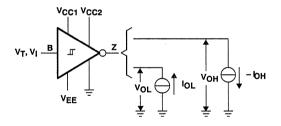


Figure 4. Receiver Test Circuit, I_{OS(H)}, I_{OS(L)}

Figure 5. Receiver Test Circuit, V_T , V_{OL} , V_{OH}

NOTES: A. The pulse generator has the following characteristics: t_W = 25 μ s, PRR = 20 kHz, Z_0 = 50 Ω .

B. C_L includes probe and jig capacitance.

C. Slew rate = $\frac{6 \text{ V}}{t_r \text{ or } t_f}$.

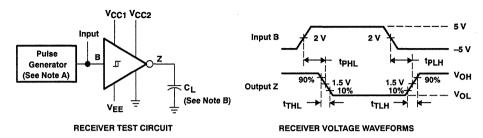


Figure 6. Receiver Propagation and Transition Times

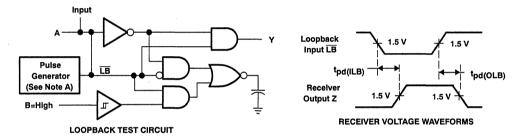


Figure 7. Loopback Entry and Exit Propagation Times

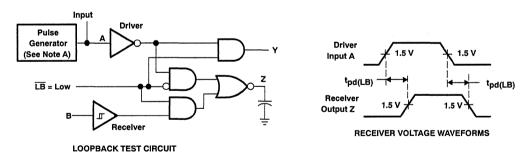


Figure 8. Loop Propagation Times in Loopback Mode

NOTES: A. The pulse generator has the following characteristics: t_W = 25 μs , PRR = 20 kHz, Z_0 = 50 Ω . B. C_L includes probe and jig capacitance.

PRINCIPLES OF OPERATION

In normal operation, the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs \overline{LB} high. Taking a particular \overline{LB} input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, -5 V, of the EIA-232-D marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75186 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = -12 V, line short circuits to voltages greater than -5 V and less than -12 V will be detected. The loopback mode should be entered only when the driver output is low, that is, the marking condition of EIA-232-D. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

When in the loopback mode, approximately 95% of the SN75186 circuit is functionally checked. There exists some low probability of fault mechanisms in circuitry not checked in the loopback mode. To reduce the chances of undetected failure, the unchecked circuitry has been designed to be more robust than that within the loopback test loop. The areas where special attention has been paid are the receiver input potential divider and resistors, the driver output blocking diode (D1), and parts of the driver clamp circuit.

Protection of the SN75186 is achieved by means of driver output current limits and a thermal trip. Although this device will withstand ± 30 V at its receiver input, package thermal dissipation limitations have to be taken into consideration if more than one receiver is connected simultaneously. This is due to the possible dissipation in the $3-k\Omega$ minimum input resistors, which is not under the control of the thermal trip. Although the supply current is higher in the loopback mode than in normal operation, the total power dissipation is not sufficient under normal worst-case conditions (of receiver input $V_1 = 15$ V + 10%, receiver output voltage = 2.4 V at 4 mA, driver load of 3 k Ω) to cause the thermal limiting circuitry to trip.

If the SN75186 goes into thermal trip, the output of the driver goes to a high-impedance state and the receiver output is held in a logic-high marking state. Both driver and receiver outputs maintain a marking state for the following circuit and do not allow indeterminate conditions to exist.

The standards specify a minimum driver output resistance to ground of 300 Ω when the device is powered off. To fully comply with EIA-232-D power-off fault conditions, many drivers need diodes in series with each supply voltage to prevent reverse current flow and driver damage. The SN75186 overcomes this need by providing a high-impedance driver output of typically 5 k Ω under power-off conditions through the use of the equivalent of these series diodes in the driver output circuit.



SN75207, SN75207B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

D1314, JULY 1973-REVISED SEPTEMBER 1989

- Plug-in Replacement for SN75107A and SN75107B with Improved Characteristics
- ± 10 mV Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- "B" Version Has Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

description

The SN75207 and SN75207B are pin-for-pin replacements for the SN75107A and SN75107B respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output.

| D OR N PACKAGE (TOP VIEW) | | | | | | |
|------------------------------|---|------|---|-----|--|--|
| 1 A 🗌 | 1 | U 14 | þ | Vcc | | |
| 1B 🗌 | 2 | 13 | | VCC | | |
| NC [| 3 | 12 | | 2A | | |
| 1 Y 🗌 | 4 | 11 | | 2B | | |
| 1G [| 5 | 10 | П | NC | | |

NC-No internal connection

FUNCTION TABLE

| DIFFERENTIAL INPUTS | STR | OBES | ОИТРИТ |
|---|-----|------|---------------|
| A-B | G | S | , |
| V _{ID} ≥ 10 mV | X | X | Н |
| | Х | L | Н |
| $-10 \text{ mV} < \text{V}_{\text{ID}} < 10 \text{ mV}$ | L | X | н |
| | Н | Н | Indeterminate |
| | Х | L | н |
| $V_{ID} \leq -10 \text{ mV}$ | L | X | Н |
| | Н | Н | L |

H = high level, L = low level, X = irrelevant

The essential difference between the unsuffixed and "B" version can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" version. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



UNSUFFIXED VERSION



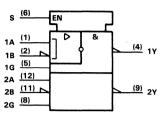
This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

These devices are characterized for operation from 0 °C to 70 °C and are available in plastic small outline (D) package or plastic dual-in-line (N) package.

Texas Instruments

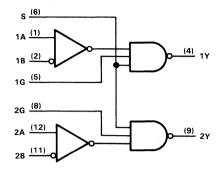
SN75207, SN75207B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

logic symbol†

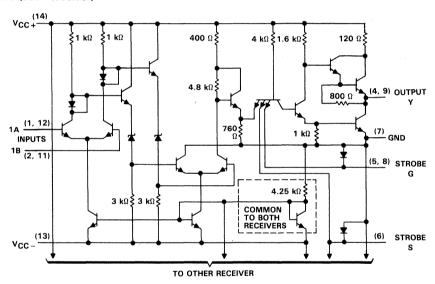


 $^\dagger \text{This}$ symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



NOTE: Resistor values shown are nominal.

design characteristics

The '207 and '207B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ± 3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to assure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) |
|---|
| Supply voltage, V _{CC} |
| Differential input voltage (see Note 2) ±6 V |
| Common-mode input voltage (see Note 3) |
| Strobe input voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature: (see Note 4) |
| D package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

- NOTES: 1. All voltage values, except differential voltages, are with respect to ground terminal.
 - 2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
 - 3. Common-mode input voltage is the average of the voltages at the A and B inputs.
 - 4. For operation above 25 °C free-air temperature, derate linearly to 608 mW at 70 °C at the rate of 7.6 mW/ °C for the D package and 736 mW at 70 °C at the rate of 9.2 mW/ °C for the N package.

SN75207, SN75207B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

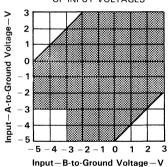
recommended operating conditions (see Note 5)

| | MIN | NOM MAX | UNIT |
|--|-----------------|----------|------|
| Supply voltage, V _{CC+} | 4.75 | 5 5.25 | V |
| Supply voltage, V _{CC} – | -4.75 | -5 -5.25 | ٧ |
| High-level differential input voltage | 0.01 | . 5 | V |
| V _{IDH} (see Note 6) | 0.01 | . 5 | \ \ |
| Low-level differential input voltage, V _{IDL} | -5 [†] | -0.01 | V |
| Common-mode input voltage, V _{IC} (see Notes 6 and 7) | -31 | 3 | V |
| Input voltage, any differential input to ground (see Note 6) | -5 [†] | 3 | V |
| High-level input voltage at strobe inputs, V _{IH(S)} | 2 | 5.5 | V |
| Low-level input voltage at strobe inputs, V _{IL(S)} | 0 | 0.8 | V |
| Low-level output current, IOL | | -16 | mA |
| Operating free-air temperature, T _A | 0 | 70 | °C |

[†] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

- NOTES: 5. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3 V and 3 V.
 - 6. The recommended combinations of input voltages fall within the shaded area of the figure shown.
 - 7. The common-mode voltage may be as low as -4 V provided that the more positive of the two inputs is not more negative than -3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



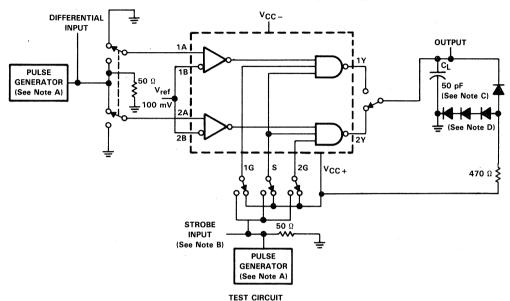
electrical characteristics over recommended free-air temperature range (unless otherwise noted)

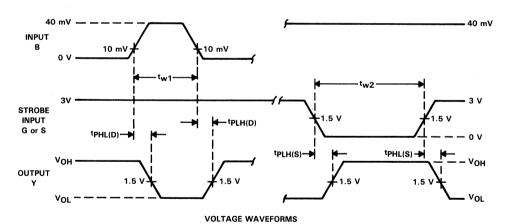
| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-----------------|---|--|-----------------------------|------|------------------|------|------|
| 1 | High-level '207 | V +5.35.V | V _{ID} = 5 V | | 30 | 75 | ^ |
| 'нн | input current '207B | $V_{CC\pm} = \pm 5.25 \text{ V}$ | $V_{ID} = -5 V$ | | 30 | 75 | μΑ |
| 1 | Low-level '207 | V + E 2E V | $V_{ID} = -5 V$ | | | - 10 | |
| IIL. | input current '207B | V _{CC±} = ±5.25 V | V _{ID} = 5 V | | | - 10 | μΑ |
| 1 | High-level input current | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IH(S)} = 2.4 \text{ V}$ | | | | 40 | μΑ |
| ΊΗ | into 1G or 2G | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IH(S)} = \pm 5.25 \text{ V}$ | | | | 1 | mA |
| l _{IL} | Low-level input current into 1G or 2G | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IL(S)} = 0.4 \text{ V}$ | | | | -1.6 | mA |
| | High-level input | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IH(S)} = 2.4 \text{ V}$ | | | | 80 | μΑ |
| ЧН | current into S | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IH(S)} = \pm 5.25 \text{ V}$ | | | | 2 | mA |
| IIL | Low-level input current into S | $V_{CC\pm} = \pm 5.25 \text{ V}, V_{IL(S)} = 0.4 \text{ V}$ | | | | -3.2 | mA |
| Voн | High-level output voltage | $V_{CC\pm} = \pm 4.75 \text{ V}, V_{IL(S)} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}, V_{IC} = -3 \text{ V to 3 V}$ | $V_{IDH} = 10 \text{ mV},$ | 2.4 | | | V |
| VOL | Low-level output voltage | $V_{CC\pm} = \pm 4.75 \text{ V}, V_{IH(S)} = 2 \text{ V}, \\ I_{OL} = 16 \text{ mA}, V_{IC} = -3 \text{ V to 3 V}$ | $V_{IDL} = -10 \text{ mV},$ | | | 0.4 | V |
| ЮН | High-level output current | $V_{CC\pm} = \pm 4.75 \text{ V}, V_{OH} = \pm 5.25 \text{ V}$ | | | | | μΑ |
| los | Short-circuit output current [‡] | V _{CC±} = ±5.25 V | | - 18 | | - 70 | mA |
| Іссн+ | Supply current from V _{CC+} , outputs high | $V_{CC\pm} = \pm 5.25 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | | | 18 | 30 | mA |
| Іссн – | Supply current from V _{CC} -, outputs high | $V_{CC\pm} = \pm 5.25 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | | | -8.4 | - 15 | mA |

 $^{^{\}dagger}AII$ typical values are at V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25 °C. $^{\ddagger}Not$ more than one output should be shorted at a time.

switching characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|---|------------------------|-----|-----|------|
| | Propagation delay time, low-to-high-level | | | 35 | ns |
| ^t PLH(D) | output, from differential inputs A and B | | ł | 35 | 115 |
| | Propagation delay time, high-to-low-level | $R_L = 470 \Omega$ | | 20 | |
| tPHL(D) | output, from differential inputs A and B | | | | ns |
| ^t PLH(S) output, from strobe input G or S | Propagation delay time, low-to-high-level | $C_L = 50 \text{ pF},$ | | 17 | |
| | output, from strobe input G or S | See Figure 1 | | 17 | ns |
| | Propagation delay time, high-to-low-level | | | 47 | |
| | output, from strobe input G or S | | | 17 | ns |





- NOTES: A. The pulse generators have the following characteristics: $Z_{out} = 50 \, \Omega$, $t_f \le 5 \, \text{ns}$, $t_{W1} = 500 \, \text{ns}$ with PRR = 1 MHz, $t_{W2} = 1 \mu s$ with PRR = 500 kHz.
 - B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
 - C. C_L includes probe and jig capacitance.
 - D. All diodes are 1N916.

FIGURE 1. PROPAGATION DELAY TIMES



TYPICAL APPLICATION DATA

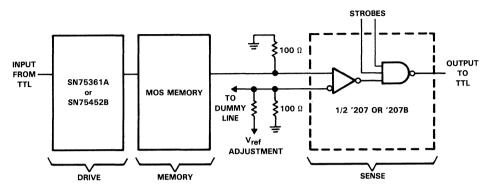
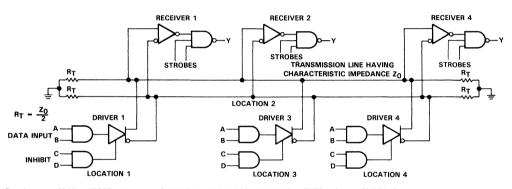


FIGURE 2. MOS MEMORY SENSE AMPLIFIER



Receivers are '207 or '207B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3. DATA-BUS OR PARTY-LINE SYSTEM

PRECAUTIONS:

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3 V and 3 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

D3381, MARCH 1990

Meets EIA Standards RS-422-A, RS485

 Meets CCITT Recommendations V.10, V.11, X.26, X.27

- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Driver Common-Mode Output Voltage Range of -7 V to 12 V
- Driver Positive- and Negative-Current Limiting
- Thermal Shutdown Protection
- Driver 3-State Outputs Active-High Enable
- Receiver Common-Mode Input Voltage Range of -12 V to 12 V
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Hysteresis . . . 50 mV Typ
- Receiver High-Input-Impedance . . .
 12 kΩ Min
- Receiver 3-State Outputs Active-Low Enable for SN751177 Only
- Operates from Single 5-V Supply

description

The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 M bits per second. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422-A, RS-485 and several CCITT recommendations.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission bus line.

The receiver features high input impedance of $12 \text{ k}\Omega$, an input sensitivity of $\pm 200 \text{ mV}$ over a common-mode input voltage range of -12 V to 12 V and typical input hysteresis of 50 mV. Failsafe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

The SN751177 and SN751178 are characterized for operation from -20°C to 85°C.

SN751177 N PACKAGE (TOP VIEW)

| 1B [| ī | U16 |] vcc |
|------|----|-----|-------|
| 1A [| 2 | 15 |] 1D |
| 1R [| 3 | 14 |] 1Y |
| RE [| 4 | 13 |] 1Z |
| 2R [| 5 | 12 |] DE |
| 2A [| 6 | 11 |] 2Z |
| 2B [| 7 | 10 |] 2Y |
| ND F | 18 | 9 | □ 2D |

SN751178 N PACKAGE (TOP VIEW)

| 1B |]1 | U16 | □vcc |
|-----|----|-----|------|
| 1A |]2 | 15 |] 1D |
| 1R | 3 | 14 |] 1Y |
| 1DE |]4 | 13 |] 1Z |
| 2R |]5 | 12 | 2DE |
| 2A | 6 | 11 |] 2Z |
| 2B | 7 | 10 |] 2Y |
| GND |]8 | 9 | 2D |

SN751177, SN751178
FUNCTION TABLE OF EACH DRIVER

| INPUT | ENABLE | OUTPUT | | |
|-------|--------|--------|---|--|
| D | DE | Y | Z | |
| Н | Н | Н | L | |
| L | Н | L | н | |
| Х | L | Z | Z | |

SN751177
FUNCTION TABLE OF EACH RECEIVER

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|----------------------------------|--------------|-------------|
| V _{ID} ≥ 0.2 V | L | Н |
| -0.2 V < V _{ID} < 0.2 V | L | ? |
| V _{ID} ≤ -0.2 V | L | L |
| X | н | Z |

SN751178
FUNCTION TABLE OF EACH RECEIVER

| DIFFERENTIAL INPUTS | OUTPUT |
|----------------------------------|--------|
| A - B | R |
| V _{ID} ≥ 0.2 V | Н |
| -0.2 V < V _{ID} < 0.2 V | ? |
| Vin ≤ -0.2 V | L |

H = high level, L = low level, ? = indeterminate,

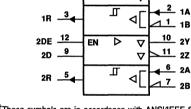
X = irrelevant, Z = high impedance (off)



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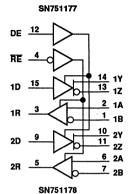
logic symbols†

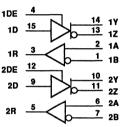
SN751177 EN1 EN2 1D 15 13 1Z 10 I 1R 3 1 1B 10 2Y 17 2D _9 11 2Z 10 6_ 2A I SN751178 1DE _4 ΕN Þ 1D _15 13_ 1Z



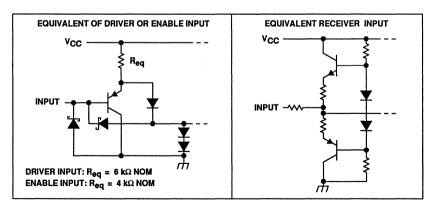
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagrams (positive logic)



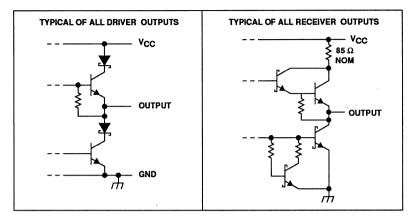


schematics of inputs



All resistor values are nominal.

schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | |
|--|---------------|
| Input voltage, DE, RE, and D inputs | 7 V |
| Input voltage range, receiver A or B inputs | 25 V to 25 V |
| Receiver differential input voltage range (see Note 2) | 25 V to 25 V |
| Output voltage range, Driver | –10 V to 15 V |
| Receiver low-level output current | 50 mA |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note | e 3) 1150 mW |
| Operating free-air temperature range, TA | 20°C to 85°C |
| Storage temperature range | 65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260°C |

- NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
 - 2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
 - 3. For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|----------------------|------|-----|-------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | DE, RE, and D inputs | 2 | | | V |
| Low-level input voltage, V _{IL} | DE, RE, and D inputs | | | 8.0 | V |
| Common-mode output voltage, V _{OC} (see Note 4) | | -7 | | 12 | V |
| High-level output current, IOH | Driver | | | - 60 | mA |
| Low-level output current, IOL | | | | 60 | mA |
| Common-mode input voltage, V _{IC} | | | | ± 12 | ٧ |
| Differential input voltage, V _{ID} | - Possivor | | | ± 12 | ٧ |
| High-level output current, IOH | | | | - 400 | μΑ |
| Low-level output current, I _{OL} | | | | 16 | mA |
| Operating free-air temperature, TA | • | - 20 | | 85 | °C |

NOTE 4: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.



DRIVER SECTIONS

driver electrical characteristics over recommended ranges of supply voltage and operating freeair temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITI | ONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|---|--------------------------|----------------------|------------------|-------|------|
| VιK | Input clamp voltage | l _j = - 18 mA | | | | - 1.5 | ٧ |
| VOH | High-level output voltage | $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, | I _{OH} = -33 mA | | 3.7 | | ٧ |
| VOL | Low-level output voltage | $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, | IOH = 33 mA | | 1.1 | | ٧ |
| VOD1 | Differential output voltage | I _O = 0 | | 1.5 | | 6 | ٧ |
| | | D: 100 O See Figure 1 | | 2 | | | |
| VOD2 | Differential output voltage | $R_L = 100 \Omega$, See Figure 1 | | 1/2 V _{OD1} | | | V |
| | | $R_L = 54 \Omega$, See Figure 1 | | 1.5 | | 5 | |
| V _{OD3} | Differential output voltage | See Note 5 | | 1.5 | | . 5 | ٧ |
| | Change in magnitude of differential | | | | | ± 0.2 | V |
| ΔIVODI | output voltage (see Note 6) | | | | | 10.2 | v |
| Voc | Common-mode output voltage | $R_1 = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | -1 | | 3 | v |
| VOC | (see Note 4) | H_ = 34 32 01 100 32, | See Figure 1 | ' | -, | | V |
| ΔIVOCI | Change in magnitude of common-mode | | | | | ± 0.2 | V |
| 400 | output voltage (see Note 6) | | | İ | | 10.2 | · · |
| <u>o</u> | Output current with power off | $V_{CC} = 0$, $V_{O} = -7 V t$ | o 12 V | | | ± 100 | μΑ |
| loz | High-impedance-state output current | $V_{O} = -7 \text{ V to } 12 \text{ V}$ | | | | ± 100 | μΑ |
| ΊΗ | High-level input current | V _{IH} = 2.7 V | | | | 20 | μA |
| IL | Low-level input current | V _{IL} = 0.4 V | , | | | - 100 | |
| | Short circuit output current | V _O = -7 V | | | | - 250 | mA |
| los | Short-circuit output current (see Note 7) | Vo = Vcc | | | | 250 | |
| | (See Note /) | V _O = 12 V | | | | 250 | |
| loo | Supply current | No load | outputs enabled | | 80 | 110 | |
| CC | Зорру синен | 140 1040 | outputs disabled | | 50 | 80 | μА |

[†]All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$

NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

- 5. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
- Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
- 7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

driver switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

| | PARAMETER | TEST CO | TEST CONDITIONS | | TYP | MAX | UNIT |
|------------------|--|---|-------------------------|--|-----|-----|------|
| t _{DD} | Differential output delay time | $R_L = 54 \Omega$, | C _L = 50 pF, | | 20 | 25 | ns |
| ^t TD | Differential output transition time | See Figure 3 | | | 27 | 35 | ns |
| tPLH | Propagation delay time, low-to-high-level output | $R_L = 27 \Omega$, | C _L = 50 pF, | | 20 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 4 | | | 20 | 25 | ns |
| ^t PZH | Output enable time to high level | R _L = 110 Ω, See Figure 5 | C _L = 50 pF, | | 80 | 120 | ns |
| tPZL | Output enable time to low level | R _L = 110 Ω, See Figure 6 | C _L = 50 pF, | | 40 | 60 | ns |
| ^t PHZ | Output disable time from high level | R _L = 110 Ω, See Figure 5 | C _L = 50 pF, | | 90 | 120 | ns |
| tPLZ | Output disable time from low level | R _L = 110 Ω, See Figure 6 | C _L = 50 pF, | | 30 | 45 | ns |

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422A | RS-485 |
|----------------------|--------------------------------------|-----------------------------------|
| IV _{OD1} I | v _o | v _o |
| IV _{OD2} I | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test termination |
| IAOD31 | | measurement 2) |
| ΔIV _{OD} I | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | IV _{OS} I | IV _{OS} I |
| ΔIVOCI | lV _{OS –} ∇ _{OS} I | IVos - Vosl |
| los | I _{sa} , I _{sb} | |
| lo | $ I_{xa} , I_{xb} $ | l _{ia} , l _{ib} |

RECEIVER SECTIONS

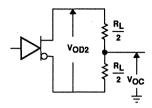
receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|---|------------|---|---------------------------|-------|------------------|-------|------|
| VTH | Differential input high threshold voltage | | $V_{O} = 2.7 V$ | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | V |
| VTL | Differential input low threshold voltage (s | ee Note 4) | $V_{O} = 0.5 V$ | l _O = 16 mA | - 0.2 | | | ٧ |
| V _{hys} | Input hysteresis (see Note 8) | | | | | 50 | | mV |
| VIK | Enable clamp voltage | SN751177 | I _j = - 18 mA | | | | - 1.5 | ٧ |
| VOH | VOH High-level output voltage | | $V_{ID} = 200 \text{ mV},$ | I _{OH} = -400 μA | 2.7 | | | V |
| Vai | V _{OL} Low-level output voltage | | Vin = 200 mV | I _{OL} = 8 mA | | | 0.45 | v |
| VOL | | | V _{ID} = -200 mV I _{OL} = | | | | 0.5 | \ \ |
| loz | High-impedance-state output current | SN751177 | $V_O = 0.4 \text{ V to 2}.$ | 4 V | | | ± 20 | μΑ |
| ι. | Line input current (see Note 9) | | Other input | V _I = 12 V | | | 1 | mA |
| l ₁ | Line input current (see Note 9) | | at 0 V | $V_1 = -7 V$ | | | - 0.8 | IIIA |
| ΉΗ | High-level enable input current | SN751177 | $V_{IH} = 2.7 V$ | | | | 20 | μΑ |
| IL | Low-level enable input current | SN751177 | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| los | Short-circuit output current (see Note 7) | | | | - 15 | | - 85 | mA |
| Icc | Supply current | | No load, | outputs enabled | | 80 | 110 | mA |
| rį | Input resistance | | | | 12 | | | kΩ |

- † All typical values are at V_{CC} = 5 V and T_A = 25°C NOTES: 4. The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
 - 7. Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
 - 8. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, VT_.
 - 9. Refer to EIA standards RS-422-A, RS-423-A, RS-485-A for exact conditions.

receiver switching characteristics at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

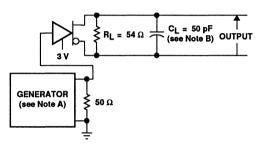
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|---|---|--|-------------------------|--------------|-----|-----|------|----|
| tpLH Propagation delay time, low-to-high-level output | | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ | | | 20 | 35 | ns | |
| tPHL | tpHL Propagation delay time, high-to-low-level output | | $C_L = 15 pF$, | See Figure 7 | | 22 | 35 | ns |
| ^t PZH | Output enable time to high level | | | | | 17 | 25 | ns |
| tPZL | Output enable time to low level | 01754477 | C _L = 15 pF, | See Figure 8 | | 20 | 27 | ns |
| tPHZ | Output disable time from high level | SN/511// | | | | 25 | 40 | ns |
| tpLZ | Output disable time from low level | | | | | 30 | 40 | ns |

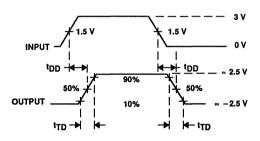


V_{ID} V_{OH}

FIGURE 1. DRIVER TEST CIRCUIT, VOD AND VOC

FIGURE 2. RECEIVER TEST CIRCUIT, VOH AND VOL





(a) DRIVER TEST CIRCUIT

(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 3. DRIVER DIFFERENTIAL OUTPUT DELAY AND TRANSITION TIMES

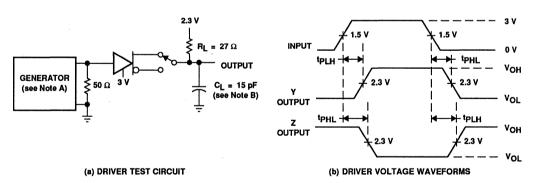
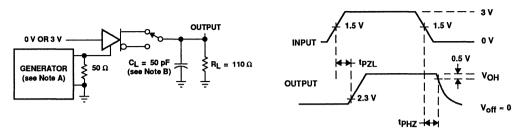


FIGURE 4. DRIVER PROPAGATION DELAY TIMES

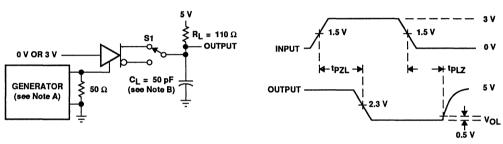
NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $Z_0 = 50 \Omega$, $t_f \leq 6$ ns. B. C_L includes probe and jig capacitance.



(a) DRIVER TEST CIRCUIT

(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES



(a) DRIVER TEST CIRCUIT

(b) DRIVER VOLTAGE WAVEFORMS

FIGURE 6. DRIVER ENABLE AND DISABLE TIMES

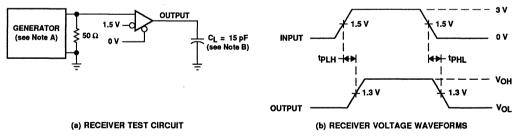
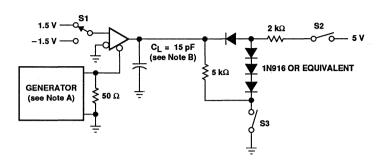


FIGURE 7. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The pulse generator has the following characteristics: PRR $\,\leq\,$ 1 MHz, 50% duty cycle, $Z_0=50~\Omega,~t_T\leq\,6$ ns., $t_f\leq\,6$ ns., $t_f\leq\,6$ ns. B. C₁ includes probe and jig capacitance.



(a) RECEIVER TEST CIRCUIT

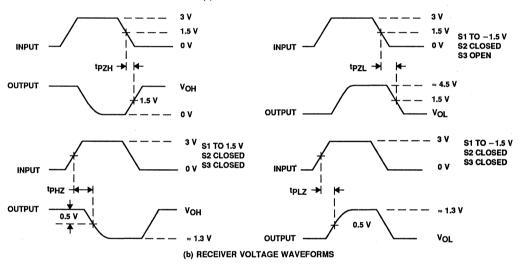


FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The pulse generator has the following characteristics: PRR \le 1 MHz, 50% duty cycle, $Z_0 = 50 \Omega$, $t_f \le 6$ ns. B. C_L includes probe and jig capacitance.

D3494, MAY 1990

- Meets IBM 360/370 Input/Output Interface Specification for 4.5 Mb/s Operation
- Single 5-V Supply
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Driver Output Short-Circuit Protection
- Driver Input/Receiver Output Compatible with TTL
- Receiver Input Resistance ... 7.4 kΩ to 20 kΩ
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low

description

The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

An open line will affect the receiver input as would a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line, by pulling either DE1 or DE2 to a low level.

D OR N PACKAGE (TOP VIEW)

| DE1 | ī | U16 | bvc. |
|-------|---|-----|------|
| RI1 | 2 | 15 | DO1 |
| RO1 [| 3 | 14 | DI1 |
| RI2 [| 4 | 13 | DO2 |
| RO2 [| 5 | 12 | DI2 |
| RI3 [| 6 | 11 | DO3 |
| RO3 [| 7 | 10 | DI3 |
| GND [| 8 | 9 | DE2 |
| | | | |

FUNCTION TABLE OF EACH DRIVER

| | INPUT | rs | OUTPUT |
|----|-------|-----|--------|
| DI | DE1 | DE2 | DO |
| L | Х | X | L |
| X | L | X | L |
| X | X | L | L |
| Н | Н | Н | Н |

FUNCTION TABLE OF EACH RECEIVER

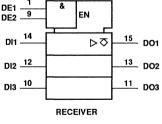
| INPUT | OUTPUT |
|-------|--------|
| RI | RO |
| L | Н |
| н | L |
| OPEN | н |

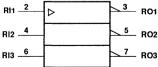
H = high level, L = low level,

X = irrelevant

logic symbols†

DRIVER



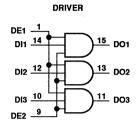


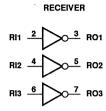
[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Texas VI

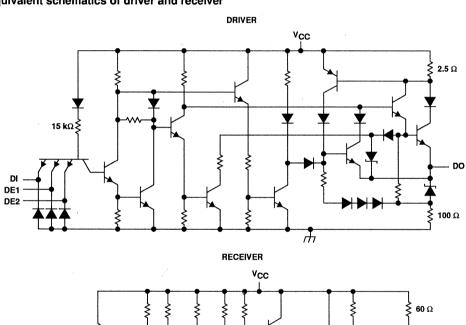
SN751730 TRIPLE LINE DRIVERS/RECEIVERS

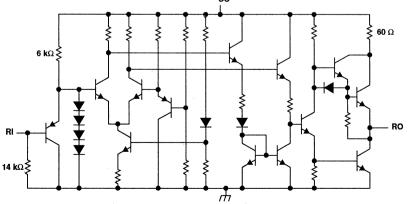
logic diagrams (positive logic)





equivalent schematics of driver and receiver





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | |
|--|--------------------------------|
| Input voltage range, V ₁ : Driver | |
| Receiver | |
| Output voltage range, VO Driver | |
| Enable input voltage range | |
| Continuous total power dissipation | . See Dissipation Rating Table |
| Operating free-air temperature range, TA | 0°C to 70°C |
| Storage temperature range | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | |

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | | |
|---------|---------------------------------------|---------------------------------|---------------------------------------|--|--|
| D | 950 mW | 7.6 mW/°C | 608 mW | | |
| N | 1150 mW | 9.2 mW/°C | 736 mW | | |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT | |
|---|----------------|------|-----|------|------|--|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V | |
| High-level input voltage, V _{IH} | Driver, Enable | 2 | | | T | |
| | Receiver | 1.55 | | | 1 ' | |
| Low-level input voltage, V _{II} | Driver, Enable | | | 0.8 | V | |
| Low-level Input voltage, VIL | Receiver | | | 1.15 | 1 ' | |
| Operating free-air temperature, TA | | 0 | | 70 | °C | |

SN751730 TRIPLE LINE DRIVERS/RECEIVERS

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT | |
|-----------|--|---------|--|---|------|------|--------------|------|
| VIK | Input clamp voltage | | $V_{CC} = 4.75 V$, | I _{IL} = - 18 mA | | | - 1.5 | ٧ |
| | | | $V_{CC} = 4.75 \text{ V},$ $I_{OH} = 59.3 \text{ mA},$ | | 3.11 | | | |
| ., | | | $V_{CC} = 5.25 \text{ V},$ $I_{OH} = 78.1 \text{ mA}$ | V _{IH} = 2 V, | | 4.10 | v | |
| Vон | High-level output voltage | | $V_{CC} = 4.75 \text{ V},$ $R_{L} = 51.4 \Omega$ | V _{IH} = 2 V, | 3.05 | | | |
| | | | $V_{CC} = 5.25 \text{ V},$ $R_L = 56.9 \Omega$ | V _{IH} = 2 V, | | | 4.20 | |
| VODH | Differential high-level output voltage | | $R_L = 46.3 \Omega \text{ or } 56.$ | 9 Ω | | | 0.50 | ٧ |
| VOL | Low-level output voltage | | $V_{CC} = 5.25 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | $l_{OL} = -0.24 \text{ mA}$ | | | 0.15 | v |
| VOL. | Low lover output voltage | | V _{IH} = 4.5 V | $R_L = 56.9 \Omega$ | | | 0.5 | • |
| l | High-level input current | DI | $V_{CC} = 5.25 V,$ | V _{IH} = 2.7 V | | | 20 | μА |
| ΊΗ | riigii-levei ilipat current | DE | VCC = 0.25 V, | VIH = 2.7 V | | | 60 | μΛ |
| 1 | Low-level input current | DI | $V_{CC} = 5.25 V$ | V _{II} = 0.4 V | | | – 400 | μА |
| IL | Low-level input current | DE | VCC = 3.23 V, | VIL = 0.4 V | | | - 1200 | μ. |
| 1 | High-level output current | | $V_{CC} = 4.75 V$, | V _{IL} = 0 | | | 100 | μА |
| ЮН | rigit-level output current | | V _{OH} = 5 V | $V_{IH} = 4.5 V$ | | | 100 | μΑ |
| los | Short-circuit output current | | $V_{CC} = 5.25 V$, | V _{IH} = 4.5 V | - 30 | | | mA |
| Іссн | 0 | | V _{CC} = 5.25 V, | $V_{I(D)} = 4.5 \text{ V},$ $V_{I(R)} = 0$ | | | 47 | mA |
| ICCL | Supply current (total package) | | No load | $V_{I(D)} = 0,$ $V_{I(R)} = 4.5 \text{ V}$ | | | 80 | IIIA |

driver switching characteristics, $V_{CC} = 5 V \pm 5\%$, $T_A = 25$ °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|---|-----|-----|------|------|
| ^t PLH | Propagation delay time, low to high level output | | | 6.5 | 12 | 18.5 | ns |
| tPHL | Propagation delay time, high to low level output | $R_L = 47.5 \Omega$ | See Figure 1 | 6.5 | 12 | 18.5 | ns |
| ΔtpD | Differential propagation delay time [†] | } _ | | | | 10 | ns |
| t _r | Output rise time | V _{CC} = 5 V, | $V_O = 0.15 \text{ to } 3.05 \text{ V},$ $C_1 = 10.2 \text{ pF},$ | 5 | 10 | | ns |
| tf | Output fall time | See Figure 1 | O[= 10.2 pr, | 5 | 13 | | ns |
| SR | Slew rate | $V_O = 1 \text{ to } 3 \text{ V}$ $C_I = 10.2 \text{ pF}$ | average, $R_L = 47.5 \Omega$, See Figure 1 | | | 0.65 | V/ns |

 $^{^{\}dagger}\Delta t_{PD} = |t_{PLH} - t_{PHL}|$

receiver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

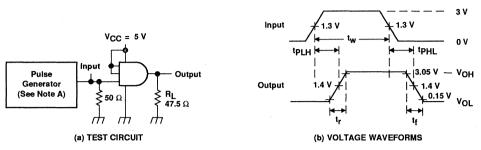
| PARAMETER | | TEST CONDITIONS | S MIN | TYP MAX | UNIT |
|-----------------|--|---|----------------|------------|------|
| VOH | High-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{I} = 1.15$ $I_{OH} = -400 \mu\text{A}$ | 5 V, | | V |
| V _{OL} | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, I_{OL} = 8 \text{ r}$ $V_{IH} = 1.55 \text{ V}, I_{OL} = 4 \text{ r}$ | | 0.5 0.4 | → V |
| rį | Input resistance | $V_{CC} = 0, 	 V_{I} = 0.15$ | 5 to 3.9 V 7.4 | 20 | kΩ |
| ΊΗ | High-level input current | $V_{CC} = 4.75 \text{ V}, V_{1H} = 3.$ | 11 V | 0.42 | mA |
| ηL | Low-level input current | $V_{CC} = 5.25 \text{V}, \text{V}_{ L} = 0.1$ | 15 V - 0.24 | 0.04 | mA |
| los | Short-circuit output current, See Note 2 | $V_{CC} = 5.25 \text{V}, V_{IL} = 0$ | - 20 | - 100 | mA |
| Іссн | Curality suggest (fasted analysis) | $V_{CC} = 5.25 \text{ V}, V_{I(D)} = 4.0 \text{ V}$ | | 47 | |
| ICCL | Supply current (total package) | No load $V_{I(D)} = 0$ $V_{I(R)} = 4$ | | 80 | mA |

NOTE 2: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

receiver switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

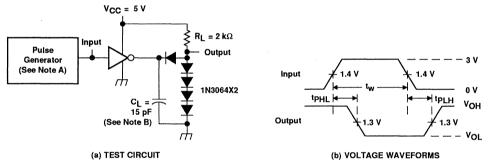
| | PARAMETER | TEST CO | ONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|----------------------------|------------------------|-----|-----|------|------|
| t _{PLH} | Propagation delay time, low to high level output | $R_1 = 2 k\Omega$. | C ₁ = 15 pF | 7.5 | 12 | 19.5 | ns |
| tPHL | Propagation delay time, high to low level output | HL = 2 KΩ, See Figure 2 | O[= 15 pr | 7.5 | 12 | 19.5 | ns |
| ΔtpD | Differential propagation delay time [†] | See Figure 2 | | | | 10 | ns |

 $^{\dagger}\Delta t_{PD} = |t_{PLH} - t_{PHL}|$



NOTE A: The pulse generator has the following characteristics: $z_0 \approx 50 \, \Omega$, $t_w \le 500 \, \text{ns}$, PRR $\le 1 \, \text{MHz}$, $t_f \le 6 \, \text{ns}$, $t_f \le 15 \, \text{ns}$

Figure 1. Driver Switching Times



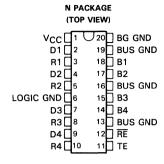
NOTES: A. The pulse generator has the following characteristics: $z_0 \approx 50 \ \Omega$, $t_W \le 500 \ ns$, PRR $\le 1 \ MHz$, $t_f \le 10 \ ns$, $t_r \le 10 \ ns$. B. C_1 includes probe and jig capacitance.

Figure 2. Receiver Switching Times

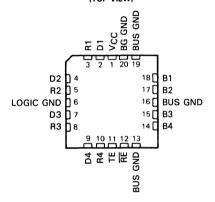
- High-Speed Quad Transceiver
- Fully Compatible with IEEE Std 896.1-1987 Futurebus Requirements
- Drives Load Impedances as Low as 10 Ω
- High-Speed Advanced Low-Power Schottky Circuits
- Low Power Dissipation . . . 81 mW Max per Channel
- High-Impedance P-N-P Inputs
- BTL™ Logic Level 1-V Bus Swing Reduces **Power Consumption**
- Low Bus-Port Capacitance
- Power-Up/Power-Down Protection (Glitch-Free)
- **Open-Collector Driver Outputs Allows** Wired-OR Connections
- Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference
- Designed to Be a Faster, Lower Power Functional Equivalent of National DS3893

description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This



FN CHIP CARRIER PACKAGE (TOP VIEW)



transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω .

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over VCC and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0°C to 70°C.

BTL is a trademark of National Semiconductor Corporation.



SN75ALS053 QUAD FUTUREBUS TRANSCEIVER

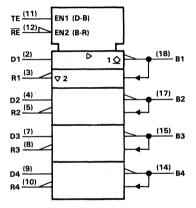
FUNCTION TABLE TRANSMIT/RECEIVE

| CONT | ROLS | CHANNELS | | |
|------|------|----------|-------|--|
| TE | RE | D →B | B → R | |
| L | L | D | R | |
| L | Н | D | D | |
| н | L | Т | R | |
| н | Н | Т | D | |

H = high level, L = low level, R = receive, T = transmit, D = disable

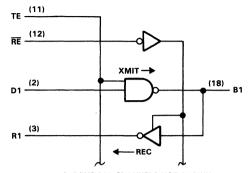
Direction of data transmission is from $\mbox{\rm Dn}$ to $\mbox{\rm Bn},$ direction of data reception is from $\mbox{\rm Bn}$ to $\mbox{\rm Rn}.$

logic symbol[†]

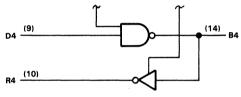


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

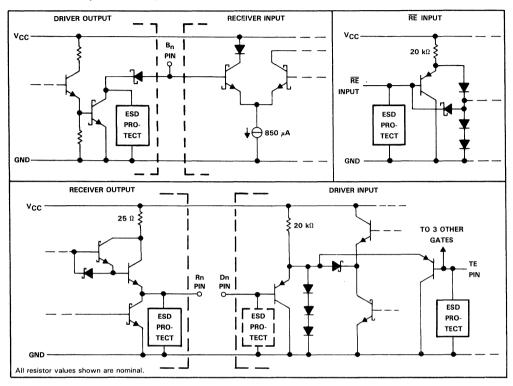
logic diagram (positive logic)



2 IDENTICAL CHANNELS NOT SHOWN



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | . 6 | ٧ |
|---|------|----|
| Control input voltage | 5.5 | ٧ |
| Driver input voltage | 5.5 | V |
| Driver output voltage | 2.5 | V |
| Receiver input voltage | 2.5 | V |
| Receiver output voltage | 5.5 | V |
| Continuous total power dissipation See Dissipation Rating | Tab | le |
| Operating free-air temperature range | 70° | ,C |
| Storage temperature range65°C to 1 | 50° | ,C |
| Case temperature for 10 seconds: FN package | 260° | 'C |
| Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: N package | 260° | 'n |

NOTE 1: Voltage values are with respect to network ground terminal.



DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| FN | 1400 mW | 11.2 mW/°C | 896 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | V |
| High-level driver and control input voltage, VIH | 2 | | | ٧ |
| Low-level driver and control input voltage, V _{IL} | | | 0.8 | V |
| Bus termination voltage | 1.9 | | 2.1 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | - | TEST CONDITIONS | MIN | TYP MAX | UNIT | |
|-------------------|---|--------------|---|-------|---------|------|--|
| VIK | Input clamp voltage at Dn, DE, or RE | | I _I = -18 mA | | -1.5 | ٧ | |
| ٧ _T | Receiver input threshold at Bn | | | 1.426 | 1.674 | V | |
| Vон | High-level output voltage at Rn | | Bn at 1.2 V, RE at 0.8 V, | 2.5 | | ٧ | |
| | | Rn | Bn at 2 V, RE at 0.8 V, IOL = 20 mA | | 0.5 | | |
| V _{OL} | Low-level output voltage | Bn | Dn at 2.4 V, TE at 2.4 V, $V_L = 2 \text{ V}, R_L = 10 \ \Omega,$ See Figure 1 | 0.75 | 1.2 | ٧ | |
| | | Dn, TE or RE | V _I = V _{CC} | | 40 | | |
| ΙН | High-level input current | Bn | $V_I = 2 V$, $V_{CC} = 0 \text{ or } 5.25 V$, Dn at 0.8 V, TE at 0.8 V, | | 100 | μΑ | |
| ŊĹ | Low-level input current at Dn, TE or RE | | V _I = 0.4 V | | - 400 | μΑ | |
| los | Short-circuit output current at Rn | | Rn at 0 V, Bn at 1.2 V, RE at 0.8 V | -70 | - 200 | mA | |
| lcc | Supply current | | | | 65 | mA | |
| C _{o(B)} | Driver output capacitance | | V _{CC} = 5 V, T _A = 25°C | | 6.5 | pF | |

switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

driver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|-----------------|----------------|--|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | | TE at 3 V , $\text{V}_1 = 2 \text{ V}$, | 2 | 7 | |
| tPHL | Propagation delay time high-to-low-level output | Dn | Bn | See Figure 2 | 2 | 7 | ns |
| tPLH | Propagation delay time, low-to-high-level output | Dn | D- | Dn at 3 V, V _L = 2 V, | 2 | 7 | |
| ^t PHL | Propagation delay time, high-to-low-level output | Dii | Bn | See Figure 2 | 2 | 7 | ns |
| ^t TLH | Transition time, low-to-high-level output | Dn | Bn | TE at 3 V, $V_L = 2 V$, | 0.5 | 5 | ns |
| ^t THL | Transition time, high-to-low-level output | Ы | ы | See Figure 2 | 0.5 | 5 | 115 |
| | Skew between driver channels † | Dn | Bn | TE at 3 V, V _L = 2 V | | 1 | ns |

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|-----------------|----------------|---|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | Bn | Rn | RE at 0.3 V, TE at 0.3 V, See Figure 3 | 2 | 8 | ne |
| ^t PHL | Propagation delay time, high-to-low-level output | DII | 1111 | The at 0.5 V, Te at 0.5 V, See Figure 5 | 2 | 8 | ns |
| tPLZ | Output disable time from low level | RE | Rn | Bn at 2 V, TE at 0.3 V, $V_L = 5$ V, $C_L = 5$ pF, $R_{L1} = 500$ Ω , See Figure 4 | | 6 | ns |
| ^t PZL | Output enable time to low level | RE | Rn | Bn at 2 V, TE at 0.3 V, $V_L=5$ V, $C_L=5$ pF, $R_{L1}=500$ Ω , See Figure 4 | | 12 | ns |
| ^t PHZ | Output disable time from high level | RE | Rn | Bn at 1 V, TE at 0.3 V, VL = 0, CL = 5 pF, RL1 = 500 Ω , See Figure 4 | | 6 | ns |
| tPZH | Output enable time to high level | RE | Rn | Bn at 1 V, TE at 0.3 V, $V_L=0$, $C_L=5$ pF, $R_{L1}=500$ Ω , See Figure 4 | | 12 | ns |
| | Skew between receiver channels [†] | Bn | Rn | RE at 0.3 V, TE at 0.3 V | | 1 | ns |

[†]Skew is the difference between the propagation delay time (tpLH or tpHL) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both tpLH and tpHL.

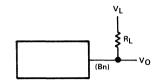
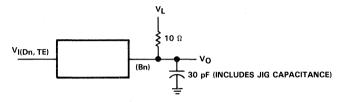
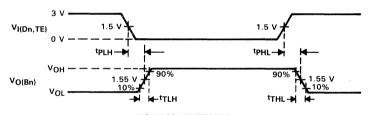


FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



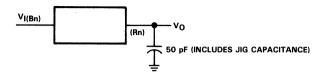
TEST CIRCUIT



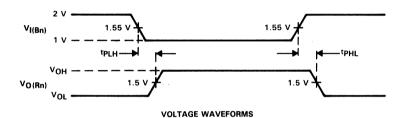
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \le 5 \text{ ns from } 10\% \text{ to } 90\%$

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

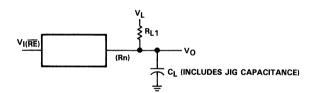


TEST CIRCUIT

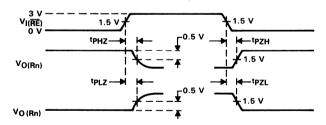


NOTE: $t_f = t_f \le 10 \text{ ns from } 10\% \text{ to } 90\%$

FIGURE 3. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEVORMS

NOTE: $t_r = t_f \le 5$ ns from 10% to 90%

FIGURE 4. PROPAGATION DELAY FROM RE TO Rn





D3025, AUGUST 1987-REVISED JUNE 1990

| SN75ALS056 Is an Octal Transceiver | |
|--|--|
| SN75ALS057 Is a Quad Transceiver | SN75ALS056 |
| High-Speed Advanced Low-Power Schottky Circuitry | DW OR N PACKAGE (TOP VIEW) |
| Low Power Dissipation 52.5 mW/Channel Max | A1 |
| High-Impedance P-N-P Inputs | A4 4 17 B4 |
| Logic Level 1-V Bus Swing Reduces Power Consumption | V _{CC} 5 16 GND A5 6 15 B5 |
| Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines | A6 |
| Power-Up/Down Protection (Glitch Free) | CS [10 11] T/R |
| Open-Collector Driver Outputs Allow Wired-OR Connections | SN75ALS057 DW OR N PACKAGE |
| Designed to Be a Faster, Lower Power | (TOP VIEW) |
| Functional Equivalent of National DS3896, DS3897 | D1 1 20 B1 R1 2 19 E1 |
| description | D2 3 18 B2 R2 4 17 E2 |
| The SN75ALS056 is an 8-channel, monolithic, | V _{CC} ☐5 16 GND |
| high-speed, advanced low-power Schottky | D3 6 15 B3 |
| device designed for 2-way data communication in a densely populated backplane. The | R3 ☐7 14 ☐ E3 D4 ☐8 13 ☐ B4 |
| SN75ALS057 is a 4-channel version with | R4 9 12 E4 |

These transceivers feature open-collector driver outputs with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pull-up termination on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as $18.5~\Omega$.

The receivers have internal low-pass filters to further improve noise immunity.

independent driver input (Dn) and receiver output (Rn) pins and a separate driver disable for each

driver (En).

The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.



logic symbols† logic diagrams (positive logic) SN75ALS056 SN75ALS056 T/R (11) CS (10) 3EN2 [B-A] CS (10) G3 (20) B1 A1 (1) XMIT -(<u>20)</u> B1 **▽** 2 (<u>19)</u> B2 A2 (2) (18) B3 A3 (3) (17)(15) В5 **6 IDENTICAL CHANNELS NOT SHOWN** A6 (7) (<u>14)</u> B6 (<u>12)</u> B8 (<u>13)</u> B7 (<u>12)</u> B8 A8 -**SN75ALS057** SN75ALS057 TE (10) EN1 [D-B] RE (11) EN2 [B-R] RE (11) & D (20) B1 E1 (19) 1 🛇 XMIT. R1 (2) ∇2 D2 (3) (1) (20) (18) B2 E2 (17) (19) R2 (4) (6) DЗ (15) _{B3} (2) (14)(7) RЗ D4 (8) (<u>13)</u> B4 (12)2 IDENTICAL CHANNELS NOT SHOWN E4 (9) R4 -(8) (13) - B4 (12)(9)

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN75ALS056 FUNCTION TABLE TRANSMIT/RECEIVE

| CONT | ROLS | CHANNELS |
|-----------------------------------|------|-----------|
| <u></u> C S | T/R | A ↔ B |
| L | Н | T (A → B) |
| L | L | R (B → A) |
| Н | Х | D |

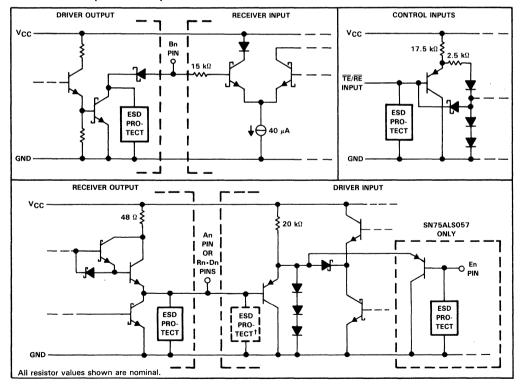
SN75ALS057 FUNCTION TABLE TRANSMIT/RECEIVE

| CC | ONTRO | LS | CHAN | INELS |
|----|-------|----|-------|-------|
| TE | RE | En | D → B | B→R |
| L | Ĺ | L | D | R |
| L | L | Н | Т | R |
| L | Н | L | Ð | D |
| L | Н | Н | Т | D |
| н | L | Х | D | R |
| Н | Н | Х | D | D |

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



[†]Additional ESD protection is on the SN75ALS057 only, which has separate receiver output and driver input pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Control input voltage |
| Driver input voltage |
| Driver output voltage |
| Receiver input voltage |
| Receiver output voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range |
| lead temperature 1.6 mm (1/16 inch) from case for 10 seconds 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| DW | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | ٧ |
| High-level driver and control input voltage, VIH | . 2 | | | ٧ |
| Low-level driver and control input voltage, VIL | | | 0.8 | ٧ |
| Bus termination voltage | 1.9 | | 2.1 | ٧ |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75ALS056 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | | TEST | CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|---|---|---|--|-------|------------------|-------|------|
| VIK | Input clamp voltage at An, | T/R, or CS | I _I = -18 mA | | | | - 1.5 | ٧ |
| VT | Receiver input threshold at | : Bn | | | 1.426 | | 1.674 | mV |
| Vон | High-level output voltage a | t An | Bn at 1.2 V, T/R at 0.8 V, | $\overline{\text{CS}}$ at 0.8 V, $I_{\text{OH}} = -400 \mu\text{A}$ | 2.4 | | | ٧ |
| | | An . | Bn at 2 V, T/R at 0.8 V, | • | | | 0.5 | |
| VOL | Low-level output voltage | Bn | An at 2 V, T/\overline{R} at 2 V, $R_L = 18.5 \Omega$, | $V_L = 2 V$, | 0.75 | | 1.2 | ٧ |
| | | An, T/\overline{R} , or \overline{CS} | VI = VCC | | | | 40 | |
| ΉΗ | High-level input current | Bn | $V_{ } = 2 V,$ An at 0.8 V, | $V_{CC} = 0 \text{ or } 5.25 \text{ V},$ T/ \overline{R} at 0.8 V | | | 100 | μΑ |
| IIL | Low-level input current at An, T/R, or CS | | V _I = 0.4 V | | | | - 400 | μΑ |
| los | Short-circuit output current at An | | An at 0 V, CS at 0.8 V, | Bn at 1.2 V, T/R at 0.8 V | -40 | | - 120 | mA |
| Icc | Supply current | | | | | | 75 | mA |
| C _{o(B)} | Driver output capacitance | | | | | 4.5 | | pF |

SN75ALS057 electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | | TEST | CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|------------------------------------|-------------------|--|--|------|------------------|-------|------------|
| VIK | Input clamp voltage at Dn, | En, TE, or RE | I _I = -18 mA | | | | -1.5 | ٧ |
| VT | Receiver input threshold at | Bn | | | 1426 | | 1674 | mV |
| Vон | High-level output voltage a | t Rn | Bn at 1.2 V, | | 2.4 | | | ٧ |
| | | Rn | Bn at 2 V, I _{OL} = 16 mA | • | | | 0.5 | |
| V _{OL} | Low-level output voltage | Bn | Dn at 2 V, TE at 0.8 V, R _L = 18.5 Ω, | V _L = 2 V, | 0.75 | | 1.2 | ٧ |
| | | Dn, En, TE, or RE | VI = VCC | | | | 40 | |
| ЧН | High-level input current | Bn | V _I = 2 V, Dn at 0.8 V, TE at 0.8 V | V _{CC} = 0 or 5.25 V, En at 0.8 V, | | | 100 | μ A |
| ΊL | Low-level input current at | On, En, TE, or RE | V _I = 0.4 V | | | | - 400 | μΑ |
| los | Short-circuit output current at Rn | | Rn at 0, RE at 0.8 V | Bn at 1.2 V, | -40 | | -120 | mA |
| Icc | Supply current | | | | | | 40 | mA |
| C _{o(B)} | Driver output capacitance | | | | | 4.5 | | pF |

 $^{^{\}dagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

SN75ALS056 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVER

switching characteristics over recommended ranges of operating free-air temperature and $V_{\hbox{\scriptsize CC}}$ (unless otherwise noted)

driver

| | PARAMETER | | TO (OUTPUT) | TEST CONDI | TIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---|-----|---|--|---------------------------|-----|------------------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | An | D- | <u>CS</u> at 0.8 ∨, | T/R at 2 V, | | | 19 | |
| tPHL | Propagation delay time, high-to-low-level output | An | Bn | V _L = 2 V, | See Figure 2 | | | 18 | ns |
| tPLH | Propagation delay time, low-to-high-level output | cs | An and T/\overline{R} at 2 V, $V_L = 2 V$, | | | 24 | | | |
| tPHL | Propagation delay time, high-to-low-level output | | Bn | See Figure 2 | | | | 20 | ns |
| ^t PLH | Propagation delay time, low-to-high-level output | T/R | P. | $V_{I(An, Bn)} = 5 \text{ V},$ R_{L2} not connected, $R_{L1} = 18 \Omega,$ | , C _L = 30 pF, | | | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | Bn | | | | | 35 | 115 |
| tTLH | Transition time, low-to-high-level output | An | Bn | <u>CS</u> at 0.8 V, | T/R at 2 V, | 1 | 3 | 11 | ns |
| tTHL | Transition time, high-to-low-level output | / | JIII | V _L = 2 V, | See Figure 2 | 1 | 3 | 6 | 115 |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

SN75ALS056 TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVER

switching characteristics over recommended ranges of operating free-air temperature and VCC (unless otherwise noted)

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN MAX | UNIT |
|------------------|---|-----------------|----------------|--|---------|------|
| ^t PLH | Propagation delay time, low-to-high-level output | Bn | An | CS at 0.8 V, T/R at 0.8 V, See Figure 4 | 18 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | DII | An | CS at 0.6 V, 1/h at 0.6 V, See Figure 4 | 18 | 115 |
| ^t PLZ | Output disable time from low level | cs | An | Bn at 2 V, T/\overline{R} at 0.8 V, $C_L=5$ pF, $V_L=5$ V, $R_{L1}=390$ Ω , R_{L2} not connected, See Figure 5 | 18 | ns |
| tPZL | Output enable time to low level | CS | An | Bn at 2 V, T/\overline{R} at 0.8 V, $C_L=30$ pF, $V_L=5$ V, $R_{L1}=390$ Ω , $R_{L2}=1.6$ k Ω , See Figure 5 | 15 | ns |
| ^t PHZ | Output disable time from high level | cs | An | Bn at 0.8 V, T/ \overline{R} at 0.8 V, C _L = 5 pF, V _L = 0, R _{L1} = 390 Ω , R _{L2} not connected, See Figure 5 | . 8 | ns |
| tPZH | Output enable time to high level | CS | An | Bn at 0.8 V, T/ \overline{R} at 0.8 V, C $_{L}$ = 30 pF, V $_{L}$ = 0, R $_{L1}$ not connected, R $_{L2}$ = 1.6 k Ω , See Figure 5 | 17 | ns |
| ^t PLZ | Output disable time from low level | T/R | An | $\overline{\text{CS}}$ at 0.8 V, V _{I(An,Bn)} = 2 V, V _L = 5 V, R _{L1} = 390 Ω , R _{L2} not connected, C _L = 5 pF, See Figure 3 | 20 | ns |
| tPZL | Output enable time to low level | T/R | An | $\overline{\text{CS}}$ at 0.8 V, V _{I(An,Bn)} = 2 V, V _L = 5 V, R _{L1} = 390 Ω , R _{L2} = 1.6 k Ω , C _L = 30 pF, See Figure 3 | 40 | ns |
| tPHZ | Output disable time from high level | T/R | An | $\overline{\text{CS}}$ at 0.8 V, V _{I(An,Bn)} = 0, V _L = 0, R _{L1} = 390 Ω , R _{L2} not connected, C _L = 5 pF, See Figure 3 | 17 | ns |
| tPZH | Output enable time to high level | T/R | An | $\overline{\text{CS}}$ at 0.8 V, V _{[(An,Bn)} = 0, V _L = 0, R _{L1} not connected, R _{L2} = 1.6 k Ω , C _L = 30 pF, See Figure 3 | - 15 | ns |
| tw(NR | Receiver noise rejection pulse duration | Bn | An or Rn | CS at 0.8 V, T/R at 0.8 V, See Figure 6 | 3 . | ns |

SN75ALS057 Trapezoidal-waveform interface bus transceiver

switching characteristics over recommended ranges of operating free-air temperature and VCC (unless otherwise noted)

driver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST COND | ITIONS | MIN | TYP [†] | MAX | UNIT | | |
|------|---|-----------------|----------------|--|---------------------------------------|------------|-----------------------|-----|------|----|----|
| tPLH | Propagation delay time, low-to-high-level output | D | B | $\overline{\text{TE}}$ at 0.8 V, $V_L = 2 \text{ V}$, | RE at 2 V, | | | 19 | | | |
| tPHL | Propagation delay time, high-to-low-level output | Dn or En | Bn | | See Figure 2 | | | 18 | ns | | |
| tPLH | Propagation delay time, low-to-high-level output | TE | Bn | Dn, En, \overline{RE} at 2 V, R _{L1} = 18 Ω , | V _L = 2 V, See Figure 2 | | | 24 | | | |
| tPHL | Propagation delay time, high-to-low-level output | | | | | | | 20 | ns | | |
| tTLH | Transition time, low-to-high-level output | D F. | D F. | Dn or En | Bn | RE at 2 V, | V _L = 2 V, | 1 | 3 | 11 | ns |
| tTHL | Transition time, high-to-low-level output | DITOLEIL | BII . | TE at 0.8 V, | See Figure 2 | 1 | . 3 | 6 | 115 | | |

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN MAX | UNIT |
|------------------|---|-----------------|----------------|---|---------|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | | | 18 | |
| ^t PHL | Propagation delay time, high-to-low-level output | Bn | Rn | RE at 0.8 V, TE at 2 V, See Figure 4 | 18 | ns |
| ^t PLZ | Output disable time from low level | RE | Rn | Bn at 2 V, \overline{TE} at 2 V, $V_L = 5$ V, $C_L = 5$ pF, $R_{L1} = 390 \Omega$, R_{L2} not connected, See Figure 5 | 18 | ns |
| ^t PZL | Output enable time to low level | RE | Rn | Bn at 2 V, \overline{TE} at 2 V, $V_L = 5$ V, $C_L = 30$ pF, $R_{L1} = 390$ Ω , R_{L2} 1.6 k Ω , See Figure 5 | 15 | ns |
| ^t PHZ | Output disable time from high level | RE. | Rn | Bn at 0.8 V, $\overline{\text{TE}}$ at 2 V, $V_L = 0$, $C_L = 5 \text{ pF}$, $R_{L1} = 390 \Omega$, R_{L2} not connected, See Figure 5 | . 17 | ns |
| ^t PZH | Output enable time to high level | RE | Rn | Bn at 0.8 V, $\overline{\text{TE}}$ at 2 V, $V_L = 0$, $C_L = 30$ pF, R_{L1} not connected, $R_{L2} = 1.6$ k Ω , See Figure 5 | 17 | ns |
| tw(NR | Receiver noise rejection pulse duration | Bn | Cn | TE at 2.0 V, RE at 0.8 V, See Figure 6 | 3 | ns |

driver plus receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--------------------------|-----------------|----------------|--|-----|-----|------|
| | Propagation delay time, | | | , | | 40 | |
| tPLH | low-to-high-level output | D | Rn | DE -+ 0.0 V TE -+ 0.0 V S Figure 7 | | 40 | |
| | Propagation delay time, | Dn | nn. | RE at 0.8 V, TE at 0.8 V, See Figure 7 | | 40 | ns |
| ^t PHL | high-to-low-level output | | , | | 40 | 40 | |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



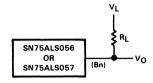
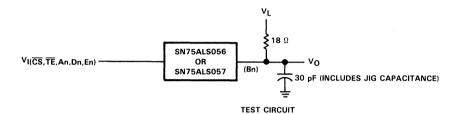
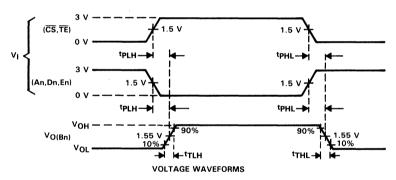


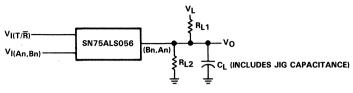
FIGURE 1. DRIVER LOW-LEVEL-OUTPUT-VOLTAGE TEST CIRCUIT



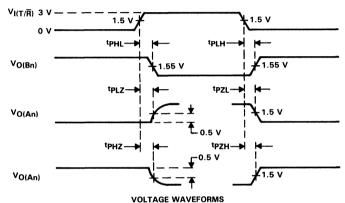


NOTE: $t_r = t_f \le 5 \text{ ns from } 10\% \text{ to } 90\%$

FIGURE 2. DRIVER PROPAGATION DELAY TIMES

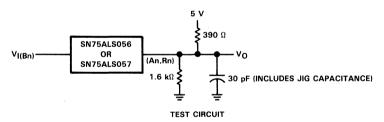


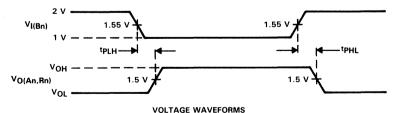
TEST CIRCUIT



NOTE: $t_r = t_f \le 5$ ns from 10% to 90%

FIGURE 3. PROPAGATION DELAY FROM T/R TO An OR Bn

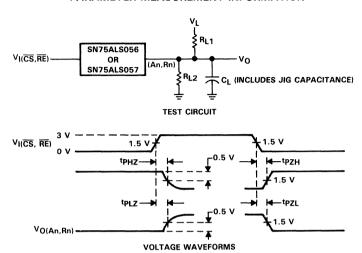




NOTE: $t_r = t_f \le 10 \text{ ns from } 10\% \text{ to } 90\%$

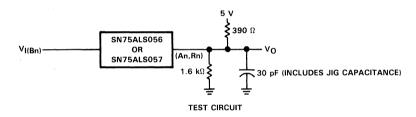
FIGURE 4. RECEIVER PROPAGATION DELAY TIMES





NOTE: $t_r = t_f \le 5 \text{ ns from } 10\% \text{ to } 90\%$

FIGURE 5. PROPAGATION DELAY FROM CS TO An OR RE TO Rn



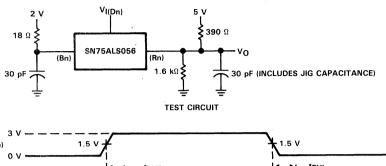


 t_W is increased until the output voltage fall just reaches 2 V. t_W is increased until the output voltage rise just reaches 0.8 V. VOLTAGE WAVEFORMS

NOTE: $t_f = t_f \le 2 \text{ ns from } 10\% \text{ to } 90\%$

FIGURE 6. RECEIVER NOISE IMMUNITY





 $V_{I(Dn)}$ tPHL. VO(Rn) **VOLTAGE WAVEFORMS**

NOTE: $t_r = t_f \le 5$ ns from 10% to 90%

FIGURE 7. DRIVER PLUS RECEIVER DELAY TIMES

SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

D3279, APRIL 1989

| • | Compatible with IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988 | DUAL-IN-LINE PACKAGE |
|---|--|---|
| | | (TOP VIEW) |
| • | Interdevice Loop-Back Paths for System Testing | TXI1 1 24 TX01 |
| | resung | H |
| • | Squelch Function Implemented on the | <u>[OOP</u> 1 ☐ 3 22 ☐ VCC |
| | Receiver Inputs | GND |
| | neceiver inputs | RXEN1 |
| • | Drivers Will Drive a Balanced 78-Ω Load | RXO1 ☐ 6 19 ☐ GND |
| _ | Transformer Coupling Not Required in | RXO2 🗍 7 18 🗍 GND |
| Ĭ | System | RXEN2 8 17 RXI2 |
| | 0,000 | GND |
| • | Power-Up/Power-Down Protection (Glitch- | <u>LOOP</u> 2 ☐ 10 15 ☐ V _{CC} |
| | Free) | TXEN2 11 14 TXO2 |
| • | Isolated Ground Pins for Reduced Noise | TXI2 12 13 TXO2 |
| | Coupling | |

description

Compatible

Fault-Condition Protection Built into the

Driver Inputs Are Level-Shifted ECL

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device will drive a $78-\Omega$ balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers will maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude will be maintained for the remainder of the packet. After the last positive packet edge transmitted into the driver, the driver will maintain a minimum of 70% of full differential output for a minimum of 200 ns, then decay down to a minimum level for the reset (idle) condition within 8 μ s. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8- μ s timeout. While operating, the driver is able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers will power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This assures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shut down and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. The RXEN pin will be driven high while the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit will also withstand a set of fault conditions while operating without causing permanent damage to the device.

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP}}1$ is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When $\overline{\text{LOOP}}1$ is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP}}2$ is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

RECEIVER FUNCTION TABLE LOOP = H

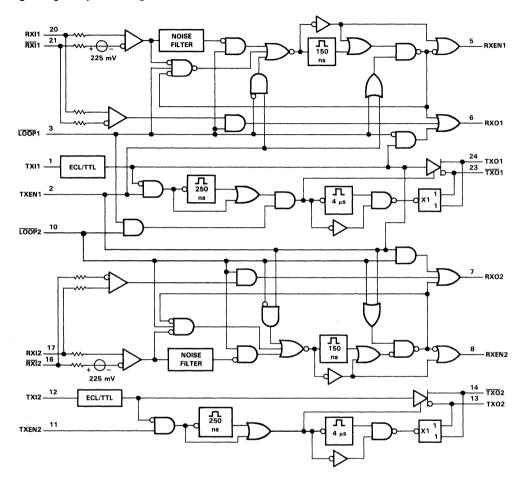
| | | OUTP | UTS |
|--|---------------|------|-----|
| RXI | PREVIOUS RXEN | RXEN | RXO |
| $V_{ID} = 1315 \text{ mV to } -175 \text{ mV, t}_W < 25 \text{ ns}$ | L | L | Н |
| $V_{ID} = -275 \text{ mV to } -1315 \text{ mV, t}_W > 50 \text{ ns}$ | X | н | L |
| $V_{ID} = 318 \text{ mV to } 1315 \text{ mV, } t_W < 130 \text{ ns}$ | н | н | н |
| $V_{ID} = 318 \text{ mV to } 1315 \text{ mV, } t_W > 175 \text{ ns}$ | X | L | Н |

DRIVER FUNCTION TABLE

| TXI | TXEN | PREVIOUS TXO | OUTPUT TXO |
|------------|------------|--------------|------------|
| L | L , | IDLE | IDLE |
| н | L | IDLE | IDLE |
| ↓ | н | IDLE | L |
| L | Н | ACTIVE | L |
| H < 200 ns | н | ACTIVE | н |
| H > 8 μs | н | ACTIVE | IDLE |
| L | L > 8 μs | ACTIVE | IDLE |
| H < 200 ns | L > 8 μs | ACTIVE . | IDLE |
| H < 200 ns | L < 200 ns | ACTIVE | н |
| H > 8 μs | L < 200 ns | ACTIVE | IDLE |
| L | L < 200 ns | ACTIVE | Ĺ |

 $H = V_I \ge V_T \text{ max}, L = V_I \le V_T \text{ min}$

logic diagram (positive logic)

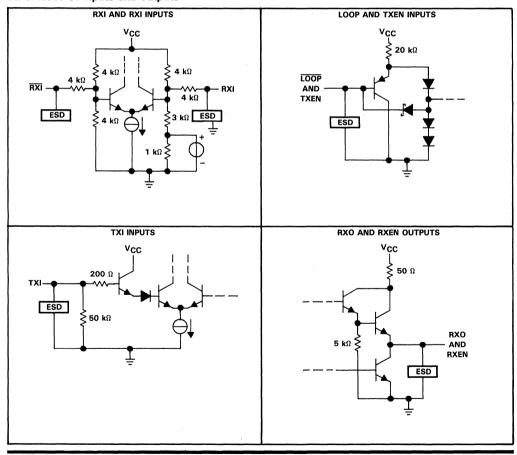


| I OOP | E1 | INIC | TIO | IN T | . V D | 1 6 |
|-------|----|------|-----|------|-------|-----|

| | INPUTS | | | | | | | OUTPUTS | | |
|-------|--------|--------|--------|--------|--------|--------|--------|---------|--------|--------|
| LOOP1 | LOOP2 | TXI1 | TXEN1 | RXI1 | RXI2 | RXO1 | RXO2 | RXEN1 | RXEN2 | TXO1 |
| L | L | L | Н | Х | Х | L | L | Н | Н | IDLE |
| L | L | н | Н | X | Х | н | Н | Н | Н | IDLE |
| L | L | X | L | Х | Х | н | Н | L | L | IDLE |
| L | Ĥ | L | Н | Х | NORMAL | L | NORMAL | Н | NORMAL | IDLE |
| L | Н | H | Н | Х | NORMAL | H | NORMAL | Н | NORMAL | IDLE |
| L | Н | X | L | Х | NORMAL | н | NORMAL | L | NORMAL | IDLE |
| Н | L | L | Н | NORMAL | Х | NORMAL | L | NORMAL | Н | IDLE |
| н | L | н | н | NORMAL | × | NORMAL | н | NORMAL | н | IDLE |
| н | L | Х | , L | NORMAL | Х | NORMAL | Н | NORMAL | L | IDLE |
| Н | Н | NORMAL | NORMAL | NORMAL | NORMAL | NORMAL | NORMAL | NORMAL | NORMAL | NORMAL |

H = high level, L = low level, X = don't care

schematics of inputs and outputs



SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| TXI and LOOP input voltage |
| TXO and TXO output voltage |
| RXI and RXI input voltage |
| RXO and RXEN output voltage |
| Continuous total power dissipation at (or below) 25 °C (see Note 2) |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate linearly to 800 mW at 70 °C at the rate of 10 mW/°C.

recommended operating conditions

| | MIN | NOM N | IAX | UNIT |
|---|------|-------|-----|------|
| Supply voltage, V _{CC} | 4.75 | 5 5 | .25 | ٧ |
| Common-mode voltage at RXI inputs, VIC | 1 | | 4.2 | V |
| Differential voltage between RXI inputs, VID | ±318 | ± 13 | 315 | mV |
| High-level input voltage, LOOP and TXEN, VIH | 2 | | | ٧ |
| Low-level input voltage, LOOP and TXEN, VIL | | | 0.8 | V |
| High-level output current, RXO and RXEN, IOH | | _ | 0.4 | mA |
| Low-level output voltage, RXO and RXEN, IOL | | | 16 | mA |
| Setup time, Driver mode, TXEN high before TXI↓, t _{su1} (see Figure 8) | 10 | | | ns |
| Setup time, Loop mode, LOOP low before TXEN1, t _{Su2} (see Figure 10) | 15 | | | ns |
| Setup time, Loop mode, TXEN high before TXI↓, t _{su3} (see Figure 10) | 10 | | | ns |
| Hold time, Loop mode, TXEN high after TXI1, th1 (see Figure 9) | 10 | | | ns |
| Hold time, Loop mode, LOOP low after TXEN↓, th ₂ (see Figure 9) | 15 | | | ns |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

| | PARAMETER | | TEST CON | DITIONS | MIN | MAX | UNIT |
|------------------|---|-------------------------|--|----------------------------|----------|--------|------|
| VIK | Clamp voltage at all inputs | I _I = -18 mA | | - 1.5 | V | | |
| | | | · · · · · · · · · · · · · · · · · · · | $V_{CC} = 4.75 \text{ V}$ | 3.202 | 3.752 | |
| | , | | TA = 0°C | V _{CC} = 5 V | 3.389 | 3.998 | V |
| | | | | V _{CC} = 5.25 V | 3.577 | 4.244 | |
| | | | | $V_{CC} = 4.75 \text{ V}$ | 3.213 | 3.797 | |
| VT | Driver input (TXI) threshold voltage | | $T_A = 25$ °C | V _{CC} = 5 V | 3.400 | 4.043 | · V |
| | | | | $V_{CC} = 5.25 \text{ V}$ | 3.588 | 4.289 | |
| | | | | $V_{CC} = 4.75 \text{ V}$ | 3.239 | 3.849 | |
| | | | $T_A = 70$ °C | $V_{CC} = 5 V$ | 3.426 | 4.095 | V |
| | | | | $V_{CC} = 5.25 \text{ V}$ | 3.614 | 4.341 | |
| VIDT | Receiver differential input threshold | voltage | | | | - 275 | mV |
| | | | TXEN at 0.8 V, LO | OP1 at 2 V, | | 4.0 | |
| | | Idle | LOOP2 at 2 V, See | Figure 1 | 1 | 4.2 | |
| | | | TXEN at 2 V, LOO | ⁵ 1 at 2 V, | | | |
| Voc | Driver output (TXO) common-mode | Active | LOOP2 at 2 V, TXI | at 3.2 V, | 1 | 4.2 | ., |
| Voc | voltage | | See Figure 1 | | | | V |
| | | | TXEN at 2 V, LOOP1 at 2 V, | | | | |
| | | Active | LOOP2 at 2 V, TXI at 4.4 V, | | 1 | 4.2 | |
| | | | See Figure 1 | | | | |
| | | Idle | TXEN at 0.8 V, LO | OP1 at 2 V, | | . 40 | |
| | | lale | LOOP2 at 2 V, See | Figure 1 | | ±40 | |
| | | | TXEN at 2 V, LOO | 51 at 2 V, | | | |
| \/ | Driver output (TXO) differential | Active | LOOP2 at 2 V, TXI | at 3.2 V, | -600 | - 1315 | mV |
| V _{OD} | voltage | | See Figure 1 | | | | mv |
| | | | TXEN at 2 V, LOO | 51 at 2 V, | | | |
| | | Active | LOOP2 at 2 V, TXI at 4.4 V, | | 600 1315 | 1315 | |
| | | 1 | See Figure 1 | | | | |
| Voн | High-level output voltage | RXO, RXEN | $I_{OH} = -0.4 \text{ mA}$ | $l_{OH} = -0.4 \text{ mA}$ | | | ٧ |
| VOL | Low-level output voltage | RXO, RXEN | I _{OL} = 16 mA | | | 0.5 | V |
| | | TXEN, LOOP | V _I = 2 V | | | 20 | |
| ΙН | High-level input current | TXI | $V_{I} = 4.5 V$ | | | 400 | μΑ |
| | | RXI, RXI | $V_{ID} = -0.5 \text{ V}, \text{ V}_{I}$ | C = 1 V to 4.2 V | | 1000 | |
| | | TXEN, LOOP | V _I = 0.8 V | | | - 200 | |
| 1 ₁ L | Low-level input current | TXI | V _I = 3.1 V | | | 100 | μΑ |
| 112 | Low level input current | | V _I = 0.3 V | | 4 | 10 | μΑ |
| | | RXI, RXI | $V_{\text{ID}} = 0.5 \text{ V}, V_{\text{IC}}$ | | | 1000 | |
| lop | Driver differential output current | Idle | TXEN at 0.8 V, LO | • | | ±4 | mA |
| -00 | | | LOOP2 at 2 V, See | | | | |
| los | Short-circuit output current [†] | RXO, RXEN | VO at 0 V, RXI at | | -40 | - 150 | mA |
| lcc | Supply current | | LOOP at 2 V, TXE | • | | 225 | mA |
| | | | TXI at 4.5 V, Outp | uts open | | | |

[†]Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.

SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS† | MIN MAX | UNIT |
|--|---------------------------------|---------|------|
| | TXO shorted to TXO, | 150 | |
| Driver fault condition current | Current measured in short | 150 | |
| | TXO at 0 V, TXO is open, | 150 | |
| | Current measured at TXO | 130 | |
| | TXO is open, TXO at 0, | 150 | |
| | Current measured at TXO | 130 | |
| Driver fault condition current | TXO at 0 V, TXO at 0 V, | 150 | mA |
| TXO shorted to T Current measured TXO at 0 V, TXO Current measured TXO is open, TXI Current measured TXO at 0 V, TXO Current measured TXO at 0 V, TXO Current measured TXO at 16 V, TX Current measured TXO at 16 V, TX Current measured TXO at 16 V, TX Current measured TXO at 16 V, TX Current measured TXO at 16 V, TX Current measured RXI shorted to RX Current measured RXI at 0 V, RXI is Current measured RXI is open, RXI Current measured RXI at 0 V, RXI at 0 V, RXI at 16 V, RXI Current measured RXI at 16 V, RXI Current measured RXI at 16 V, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured RXI at open, RXI Current measured | Current measured at TXO and TXO | 130 | """ |
| | TXO at 16 V, TXO is open, | 150 | |
| | Current measured at TXO | 130 | |
| | TXO is open, TXO at 16 V, | 150 | |
| | Current measured at TXO | 130 | |
| | TXO at 16 V, TXO at 16 V, | 150 | |
| | Current measured at TXO and TXO | 150 | |
| | RXI shorted to RXI, | 10 | |
| | Current measured in short | 2 | |
| | RXI at 0 V, RXI is open, | 3 | |
| | Current measured at RXI | 3 | |
| | RXI is open, RXI at 0 V, | 3 | |
| | Current measured at RXI | 3 | |
| Receiver fault condition current | RXI at 0 V, RXI at 0 V, | 3 | mA |
| neceiver fault condition current | Current measured at RXI and RXI | 3 | |
| | RXI at 16 V, RXI at open, | 10 | |
| | Current measured at RXI | 10 | |
| | RXI at open, RXI at 16 V, | 10 | |
| | Current measured at RXI | 10 | |
| | RXI at 16 V, RXI at 16 V, | 10 | |
| | Current measured at RXI and RXI | 10 | |

[†]Fault conditions should be measured on only one channel at a time.

switching characteristics over recommended ranges of operating free-air temperature and VCC (unless otherwise noted)

driver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|---|-----------------|---------------------|----------------------------|-----|-------|------|
| ^t PLH | Propagation delay time, low-to-high level output | TXI | тхо, Тхо | TXEN at 2 V, See Figure 3 | | 15 | ns |
| ^t PHL | Propagation delay time, high-to-low level output | TXI | тхо, Тхо | TXEN at 2 V, See Figure 3 | | 15 | ns |
| tPIL | Propagation delay time, idle-to-low level output | TXI | τχο, τχο | TXEN at 2 V, See Figure 4 | | 25 | ns |
| tPIL | Propagation delay time, idle-to-low level output | TXEN | тхо, Тхо | TXI at 3.2 V, See Figure 5 | | 25 | ns |
| * | Propagation delay time, | TXI | TXO, TXO | TXEN at 2 V, See Figure 6 | 200 | | |
| tPH70 | high-to-70% level output | TXEN | TXO, TXO | TXI at 4.4 V, See Figure 7 | 200 | | ns |
| * | Propagation delay time, | TXI | TXO, TXO | TXEN at 2 V, See Figure 6 | 200 | 8000 | |
| tPHI | high-to-idle output | TXEN | TXO, TXO | TXI at 4.4 V, See Figure 7 | 200 | 8000 | ns |
| ٧u | Driver output differential undershoot | TXI | тхо, Тхо | TXEN at 2 V, See Figure 6 | | - 100 | mV |
| ^t skew | Driver caused signal skew (tpLH - tpHL) | TXI | тхо, тхо | TXEN at 2 V, See Figure 3 | | ±3 | ns |
| t _r | Rise time, TXO, TXO | | | TXEN at 2 V, See Figure 3 | 1 | 5 | ns |
| tf | Fall time, TXO, TXO | | | TXEN at 2 V, See Figure 3 | 1 | 5 | ns |

receiver

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|-----------------|----------------|--|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high level output | RXI, RXI | RXO | V _{IC} = 1 V to 4.2 V, See Figure 11 | | 15 | ns |
| ^t PHL | Progagation delay time, high-to-low level output | RXI, RXI | RXO | V _{IC} = 1 V to 4.2 V, See Figure 11 | | 15 | ns |
| ^t PLH | Start-up delay time, low-to-high level output | RXI, RXI | RXEN | $V_{IC} = 1 \text{ V to } 4.2 \text{ V,}$ $V_{ID} = -500 \text{ mV, See Figure } 13$ | | 50 | ns |
| ^t PHL | Shutdown delay time, high-to-low level output | RXI, RXI | RXEN | V _{IC} = 1 V to 4.2 V, V _{ID} = 500 mV, See Figure 13 | 130 | 175 | ns |
| ^t skew | Receiver caused signal skew (tpLH - tpHL) | RXI, RXI | RXO | $V_{IC} = 1 V \text{ to } 4.2 V,$ $V_{ID} = 500 \text{ mV}, \text{ See Figure } 11$ | | ±3 | ns |
| t _W | Pulse duration at RXI and (to not activate squelch) | RXI | | $V_{IC} = 1 \text{ V to } 4.2 \text{ V,}$ $V_{ID} = -175 \text{ mV, See Figure } 12$ | 25 | | ns |
| t _w | Pulse duration at RXI and (to activate squelch) | RXI | | $V_{IC} = 1 \text{ V to } 4.2 \text{ V,}$ $V_{ID} = -275 \text{ mV, See Figure } 12$ | | 50 | ns |
| t _{r1} | Rise time, RXO | | | $V_{IC} = 1 \text{ V to } 4.2 \text{ V,}$ $V_{ID} = \pm 500 \text{ mV, See Figure } 11$ | 1 | 8 | ns |
| t _{r2} | Rise time, RXEN | | | $V_{IC} = 1 \text{ V to } 4.2 \text{ V,}$ $V_{ID} = \pm 500 \text{ mV, See Figure } 13$ | 1 | 8 | ns |
| t _{f1} | Fall time, RXO | | | $V_{IC} = 1 \text{ V to 4.2 V},$ $V_{ID} = \pm 500 \text{ mV}, \text{ See Figure 11}$ | 1 | 8 | ns |
| t _{f2} | Fall time, RXEN | | | $V_{IC} = 2.5 \text{ V}, V_{ID} = \pm 500 \text{ mV},$ See Figure 13 | 1 | 8 | ns |
| t _{valid} | RXO valid after RXEN high | 1 | | See Figure 11 | -10 | 15 | ns |

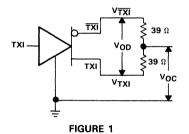
SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

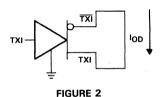
switching characteristics over recommended ranges of operating free-air temperature and V_{CC} (unless otherwise noted)

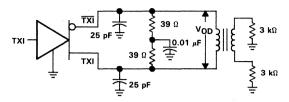
loop

| | PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|-----------------|----------------|--|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high level output | TXI | RXO | LOOP at 0.8 V, TXEN at 2 V, See Figure 14 | | 30 | ns |
| [†] PHL | Propagation delay time, high-to-low level output | TXI . | RXO | LOOP at 0.8 V, TXEN at 2 V, See Figure 14 | | 30 | ns |
| [†] PLH | Propagation delay time, low-to-high level output | TXEN | RXEN | LOOP at 0.8 V, See Figure 15 | | 50 | ns |
| ^t PHL | Propagation delay time, high-to-low level output | TXEN | RXEN | LOOP at 0.8 V, See Figure 15 | | 50 | ns |

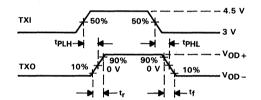
PARAMETER MEASUREMENT INFORMATION







TEST CIRCUIT

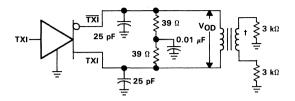


VOLTAGE WAVEFORMS

TRANSFORMER SPECIFICATIONS

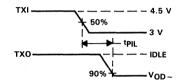
| Turns Ratio | 1:1 |
|--------------------------|-------------|
| Magnetizing Inductance | 26 to 30 μH |
| Winding Resistance | 0.6 Ω Max |
| Rise Time 10% to 90% | 5 ns Max |
| Interwinding Capacitance | 25 pF |
| Leakage Inductance | 0.25 μH Max |
| Inductive Q | 1250 Min |

FIGURE 3



[†]See Figure 3

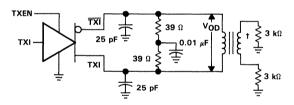
TEST CIRCUIT



VOLTAGE WAVEFORMS

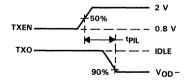
NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

FIGURE 4

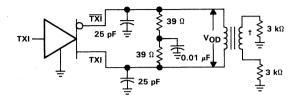


TEST CIRCUIT

[†]See Figure 3

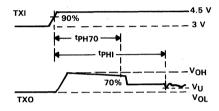


VOLTAGE WAVEFORMS
FIGURE 5



[†]See Figure 3

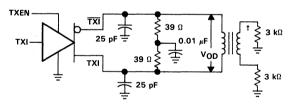
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

FIGURE 6



[†]See Figure 3

TEST CIRCUIT

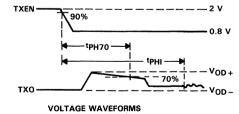
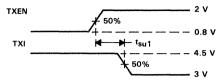
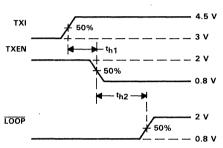


FIGURE 7



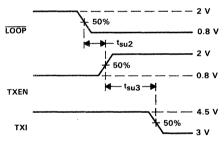
NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

FIGURE 8



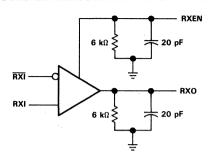
NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

FIGURE 9

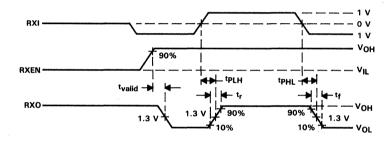


NOTE: Input $t_{\rm f} \le 5$ ns from 10% to 90%; $t_{\rm f} \le 5$ ns from 90% to 10%

FIGURE 10



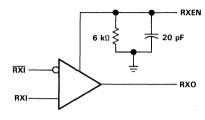
TEST CIRCUIT



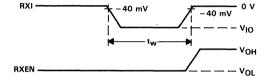
VOLTAGE WAVEFORMS

NOTE: Input $t_{f} \leq$ 5 ns from 10% to 90%; $t_{f} \leq$ 5 ns from 90% to 10%

FIGURE 11

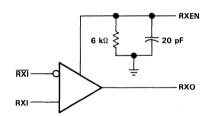


TEST CIRCUIT

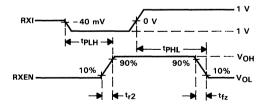


VOLTAGE WAVEFORMS

FIGURE 12



TEST CIRCUIT

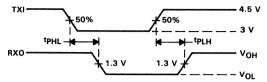


VOLTAGE WAVEFORMS

NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

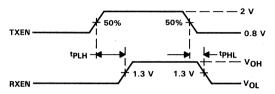
FIGURE 13





NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10%

FIGURE 14

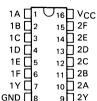


NOTE: Input $t_r \le 5$ ns from 10% to 90%; $t_f \le 5$ ns from 90% to 10% FIGURE 15

D1334, SEPTEMBER 1987-REVISED AUGUST 1989

- Permits Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair
- Operates with 50- Ω to 500- Ω Transmission Lines
- TTL-Compatible with 5-V Supply
- 2.4-V Output at IOH = -75 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- IMPACT™ Low-Power Schottky Technology
- Improved Replacement for the SN75121 and Signetics 8T13
- Glitchless Power-Up/Power-Down
- Short-Circuit Protection
- AND-OR Logic Configuration
- High Speed . . . Maximum Propagation
 Delay Time of 14 ns at C_I = 15 pF

D OR N PACKAGE (TOP VIEW)



FUNCTION TABLE

| INPUTS | | | | | | OUTPUT |
|------------------------------|---|---|---|---|---|--------|
| Α | В | С | D | E | F | Υ |
| Н | Н | Н | Н | Х | Х | Н |
| х | Х | Х | Х | Н | Н | н |
| All other input combinations | | | | | | L |

H = high level

L = low level

X = irrelevant

description

The SN75ALS121 dual line driver is designed for digital data transmission over lines having impedances from 50 to 500 Ω . It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 volts. All inputs are in conventional TTL configuration. Gating can be used during power-up and power-down sequences to ensure that no noise is introduced on the line.

The SN75ALS121 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

The SN75ALS121 is characterized for operation from 0°C to 70°C.

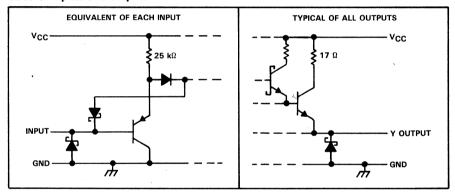
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logic diagram (positive logic) logic symbol† ≥10 1C 3 7 1Y ℧ 1D 4 1F 6 10 10 2A -11 2C 12 9 2Y 12 2D 13 13 14 14 2E 2F _15

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Output voltage |
| Continuous total dissipation at (or below) 25 °C free air temperature (see Note 2): |
| D package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the D package linearly to 608 mW at 70 °C at the rate of 7.6 mW/°C and the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.8 | ٧ |
| High-level output current, IOH | | | - 75 | mA |
| Operating free-air temperature range, T _A | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------|------------------------------|---------------------------------------|--|------------------------|-------|-------|-------|------|
| VIK | Input clamp voltage | $V_{CC} = 5 V$, | I _I = -12 mA | | | | - 1.5 | ٧ |
| V _{(BR)I} | Input breakdown voltage | $V_{CC} = 5 V$, | l _l = 10 mA | | 5.5 | | | ٧ |
| Vон | High-level output voltage | V _{IH} = 2 V, | I _{OH} = -75 mA, | See Note 3 | 2.4 | 3.2 | | ٧ |
| ¹ он | High-level output current | $V_{CC} = 5 V,$ $T_A = 25 ^{\circ}C,$ | V _{IH} = 4.5 V, See Note 3 | V _{OH} = 2 V, | - 100 | - 200 | - 250 | mA |
| loL | Low-level output current | $V_{1L} = 0.8 V,$ | $V_{OL} = 0.4 V,$ | See Note 3 | | | -800 | μΑ |
| IO(off) | Off-state output current | $V_{CC} = 3 V$, | V _O = 3 V | | | | 500 | μΑ |
| Iн | High-level input current | V _I = 4.5 V | | | | | 40 | μΑ |
| l _{IL} | Low-level input current | V _I = 0.4 V | | | | | -250 | μΑ |
| los | Short-circuit output current | V _{CC} = 5 V | | | | - 5 | - 30 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = 5.25 \text{ V},$ | All inputs at 2 V, | No load | | 9 | 14 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 V$, | All inputs at 0.8 V, | No load | | 13 | 30 | . mA |

 $^{^{\}dagger}$ All typical values are at VCC = 5 V and TA = 25 °C.

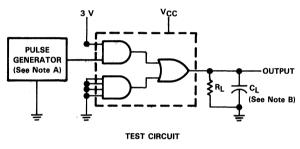
NOTE 3: The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

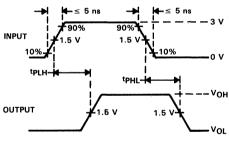
switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER TEST CONDITIONS | | MIN | TYP | MAX | UNIT | | | |
|---------------------------|--------------------------|------------|---------------------------------|--------------|------|----|----|-----|
| | Propagation delay time, | | | | | 6 | 14 | ns |
| tPLH | low-to-high-level output | P 27.0 | C 15 -5 | See Figure 1 | | | 14 | 115 |
| | Propagation delay time, | n[=3/11, | = 37 Ω, C _L = 15 pF, | See Figure 1 | | 4 | 14 | ns. |
| tPHL | high-to-low-level output | | | | | * | 14 | 115 |
| | Propagation delay time, | | | | | 18 | 30 | ns |
| tPLH | low-to-high-level output | P 27.0 | C: - 1000 nE | See Figure 1 | | 10 | 30 | 115 |
| | Propagation delay time, | n[= 3/11, | C _L = 1000 pF, | See rigure i | | 29 | 50 | ns |
| †PHL | high-to-low-level output | | | | | 29 | 50 | 118 |

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V and $T_A = 25$ °C.

PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, $t_W = 200 \text{ ns}$, duty cycle = 50%.

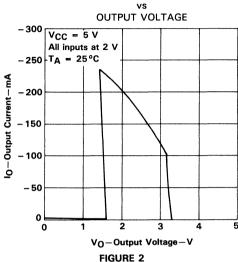
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT



- Meets IBM 360 Input Interface Specifications
- Permits Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair
- TTL-Compatible with 5-V Supply
- 3.11-V Output at IOH = -59.3 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- IMPACT™ Low-Power Schottky Technology
- Improved Replacement for the SN75123 and Signetics 8T13
- Glitchless Power-Up/Power-Down
- Short-Circuit Protection
- AND-OR Logic Configuration
- High Speed . . . Maximum Propagation
 Delay Time of 14 ns at C_L = 15 pF

description

The SN75ALS123 dual line driver is specifically designed to meet the input interface specifications for the IBM System 360. It is compatible with standard TTL logic and supply voltage levels. The low-impedance, emitterfollower outputs drive terminated lines such as coaxial cable, strip line, or twisted pair. The uncommitted output allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All inputs are in conventional TTL configuration. Gating can be used during power-up and powerdown sequences to ensure that no noise is introduced on the line.

The SN75ALS123 employs the IMPACT™ process to achieve fast switching speeds, low power dissipation, and reduced input current requirements.

The SN75ALS123 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE (TOP VIEW)

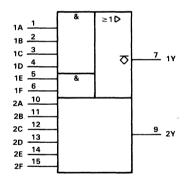
| 1C 1D | 1 U 2 3 4 5 6 | 16 15 14 13 12 | VCC]2F]2E]2D]2C]2B |
|---------|------------------------------|----------------------------|--|
| | - | 12 11 10 9 | _ |

FUNCTION TABLE

| INPUTS | | | | | | OUTPUT |
|--------|---------|---------|------|---------|----|--------|
| A | В | С | D | E | F | Υ |
| Н | Н | Н | Н | X | х | Н |
| Х | X | Х | Х | Н | н | н |
| Α | II othe | r input | comb | ination | ns | L |

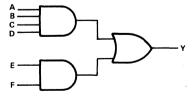
H = high level L = low level X = irrelevant

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)

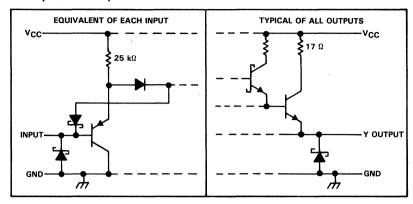


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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage |
| Output voltage |
| Continuous total dissipation at (or below) 25 °C free air temperature (see Note 2): |
| D package 950 mW |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the D package to 608 mW at 70 °C at the rate of 7.6 mW/°C and the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|-------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | ٧ |
| High-level output current, IOH | | | - 100 | mA |
| Operating free-air temperature range, TA | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | 3 | MIN | TYP [†] | MAX | UNIT |
|--------------------|------------------------------|--|--|------------------------------|-------------|------------------|-------|----------|
| VIK | Input clamp voltage | $V_{CC} = 5 V$, | I _I = -12 mA | | | | -1.5 | V |
| V _{(BR)I} | Input breakdown voltage | V _{CC} = 5 V, | lj = 10 mA | | 5.5 | | | ٧ |
| Vari | High-level output voltage | V _{CC} = 5 V, See Note 3 | V _{IH} = 2 V, | $I_{OH} = -59.3 \text{ mA},$ | 2.9 3.11 | | | > |
| Vон | riigii-level output voitage | $V_{CC} = 5 V$, $T_A = 25 ^{\circ}C$, | V _{IH} = 2 V, See Note 3 | $I_{OH} = -59.3 \text{ mA},$ | | 3.3 | | V |
| VOL | Low-level output voltage | $V_{IL} = 0.8 V,$ | $I_{OL} = -240 \mu A$ | See Note 2 | | | 0.15 | V |
| ЮН | High-level output current | $V_{CC} = 5 \text{ V},$ $T_A = 25 ^{\circ}\text{C},$ | V _{IH} = 4.5 V, See Note 3 | $V_{OH} = 2 V$, | - 100 | - 200 | -250 | mA |
| IO(off) | Off-state output current | $V_{CC} = 0$, | V _O = 3 V | | | | 40 | μΑ |
| ΊΗ | High-level input current | V _I = 4.5 V | | | | | 40 | μΑ |
| IL | Low-level input current | V _I = 0.4 V | | | | | - 250 | μΑ |
| los | Short-circuit output current | V _{CC} = 5 V | | | | -5 | - 30 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = 5.25 V,$ | All inputs at 2 V, | No load | | 9 | 14 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 V,$ | All inputs at 0.8 V, | No load | | 13 | 30 | mA |

NOTE 3. The output voltage and current limits are ensured for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|---|---|-----|------------------|-----|------|
| tpLH Propagation delay time, low-to-high-level output | D. 50.0 C. 15.55 See Figure 1 | | 4 | 14 | ns |
| tphL Propagation delay time, high-to-low-level output | $R_L = 50 \Omega$, $C_L = 15 pF$, See Figure 1 | | 5 | 14 | ns |
| tpLH Propagation delay time, low-to-high-level output | $R_L = 50 \Omega$, $C_L = 100 pF$, See Figure 1 | | 8 | 20 | ns |
| tpHL Propagation delay time, high-to-low-level output | | | 8 | 20 | ns |

[†]All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25 \text{ °C}$.

PARAMETER MEASUREMENT INFORMATION

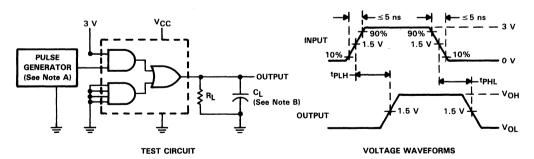


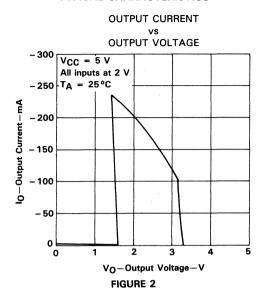
FIGURE 1. SWITCHING TIMES

NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \ \Omega$, $t_w = 200 \ ns$, duty cycle = 50%.

B. C_L includes probe and jig capacitance.



TYPICAL CHARACTERISTICS



SN75ALS125, SN75ALS127 SEVEN-CHANNEL LINE RECEIVERS

D2239, APRIL 1987-REVISED AUGUST 1989

Meets IBM 360/370 I/O Specification

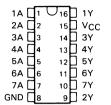
- Input Resistance . . . 7 k Ω to 20 k Ω
- Output Compatible with TTL
- IMPACT™ Low-Power Schottky Technology
- Operates from Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low
- Glitch-Free Power-Up and Power-Down
- Seven Channels in One 16-Pin Package
- Standard V_{CC} and Ground Positioning on SN75ALS127

description

The SN75ALS125 and SN75ALS127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Employing the IMPACT™ process allows low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

The SN75ALS125 and SN75ALS127 are characterized for operation from 0 °C to 70 °C.

SN75ALS125 . . . D, J, OR N PACKAGE (TOP VIEW)



SN75ALS127 . . . D, J, OR N PACKAGE (TOP VIEW)

| 1A [| 1 | U ₁₆ | Vcc |
|-------|---|-----------------|-----|
| 2A 🗌 | 2 | 15 | 1Y |
| за 🗌 | 3 | 14 | 2Y |
| 4A 🗀 | 4 | 13 | 3Y |
| 5A 🗌 | 5 | 12 | 4Y |
| 6A 🗌 | 6 | 11 | 5Y |
| 7A 🗌 | 7 | 10 | 6Y |
| GND [| 8 | 9 | 7Y |

logic symbols†

SN75ALS125 1<u>6</u> 1Y D 9_ 2Y 2 14_ 3Y ЗА 13 4 **4**Y 12 5 5Y 5A 6 11 6Y 6A 10 77

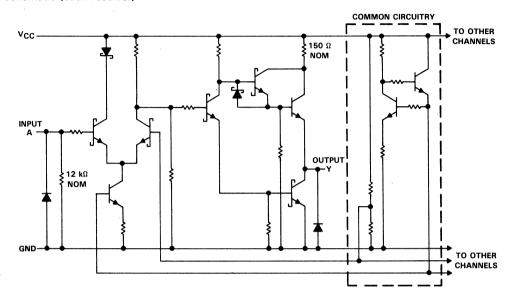
15 1Y D 2 14 2Δ 3 13 34 37 12 **4**Y 4Α 5 11 5Α 5Y 6 10 6Y 6A 9 **7**Y

SN75ALS127

IMPACT is a trademark of Texas Instruments Incorporated

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|---|
| Input voltage range |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| D package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above $25\,^{\circ}\text{C}$ free-air temperature, derate the D package to 608 mW at $70\,^{\circ}\text{C}$ at the rate of $7.6\,$ mW/ $^{\circ}\text{C}$, the J package to 656 mW/°C at 70 °C at the rate of 8.2 mW/°C, and the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-----|-----|------|------|
| Supply voltage, VCC | 4.5 | 5 | 5.5 | ٧ |
| High-level input voltage, VIH | 1.7 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.7 | V |
| High-level output current, IOH | | | -0.4 | V |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

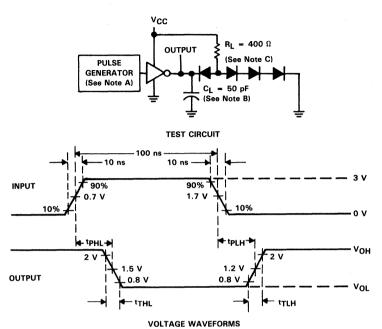
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-----------|---|---|---------------------------|-----|------------------|------|------|
| Voн | High-level output voltage | $V_{CC} = 4.5 \text{ V}, V_{IL} = 0.7 \text{ V},$ | I _{OH} = -0.4 mA | 2.4 | 3.1 | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = 4.5 \text{ V}, V_{IH} = 1.7 \text{ V},$ | I _{OL} = 16 mA | | 0.4 | 0.5 | V |
| ΊΗ | High-level input current | V _{CC} = 5.5 V, V _I = 3.11 V | | | 0.3 | 0.42 | mA |
| liL | Low-level input current | $V_{CC} = 5.5 \text{ V}, V_{I} = 0.15 \text{ V}$ | | | | 30 | μΑ |
| los | Short-circuit output current [‡] | $V_{CC} = 5.5 \text{ V}, V_{O} = 0$ | | -18 | | - 60 | mA |
| rį | Input resistance | $V_{CC} = 4.5 \text{ V}, 0, \text{ or open},$ $\Delta V_{I} = 0.15 \text{ V to } 4.15 \text{ V}$ | | 7 | | 20 | kΩ |
| 1 | Complete | $V_{CC} = 5.5 \text{ V}, I_{OH} = -0.4 \text{ mA},$ All inputs at 0.7 V | | | 15 | 25 | mA |
| lcc | Supply current | V _{CC} = 5.5 V, I _{OL} = 16 mA, All inputs at 4 V | | | 28 | 47 | mA |

switching characteristics over recommended operating temperature range (unless otherwise noted), VCC = 5 V

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | 7 | 14 | 25 | ns |
| tPHL | Propagation delay time, high-to-low-level output | | 10 | 18 | 30 | ns |
| tPLH tPHL | Ratio of propagation delay times | $R_L = 400 \Omega$, $C_L = 50 pF$, See Figure 1 | 0.5 | 0.8 | 1.3 | |
| tTLH | Transition time, low-to-high-level output | | 1 | 7 | 12 | ns |
| ^t THL | Transition time, high-to-low-level output | | 1 | 3 | 12 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Not more than one output should be shorted at a time.



NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50 \ \Omega$, PRR $\leq 5 \ MHz$.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

FIGURE 1

SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2525, JUNE 1986-REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

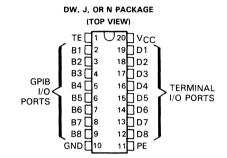
- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN75ALS160 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky designed device for two-way communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS160 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.



FUNCTION TABLES

EACH DRIVER

EACH RECEIVER

| 11 | NPUT | OUTPUT | |
|----|------|--------|----------------|
| D | TE | PE | В |
| Н | Н | Н | Н |
| L | Н | Х | L |
| н | Х | L | z.† |
| Х | L | Х | Z [†] |

| INPUTS | | | OUTPUT | | |
|--------|----|----|--------|--|--|
| В | TE | PE | D | | |
| L | L | Х | L | | |
| Н | L | Х | н | | |
| Х | Н | X | Z | | |

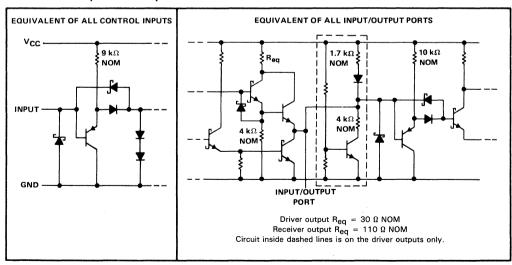
H = high level, L = low level, X = irrelevant,

Z = high-impedance state.

[†] This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

logic diagram (positive logic) logic symbol† PE (11) M1 [3S] M2 [0C] TE (1) EN3 [XMT] D1 (19) EN4 [RCV] (<u>2)</u> B1 (<u>2)</u> B1 3 (1 ▽/2 ☆ D2 (18) (18)(3) B2 **B2** (<u>4)</u> B3 D3 (17) (5) (6) (<u>4)</u> B3 D5 (7) D4 (16) (8) (5) - 84 TERMINAL GPIB D5 (15) 1/0 [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and (6) B5 PORTS IEC Publication 617-12. □ Designates 3-state outputs. D6 —(14) ◆ Designates passive-pullup outputs. (7<u>)</u> B6 D7 (13) (8)₋ B7 D8 —(12)

schematics of inputs and outputs



(9)

SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

| absolute maximum ratings over operating free-air temperature range (unless otherwise noted) |
|---|
| Supply voltage, VCC (see Note 1) |
| Input voltage |
| Low-level driver output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| DW package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260°C |
| NOTES: 1. All voltage values are with respect to network ground terminal. |
| 2. For operation above 25 °C free-air temperature, derate the DW and J packages to 656 mW at 70 °C at the rate of 8.2 mW/°C |

and derate the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, VIL | | | | 0.8 | V |
| Illustration of the second sec | Bus ports with pullups active | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| I | Bus ports | | | 48 | |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | TYP [†] | MAX | UNIT | |
|-----------------------|--|-----------|--|---|------|------------------|-------------|--------|--|
| VIK | Input clamp voltage | | I _I = -18 mA | | | -0.8 | - 1.5 | V | |
| V _{hys} | Hysteresis (V _{T +} - V _{T -}) | Bus | | | 0.4 | 0.65 | | ٧ | |
| V _{OH} ‡ | High-level | Terminal | $I_{OH} = -800 \mu$ | A, TE at 0.8 V | 2.7 | 3.5 | | v | |
| voH. | output voltage | Bus | $I_{OH} = -5.2 \text{ m}$ | nA, PE and TE at 2 V | 2.5 | 3.3 | | l v | |
| Voi | Low-level | Terminal | $I_{OL} = 16 \text{ mA},$ | TE at 0.8 V | | 0.3 | 0.5 | v | |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA},$ | TE at 2 V | | 0.35 | 0.5 | \ \ \ | |
| l _l | Input current at maximum input voltage | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ | |
| 1н | High-level input current | Terminal, | $V_I = 2.7 V$ | | | 0.1 | 20 | μΑ | |
| IIL . | Low-level input current | PE, or TE | $V_1 = 0.5 V$ | | | - 10 | - 100 | μΑ | |
| V _{I/O(bus)} | Voltage at bus port | | Driver disabled II(bus) = 0 | | 2.5 | 3.0 | 3.7 | v | |
| VI/O(bus) | Voltage at bus port | | Dilver disabled | $I_{I(bus)} = -12 \text{ mA}$ | | | - 1.5 | • | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | | |
| | | | | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | | |
| I _{I/O(bus)} | Current into bus port | Power on | Driver disabled | V _{I(bus)} = 2.5 V to 3.7 V | | | 2.5 -3.2 | mA | |
| | | | | V _{I(bus)} = 3.7 V to 5 V | 0 | | 2.5 | 2.5 | |
| | | | | $V_{I(bus)} = 5 V \text{ to } 5.5 V$ | 0.7 | | 2.5 |] | |
| | | Power off | $V_{CC} = 0$, | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | 40 | μΑ | |
| laa | Short-circuit | Terminal | | | - 15 | -35 | - 75 | mA | |
| los | output current | Bus | | | - 25 | - 50 | -125 | I IIIA | |
| loo | ICC Supply current | | No load | Ferminal outputs low and enabled | | 42 | 65 | mA | |
| ICC | опррту силент | | INO IOAU E | Bus outputs low and enabled | | 52 | 80 | | |
| C _{i/o(bus)} | Bus-port capacitance | | $V_{CC} = 5 \text{ V to } 0$, $V_{I/O} = 0 \text{ to } 2 \text{ V}$, $f = 1 \text{ MHz}$ | | | 30 | | pF | |

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies to 3-state outputs only.

SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), VCC = 5 V

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|----------|----------|------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | | _ | C _I = 30 pF, | | 7 | 20 | |
| tPHL | Propagation delay time, high-to-low-level output | Terminal | Bus | See Figure 1 | | 8 | 20 | ns |
| tPLH | Propagation delay time, low-to-high-level output | _ | <u>.</u> | C _L = 30 pF, | | 7 | 14 | |
| tPHL | Propagation delay time, high-to-low-level output | Bus | Terminal | See Figure 2 | | 9 | 14 | ns |
| tPZH | Output enable time to high level | | TE Bus | | | 19 | 30 | 0 |
| tPHZ | Output disable time from high level | T | | C _L ≈ 15 pF, | | 5 | 12 | |
| tPZL | Output enable time to low level |) 'E | | See Figure 3 | | 16 | 35 | ns |
| tPLZ | Output disable time from low level | | | | | 9 | 20 | |
| ^t PZH | Output enable time to high level | | | | | 13 | 30 | |
| tPHZ | Output disable time from high level | TE | T | $C_L \approx 15 \text{ pF},$ | | 12 | 20 | |
| tPZL | Output enable time to low level | } '= | Terminal | See Figure 4 | | 12 | 20 | ns |
| tPLZ | Output disable time from low level |] | | | | 11 | 20 | |
| t _{en} | Output pull-up enable time | PE | Bus | C _L = 15 pF, | | 11 | 22 | ne |
| tdis | Output pull-up disable time | FE | bus | See Figure 5 | | 6 | 12 | ns |

 $^{^{\}dagger}$ Typical values are at $T_A = 25$ °C.

PARAMETER MEASUREMENT INFORMATION

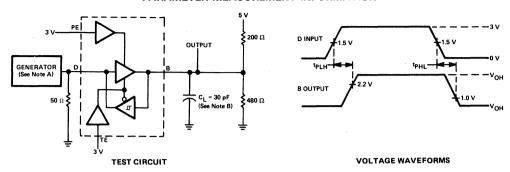


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

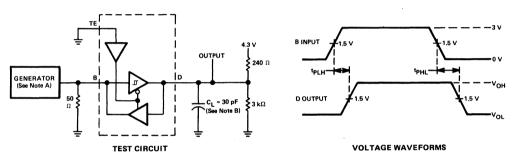


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

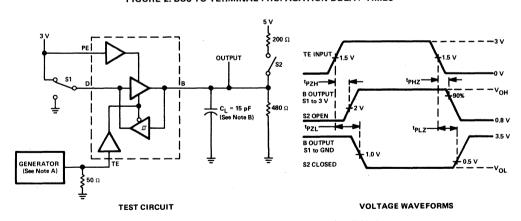


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} =$ 50 Ω .
 - B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

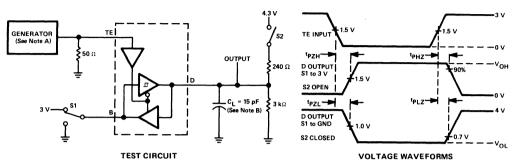


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

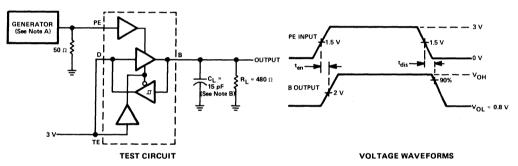
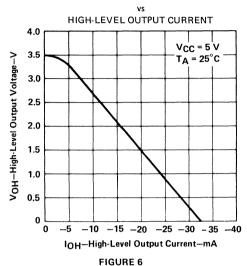


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

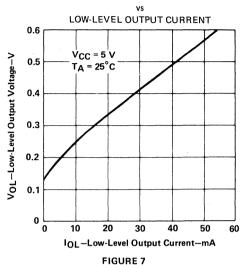
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.

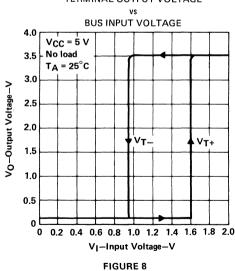
TERMINAL HIGH-LEVEL OUTPUT VOLTAGE

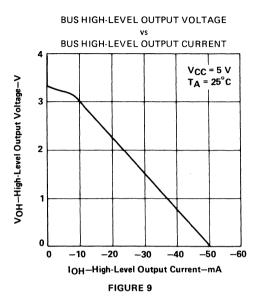


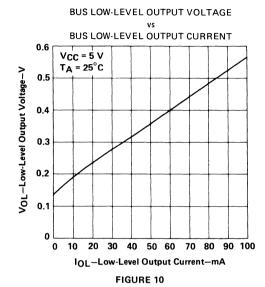
TERMINAL LOW-LEVEL OUTPUT VOLTAGE

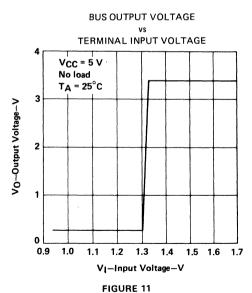


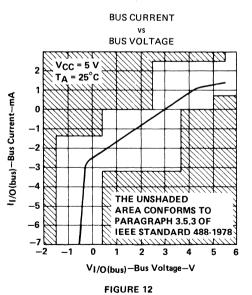
TERMINAL OUTPUT VOLTAGE











SN75ALS161 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2618, JUNE 1986-REVISED AUGUST 1989

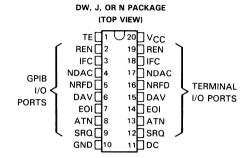
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- **Bus-Terminating Resistors Provided on Driver Outputs**
- No Loading of Bus When Device Is Powered Down (VCC = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN75ALS161 eight-channel generalpurpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the busmanagement and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS161 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.



CHANNEL IDENTIFICATION TABLE

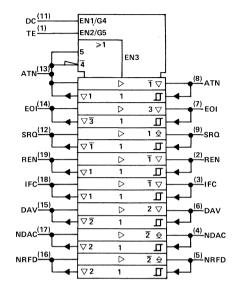
| NAME | IDENTITY | CLASS |
|------|--------------------|------------|
| DC | Direction Control | Control |
| TE | Talk Enable | Control |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | Management |
| IFC | Interface Clear | |
| EOI | End or Identify | |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | Hallster |

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when VCC = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS161 is manufactured in a 20-pin package and is characterized for operation from 0 °C to 70 °C.

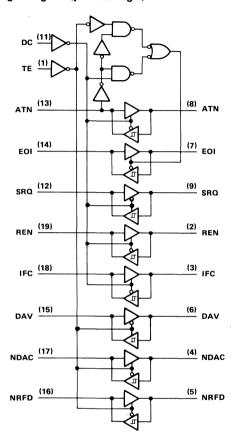
INSTRUMENTS

logic symbol†



- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- □ Designates 3-state outputs.
- → Designates passive-pullup outputs.

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

| CONTROLS | | | BU | JS-MANA | GEMENT | CHANNE | _S | DATA-TRANSFER CHANNI | | |
|----------|----|------------------|------------------|--|--------|--------|----|----------------------|------|---------------|
| DC | TE | ATN [‡] | ATN [‡] | ATN [‡] SRQ REN IFC EOI (Controlled by DC) | | | | | NDAC | NRFD y TE) |
| Н | Н | Н | | - | | | Т | _ | _ | _ |
| Н | Н | L | " | R T R | R | R | | . R | R | |
| L | L | Н | | | - | - | R | | _ | _ |
| L | L | L |]_' | R | 1 | 1 | Т | R | | |
| Н | L | Х | R | Т | R | R | R | R | Т | Т |
| L | Н | X | T | R | Т | Т | Т | Т | R | R |

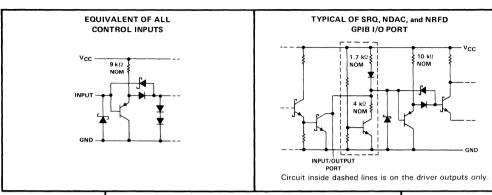
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

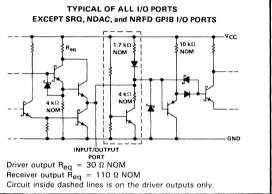
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[‡]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Low-level driver output current |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): |
| DW package |
| J package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260 °C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the DW and J packages to 656 mW at 70 °C at the rate of 8.2 mW/°C, and derate the N package to 736 mW at 70 °C at the rate of 9.2 mW/°C.



recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|-------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| ligh-level input voltage, V _{IH} ow-level input voltage, V _{IL} ligh-level output current, I _{OH} ow-level output current, I _{OL} | Bus ports with pullups active | | | -5.2 | mA |
| | Terminal ports | | | -800 | μΑ |
| Law level autout avenue la | Bus ports | | | 48 | ^ |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CO | NDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------------|---|-------------------|---|---|------|------------------|----------------------|------|
| V _{IK} | Input clamp voltage | | I _I = -18 mA | | | -0.8 | - 1.5 | ٧ |
| V_{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | | | 0.4 | 0.65 | | ٧ |
| Vон [‡] | High-level | Terminal | $I_{OH} = -800 \mu A$ | | 2.7 | 3.5 | | v |
| vOH. | output voltage | Bus | IOH = -5.2 mA | | 2.5 | 3.3 | | ľ |
| Voi | Low-level | Terminal | I _{OL} = 16 mA | | | 0.3 | 0.5 | V |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA}$ | | | 0.35 | 0.5 | |
| lj | Input current at maximum input voltage | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ |
| ΊΗ | High-level | Terminal and | V _I = 2.7 V | - | | 0.1 | 20 | μΑ |
| IIL | Low-level input current | control inputs | V _I = 0.5 V | | | - 10 | - 100 | μΑ |
| V _{I/O(bus)} | Voltage at bus port | <u> </u> | Driver disabled | $I_{l(bus)} = 0$ $I_{l(bus)} = -12 \text{ mA}$ | 2.5 | 3.0 | 3.7 -1.5 | ٧ |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | |
| II/O(bus) | Current into bus port | Power on | Driver disabled | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ $V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$ | 0 | | -3.2 +2.5 -3.2 | mA |
| 1/O(bus) | Surront into bus port | Towar on | Direct disabled | $V_{l(bus)} = 3.7 \text{ V to 5 V}$ $V_{l(bus)} = 5 \text{ V to 5.5 V}$ | 0.7 | | 2.5 | |
| | | Power off | $V_{CC} = 0$, | V _{I(bus)} = 0 to 2.5 V | | | 40 | μA |
| 1 | Short-circuit | Terminal | | | - 15 | - 35 | - 75 | mA |
| los | output current | Bus | | | - 25 | - 50 | - 125 | |
| Icc | Supply current | | No load, | TE and DC low | | 55 | 75 | mA |
| C _{i/o(bus)} | Bus-port capacitance | | $V_{CC} = 5 \text{ V to 0}$ $V_{UQ} = 0 \text{ to 2 V}$ | | | 30 | | рF |

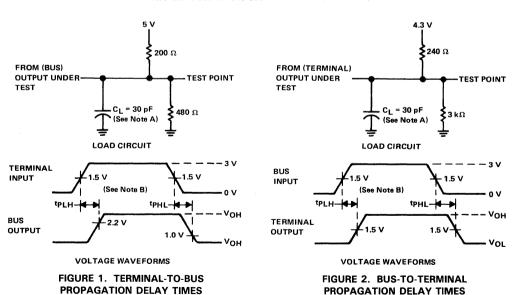
 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies to 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN TYP [†] | MAX | UNIT |
|------------------|--|----------|-----------------------|-------------------------|----------------------|----------|------|
| tPLH | Propagation delay time, low-to-high-level output | TiI | Bus | C _L = 30 pF, | 10 | 20 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | Terminal | Bus | See Figure 1 | 12 | 20 | |
| tPLH | Propagation delay time, low-to-high-level output | D | T | C _L = 30 pF, | 5 | 10 | |
| tPHL | Propagation delay time, high-to-low-level output | Bus | Terminal | See Figure 2 | 7 | 14 | ns |
| tPZH tPHZ | Output enable time to high level Output disable time from high level | TE or DC | BUS (ATTN, EOI, | C _L = 15 pF, | | 30 20 | ns |
| tPZL tPLZ | Output enable time to low level Output disable time from low level | 12 01 50 | REN, IFC, and DAV) | See Figure 3 | | 45 20 | 113 |
| tPZH tPHZ | Output enable time to high level Output disable time from high level | TE or DC | Terminal | C _L = 15 pF, | | 30 25 | ns |
| tPZL tPLZ | Output enable time to low level Output disable time from low level | | | See Figure 4 | | 30 25 | |

[†]All typical values are at T_A = 25 °C.

PARAMETER MEASUREMENT INFORMATION

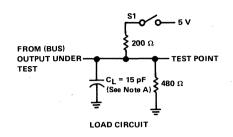


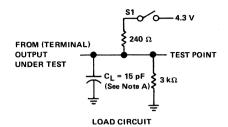
NOTES: A. CL includes probe and jig capacitance.

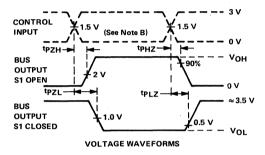
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} = 50 \Omega$.



PARAMETER MEASUREMENT INFORMATION







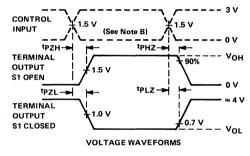


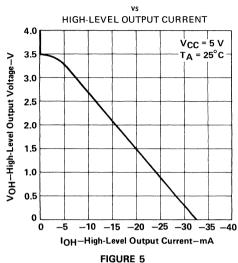
FIGURE 3. BUS ENABLE AND DISABLE TIMES

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} = 50 \Omega$.

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE



TERMINAL LOW-LEVEL OUTPUT VOLTAGE

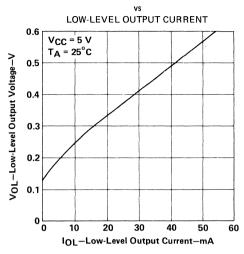
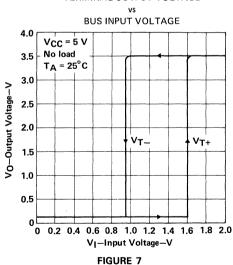
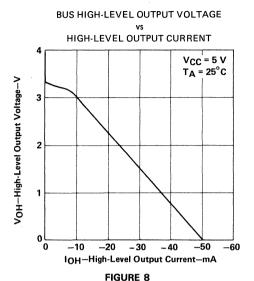
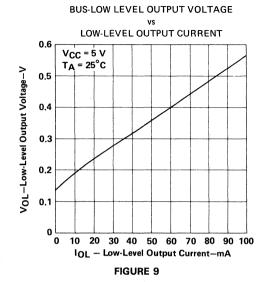


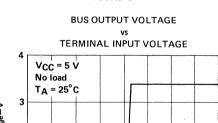
FIGURE 6

TERMINAL OUTPUT VOLTAGE









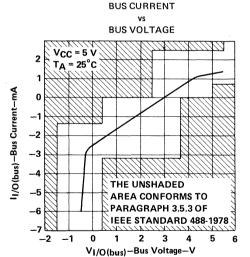


FIGURE 11

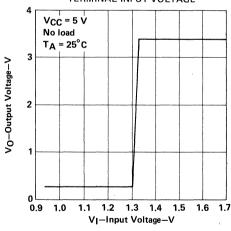


FIGURE 10

SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2618, JUNE 1986-REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

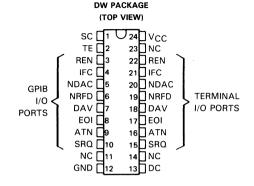
The SN75ALS162 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

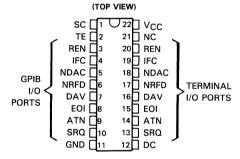
The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration

to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC} = 0$. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

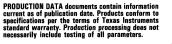
The SN75ALS162 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.





N PACKAGE

NC-No internal connection.

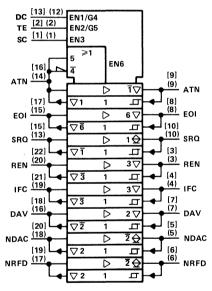




CHANNEL IDENTIFICATION TABLE

| NAME | IDENTITY | CLASS |
|------|--------------------|------------|
| DC | Direction Control | |
| TE | Talk Enable | Control |
| sc | System Control | |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | Management |
| IFC | Interface Clear | |
| EOI | End or Identify | |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | rranster |

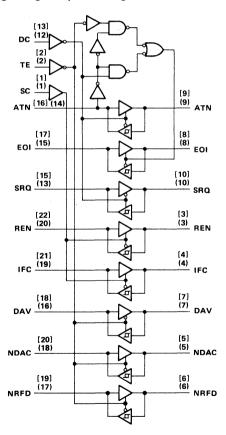
logic symbol†



 $^{\dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

- ▼ Designates 3-state outputs.
- ◆ Designates passive-pullup outputs.

logic diagram (positive logic)



- [] Denotes pin numbers for DW package.
- () Denotes pin numbers for N package.



RECEIVE/TRANSMIT FUNCTION TABLE

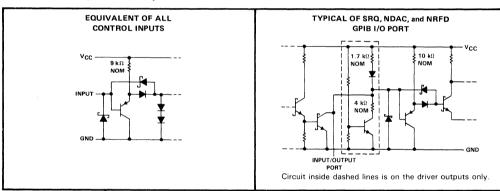
| | CONTROLS | | | | BUS-MANAGEMENT CHANNELS | | | | DATA-TRANSFER CHANNELS | | | |
|----|----------|----|------|------------------|-------------------------|------------|-----------|-----|------------------------|-------------|------|--|
| sc | DC | TE | ATN† | ATN [†] | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD | |
| | 1 | | | (Controlle | d by DC) | (Controlle | ed by SC) | | (Co | ntrolled by | TE) | |
| | Н | Н | Н | | | | | T | - | R | _ | |
| | Н | Н | L | 1 " | R T | | | R | ' | n | R | |
| | L | L | Н | | R | | | R | R | т | _ | |
| | Ļ | L | L | l' | n | | | T | n | ' I | | |
| | Н | L | Х | R | Т | | | R | R | Т | T | |
| | L | Н | X | Т | R | | | Т | Т | R | R | |
| Н | | | | | | Т | Т | | | | | |
| L | | | | | | R | R | | | | | |

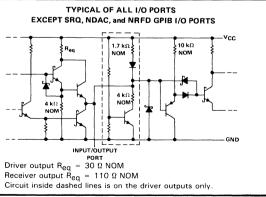
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs





SN75ALS162 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) 7 V Input voltage 5.5 V |
|--|
| Low-level driver output current |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): |
| DW package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260°C |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate the DW package to 864 mW at 70 °C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70 °C at the rate of 13.6 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|--------------------------------|------|-----|------|------|
| Supply voltage, VCC | | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, V _{IH} | | 2 | | | . V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| III b level of the second level | Bus ports with 3-state outputs | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| Law laws autout automat Law | Bus ports | | | 48 | - A |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| Operating free-air temperature, TA | | | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CO | NDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------------|---|-----------------|--|---|------|------------------|----------------|--------|
| VIK | Input clamp voltage | | I _I = -18 mA | | | -0.8 | - 1.5 | ٧ |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | | | 0.4 | 0.65 | | V |
| ., t | High-level | Terminal | $I_{OH} = -800 \mu A$ | | 2.7 | 3.5 | | ,, |
| V _{OH} ‡ | output voltage | Bus | I _{OH} = -5.2 mA | | 2.5 | 3.3 | | ٧ |
| 17 | Low-level | Terminal | I _{OL} = 16 mA | | | 0.3 | 0.5 | v |
| v_{OL} | output voltage | Bus | I _{OL} = 48 mA | | | 0.35 | 0.5 | 1 ° |
| l _l | Input current at maximum input voltage | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ |
| ΊΗ | High-level input current | Terminal and | V _I = 2.7 V | | | 0.1 | 20 | μΑ |
| 1 | Low-level | control | VI = 0.5 V | | | 10 | - 100 | μА |
| ΙΙL | input current | inputs | V = 0.5 V | | | - 10 | - 100 | μΑ |
| V _{I/O(bus)} | Voltage at bus port | | Driver disabled | I _{I(bus)} = 0 | 2.5 | 3.0 | 3.7 - 1.5 | V |
| | | | | I _{I(bus)} = -12 mA | 4.0 | | - 1.5 | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | ļ |
| | | | | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | - 3.2 | 1 |
| I/O(bus) | Current into bus port | Power on | Driver disabled | $V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$ | | | + 2.5 - 3.2 | mA |
| | | | | V _{I(bus)} = 3.7 V to 5 V | 0 | | 2.5 | |
| | | | | $V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$ | 0.7 | | 2.5 | |
| | | Power off | $V_{CC} = 0$, | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | - 40 | μΑ |
| 1 | Short-circuit | Terminal | | | - 15 | -35 | - 75 | mA |
| los | output current | Bus | | | - 25 | - 50 | - 125 | 1 IIIA |
| Icc | Supply current | | No load, | TE, DC, and SC low | | 55 | 75 | mA |
| C _{i/o(bus)} | Bus-port capacitance | | $V_{CC} = 5 \text{ V to } 0$, $V_{I/O} = 0 \text{ to } 2 \text{ V}$, | | | 30 | | pF |

 $^{^{\}dagger}All$ typical values are at VCC = 5 V, TA = 25 °C. $^{\ddagger}V_{OH}$ applies for 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN TYP [†] | мах | UNIT |
|------------------------------|---|---------------------|---|---|----------------------|----------------------|------|
| [†] PLH | Propagation delay time, low-to-high-level output | Terminal | Bus | C _L = 30 pF, | 10 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Terrima | Dus | See Figure 1 | 12 | 20 | |
| tPLH | Propagation delay time, low-to-high-level output | Pue | Torminal | C _L = 30 pF, | 5 | 10 | |
| tPHL | Propagation delay time, high-to-low-level output | Bus | Terminal | See Figure 2 | 7 | 14 | ns |
| tPZH tPHZ tPZL tPLZ | Output enable time to high level Output disable time from high level Output enable time to low level Output disable time from low level | TE, DC, or SC | BUS (ATTN, EOI, REN, IFC, and DAV) | C _L = 15 pF, See Figure 3 | | 30 20 45 20 | ns |
| tPZH tPHZ tPZL tPLZ | Output enable time to high level Output disable time from high level Output enable time to low level Output disable time from low level | TE, DC, or SC | Terminal | C _L = 15 pF, See Figure 4 | | 30 25 30 25 | ns |

 $^{^{\}dagger}$ All typical values are at $T_{A} = 25 \, ^{\circ}$ C.

PARAMETER MEASUREMENT INFORMATION

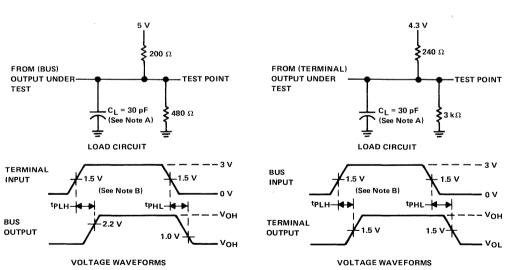


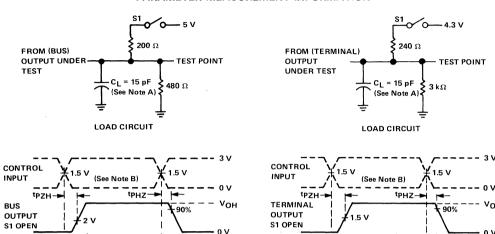
FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} = 50 \Omega$.

PARAMETER MEASUREMENT INFORMATION



≈ 3.5 V

VOL

0.5 V

VOLTAGE WAVEFORMS

FIGURE 3. BUS ENABLE AND
DISABLE TIMES

tPLZ-

FIGURE 4. TERMINAL ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS

tPLZ-➤

0.7 V

· VOL

NOTES: A. C_L includes probe and jig capacitance.

tPZL-

BUS

OUTPUT

S1 CLOSED

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{f} \leq$ 6 ns, $t_{f} \leq$ 6 ns, $t_{Out} = 50~\Omega$.

tPZL -

TERMINAL

S1 CLOSED

OUTPUT

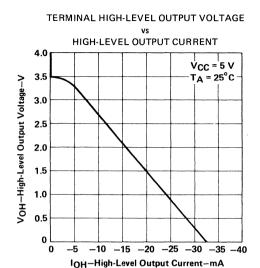
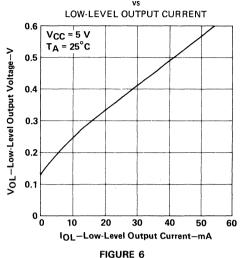
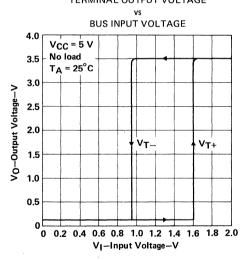


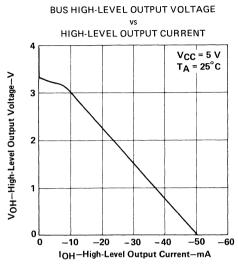
FIGURE 5

TERMINAL LOW-LEVEL OUTPUT VOLTAGE



TERMINAL OUTPUT VOLTAGE





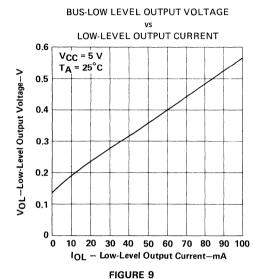
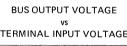
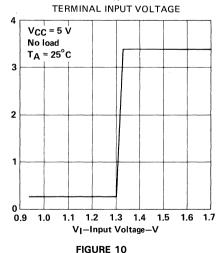


FIGURE 8





Vo-Output Voltage-V

BUS CURRENT

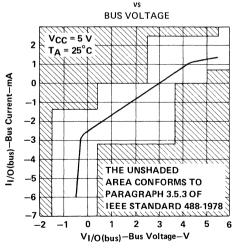


FIGURE 11

SN75ALS163 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2611, JUNE 1986-REVISED SEPTEMBER 1989

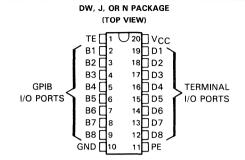
- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, highspeed. Advanced Low-Power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $V_{CC} = 0$.

The SN75ALS163 is characterized for operation from 0°C to 70°C.



FUNCTION TABLES

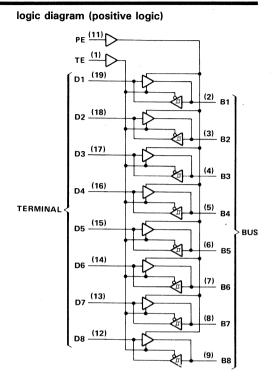
| | EAC | H DRI | VER | EACH RECEIVER | | | |
|---|--------|-------|--------|---------------|-------|----|--------|
| | INPUTS | 3 | OUTPUT | | INPUT | 3 | OUTPUT |
| D | TE | PE | В | В | TE | PE | D |
| Н | Н | Н | Н | L | L | Х | L |
| L | Н | Х | L | Н | L | X | н |
| Н | Х | L | z | X | Н | X | z |
| X | L | X | Z | | | | |

H = high level, L = low level, X = irrelevant, Z = High-impedance state

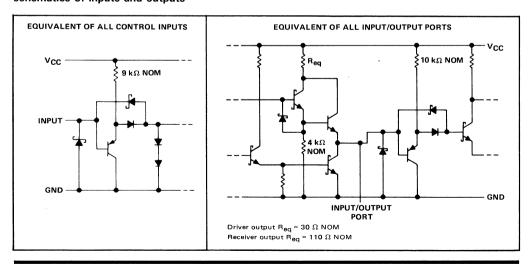
SN75ALS163 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

logic symbol† PE (11) M1 [3S] M2 [0C] EN3 [XMT] EN4 [RCV] D1 (19) ٥ (<u>2)</u> B1 3 (1 ▽/2 🗘 D2 (18) (<u>3)</u> B2 (<u>4)</u> B3 (5) (16)В4 (6) (15)D5 D6 (14) (7) В6 (8)

- † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇ Designates 3-state outputs.



schematics of inputs and outputs



SN75ALS163 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

| absolute maximum ratings over operating free-air temperature range (unless otherwise noted) |
|---|
| Supply voltage, VCC (see Note 1) |
| Input voltage |
| Low-level driver output current |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package 300 °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package 260 °C |

NOTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR | TA = 70°C POWER RATING |
|---------|---------------------------------------|--------------------|---------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW |
| J | 1025 mW | 8.2 mW/°C | 656 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| High level autout august 1 | Bus ports with pullups active | | | -5.2 | mA |
| High-level output current, IOH | Terminal ports | | | -800 | μΑ |
| 1 1 1 1 | Bus ports | | | 48 | 4 |
| Low-level output current, IOL | Terminal ports | | | 16 | mA |
| Operating free-air temperature range, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | | TEST | CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|----------------------|---|------------|-------------------------------------|-------|------------------------------|------|------------------|-------------|------|
| VIK | Input clamp voltage | | I _I = -18 mA | | | | -0.8 | - 1.5 | ٧ |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | Bus | | | | 0.4 | 0.65 | | ٧ |
| V _{OH} ‡ | High-level | Terminal | $I_{CH} = -800$ | μА, | TE at 0.8 V | 2.7 | 3.5 | | V |
| vOH. | output voltage | Bus | $I_{OH} = -5.2$ | mΑ, | PE and TE at 2 V | 2.5 | 3.3 | | · · |
| Val | Low-level | Terminal | I _{OL} = 16 mA | ١, | TE at 0.8 V | | 0.3 | 0.5 | V |
| VOL | output voltage | Bus | $I_{OL} = 48 \text{ mA}$ | ١, | TE at 2 V | | 0.35 | 0.5 | · · |
| lau | High-level output current | Bus | $V_0 = 5.5 V$, | | PE at 0.8 V, | | | 100 | ^ |
| Іон | (open-collector mode) | bus | D and TE at 2 | 2 V | | 1 | | 100 | μΑ |
| 1 | Off-state output current | Bus | PE at 2 V, | | V _O = 2.7 V | | | 20 | μΑ |
| loz | (3-state mode) | bus | TE at 0.8 V | | $V_0 = 0.5 V$ | | | - 100 | μΑ |
| 1. | Input current at | Terminal | V _I = 5.5 V | | | | 0.2 | 100 | μΑ |
| 11 | maximum input voltage | Terrifical | V = 5.5 V | | | | 0.2 | 100 | μΑ |
| ΙН | High-level input current | Terminal, | $V_{ } = 2.7 V$ | | | | 0.1 | 20 | μΑ |
| կլ | Low-level input current | PE, or TE | $V_1 = 0.5 V$ | | | | -10 | - 100 | μΑ |
| | Short-circuit | Terminal | | | | - 15 | -35 | - 75 | mA |
| los | output current | Bus | | | - 25 | - 50 | - 125 | mA | |
| 1 | Complex accurant | | No lood | Term | inal outputs low and enabled | | 42 | 65 | mA |
| lcc | Supply current | | No load Bus outputs low and enabled | | | 52 | 80 | IIIA | |
| C _{i/o(bus} | Bus-port capacitance | | V _{CC} = 5 V o | or O, | $V_{I/O} = 0$ to 2 V, | | 30 | | рF |

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 V$

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP§ | MAX | UNIT |
|------------------|---|----------|----------|--------------------------|-----|------|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | T | | C _L = 30 pF, | | 7 | 20 | _ |
| ^t PHL | Propagation delay time, high-to-low-level output | Terminal | Bus | See Figure 1 | | 8 | 20 | ns |
| ^t PLH | Propagation delay time, low-to-high-level output | Bus | Terminal | C _L = 30 pF, | | 7 | 14 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | bus | remma | See Figure 2 | | 9 | 14 | 115 |
| ^t PZH | Output enable time to high level | | | | | 19 | 30 | |
| ^t PHZ | Output disable time from high level | TE | Bus | C _L = 15 pF, | | 5 | 12 | ns |
| ^t PZL | Output enable time to low level | ١. | TE Bus | See Figure 3 | | 16 | 35 | 113 |
| ^t PLZ | Output disable time from low level | | | | | 9 | 20 | |
| tPZH | Output enable time to high level | | | | | 13 | 30 | |
| ^t PHZ | Output disable time from high level | TE TE | T | $C_{L} = 15 \text{ pF},$ | | 12 | 20 | |
| tPZL | Output enable time to low level | '5 | Terminal | See Figure 4 | | 12 | 20 | ns |
| tPLZ | Output disable time from low level | | | | | 11 | 20 | |
| t _{en} | Output pull-up enable time | PE | Bus | C _L = 15 pF, | | 11 | 22 | |
| tdis | Output pull-up disable time |] PE | bus | See Figure 5 | | 6 | 12 | ns |

 $^{^{\}S}$ All typical values are at $T_A = 25\,^{\circ}$ C.

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. ‡ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

PARAMETER MEASUREMENT INFORMATION

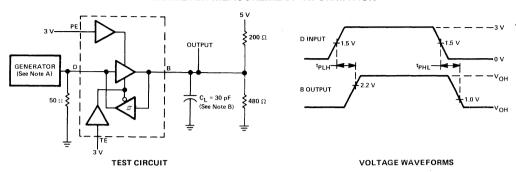


FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

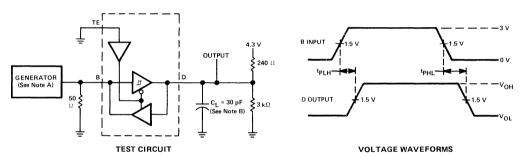


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

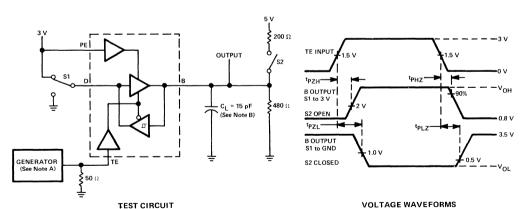


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{OUT} =$ 50 Ω .

B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

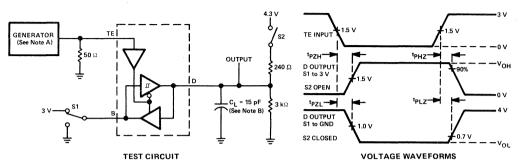


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

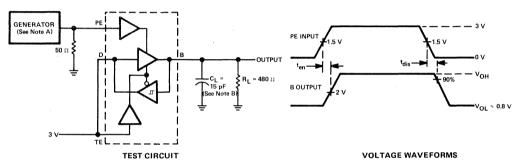
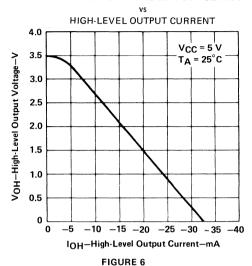


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

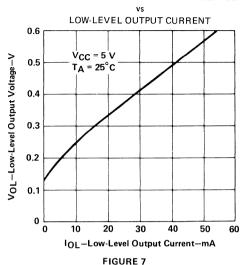
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_{out} =$ 50 Ω .

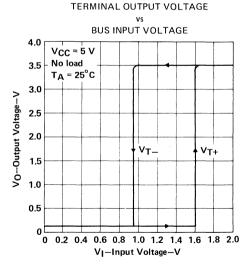
B. C_L includes probe and jig capacitance.

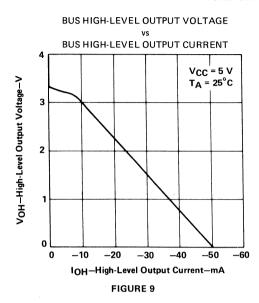
TERMINAL HIGH-LEVEL OUTPUT VOLTAGE

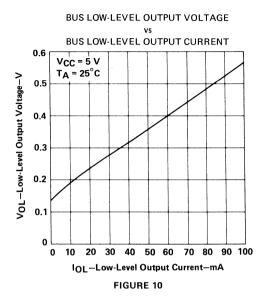


TERMINAL LOW-LEVEL OUTPUT VOLTAGE









BUS OUTPUT VOLTAGE

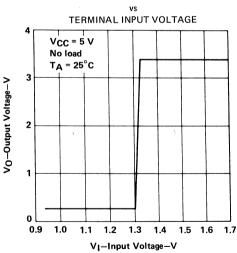


FIGURE 11

SN75ALS164 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

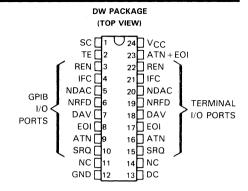
D2908 JUNE 1986-BEVISED AUGUST 1989

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Multicontrollers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (Vcc = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

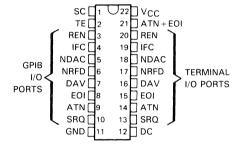
description

The SN75ALS164 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS164 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS164 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. All outputs are disabled (at a high-impedance state) during V_{CC} power-up and power-down transitions for glitch-free operation. The direction of data flow through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SN75ALS164 is identical to the SN75ALS162 with the addition of an OR gate to help simplify board layouts in several popular applications. The ATN and EOI signals are ORed to pin 21, which is a standard totem-pole output.



N DUAL-IN-LINE PACKAGE (TOP VIEW)



NC-No internal connection.

CHANNEL IDENTIFICATION TABLE

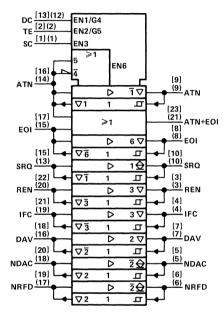
| NAME | IDENTITY | CLASS |
|-----------|--------------------|-------------|
| DC | Direction Control | |
| TE | Talk Enable | Control |
| SC | System Control | |
| ATN | Attention | |
| SRQ | Service Request | Bus |
| REN | Remote Enable | Management |
| IFC | Interface Clear | |
| EOI | End or Identify | |
| ATN + EOI | ATN logical OR EOI | Logic |
| DAV | Data Valid | Data |
| NDAC | Not Data Accepted | Transfer |
| NRFD | Not Ready for Data | i i alisiel |

Texas VI

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS164 is manufactured in a 22-pin dual-in-line N package and in 24-pin DW package, and is characterized for operation from 0°C to 70°C.

logic symbol†

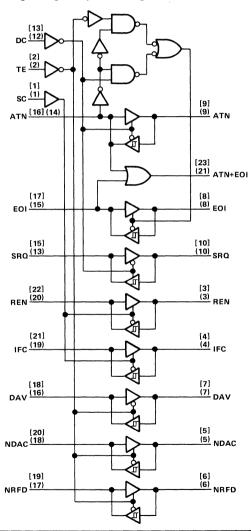


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

▽Designates 3-state outputs.

Designates passive-pullup outputs.

logic diagram (positive logic)



^[] Denotes pin numbers for DW package.

⁽⁾ Denotes pin numbers for N package.

RECEIVE/TRANSMIT FUNCTION TABLE

| CONTROLS | | | В | BUS-MANAGEMENT CHANNELS | | | | DATA-TRANSFER CHANNELS | | | |
|----------|----|----|------|-------------------------|----------|------------|-----------|------------------------|-----|-------------|-------|
| sc | DC | TE | ATN† | ATN [†] | SRQ | REN | IFC | EOI | DAV | NDAC | NRFD |
| | | | | (Controlle | d by DC) | (Controlle | ed by SC) | | (Co | ntrolled by | / TE) |
| | Н | Н | Н | R | _ | | | Т | _ | R | |
| | Н | Н | L | <u> </u> | ' | | | R | ' | n | R |
| | L | L | Н | | R | | | R | R | Т | т |
| | L | L | L | ' | | | | Т | | | ' |
| | Н | L | Х | R | Т | | | R | R | · T | Т |
| | L | Н | Х | Т | R | | | Т | Т | R | R |
| Н | | | | | | Т | Т | | | | |
| L | | | | | | R · | R | | | | |

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

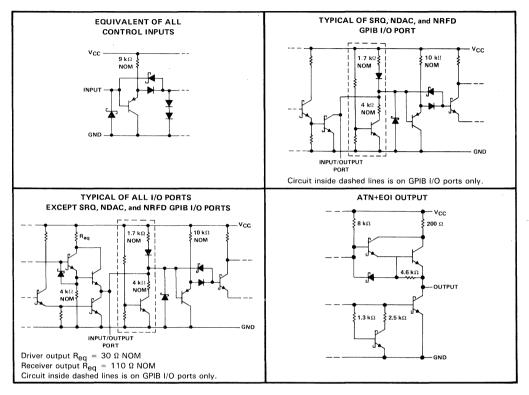
Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

[†]ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

ATN + EOI FUNCTION TABLE

| INPL | JTS | OUTPUT |
|------|-----|-----------|
| ATN | EOI | ATN + EOI |
| Н | Х | H |
| × | Н | н |
| L | L | L |

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) 7 V Input voltage 5.5 V |
|---|
| Low-level driver output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2): |
| DW package |
| N package |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds: DW or N package \ldots 260 °C |

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. For operation above 25 °C free-air temperature, derate the DW package to 864 mW at 70 °C at the rate of 10.8 mW/°C, and derate the N package to 1088 mW at 70 °C at the rate of 13.6 mW/°C.

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|--|--------------------------------|---|------|-----|------|------|
| Supply voltage, V _{CC} | | 4 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V _{IH} | • | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | | 0.8 | V |
| | Bus ports with 3-state outputs | | | | 5.25 | mA |
| High-level output current, IOH | Terminal ports | | | | -800 | _ |
| | ATN + EOI | | | | -400 | μΑ |
| 110000000000000000000000000000000000000 | Bus ports | | | | 48 | |
| Low-level output current, IOL | Terminal ports | | | | 16 | mA |
| | ATN + EOI | | | | 4 | 1 |
| Operating free-air temperature, T _A | | 0 | | 70 | °C | |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | | TEST CO | NDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------------------|--|------------|---------------------------------------|---|------|------------------|-------|------|
| VIK | Input clamp voltage | | I _I = -18 mA | | | -0.8 | -1.5 | V |
| V _{hys} | Hysteresis (V _{T+} - V _T) | Bus | | | 0.4 | 0.65 | | V |
| | | Terminal | I _{OH} = -800 μA | 1 | 2.7 | 3.5 | | |
| VoH [‡] | High-level output voltage | Bus | I _{OH} = -5.2 m/ | 4 | 2.5 | 3.3 | | V |
| | | ATN + EOI | !OH = 400 μA | 1 | 2.7 | | | |
| | | Terminal | IOL = 16 mA | | | 0.3 | 0.5 | |
| V_{OL} | Low-level output voltage | Bus | I _{OL} = 48 mA | | | 0.35 | 0.5 | V |
| | | ATN + EOI | IOL = 4 mA | | | | 0.4 | |
| 1. | Input current at | Terminal § | V _I = 5.5 V | | | 0.2 | 100 | |
| Ц | maximum input voltage | ATN, EOI | V _I = 5.5 V | | | | 200 | μΑ |
| | | Terminal | V _I = 2.7 V | | | 0.1 | 20 | |
| ΉΗ | High-level input current | control | VI - 2.7 V | | | 0.1 | 20 | μΑ |
| | | ATN, EOI | $V_1 = 2.7 \text{ V}$ | | | | 40 | |
| | | Terminal | V _I = 0.5 V | | | - 10 | - 100 | |
| ηL | Low-level input current | control | • | | | - 10 | - 100 | μΑ |
| | | ATN, EOI | .V _I = 0.5 V | | | | - 500 | |
| VI/O(bus) | Voltage at bus port | | Driver disabled | I _{I(bus)} = 0 | 2.5 | 3.0 | 3.7 | V |
| 1,0(000) | | | Direct disabled | $I_{l(bus)} = -12 \text{ mA}$ | | | - 1.5 | |
| | | | | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | |
| | | | | $V_{I(bus)} = 0.4 \text{ V to } 2.5 \text{ V}$ | 0 | | -3.2 | |
| II/O(bus) | Current into bus port | Power on | Driver disabled | $V_{I(bus)} = 2.5 \text{ V to } 3.7 \text{ V}$ | 1 | | +2.5 | mA |
| ·1/O(bus) | Sarrent into Bas port | 104401 011 | Dilver disabled | | | | -3.2 | |
| | | | | $V_{l(bus)} = 3.7 \text{ V to 5 V}$ | 0 | | 2.5 | |
| | | | | $V_{I(bus)} = 5 \text{ V to } 5.5 \text{ V}$ | 0.7 | | 2.5 | |
| | | Power off | $V_{CC} = 0$, | $V_{I(bus)} = 0 \text{ to } 2.5 \text{ V}$ | | | - 40 | μΑ |
| | | Terminal | | | - 15 | - 35 | - 75 | |
| los | Short-circuit output current | Bus | | | - 25 | - 50 | - 125 | mA |
| | | ATN + EOI | | | - 10 | | - 100 | |
| lcc | Supply current | | No load, | TE, DC, and SC low | | 55 | 75 | mA |
| C _{i/o(bus)} | Ci/o/bus) Bus-port capacitance | | $V_{CC} = 5 V \text{ to 0},$ | | | 30 | | |
| -1/0(bus) | | | $V_{I/O} = 0 \text{ to } 2 \text{ V}$ | , f = 1 MHz | | 00 | | pF |

 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C. ‡ VOH applies for 3-state outputs only. § Except ATN and EOI terminal pins.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), VCC = 5 V

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|------------------------------------|-------------|---|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | Terminal | Bus | C _L = 30 pF, | | 10 | 20 | ns |
| tPHL | Propagation delay time, high-to-low-level output | remina | Dus | See Figure 1 | | 12 | 20 | |
| tPLH | Propagation delay time low-to-high-level output | Bus | Terminal | C _L = 30 pF, | | 5 | 10 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | Dus | Terrima | See Figure 2 | | 7 | 14 | 115 |
| tPLH | Propagation delay time, low-to-high-level output | Terminal ATN or Terminal EOI | ATN + EOI | C _L = 15 pF, See Figure 3 | | 3.5 | 10 | ns |
| tPHL | Propagation delay time, high-to-low-level output | Terminal ATN or Terminal EOI | ATN + EOI | C _L = 15 pF, See Figure 3 | | 7 | 15 | ns |
| tPZH | Output enable time to high level | TE, DC, | BUS | | | | 30 | |
| tPHZ | Output disable time from high level | or | (ATTN, EOI, | $C_L = 15 pF$, | | | 20 | ns |
| tPZL | Output enable time to low level | sc | REN, IFC, | See Figure 4 | | | 45 | |
| tPLZ | Output disable time from low level | | and DAV) | | | | 20 | |
| tPZH | Output enable time to high level | TE, DC, | | | | | 30 | |
| tPHZ | Output disable time from high level | or | Terminal | $C_L = 15 pF$, | | | 25 | ns |
| tPZL | Output enable time to low level | sc | | See Figure 5 | | | 30 | |
| tPLZ | Output disable time from low level | | | | | | 25 | |

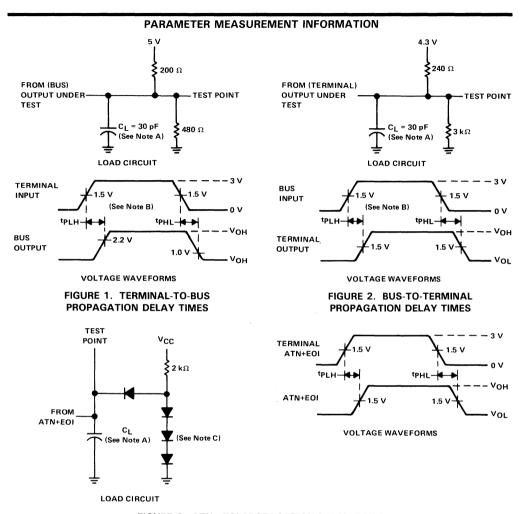
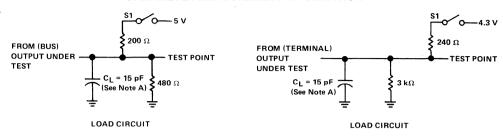
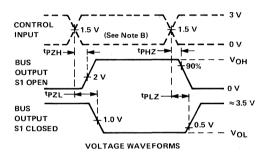


FIGURE 3. ATN + EOI PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \le 6 \text{ ns}, Z_{out} = 50 \Omega.$
- C. All diodes are 1N916 or 1N3064.





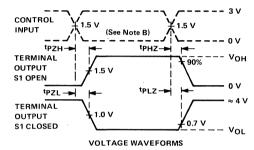
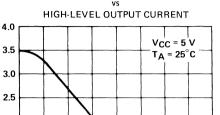


FIGURE 4. BUS ENABLE AND DISABLE TIMES

FIGURE 5. TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 6 ns, $t_{out} =$ 50 Ω .



TERMINAL HIGH-LEVEL OUTPUT VOLTAGE

2.5 2.0 1.5 1.0 0.5 0 0 -5 -10 -15 -20 -25 -30 -35 -40

VOH-High-Level Output Voltage-V

IOH—High-Level Output Current—mA
FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE

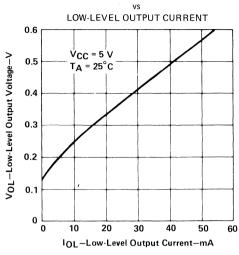


FIGURE 7

TERMINAL OUTPUT VOLTAGE

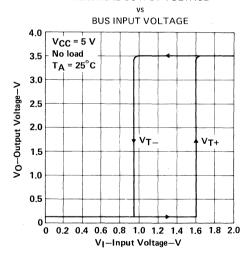
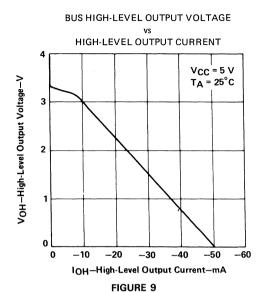
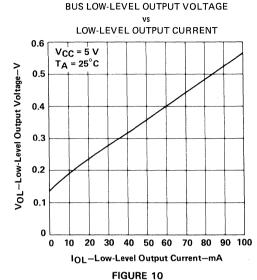
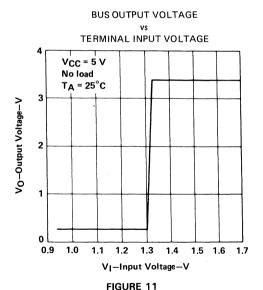
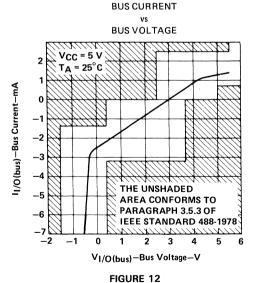


FIGURE 8









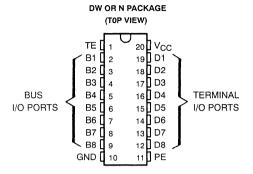
D3011, JUNE 1986-REVISED AUGUST 1989

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)
- · Power-Up/Power-Down Protection (Glitch-Free)
- Driver and Receiver Can Be Disabled Simultaneously

description

The SN75ALS165 eight-channel general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device designed for two-way communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If Talk



FUNCTION TABLES

| FACH | DRIVER |
|------|--------|
| | |

| EACH | REC | FIV | E |
|------|-----|-----|---|
| | | _ | _ |

| INPUTS | | OUTPUT | - 1 | NPUT | ·s | OUTPUT | |
|--------|----|--------|----------------|------|----|--------|---|
| D | TE | PE | В | В | TE | PE | D |
| Н | Н | Н | Н | L | L | Н | L |
| L | Н | Х | L | Н | L | Н | Н |
| Н | Χ | L | Z^{\dagger} | Х | Н | Х | Z |
| X | L | Х | Z [†] | Χ | X | L | Z |

H = high level, L = low level, X = irrelevant.

Z = high impedance state

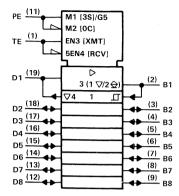
† This is the high impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. Taking TE and PE low places both the drivers and receivers in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature is incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when $V_{CC} = 0$. When combined with the SN75ALS161 or SN75ALS162 management bus transceiver, the pair provides the complete 16-wire interface for the IEEE 488 bus.

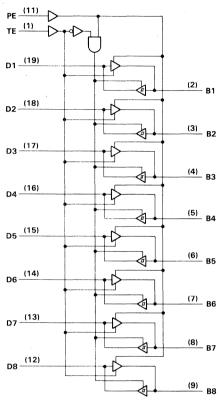
The SN75ALS165 is manufactured in a 20-pin package and is characterized for operation from 0°C to 70°C.

logic symbol[†]

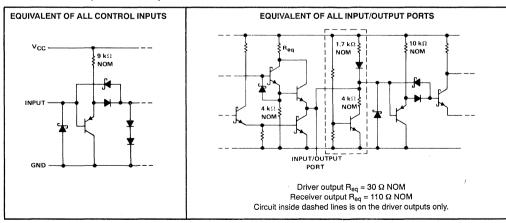


- [†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- ∇ Designates 3-state outputs
- Θ Designates passive-pullup outputs

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | 7 V |
|--|------------------------------|
| Input voltage | 5.5 V |
| Low-level driver output current | 100 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | 65°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from the case for 10 seconds | 260°C |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING |
|---------|----|---------------------------------------|--|---------------------------------------|
| | DW | 1025 mW | 8.2 mW/°C | 656 mW |
| | N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | | MIN | МОМ | MAX | UNIT |
|--|-------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, V _{IH} | | | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| High-level output current, I _{OH} | Bus ports with pullups active | | | -5.2 | mA |
| riigir-iever output current, 10H | Terminal ports | | | -800 | μΑ |
| Law level output surrent 1 | Bus ports Terminal ports | | | 48 | mA |
| ow-level output current, I _{OL} | | | - | 16 | IIIA |
| Operating free-air temperature, T _A | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT | |
|-----------------------|--|-----------------|--|---|------------------|------|------|----------|
| VIK | Input clamp voltage | | $I_1 = -18 \text{ mA}$ | | | -0.8 | 1.5 | V |
| V_{hys} | Hysteresis (V _{T+} V _{T-}) | Bus | | | 0.4 | 0.65 | | ٧ |
| V _{OH} ‡ | High-level | Terminal | $I_{OH} = -800 \mu A$, | TE at 0.8 V | 2.7 | 3.5 | | |
| VOH. | output voltage | Bus | $I_{OH} = -5.2 \text{ mA},$ | PE and TE at 2 V | 2.5 | 3.3 | | v |
| V _{OL} | Low-level | Terminal | I _{OL} = 16 mA, | TE at 0.8 V | | 0.3 | 0.5 | V |
| VOL | output voltage | Bus | I _{OL} = 48 mA, | TE at 2 V | | 0.35 | 0.5 | v |
| l _i | Input current at maximum input voltage | Terminal | V _I = 5.5 V | | | 0.2 | 100 | μΑ |
| I _{IH} | High-level input current | Terminal and | V _i = 2.7 V | | | 0.1 | 20 | μΑ |
| I _{IL} | Low-level input current | control | V ₁ = 0.5 V | | | -10 | -100 | μА |
| \/ | Voltage at bus port | | Driver disabled | I _{I(bus)} = 0 | 2.5 | 3 | 3.7 | V |
| V _{I/O(bus)} | voltage at bus port | | Driver disabled | I _{I(bus)} = -12 mA | | | -1.5 | v |
| | | Power on | Driver disabled | $V_{I(bus)} = -1.5 \text{ V to } 0.4 \text{ V}$ | -1.3 | | | |
| | | | | V _{i(bus)} = 0.4 V to 2.5 V | 0 | | -3.2 | |
| I _{I/O(bus)} | Current into bus port | | | V _{I(bus)} = 2.5 V to 3.7 V | | | 2.5 | mA |
| ·I/O(ous) | | | | | | | -3.2 | |
| | | | | V _{i(bus)} = 3.7 V to 5 V | 0 | | 2.5 | |
| | | | | V _{I(bus)} = 5 V to 5.5 V | 0.7 | | 2.5 | |
| | | Power off | V _{CC} = 0 , | V _{I(bus)} = 0 to 2.5 V | | | 40 | μΑ |
| los | Short-circuit | Terminal | | | -15 | -35 | -75 | mA |
| .05 | output current | Bus | | | -25 | -50 | -125 | |
| lcc | Supply current | | No load | Terminal outputs low and enabled | | 42 | 65 | mA |
| .00 | | | | Bus outputs low and enabled | | 52 | 80 | 1117 \ |
| C _{i/o(bus)} | Bus-port capacitance | | V _{CC} = 5 V to 0, f = 1 MHz | | | 30 | | pF |

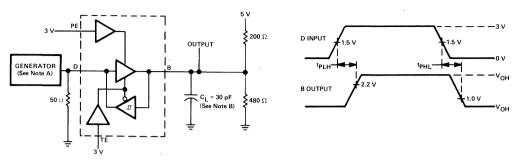
 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25°C.

 $[\]ensuremath{^{\ddagger}}\ensuremath{\text{V}_{\text{OH}}}$ applies for 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|-------------------------------------|-----------------|--------------|--------------------------|-----|------|-----|------|
| t _{PLH} | Propagation delay time, | | | | | 7 | 20 | |
| 7-671 | low-to-high-level output | Terminal | Bus | $C_L = 30 pF$, | | | | ns |
| t _{PHL} | Propagation delay time, | Termina | Dus | See Figure 1 | | 8 | 20 | 113 |
| TPHL | high-to-low-level output | İ | | | | Ü | 20 | |
| | Propagation delay time, | | | | | 7 | 14 | |
| t _{PLH} | low-to-high-level output | Bug | Torminal | $C_{L} = 30 \text{ pF},$ | | , | 14 | |
| t _{PHL} | Propagation delay time, | Bus | Bus Terminal | See Figure 2 | | 9 | 14 | ns |
| 1PHL | high-to-low-level output | | | | | 9 | '" | |
| t _{PZH} | Output enable time to high level | | Bus | | | 19 | 30 | |
| t _{PHZ} | Output disable time from high level |] _{TE} | | $C_L = 15 pF$, | | 5 | 12 | ns |
| t _{PZL} | Output enable time to low level |] '= | | See Figure 3 | | 16 | 35 | ns |
| t _{PLZ} | Output disable time from low level | 1 | | | | 9 | 20 | |
| t _{PZH} | Output enable time to high level | | | | | 13 | 30 | |
| t _{PHZ} | Output disable time from high level | TE | Terminal | $C_L = 15 pF$, | | 12 | 20 | |
| t _{PZL} | Output enable time to low level | 1 '5 | reminai | See Figure 4 | | 12 | 20 | ns |
| t _{PLZ} | Output disable time from low level | | | | | 11 | 20 | |
| t _{en} | Output pull-up enable time | DE. | T | $C_L = 15 pF$, | | 11 | 22 | |
| t _{dis} | Output pull-up disable time | PE | Terminal ' | See Figure 5 | | 6 | 12 | ns |

[†] All typical values are at $T_A = 25$ °C.



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES

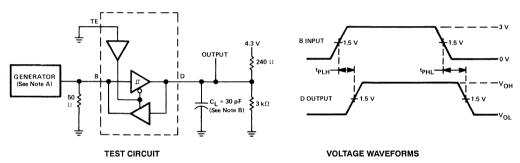


FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

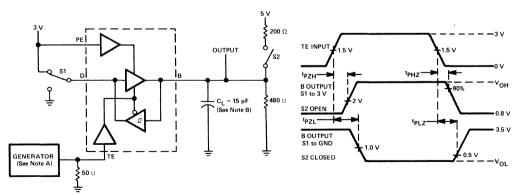


FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_f ≤ 6 ns, t_f ≤ 6 ns, $Z_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.



PARAMETER MEASUREMENT INFORMATION

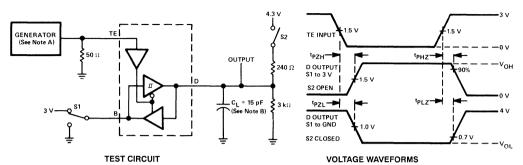


FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES

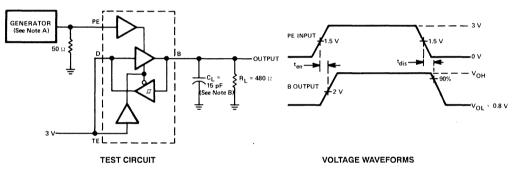
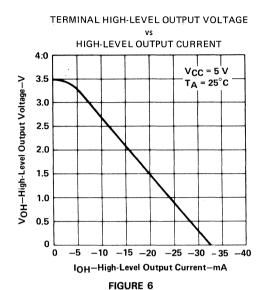
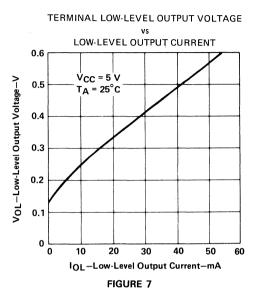


FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

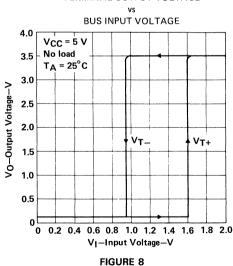
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 6 ns, $t_{f} \le$ 7 ns, $t_{f} \le$ 8 ns, $t_{f} \le$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, $t_{f} \ge$ 9 ns, t_{f}

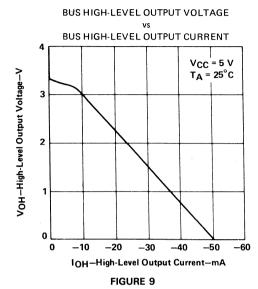
B. C_L includes probe and jig capacitance.

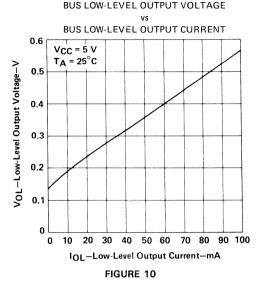


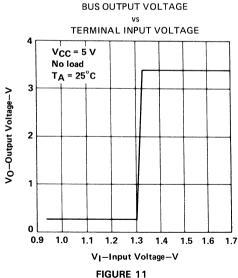


TERMINAL OUTPUT VOLTAGE









SN75ALS170 TRIPLE DIFFERENTIAL BUS TRANSCEIVER

D3040, AUGUST 1987-REVISED MAY 1990

- Three Bidirectional Transceivers
- Driver Meets EIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements
 90 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ± 60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Features Independent Direction Controls for Each Channel

J PACKAGE (TOP VIEW)

| _ | | ı |
|-----------------|------|-------------------|
| 1D[1 | U 14 |] 1B |
| 1DIR[] 2 | 13 |] 1A |
| GND[]₃ | 12 |] v _{cc} |
| 2D [] 4 | 11 | 2B |
| 2DIR[5 | 10 |] 2A |
| 3D [] 6 | 9 |] 3B |
| 3DIR[] 7 | 8 |] 3A |
| | | |

Function Table (each driver)

| INPUT | DIR | ОЦТІ | PUTS |
|-------|-----|------|------|
| D | DIR | Α | В |
| Н | Н | Н | L |
| L | Н | L | Н |
| × | L | z | Z |

Function Table (each receiver)

| DIFFERENTIAL INPUTS A – B | DIR | OUTPUT R |
|-----------------------------------|-----|-------------|
| V _{ID} ≥ 0.3 V | L | Н |
| - 0.3 V < V _{ID} < 0.3 V | L | ? |
| V _{ID} ≤ -0.3V | L | L |
| X | Н | Z |

H = high level, L = low level, ? = indeterminate;

X = irrelevant, Z = high impedance (off)

description

The SN75ALS170 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

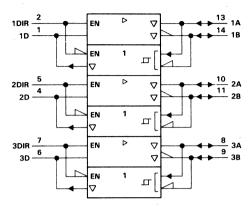
The SN75ALS170 operates from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 is characterized for operation from 0°C to 70°C.



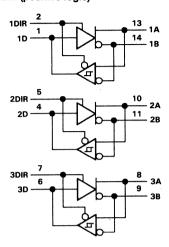
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logic symbol†

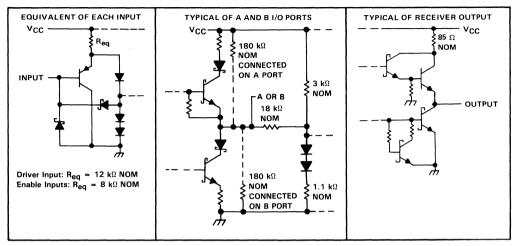


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|--|-------------|
| Voltage at any bus terminal | 0 V to 15 V |
| Enable input voltage | 5.5 V |
| Continuous total power dissipation See Dissipation R | ating Table |
| Operating free-air temperature range |)°C to 70°C |
| Storage temperature range65° | C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | 300°C |

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|----------------------------------|---------------------------------------|
| . j | 1025 mW | 8.2 mW/°C | 656 mW |

recommended operating conditions

| | | | MIN | TYP | MAX | UNIT |
|--|----------|--|------|-----|------|-------|
| Supply voltage, V _{CC} | | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common mode), V _I or V _{IC} | | | | 12 | V | |
| | | | | -7 | • | |
| High-level input voltage, VIH | D, DIR | | 2 | | | ٧ |
| Low-level input voltage, VIL | D, DIR | | | | 8.0 | V |
| Differential input voltage, V _{ID} (see Note 2) | | | | | ±12 | V |
| High-level output current, IOH | Driver | | | | -60 | mA |
| High-lever output current, IOH | Receiver | | | | -400 | μΑ |
| 1 1 1 1 1 | Driver | | | | 60 | mA |
| Low-level output current, IOL | Receiver | | | | 8 | 111/4 |
| Operating free-air temperature, TA | | | 0 | | 70 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST COND | DITIONS† | MIN | TYP‡ | MAX | UNIT |
|-------------------|---|--|---|----------------------|----------|-----------|------|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | ٧ |
| Vo | Output voltage | IO = 0 | | 0 | | 6 | ٧ |
| VOH | High-level output voltage | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V | IOH = -55 mA | 2.7 | | | ٧ |
| VOL | Low-level output voltage | $V_{CC} = 4.75 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | V _{IH} = 2 V, I _{OL} = 55 mA | | | 1.7 | ٧ |
| VOD1 | Differential output voltage | IO = 0 | | 1.5 | | 6 | V |
| VOD2 | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | 1/2 V _{OD1} | | | ٧ |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V |
| V _{OD3} | Differential output voltage | $V_{\text{test}} = -7 \text{ V to } 12 \text{ V},$ | See Figure 2 | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | | | | ±0.2 | ٧ |
| Voc | Common-mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | +3 -1 | ٧ |
| Δ V _{OC} | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | ٧ |
| Ю | Output current | Output disabled, See Note 3 | $V_{O} = 12 V$ $V_{O} = -7 V$ | | | 1 -0.8 | mA |
| IH | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| ΊL | Low-level input current | V _I = 0.4 V | | | | -400 | μA |
| | | V _O = -7 V | | | | -250 | |
| loo | Short-circuit output current¶ | $V_O = 0$ | | | | -150 | mA |
| los | Short-circuit output current." | VO = VCC | | | | 250 | IIIA |
| | | V _O = 12 V | | | | 250 | |
| lcc | Supply current | No load | Outputs enabled Outputs disabled | | 69 57 | 90 78 | mA |

[†] The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

[‡] All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta \mid V_{OD} \mid$ and $\Delta \mid V_{OC} \mid$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

[¶] Duration of the short-circuit current should not exceed one second.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-----------------|-------------------------------------|---|--|-----|------------------|-----|------|
| ton | Differential-output delay time | $R_L = 54 \Omega$, See Figure 3 | $C_L = 50 pF$, | 3 | 8 | 13 | ns |
| [†] DD | | $R_{L1} = R_{L3} = 165 \Omega,$ $C_{L} = 60 \text{ pF},$ | $R_{L2} = 75 \Omega$, See Figure 6 | 3 | 8 | 13 | 113 |
| | 5 | $R_L = 54 \Omega$, See Figure 3 | C _L = 50 pF, | | 1 | 6 | ns |
| | Skew (tDDH-tDDL) | $R_{L1} = R_{L3} = 165 \Omega,$ $C_{L} = 60 \text{ pF},$ | $R_{L2} = 75 \Omega$, See Figure 6 | | 1 | 6 | 115 |
| tro | Differential-output transition time | R _L = 54 Ω, See Figure 3 | C _L = 50 pF, | 3 | 8 | 13 | ns |
| ^t TD | | $R_{L1} = R_{L3} = 165 \Omega,$ $C_{L} = 60 pF,$ | $R_{L2} = 75 \Omega$, See Figure 6 | 3 | 8 | 13 | 113 |
| tPZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 30 | 50 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 30 | 50 | ns |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | 3 | 8 | 13 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | 3 | 8 | 13 | ns |
| tPDE | Differential-output enable time | $R_{L1} = R_{L3} = 165 \Omega$, | $R_{L2} = 75 \Omega$, | 8 | 30 | 45 | ns |
| tPDZ | Differential-output disable time | C _L = 60 pF, | See Figure 7 | 5 | 10 | 15 | ns |

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--|--|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | Vo | V _o |
| VOD2 | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| VOD3 | | V _t (Test Termination Measurement 2) |
| V _{test} | | V _{tst} |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | Vos | V _{os} |
| Δ V _{OC} | $\mid V_{OS} - \overline{V}_{OS} \mid$ | $\mid V_{OS} - \overline{V}_{OS} \mid$ |
| los | I _{sa} , I _{sb} | |
| 10 | I _{xa} , I _{xb} | l _{ia} , l _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST C | TEST CONDITIONS | | TYP [†] | MAX | UNIT |
|------------------|---|---|--------------------------|-------|------------------|------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.3 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$ | I _O = 8 mA | -0.3‡ | | | ٧ |
| V _{hys} | Hysteresis [§] | | | | 60 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | -1.5 | ٧ |
| V _{OH} | High-level output voltage | V _{ID} = 300 mV, See Figure 8 | $I_{OH} = -400 \mu A$, | 2.7 | | | ٧ |
| VOL | Low-level output voltage | V _{ID} = - 300 mV, See Figure 8 | I _{OL} = 8 mA, | | | 0.45 | ٧ |
| loz | High-impedance-state output current | V _O = 2.4 V | | | | 20 | μА |
| 102 | riigh-impedance-state output current | $V_0 = 0.4 \text{ V}$ | | | | -400 | μΛ |
| l _l | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA |
| 4 | Line input current | See Note 4 | $V_1 = -7 \text{ V}$ | | | 0.8 | шА |
| Ιн | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| IL | Low-level enable-input current | V _{IL} = 0.4 V | , | | | -100 | μА |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | V _{ID} = 300 mV, | V _O = 0 | -15 | | -85 | mA |
| loo | Supply current | No load | Outputs enabled | | 69 | 90 | mA |
| lcc | Supply current | NO IOAU | Outputs disabled | | 57 | 78 | iiiA |

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|--|--|---------------|-----|------|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | 0 45 5 | 9 | 14 | 19 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ See Figure 9 | CL = 15 pF, | 9 | 14 | 19 | ns |
| | Skew (tpLH - tpHL) | See rigule 9 | | | 2 | 6 | ns |
| ^t PZH | Output enable time to high level | C _I = 15 pF, | See Figure 10 | | 7 | 14 | ns |
| tPZL | Output enable time to low level | OL = 15 pr, | | | 7 | 14 | ns |
| ^t PHZ | Output disable time from high level | C _I = 15 pF, | See Figure 10 | | 20 | 35 | ns |
| tPLZ | Output disable time from low level | о[– 13 рг, | | | 8 | 17 | ns |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

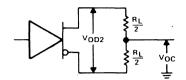


FIGURE 1. DRIVER VOD AND VOC

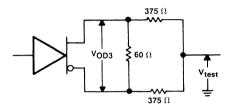


FIGURE 2. DRIVER VOD3

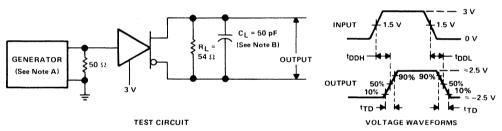


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 6 ns, $Z_0 = 50 \Omega$.

B. CL includes probe and jig capacitance.

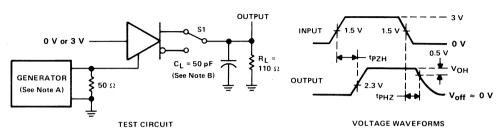


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

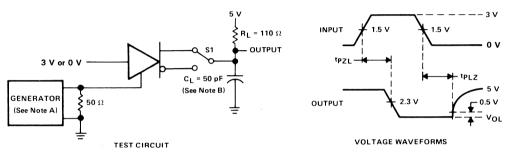


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 6 ns, $Z_0 = 50 \Omega$.

B. C_L includes probe and jig capacitance.

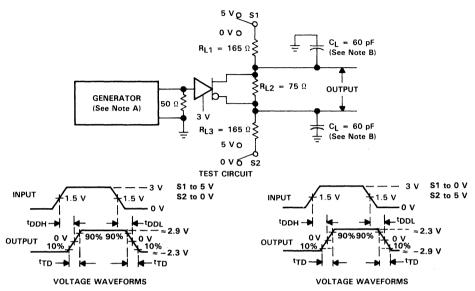
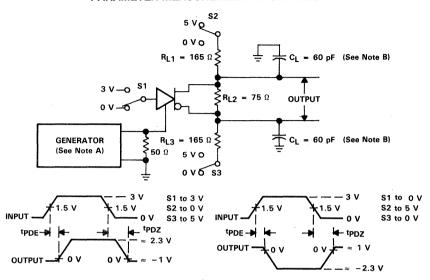


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f

B. C₁ includes probe and jig capacitance.



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR < 1 MHz, 50% duty cycle, tr < 6 ns, tr < 6 ns, $Z_0 = 50 \Omega$.

B. CL includes probe and jig capacitance.

FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

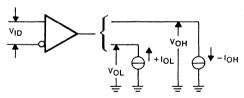


FIGURE 8. RECEIVER VOH AND VOL

PARAMETER MEASUREMENT INFORMATION INPUT 1.5 V OUTPUT GENERATOR - 0 V (See Note A) 1.5 V C_L = 15 pF - tPHL (See Note B) - Voh OUTPUT VOL TEST CIRCUIT **VOLTAGE WAVEFORMS** FIGURE 9. RECEIVER PROPAGATION DELAY TIMES -1.5 V ---C_L = 15 pF 1N916 OR EQUIVALENT (See Note B) GENERATOR **50** Ω (See Note A) S3 **TEST CIRCUIT** S1 to 1.5 V INPUT V S2 open INPUT S3 closed S1 to -1.5 V 0 V V S2 closed S3 open tPZH → tPZL- ₩ Vон ≈4.5 V OUTPUT OUTPUT VOL - 3 V - — 3 V S1 to 1.5 V S1 to -1.5 V INPUT INPUT S2 closed S2 closed S3 closed S3 closed tPHZ~ tPLZ — ۷он ≈1.3 V OUTPUT OUTPUT VOL

FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, $t_f \leq$

VOLTAGE WAVEFORMS

B. CL includes probe and jig capacitance.

DRIVER HIGH-LEVEL OUTPUT VOLTAGE DRIVER HIGH-LEVEL OUTPUT CURRENT 5 VCC = 5 V VOH-High-Level Output Voltage-V 4.5 TA = 25°C 4 3.5 3 2.5 2 1.5 0.5 0 -20 -60 -80 -100 -120 0 IOH-High-Level Output Current-mA

DRIVER LOW-LEVEL OUTPUT VOLTAGE DRIVER LOW-LEVEL OUTPUT CURRENT VCC = 5 V 4.5 VOL - Low-Level Output Voltage - V TA = 25°C 4 3.5 3 2.5 2 1.5 1 0.5 0 20 60 100 120 IOL - Low-Level Output Current - mA

FIGURE 11

FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE

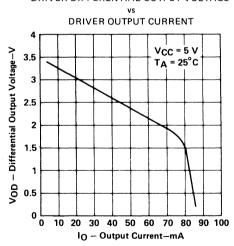


FIGURE 13

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

VS

HIGH-LEVEL OUTPUT CURRENT

VID = 0.3 V

TA = 25 °C

VCC = 5.25 V

VCC = 5.25 V

FIGURE 14

-20

-30

IOH-High-Level Output Current-mA

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

-40

-50

٥Ĺ

-10

RECEIVER LOW-LEVEL OUTPUT CURRENT

0.6

V_{CC} = 5 V

T_A = 25 °C

V_{ID} = -300 mV

0.4

0.5

0.5

0.1

0.1

0.2

10L—Low Level Output Current—mA

FIGURE 16

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

VS

FREE-AIR TEMPERATURE

5

VCC = 5 V

VID = 300 mV

IOH = -440 μA

-40 -20 0 20 40 60 80 100 120

TΔ - Free-Air Temperature - °C

FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

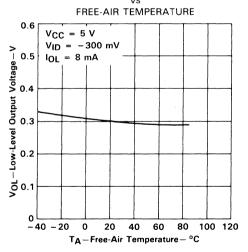


FIGURE 17

RECEIVER OUTPUT VOLTAGE

ENABLE VOLTAGE

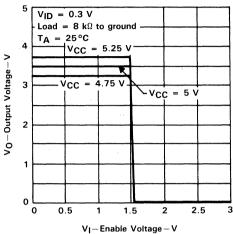
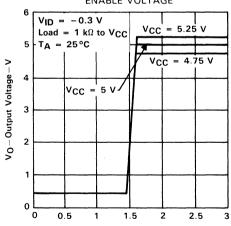


FIGURE 18

RECEIVER OUTPUT VOLTAGE

vs

ENABLE VOLTAGE



V_I-Enable Voltage-V

FIGURE 19

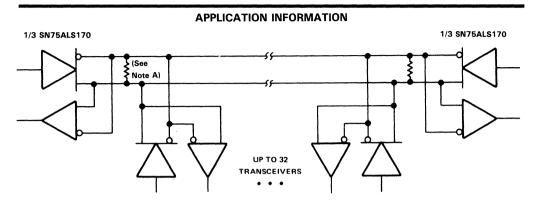


FIGURE 20. TYPICAL APPLICATION CIRCUIT

NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

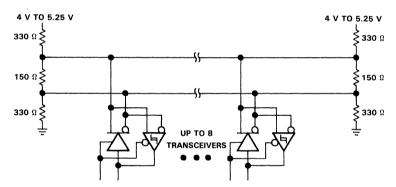


FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

APPLICATION INFORMATION DB(6) DB(5) - DB(5) - DB(4) SN74LS00 DB(3) DB(2) - DB(2) DB(1) - DB(1) DB(0) - DB(0) DB(P) - D8(P) - ACK SB4 SB3 SB2 SB1 SB0 SBP INIT ACK ATN TARGET MSG C/D I/O BSYIN SELINI SBEN - ATN MSG - MSG TO SCSI BUS CONTROLLER SN75ALS170 C/D - C/D REQ SN75ALS170 SEN1 SEN2 -BSY - SEL RST TO RESET LOGIC

FIGURE 22. TYPICAL DIFFERENTIAL SCSI BUS INTERFACE IMPLEMENTATION



SN75ALS171 TRIPLE DIFFERENTIAL BUS TRANSCEIVER

J PACKAGE

D3041, AUGUST 1987-REVISED MAY 1990

- Three Bidirectional Transceivers
- Driver Meets FIA Standards RS-422A and RS-485 and CCITT Recommendations V.11 and X.27 and ANSI Standard X3.131-1986
- **High-Speed Advanced Low-Power Schottky** Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew . . . 6 ns Max
- **Designed for Multipoint Transmission on** Long Bus Lines in Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output **Bus Voltages Ranges**
- Driver Output Capacity . . . ± 60 mA
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current** Limitina
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ± 300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Low Supply Current Requirements 90 mA Max

(TOP VIEW) 1R [20 I 1B 1DE 1 2 19 1A 1D 🛛 3 18 RE GND [17 T CDE GND [16 V_{CC} 2R [] 6 15 D 2B 2DE 🕇 7 14 T 2A 13 T 3B 2D 🛮 8

3R 🛮 9

3DF

FUNCTION TABLE (EACH DRIVER)

12 T 3A

3D

| INPUT | ENABLE | | OUTPUTS | | |
|-------|--------|-----|---------|---|--|
| D | DE | CDE | Α | В | |
| Н | Н | Н | Н | L | |
| L | н | Н | L | Н | |
| X | L | X | Z | Z | |
| X | X | L | z | Z | |

FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL INPUTS | ENABLE | OUTPUT | |
|----------------------------------|--------|--------|--|
| A – B | RE | R | |
| V _{ID} ≥ 0.3 V | L | Н | |
| -0.3 V < V _{ID} < 0.3 V | L | ? | |
| $V_{ID} \leq -0.3 V$ | L | L | |
| x | н | Z | |

H = high level, L = low level, ? = indeterminate,

X = irrelevant, Z = high impedance (off)

description

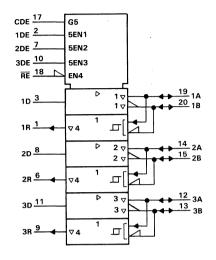
The SN75ALS171 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27 and ANSI Standard X3.131-1986.

The SN75ALS171 operates from a single 5-V power supply. The drivers and receivers have individual activehigh and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or VCC is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

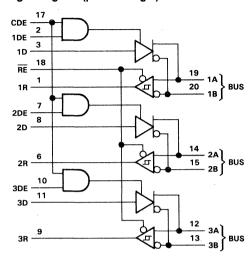
The SN75ALS171 is characterized for operation from 0°C to 70°C.



logic symbol†

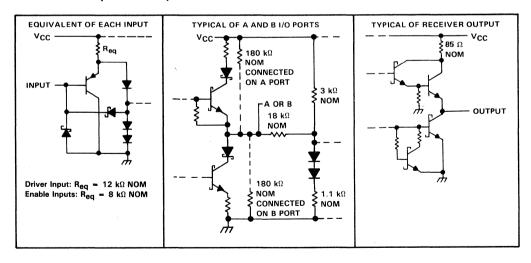


logic diagram (positive logic)



 $^{^{\}dagger}\text{This}$ symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|--|
| Voltage at any bus terminal |
| Enable input voltage |
| Continuous total power dissipation |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds |

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| J | 1025 mW | 8.2 mW/°C | 656 mW |

recommended operating conditions

| | | MIN | TYP | MAX | UNIT |
|--|--------------------|------|-----|-------|------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or common mode), V _I or V _{IC} | | -7 | | 12 | V |
| High-level input voltage, VIH | D, CDE, DE, and RE | 2 | | | V |
| Low-level input voltage, VIL | D, CDE, DE, and RE | | | 0.8 | V |
| Differential input voltage, V _{ID} (see Note 2) | | | | ±12 | V |
| | Driver | | | - 60 | mA |
| High-level output current, IOH | Receiver | | | - 400 | μΑ |
| I am I am I am I am I am I am I am I am | Driver | | | 60 | |
| Low-level output current, IOL | Receiver | | | 8 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating freeair temperature (unless otherwise noted)

| | PARAMETER | TEST CONE | OITIONS† | MIN | TYP‡ | MAX | UNIT |
|-------------------|---|---|---|----------------------|------|--------------|------|
| VIK | Input clamp voltage | $I_{I} = -18 \text{ mA}$ | | | | -1.5 | ٧ |
| Vo | Output voltage | IO = 0 | | 0 | | 6 | ٧ |
| Vон | High-level output voltage | $V_{CC} = 4.75 \text{ V},$ $V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}$ | I _{OH} = -55 mA | 2.7 | | | ٧ |
| V _{OL} | Low-level output voltage | $V_{CC} = 4.75 \text{ V},$ $V_{1L} = 0.8 \text{ V},$ | V _{IH} = 2 V, I _{OL} = 55 mA | | | 1.7 | ٧ |
| VOD1 | Differential output voltage | IO = 0 | | 1.5 | | 6 | ٧ |
| V _{OD2} | Differential output voltage | $R_L = 100 \Omega$, | See Figure 1 | 1/2 V _{OD1} | | | V |
| | D''. | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | V |
| V _{OD3} | Differential output voltage | $V_{\text{test}} = -7 \text{ V to } 12 \text{ V},$ | See Figure 2 | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | | | | ±0.2 | ٧ |
| Voc | Common-mode output voltage | $R_L = 54 \Omega \text{ or } 100 \Omega,$ | See Figure 1 | | | +3 -1 | ٧ |
| Δ V _{OC} | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | ٧ |
| Ю | Output current | Output disabled, See Note 3 | $V_{O} = 12 V$ $V_{O} = -7 V$ | | | 1 0.8 | mA |
| liн | High-level enable-input current | D and DE CDE | V _{IH} = 2.7 V | | | 20 60 | |
| I _{IL} | Low-level enable-input current | D and DE CDE | V _{IL} = 0.4 V | | | -100 -900 | μА |
| * | | V _O = -7 V | | <u> </u> | | -250 | |
| loo | Short-circuit output current [¶] | $V_O = 0$ | | | | -150 | mA |
| los | Short-circuit output current." | $V_O = V_{CC}$ | | | | 250 | mA |
| | | V _O = 12 V | | - | | 250 | |
| lcc | Supply current | No load | Outputs enabled | | 69 | 90 | mA |
| | cupply current | | Outputs disabled | | 57 | 78 | |

[†] The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs. ‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

 $[\]frac{1}{2}$ $\frac{1}{2}$ p>¶</sup> Duration of the short-circuit current should not exceed one second.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | PARAMETER TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT | | | |
|------------------|-------------------------------------|-------------------------------------|------------------------|-----|------------------|-----|------|---|---|-----|
| | , | $R_L = 54 \Omega$, See Figure 3 | $C_L = 50 pF$, | 3 | 8 | 13 | | | | |
| tDD | Differential-output delay time | $R_{L1} = R_{L3} = 165 \Omega,$ | $R_{L2} = 75 \Omega$, | | | | ns | | | |
| | | $C_L = 60 pF$, | $V_{TERM} = 5 V$, | 3 | 8 | 13 | | | | |
| | | See Figure 6 | | | | | | | | |
| | | $R_L = 54 \Omega$, | $C_L = 50 \text{ pF},$ | | 1 | 6 | | | | |
| | Skew (tppH-tppL) | See Figure 3 | | | | Ŭ | ns | | | |
| | Skew (LiDDH iDDL L) | $R_{L1} = R_{L3} = 165 \Omega$, | $R_{L2} = 75 \Omega$, | | | | | 1 | 6 | 110 |
| | | $C_L = 60 pF$, | See Figure 6 | | | U | | | | |
| | | $R_L = 54 \Omega$, | $C_L = 50 pF$, | 3 | 8 | 13 | | | | |
| | | See Figure 3 | | 3 | G | 10 | | | | |
| tTD | Differential-output transition time | $R_{L1} = R_{L3} = 165 \Omega$, | $R_{L2} = 75 \Omega$ | | | | ns | | | |
| | | C _L = 60 pF, | $V_{TERM} = 5 V$, | 3 | 8 | 13 | | | | |
| | | See Figure 6 | | | | | | | | |
| ^t PZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 30 | 50 | ns | | | |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 30 | 50 | ns | | | |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | 3 | 8 | 13 | ns | | | |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | 3 | 8 | 13 | ns | | | |
| tPDE | Differential-output enable time | $R_{L1} = R_{L3} = 165 \Omega$, | $R_{L2} = 75 \Omega$, | 8 | 30 | 45 | ns | | | |
| tPDZ | Differential-output disable time | C _L = 60 pF, | See Figure 7 | 5 | 10 | 15 | ns | | | |

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--------------------------------------|--|
| Vo | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | V _o | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| VOD3 | | V _t (Test Termination Measurement 2) |
| V _{test} | | V _{tst} |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | V _{os} | V _{os} |
| Δ V _{OC} | $ V_{OS} - \overline{V}_{OS} $ | $\mid V_{OS} - \overline{V}_{OS} \mid$ |
| los | I _{sa} , I _{sb} | |
| 10 | l _{xa} , l _{xb} | lia, lib |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage. supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CO | ONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------|---|---|-------------------------|-----------------|-----|------|------|----|
| VTH | Differential-input high-threshold voltage | V _O = 2.7 V, | $I_0 = -0.4 \text{ mA}$ | | | 0.3 | ٧ | |
| V_{TL} | Differential-input low-threshold voltage | $V_{O} = 0.5 V$ | I _O = 8 mA | -0.3‡ | | | ٧ | |
| V _{hys} | Hysteresis [§] | | | | 60 | | mV | |
| VIK | Enable-input clamp voltage | $I_{\rm I} = -18~{\rm mA}$ | | | | -1.5 | V | |
| Vон | High-level output voltage | V _{ID} = 300 mV, See Figure 8 | $I_{OH} = -400 \mu A$ | 2.7 | | | ٧ | |
| VOL | Low-level output voltage | V _{ID} = - 300 mV, See Figure 8 | I _{OL} = 8 mA, | | , | 0.45 | ٧ | |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | | | | ±20 | μА | |
| 1. | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA | |
| 11 | Line input current | See Note 4 | $V_I = -7 \text{ V}$ | | | -0.8 | MA | |
| lн | High-level enable-input current | V _{IH} = 2.7 V | | | | 60 | μА | |
| IL | Low-level enable-input current | V _{IL} = 0.4 V | | | | -300 | μА | |
| rį | Input resistance | | | 12 | | | kΩ | |
| los | Short-circuit output current | V _{ID} = 300 mV, | V _O = 0 | -15 | | -85 | mA | |
| loo | Cumply automat | C | No load | Outputs enabled | | 69 | 90 | mA |
| ICC | Supply current | No load | Outputs disabled | | 57 | 78 | шА | |

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|---|-----------------|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | ., , , , , , , , , , , , , , , , , , , | | | 14 | 19 | ns |
| tPHL | Propagation delay time, high-to-low-level output | V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 9 | $C_L = 15 pF$, | 9 | 14 | 19 | ns |
| | Skew (tpLH - tpHL) | See rigule 9 | | | 2 | 6 | ns |
| t _{PZH} | Output enable time to high level | C _I = 15 pF, | See Figure 10 | | 7 | 14 | ns |
| tPZL | Output enable time to low level | OL = 15 pr , | See rigule 10 | | 7 | 14 | ns |
| tPHZ | Output disable time from high level | C ₁ = 15 pF, See Figure 10 | | 20 | 35 | ns | |
| tPLZ | Output disable time from low level | O[= 15 pr, | See Figure 10 | | 8 | 17 | ns |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

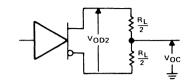


FIGURE 1. DRIVER VOD AND VOC

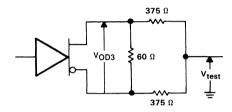


FIGURE 2. DRIVER VOD3

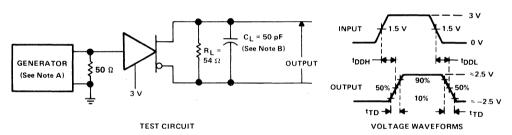


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 7 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 8 ns, $t_f \leq$ 9 ns, t_f

B. CL includes probe and jig capacitance.

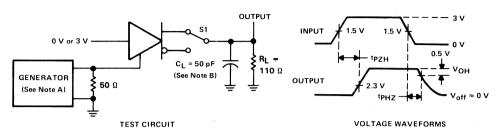


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

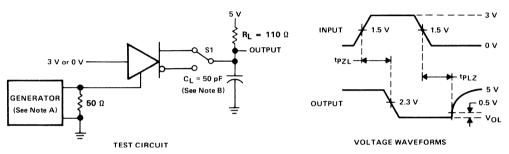


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR < 1 MHz, 50% duty cycle, t_f < 6 ns, t_f < 6 ns, $Z_0 = 50 \Omega$. B. CL includes probe and jig capacitance.

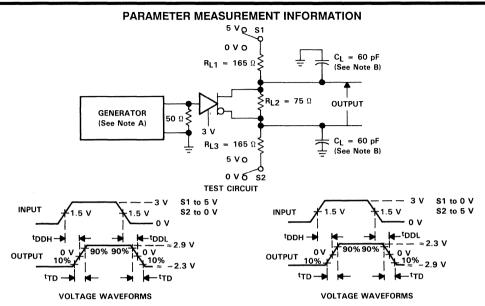


FIGURE 6. DRIVER DELAY AND TRANSITION TIMES WITH DOUBLE-DIFFERENTIAL-SCSI TERMINATION FOR THE LOAD

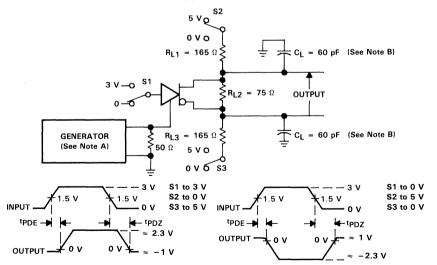


FIGURE 7. DRIVER DIFFERENTIAL-ENABLE AND DISABLE TIMES WITH A DOUBLE-SCSI TERMINATION

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.

B. C_L includes probe and jig capacitance.



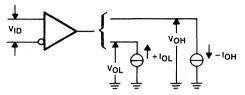


FIGURE 8. RECEIVER VOH AND VOL

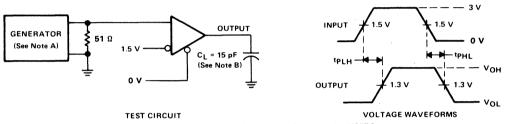


FIGURE 9. RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 7 ns, $t_f \le$ 8 ns, $t_f \le$ 8 ns, $t_f \le$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, t_f

B. CL includes probe and jig capacitance.

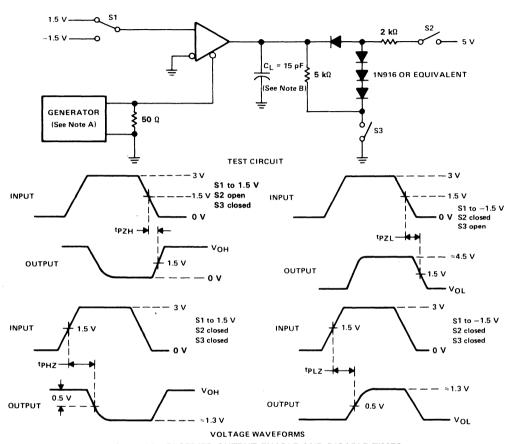
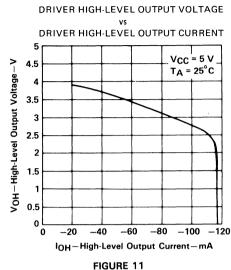


FIGURE 10. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \le 1 MHz, 50% duty cycle, $t_r \le$ 6 ns, $t_f \le$ 7 ns, $t_f \le$ 8 ns, $t_f \le$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, $t_f \ge$ 9 ns, t_f

B. CL includes probe and jig capacitance.



DRIVER LOW-LEVEL OUTPUT VOLTAGE DRIVER LOW-LEVEL OUTPUT CURRENT

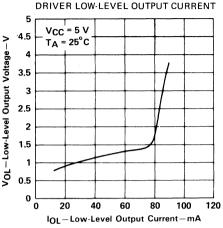


FIGURE 12

DRIVER DIFFERENTIAL OUTPUT VOLTAGE

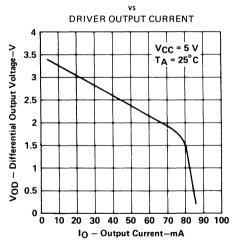


FIGURE 13

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

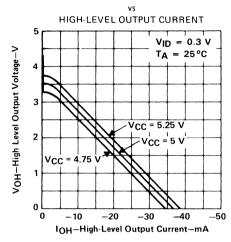


FIGURE 14

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

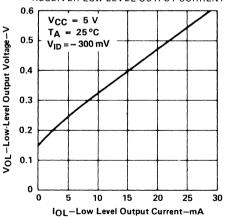


FIGURE 16

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

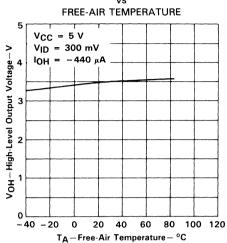


FIGURE 15

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

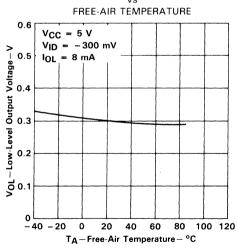
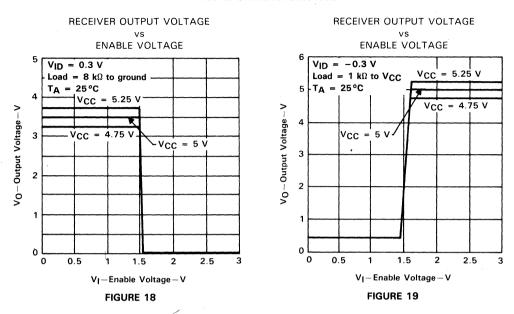
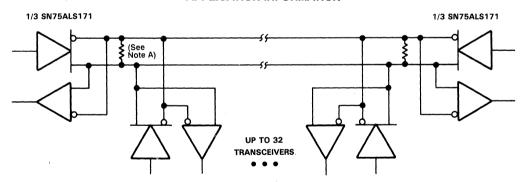


FIGURE 17



APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 20. TYPICAL APPLICATION CIRCUIT

APPLICATION INFORMATION

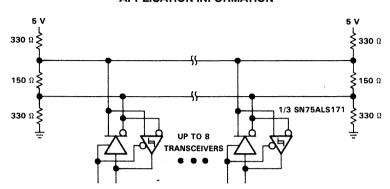


FIGURE 21. TYPICAL DIFFERENTIAL SCSI APPLICATION CIRCUIT

APPLICATION INFORMATION DB(6) 10 - DB(5) DB(4) DB(3) - DB(1) DB(0) - DB(0) DB(P) -- DB(P) SB6 SB5 SB4 SB3 SB2 SB1 SB0 SBP ACK ATN TARGET MSG C/D I/O REQ BSYOUT BSYIN SELOUT TO SCSI BUS CONTROLLER C/D - C/D 1/0 ARB REQ SEN1 7 SEN2 SEN3 EN4 18 - SEL RST - RST TO RESET LOGIC

FIGURE 22. TYPICAL DIFFERENTIAL SCSI BUS INTERFACE IMPLEMENTATION



SN75ALS191 DUAL DIFFERENTIAL LINE DRIVER

D3068, DECEMBER 1987-REVISED AUGUST 1989

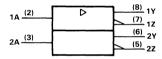
- Meets EIA Standard RS-422-A
- High Speed, Low-Power ALS Design
- TTL-and CMOS-Input Compatibility
- Single 5-V Supply Operation
- Output Short-Circuit Protection
- Improved Replacement for the UA9638

description

The SN75ALS191 is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-volt power supply and is supplied in 8-pin packages.

The SN75ALS191 is characterized for operation from 0°C to 70°C.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

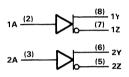
D OR P PACKAGE (TOP VIEW)

| vcc ☐ | 1 | U | 8 |]1Y |
|-------|---|---|---|-----|
| 1 A 🗌 | 2 | | 7 |]1Z |
| 2A 🗌 | 3 | | 6 |]2Y |
| GND [| 4 | | 5 |]2Z |

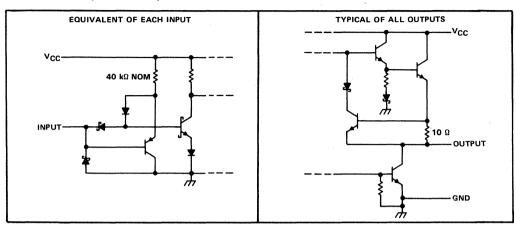
FUNCTION TABLE (EACH DRIVER)

| Ì | INPUT | OUT | PUTS |
|---|-------|-----|------|
| | Α | Y | Z |
| | Н | Н | L |
| | L | L | н |

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage, V ₁ |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values except differential output voltage V_{OD} are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| High-level output current, IOH | | | - 50 | mA |
| Low-level output current, IOL | | | 50 | mA |
| Operating free-air temperature, TA | | | 70 | °C |

electrical characteristics over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDIT | TIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|-------------------------------------|--|--------------------------------|------|------------------|------------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 \text{ V}, I_{I} = -18 \text{ m/s}$ | 1 | | -1 | -1.2 | V |
| Vон | High-level output voltage | | I _{OH} = -10 mA | 2.5 | 3.3 | | V |
| -011 | | | I _{OH} = -40 mA | 2 | | | |
| VOL | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ | $V_{IL} = 0.8 V$ | | | 0.5 | v |
| | | I _{OL} = 40 mA | | | | | |
| V _{OD1} | Differential output voltage | $V_{CC} = 5.25 \text{ V}, I_{O} = 0$ | | | | $2V_{OD2}$ | V |
| VOD2 | Differential output voltage | | | 2 | | | V |
| | Change in magnitude of ‡ | | | | | ±0.4 | v |
| △ V _{OD} | differential output voltage | | | | ±0.4 | V | |
| Voc | Common-mode output voltage § | $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V, R}_{L} = 100 \Omega, \text{ See Figure 1}$ | | | | 3 | ٧ |
| A1 W 1 | Change in magnitude of [‡] | | | | | ±0.4 | v |
| △ Voc I | common-mode output voltage | | | | | ±0.4 | ı v |
| | | | V _O = 6 V | | 0.1 | 100 | |
| 10 | Output current with power off | V _{CC} = 0 | $V_0 = -0.25 \text{ V}$ | | -0.1 | - 100 | μΑ |
| | | | $V_0 = -0.25 \text{ V to 6 V}$ | | | ± 100 | |
| lį | Input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$ | | | | 50 | μΑ |
| ΉΗ | High-level input current | $V_{CC} = 5.25 \text{ V}, \text{ V}_{j} = 2.7 \text{ V}$ | | | | 25 | μΑ |
| ijL | Low-level input current | $V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.5 \text{ V}$ | | | | -200 | μΑ |
| los | Short-circuit output current¶ | $V_{CC} = 5.25 \text{ V}, V_{O} = 0$ | | - 50 | | - 150 | mA |
| Icc | Supply current (all drivers) | V _{CC} = 5.25 V, No load, | All inputs at 0 V | | 32 | 40 | mA |

[†]All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25 ^{\circ}\text{C}$.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), $V_{CC} = 5 \text{ V}$

| PARAMETER | | TEST CONDITION | | MIN | TYP# | MAX | UNIT |
|-----------|-------------------------------------|-------------------------|------------------------|-----|------|-----|------|
| tDD | Differential-output delay time | C: - 15 pF | R _I = 100 Ω | | 3.5 | 7 | ns |
| tTD | Differential-output transition time | C _L = 15 pF, | _ | | 3.5 | 7 | ns |
| | Skew | See Figure 2 | | | 1.5 | 4 | ns |

 $^{^{\#}}$ Typical values are at T_A = 25 °C.

[‡]Δ| V_{OD} | and Δ| V_{OC} | are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

¶Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

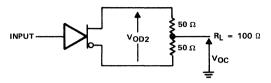
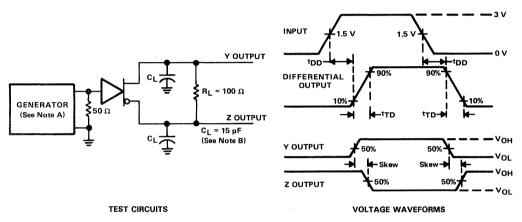


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



NOTES: A. The input pulse generator has the following characteristics: $Z_{OUT} = 50 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$, $t_f = \leq 5 \text{ ns}$.

B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

D2931, JUNE 1986-REVISED AUGUST 1989

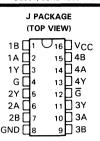
- Meets EIA Standards RS-422-A and RS-423-A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . 7 V to 7 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-V Supply
- Low ICC Requirements:
 ICC . . . 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

description

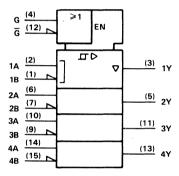
The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using Advanced Low-Power Schottky technology. technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of EIA Standards RS-422-A and RS-423-A. It features 3-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of \pm 200 mV over a common-mode input voltage range of -7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS193 is characterized for operation from 0°C to 70°C.

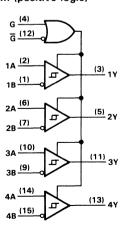


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENABLES | | OUTPUT |
|---|---------|---|--------|
| A-B | G | G | Υ |
| V > 0.2 V | Н | Х | • н |
| V _{ID} ≥ 0.2 V | Х | L | Н |
| 0.01/2.1/2.2001/ | Н | X | ? |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | Х | Ł | ? |
| V 02V | Н | X | L |
| V _{ID} ≤ ~0.2 V | X | L | L |
| X | L | Н | Z |

H = high level

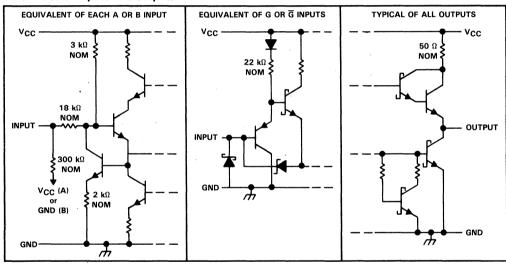
L = low level

X = irrelevant

? = indeterminate

Z = high impedance (off)

schematics of inputs and outputs



SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage, A or B inputs |
| Differential input voltage (see Note 2) |
| Enable input voltage |
| Low-level output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3) 1025 mW |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

- 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. For operation above 25 °C free-air temperature, derate the J package to 656 mW at 70 °C at the rate of 8.2 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V _{IC} | | | ±7 | V |
| Differential input voltage, V _{ID} → | | | ±12 | V |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | ٧ |
| High-level output current, IOH | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------------|---|---|--------------------------|--------------------|------------------|-------|----------|
| V _{T+} | Positive-going threshold voltage | | | | | 200 | mV |
| VT- | Negative-going threshold voltage | | | - 200 [‡] | | | mV |
| V _{hys} | Hysteresis § | | | | 120 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | - 1.5 | V |
| Voн | High-level output voltage | V _{ID} = 200 mV, See Figure 1 | $I_{OH} = -400 \mu A$, | 2.7 | 3.6 | | V |
| VOL | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ | $I_{OL} = 8 \text{ mA}$ | | | 0.45 | V |
| VOL | Low level output voltage | See Figure 1 | $I_{OL} = 16 \text{ mA}$ | | | 0.5 | |
| In- High impodence ato | High-impedance-state output current | 1 Vcc = 5.25 V | $V_0 = 2.4 \text{ V}$ | | | 20 | μΑ |
| loz | riigii-iiiipedance-state output current | | $V_O = 0.4 V$ | | | - 20 | <u> </u> |
| ļ. | Line input current | Other input at 0 V, | V _I = 15 V | | 0.7 | 1.2 | mA |
| կ | See ! | See Note 4 | $V_{I} = -15 \text{ V}$ | | - 1.0 | -1.7 | '''^ |
| 1 | High lovel anable input averant | | $V_{IH} = 2.7 V$ | | | 20 | μΑ |
| ۱н | High-level enable-input current | | V _{IH} = 5.25 V | | | 100 | μΑ |
| IIL | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| | Input resistance | | | 12 | 18 | | kΩ |
| los | Short-circuit output current | V _{ID} = 3 V, See Note 5 | V _O = 0, | - 15 | - 78 | - 130 | mA |
| Icc | Supply current | Outputs disabled | | | 22 | 35 | mA |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -2.5 \text{ V to } 2.5 \text{ V, } C_L = 15 \text{ pF,}$ | | | 15 | 22 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | See Figure 2 | | | 15 | 22 | ns |
| tPZH | Output enable time to high level | $C_L = 15 pF$, | See Figure 3 | | 13 | 25 | ns |
| tPZL | Output enable time to low level | $C_L = 15 pF$, | See Figure 3 | | 11 | 25 | ns |
| tPHZ | Output disable time from high level | $C_L = 5 pF$, | See Figure 3 | | 13 | 25 | ns |
| tPLZ | Output disable time from low level | C _L = 5 pF, | See Figure 3 | | 15 | 22 | ns |

[†] The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_T_. See Figure 4.

NOTES: 4. Refer to EIA Standard RS-422-A and RS-423-A for exact conditions.

^{5.} Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

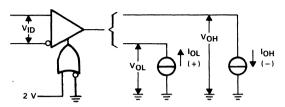
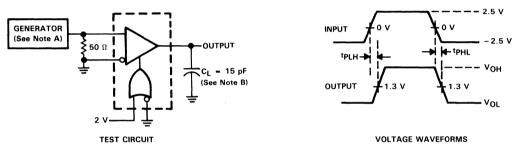


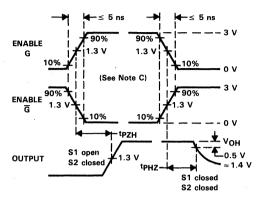
FIGURE 1. VOH, VOL

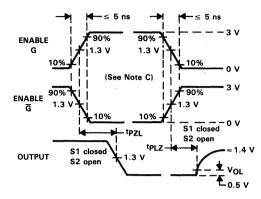


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} = 50 \Omega$, $t_f \leq 6$ ns, $t_f \leq 6$ ns.

B. C_L includes probe and jig capacitance.

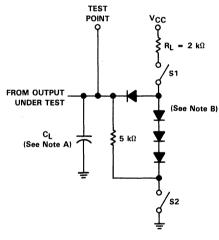
FIGURE 2. tpLH, tpHL





VOLTAGE WAVEFORMS FOR tPHZ, tPZH

VOLTAGE WAVEFORMS FOR tPLZ, tPZL



LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.

- B. All diodes are 1N3064 or equivalent.
- C. Enable G is tested with \overline{G} high; \overline{G} is tested with G low.

FIGURE 3. tpHZ, tpZH, tpLZ, tpZL

FIGURE 7

TYPICAL CHARACTERISTICS

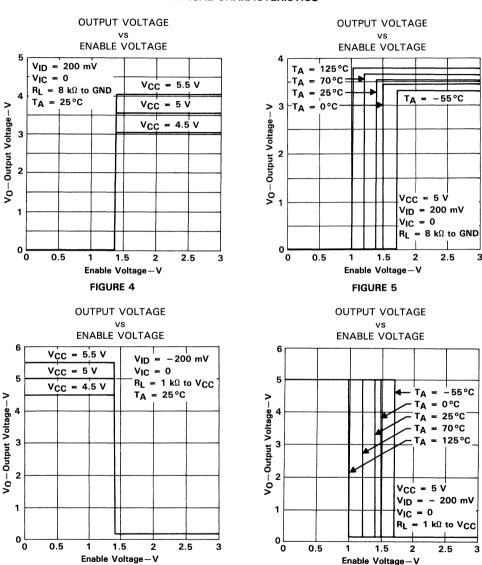
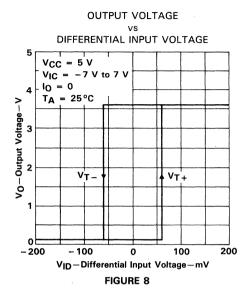
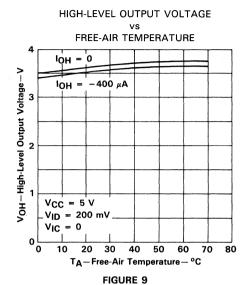
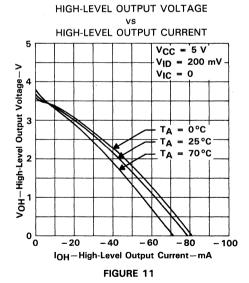


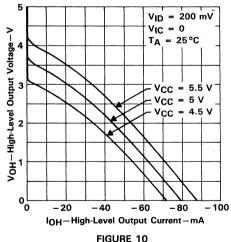
FIGURE 6





HIGH-LEVEL OUTPUT VOLTAGE HIGH-LEVEL OUTPUT CURRENT 5 $V_{IC} = 0$ TA = 25°C

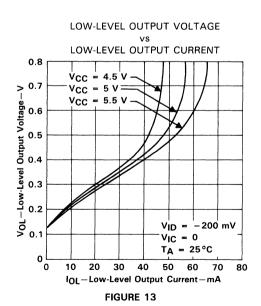


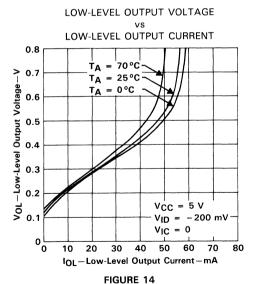


LOW-LEVEL OUTPUT VOLTAGE

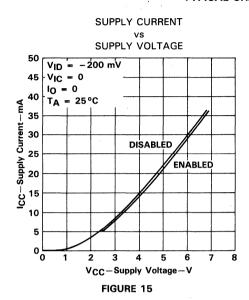
FREE-AIR TEMPERATURE 0.4 $V_{CC} = 5 V$ $V_{ID} = -200 \text{ mV}$ VOL – Low-Level Output Voltage – V $V_{IC} = 0$ $I_0 = 8 \text{ mA}$ $I_0 = 0$ o 10 30 40 50 60 70 TA-Free-Air Temperature-°C

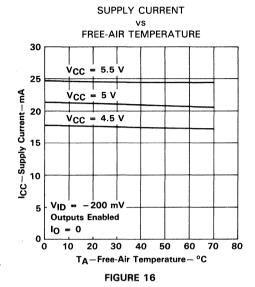
FIGURE 12

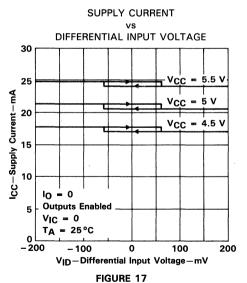


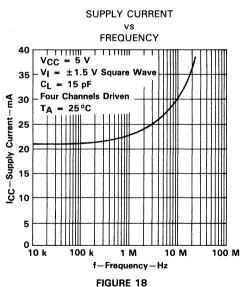


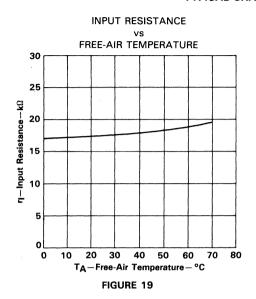


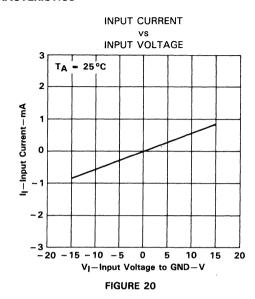












SWITCHING CHARACTERISTICS

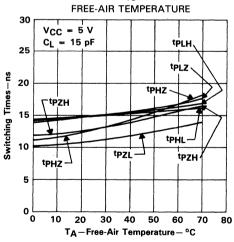


FIGURE 21

PROPAGATION DELAY TIME

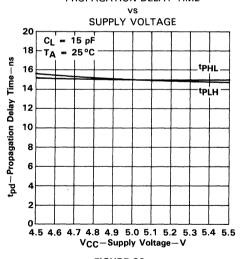


FIGURE 22

SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

D3203, JANUARY 1989

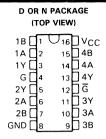
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . -7 V to 7 V
- Input Sensitivity . . . ±300 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-V Supply
- Low ICC Requirements: ICC . . . 35 mA Max
- Improved Speed and Power Consumption Compared to AM26LS32A

description

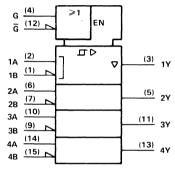
The SN75ALS197 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of CCITT Recommendations V.10, V.11, X.26, and X.27. It features three-state outputs that permit direct connection to a bus-organized system with a Fail-Safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 300 mV over a common-mode input voltage range of -7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0 °C to 70 °C.

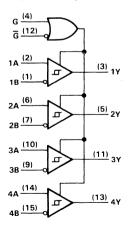


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENABLES | | OUTPUT |
|----------------------------------|---------|---|--------|
| A-B | G | G | ` Y |
| W 0.3 W | Н | Х | Н |
| V _{ID} ≥ 0.3 V | х | L | Н |
| -0.3 V < V _{ID} < 0.3 V | Н | X | ? |
| | × | L | ? |
| V 02V | Н | Х | L |
| V _{ID} ≤ -0.3 V | X | L | L |
| X | L | Н | Z |

H = high level

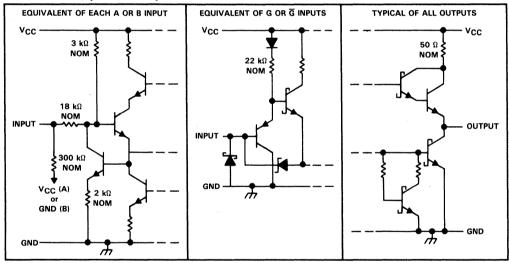
L = low level

X = irrelevant

? = indeterminate

Z = high-impedance (off)

schematics of inputs and outputs



SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage, A or B inputs |
| Differential input voltage (see Note 2) |
| Enable input voltage |
| Low-level output current |
| Continuous total dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR | T _A = 70°C POWER RATING |
|---------|---------------------------------------|--------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V _{IC} | | | ±7 | V |
| Differential input voltage, V _{ID} | | | ±12 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | V |
| High-level output current, IOH | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, TA | 0 | | 70 | °C |

SN75ALS197 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|------------------|-------------------------------------|---------------------------|-------------------------|-------------------|------|-------|------|--|
| V _{T+} | Positive-going threshold voltage | | | | | 300 | mV | |
| VT- | Negative-going threshold voltage | | | -300 [‡] | | | mV | |
| V _{hys} | Hysteresis § | | | | 120 | | mV | |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | -1.5 | V | |
| Voн | High-level output voltage | V _{ID} = 300 mV, | $I_{OH} = -400 \mu A$ | 2.7 | 3.6 | | V | |
| \/-· | Low-level output voltage | V _{ID} = -300 mV | IOL = 8 mA | | | 0.45 | V | |
| VOL | | | I _{OL} = 16 mA | | | 0.5 | | |
| 1 | High-impedance-state output current | V _{CC} = 5.25 V | V _O = 2.4 V | | | 20 | μΑ | |
| loz | | | $V_0 = 0.4 V$ | | | - 20 | μΑ | |
| 1. | Line input current | Other input at 0 V, | V _I = 15 V | | 0.7 | 1.2 | mA | |
| 11 | | See Note 3 | $V_1 = -15 \text{ V}$ | | -1.0 | - 1.7 | | |
| 1 | High-level enable-input current | | $V_{IH} = 2.7 V$ | | | 20 | μА | |
| ¹IH. | | | $V_{IH} = 5.25 V$ | | | 100 | μΑ. | |
| ΊL | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ | |
| | Input resistance | | | 12 | 18 | | kΩ | |
| 1 | Short-circuit output current | $V_{ID} = 3 V$, | V _O = 0, -15 | | 70 | 130 | mA | |
| los | | See Note 4 | | - 15 | - 78 | 130 | mA | |
| lcc | Supply current | Outputs disabled | | | 22 | 35 | mA | |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|--|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = -2.5 \text{ V to } 2.5 \text{ V, } C_L = 15 \text{ pF,}$ | | | 15 | 22 | ns |
| ^t PHL | Propagation delay time, high-to-low-level output | See Figure 2 | | | 15 | 22 | ns |
| tPZH | Output enable time to high level | C 15 - F | C F: 2 | | 13 | 25 | |
| tPZL | Output enable time to low level | C _L = 15 pF, | See Figure 3 | | 11 | 25 | ns |
| tPHZ | Output disable time from high level | C 15 -5 | C Fi 2 | | 13 | 25 | |
| ^t PLZ | Output disable time from low level | $C_L = 15 pF$, | See Figure 3 | | 15 | 22 | ns |

[†] The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTES: 3. Refer to CCITT Recommendation V.10 and V.11 for exact conditions.

^{4.} Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

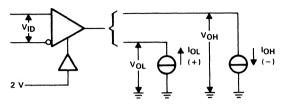
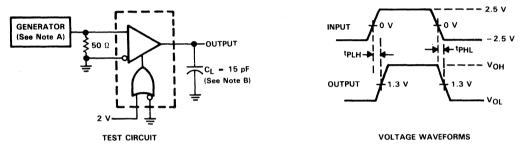


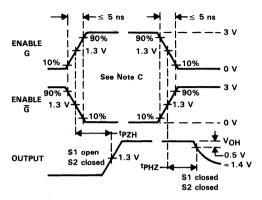
FIGURE 1. VOH, VOL

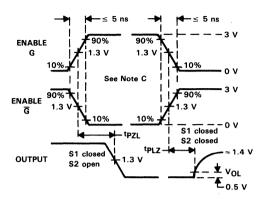


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{out} = 50 Ω , $t_r \leq$ 6 ns, $t_f \leq$ 6 ns.

B. C_L includes probe and jig capacitance.

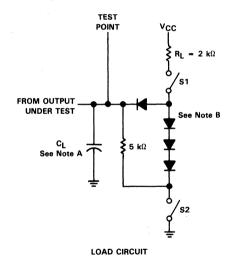
FIGURE 2. tpLH, tpHL





VOLTAGE WAVEFORMS FOR tPHZ, tPZH

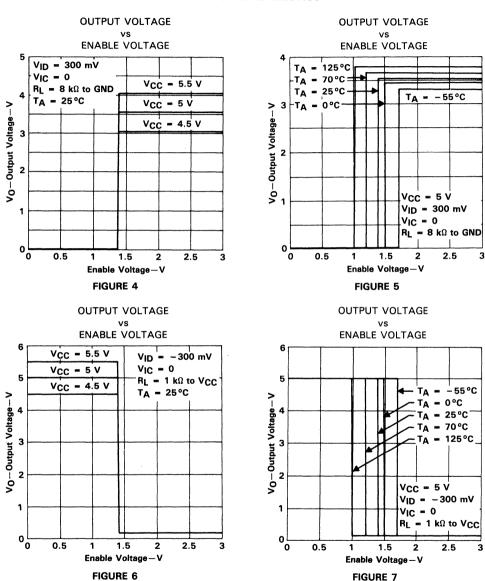
VOLTAGE WAVEFORMS FOR tPLZ, tPZL

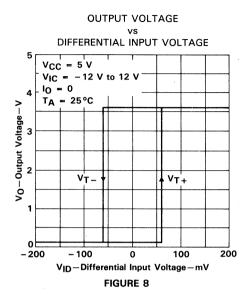


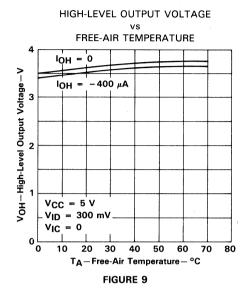
NOTES: A. C_L includes probe and jig capacitance. B. All diodes are 1N3064 or equivalent.

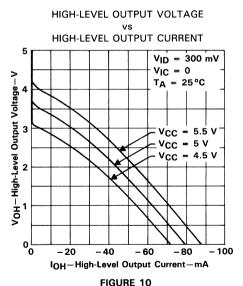
- C. Enable G is tested with G high; G is tested with G low.

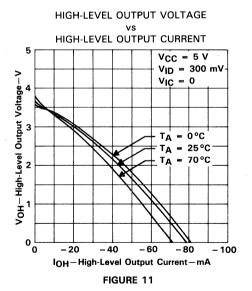
FIGURE 3. tpHZ, tpZH, tpLZ, tpZL







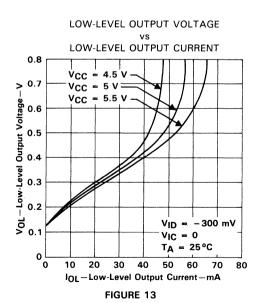


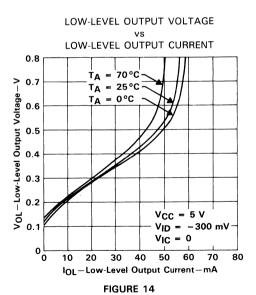


LOW-LEVEL OUTPUT VOLTAGE

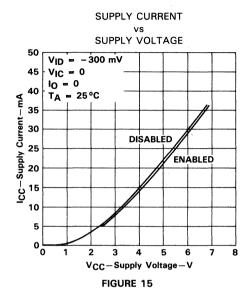
FREE-AIR TEMPERATURE 0.4 $V_{CC} = 5 V$ $V_{ID} = -300 \text{ mV}$ VOL-Low-Level Output Voltage-V VIC = 0 0.3 IO = 8 mA0.2 $I_0 = 0$ 0.1 80 30 40 50 60 70 0 TA-Free-Air Temperature-°C

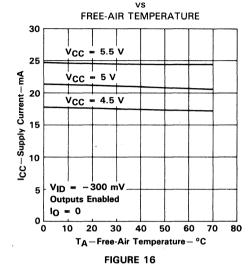
FIGURE 12



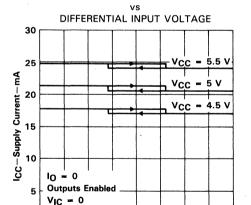


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SUPPLY CURRENT



SUPPLY CURRENT

SUPPLY CURRENT vs

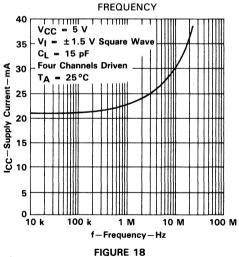


FIGURE 17

0

VID-Differential Input Voltage-mV

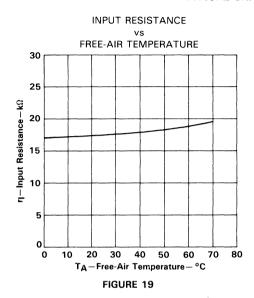
TA = 25°C

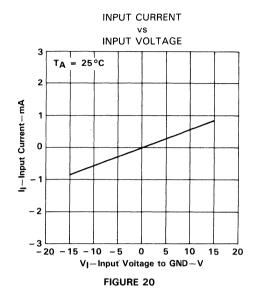
- 100

-200

200

100





SWITCHING CHARACTERISTICS

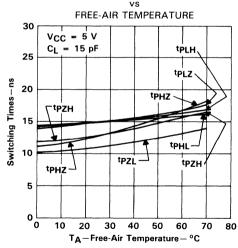


FIGURE 21

PROPAGATION DELAY TIME vs

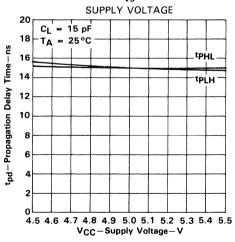


FIGURE 22

SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

D3204, JANUARY 1989

- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- 7 V to 7 V Common-Mode Range with 300-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement . . . 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

description

The SN75ALS199 is a monolithic quadruple line receiver with three-state outputs designed using Advanced Low-Power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specifications of CCITT Recommendations V.10, V.11, X.26 and X.27.

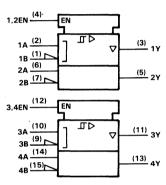
The SN75ALS199 features three-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of $\pm\,300$ mV over a common-mode input voltage range of $\pm\,7$ V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE (TOP VIEW)

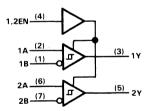
| 1B [[1 | U ₁₆ |] Vcc |
|---------------|-----------------|---------|
| 1A 🛮 2 | 15 |] 4B |
| 1Y □ 3 | 14 |] 4A |
| 1,2EN 🛮 4 | 13 |] 4Y |
| 2Y □ 5 | 12 |] 3,4EN |
| 2A ∏6 | 11 |] 3Y |
| 2B 🔲 7 | 10 |] 3A |
| GND ∏8 | 9 | ີ 3B |

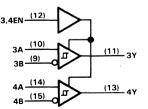
logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram







Copyright © 1986, Texas Instruments Incorporated

FUNCTION TABLE (EACH RECEIVER)

| DIFFERENTIAL | ENA | BLES | OUTPUT |
|----------------------------------|-----|------|--------|
| A-B | G | Ğ | Y |
| V 02 V | H | Х | Н |
| V _{ID} ≥ 0.3 V | Х | L | н |
| -0.3 V < V _{ID} < 0.3 V | Н | Х | ? |
| -0.3 V < VID < 0.3 V | Х | L | ? |
| V _{ID} ≤ -0.3 V | Н | Х | L |
| VID ≤ -0.5 V | Х | L | L |
| X | L | Н | Z |

H = high level

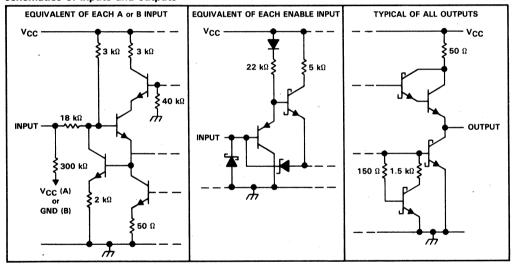
= low level

X = irrelevant

? = indeterminate

Z = high-impedance (off)

schematics of inputs and outputs



SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|--|------|
| Input voltage, A or B inputs, V _I ±1! | 5 V |
| Differential input voltage (see Note 2) | 5 V |
| Enable input voltage | 7 V |
| Low-level output current | mΑ |
| Continuous total dissipation See Dissipation Rating Ta | ıble |
| Operating free-air temperature range |)°C |
| Storage temperature range65°C to 150 |)°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |)°C |

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR | T _A = 70°C POWER RATING |
|---------|---------------------------------------|--------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | ٧ |
| Common-mode input voltage, V _{IC} | | | ±7 | ٧ |
| Differential input voltage, V _{ID} | | | ±12 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | ٧ |
| High-level output current, IOH | | | -400 | μΑ |
| Low-level output current, IOL | | | 16 | mA |
| Operating free-air temperature, TA | 0 | | 70 | ,°C |

SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|------------------|--------------------------------------|--|---|-------|------------------|-------------|------|
| VT+ | Positive-going threshold voltage | | | | | 300 | mV |
| VT- | Negative-going threshold voltage | | | -300‡ | | | mV |
| V _{hys} | Hysteresis § | | | | 120 | | mV |
| VIK | Enable-input clamp voltage | I _I = -18 mA | | | | -1.5 | ٧ |
| Voн | High-level output voltage | $V_{ID} = 300 \text{ mV},$ | $I_{OH} = -400 \mu A$ | 2.7 | 3.6 | | ٧ |
| V _{OL} | Low-level output voltage | V _{ID} = -300 mV | I _{OL} = 8 mA | | | 0.45 | ٧ |
| loz | High-impedance state output current | $V_{1L} = 0.8 \text{ V},$ $V_{O} = 2.7 \text{ V}$ | V _{ID} = −3 V, | | | 20 | μА |
| 102 | riigh-impedance state output current | $V_{IL} = 0.8 \text{ V},$ $V_{O} = 0.5 \text{ V}$ | V _{IO} = 3 V, | | | - 20 | μΑ |
| lį | Line input current | Other input at 0 V, See Note 3 | $V_{j} = 15 \text{ V}$ $V_{j} = -15 \text{ V}$ | | 0.7 -1.0 | 1.2 -1.7 | mA |
| ЧН | High-level enable-input current | , | V _{IH} = 2.7 V V _{IH} = 5.25 V | | | 20 100 | μΑ |
| IIL | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| | Input resistance | | | 12 | 18 | | kΩ |
| los | Short-circuit output current | V _{ID} = 3 V, See Note 4 | V _O = 0, | -15 | - 78 | - 130 | mA |
| Icc | Supply current | Outputs disabled | | | 22 | 35 | mA |

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|--|----------------------------------|-------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = 0 V to 3 V$, | C _L = 15 pF, | | 15 | 22 | ns |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 2 | | | 15 | 22 | ns |
| tPZH | Output enable time to high level | C. 15 - F | See Figure 3 | | 13 | 25 | |
| tPZL | Output enable time to low level | C _L = 15 pF, See Figu | | | 11 | 25 | ns |
| tPHZ | Output disable time from high level | C. 15 - F | See Figure 3 | | 13 | 25 | ns |
| tPLZ | Output disable time from low level | C _L = 15 pF, | See rigure 3 | | 15 | 22 | IIS |

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. NOTES: 3. Refer to CCITT Recommendations V.10 and V.11 for exact conditions.

^{4.} Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

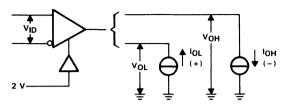
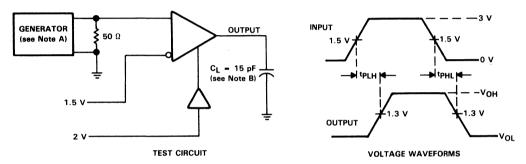


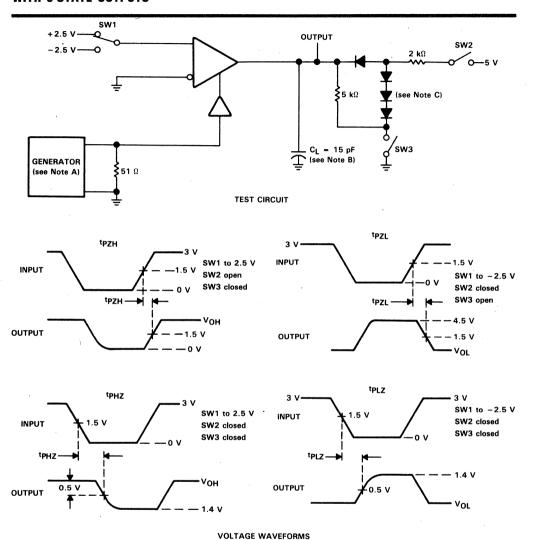
FIGURE 1. VOH, VOL



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{out} = 50 Ω , $t_f \leq$ 6 ns, $t_f \leq$ 6 ns.

B. C_L includes probe and jig capacitance.

FIGURE 2. PROPAGATION DELAY TIMES

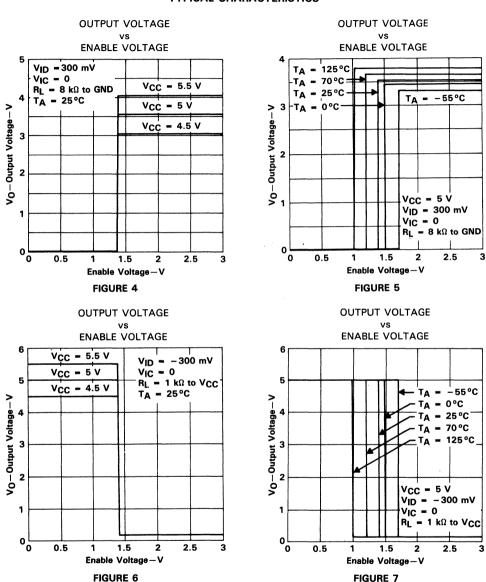


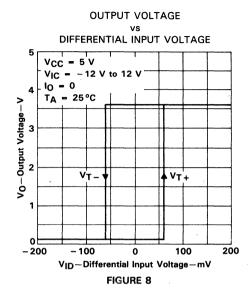
TOLINGE TIME ON

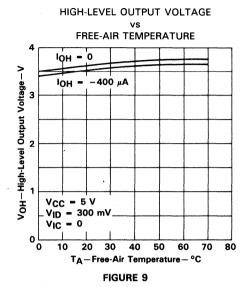
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, Z_{out} = 50 Ω , $t_f \leq$ 6 ns. $t_f \leq$ 6 ns.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or equivalent.

FIGURE 3. ENABLE AND DISABLE TIMES









HIGH-LEVEL OUTPUT VOLTAGE HIGH-LEVEL OUTPUT CURRENT 5

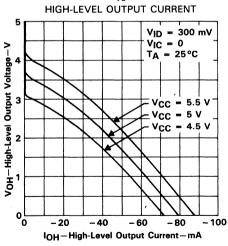
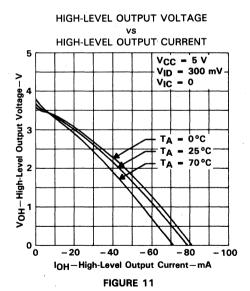


FIGURE 10



LOW-LEVEL OUTPUT VOLTAGE

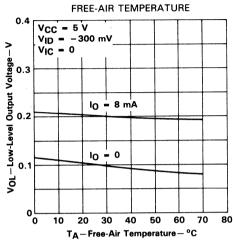


FIGURE 12



vs LOW-LEVEL OUTPUT CURRENT

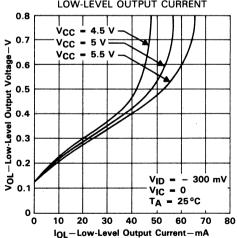


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE

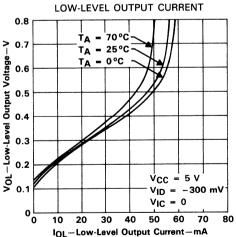
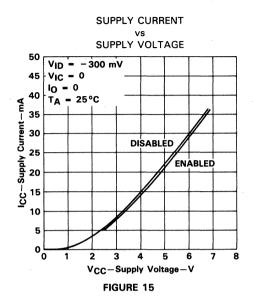
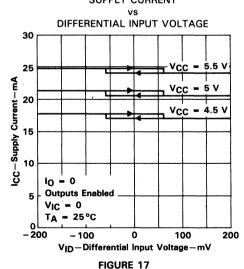


FIGURE 14









SUPPLY CURRENT

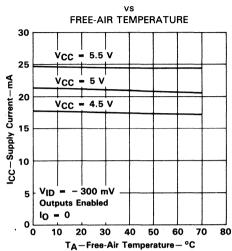
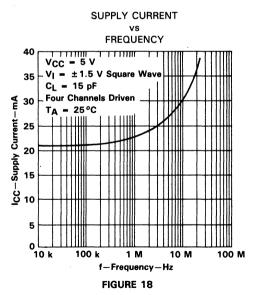
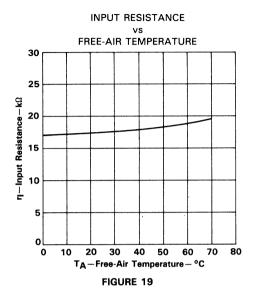
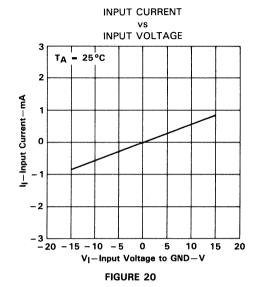


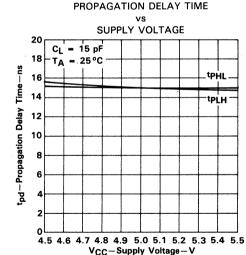
FIGURE 16

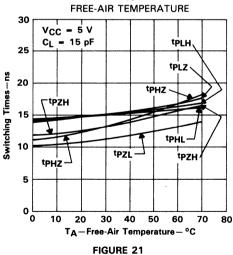






SWITCHING CHARACTERISTICS vs FREE-AIR TEMPERATURE





SN65C189, SN65C189A, SN75C189A OUADRUPLE LOW-POWER LINE RECEIVERS

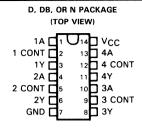
D3144, OCTOBER 1988-REVISED JULY 1990

- Meets Standard EIA-232-D (Revision of RS-232-C)
- Low Supply Current . . . 420 μA Typ
- Preset On-Chip Input Noise Filter
- Built-in Input Hysteresis
- Response and Threshold Control Inputs
- Push-Pull Outputs
- ESD Protection Exceeds 1000 V Per MIL-STD-883C, Method 3015
- Functionally Interchangeable and Pin Compatible with Texas Instruments SN75189/SN75189A, Motorola MC1489/MC489A, and National Semiconductor DS14C88A

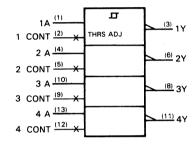
description

The SN65C189, SN65C189A, SN75C189, and SN75C189A are low-power bipolar quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform with Standard ANSI/EIA-232-D-1986, which supersedes RS-232-C.

The SN65C189 and SN75C189 have a 0.25 V typical hysteresis compared with 1 V for the SN65C189A and SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response control pins. The output is in the high logic state if the input is left open circuited or shorted to ground.

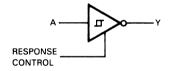


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)



These devices have an on-chip filter that rejects input pulses of shorter than $1-\mu$ s minimum duration. An external capacitor may be connected from the control pins to ground to provide further input noise filtering for each receiver.

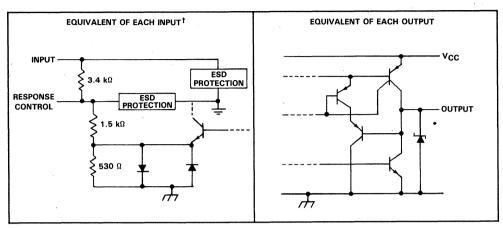
The SN65C189, SN75C189A, and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers will interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C189, SN75C189, SN65C189A, and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS or 74F logic families.

The SN65C189 and SN65C189A are characterized for operation from $-40\,^{\circ}$ C to 85 °C. The SN75C189 and SN75C189A are characterized for operation from 0 °C to 70 °C.

Texas VI

SN65C189, SN65C189A, SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

schematic of inputs and outputs



[†]All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|--|----------------------------|
| Input voltage range | 30 V to 30 V |
| Output voltage range | to V _{CC} + 0.3 V |
| Continuous total dissipation See Dissipation | ation Rating Table |
| Operating free-air temperature range: SN65C189, SN65C189A | -40°C to 85°C |
| SN75C189, SN75C189A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| DB | 525 mW | 4.2 mW/°C | 273 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|--|--------------------------------|---|------|-----|------|----------|
| Supply voltage, VCC | | | 4.5 | 5 | 6 | V |
| Input voltage, V _I (see Note 2) | | | - 25 | | 25 | V |
| High-level output current, IOH | High-level output current, IOH | | | | -3.2 | mA |
| Low-level output current, IOL | Low-level output current, IOL | | | | 3.2 | mA |
| Response control current | | | ±1 | | mA | |
| Operating free six terms are T. | SN65C189, SN65C189A | | -40 | | 85 | °C |
| Operating free-air temperature, TA | SN75C189, SN75C189A | 1 | 0 | | 70 | |

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.



SN65C189, SN65C189A, SN75C189, SN75C189A OUADRUPLE LOW-POWER LINE RECEIVERS

electrical characteristics over recommended free-air temperature range, $V_{CC} = 5 \text{ V} \pm 10\%$ (unless otherwise noted) (See Note 3)

| PARAMETERS | | TEST COND | ITIONS | MIN | TYP [†] | MAX | UNIT | |
|------------------|-------------------------|---------------------------------|---|---|------------------|------|------|-------|
| V- | Positive-going | SN75C189 | See Figure 1 | | 1 | | 1.5 | V |
| V _{T+} | threshold level | SN75C189A | See rigure 1 | | 1.6 | | 2.25 | · · |
| VT- | Negative-going | SN75C189 | See Figure 1 | | 0.75 | | 1.25 | V |
| v1- | threshold level | SN75C189A | See rigure i | | 0.75 | 1 | 1.25 | · · |
| | Input hysteresis | SN75C189 | San Eigura 1 | | 0.15 | 0.33 | | V |
| V _{hys} | input nysteresis | SN75C189A | See Figure 1 | See Figure 1 | | 0.97 | | \ \ \ |
| | | | $V_{CC} = 4.5 \text{ V to 6 V}, \qquad V_{I} = 0.75 \text{ V},$ | | 3.5 | | | |
| ∨он | High-level output vo | High-level output voltage IOH = | $I_{OH} = -20 \mu A$ | $H = -20 \mu A$ | | | | V |
| | | | $V_1 = 0.75 V$ | $V_1 = 0.75 \text{ V}, \qquad I_{OH} = -3.2 \text{ mA}$ | | | | |
| V | Low-level output vol | to a o | $V_{CC} = 4.5 \text{ V to 6 V},$ | $V_I = 3 V$, | | | 0.4 | V |
| VOL | Low-level output voi | tage | I _{OL} = 3.2 mA | | | | 0.4 | _ v |
| 1 | High-level input curr | ont | See Figure 2 | V _I = 25 V | 3.6 | | 8.3 | mA |
| lн | riigii-level input cuir | ent | See Figure 2 | V _I = 3 V | 0.43 | | 1 | IIIA |
| | Laureliane | $V_{1} = -25 \text{ V}$ | | -3.6 | | -8.3 | ^ | |
| IIL | Low-level input curre | ent. | See Figure 2 $V_1 = -3 \text{ V}$ | | -0.43 | | - 1 | mA |
| los | Short-circuit output | current | See Figure 3 | | | | - 35 | mA |
| Icc | Supply current | | V _I = 5 V, No load, See F | igure 2 | | 420 | 700 | μΑ |

 $^{^{\}dagger}$ All typical values are at $T_{A} = 25 \,^{\circ}$ C.

NOTE 3: All characteristics are measured with response control terminal open.

switching characteristics at $T_A = 25$ °C, $V_{CC} = 5$ V $\pm 10\%$

| | PARAMETERS | TEST COM | NDITIONS | MIN TYP MAX | | UNIT | |
|-------------------|--|-------------------------|--------------|-------------|--|------|----|
| tPLH | Propagation delay time, low-to-high-level output | C _L = 50 pF, | See Figure 4 | | | 6 | μS |
| tPHL | Propagation delay time high-to-low-level output | C _L = 50 pF, | See Figure 4 | | | 6 | μS |
| tTLH | Transition time, high-to-low-level output [‡] | C _L = 50 pF, | See Figure 4 | | | 500 | ns |
| ^t THL | Transition time, high-to-low-level output [‡] | C _L = 50 pF, | See Figure 4 | | | 300 | ns |
| t _{w(N)} | Duration of longest pulse rejected as noise § | C _L = 50 pF, | See Figure 4 | 1 | | 6 | μS |

[‡]Measured between 10% and 90% points of output waveform.

[§]The intent of this specification is that any input pulse of less than 1 μ s will have no effect on the output, and any pulse duration of greater than 6 μ s will cause the output to change state twice. Reaction to a pulse duration between 1 μ s and 6 μ s is uncertain.

PARAMETER MEASUREMENT INFORMATION[†]

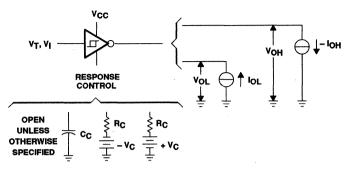
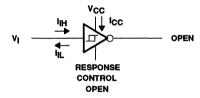


FIGURE 1. VT+, VT-, VOH, VOL



ICC is tested for all four receivers simultaneously

FIGURE 2. IIH, IIL, ICC

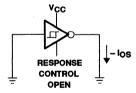
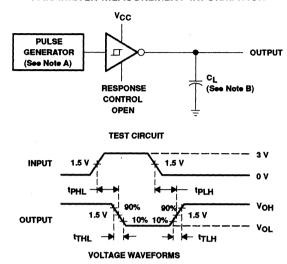


FIGURE 3. IOS

[†]Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

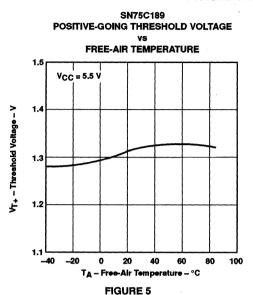
PARAMETER MEASUREMENT INFORMATION

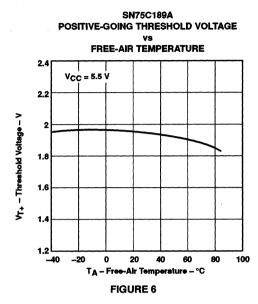


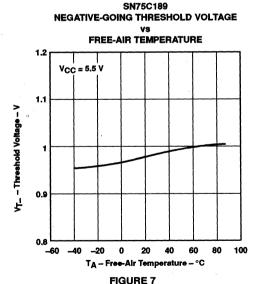
NOTES: A. The pulse generator has the following characteristics: Z₀ = 50 Ω , t_W = 25 μ s.

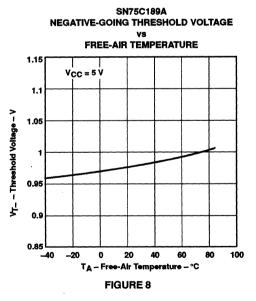
B. C_L includes probe and jig capacitances.

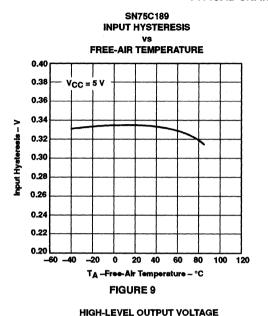
FIGURE 4. SWITCHING TIMES

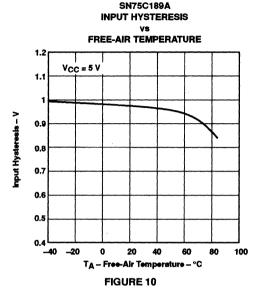












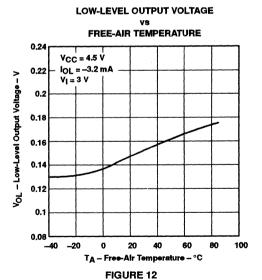
FREE-AIR TEMPERATURE 3.8 VCC = 4.5 V NOM = -3.2 mA VI = 0.75 V 3.4 NI = 0.75 V 2.8 2.8 2.8 2.8

20

T_A – Free-Air Temperature – °C FIGURE 11

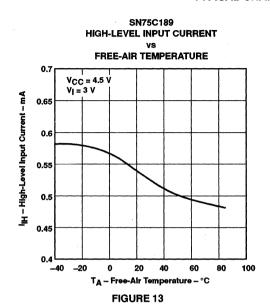
-20

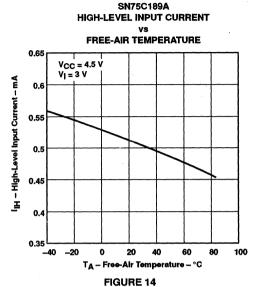
-40

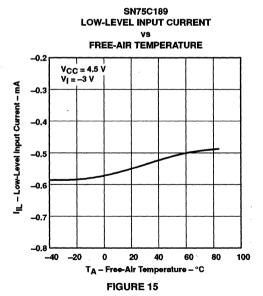


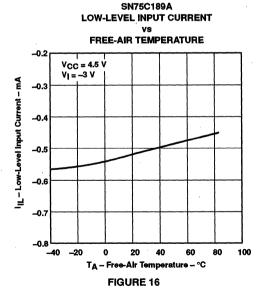
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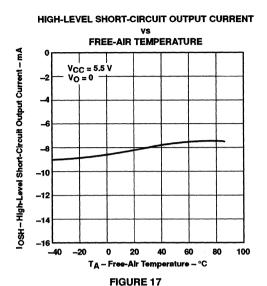
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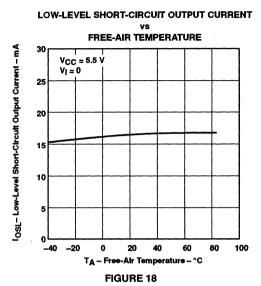


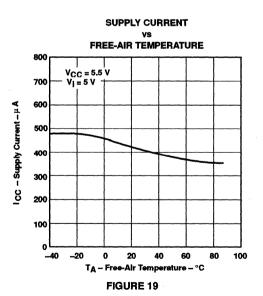


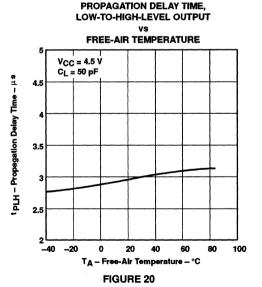


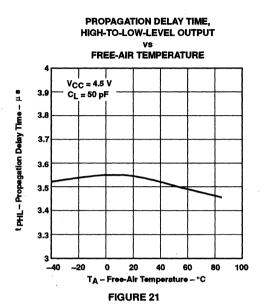


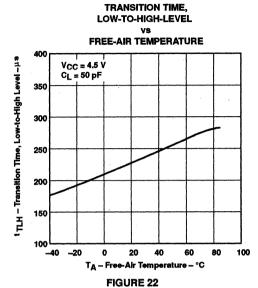




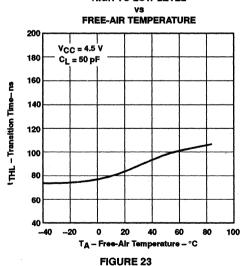








TRANSITION TIME,



D3472, JULY 1990

- Meets EIA-232-D (Revision of RS-232-C)
- Very Low Supply Current . . . 115 μA Typ
- Sleep Mode:

DS1488

- 3-State Outputs in High-Impedance State Ultra Low Supply Current . . . 17 µA Typ
- Improved Functional Replacement for: SN75188
 Motorola MC1488
 National Semiconductor DS14C88 and
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/μs
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ± 4.5 V to ± 15 V
- ESD-Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2

description

The SN65C198 and SN75C198 are monolithic low-power BI-MOS quadruple line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI/EIA-232-D-1986.

The Sleep Mode input \overline{SM} can be used to switch the outputs to high impedance, which avoids the transmission of corrupted data during power up and allows significant system power savings during data-off periods.

The SN65C198 is characterized for operation from -40°C to 85°C. The SN75C198 is characterized for operation from 0°C to 70°C.

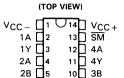
FUNCTION TABLE

| INPUTS | | | OUTPUT |
|--------|---|---|--------|
| SM | Α | В | Υ |
| Н | Н | Н | L |
| н | L | X | н |
| Н | Х | L | Н |
| L | Х | X | z |

H = high level, L = low level,

X = irrelevant,

Z = high-impedance



9 3A

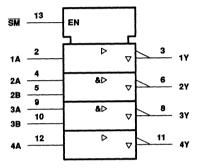
8 T 3Y

2Y [

GND ∏7

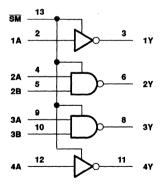
D. DB. OR N PACKAGE

logic symbol†

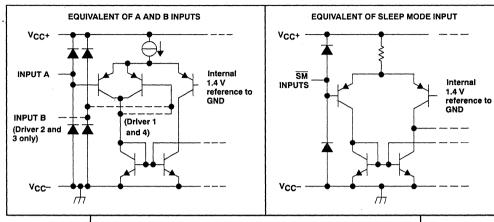


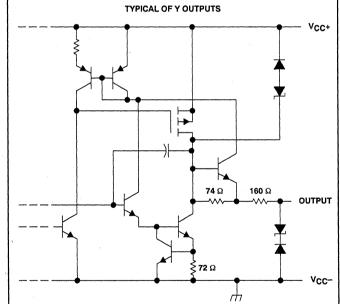
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs





All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC+} (see Note 1) | V |
|---|-----|
| Supply voltage, VCC – | i۷ |
| Input voltage range | V |
| Output voltage range | i V |
| Continuous total power dissipation See Dissipation Rating Tal | ble |
| Operating free-air temperature range: SN65C19840°C to 85 | °C |
| SN75C198 | °C |
| Storage temperature range – 65 °C to 150 | °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | |

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| DB | 525 mW | 4.2 mW/°C | 273 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT | |
|--|------|----------------|----------------------|------|------------------|------|--|
| Supply voltage, V _{CC+} | | | 4.5 | 12 | 15 | ٧ | |
| Supply voltage, V _{CC} – | | | -4.5 | - 12 | - 15 | ٧ | |
| input voltage, V _I (see Note 2) | | | V _{CC} - +2 | | V _{CC+} | V | |
| High-level input voltage, VIH | | 2 | | | ٧ | | |
| Low-level input voltage, VIL | A an | A and B inputs | | | 0.8 | V | |
| | SM i | nput. | | | 0.6 | V | |
| Operating free-air temperature, TA | | SN65C198 | -40 | | 85 | °C | |
| | | SN75C198 | 0 | | 70 | ٠ | |

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

SN65C198, SN75C198 QUADRUPLE LOW-POWER LINE DRIVER

electrical characteristics over recommended free-air temperature range, $V_{CC\pm} = \pm 12 \text{ V}$, $\overline{\text{SM}}$ at 2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT | |
|-----------|--|--|--------------------------------------|------|------------------|--------|------|--|
| V | High-level output voltage | V _{IL} = 0.8 V, | $V_{CC\pm} = \pm 5 V$ | 4 | | | V | |
| Vон | night-level output voltage | $R_L = 3 K\Omega$ | $V_{CC\pm} = \pm 12 \text{ V}$ | 10 | | | · · | |
| V | Low-level output voltage (see Note 2) | V _{IH} = 2 V, | $V_{CC\pm} = \pm 5V$ | | | -4 | V | |
| VOL | Low-level output voltage (see Note 2) | $R_L = 3 k\Omega$ | $V_{CC\pm} = \pm 12V$ | | | -10 | · · | |
| ΊΗ | High-level input current | V _I = 5 V | | | , | 10 | μΑ | |
| IIL | Low-level input current | V _I = 0 | | | | - 10 | μΑ | |
| | | | $V_0 = 12 V$, | | | 100 | | |
| | High-impedance state output current | SM at 0.6 V | $V_{CC\pm} = \pm 12 V$ | | | 100 | | |
| loz | nigh-impedance state output current | | $V_0 = -12 V$, | | -100 | | μΑ | |
| | | | $V_{CC\pm} = \pm 12 V$ | | | - 100 | | |
| Iosh | High-level short-circuit output current [‡] | V _I = 0.8 V, | $V_0 = 0$ or V_{CC} | -4.5 | - 10 | - 19.5 | mA | |
| IOSL | Low-level short-circuit output current [‡] | V ₁ = 2 V, | $V_0 = 0 \text{ or } V_{CC+}$ | 4.5 | 10 | 19.5 | mA | |
| ro | Output resistance with power off | $V_{CC\pm} = 0$, | $V_0 = -2 \text{ V to } 2 \text{ V}$ | 300 | | | Ω | |
| | , | A and B inputs at 0.8 V | $V_{CC\pm} = \pm 5 V$ | | 90 | 160 | | |
| 100 | Supply ourrent from Voc | or 2 V, no load | $V_{CC\pm} = \pm 12 V$ | | 95 | 160 | μА | |
| 100+ | Supply current from V _{CC+} | A and B inputs at 0.8 V or | $V_{CC\pm} = \pm 5 V$ | | 17 | 40 | μΛ | |
| | · · · · · · · · · · · · · · · · · · · | 2 V, R _L = $3 k\Omega$, \overline{SM} at 0.6 V | $V_{CC\pm} = \pm 12 V$ | | 17 | 40 | | |
| | Supply current from V _{CC} – | A and B inputs at 0.8 V | $V_{CC\pm} = \pm 5 V$ | | - 90 | - 160 | | |
| loo | | or 2 V, no load | $V_{CC\pm} = \pm 12 V$ | | -95 | - 160 | | |
| I'CC - | | A and B inputs at 0.8 V or | V _{CC±} = ±5 V | | -17 | - 40 | μΑ | |
| | | 2 V, $R_L = 3 k\Omega$, \overline{SM} at 0.6 V | $V_{CC\pm} = \pm 12 V$ | | - 17 | -40 | | |

[†]All typical values are at $T_A = 25$ °C.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12 \text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|--|---|--------------------------|------|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output § | | | | | 3 | μS |
| tPHL | Propagation delay time, high-to-low-level output§ | $R_L = 3 k\Omega \text{ to } 7 k\Omega$ | $C_L = 15 pF$, | | | 3.5 | μS |
| tTLH | Transition time, low-to-high-level output | See Figure 1 | | 0.53 | 1 | 3.2 | μS |
| †THL | Transition time, high-to-low-level output | | | 0.53 | 1 | 3.2 | μS |
| tTLH | Transition time, low-to-high-level output# | $R_L = 3 k\Omega \text{ to } 7 k\Omega$ | $C_L = 2500 \text{ pF},$ | | 1.5 | | μs |
| tTHL | Transition time, high-to-low-level output# | See Figure 2 | | | 1.5 | | μS |
| tPZH | Output enable time to high level | $R_L = 3 k\Omega \text{ to } 7 k\Omega$ | C _L = 15 pF, | | | 50 | μs |
| tPHZ | Output disable time from high level | See Figure 3 | | | | 10 | μs |
| ^t PZL | Output enable time to low level | $R_L = 3 k\Omega$ to $7 k\Omega$, | C _L = 15 pF, | | | 15 | μS |
| tPLZ | Output disable time from low level | See Figure 4 | | | | 10 | μS |
| SR | Output slew rate# | $R_L = 3 k\Omega \text{ to } 7 k\Omega$ | C _L = 15 pF | 6 | 15 | 30 | V/μs |

[†]All typical values are at $T_A = 25$ °C.

[‡]Not more than one output should be shorted at a time.

 $^{^{\}S}$ tpHL and tpLH include the additional time due to on-chip slew rate and are measured at the 50% points.

Measured between 10% and 90% points of output waveform.

 $^{^{\#}}$ Measured between 3-V and -3-V points of output waveform.

PARAMETER MEASUREMENT INFORMATION

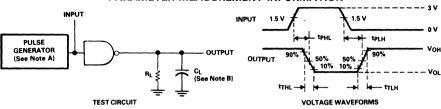


FIGURE 1. PROPAGATION AND TRANSITION TIMES

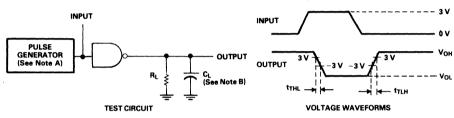


FIGURE 2. PROPAGATION AND TRANSITION TIMES

NOTE: A. The pulse generator has the following characteristics: $t_W = 25~\mu s$, PRR = 20 kHz, $Z_0 = 50~\Omega$, $t_f = t_f \le 50~ns$. B. C_L includes probe and jig capacitance.

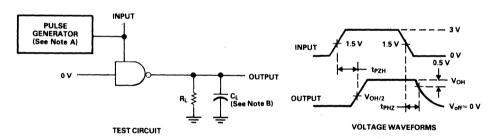


FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

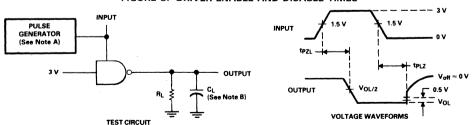
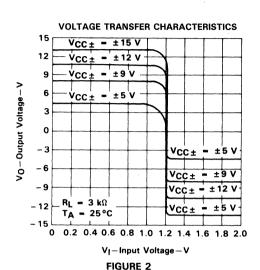


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

NOTE: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, PRR = 20 kHz, $Z_0 = 50 \Omega$, $t_f = t_f \le 50 ns$. B. C_I includes probe and jig capacitance.





SHORT-CIRCUIT OUTPUT CURRENT

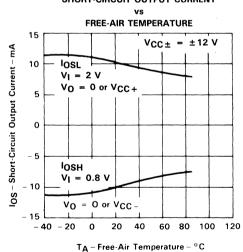
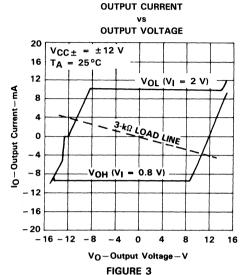
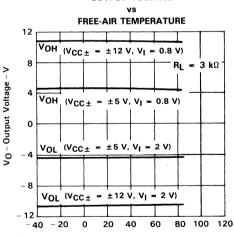


FIGURE 4

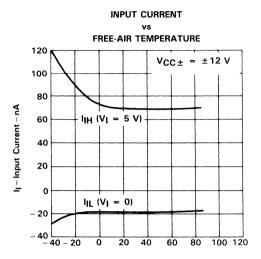


OUTPUT VOLTAGE



TA - Free-Air Temperature - °C

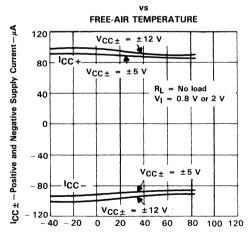
FIGURE 5



T_A - Free-Air Temperature - °C

FIGURE 6

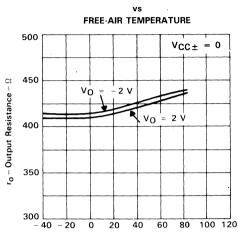
SUPPLY CURRENT



T_A - Free-Air Temperature - °C

FIGURE 8

POWER-OFF OUTPUT RESISTANCE



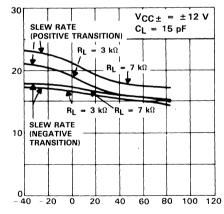
TA ~ Free-Air Temperature - °C

FIGURE 7

OUTPUT SLEW RATE

vs

FREE-AIR TEMPERATURE



TA - Free-Air Temperature - °C

FIGURE 9

SR - Ouput Slew Rate - V/µs

PROPAGATION DELAY TIME

vs FREE-AIR TEMPERATURE $R_L = 7 k\Omega$ tPHL $R_L = 3 k\Omega$ tpd - Propagation Delay Time - µs 1.5 $V_{CC\pm} = \pm 12 V$ CL = 15 pF = 3 kΩ ^tPLH = 7 kΩ 0.5 - 40 - 20 20 40 60 80 100 120

T_A - Free-Air Temperature - °C

FIGURE 10

OUTPUT ENABLE TIME TO HIGH LEVEL

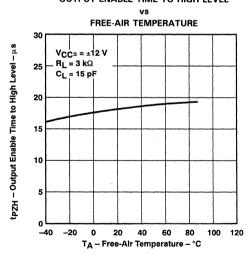
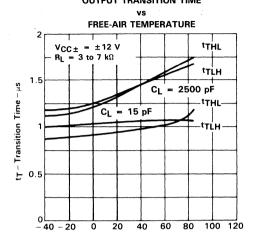


FIGURE 12

OUTPUT TRANSITION TIME



TA - Free-Air Temperature - °C

FIGURE 11

OUTPUT DISABLE TIME FROM HIGH LEVEL

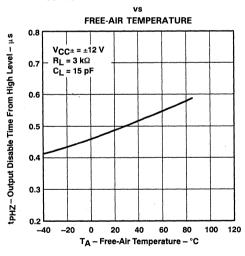


FIGURE 13

OUTPUT DISABLE TIME FROM LOW LEVEL

TYPICAL CHARACTERISTICS

OUTPUT ENABLE TIME TO LOW LEVEL FREE-AIR TEMPERATURE tPZL - Output Enable Time to Low Level - μs VCC± = ±12 V $R_L = 3 k\Omega$ 7 CL = 15 pF 3 2 -40 -20 40 60 80 100 120

FREE-AIR TEMPERATURE $t_{\mbox{\footnotesize PLZ}}-\mbox{\footnotesize Output Disable Time From Low Level}-\mbox{}\mu\mbox{\footnotesize s}$ V_{CC}± = ±12 V $R_L = 3 k\Omega$ 2.5 C_ = 15 pF 2 1.5 0.5 80 -40 -20 100 120 20 40 60 T_A - Free-Air Temperature - °C

FIGURE 15

FIGURE 14

TA - Free-Air Temperature - °C

D3272, MARCH 1989

- Bidirectional Transceiver
- Suitable for Most EIA Standards RS-422-A and RS-485 Applications
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-V Supply
- Low Power Requirements

description

The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. These transceivers are suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or VCC = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

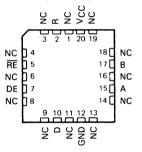


| R | <u></u> | U 8 | □vcc |
|----|---------|------------|------|
| RE | 2 | 7 | В |
| DE |]3 | 6 | DΑ |
| D | 4 | 5 | GND |

W PACKAGE

| R | T1 | U 14 | ∐ ∨cc |
|----|------------|-------------|-------|
| NC | | 13 | Пис |
| RE | □ 3 | 12 | В |
| NC | 4 | 11 | □ NC |
| DE | □ 5 | 10 | _ A |
| NC | □6 | 9 | D NC |
| D | □7 | 8 | GND |
| | | | |

FK PACKAGE



NC-No internal connection

FUNCTION TABLE (DRIVER)

| INPUT | ENABLE | OUTPUTS | |
|-------|--------|---------|---|
| D | DE | Α | В |
| Н | . н | Н | L |
| L | н | L | Н |
| X | Ł | z | Z |

FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|-----------------------------------|--------------|-------------|
| V _{ID} ≥0.2 V | L | н |
| -0.2 V <v<sub>ID<0.2 V</v<sub> | L | ? |
| V _{ID} ≤ -0.2 V | L | L |
| × | н | z |

H = high level, L = low level, ? = indeterminate,

X = irrelevant, Z = high impedance (off)



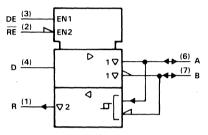
Copyright © 1989, Texas Instruments Incorporated

description (continued)

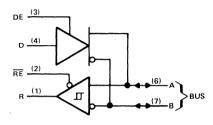
The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive-and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150 °C. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of \pm 200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from -40°C to 110°C.

logic symbol†



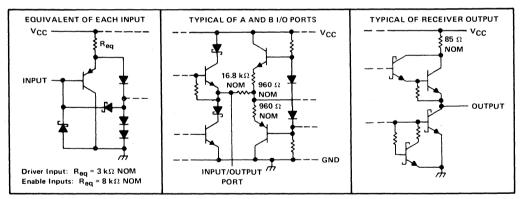
logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the JG package.

schematics of inputs and outputs.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | V |
|---|-----|
| Voltage at any bus terminal | V |
| Enable input voltage | V |
| Continuous total dissipation See Dissipation Rating Tal | ble |
| Operating free-air temperature range40°C to 110 | °C |
| Storage temperature range65°C to 150 | °C |
| Case temperature for 60 seconds: FK package | |
| Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: JG or W package 300 | °C |

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING | TA = 110°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|----------------------------|
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 440 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 546 mW | 336 mW |
| w | 1000 mW | 8.0 mW/°C | 640 mW | 520 mW | 320 mW |

recommended operating conditions

| | | MIN | TYP | MAX | UNIT |
|--|---------------------|------|-----|------|----------|
| Supply voltage, V _{CC} | | 4.75 | 5 | 5.25 | V |
| Voltage at any bus terminal (separately or comm | con model. W. or W | | | 12 | V |
| voltage at any bus terminal (separately or comin | ion mode, vi or vic | | | - 7 | ' |
| High-level input voltage, VIH | D, DE, and RE | 2 . | | | ٧ |
| Low-level input voltage, V _{IL} | D, DE, and RE | | | 0.8 | ٧ |
| Differential input voltage, V _{ID} (see Note 2) | | | | ±12 | V |
| High-level output current, IOH | Driver | | | -60 | mA |
| nigh-level output current, IOH | Receiver | | | -400 | μΑ |
| Love lovel cutout current lov | Driver | | | 60 | |
| Low-level output current, IOL | Receiver | | | 8 | mA |
| Operating free-air temperature, TA | | -40 | | 110 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST COND | DITIONS† | MIN | TYP‡ | MAX | UNIT | |
|-------------------|---|--|-----------------------|-----|------|--|------|--|
| VIK | Input clamp voltage | I _I = -18 mA | | | | - 1.5 | V | |
| ٧o | Output voltage | 10 = 0 | | 0 | | 6 | V | |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 6 | V | |
| 1/1 | Differential cutnut valence | $R_L = 100 \Omega$, | See Figure 1 | 2 | | | ٧ | |
| V _{OD2} | Differential output voltage | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | ٧ | |
| V _{OD3} | Differential output voltage | See Note 3 | | | 4 | | V | |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | , | | | ±0.2 | ٧ | |
| Voc | Common-mode output voltage | $R_L = 54 \Omega$, | See Figure 1 | | - | 3 | ٧ | |
| Δ Voc | Change in magnitude of common-mode output voltage § | | | | | ±0.2 | ٧ | |
| | • | Outputs disabled, | V _O = 12 V | | | 1 | | |
| Ю | Output current | See Note 4 | $V_0 = -7 V$ | | | 6 2.5 5 4 ±0.2 3 ±0.2 1 -0.8 20 -400 -250 -150 250 250 42 70 | mA | |
| lн | High-level input current | V ₁ = 2.4 V | | | | 20 | μΑ | |
| ΙΙΓ | Low-level input current | V _I = 0.4 V | | | | -400 | μΑ | |
| | | V _O = -7 V | | | | - 250 | | |
| los | Chart singuit quenut gurrant | V _O = 0 V _O = V _{CC} | | | | - 150 | A | |
| | Short-circuit output current | | | 250 | | mA | | |
| | | V _O = 12 V | | | | 250 | | |
| loo | Supply ourrent (total package) | No load | Outputs enabled | | 42 | 70 | mA | |
| lcc | Supply current (total package) | INU IUAU | Outputs disabled | | 26 | 6 5 ±0.2 3 ±0.2 1 -0.8 20 -400 -250 -150 250 | IIIA | |

 $^{^{\}dagger}$ The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs. ‡ All typical values are at V_{CC} = 5 V and T_A = 25 °C.

driver switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|----------------------|--------------|-----|-----|-----|------|
| tDD | Differential-output delay time | $R_1 = 54 \Omega$, | Can Figure 2 | | 15 | 22 | ns |
| tTD | Differential-output transition time | nL = 54 11, | See Figure 3 | | 20 | 30 | ns |
| ^t PZH | Output enable time to high level | $R_L = 110 \Omega$, | See Figure 4 | | 85 | 120 | ns |
| tPZL | Output enable time to low level | $R_L = 110 \Omega$, | See Figure 5 | | 40 | 60 | ns |
| tPHZ | Output disable time from high level | $R_L = 110 \Omega$, | See Figure 4 | | 150 | 250 | ns |
| tPLZ | Output disable time from low level | $R_L = 110 \Omega$, | See Figure 5 | | -20 | 30 | ns |

 $^{^{\}S}\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--|-----------------------------------|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | Vo | V _o |
| V _{OD2} | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test Termination |
| 1,40031 | | Measurement 2) |
| Δ V _{OD} | $ V_t - \overline{V}_t $ | $ V_t - \overline{V}_t $ |
| Voc | V _{os} | V _{os} |
| Δ V _{OC} | $ V_{os} - \overline{V}_{os} $ | Vos - ∇os |
| los | I _{sa} , I _{sb} | |
| Ю | ll _{xa} l, ll _{xb} l | lia, lib |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------|---|--|-------------------------|-------------------|-----|-------|------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$, | IO = 8 mA | -0.2 [‡] | | | ٧ |
| Vhys | Hysteresis [§] | | | | 50 | | mV |
| VIK | Enable-input clamp voltage | lj = −18 mA | | | | - 1.5 | . ^ |
| Voн | High-level output voltage | V _{ID} = -200 mV, See Figure 2 | $I_{OH} = -400 \mu A$ | 2.7 | | | ٧ |
| VOL | Low-level output voltage | V _{ID} = -200 mV, See Figure 2 | IOL = 8 mA, | | | 0.45 | > |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | | | | ± 20 | μΑ |
| 1. | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA |
| 11 | Line input current | See Note 5 | $V_I = -7 V$ | | | -0.8 | IIIA |
| ΊΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| IIL | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | μΑ |
| rį | Input resistance | V _I = 12 V | | 12 | | | kΩ |
| los | Short-circuit output current | | | -15 | | - 85 | mA |
| Icc | Supply current (total package) | No load | Outputs enabled | | 42 | 70 | mA |
| | Capp., cac (total package) | 1.0.000 | Outputs disabled | <u> </u> | 26 | 35 | |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

receiver switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|---------------------------------------|--------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | $V_{ID} = 0 \text{ to } 3 \text{ V},$ | | | 21 | 35 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | $C_L = 15 pF$, | See Figure 6 | | 23 | 35 | ns |
| tPZH | Output enable time to high level | C 15 -F | Can Firma 7 | | 10 | 20 | ns |
| tPZL | Output enable time to low level | $C_L = 15 \text{ pF},$ | See Figure 7 | | 12 | 20 | ns |
| tPHZ | Output disable time from high level | C ₁ = 15 pF, | See Figure 7 | | 20 | 35 | ns |
| tPLZ | Output disable time from low level | C[= 15 pr, | See rigure / | | 17 | 25 | ns |



[‡]The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§]Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage,

NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

PARAMETER MEASUREMENT INFORMATION

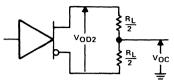


FIGURE 1. DRIVER VOD AND VOC

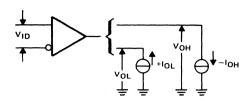


FIGURE 2. RECEIVER VOH AND VOL

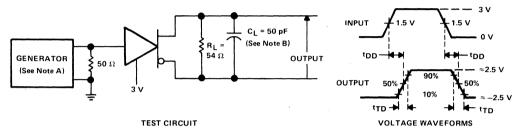


FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

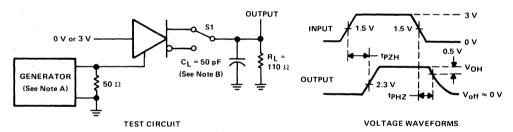


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

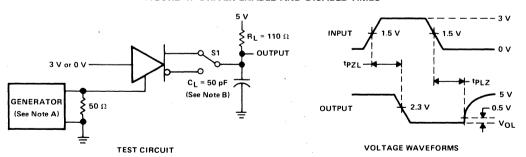


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 5 ns, $Z_0 = 50 \Omega$.
 - B. C_L includes probe and jig capacitance.
 - C. Equivalent test circuits may be substituted for actual testing.



PARAMETER MEASUREMENT INFORMATION

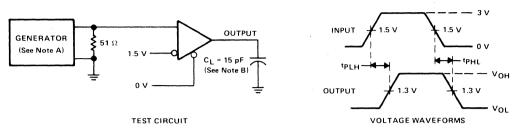


FIGURE 6. RECEIVER PROPAGATION DELAY TIMES

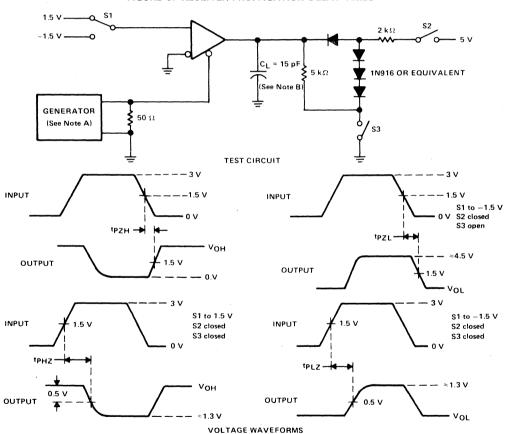
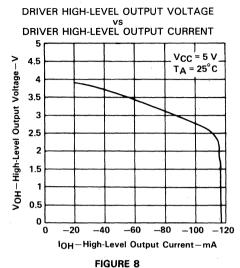


FIGURE 7. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 5 ns, $Z_0 = 50 \Omega$.
 - B. CL includes probe and jig capacitance.
 - C. Equivalent test circuits may be substituted for actual testing.



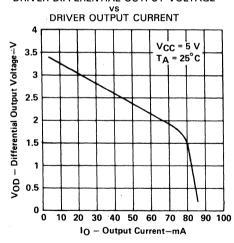
TYPICAL CHARACTERISTICS



DRIVER LOW-LEVEL OUTPUT VOLTAGE VS
DRIVER LOW-LEVEL OUTPUT CURRENT VCC'= 5 V 4.5 TA = 25°C 4 VOL -- Low-Level Output Voltage 3.5 3 2.5 2 1,5 1 0.5 0 20 40 60 80 100 120 IOL-Low-Level Output Current-mA

FIGURE 9

DRIVER DIFFERENTIAL OUTPUT VOLTAGE



TYPICAL CHARACTERISTICS

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE

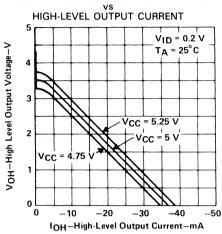


FIGURE 11

RECEIVER LOW-LEVEL OUTPUT VOLTAGE
vs
RECEIVER LOW-LEVEL OUTPUT CURRENT

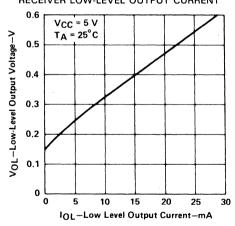


FIGURE 13

RECEIVER HIGH-LEVEL OUTPUT

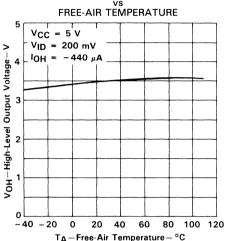


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs

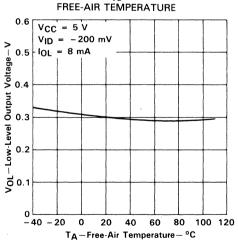
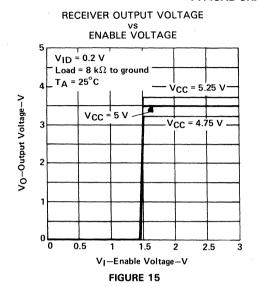
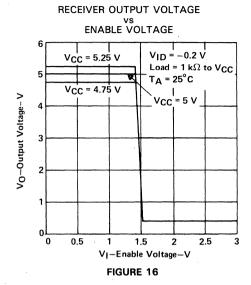


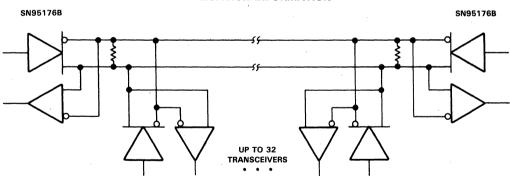
FIGURE 14

TYPICAL CHARACTERISTICS





APPLICATION INFORMATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 17. TYPICAL APPLICATION CIRCUIT

TCM78808 OCTAL ASYNCHRONOUS RECEIVER/TRANSMITTER

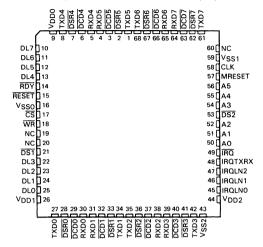
D2941, APRIL 1986-REVISED JULY 1990



Programmable Baud Rates Individually Selectable for the Transmitter/Receiver of Each Line (50 to 19,200 Baud)

- Summary Registers Allow a Single Read to Detect a Data Set Change or to Determine the Cause of an Interrupt on Any Line
- Triple Buffers for Each Receiver
- Device Scanner Mechanism Reports Interrupt Requests Due to Transmitter/Receiver Interrupts
- Independently Programmable Lines for Interrupt-Driven Operation
- Modem Status Change Detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) Signals
- Programmable Interrupts for Modem Status Changes
- Synchronizes Critical Read-Only Registers
- Replaces Eight Signetics 2661 UARTs
- Direct Second Source to DEC DC349 (78808)

FN, HA, OR HB PACKAGE (TOP VIEW-LID UP FOR HA OR HB)



NC-No internal connection

PACKAGE DESIGNATIONS

| DESCRIPTION | TI | DEC |
|-------------------|----|-----|
| Cerquad Gull-Wing | HA | GA |
| Cerquad Straight | НВ | FA |
| Plastic PLCC | FN | |

description

The TCM78808 octal asynchronous receiver/transmitter is designed for the new generations of asynchronous serial communications and for microcomputer systems. The device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines.

On-chip baud rate generation allows the designer to select and program any one of 16 rates between 50 and 19,200 baud. Baud rates are selectable for each receiver and transmitter. A built-in scanning mechanism provides an alternative to the customary polling of status registers.

The TCM78808 functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, baud rates, etc.). Each individual serial line functions as a one-line UART-type device.

An integral interrupt scanner checks for device interrupt conditions on the eight lines of the TCM78808. Its scanning algorithm is designed to give priority to receivers over transmitters. The scanner can also be programmed to check for interrupts due to changes in modem control signals (DSR and DCD).

The TCM78808 contains two types of programmable registers: line specific and summary. The six linespecific registers provide independent control of each of the eight serial lines. Two summary registers consolidate information about the current state of all eight lines and allow programs to service device interrupts quickly and efficiently.



TCM78808 OCTAL ASYNCHRONOUS RECEIVER/TRANSMITTER

Each of the eight serial data lines in the TCM78808 has a set of line-specific registers for buffering data into and out of the line and for external control of line characteristics. The receiver buffer register comprises a character assembly register plus a two-entry, first-in first-out (FIFO) buffer. The transmitter holding register provides similar functions on the output side. Information about the current state of the given line is contained in the (read-only) status register. Two mode registers control communications parameters. One mode register handles stop bits, parity, character length, and modem control interrupt enable (MCIE). The second mode register sets the incoming and outgoing baud rates. The command register controls various other functions of the given line.

The TCM78808 has a pair of summary registers that provide the current status of all eight serial data lines. This makes it possible to determine that line status has changed with a single read operation. The (read-only) interrupt summary register indicates that an interrupt has occurred and contains both the line number that generated the interrupt and the corresponding direction of flow (transmitter or receiver). With both MCIEs set and receiver interrupt enabled, the interrupt summary register will respond to changes in $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$. The data-set-change summary register monitors changes in $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ on a line-by-line basis and indicates whether a modern status change has occurred on each data line subsequent to the last time the corresponding bit was cleared.

The TCM78808 is characterized for operation from 0°C to 70°C.

| SIGNAL | DESCRIPTION | | | | |
|--|--|--|--|--|--|
| A0 THRU A5 | Address bits 0 through 5 select the internal registers in the TCM78808. | | | | |
| CLK | Clock input for timing | | | | |
| CS | Chip Select. When low, activates the TCM78808 to receive and transmit data over data lines DLO through DL7. | | | | |
| DCD0 THRU DCD7 | Data-Set Carrier Detect inputs monitor data-set carrier detect signals from modems. | | | | |
| DLO THRU DL7 | Data Lines 0 through 7 receive and transmit the parallel data. | | | | |
| DS1, DS2 | DST, DS2 Data Strobes 1 and 2 receive timing information for data transfers. The DS1 and DS2 inputs must be connected together. | | | | |
| DSRO THRU DSR7 | THRU DSR7 Data Set Ready inputs monitor data-set-ready signals from modems. | | | | |
| ĪRO | Interrupt Request output requests a processor interrupt. | | | | |
| IRQLNO THRU IRQLN2 | Interrupt Request Line number outputs indicate the line number of the originating interrupt request. | | | | |
| IRQTXRX | Interrupt Request Transmit/Receive output indicates whether an interrupt request is for transmitting or receiving | | | | |
| | data. | | | | |
| MRESET | Manufacturing Reset. For manufacturing use | | | | |
| RDY | Ready output indicates when the TCM78808 is ready to participate in data-transfer cycles. | | | | |
| RESET | Reset input initializes the internal logic. | | | | |
| RXD0 THRU RXD7 | Receive Data inputs accept asynchronous bit-serial data input streams. | | | | |
| TXD0 THRU TXD7 | Transmit Data output provides asynchronous bit-serial data output streams. | | | | |
| V _{DD0} THRU V _{DD2} | 5-V nominal power supply | | | | |
| V _{SS0} THRU V _{SS2} | Ground reference | | | | |
| WR | Write input specifies direction of data transfer on the DLO through DL7 lines. | | | | |

functional block diagram RDY-- TXDO DS1 RXD0 CHANNEL 0 WR-DSRO I/O INTERRUPT CONTROL SUMMARY DCDO DLO-DL7 REGISTER LOGIC TXD1 cs -RXD1 CHANNEL 1 RESET DSR1 - DCD1 -TXD2 ĪRQ-- RXD2 INTERRUPT CHANNEL 2 IRQLNO-IRQLN2 - DSR2 CONTROL LOGIC - DCD2 DATA SET IRQTXRX-CHANGE - TXD3 SUMMARY - RXD3 CHANNEL 3 DS2 - DSR3 ADDRESS DECODE - DCD3 A0-A5 LOGIC - TXD4 - RXD4 BAUD **CHANNEL 4** - DSR4 RATE GENERATOR - DCD4 - TXD5 - RXD5 CHANNEL 5 DSR5 CLOCK - DCD5 GENERATOR MRESET-- TXD6 - RXD6 CHANNEL 6 - DSR6 DATA BUS - DCD6 - TXD7 - RXD7 CHANNEL 7 - DSR8 CONTROL BUS - DCD8

absolute maximum ratings over operating free-air temperature range

| Supply voltage, VDD(see Note 1) | 7.V |
|---|---------------------|
| Input voltage, V _I | \dots -5 V to 7 V |
| Input current, I | -30 mA to 5 mA |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range: HA or HB package | -65°C to 150°C |
| FN package | . 0°C to 125°C |

NOTE 1: All voltage values are with respect to VSS1 and VSS2.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|------|------|
| Supply voltage, V _{DD} | 4.75 | 5. | 5.25 | V |
| High-level input voltage, V _{IH} | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5.25 V (unless otherwise noted)

| | PARA | METER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|--|--------------------------------------|--|------|------|------|
| VOH High-level output voltage | | ut voltage | $V_{DD}=4.75$ V, I_{OH} for DL0 thru DL7 = -3.5 mA, I_{OH} for all other (except \overline{IRQ} and \overline{RDY}) = -2 mA | 2.4 | | ٧ |
| V _{OL} Low-level output voltage | | ut voltage | V _{DD} = 4.75 V, I _{OL} for DL0 thru DL7 = 5.5 mA, I _{OL} for all other = 3.5 mA | | 0.4 | ٧ |
| ΊΗ | IH High-level input current | | V _I = 5.25 V | | 10 | μΑ |
| ΊL | Low-level input current | | V _I = 0 | | - 10 | μΑ |
| | Short-circuit | DLO-DL7 | | - 50 | 180 | |
| | OS output current | All other outputs except IRQ and RDY | V _{DD} = 5.25 V | - 30 | -110 | mA |
| lozh‡ | Off-state outpu | t current, ge applied | V _O = 2.4 V | | - 10 | μΑ |
| lozL‡ | OZL [‡] Off-state output current, low-level voltage applied | | V _O = 0.4 V | | 10 | μΑ |
| IDD | DD Supply current | | $V_{DD} = 5 \text{ V}, \qquad T_{A} = 25 ^{\circ}\text{C}$ | | 200 | mA |
| Ci | C _i Input capacitance | | | | 4 | pF |
| C _{io} § | Input/output ca | pacitance | | | 5 | pF |

[†] Not more than one output should be short circuited at a time, and the duration of the short should not exceed 1 second.

[‡] All 3-state output drivers are wired in an I/O configuration. The parameters include the driver and receiver input currents.

 $[\]S$ This parameter includes the capacitive loads of the output driver and the receiver input.

bus read and write timing requirements (see Figures 3 and 4)

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|-----------------|------|-----|------|
| tw1 | Pulse duration, DS1/DS2 low | WR high | 0.18 | 10 | μS |
| tw2 | Pulse duration, DS1/DS2 high | | 450 | | ns |
| tw3 | Pulse duration, DS1/DS2 low | WR low | 0.13 | 10 | μS |
| t _{su1} | Setup time, A5-A0 valid before $\overline{DS1}$ and $\overline{DS2}$ low | | 30 | | ns |
| t _{su2} | Setup time, WR high before DS1 and DS2 low | | 30 | | ns |
| t _{su3} | Setup time, $\overline{\text{CS}}$ low before $\overline{\text{DS1}}$ and $\overline{\text{DS2}}$ low | | 30 | | ns |
| t _{su4} | Setup time, DL7-DL0 valid before $\overline{\text{DS1}}$ and $\overline{\text{DS2}}$ low | | 130 | | ns |
| t _{h1} | Hold time, A5-A0 valid after $\overline{DS1}$ and $\overline{DS2}$ high | | 10 | | ns |
| t _{h2} | Hold time, $\overline{\text{WR}}$ high or low after $\overline{\text{DS1}}$ and $\overline{\text{DS2}}$ high | | 10 | | ns |
| th3 | Hold time, CS low after DS1 and DS2 high | | 10 | | ns |
| t _h 4 | Hold time, DL7-DL0 valid after DS1 and DS2 high | | 30 | | ns |
| t _V | Valid time, DL7-DL0 after $\overline{\text{DS1}}$ and $\overline{\text{DS2}}$ high | | 0 | | ns |

write switching characteristics (see Figures 3 and 4)

| | PARAMETER | TEST CONDITIONS | MIN MAX | UNIT |
|-------------------|---|-------------------------|---------|------|
| t _{en} | Enable time | C _L = 150 pF | 165 | ns |
| | | C _L = 50 pF | 50 | |
| ^t dis | Disable time | C _L = 100 pF | 60 | ns |
| | | Cլ = 150 pF | 65 | |
| t _{pd1} | Propagation delay time, from $\overline{\text{CS}}$ low to $\overline{\text{RDY}}$ low | C _L = 50 pF | 90 | ns |
| tpd2 [†] | Propagation delay time, from $\overline{\text{CS}}$ high to $\overline{\text{RDY}}$ high | C _L = 50 pF | 210 | ns |
| tpd3 | Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to DL7-DL0 valid | C _L = 150 pF | 165 | ns |
| tpd4 [†] | Propagation delay time, from $\overline{DS1}$ and $\overline{DS2}$ low to \overline{IRQ} high | C _L = 50 pF | 635 | ns |

[†]Total rise time is dependent upon internal delay plus the pull-up delay introduced by the external resistor being used. Parameter t_{pd2} is calculated from $t_{pd2} = 75$ ns + R_{CL}, and t_{pd4} is calculated from $t_{pd4} = 500$ ns + R_{CL} where R = value of the resistor that connects to C_L in Figure 1.

write timing requirements (see Figure 5)

| | | TEST CONDITIONS | MIN MAX | UNIT |
|------------------|---|------------------------|---------|------|
| fclock | Clock frequency | | 4.9152 | MHz |
| t _{w4} | Pulse duration, clock high or low | | 95 | ns |
| tw5 | Pulse duration, RESET low | | 1 | μS |
| tw6 | Pulse duration, DCD7-DCD0 and DSR7-DSR0 high or low | | 1 | μS |
| tw7 | Pulse duration, TXD7-TXD0 high or low | | 250 | ns |
| t _{su5} | Setup time, DS1 and DS2 high before RESET high | | 900 | ns |
| t _{su6} | Setup time, MRESET high before RESET low | | 250 | ns |
| ^t h5 | Hold time, DS1 and DS2 high after RESET high | | 1 | μS |
| th6 | Hold time, MRESET high after RESET high | | 250 | ns |
| ^t d1 | Delay time, IRQLN2-IRQLN0 and IRQTXRX valid to IRQ low | C _L = 50 pF | 100 | ns |
| t _{d2} | Hold time, IRQLN2-IRQLN0 and IRQTXRX valid after IRQ high | $C_L = 50 pF$ | 100 | ns |

PARAMETER MEASUREMENT INFORMATION

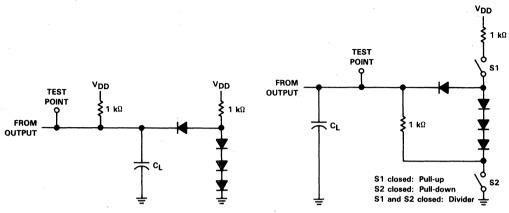


FIGURE 1. STANDARD OUTPUT LOAD CIRCUIT

FIGURE 2. 3-STATE OUTPUT LOAD CIRCUIT

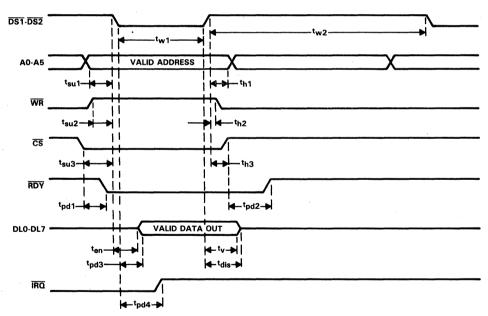
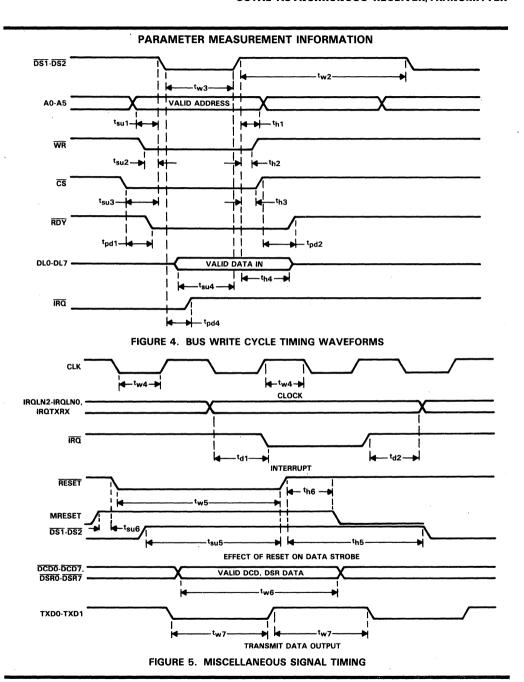
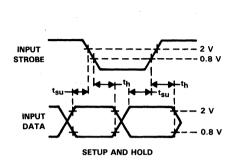


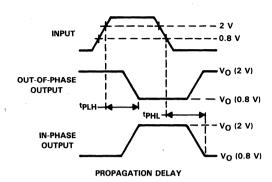
FIGURE 3. BUS READ CYCLE TIMING WAVEFORMS





PARAMETER MEASUREMENT INFORMATION





NOTE: $t_{pd} = t_{PLH}$ or t_{PHL}

FIGURE 6. VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

electrical operation

data and address

data lines (DL7 through DL0)

These lines are used for the parallel transmission and reception of data between the CPU and the TCM78808. The receivers are activated by the data strobe $(\overline{DS1}, \overline{DS2})$ signal. The output drivers are active only when the chip select (\overline{CS}) signal is low (active), the data strobe $(\overline{DS1}, \overline{DS2})$ signal goes low (active), and the write (\overline{WR}) signal is high (inactive). The drivers will become inactive (high impedance) within 50 ns when one or more of the following occurs: the chip select (\overline{CS}) signal goes high, the data strobe $(\overline{DS1}, \overline{DS2})$ goes high, or the write (\overline{WR}) signal goes low.

address lines (A5 through A0)

These lines select which internal register is accessible through the data I/O lines (DL7 through DL0) when the data strobe ($\overline{DS1}$, $\overline{DS2}$) and chip select (\overline{CS}) signals are low. Table 1 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the (\overline{WR}) signal is high, the address accesses the receiver buffer register. When \overline{WR} is low, it accesses the transmitter holding register.

TABLE 1. TCM78808 REGISTERS ADDRESS SELECTION

| ADDRESS LINE† | | | | ŧ | | READ/ | |
|---------------|----|----|-----|----|----|------------|-------------------------------|
| A5 | Α4 | АЗ | A2 | Α1 | ΑO | WRITE | REGISTER |
| L | L | L | L | L | L | Read | Line O Receiver Buffer |
| L | L | L | L | L | L | Write | Line 0 Transmitter Holding |
| L | L | L | L | L | н | Read | Line 0 Status |
| L | L | L | L | Н | L | Read/Write | Line 0 Mode Registers 1 and 2 |
| L | L | L | L | Н | н | Read/Write | Line 0 Command |
| L | L | Н | L | L | L | Read | Line 1 Receiver Buffer |
| L | L | Н | L | L | L | Write | Line 1 Transmitter Holding |
| L | Ł | н | L | L | н | Read | Line 1 Status |
| L | L | н | L | Н | L | Read/Write | Line 1 Mode Registers 1 and 2 |
| L | L | н | L | Н | Н | Read/Write | Line 1 Command |
| L | Н | L | L | L | L | Read | Line 2 Receiver Buffer |
| L | н | L | L | L | L | Write | Line 2 Transmitter Holding |
| L | н | L | L | L | Н | Read | Line 2 Status |
| L | Н | L | L | Н | L | Read/Write | Line 2 Mode Registers 1 and 2 |
| L | Н | L | L | Н | Н | Read/Write | Line 2 Command |
| L | Н | Н | L | L | L | Read | Line 3 Receiver Buffer |
| L | Н | Н | L | L | L | Write | Line 3 Transmitter Holding |
| L | Н | Н | L | L | Н | Read | Line 3 Status |
| L | Н | Н | L | Н | L | Read/Write | Line 3 Mode Registers 1 and 2 |
| L | Н | Н | L | Н | Н | Read/Write | Line 3 Command |
| Н | L | L | L | L | L | Read | Line 4 Receiver Buffer |
| Н | L | L | L | L | L | Write | Line 4 Transmitter Holding |
| н | L | L | L | L | Н | Read | Line 4 Status |
| н | L | L | L | Н | L | Read/Write | Line 4 Mode Registers 1 and 2 |
| Н | L | L | L | Н | Н | Read/Write | Line 4 Command |
| Н | L | Н | L | L | L | Read | Line 5 Receiver Buffer |
| Н | L | Н | L | L | L | Write | Line 5 Transmitter Holding |
| Н | L | Н | L | L | H | Read | Line 5 Status |
| Н | L | Н | L | Н | L | Read/Write | Line 5 Mode Registers 1 and 2 |
| Н | L | Н | L | Н | Н | Read/Write | Line 5 Command |
| Н | Н | L | L | L | L | Read | Line 6 Receiver Buffer |
| Н | Н | L | L | L | L | Write | Line 6 Transmitter Holding |
| Н | Н | L | L | L | Н | Read | Line 6 Status |
| Н | Н | L | · L | Н | L | Read/Write | Line 6 Mode Registers 1 and 2 |
| Н | Н | L | L | Н | Н | Read/Write | Line 6 Command |
| Н | Н | Н | L | L | L | Read | Line 7 Receiver Buffer |
| Н | Н | Н | Ļ | L | L | Write | Line 7 Transmitter Holding |
| Н | Н | Н | L | L | Н | Read | Line 7 Status |
| Н | Н | Н | L | Н | L | Read/Write | Line 7 Mode Registers 1 and 2 |
| Н | Н | Н | L | Н | Н | Read/Write | Line 7 Command |
| X | X | Х | Н | L | L | Read | Interrupt Summary |
| X | X | X | Н | L | Н. | Read | Data Set Change Summary |

[†]X = Either L or H



bus transaction control

chip select (CS)

This signal, when low, permits data transfers through the DL7 through DL0 lines to or from the internal registers. Data transfer is controlled by the data strobe $(\overline{DS1}, \overline{DS2})$ signal and the write (\overline{WR}) signal.

data strobe (DS1, DS2)

The data strobe inputs (DS1 and DS2) must be connected together. This input receives timing information for data transfers. During a write cycle, the CPU activates the data strobe signal when valid output data is available and deactivates the data strobe signal before the data is removed. During a read cycle, the CPU activates the data strobe signal, and the TCM78808 transfers the valid data.

When the data strobe signal is high, the DL7 through DL0 lines are in a high-impedance state.

write (WR)

The write (WR) signal specifies the direction of data transfer on the DL7 through DL0 pins by controlling the direction of their transceivers. If the WR signal is low during a data transfer (with the CS, DS1, and DS2 signals also low), the TCM78808 receives data from DL7 through DL0. If the WR signal is high during a write data transfer, the TCM78808 drives data onto the DL7 through DL0 lines.

interrupt request (IRQ)

The \overline{IRQ} output is an active-low, open-drain output. The integral interrupt scanner drives the \overline{IRQ} signal low when it has detected an interrupt condition on one of the eight serial data lines.

interrupt request transmit/receive (IRQTxRx)

This signal indicates when the interrupt scanner stops and activates \overline{IRQ} because of a transmitter interrupt condition (IRQTxRx = H) or because of a receiver interrupt condition (IRQTxRx = L). The signal is valid only while the \overline{IRQ} signal is low. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

interrupt request line number (IRQLN2 through IRQLN0)

These lines indicate the line number at which the TCM78808 interrupt scanner stopped and activated the interrupt request (\overline{IRQ}) signal. The number on these lines is valid only while the \overline{IRQ} signal is low. Line IRQLN2 is the high-order bit, and the IRQLN0 line is the low-order bit.

The state of these signals also appears as bits in the interrupt summary register: IRQLN2 as bit 3, IRQLN1 as bit 2, and IRQLN0 as bit 1. Table 2 shows the line numbers corresponding to settings of IRQLN2 through IRQLN0.

TABLE 2. TCM78808 INTERRUPT REQUEST LINE INDICATIONS

| IRQLN2 | IRQLN1 | IRQLNO | INTERRUPT REQUEST LINE NUMBER |
|--------|--------|--------|-------------------------------|
| L | L | L | 0 |
| L | L | н | . 1 |
| L | н | L | 2 |
| L | н | н | 3 |
| Н | L | L | 4 |
| н | L | н | 5 |
| н | н | L | 6 |
| Н | н | н | 7 |

serial data

transmit data (TXD7 through TXD0)

These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and at a low level when the TxBRK bit in the command register of the associated line is set.

receive data (RXD7 through RXD0)

These lines accept asynchronous bit-serial data streams. The input signals must remain at the high level for at least one-half bit time before a high-to-low transition is recognized. A high-to-low transition is required to signal the beginning of a start bit and initiate data reception.

modem signals

data set ready (DSR7 through DSR0)

These eight inputs, one for each serial data line on the TCM78808, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a \overline{DSR} pin causes the \overline{DSR} bit (bit 7) in the status register of the corresponding line to be activated. A TTL high at a \overline{DSR} pin causes the \overline{DSR} bit in the status register of the corresponding line to be inactive. A change of this input from high to low or low to high causes the activation of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one level to the other and back again that occur within 1 μ s may not be detected.

carrier detect (DCD7 through DCD0)

These eight inputs, one for each serial data line of the TCM78808, are typically connected through intervening level converters to the received-line-signal-detect (also called carrier-detect) outputs of modems. A TTL low at a \overline{DCD} input causes the \overline{DCD} bit of the corresponding line status register to be deactivated. A change of this input from high to low or low to high causes the activation of the data-set-change (DSCHNG) bit that corresponds to this line in the data-set-change summary register. Changes from one level to the other and back again that occur within 1 μ s may not be detected.

general control signals

ready (RDY)

The \overline{RDY} output is an open-drain output. Upon detecting a negative transition of \overline{CS} , the TCM78808 activates the \overline{RDY} signal to indicate readiness to take part in data transfer cycles. The \overline{RDY} signal deactivates on the trailing edge of \overline{CS} .

reset (RESET)

When the RESET input goes low, the TxD7 through TxD0 lines are low, and all internal status bits listed in the Architecture Summary paragraph are cleared.

manufacturing reset (MRESET)

This signal is for manufacturing use only. The input should be connected to ground for normal operation.

clock signals

clock input (CLK)

All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz $\pm 0.1\%$, and duty cycle is 50 $\pm 5\%$.

architecture summary

line-specific registers

Each of the eight serial data lines has a set of registers for buffering data into and out of the line and for external control of the line characteristics. These registers are selected for access by setting the appropriate address on lines A5 through A0. Lines A5 through A3 select one of the eight data lines. Lines A2 through A0 select the specific register for that line. Refer to Table 1 for the register address assignments.

receiver buffer register

Each line receiver consists of a character-assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line command register is set, received characters are moved automatically into the line receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The activation of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{\text{IRQ}}$ signal is low). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{\text{IRQ}}$ signal is high), and the interrupt scanner resumes operation.

If there is another entry in a line FIFO, the RxRDY bit remains active. When the interrupt scanner reaches this line again, the activation of RxRDY causes the scanner to halt and generate another interrupt (IRO goes low).

The RESET signal clears the RxEN bit and initializes the receiver logic. The RxRDY flag is cleared, and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.



transmitter holding register

Each line has a transmitter holding register that can be written to. When the TxEN bit in the line command register is set and the serialization logic becomes idle, characters are automatically moved from the output of this register into the transmitter serialization logic.

When this register is empty, the TxRDY bit in the line status register is set. If the transmitter interrupt enable (TxIE) bit in the line command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared, and the scanner resumes operation.

The RESET signal also initializes the transmitter logic. The TxRDY flag is cleared, and the transmitter holding register contents are lost. The transmitter enable (TxEN) bit in the line command register is also cleared by RESET. Software clearing of TxEN alone produces results different from the full RESET in that the transmitter holding register contents are not lost. They are transmitted when TxEN is set again.

status register

Each line has a read-only status register that provides information about the current state of the given line. This register indicates the readiness of a line for transmission or reception of data and flags error conditions in its bit fields. Figure 7 shows the format of the status register. Table 3 lists the flag bits in each register.

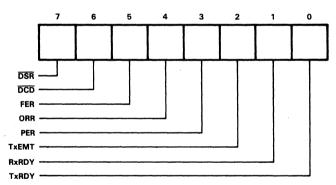


FIGURE 7. TCM78808 STATUS REGISTERS (LINE 0 THROUGH 6) FORMAT

TABLE 3. TCM78808 STATUS REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

| BIT | DESCRIPTION | | | | | | |
|-----|---|--|--|--|--|--|--|
| 7 | DSR (Data Set Ready). This bit is the inverted state of the DSR line. | | | | | | |
| 6 | DCD (Data Set Carrier Detect). This bit is the inverted state of the DCD line. | | | | | | |
| 5 | FER (Frame Error). Set when the received character currently displayed in the receiver buffer register was not framed by a stop | | | | | | |
| | bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register | | | | | | |
| | that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing | | | | | | |
| | RxEN (bit 2) of the command register, by RESET, or by setting the reset error RERR (bit 4) of the command register. | | | | | | |
| 4 | ORR (Overrun error). Set when the character in the receiver buffer was not read before another character was received. Cleared | | | | | | |
| | by clearing RxEN (bit 2) of the command register, by RESET, or by setting reset error RERR (bit 4) of the command register. | | | | | | |
| 3 | PER (Parity Error). If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect | | | | | | |
| | parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by RESET, by setting reset error RERR (bit 2) | | | | | | |
| | of the command register, or by reading the current character in the receiver buffer register. | | | | | | |
| 2 | TxEMT (Transmitter Empty). Set when the transmitter serialization logic for the associated line has completed transmission of | | | | | | |
| | a character, and no new character has been loaded into the transmission holding register. Cleared by loading the transmitter | | | | | | |
| | holding register, by clearing TxEN(0) of the command register, or by RESET. | | | | | | |
| 1 | RxRDY (Receiver Buffer Ready). When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared | | | | | | |
| | by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by RESET. | | | | | | |
| 0 | TxRDY (Transmitter Holding Register Ready). When set, this bit indicates that the transmitter holding register is empty. Cleared | | | | | | |
| | when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by | | | | | | |
| 1 | clearing TxEN (bit 0) in the command register, or RESET. This bit is initially set when the transmitter logic is enabled by the setting | | | | | | |
| | of the TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback | | | | | | |
| | modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared. | | | | | | |

mode registers 1 and 2

These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the eight communications lines has two of these registers, both accessed by the same address on A5 through A0. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1. The pointer is reset to point to mode register 1 by RESET or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 8 shows the format of mode registers 1, and Table 4 describes the function of the register information.

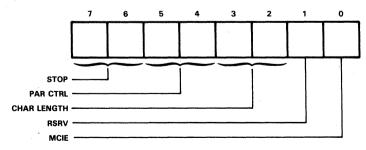


FIGURE 8. TCM78808 MODE REGISTERS 1 (LINE 0-6) FORMAT



TABLE 4. TCM78808 MODE REGISTERS 1 (LINES 0 THROUGH 6) DESCRIPTION

| BIT | | DESCRIPTION | | | | | | | | |
|-----|-------------|---|---------------------|--|--|--|--|--|--|--|
| 7,6 | STOP. The | STOP. These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits | | | | | | | | |
| | are cleare | by RESE | ⊺. | | | | | | | |
| | Bit 7 | Bit 6 | Stop Bits | | | | | | | |
| | L | L | Invalid | | | | | | | |
| ĺ | L | Н | 1.0 | • | | | | | | |
| ĺ | Н | L | 1.5 | | | | | | | |
| Ĺ | н | Н | 2.0 | | | | | | | |
| 5,4 | PAR CTRI | (Parity co | ntrol). These bit | s determine parity as follows and are cleared by $\overline{\text{RESET}}$. (X = either H or L) | | | | | | |
| | Bit 5 | Bit 4 | Parity Type | | | | | | | |
| 1 | н | н | Even | • | | | | | | |
| | L | Н | Odd | | | | | | | |
| | Х | L | Disabled | | | | | | | |
| 3,2 | CHARLEN | IGTH (Char | acter length). Th | ese bits determine the length (excluding start bit, parity, and stop bits) of the characters | | | | | | |
| | received a | nd sent. R | eceived characte | rs of less than 8 bits are "right aligned" in the receiver buffer with unused high-order | | | | | | |
| | bits equal | to zero. Par | ity bits are not sh | own in the receiver buffer. The character length bits are cleared by RESET. The character | | | | | | |
| | length bits | s are define | ed as follows: | | | | | | | |
| | Bit 3 | Bit 2 | Bit Length | | | | | | | |
| 1 | L | Ł | 5 | | | | | | | |
| | L | н | 6 | | | | | | | |
| | Н | L | 7 | | | | | | | |
| | Н | Н | 8 | , | | | | | | |
| 11 | RSRV. Re | served and | cleared by RES | ET. | | | | | | |
| 0 | MCIE (Mo | dem contro | l interrupt enable |). When set and RxIE (bit 5) of the command register is set, the modem control interrupts | | | | | | |
| | are enable | d. Refer to | the interrupt S | canner and Interrupt Handling information. Cleared by RESET. | | | | | | |

Figure 9 shows the format of mode registers 2, and Table 5 indicates the baud rate selections of the register. Bits 7 through 4 of mode register 2 control the transmitter baud rate, and bits 3 through 0 control the receiver baud rate. These registers are cleared by RESET.

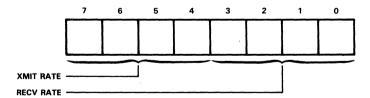


FIGURE 9. TCM78808 MODE REGISTERS 2 (LINE 0 THROUGH 6) FORMAT

TABLE 5. TCM78808 MODE REGISTERS 2 (LINES 0 THROUGH 6) DESCRIPTION

| BIT | | | | | | 0 | ESCI | RIPTIO | N · | | |
|-----|-------|--------|---------|--------|-----------|-------|-------|---------|----------------|-------------|-----------|
| 7-0 | XMI | T RAT | E/REC | V RAT | E (Transi | nitte | r/Rec | eiver F | Rate), Selects | the baud ra | te of the |
| | trans | smitte | r (bits | 7 thro | ugh 4) ar | nd re | ceive | r (bits | 3 through 0) | as follows: | |
| | Т | ransm | itter E | Bits | R | eceiv | er Bi | ts | Nominal | Actual | Error † |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Rate | Rate | (percent) |
| | L | L | L | L | L | L | L | L | 50 | same | |
| | L | L | L | н | L | L | L | Н | 75 | same | |
| | L | L | Н | L | L | L | Н | L | 110 | 109.09 | 0.826 |
| | L | L | н | Н | L | L | Н | Н | 134.5 | 133.33 | 0.867 |
| 1 | L | Н | L | L | L | Н | L | Ļ | 150 | same | |
| | L | Н | L | Н | L | Н | L | н | 300 | same | |
| | L | Н | н | L | L | Н | Н | L | 600 | same | **** |
| | L | Н | Н | Н | L | Н | Н | н | 1200 | same | |
| | н | L | L | L | Η, | L | Ł | Ľ | 1800 | 1745.45 | 3.03 |
| | н | L | L | Н | н | L | L | Н | 2000 | 2021.05 | 1.05 |
| | н | L | н | L | н | L | н | L | 2400 | same | |
| | н | L | Н | н | н | L | Н | Н | 3600 | 3490.91 | 3.03 |
| | н | Н | L | L | н | · H | L | L | 4800 | same | - |
| | н | Н | L | н | н | Н | L | н . | 7200 | 6981.81 | 3.03 |
| 1 | н | н | н | L | н | Н | Н | L | 9600 | same | |
| | Н | н | н | н | Н | Н | Н | Н | 19200 | same | |

[†]. The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1%. This variance results in an error that must be added to the error listed in the error column.

command register

These read/write registers control various functions on the selected line. Figure 10 shows the format of the command registers, and Table 6 describes the function of the register information.

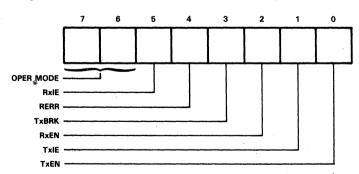


FIGURE 10. TCM78808 COMMAND REGISTERS (LINE 0 THROUGH 6) FORMAT

TABLE 6. TCM78808 COMMAND REGISTERS (LINES 0 THROUGH 7) DESCRIPTION

| BIT | DESCRIPTION | | | | | |
|----------|---|--|--|--|--|--|
| 7,6 | OPER MODE (Operation Mode). These bits control the operating mode of the channel as follows. These bits are cleared by RESET. | | | | | |
| | Bit 7 Bit 6 Operating Mode | | | | | |
| Ì | L L Normal operation | | | | | |
| ì | L H Automatic echo | | | | | |
| 1 | H L Local loopback | | | | | |
| , | H H Remote loopback | | | | | |
| 5 | RxIE (Receiver Interrupt Enable). When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt. | | | | | |
| 4 | RERR (Reset Error). When set, this bit clears the framing error, overrun error, and parity error of the status register associated | | | | | |
| | with this line. This bit is cleared by RESET. It is not self-clearing. | | | | | |
| 3 | TxBRK (Transmit Break). When set, this bit forces the appropriate TxD7-TxD0 line to the spacing state at the conclusion of | | | | | |
| 1 | the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character | | | | | |
| İ | pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length | | | | | |
| 1 | obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between | | | | | |
| | the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by RESET. | | | | | |
| 2 | RxEN (Receiver Enable). When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received | | | | | |
| 1 | character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions | | | | | |
| <u> </u> | associated with this line, and initializes all receiver logic. This bit is cleared by RESET. | | | | | |
| 1 | TxIE (Transmit Interrupt Enable). When set, the state of the associated TxRDY flag (bit 0) of the status register is made available | | | | | |
| ł | to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is set and, | | | | | |
| | if so, generates an interrupt. | | | | | |
| 0 | TxEN (Transmitter Enable). When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the | | | | | |
| İ | characters that follow, but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the | | | | | |
| | status register, clears any transmitter interrupt conditions associated with the transmitter holding register, and initializes all | | | | | |
| | transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register | | | | | |
| L | is retained so that XON/XOFF situations can be properly processed. This bit is cleared by RESET. | | | | | |

Bits 5 through 0 enable the line receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to the "Interrupt Scanner and Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are normal operation, automatic echo, local loopback, and remote loopback.

normal operation

The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. The RxEN bit must be set. Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. The TxEN bit must be set.

automatic echo

The serial data received is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxDn pin for serial output. TxEN is ignored, and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.

local loopback

The serial data from the RxDn input is ignored, and the receiver serial input receives data from the transmitter serial output. That data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. The TxEN bit must be set. The transmission goes only to the receiver serial input; the TxDn output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.

remote loopback

The serial data received on the RxDn line is returned to the TxDn line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

summary registers

The TCM78808 contains two registers that summarize the current status of all eight serial data lines, making it possible to determine that a line status has changed with a a single read operation. These registers are selected for access by setting the appropriate address on inputs A2 through A0. Because the registers are shared by eight serial lines, the line-selection bits A5 through A3 are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

interrupt summary register

This read-only register indicates that a transmitter or receiver interrupt condition has occurred and indicates the line number that generated the interrupt. Figure 11 shows the format of the interrupt summary register, and Table 7 describes register information.

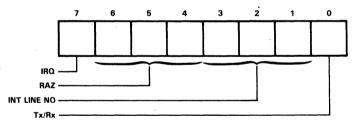


FIGURE 11. TCM78808 INTERRUPT SUMMARY REGISTER FORMAT

TABLE 7. TCM78808 INTERRUPT SUMMARY REGISTER DESCRIPTION

| BIT | DESCRIPTION | | | | | |
|--------|---|--|--|--|--|--|
| 7 | IRQ (Interrupt Request). When set, this bit indicates that the interrupt scanner has found an interrupting condition among | | | | | |
| | the eight serial lines of the TCM78808. These conditions also result in activating the IRQ signal. | | | | | |
| 6,5,4 | RAZ (Read as Zero). Not used | | | | | |
| 3,2,1† | INT LINE NO (Interrupting Line Number). These bits indicate the line number upon which an interrupting condition was found. | | | | | |
| | These bits correspond to the IRQLN2-IRQLNO signals: bit 3 = IRQLN2, bit 2 = IRQLN1, and bit 1 = IRQLNO. See Table 2. | | | | | |
| 0† | Tx/Rx (Transmit/Receive). This bit indicates whether the interrupting condition was caused by a transmitter (Tx/Rx = 1) | | | | | |
| | or a receiver (Tx/Rx = 0). This bit corresponds to the IRQTxRx signal of the TCM78808 and is set when IRQTxRx is set. | | | | | |

[†] Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

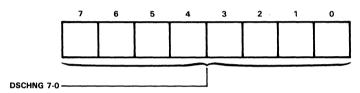


FIGURE 12. TCM78808 DATA SET CHANGE SUMMARY REGISTER FORM

When the MCIE bit in a line mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and generate an interrupt. The data set change summary register bits are cleared by writing a high into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled, and writeback should directly follow the read operation.

The $\overline{\text{RESET}}$ signal disables and initializes the data set change logic. When the $\overline{\text{RESET}}$ signal is high, future changes in $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ are reported as they occur.

interrupt scanner and interrupt handling

The interrupt scanner is a 4-bit counter that sequentially checks lines 0 through 7 for a receiver interrupt (counter positions 0 through 7) and then checks the lines in the same order for a transmitter interrupt (counter positions 8 through 15). If the scanner detects an interrupt condition, it stops, and the $\overline{\text{IRQ}}$ signal goes low. An interrupt must be serviced by software, or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = H) or if either of the line modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG, RxIE, and MCIE all high).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE both high).

When the scanner detects an interrupt, it reports the line number on the IRQ2-IRQ0 lines. The IRQTxRx signal is high for a transmitter interrupt and is low for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{\text{IRQ}}$ line goes high, and the scanner is restarted for each of the following three types of interrupt conditions:

- 1. Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line receiver), thus giving receivers priority over transmitters.

edge-triggered and level-triggered interrupt systems

If the interrupt system of the TCM78808 is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{\text{IRQ}}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{\text{IRQ}}$ line can be connected only to a processor that uses level-triggered interrupts.

modem handling

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deactivating the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The setting of the TxEMT bit to indicate that transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register, and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to be set before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character [a start bit - 5, 6, 7, or 8 data bits (plus parity bit if enabled) and 1, 1.5, or 2 stop bits], and multiplying by either two characters or one depending on when TxEMT monitoring begins.

D3408. NOVEMBER 1988 - REVISED JANUARY 1990

- Bidirectional Transceiver
- Meets EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for 25-MBaud Operation in Both Serial and Parallel Applications
- Low Skew 8 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 30 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 70 mV Typ
- Fail Safe . . . High Receiver Output with Inputs Open
- Operates from a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Interchangeable with National DS3695

description

The TL3695 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standards RS-422-A and RS-485 and CCITT recommendations V.11 and X.27.

The TL3695 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs

D OR P PACKAGE (TOP VIEW)

| R | Ū₁ | U 8 | D vcc |
|----|----------|-----|-------|
| RE | 2 | 7 | В |
| DE | □3 | 6 |] A |
| D | 4 | 5 | GND |

FUNCTION TABLE (DRIVER)

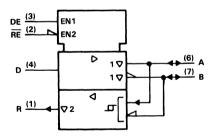
| INPUT | ENABLE | OUT | PUTS |
|-------|--------|-----|------|
| D | DE | Α | В |
| Н | н | Н | L |
| | н | L | Н |
| x | L | Z | Z |

FUNCTION TABLE (RECEIVER)

| DIFFERENTIAL INPUTS | ENABLE | OUTPUT |
|---|--------|--------|
| A – B | RE | R |
| V _{ID} ≥ 0.2 V | L | н |
| $-0.2 \text{ V} < \text{V}_{\text{ID}} < 0.2 \text{ V}$ | L | ? |
| $V_{ID} \leq -0.2 V$ | L | L |
| X | н | Z |
| Inputs Open | L | н |

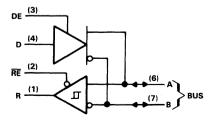
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†

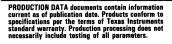


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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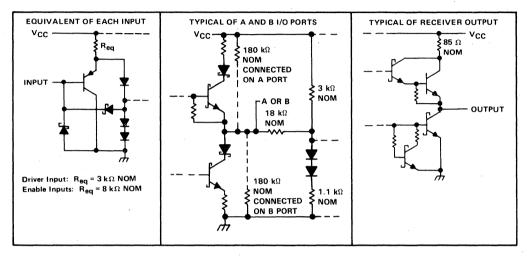




and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} | 7 V |
|--|--------------------------------|
| Voltage range at any bus terminal | – 10 V to 15 V |
| Enable input voltage | 5.5 V |
| Continuous total power dissipation | . See Dissipation Rating Table |
| Operating free-air temperature range, T _A | 0°C to 70°C |
| Storage temperature range | – 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P packa | age 260°C |

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| Р | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | | | MIN | TYP | MAX | UNIT |
|--|-------------------------|--|------|-----|------|------|
| Supply voltage, VCC | | | 4.75 | 5 | 5.25 | ٧ |
| Voltage at any bus terminal (congretaly o | common mode). Vi or Via | | | | 12 | v |
| Voltage at any bus terminal (separately or common mode), VI or VIC | | | | | -7 | |
| High-level input voltage, VIH | D, DE, and RE | | 2 | | | ٧ |
| Low-level input voltage, VIL | D, DE, and RE | | | | 0.8 | V |
| Differential input voltage, VID (see Note 2 | | | | | ±12 | ٧ |
| High-level output current, IOH | Driver | | | | -60 | mA |
| High-level output current, IOH | Receiver | | | | -400 | μΑ |
| Low-level output current, IOI | Driver | | | | 60 | mA |
| Low-level output current, IOL | Receiver | | | | 8 | ША |
| Operating free-air temperature, TA | | | 0 | | 70 | °C |

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating freeair temperature (unless otherwise noted)

| | PARAMETER | TEST CON | TEST CONDITIONS† | | | MAX | UNIT |
|-------------------|---|--|-----------------------|----------------------|---|------|--------|
| VIK | Input clamp voltage | I _I = -18 mA | | | | -1.5 | ٧ |
| Vo | Output voltage | IO = 0 | | 0 | | 6 | ٧ |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 5 | ٧ |
| | | $R_{l} = 100 \Omega$ | See Figure 1 | 1/2 V _{OD1} | | | |
| V _{OD2} | Differential output voltage | 110 022, | | 2 | | | ٧ |
| | | $R_L = 54 \Omega$, | See Figure 1 | 1.5 | 2.5 | 5 | ٧ |
| V _{OD3} | Differential output voltage | $V_{\text{test}} = -7 \text{ V to } 12 \text{ V},$ | See Figure 2 | 1.5 | | 5 | ٧ |
| Δ V _{OD} | Change in magnitude of differential output voltage§ | | | | | ±0.2 | ٧ |
| Voc | Common-mode output voltage | $R_L = 54 \Omega$, | See Figure 1 | | | 3 | ٧ |
| Δ V _{OC} | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | ٧ |
| 1 = | Outside a second | Output disabled, | V _O = 12 V | | *************************************** | 1 | mA |
| Ю | Output current | See Note 3 | $V_0 = -7 \text{ V}$ | | | -0.8 | mA |
| ΊΗ | High-level input current | V _I = 2.4 V | | | | 20 | μΑ |
| ηL | Low-level input current | V _I = 0.4 V | | | | -200 | μΑ |
| | | $V_0 = -7 V$ | | | | -250 | |
| loo | Short-circuit output current | VO = 0 | AO = ACC | | | -150 | mA |
| los | Short-circuit output current | VO = VCC | | | | 250 | IIIA |
| | | $V_0 = 12 V$ | | | | 250 | |
| loo | Supply current | No load | Outputs enabled | | 23 | 50 | mA |
| lcc | oupply current | INO IOAU | Outputs disabled | | 19 35 | | 1111/4 |

[†] The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs. [‡] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

[§] Δ | V_{OD} | and Δ | V_{OC} | are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | TEST | CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|-------------------------------------|-------------------------------------|----------------------|--------------|-----|-----|-----|------|
| tDD | Differential-output delay time | | | | | 8 | 22 | ns |
| | Skew (tDDH-tDDL) | $C_{L1} = C_{L2} = 100 \text{ pF},$ | $R_L = 60 \Omega$, | See Figure 3 | | 1 | 8 | ns |
| †TD | Differential output transition time | | | | | 8 | 18 | ns |
| ^t PZH | Output enable time to high level | C _L = 100 pF, | $R_L = 500 \Omega$, | See Figure 4 | | | 50 | ns |
| tPZL | Output enable time to low level | C _L = 100 pF, | $R_L = 500 \Omega$, | See Figure 5 | | | 50 | ns |
| ^t PHZ | Output disable time from high level | C _L = 15 pF, | $R_L = 500 \Omega$, | See Figure 4 | | 8 | 30 | ns |
| tPLZ | Output disable time from low level | $C_L = 15 pF$, | $R_L = 500 \Omega$, | See Figure 5 | | 8 | 30 | ns |

 $^{^{\}dagger}$ All typical values are at $V_{CC} = 5$ V, $T_{A} = 25$ °C.

SYMBOL EQUIVALENTS

| DATA SHEET PARAMETER | RS-422-A | RS-485 |
|----------------------|--|--|
| v _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| VOD1 | Vo | V _o |
| VOD2 | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| V _{OD3} | | V _t (Test Termination Measurement 2) |
| V _{test} | | V _{tst} |
| Δ V _{OD} | $ \vee_t - \overline{\vee}_t $ | $ V_t - \overline{V}_t $ |
| Voc . | V _{os} | V _{os} |
| Δ V _{OC} | Vos - Vos | $ V_{OS} - \overline{V}_{OS} $ |
| los | I _{sa} , I _{sb} | |
| lo | I _{xa} , I _{xb} | I _{ia} , I _{ib} |

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST C | ONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|---|-------------------------|-------|-----|------|-------|
| VTH | Differential-input high-threshold voltage | $V_0 = 2.7 V$, | $I_0 = -0.4 \text{ mA}$ | | | 0.2 | ٧ |
| VTL | Differential-input low-threshold voltage | $V_0 = 0.5 V$, | 1 _O = 8 mA | -0.2‡ | | | V |
| V _{hys} | Hysteresis [§] | V _{OC} = 0 | | | 70 | | mV |
| VIK | Enable-input clamp voltage | $I_{\parallel} = -18 \text{ mA}$ | | | | -1.5 | V |
| Vон | High-level output voltage | V _{ID} = 200 mV or Inp | uts open | 2.4 | | | V |
| VOH | riigii-ievei output voitage | $I_{OH} = -400 \mu A$ | See Figure 6 | 2.4 | | | v |
| VOL | Low-level output voltage | $V_{ID} = -200 \text{ mV},$ | IOL = 16 mA | | | 0.5 | V |
| VOL | Low-level output voltage | See Figure 6 | IOL = 8 mA | | | 0.45 | ٧ |
| loz | High-impedance-state output current | $V_0 = 0.4 \text{ V to } 2.4 \text{ V}$ | | | | ±20 | μΑ |
| lı. | Line input current | Other input = 0 V, | V _I = 12 V | | | 1 | mA |
| 11 | cine input current | See Note 4 | V _I = -7 V | | | -0.8 | "" |
| ΊΗ | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | μΑ |
| 11L | Low-level enable-input current | V _{IL} = 0.4 V | | | | -100 | μΑ |
| rį | Input resistance | | | 12 | | | kΩ |
| los | Short-circuit output current | V _O = 0 | | -15 | | -85 | mA |
| loo | Supply current | No load | Outputs enabled | | 23 | 50 | mA |
| Icc | | 140 load | Outputs disabled | | 19 | 35 | 111/4 |

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | TEST CONDIT | TIONS | MIN | TYP† | MAX | UNIT |
|------------------|--|--|-----------------|-----|------|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V},$ | $C_L = 15 pF$, | | 14 | 37 | ns |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 7 | | | 14 | 37 | ns |
| ^t PZH | Output enable time to high level | C ₁ = 15 pF, | See Figure 8 | | 7 | 20 | ns |
| t _{PZL} | Output enable time to low level | C[= 15 pr, | See Figure 6 | | 7 | 20 | ns |
| tPHZ | Output disable time from high level | $C_{l} = 15 pF,$ | See Figure 8 | | 7 | 16 | ns |
| tPLZ | Output disable time from low level | 10[= 15 pr, | See Figure 6 | | 8 | 16 | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§] Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

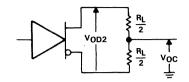


FIGURE 1. DRIVER VOD AND VOC

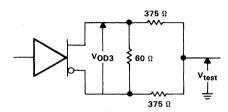
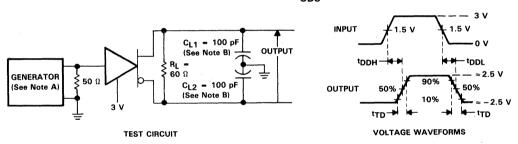


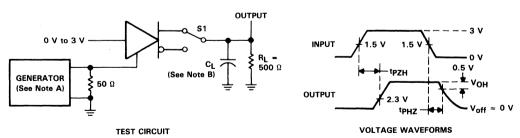
FIGURE 2. DRIVER VOD3



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $z_{out} =$ 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

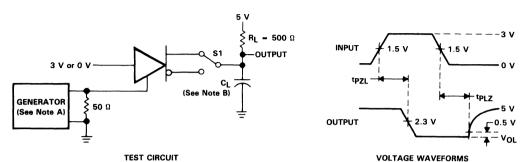


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_{\Gamma} \leq$ 10 ns, t

B. C_L includes probe and jig capacitance. (See switching characteristics — test conditions)

FIGURE 4. DRIVER ENABLE AND DISABLE TIMES





NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, t_f \leq 10 ns, t_f \leq 10 ns, Z_{out} = 50 Ω .

B. C_L includes probe and jig capacitance. (See switching characteristics - test conditions)

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

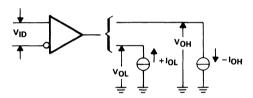
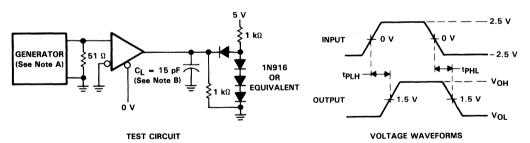


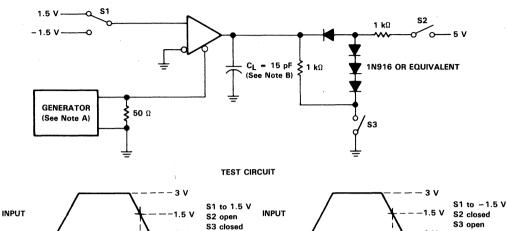
FIGURE 6. RECEIVER VOH AND VOL

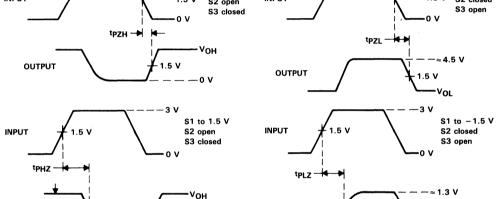


NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 10 ns, $t_f \leq$ 10 ns, $Z_{out} = 50 \Omega$.

B. C_L includes probe and jig capacitance.

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES





VOLTAGE WAVEFORMS

≈ 1.3 V

OUTPUT

VOL

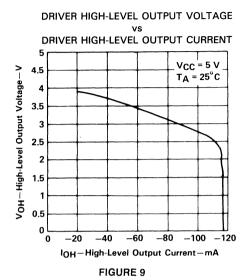
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_f \leq$ 10 ns, $t_f \leq$ 10 ns, $t_{out} = 50 \ \Omega$.

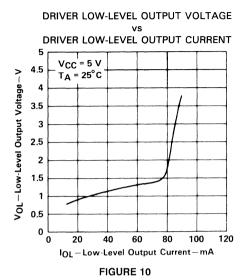
B. C_L includes probe and jig capacitance.

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

OUTPUT

TYPICAL CHARACTERISTICS





DRIVER DIFFERENTIAL OUTPUT VOLTAGE

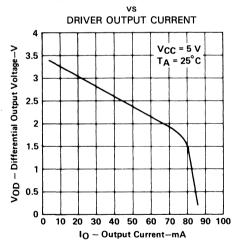


FIGURE 11

TYPICAL CHARACTERISTICS



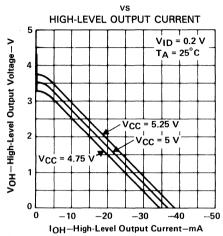


FIGURE 12

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs

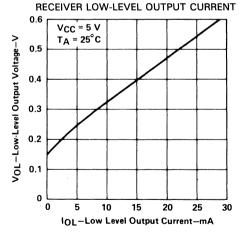


FIGURE 14

RECEIVER HIGH-LEVEL OUTPUT

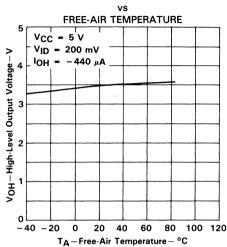


FIGURE 13

RECEIVER LOW-LEVEL OUTPUT VOLTAGE

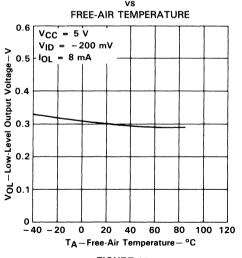
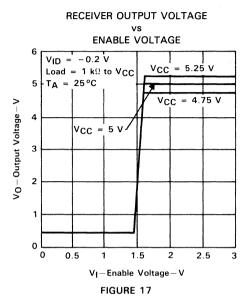


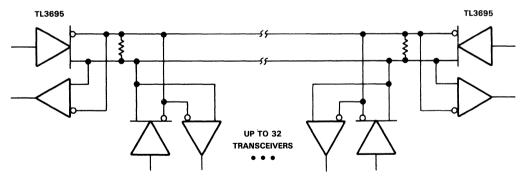
FIGURE 15

TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE **ENABLE VOLTAGE** $V_{ID} = 0.2 \text{ V}$ Load = $8 k\Omega$ to ground. TA = 25°C 4 $V_{CC} = 5.25 \text{ V}$ Vo-Output Voltage-V 4.75 3 -Vcc = 5 V 2 1 0 0.5 1.5 2.5 V_I-Enable Voltage-V FIGURE 16



APPLICATION INFORMATION

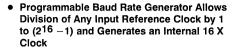


NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18. TYPICAL APPLICATION CIRCUIT

TL16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT

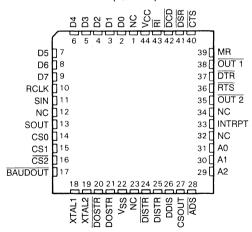
D3096, MARCH 1988 - REVISED APRIL 1989



- Full Double Buffering Eliminates the Need for Precise Synchronization
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from the Serial Data Stream
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
 - 5-, 6-, 7-, or 8-Bit Characters
 - Even-, Odd-, or No-Parity Bit Generation and Detection
 - 1-, 1 1/2-, or 2-Stop Bit Generation
 - Baud Generation (DC to 256 Kilobits per Second)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- Three-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
 - Loopback Controls for Communications Link Fault Isolation
 - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Easily Interfaces to Most Popular Microprocessors
- Faster Plug-In Replacement for National Semiconductor NS16C450

N DUAL-IN-LINE PACKAGE (TOP VIEW) U40 D VCC D0 🗖 1 D1 [39 🗖 RI D2 🗖 3 38 DCD D3 🗖 4 37 DSR 36 CTS D4 Π_{5} D5 🗖 6 35 MR 34 OUT 1 D6 [D7 🗖 8 33 DTR 32 RTS RCLK 19 31 OUT 2 SIN 10 30 INTRPT SOUT 11 CS0 1 12 29 NC CS1 🗖 13 28 1 A0 CS2 **□** 14 27 1 A1 BAUDOUT 15 26 A2 25 ADS XTAL1 16 XTAL2 d 17 24 CSOUT DOSTR 18 23 DDIS DOSTR 19 22 DISTR 21 DISTR ۷ss 🗀 20

FN PACKAGE (TOP VIEW)



NC-No internal connection

description

The TL16C450 is a CMOS version of an Asynchronous Communications Element (ACE). It typically functions in a microcomputer system as a serial input/output interface.

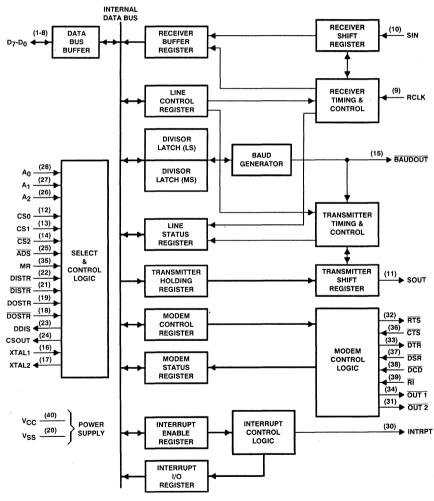
The TL16C450 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of

Texas VI

the ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2¹⁶ –1) and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

block diagram



Pin numbers shown are for the N package.



TL16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT

| PIN | | 1/0 | DESCRIPTION |
|----------------|--------------------|-----|---|
| NAME | NO.† | | |
| A0 | 28 [31] | | Register Select. Three inputs used during read and write operations to select the ACE register to read |
| A1 | 27 [30] | | from or write to. Refer to Table 1 for register addresses, also refer to the Address Strobe (ADS) signal |
| A2 | 26 [29] | | description. |
| ĀDS | 25 [28] | ı | Address Strobe. When $\overline{\text{ADS}}$ is active (low), the Register Select signals (A0, A1, and A2) and Chip Select signals (CS0, CS1, $\overline{\text{CS2}}$) drive the internal select logic directly; when high, the Register Select and Chip Select signals are held in the state they were in when the low-to-high transition of $\overline{\text{ADS}}$ occurred. |
| BAUDOUT | 15 [17] | 0 | Baud Out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the Baud Generator Divisor Latches. BAUDOUT may also be used for the receiver section by tying this output to the RCLK input. |
| CS0 | 12 [14] | | Chin Colont, When active /high and law respectively), those three inputs colont the ACE. Defects the |
| CS1 | 13 [15] | | Chip Select. When active (high and low, respectively), these three inputs select the ACE. Refer to the ADS (Address Strobe) signal description. |
| CS2 | 14 [16] | | Abo (Address Strobe) signal description. |
| CSOUT | 24 [27] | 0 | Chip Select Out. When CSOUT is high, it indicates that the ACE has been selected by the Chip Select inputs (CS0, CS1, and $\overline{\text{CS2}}$). CSOUT is low when the chip is deselected. |
| CTS | 36 [40] | ı | Clear To Send. CTS is a modern status signal whose condition can be checked by reading bit 4 (CTS) of the Modern Status Register. Bit 0 (DCTS) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when CTS changes state, an interrupt is generated. |
| D0 | 1 [2] | | |
| D1 | 2 [3] | İ | |
| D2 | 3 [4] | | |
| D3 | 4 [5] | | Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information |
| D4 | 5 [6] | 1/0 | between the ACE and the CPU. |
| D5 | 6 [7] | | |
| D6 | 7 [8] | | |
| D7 | 8 [9] | | |
| DCD | 38 [42] | 1 | Data Carrier Detect. \overline{DCD} is a modem status signal whose condition can be checked by reading bit 7 (DCD) of the Modem Status Register. Bit 3 (DDCD) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when the \overline{DCD} changes state, an interrupt is generated. |
| DDIS | 23 [26] | 0 | Driver Disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver. |
| DISTR DISTR | 22 [25] 21 [24] | ı | Data Input Strobes. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., DISTR tied low or DISTR tied high). |
| DOSTR DOSTR | 19 [21] 18 [20] | 1 | Data Output Strobes. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., DOSTR tied low or DOSTR tied high). |
| DSR | 37 [41] | 1 | Data Set Ready. \overline{DSR} is a modem status signal whose condition can be checked by reading bit 5 (DSR) of the Modem Status Register. Bit 1 (DDSR) of the Modem Status Register indicates that this signal has changed state since the last read from the Modem Status Register. If the modem status interrupt is enabled when the \overline{DSR} changes state, an interrupt is generated. |
| DTR | 33 [37] | 0 | Data Terminal Ready. When active (low), \overline{DTR} informs a modem or data set that the ACE is ready to establish communication. \overline{DTR} is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. \overline{DTR} is placed in the inactive state either as a result of a Master Reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register. |
| INTRPT | 30 [33] | 0 | Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (inactivated) either when the interrupt is serviced or as a result of a Master Reset. |

[†] Pin numbers shown in brackets are for the FN package.



TL16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT

| | PIN | | |
|-----------------|--------------------|-----|--|
| NAME | NO.† | 1/0 | DESCRIPTION |
| MR | 35 [39] | I | Master Reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions. |
| OUT 1 OUT 2 | 34 [38] 31 [35] | 0 | Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective Modern Control Register bits (OUT 1 and OUT 2) high. OUT 1 and OUT 2 are set to their inactive (high) states as a result of Master Reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR. |
| RCLK | 9 [10] | 1 | Receiver Clock. The 16 X baud rate clock for the receiver section of the ACE. |
| Ri | 39 [43] | ı | Ring Indicator. $\overline{\text{RI}}$ is a modern status signal whose condition can be checked by reading bit 6 (RI) of the Modern Status Register. Bit 2 (TERI) of the Modern Status Register indicates that the $\overline{\text{RI}}$ input has transitioned from a low to a high state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when this transition occurs, an interrupt is generated. |
| RTS | 32 [36] | 0 | Request to Send. When active, informs the modem or data set that the ACE is ready to transmit data. RTS is set to its active state by setting the RTS Modem Control Register bit and is set to its inactive (high) state either as a result of a Master Reset or during loop mode operations or by resetting bit 1 (RTS) of the MCR. |
| SIN | 10 [11] | 1 | Serial Input. Serial data input from a connected communications device. |
| SOUT | 11 [13] | 0 | Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of Master Reset. |
| VCC | 40 [44] | | 5-V Supply Voltage |
| V _{SS} | 20 [22] | | Supply Common |
| XTAL1 XTAL2 | 16 [18] 17 [19] | I/O | External Clock. Connects the ACE to the main timing reference (clock or crystal). |

[†] Pin numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | to 7 V |
|---|--------|
| Input voltage range at any input, V₁ | to 7 V |
| Output voltage range, VO | to 7 V |
| Continuous total dissipation at (or below) 70°C free-air temperature: | |
| FN package | 00 mW |
| N package | 00 mW |
| Operating free-air temperature range | o 70°C |
| Storage temperature range –65°C to | 150°C |
| Case temperature for 10 seconds: FN package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package | 260°C |
| NOTE 1: All voltage values are with respect to VSS. | |

recommended operating conditions

| · | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | · 2 | | VCC | V |
| Low-level input voltage, VIL | -0.5 | | 0.8 | V |
| Operating free-air temperature, T _A | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------------------|-------------------------------|---|-----|------------------|-----|------|
| V _{OH} [‡] | High-level output voltage | I _{OH} = -1 mA | 2.4 | | | ٧ |
| V _{OL} ‡ | Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | ٧ |
| likg | Input leakage current | $V_{CC} = 5.25 \text{ V},$ $V_{SS} = 0,$ $V_{I} = 0 \text{ to } 5.25 \text{ V},$ All other pins floating | | | ±10 | μА |
| loz | High-impedance output current | $V_{CC} = 5.25 \text{ V},$ $V_{SS} = 0,$ $V_{O} = 0 \text{ V to } 5.25 \text{ V},$ chip selected, write mode or, chip deselected | | | ±20 | μΑ |
| lcc | Supply current | V _{CC} = 5.25 V, T _A = 25°C, SIN, DSR, DCD, CTS, and $\overline{\text{RI}}$ at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs. Baud rate = 50 kilobits per second | | | 10 | mA |
| CXTAL1 | Clock input capacitance | | | 15 | 20 | pF |
| CXTAL2 | Clock output capacitance | V _{CC} = 0, V _{SS} = 0, | | 20 | 30 | pF |
| Ci | Input capacitance | f = 1 MHz, T _A = 25°C, All other pins grounded | | 6 | 10 | pF |
| Co | Output capacitance | 7 iii oirioi pirio groundou | | 10 | 20 | pF |

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | MIN | MAX | UNIT |
|-------------------|---|--------|------|-----|------|
| tcR | Cycle time, read (t _{W7} + t _{d8} + t _{d9}) | | 175 | | ns |
| tcW | Cycle time, write (tw6 + td5 + td6) | | 175 | | ns |
| t _{w5} | Pulse duration, address strobe low | 2, 3 | 15 | | ns |
| tw6 | Pulse duration, write strobe | 2 | 80 | | ns |
| tw7 | Pulse duration, read strobe | 3 | 80 | i | ns |
| twMR | Pulse duration, master reset | | 1000 | | ns |
| t _{su1} | Setup time, address | 2,3 | 15 | | ns |
| t _{su2} | Setup time, chip select | 2,3 | 15 | | ns |
| t _{su3} | Setup time, data | 2 | 15 | | ns |
| th1 | Hold time, address | 2,3 | 0 | | ns |
| th2 | Hold time, chip select | 2,3 | 0 | | ns |
| th3 | Hold time, write to chip select | 2 | 20 | | ns |
| th4 | Hold time, write to address | 2 | 20 | | ns |
| t _{h5} | Hold time, data | 2 | 15 | | ns |
| th6 | Hold time, read to chip select | 3 | 20 | | ns |
| th7 | Hold time, read to address | 3 | 20 | | ns |
| td4 [§] | Delay time, select to write | 2 | 15 | | ns |
| td5 [§] | Delay time, address to write | 2 | 15 | | ns |
| ^t d6 | Delay time, write cycle | 2 | 80 | | ns |
| t _{d7} § | Delay time, chip select to read | 3 | 15 | | ns |
| td8§ | Delay time, address to read | 3 | 15 | | ns |
| t _d 9 | Delay time, read cycle | 3 | 80 | | ns |

[§] Only applies when ADS is low.

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ These parameters apply for all outputs except XTAL2.

TL16C450 ASYNCHRONOUS COMMUNICATIONS ELEMENT

system switching characteristics over recommended ranges of supply voltage and operating freeair temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|-----------------------------------|--------|-------------------------|-----|------|------|
| t _{w1} | Pulse duration, clock high | 1 | f = 9 MHz maximum | 50 | | ns |
| tw2 | Pulse duration, clock low | 1 | f = 9 MHz maximum | 50 | | ns |
| t _{d3} | Delay time, select to CS output | 2,3 | C _L = 100 pF | | 70 | ns |
| ^t d10 | Delay time, read to data | 3 | C _L = 100 pF | . 1 | 60 . | ns |
| ^t d11 | Delay time, read to floating data | 3 | C _L = 100 pF | 0 | 60 | ns |
| tdis(R) | Read to driver disable | 3 | C _L = 100 pF | | 60 | ns |

baud generator switching requirements over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|---------------------------------|--------|---|-----|-----|------|
| tw3 | Pulse duration, BAUDOUT low | 1 | $f = 6.25 \text{ MHz}, \text{CLK} \div 1,$ $\text{C}_L = 100 \text{ pF}$ | 80 | | ns |
| t _{w4} | Pulse duration, BAUDOUT high | 1 | $f = 6.25 \text{ MHz}, \text{ CLK} \div 1,$ $C_L = 100 \text{ pF}$ | 80 | | ns |
| ^t d1 | Delay time, BAUDOUT low to high | 1 | C _L = 100 pF | | 125 | ns |
| t _{d2} | Delay time, BAUDOUT high to low | 1 | C _L = 100 pF | | 125 | ns |

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|--------|-------------------------|-----|-----|----------------|
| td12 | Delay time, RCLK to sample | 4 | | | 100 | ns |
| ^t d13 | Delay time, stop to set interrupt | 4 | | 1 | 1 | RCLK cycles |
| td14 | Delay time, read RBR/LSR to reset interrupt | 4 | C _L = 100 pF | | 140 | ns |

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|--------|-------------------------|-----|-----|-------------------|
| ^t d15 | Delay time, initial write THR to transmit start | 5 | | 8 | 24 | baudout cycles |
| ^t d16 | Delay time, stop to interrupt | 5 | | 8 | 8 | baudout cycles |
| t _{d17} | Delay time, write THR to reset interrupt | 5 | C _L = 100 pF | | 140 | ns |
| ^t d18 | Delay time, initial write to interrupt (THRE) | 5 | | 16 | 32 | baudout cycles |
| t _{d19} | Delay time, read IIR to reset interrupt (THRE) | 5 | C _L = 100 pF | | 140 | ns |

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|---|-------------------------|-----|-----|------|
| t _{d20} | Delay time, write MCR to output | 6 | C _L ≈ 100 pF | | 100 | ns |
| t _{d21} | Delay time, modem input to set interrupt | 6 | C _L = 100 pF | | 170 | ns |
| t _{d22} | Delay time, read MSR to reset interrupt | 6 | C _L = 100 pF | | 140 | ns |



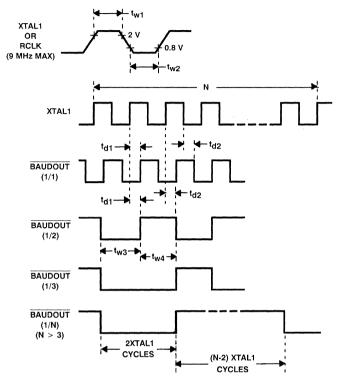
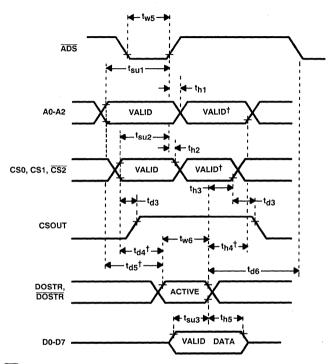
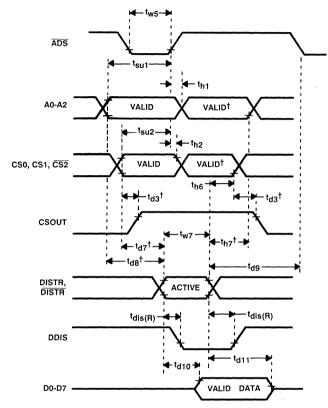


FIGURE 1. BAUD GENERATOR TIMING



[†] Applicable only when ADS is tied low.

FIGURE 2. WRITE CYCLE TIMING



 $[\]dagger$ Applicable only when $\overline{\text{ADS}}$ is tied low.

FIGURE 3. READ CYCLE TIMING

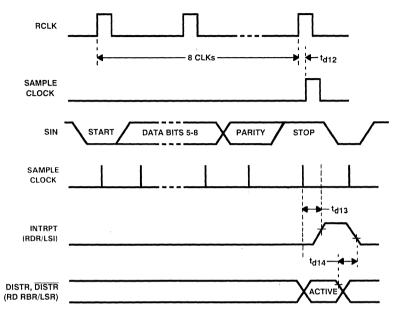


FIGURE 4. RECEIVER TIMING

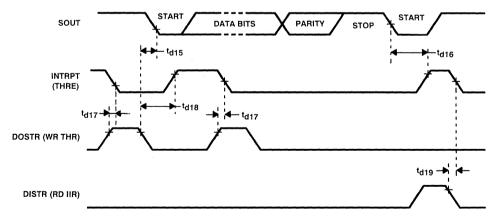
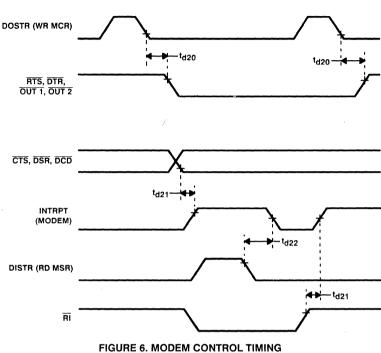


FIGURE 5. TRANSMITTER TIMING





TYPICAL APPLICATION DATA

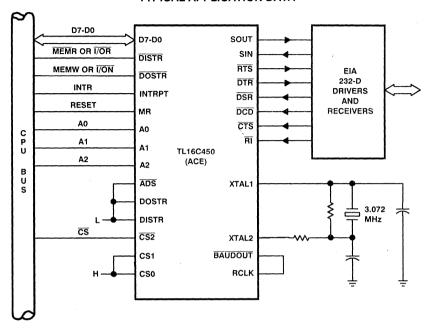


FIGURE 7. BASIC TL16C450 CONFIGURATION

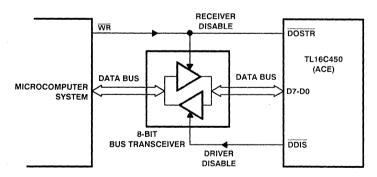


FIGURE 8. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS



TYPICAL APPLICATION DATA

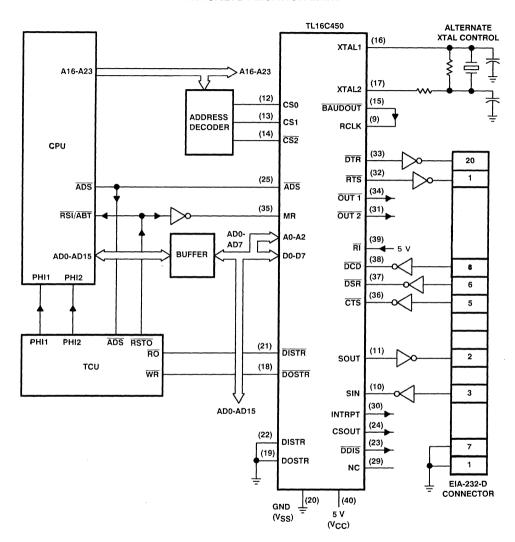


FIGURE 9. TYPICAL TL16C450 CONNECTION TO A CPU

TABLE 1. REGISTER SELECTION

| DLAB | A2 | A1 | A0 | REGISTER |
|------|----|----|----|--|
| 0 | Ĺ | L | L | Receiver buffer (read), transmitter holding register (write) |
| 0 | L | L | Н | Interrupt enable |
| X | Ŀ | Н | L | Interrupt identification (read only) |
| X | L | Н | Н | Line control |
| X | Н | L | L | Modem control |
| X | Н | L | Н | Line status |
| X | Н | Н | L | Modem status |
| X | Н | Н | Н | Scratch |
| 1 | L | L | L | Divisor latch (LSB) |
| 1 | L | L. | Н | Divisor Latch (MSB) |

[†] The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

| REGISTER/SIGNAL | RESET CONTROL | RESET STATE |
|---|--------------------------|---|
| Interrupt Enable Register | Master Reset | All bits low (0-3 forced and 4-7 permanent) |
| Interrupt Identification Register | Master Reset | Bit 0 is high, bits 1 and 2 are low, and bits 3-7 are permanently low |
| Line Control Register | Master Reset | All bits low |
| Modem Control Register | Master Reset | All bits low |
| Line Status Register | Master Reset | Bits 5 and 6 are high, all other bits are low |
| Modem Status Register | Master Reset | Bits 0-3 are low, bits 4-7 are input signals |
| SOUT | Master Reset | High |
| INTRPT (Receiver Error Flag) | Read LSR/MR | Low |
| INTRPT (Received Data Available) | Read RBR/MR | Low |
| INTRPT (Transmitter Holding Register Empty) | Read IIR/Write THR/MR | Low |
| INTRPT (Modern Status Changes) | Read MSR/MR | Low |
| OUT 2 | Master Reset | High |
| RTS | Master Reset | High |
| DTR | Master Reset | High |
| OUT 1 | Master Reset | High |
| Scratch Register | Master Reset | No effect |
| Divisor Latch (LSB and MSB) Registers | Master Reset | No effect |
| Receiver Buffer Register | Master Reset | No effect |
| Transmitter Holding Register | Master Reset | No effect |

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

| | | | | | REG | ISTER ADDR | ESS | | | | |
|---------------|--|---|---|---|---|------------------------------------|--|--|---------------------|---------------------------|----------------|
| | 0 DLAB≃0 | 0 DLAB=0 | 1 DLAB=0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 DLAB = 1 | 1 DLAB=1 |
| Bit No. | Receiver Buffer Register (Read Only) | Transmitter Holding Register (Write Only) | Interrupt Enable Register | Interrupt Ident. Register (Read Only) | Line Control Register | MODEM Control Register | Line Status Register | MODEM Status Register | Scratch Register | Divisor Latch (LSB) | Latch (MSB) |
| | RBR | THR | IER | IIR | LCR | MCR | LSR | MSR | SCR | DLL | DLM |
| 0 | Data Bit 0* | Data Bit 0 | Enable Received Data Available Interrupt (ERBFI) | "0" if Interrupt Pending | Word Length Select Bit 0 (WLS0) | Data Terminal Ready (DTR) | Data Ready (DR) | Delta Clear to Send (DCTS) | Bit 0 | Bit 0 | Bit 8 |
| 1 | Data Bit 1 | Data Bit 1 | Enable Transmitter Holding Register Empty Interrupt (ETBEI) | Interrupt ID Bit (0) | Word Length Select Bit 1 (WLS1) | Request to Send (RTS) | Overrun Error (OE) | Delta Data Set Ready (DDSR) | Bit 1 | Bit 1 | Bit 9 |
| 2 | Data Bit 2 | Data Bit 2 | Enable Receiver Line Status Interrupt (ELSI) | Interrupt ID Bit (1) | Number of Stop Bits (STB) | Out 1 | Parity Error (PE) | Trailing Edge Ring Indicator (TERI) | Bit 2 | Bit 2 | Bit 10 |
| 3 | Data Bit 3 | Data Bit 3 | Enable MODEM Status Interrupt (EDSSI) | 0 | Parity Enable (PEN) | Out 2 | Framing Error (FE) | Delta Data Carrier Detect (DDCD) | Bit 3 | Bit 3 | Bit 11 |
| Data Bit 4 | Data Bit 4 | 0 | 0 | Even Parity Select (EPS) | Loop | Break Interrupt (BI) | Clear to Send (CTS) | Bit 4 | Bit 4 | Bit 12 | |
| 5 | Data Bit 5 | Data Bit 5 | 0 | 0 | Stick Parity | 0 | Transmitter Holding Register (THRE) | Cata Set Ready (DSR) | Bit 5 | Bit 5 | Bit 13 |
| 6 | Data Bit 6 | Data Bit 6 | 0 | 0 | Set Break | 0 | Transmitter Empty (TEMT) | Ring Indicator (RI) | Bit 6 | Bit 6 | Bit 14 |
| 7 | Data Bit 7 | Data Bit 7 | 0 | 0 | Divisor Latch Access Bit (DLAB) | 0 | 0 | Data Carrier Detect (DCD) | Bit 7 | Bit 7 | Bit 15 |

^{*} Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register and a Receiver Buffer Register. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's Receiver Shift Register receives serial data from the Serial Input (SIN) pin. The Receiver Shift Register then converts the data to a parallel form and loads it into the Receiver Buffer Register. When a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register and a Transmitter Shift Register. Timing is supplied by the Baud Out (BAUDOUT) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE Transmitter Holding Register receives data off the Internal Data Bus and, when the shift register is idle, moves it into the Transmitter Shift Register. The Transmitter Shift Register serializes the data and outputs it at the Serial Output (SOUT). If the Transmitter Holding Register is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.
- Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.
- Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.
- Bit 3. This bit, when set to logic 1, enables the Modern Status interrupt.
- Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 - Receiver line status (highest priority)

Priority 2 - Receiver data ready

Priority 3 — Transmitter holding register empty

Priority 4 — Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the Interrupt Identification Register are not used and are always set at logic 0.

TABLE 4. INTERRUPT CONTROL FUNCTIONS

| IDE | INTERRUPT IDENTIFICATION REGISTER | | ENTIFICATION PRIORIT | | PRIORITY LEVEL | INTERRUPT TYPE | INTERRUPT SOURCE | INTERRUPT RESET METHOD | |
|-------|-----------------------------------|-------|----------------------|------------------------------------|---|---|------------------|---------------------------|--|
| BIT 2 | BIT 1 | BIT 0 | 1 | | | | | | |
| 0 | 0 | 1 | None | None | None | _ | | | |
| 1 | 1 | 0 | 1 | Receiver line status | Overrun error, parity error, framing error or break interrupt | Reading the Line Status register | | | |
| 1 | 0 | 0 | 2 | Received data available | Receiver data available | Reading the Receiver buffer Buffer register | | | |
| 0 | 1 | 0 | 3 | Transmitter Holding register empty | Transmitter Holding register empty | Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register | | | |
| 0 | 0 | 0 | 4 | Modem status | Clear to Send, Data Set Ready, Ring Indicator, or Data Carrier Detect | Reading the Modem Status register | | | |

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

| Bit 1 | Bit 0 | Word Length |
|-------|-------|-------------|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The Receiver checks the first Stop bit only, regardless of the number of Stop bits selected. The number of Stop bits generated, in relation to word length and bit 2, is shown in the following.

| Bit 2 | Word Length Selected by Bits 1 and 2 | Number of Stop Bits Generated |
|-------|---|----------------------------------|
| 0 | Any word length | 1 |
| 1 | 5 bits | 1 1/2 |
| 1 | 6 bits | 2 |
| 1 | 7 bits | 2 |
| 1 | 8 bits | 2 |

- Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.
- Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).
- Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1.
- Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.
- Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 (DTR) controls the Data Terminal Ready (DTR) output. Setting this bit to a logic 1 forces the DTR output to its active state (low). When bit 0 is set to a logic 0, DTR goes high.
- Bit 1. Bit 1 (RTS) controls the Request to Send (RTS) output in a manner identical to Bit 0's control over the DTR output.
- Bit 2. Bit 2 (OUT 1) controls the Output 1 (OUT 1) signal, a user designated output signal, in a manner identical to Bit 0's control over the DTR output.
- Bit 3. Bit 3 (OUT 2) controls the Output 2 ($\overline{\text{OUT 2}}$) signal, a user designated output signal, in a manner identical to Bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:
 - 1. The transmitter Serial Output (SOUT) is set high.
 - 2. The receiver Serial Input (SIN) is disconnected.
 - 3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
 - 4. The four modem control inputs (CTS, DSR, DCD, and RI) are disconnected.
 - 5. The four modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs.
 - 6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register and is reset to logic 0 by reading the Receiver Buffer Register.
- Bit 1[‡]. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register.
- Bit 2[‡]. Bit 2 is the Parity Error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register.
- Bit 3[‡]. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register.
- [†] The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment
- [‡] Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.



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- Bit 4[‡]. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register.
- Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to a logic 1 condition when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU.
- Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0.
- Bit 7. This bit is always reset to logic 0.
- ‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 is the Delta Clear to Send (DCTS) indicator. This bit indicates that the $\overline{\text{CTS}}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.
- Bit 1. Bit 1 is the Delta Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{\rm DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.
- Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{\rm RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.
- Bit 3. Bit 3 is the Delta Data Carrier Detect (DDCD) indicator. This bit indicates that the \overline{DCD} input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modern Status Interrupt is enabled, a Modern Status Interrupt is generated.
- Bit 4. Bit 4 is the complement of the Clear to Send (CTS) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).
- Bit 5. Bit 5 is the complement of the Data Set Ready (DSR) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 0 (DTR).
- Bit 6. Bit 6 is the complement of the Ring Indicator (\overline{RI}) input. If Bit 4 (loop) of the Modern Control register is set to a logic 1, this bit is equivalent to the Modern Control registers bit 2 (OUT 1).
- Bit 7. Bit 7 is the complement of the Data Carrier Detect (\overline{DCD}) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).



scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable Baud Generator that takes a clock input in the range between DC and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the Baud Generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XTAL1 frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called Divisor Latches, are used to store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization of the ACE in order to ensure desired operation of the Baud Generator. When either of the Divisor Latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6, which follow, illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

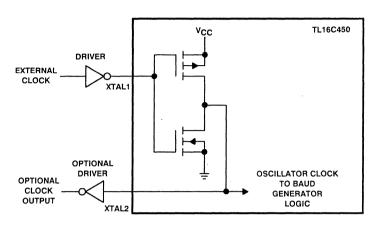
Refer to Figure 10 for examples of typical clock circuits.

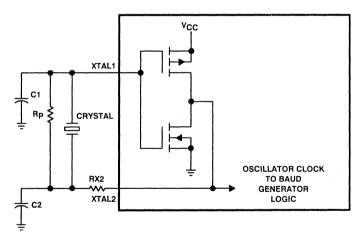
TABLE 5. BAUD RATES USING A 1.8432-MHz CRYSTAL

| DESIRED BAUD RATE | DIVISOR USED TO GENERATE 16 X CLOCK | PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL |
|----------------------|---|---|
| 50 | 2304 | |
| 75 | 1536 | |
| 110 | 1047 | 0.026 |
| 134.5 | 857 | 0.058 |
| 150 | 768 | |
| 300 | 384 | |
| 600 | 192 | |
| 1200 | 96 | |
| 1800 | 64 | |
| 2000 | 58 | 0.69 |
| 2400 | 48 | |
| 3600 | 32 | |
| 4800 | 24 | |
| 7200 | 16 | |
| 9600 | 12 | |
| 19200 | 6 | |
| 38400 | 3 | |
| 56000 | 2 | 2.86 |

TABLE 6. BAUD RATES USING A 3.072-MHz CRYSTAL

| DESIRED BAUD RATE | DIVISOR USED TO GENERATE 16 X CLOCK | PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL |
|----------------------|---|---|
| 50 | 3840 | |
| 75 | 2560 | |
| 110 | 1745 | 0.026 |
| 134.5 | 1428 | 0.034 |
| 150 | 1280 | |
| 300 | 640 | |
| 600 | 320 | |
| 1200 | 160 | |
| 1800 | 107 | 0.312 |
| 2000 | 96 | |
| 2400 | 80 | |
| 3600 | 53 | 0.628 |
| 4800 | 40 | |
| 7200 | 27 | 1.23 |
| 9600 | 20 | |
| 19200 | 10 | |
| 38400 | 5 | |





TYPICAL CRYSTAL OSCILLATOR NETWORK

| CRYSTAL | Rp | R _{X2} | C ₁ | C ₂ |
|---------|------|-----------------|----------------|----------------|
| 3.1 MHz | 1 ΜΩ | 1.5 kΩ | 10-30 pF | 40-60 pF |
| 1.8 MHz | 1 ΜΩ | 1.5 kΩ | 10-30 pF | 40-60 pF |

FIGURE 10. TYPICAL CLOCK CIRCUITS



TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

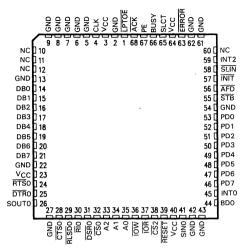
D3284, MAY 1989-REVISED JANUARY 1990

- Integrates Most Communications Card Functions From the IBM PC/AT or Compatibles with Single-/ or Dual-Channel Serial Ports
- TL16C451 Consists of One TL16C450 Plus Centronix Printer Interface
- TL16C452 Consists of Two TL16C450s Plus Centronix Printer Interface
- Fully Programmable Serial Interface Characteristics:
 - 5-, 6-, 7-, or 8-Bit Characters
 - Even-, Odd-, or No-Parity Bit Generation and Detection
 - 1-, 1 1/2-, or 2 Stop-Bit Generation
 - Programmable Baud Rate (DC to 256 Kilobits per Second)
- Fully Double Buffered for Reliable Asynchronous Operation

description

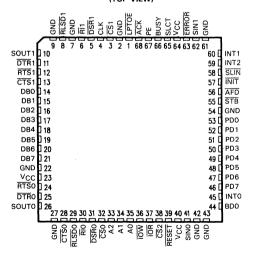
The TL16C451 and TL16C452 provide singleand dual-channel (respectively) serial interfaces along with a single Centronix parallel-port interface. The serial interfaces provide a serial-toparallel conversion for data received from a peripheral device or modem and a parallel-toserial conversion for data transmitted by a computer CPU. The parallel interface provides a bidirectional parallel data port that fully conforms to the requirements for a Centronix-type printer. A computer CPU can read the status of the asynchronous-communications-element (ACE) interfaces at any point in the operation. The status includes the state of the modern signals (CTS, DSR, RLSD, and RI) and any changes to these signals that have occurred since the last time they were read, the state of the transmitter and receiver including errors detected on received data, and printer status. The TL16C451 and TL16C452 provide control for modem signals (RTS and DTR), interrupt enables, baudrate programming, and parallel-port control signals.

TL16C451 . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

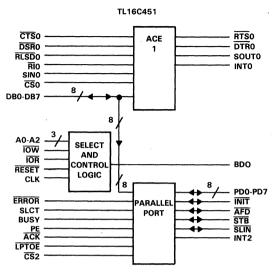
TL16C452 . . . FN PACKAGE (TOP VIEW)

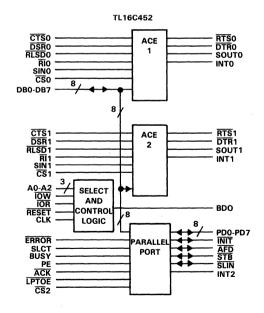




TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

functional block diagrams





TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

| PIN NAME [†] | NO. | I/O | DESCRIPTION |
|--------------------------------------|----------------|-----|--|
| A0 A1 A2 | 35 34 33 | ı | Register Select. Three inputs used during read and write operations to select the register to read from or write to. Refer to Table 1 for register addresses, also refer to the chip select signals (CS0, CS1, CS2). |
| ACK | 68 | ı | Line Printer Acknowledge. This input goes low to indicate a successful data transfer has taken place. It generates a printer-port interrupt during its positive transition. |
| ĀFD | 56 | 1/0 | Line Printer Autofeed. This open-drain line provides the line printer with a low signal when continuous-form paper is to be autofed to the printer. An internal pullup is provided. |
| BDO | 44 | 0 | Bus Buffer Output. This output is active (high) when the CPU is reading data. When active, this output can be used to disable an external transceiver. |
| BUSY | 66 | 1 | Line Printer Busy. This is an input line from the line printer that goes high when the line printer is not ready to accept data. |
| CLK | 4 | 1/0 | External Clock. Connects the ACE to the main timing reference. |
| CS0 CS1 [V _{CC}] CS2 | 32 3 38 | 1 | Chip Selects. Each chip select enables read and write operations to its respective channel. CS0 and CS1 select serial channels 0 and 1, respectively, and CS2 selects the parallel port. |
| CTS0 CTS1 [GND] | 28 13 | - | Clear To Send. \overline{CTS} is an active-low modern status signal whose state can be checked by reading bit 4 (CTS) of the Modern Status Register. Bit 0 (DCTS) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when \overline{CTS} changes state, an interrupt is generated. |
| DB0 | 14 | | , |
| DB1 | 15 | ļ | |
| DB2 | 16 | | |
| DB3 | 17 | 1/0 | Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information |
| DB4 | 18 | " | between the TL16C451/TL16C452 and the CPU. DB0 is the least significant bit (LSB). |
| DB5 | 19 | | |
| DB6 | 20 | | |
| DB7 | 21 | ļ | |
| DSR0 DSR1 [GND] | 31 5 | l | Data Set Ready. DSR is an active-low modern status signal whose state can be checked by reading bit 5 (DSR) of the Modern Status Register. Bit 1 (DDSR) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the modern status interrupt is enabled when the DSR changes state, an interrupt is generated. |
| DTR0 DTR1 [NC] | 25 11 | 0 | Data Terminal Ready. When active (low), $\overline{\text{DTR}}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{\text{DTR}}$ is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. $\overline{\text{DTR}}$ is placed in the inactive state either as a result of a reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register. |
| ERROR | 63 | ı | Line Printer Error. This is an input line from the line printer. The line printer reports an error by holding this line low during the error conditon. |
| INIT | 57 | 1/0 | Line Printer Initialize. This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started. An internal pullup is provided. |
| INTO INT1 [NC] | 45 60 | 0 | Interrupt. INTn is an active-high 3-state output that is enabled by bit 3 of the MCR. When active , INTn informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available, the transmitter holding register is empty, and an enabled modem status interrupt. The INTn output is reset (low) either when the interrupt is serviced or as a result of a reset. |
| INT2 | 59 | 0 | Printer Port Interrupt. This signal is an active-high 3-state output generated by the positive transition of ACK. It is enabled by bit 4 of the Write Control Register. |
| IOR | 37 | ı | Data Read Strobe. When IOR input is active (low) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. |
| ĪOW | 36 | ı | Data Write Strobe. When IOW input is active (low) while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. |

 $[\]ensuremath{^{\dagger}}$ Names shown in brackets are for the TL16C451.



TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

| PIN | | | |
|----------------------|-------------------------------------|-----|---|
| NAME [†] | NO. | 1/0 | DESCRIPTION |
| LPTOE | 1 | ı | Parallel Data Output Enable. When low, this signal enables the Write Data Register to the PD0-PD7 lines. A high puts the PD0-PD7 lines in the high-impedance state allowing them to be used as inputs. LPTOE is usually tied low for line printer operation. |
| PD0-PD7 | 53-46 | 1/0 | Parallel Data Bits (0-7). These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when <u>LPTOE</u> is high. |
| PÉ | 67 | ı | Line Printer Paper Empty. This is an input line from the line printer that goes high when the printer runs out of paper. |
| RESET | 39 | ı | Reset. When active (low), RESET clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions. |
| RIO RI1 [GND] | 30 6 | ı | Ring Indicator. $\overline{\mathbb{N}}$ is an active-low modem status signal whose state can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 (TERI) of the Modem Status Register indicates that the $\overline{\mathbb{N}}$ input has transitioned from a low to a high state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when this transition occurs, an interrupt is generated. |
| RLSD0 RLSD1 [GND] | 29 8 | 1 | Receive Line Signal Detect. RLSD0 is an active-low modern status signal whose state can be checked by reading bit 7 of the Modern Status Register. Bit 3 (DRLSD) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when RLSD0 changes state, an interrupt is generated. This bit is low when a data carrier is detected. |
| RTS0 RTS1 [NC] | 24 12 | 0 | Request To Send. When active (low), this signal informs the modern or data set that the ACE is ready to transmit data. RTS is set to its active state by setting the RTS Modern Control Register bit and is set to its inactive (high) state either as a result of a reset or during loop mode operations or by resetting bit 1 (RTS) of the modern control register. |
| SIN0 SIN1 [GND] | 41 62 | 1 | Serial Input. Serial data input from a connected communications device. |
| SLCT | 65 | ī | Line Printer Selected. This is an input line from the line printer that goes high when the line printer has been selected. |
| SLIN | 58 | 1/0 | Line Printer Select. This open-drain line selects the printer when it is active (low). An internal pullup is provided. |
| SOUT0 SOUT1 [NC] | 26 10 | 0 | Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of reset. |
| STB | 55 | 1/0 | Line Printer Strobe. This open-drain line provides communication synchronization between the TL16C451/TL16C452 and the line printer. When it is active (low), it provides the line printer with a signal to latch the data currently on the parallel port. An internal pullup is provided. |
| vcc | 23,40, 64 | | 5-V Supply Voltage |
| GND | 2,7,9, 22,27, 42,43, 54,61 | | Supply Common |

[†] Names shown in brackets are for the TL16C451.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range, VCC (see Note 1) | V to 7 V |
|--|----------|
| Input voltage range at any input, V _I | V to 7 V |
| Output voltage range, VO | V to 7 V |
| Continuous total power dissipation | 100 mW |
| Operating free-air temperature range | to 70°C |
| Storage temperature range | o 150°C |
| Case temperature for 10 seconds | 260°C |

NOTE 1: All voltage values are with respect to GND.



TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | Vcc | V |
| Low-level input voltage, VIL | -0.5 | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|-------------------------------|--|-----|------------------|-----|------|
| VOH | High-level output voltage | $I_{OH} = -0.4$ mA on DB0-DB7 $I_{OH} = -2$ mA to 4 mA on PD0-PD7 $I_{OH} = -0.2$ mA on \overline{INIT} , \overline{AFD} , \overline{STB} , and \overline{SLIN} $I_{OH} = -0.2$ mA on all other outputs | 2.4 | | | ٧ |
| V _{OL} | Low-level output voltage | IOL = 4 mA on DB0-DB7 IOL = 12 mA on PD0-PD7 IOL = 10 mA on INIT, AFD, STB, and SLIN (see Note 2) IOL = 2 mA on all other outputs | | | 0.4 | V |
| l _{lkg} | Input leakage current | V _{CC} = 5.25 V, V _{SS} = 0, V _I = 0 to 5.25 V, All other pins floating | | 44 | ±10 | μА |
| loz | High-impedance output current | V _{CC} = 5.25 V, V _{SS} = 0, V _O = 0 to 5.25 V, Chip selected and write mode, or chip deselected | | | ±20 | μА |
| lcc | Supply current | V _{CC} = 5.25 V, T _A = 25°C, SIN, DSR, RLSD, CTS, and RI at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs. Baud rate = 50 kilobits per second | | | 10 | mA |
| CXTAL1 | Clock input capacitance | | | 15 | 20 | pF |
| CXTAL2 | Clock output capacitance | $V_{CC} = 0,$ $V_{SS} = 0,$ $V_{\Delta} = 25^{\circ}C.$ | | 20 | 30 | pF |
| Ci | Input capacitance | f = 1 MHz, T _A = 25°C, All other pins grounded | | 6 | 10 | pF |
| Co | Output capacitance | | | 10 | 20 | pF |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: INIT, AFD, STB, and SLIN are open-collector output pins that each have an internal pullup to V_{CC}. This will generate a maximum of 2 mA of internal I_{OL} per pin. In addition to this internal current, each pin will sink at least 10 mA while maintaining the V_{OL} specification of 0.4 V Max.

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system timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | MIN MAX | UNIT |
|------------------|---|--------|---------|------|
| t _{cR} | Cycle time, read $(t_{W7} + t_{d8} + t_{d9})$ | | 175 | ns |
| t _{cW} | Cycle time, write (tw6 + td5 + td6) | | 175 | ns |
| t _{w1} | Pulse duration, clock high | 1 | 50 | ns |
| t _{w2} | Pulse duration, clock low | 1 | 50 | ns |
| t _{w5} | Pulse duration, write strobe | 2 | 80 | ns |
| tw6 | Pulse duration, read strobe | 3 | 80 | ns |
| twRST | Pulse duration, reset | | 1000 | ns |
| t _{su1} | Setup time, address | 2,3 | 15 | ns |
| t _{su2} | Setup time, chip select | 2,3 | 15 | ns |
| t _{su3} | Setup time, data | 2 | 15 | ns |
| t _{h1} | Hold time, address | 2,3 | 20 | ns |
| th2 | Hold time, chip select | 2,3 | 20 | ns |
| th3 | Hold time, data | 2 | 15 | ns |
| t _d 3 | Delay time, write cycle | 2 | 80 | ns |
| t _{d4} | Delay time, read cycle | 3 | 80 | ns |

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|-----------------------------------|--------|-------------------------|-----|-----|------|
| ^t d5 | Delay time, read to data | 3 | C _L = 100 pF | | 60 | ns |
| t _{d6} | Delay time, read to floating data | 3 | C _L = 100 pF | 0 | 60 | ns |
| tdis(R) | Read to driver disable | 3 | C _L = 100 pF | | 60 | ns |

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|---|--------|-------------------------|-----|-----|----------------|
| t _{d7} | Delay time, RCLK to sample | 4 | | | 100 | ns |
| t _{d8} | Delay time, stop to set interrupt | 4 | | 1 | 1 | RCLK cycles |
| t _{d9} | Delay time, read RBR/LSR to reset interrupt | 4 | C _L = 100 pF | | 140 | ns |

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|--------|-------------------------|-----|-----|-------------------|
| ^t d10 | Delay time, initial write THR to transmit start | 5 | | 8 | 24 | baudout cycles |
| ^t d11 | Delay time, stop to interrupt | 5 | | 8 | 8 | baudout cycles |
| t _{d12} | Delay time, write THR to reset interrupt | 5 | C _L = 100 pF | | 140 | ns |
| ^t d13 | Delay time, initial write to interrupt (THRE) | 5 | | 16 | 32 | baudout cycles |
| td14 | Delay time, read IIR to reset interrupt (THRE) | 5 | C _L = 100 pF | | 140 | ns |

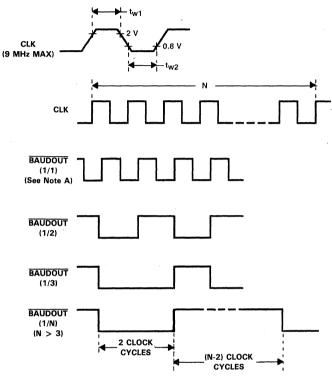
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modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------|--|--------|-------------------------|-----|-----|------|
| td15 | Delay time, write MCR to output | 6 | C _L = 100 pF | | 100 | ns |
| td16 | Delay time, modem input to set interrupt | 6 | C _L = 100 pF | | 170 | ns |
| td17 | Delay time, read MSR to reset interrupt | 6 | C _L = 100 pF | | 140 | ns |

parallel port switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|--------|-------------------------|-----|-----|------|
| t _{d18} | Delay time, write parallel port control to output | 7 | C _L = 100 pF | | 60 | ns |
| td19 | Delay time, write parallel port data to output | 7 | C _L = 100 pF | | 60 | ns |
| t _{d20} | Delay time, output enable to data | 7 | Cլ = 100 pF | | 60 | ns |
| t _{d21} | Delay time, ACK to INT2 | 7 | C _L = 100 pF | | 100 | ns |



NOTE A: BAUDOUT is an internally generated signal used in the receiver and transmitter circuits to synchronize data.

FIGURE 1. BAUD GENERATOR TIMING

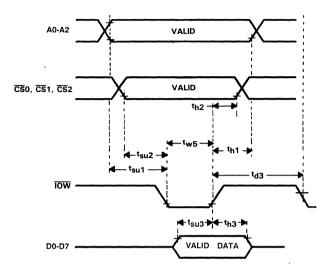


FIGURE 2. WRITE CYCLE TIMING

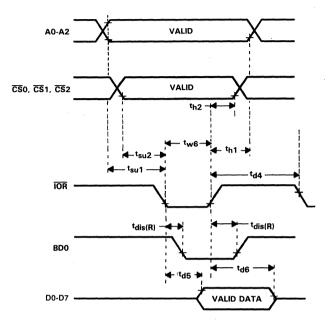


FIGURE 3. READ CYCLE TIMING

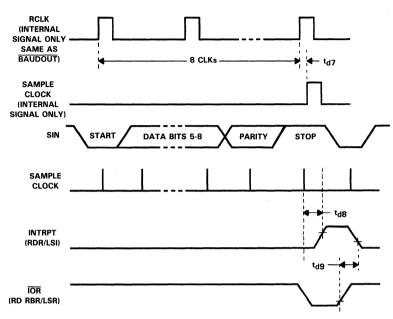


FIGURE 4. RECEIVER TIMING

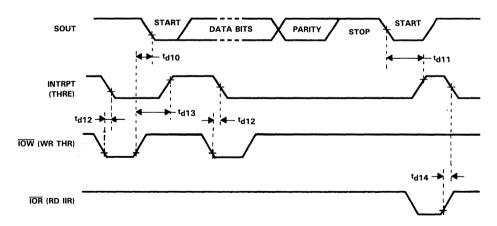
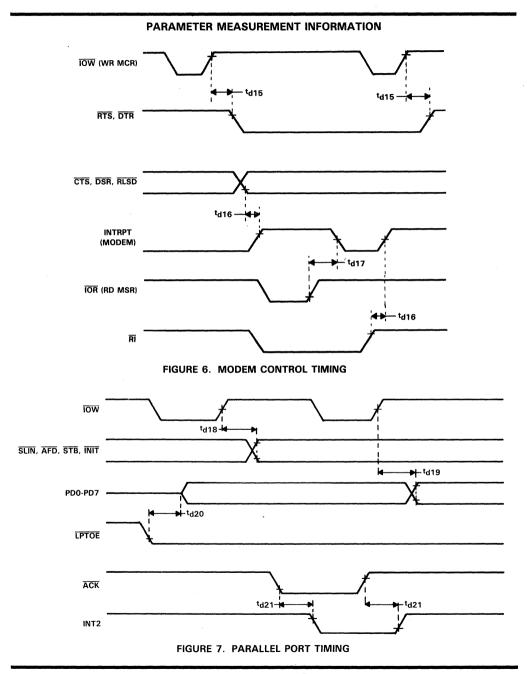
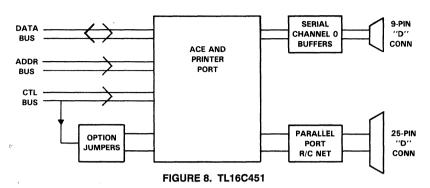


FIGURE 5. TRANSMITTER TIMING





APPLICATION INFORMATION



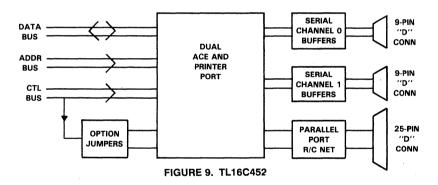


TABLE 1. REGISTER SELECTION

| DLAB† | A2 | A1 | A0 | REGISTER |
|-------|----|----|----|--|
| 0 | L | L | L | Receiver buffer (read), transmitter holding register (write) |
| 0 | L | L | Н | Interrupt enable |
| X | L | Н | L | Interrupt identification (read only) |
| X | L | Н | Н | Line control |
| X | Н | L | L | Modem control |
| X | Н | L | Н | Line status |
| X | Н | Н | L | Modem status |
| X | Н | Н | Н | Scratch |
| 1 | L | L | L | Divisor latch (LSB) |
| 1 | L | L | Н | Divisor Latch (MSB) |

[†] The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

| REGISTER/SIGNAL | RESET CONTROL | RESET STATE |
|---|-----------------------------|---|
| Interrupt Enable Register | Reset | All bits low (0-3 forced and 4-7 permanent) |
| Interrupt Identification Register | Reset | Bit 0 is high, bits 1 and 2 are low, and bits 3-7 are permanently low |
| Line Control Register | Reset | All bits low |
| Modem Control Register | Reset | All bits low |
| Line Status Register | Reset | Bits 5 and 6 are high, all other bits are low |
| Modem Status Register | Reset | Bits 0-3 are low, bits 4-7 are input signals |
| SOUT | Reset | High |
| INTRPT (Receiver Error Flag) | Read LSR/Reset | Low |
| INTRPT (Received Data Available) | Read RBR/Reset | Low |
| INTRPT (Transmitter Holding Register Empty) | Read IIR/Write THR/Reset | Low |
| INTRPT (Modern Status Changes) | Read MSR/Reset | Low |
| OUT 2 (interrupt enable) | Reset | High |
| RTS | Reset | High |
| DTR | Reset | High |
| OUT 1 | Reset | High |
| Scratch Register | Reset | No effect |
| Divisor Latch (LSB and MSB) Registers | Reset | No effect |
| Receiver Buffer Registers | Reset | No effect |
| Transmitter Holding Registers | Reset | No effect |

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

| Γ | | | | | REG | ISTER ADDR | IESS | | | | |
|------------|--|---|---|---|---|------------------------------------|--|---|---------------------|---------------------------|----------------|
| | 0 DLAB=0 | 0 DLAB=0 | 1 DLAB=0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 DLAB = 1 | 1 DLAB=1 |
| Bit No. | Receiver Buffer Register (Read Only) | Transmitter Holding Register (Write Only) | Interrupt Enable Register | Interrupt Ident. Register (Read Only) | Line Control Register | Modem Control Register | Line Status Register | Modem Status Register | Scratch Register | Divisor Latch (LSB) | Latch (MSB) |
| | RBR | THR | IER | IIR | LCR | MCR | LSR | MSR | SCR | DLL | DLM |
| 0 | Data Bit 0* | Data Bit 0 | Enable Received Data Available Interrupt (ERBFI) | "0" if Interrupt Pending | Word Length Select Bit 0 (WLS0) | Data Terminal Ready (DTR) | Data Ready (DR) | Delta Clear to Send (DCTS) | Bit 0 | Bit 0 | Bit 8 |
| 1 | Data Bit 1 | Data Bit 1 | Enable Transmitter Holding Register Empty Interrupt (ETBEI) | Interrupt ID Bit (0) | Word Length Select Bit 1 (WLS1) | Request to Send (RTS) | Overrun Error (OE) | Delta Data Set Ready (DDSR) | Bit 1 | Bit 1 | Bit 9 |
| 2 | Data Bit 2 | Data Bit 2 | Enable Receiver Line Status Interrupt (ELSI) | Interrupt ID Bit (1) | Number of Stop Bits (STB) | Out 1 | Parity Error (PE) | Trailing Edge Ring Indicator (TERI) | Bit 2 | Bit 2 | Bit 10 |
| 3 | Data Bit 3 | Data Bit 3 | Enable MODEM Status Interrupt (EDSSI) | 0 | Parity Enable (PEN) | Out 2 (Interrupt Enable) | Framing Error (FE) | Delta Receive Line Signal Detect (DRLSD) | Bit 3 | Bit 3 | Bit 11 |
| 4 | Data Bit 4 | Data Bit 4 | 0 | 0 | Even Parity Select (EPS) | Ľoop | Break Interrupt (BI) | Clear to Send (CTS) | Bit 4 | Bit 4 | Bit 12 |
| 5 | Data Bit 5 | Data Bit 5 | 0 | 0 | Stick Parity | 0 | Transmitter Holding Register (THRE) | Data Set Ready (DSR) | Bit 5 | Bit 5 | Bit 13 |
| 6 | Data Bit 6 | Data Bit 6 | 0 | 0 | Set Break | 0 | Transmitter Empty (TEMT) | Ring Indicator (RI) | Bit 6 | Bit 6 | Bit 14 |
| 7 | Data Bit 7 | Data Bit 7 | 0 | 0 | Divisor Latch Access Bit (DLAB) | 0 | 0 | Receive Line Signal Detect (RLSD) | Bit 7 | Bit 7 | Bit 15 |

^{*} Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register and a Receiver Buffer Register. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's Receiver Shift Register receives serial data from the Serial Input (SIN) pin. The Receiver Shift Register then converts the data to a parallel form and loads it into the Receiver Buffer Register. When a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register and a Transmitter Shift Register. Timing is supplied by the Baud Out (BAUDOUT) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE Transmitter Holding Register receives data off the Internal Data Bus and, when the shift register is idle, moves it into the Transmitter Shift Register. The Transmitter Shift Register serializes the data and outputs it at the Serial Output (SOUT). If the Transmitter Holding Register is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.
- Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.
- Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.
- Bit 3. This bit, when set to logic 1, enables the Modern Status interrupt.
- Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 — Receiver line status (highest priority)

Priority 2 - Receiver data ready

Priority 3 - Transmitter holding register empty

Priority 4 — Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to identify the highest priority interrupt pending, as indicated in Table 4.

Bits 3 thru 7. Bits 3 through 7 in the Interrupt Identification Register are not used and are always set at logic 0.

TABLE 4. INTERRUPT CONTROL FUNCTIONS

| IDE | INTERRUPT IDENTIFICATION REGISTER | | ENTIFICATION PRIORITY | | PRIORITY LEVEL | INTERRUPTITYPE INTERRUPT SOURCE | | INTERRUPT RESET METHOD |
|-------|---|-------|-----------------------|------------------------------------|--|---|--|---------------------------|
| BIT 2 | BIT 1 | BIT 0 | | | | | | |
| 0 | 0 | 1 | None | None | None | | | |
| 1 | 1 | 0 | 1 | Receiver line status | Overrun error, parity error, framing error or break interrupt | Reading the Line Status register | | |
| 1 | 0 | 0 | 2 | Received data available | Receiver data available | Reading the Receiver buffer Buffer register | | |
| 0 | 1 | 0 | 3 | Transmitter Holding register empty | Transmitter Holding register empty | Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register | | |
| 0 | 0 | 0 | . 4 | Modern status | Clear to Send, Data Set Ready, Ring Indicator, or Receive Line Signal Detect | Reading the Modem Status register | | |

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

| Bit 1 | Bit 0 | Word Length |
|-------|-------|-------------|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The number of Stop bits generated, in relation to word length and bit 2, is as follows:

| Bit 2 | Word Length Selected | Number of Stop |
|-------|----------------------|----------------|
| Dit 2 | by Bits 1 and 2 | Bits Generated |
| 0 | Any word length | 1 |
| 1 | 5 bits | 1 1/2 |
| 1 | 6 bits | 2 |
| 1 | 7 bits | 2 |
| 1 | 8 bits | 2 |

- Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.
- Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic is in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).
- Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1.
- Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic, it only effects the serial output.
- Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 (DTR) controls the Data Terminal Ready (DTR) output. Setting this bit to a logic 1 forces the DTR output to its active state (low). When bit 0 is set to a logic 0, DTR goes high.
- Bit 1. Bit 1 (RTS) controls the Request to Send (RTS) output in a manner identical to Bit 0's control over the DTR output.
- Bit 2. Bit 2 (OUT 1) is a reserved location used only in the loopback mode.
- Bit 3. Bit 3 (OUT 2) controls the output enable for the interrupt signal. When set to a logic 1, the interrupt is enabled. When bit 3 is set to a logic 0, the interrupt is disabled.
- Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:
 - 1. The transmitter Serial Output (SOUT) is set high.
 - 2. The receiver Serial Input (SIN) is disconnected.
 - 3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
 - 4. The four modern status inputs (CTS, DSR, RLSD, and RI) are disconnected.
 - The modem control register bits (DTR, RTS, OUT1, and OUT2) are connected to the modem status register bits (DSR, CTS, RI, and RLSD), respectively.
 - 6. The four modern control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register and is reset to logic 0 by reading the Receiver Buffer Register.
- Bit 1[‡]. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register.
- Bit 2[‡]. Bit 2 is the Parity Error (PE) indicator. When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register.
- Bit 3[‡]. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register.
- [†] The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
- [‡] Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.



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- Bit 4[‡]. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register.
- Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to a logic 1 condition when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU.
- Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0.
- Bit 7. This bit is always reset to logic 0.

‡ Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 is the Delta Clear to Send (DCTS) indicator. This bit indicates that the $\overline{\text{CTS}}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.
- Bit 1. Bit 1 is the Delta Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{\rm DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrrupt is enabled, a Modem Status Interrupt is generated.
- Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{\rm RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modern Status Interrupt is enabled, a Modern Status Interrupt is generated.
- Bit 3. Bit 3 is the Delta Receive Line Signal Detect (DRLSD) indicator. This bit indicates that the RLSD input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.
- Bit 4. Bit 4 is the complement of the Clear to Send (CTS) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).
- Bit 5. Bit 5 is the complement of the Data Set Ready (DSR) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 0 (DTR).
- Bit 6. Bit 6 is the complement of the Ring Indicator (RI) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 2 (OUT 1).
- Bit 7. Bit 7 is the complement of the Receive Line Signal Detect (RLSD) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).



scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable Baud Generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the Baud Generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = CLK frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called Divisor Latches, are used to store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization of the ACE in order to ensure desired operation of the Baud Generator. When either of the Divisor Latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

interrupt control logic

The interrupt control logic is shown in Figure 9.

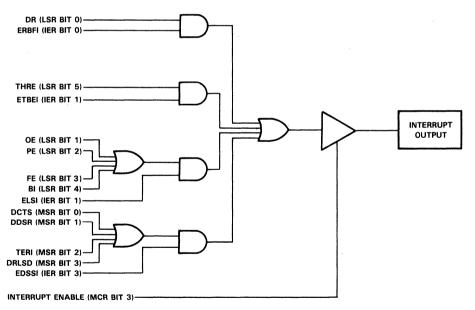


FIGURE 9. INTERRUPT CONTROL LOGIC

TL16C451, TL16C452 ASYNCHRONOUS COMMUNICATIONS ELEMENTS

parallel port registers

The parallel port registers interface either device to a Centronix-style printer. When Chip Select 2 ($\overline{\text{CS2}}$) is low, the parallel port is selected. Tables 5 and 6 show the registers associated with this parallel port. The read or write function of the register is controlled by the state or the read ($\overline{\text{IOR}}$) and write ($\overline{\text{IOW}}$) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (BUSY), Acknowledge (ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines, which are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (INIT), Autofeed the Paper (AFD), and Strobe (STB), which informs the printer of the presence of a valid byte on the parallel bus. These signals are set to 0 when a reset occurs. The Write Data Register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 5. PARALLEL PORT REGISTERS

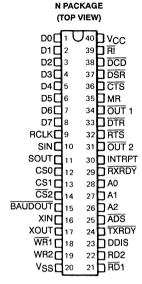
| REGISTER | REGISTER BITS | | | | | | | | |
|---------------|---------------|-------|-------|---------|-------|-------|-------|-------|--|
| REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| Read Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| Read Status | BUSY | ACK | PE | SLCT | ERROR | 1 | 1 | 1 | |
| Read Control | 1 | 1 | 1 | IRQ ENB | SLIN | INIT | AFD | STB | |
| Write Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| Write Control | 1 | 1 | 1 | IRQ ENB | SLIN | INIT | AFD | STB | |

TABLE 6. PARALLEL PORT REGISTER SELECT

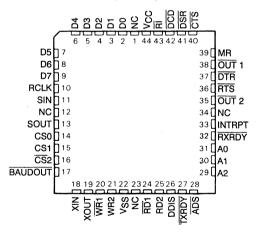
| | co | REGISTER SELECTED | | | |
|-----|-----|-------------------|----|----|-------------------|
| IOR | IOW | CS2 | A1 | A0 | REGISTER SELECTED |
| L | Н | L | L | L | Read Data |
| L | Н | L | L | Н | Read Status |
| L | Н | L | Н | L | Read Control |
| L | Н | L | Н | Н | Invalid |
| Н | L | Ļ | L | L | Write Data |
| Н | L | L | L | Н | Invalid |
| Н | L | L | Н | L | Write Control |
| Н | L | L | Н | Н | Invalid |

D3128, AUGUST 1989 - REVISED FEBRUARY 1990

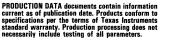
- Capable of Running with All Existing TL16C450 Software
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- In the FIFO Mode, Transmitter and Receiver Are Each Buffered with 16-Byte FIFOs to Reduce the Number of Interrupts to the CPU
- In the TL16C450 Mode, Holding and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2¹⁶ -1) and Generates an Internal 16 X Clock
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from the Serial Data Stream
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Fully Programmable Serial Interface Characteristics:
 - 5-, 6-, 7-, or 8-Bit Characters
 - Even-, Odd-, or No-Parity Bit Generation and Detection
 - 1-, 1 1/2-, or 2-Stop Bit Generation
 - Baud Generation (DC to 256 Kilobits per Second)
- False-Start Bit Detection
- Complete Status Reporting Capabilities
- 3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities:
 - Loopback Controls for Communications Link Fault Isolation
 - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Faster Plug-In Replacement for National Semiconductor NS16550A



FN PACKAGE (TOP VIEW)



NC - No internal connection





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description

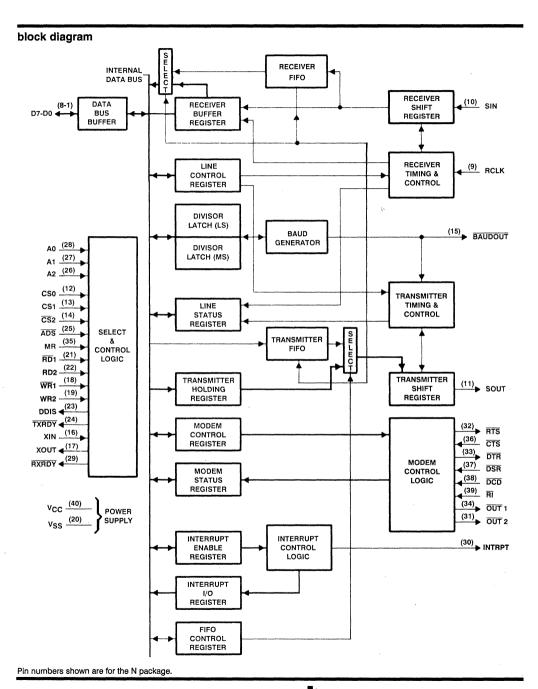
The TL16C550A is a functional upgrade of the TL16C450 Asynchronous Communications Element (ACE). Functionally identical to the TL16C450 on powerup (Character Mode[†]), the TL16C550A can be placed in an alternate mode (FIFO) to relieve the CPU of excessive software overhead.

In this mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits or error data per byte in the receiver FIFO) to be stored in both receive and transmit modes. To minimize system overhead and maximize system efficiency, all logic is on the chip. Two of the TL16C450 pin functions (pins 24 and 29 on the N package and pins 27 and 32 on the FN package) have been changed to allow signalling of DMA transfers.

The TL16C550A performs serial-to-parallel conversion on data received from a peripheral device or modern and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes: the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C550A ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2¹⁶ –1) and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

† The TL16C550A can also be reset to the TL16C450 mode under software control.





| PIN | | | | | | |
|--|--|-----|--|--|--|--|
| NAME | NO.† | 1/0 | DESCRIPTION | | | |
| A0 A1 A2 | 28 [31] 27 [30] 26 [29] | ı | Register Select. Three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the Address Strobe (ADS) signal description. | | | |
| ADS | 25 [28] | 1 | Address Strobe. When \overline{ADS} is active (low), the Register Select signals (A0, A1, and A2) and Chip Select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the Register Select and Chip Select signals are held in the state they were in when the low-to-high transition of \overline{ADS} occurred. | | | |
| BAUDOUT | 15 [17] | 0 | Baud Out. 16 X clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the Baud Generator Divisor Latches. BAUDOUT may also be used for the receiver section by tying this output to the RCLK input. | | | |
| CS0 CS1 CS2 | 12 [14] 13 [15] 14 [16] | - | Chip Select. When active (high, high, and low, respectively), these three inputs select the ACE. If any of these inputs are inactive, the ACE remains inactive. Refer to the ADS (Address Strobe) signal description. | | | |
| СТЅ | 36 [40] | 1 | Clear To Send. $\overline{\text{CTS}}$ is a modern status signal whose condition can be checked by reading bit 4 (CTS) of the Modern Status Register. Bit 0 (DCTS) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when $\overline{\text{CTS}}$ changes state, an interrupt is generated. | | | |
| D0 D1 D2 D3 D4 D5 D6 D7 | 1 [2] 2 [3] 3 [4] 4 [5] 5 [6] 6 [7] 7 [8] 8 [9] | I/O | Data Bus. Eight 3-state data lines provide a bidirectional path for data, control, and status information between the ACE and the CPU. | | | |
| DCD | 38 [42] | I | Data Carrier Detect. DCD is a modern status signal whose condition can be checked by reading bit 7 (DCD) of the Modern Status Register. Bit 3 (DDCD) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the Modern Status Interrupt is enabled when the DCD changes state, and interrupt is generated. | | | |
| DDIS | 23 [26] | 0 | Driver Disable. This output is active (high) when the CPU is not reading data. When active, this output can be used to disable an external transceiver. | | | |
| DSR | 37 [41] | l | Data Set Ready. DSR is a modern status signal whose condition can be checked by reading bit 5 (DSR) of the Modern Status Register. Bit 1 (DDSR) of the Modern Status Register indicates that this signal has changed state since the last read from the Modern Status Register. If the modern status interrupt is enabled when the DSR changes state, an interrupt is generated. | | | |
| DTR | 33 [37] | 0 | Data Terminal Ready. When active (low), $\overline{\text{DTR}}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{\text{DTR}}$ is placed in the active state by setting the DTR bit of the Modem Control Register to a high level. $\overline{\text{DTR}}$ is placed in the inactive state either as a result of a Master Reset or during loop mode operation or resetting bit 0 (DTR) of the Modem Control Register. | | | |
| INTRPT | 30 [33] | 0 | Interrupt. When active (high), INTRPT informs the CPU that the ACE has a interrupt to be serviced. Four conditions that cause an interrupt to be issued are; a receiver error, received data is available or timeout (FIFO mode only), the transmitter holding register is empty, and an enabled modem status interrupt. The INTRPT output is reset (deactivated) either when the interrupt is serviced or as a result of a Master Reset. | | | |
| MR | 35 [39] | I | Master Reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2, ACE Reset Functions. | | | |
| OUT1 OUT2 | 34 [38] 31 [35] | 0 | Outputs 1 and 2. User-designated output pins that are set to their active states by setting their respective Modem Control Register bits (OUT 1 and OUT 2) high. OUT 1 and OUT 2 are set to their inactive (high) states as a result of Master Reset or during loop mode operations or by resetting bit 2 (OUT 1) or bit 3 (OUT 2) of the MCR. | | | |
| RCLK | 9 [10] | 1 | Receiver Clock. The 16 X baud rate clock for the receiver section of the ACE. | | | |
| RD1 RD2 | 21 [24] 22 [25] | | Read inputs. When either input is active (high or low, respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation; the other input should be tied in its inactive state (i.e., RD2 tied low or $\overline{\text{RD}}$ 1 tied high). | | | |

[†] Pin numbers shown in brackets are for the FN package.



| PIN | | T | |
|-----------------|--------------------|-----|--|
| NAME NO.† | | 1/0 | DESCRIPTION |
| RI | 39 [43] | 1 | Ring indicator. $\overline{\text{RI}}$ is a modem status signal whose condition can be checked by reading bit 6 (RI) of the Modem Status Register. Bit 2 (TERI) of the Modem Status Register indicates that the $\overline{\text{RI}}$ input has transitioned from a low to a high state since the last read from the Modem Status Register. If the Modem Status Interrupt is enabled when this transition occurs, an interrupt is generated. |
| RTS | 32 [36] | 0 | Request to Send. When active, informs the modem or data set that the ACE is ready to transmit data. RTS is set to its active state by setting the RTS Modem Control Register bit and is set to its inactive (high) state either as a result of a Master Reset or during loop-mode operations or by resetting bit 1 (RTS) of the MCR. |
| RXRDY | 29 [32] | 0 | Receiver Ready Output. Receiver DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16V450 mode, only DMA Mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the receiver FIFO has been emptied. In DMA Mode 0 (FCRO = 0 or FCRO = 1, FCR3 = 0), if there is at least 1 character in the receiver FIFO or receiver holding register, RXRDY will be active (low). When RXRDY has been active but there are no characters in the FIFO or holding register, RXRDY will go inactive (high). In DMA Mode 1 (FCRO = 1, FCR3 = 1), when the trigger level or the timeout has been reached, RXRDY will go inactive (low); when it has been active but there are no more characters in the FIFO or holding register, it will go inactive (high). |
| SIN | 10 [11] | 1 | Serial Input. Serial data input from a connected communications device. |
| SOUT | 11 [13] | 0 | Serial Output. Composite serial data output to a connected communication device. SOUT is set to the Marking (logic 1) state as a result of Master Reset. |
| TXRDY | 24 [27] | 0 | Transmitter Ready Output. Transmitter DMA signalling is available with this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating in the TL16C450 mode, only DMA mode 0 is allowed. Mode 0 supports single-transfer DMA in which a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA in which multiple transfers are made continuously until the transmit FIFO has been filled. |
| VCC | 40 [44] | | 5-V Supply Voltage |
| V _{SS} | 20 [22] | | Supply Common |
| WR1 WR2 | 18 [20] 19 [21] | _ | Write Inputs. When either input is active (high or low, respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs if required to transfer data during a write operation; the other input should be tied in its inactive state (i.e., WR2 tied low or $\overline{\text{WR}}$ 1 tied high). |
| XIN XOUT | 16 [18] 17 [19] | I/O | External Clock. Connects the ACE to the main timing reference (clock or crystal). |

 $[\]ensuremath{^{\dagger}}$ Pin numbers shown in brackets are for the FN package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)

| Supply voltage range, V _{CC} (see Note 1) | \dots -0.5 V to 7 V |
|---|-------------------------|
| Input voltage range at any input, V ₁ | \dots -0.5 V to 7 V |
| Output voltlage range, VO | \dots -0.5 V to 7 V |
| Operating free-air temperature range, T _A | 0°C to 70°C |
| Storage temperature range | - 65°C to 150°C |
| Case temperature for 10 seconds: FN package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package | 260°C |

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-------|-----|------|------|
| Supply voltage, VCC | 4.75 | 5 | 5.25 | ٧ |
| High-level input voltage, VIH | 2 | | Vcc | V |
| Low-level input voltage, V _{IL} | - 0.5 | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN TYPT | MAX | UNIT |
|-------------------|-------------------------------|--|----------|-----|------|
| VOH [‡] | High-level output voltage | I _{OH} = -1 mA | 2.4 | | V. |
| V _{OL} ‡ | Low-level output voltage | I _{OL} = 1.6 mA | | 0.4 | ٧ |
| l _{lkg} | Input leakage current | $\begin{split} &V_{CC}=5.25 \text{ V}, &V_{SS}=0, \\ &V_{I}=0 \text{ to } 5.25 \text{ V}, \\ &\text{All other pins floating} \end{split}$ | | ±10 | μΑ |
| loz | High-impedance output current | V _{CC} = 5.25 V, V _{SS} = 0, V _O = 0 to 5.25 V, Chip selected in Write mode or Chip deselected | | ±20 | μА |
| lcc | Supply current | V _{CC} = 5.25 V, T _A = 25°C, SIN, DSR, DCD, CTS, and Ri at 2 V, All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second | | 10 | mA |
| CXIN | Clock input capacitance | | 15 | 20 | pF |
| CXOUT | Clock output capacitance | $V_{CC} = 0,$ $V_{SS} = 0,$ | ±20 | рF | |
| Ci | Input capacitance | All other inputs at 0.8 V, XTAL1 at 4 MHz, No load on outputs, Baud rate = 50 kilobits per second | 6 | 10 | pF |
| Co | Output capacitance | | 10 | 20 | pF |

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | ALT. SYMBOL | FIGURE | MIN MAX | UNIT |
|-------------------|---|------------------|--------|---------|------|
| t _{cR} | Cycle time, read (t _{w7} + t _{d8} + t _{d9}) | RC | | 175 | ns |
| tcW | Cycle time, write (tw6 + td5 + td6) | WC | | 175 | ns |
| t _{w5} | Pulse duration, address strobe low | t _{ADS} | 2,3 | 15 | ns |
| tw6 | Pulse duration, write strobe | twr | 2 | 80 | ns |
| tw7 | Pulse duration, read strobe | tRD | 3 | 80 | ns |
| tw8 | Pulse duration, master reset | tMR | | 1 | μs |
| t _{su1} | Setup time, address | t _{AS} | 2,3 | 15 | ns |
| t _{su2} | Setup time, chip select | tcs | 2,3 | 15 | ns |
| t _{su3} | Setup time, data | t _{DS} | 2 | 15 | ns |
| ^t h1 | Hold time, address | t _{AH} | 2,3 | 0 | ns |
| th2 | Hold time, chip select | tCH | 2,3 | 0 | ns |
| th3 | Hold time, write to chip select | twcs | 2 | 20 | ns |
| th4 | Hold time, write to address | twa | 2 | 20 | ns |
| th5 | Hold time, data | , tDH | 2 | 15 | ns |
| th6 | Hold time, read to chip select | tRCS | 3 | 20 | ns |
| th7 | Hold time, read to address | t _{RA} | 3 | 20 | ns |
| t _{d4} § | Delay time, select to write | tcsw | 2 | 15 | ns |
| t _{d5} § | Delay time, address to write | t _{AW} | 2 | 15 | ns |
| ^t d6 | Delay time, write cycle | twc | 2 | 80 | ns |
| t _{d7} § | Delay time, chip select to read | t _{CSR} | 3 | 15 | ns |
| t _{d8} § | Delay time, address to read | t _{AR} | 3 | 15 | ns |
| ^t d9 | Delay time, read cycle | t _{RC} | . 3 | 80 | ns |

[§] Only applies when ADS is low.



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ These parameters apply for all outputs except XOUT.

system switching characteristics over recommended ranges of supply voltage and operating freeair temperature (see Note 2)

| | PARAMETER | ALT. SYMBOL | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|-----------------------------------|-------------|--------|-------------------------|-----|-----|------|
| tw1 | Pulse duration, clock high | txH | 1 | f = 9 MHz maximum | 50 | | ns |
| tw2 | Pulse duration, clock low | tXL | 1 | f = 9 MHz maximum | 50 | | ns |
| td10 | Delay time, read to data | tRVD | 3 | C _L = 100 pF | | 60 | ns |
| ^t d11 | Delay time, read to floating data | tHZ | 3 | C _L = 100 pF | 0 | 60 | ns |
| tdis(R) | Read to driver disable | tRDD | 3 | C _L = 100 pF | | 60 | ns |

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | ALT. SYMBOL | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|---------------------------------|------------------|--------|---|-----|-----|------|
| twз | Pulse duration, BAUDOUT low | tLW | 1 | $f = 9 \text{ MHz}, \text{CLK} \div 2,$ $\text{C}_{\text{L}} = 100 \text{ pF}$ | 80 | | ns |
| t _{w4} | Pulse duration, BAUDOUT high | tHW | 1 | f = 9 MHz, CLK ÷ 2, C _L = 100 pF | 100 | | ns |
| t _{d1} | Delay time, BAUDOUT low to high | tBLD | 1 | C _L = 100 pF | | 125 | ns |
| t _{d2} | Delay time, BAUDOUT high to low | ^t BHD | 1 | C _L = 100 pF | | 125 | ns |

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 3)

| | PARAMETER | ALT. SYMBOL | FIGURE | TEST CONDITIONS | MIN MAX | UNIT |
|------------------|--|-------------------|-----------|-------------------------|---------|----------------|
| td12 | Delay time, RCLK to sample | tSCD | 4 | | 100 | ns |
| t _{d13} | Delay time, stop to set interrupt or read RBR to LSI interrupt | ^t SINT | 4,5,6,7,8 | | 1 | RCLK cycles |
| td14 | Delay time, read RBR/LSR to reset interrupt | t _{RINT} | 4,5,6,7,8 | C _L = 100 pF | 150 | ns |

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | ALT. SYMBOL | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|------------------|--------|-------------------------|-----|-----|-------------------|
| ^t d15 | Delay time, initial write to transmit start | ^t IRS | 9 | | 8 | 24 | baudout cycles |
| ^t d16 | Delay time, stop to interrupt | ^t STI | 9 | | 8 | 8 | baudout cycles |
| td17 | Delay time, write THR to reset interrupt | tHR | 9 | C _L = 100 pF | | 140 | ns |
| t _{d18} | Delay time, initial write to interrupt (THRE) | ^t SI | 9 | | 16 | 32 | baudout cycles |
| t _{d19} | Delay time, read IIR to reset interrupt (THRE) | tiR | 9 | C _L = 100 pF | | 140 | ns |
| t _{d20} | Delay time, write to TXRDY inactive | twxı | 10,11 | C _L = 100 pF | | 195 | ns |
| t _{d21} | Delay time, start to TXRDY active . | t _{SXA} | 10,11 | C _L = 100 pF | | 8 | baudout cycles |

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | ALT. SYMBOL | FIGURE | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|------------------|--------|-------------------------|-----|-----|------|
| t _{d22} | Delay time, write MCR to output | tMDO | 12 | C _L = 100 pF | | 100 | ns |
| t _{d23} | Delay time, modem interrupt to set interrupt | t _{SIM} | 12 | C _L = 100 pF | | 170 | ns |
| t _{d24} | Delay time, read MSR to reset interrupt | tRIM | 12 | C _L = 100 pF | | 140 | ns |

NOTES: 2. Charge and discharge time is determined by VOL, VOH, and external loading.

^{3.} In FIFO mode RC = 425 ns (minimum) between reads of the receiver FIFO and the status registers (interrupt identification register or line status register).

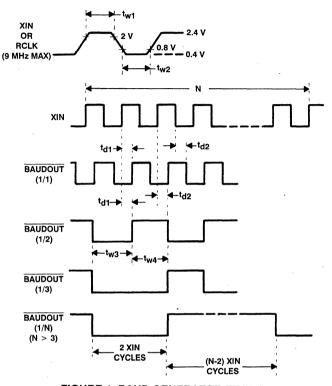
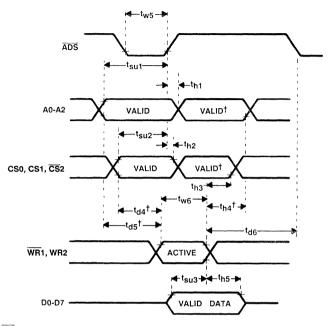
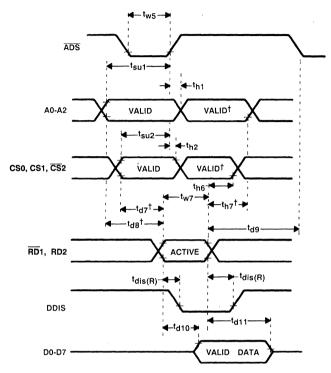


FIGURE 1. BAUD GENERATOR TIMING



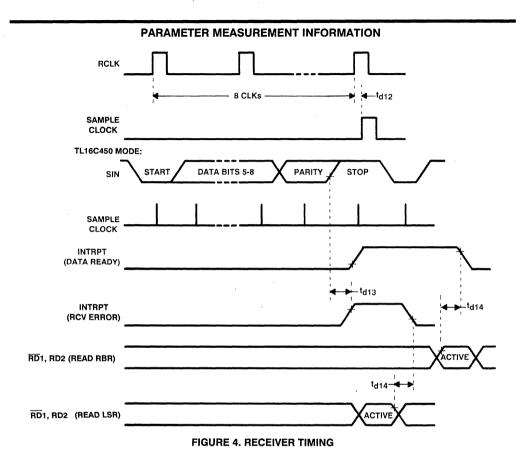
 $^{^\}dagger$ Applicable only when $\widetilde{\text{ADS}}$ is tied low.

FIGURE 2. WRITE CYCLE TIMING



 $^{^{\}dagger}$ Applicable only when $\overline{\text{ADS}}$ is tied low.

FIGURE 3. READ CYCLE TIMING



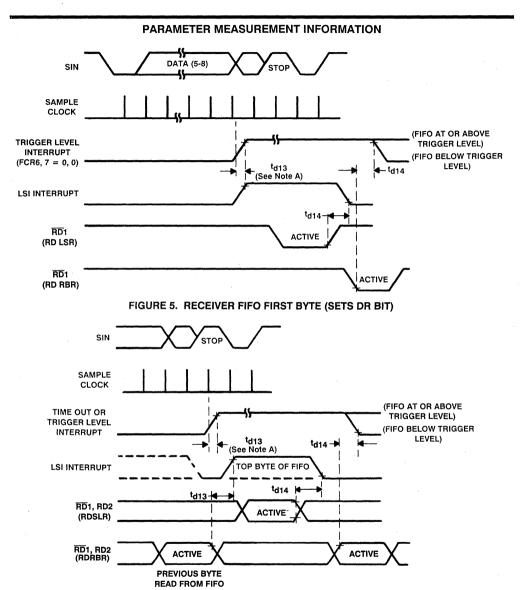
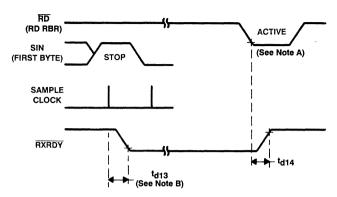


FIGURE 6. RECEIVER FIFO BYTES OTHER THAN THE FIRST BYTE (DR INTERNAL BIT ALREADY SET)

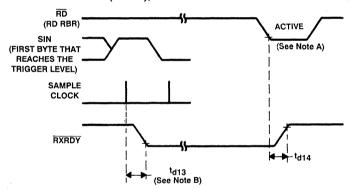
NOTE A: For a timeout interrupt, $t_{d13} = 8$ RCLKs.





NOTES: A.This is the reading of the last byte in the FIFO. B. For a timeout interrupt, t_{d13} = 8 RCLKs.

FIGURE 7. RECEIVER READY (PIN 29), FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0 (MODE 0)



NOTES: A.This is the reading of the last byte in the FIFO. B. For a timeout interrupt, t_{d13} = 8 RCLKs.

FIGURE 8. RECEIVER READY (PIN 29) FCR = 1 AND FCR3 = 1 (MODE 1)

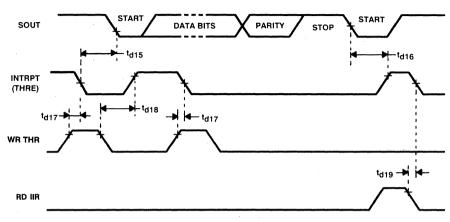


FIGURE 9. TRANSMITTER TIMING

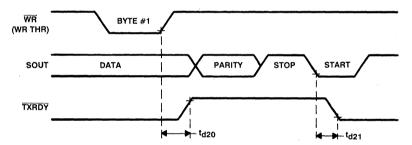


FIGURE 10. TRANSMITTER READY (PIN 24), FCR0 = 0 OR FCR0 = 1 AND FCR3 = 0 (MODE 0)

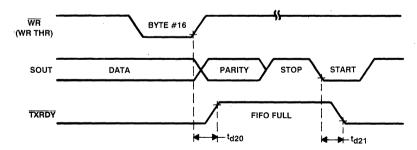


FIGURE 11. TRANSMITTER READY (PIN 24) FCR0 = 1 AND FRCR3 = 1 (MODE 1)



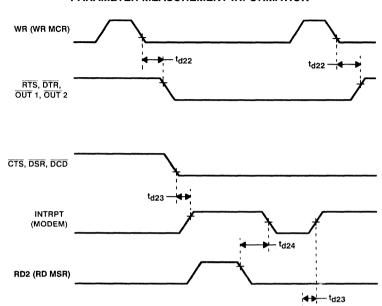


FIGURE 12. MODEM CONTROL TIMING

RI

APPLICATION INFORMATION

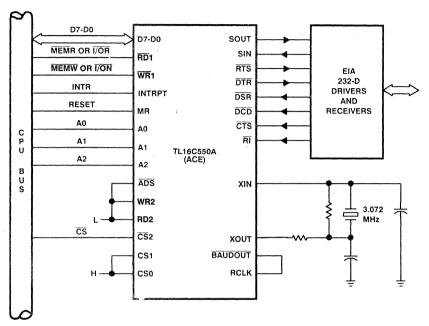


FIGURE 13. BASIC TL16C550A CONFIGURATION

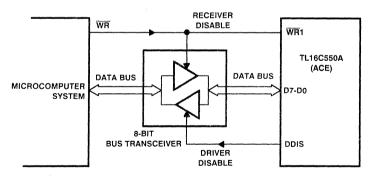


FIGURE 14. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS

APPLICATION INFORMATION TL16C550A ALTERNATE XTAL CONTROL (16)XIN A16-A23 A16-A23 XOUT (12)(15)CS₀ BAUDOUT ADDRESS (13)(9) CS1 RCLK DECODER (14) CS2 CPU DTR 20 (32)1 RTS (25)ADS ADS (34) OUT 1 (35) (31)OUT 2 RSI/ABT MR AD0-A0-A2 (39) AD7 RΪ BUFFER D0-D7 AD0-AD15 (38) DCD 8 PHI2 (37)PHI1 DSR 6 (36) CTS 5 PHI1 PHI2 ADS RSTO (21) (11)RD1 RD 2 SOUT TCU (18)WR1 WR (10) 3 SIN (30) AD0-AD15 INTRPT (24)TXRDY (22)RD2 7 DDIS (19)WR2 (29)RXRDY EIA-232-D CONNECTOR (20)(40) GND 5 V (VSS) (Vcc)

FIGURE 15. TYPICAL TL16C550A CONNECTION TO A CPU

TABLE 1. REGISTER SELECTION

| DLAB | A2 | A1 | A0 | REGISTER | | |
|------|----|----|----|--|--|--|
| 0 | L | L | L | Receiver buffer (read), transmitter holding register (write) | | |
| 0 | L | L | Н | Interrupt enable | | |
| X | L | Н | L | Interrupt identification (read only) | | |
| X | L | Н | L | FIFO control (write) | | |
| X | L. | Н | Н | Line control | | |
| X | Н | L | L | Modem control | | |
| X | Н | L | Н | Line status | | |
| X | Н | Н | L | Modem status | | |
| X | Н | Н | Н | Scratch | | |
| 1 | L | L | L | Divisor latch (LSB) | | |
| 1 | L | L | Н | Divisor Latch (MSB) | | |

[†] The Divisor Latch Access Bit (DLAB) is the most significant bit of the Line Control Register. The DLAB signal is controlled by writing to this bit location (see Table 3).

TABLE 2. ACE RESET FUNCTIONS

| REGISTER/SIGNAL | RESET CONTROL | RESET STATE |
|---|--------------------------|---|
| Interrupt Enable Register | Master Reset | All bits low (0-3 forced and 4-7 permanent) |
| Interrupt Identification Register | Master Reset | Bit 0 is high, bits 1-3 are low, and bits 4-7 are permanently low |
| FIFO Control Register | Master Reset | All bits low |
| Line Control Register | Master Reset | All bits low |
| Modem Control Register | Master Reset | All bits low (5-7 permanent) |
| Line Status Register | Master Reset | Bits 5 and 6 are high, all other bits are low |
| Modem Status Register | Master Reset | Bits 0-3 are low, bits 4-7 are input signals |
| SOUT | Master Reset | High |
| INTRPT (Receiver Error Flag) | Read LSR/MR | Low |
| INTRPT (Received Data Available) | Read RBR/MR | Low |
| INTRPT (Transmitter Holding Register Empty) | Read IIR/Write THR/MR | Low |
| INTRPT (Modern Status Changes) | Read MSR/MR | Low |
| OUT 2 | Master Reset | High |
| RTS | Master Reset | High |
| DTR | Master Reset | High |
| OUT 1 | Master Reset | High |
| Scratch Register | Master Reset | No effect |
| Divisor Latch (LSB and MSB) Registers | Master Reset | No effect |
| Receiver Buffer Registers | Master Reset | No effect |
| Transmitter Holding Registers | Master Reset | No effect |
| RCVR FIFO | MR/FCR1·FCR0/ ΔFCR0 | All bits low |
| XMIT FIFO | MR/FCR2·FCR0/ ΔFCR0 | All bits low |

accessible registers

The system programmer, via the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers are used to control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

TABLE 3. SUMMARY OF ACCESSIBLE REGISTERS

| <u> </u> | | | | | | REGISTER | ADDRESS | | | | | |
|------------|--|---|---|---|--|---|------------------------------------|--|--|---------------------|---------------------------|----------------|
| ĺ | 0 DLAB = 0 | 0 DLAB=0 | 1 DLAB=0 | 2 | 2 | 3 | 4 | 5 | 6 | 7 | 0 DLAB = 1 | 1 DLAB=1 |
| Bit No. | Receiver Buffer Register (Read Only) | Transmitter Holding Register (Write Only) | Interrupt Enable Register | Interrupt Ident. Register (Read Only) | FIFO Control Register (Write Only) | Line Control Register | MODEM Control Register | Line Status Register | MODEM Status Register | Scratch Register | Divisor Latch (LSB) | Latch (MSB) |
| | RBR | THR | IER | IIR | FCR | LCR | MCR | LSR* | MSR | SCR | DLL | DLM |
| 0 | Data Bit 0 [†] | Data Bit 0 | Enable Received Data Available Interrupt (ERBI) | "0" if Interrupt Pending | FIFO Enable | Word Length Select Bit 0 (WLS0) | Data Terminal Ready (DTR) | Data Ready (DR) | Delta Clear to Send (ΔCTS) | Bit 0 | Bit 0 | Bit 8 |
| 1 | Data Bit 1 | Data Bit 1 | Enable Transmitter Holding Register Empty Interrupt (ETBEI) | Interrupt ID Bit (0) | Receiver FIFO Reset | Word Length Select Bit 1 (WLS1) | Request to Send (RTS) | Overrun Error (OE) | Delta Data Set Ready (ΔDSR) | Bit 1 | Bit 1 | Bit 9 |
| 2 | Data Bit 2 | Data Bit 2 | Enable Receiver Line Status Interrupt (ELSI) | Interrupt ID Bit (1) | Transmitter FIFO Reset | Number of Stop Bits (STB) | Out 1 | Parity Error (PE) | Trailing Edge Ring Indicator (TERI) | Bit 2 | Bit 2 | Bit 10 |
| 3 | Data Bit 3 | Data Bit 3 | Enable MODEM Status Interrupt (EDSSI) | Interrupt ID Bit (2) (Note 4) | DMA Mode Select | Parity Enable (PEN) | Out 2 | Framing Error (FE) | Delta Data Carrier Detect (\DCD) | Bit 3 | Bit 3 | Bit 11 |
| 4 | Data Bit 4 | Data Bit 4 | 0 | 0 | Reserved | Even Parity Select (EPS) | Loop | Break Interrupt (BI) | Clear to Send (CTS) | Bit 4 | Bit 4 | Bit 12 |
| 5 | Data Bit 5 | Data Bit 5 | 0 | 0 | Reserved | Stick Parity | 0 | Transmitter Holding Register (THRE) | Data Set Ready (DSR) | Bit 5 | Bit 5 | Bit 13 |
| 6 | Data Bit 6 | Data Bit 6 | 0 | FIFOs Enabled (Note 4) | Receiver Trigger (LSB) | Set Break | 0 | Transmitter Empty (TEMT) | Ring Indicator (RI) | Bit 6 | Bit 6 | Bit 14 |
| 7 | Data Bit 7 | Data Bit 7 | 0 | FIFOs Enabled (Note 4) | Receiver Trigger (MSB) | Divisor Latch Access Bit (DLAB) | 0 | Error in RCVR FIFO (Note 4) | Data Carrier Detect (DCD) | Bit 7 | Bit 7 | Bit 15 |

[†] Bit 0 is the least significant bit. It is the first bit serially transmitted or received. NOTE 4: These bits are always 0 in the TL16C450 mode.

receiver buffer register (RBR)

The ACE's receiver section consists of a Receiver Shift Register (RSR) and a Receiver Buffer Register (RBR). The RBR is actually a 16-byte FIFO. Timing is supplied by the 16 X Receiver Clock (RCLK). Receiver section control is a function of the ACE's Line Control Register.

The ACE's RSR receives serial data from the Serial Input (SIN) pin. The RSR then deserializes the data and moves it into the RBR FIFO. In the TL16C450 mode, when a character is placed in the Receiver Buffer Register and the Received Data Available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the Receiver Buffer Register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO Control Register.

transmitter holding register (THR)

The ACE's transmitter section consists of a Transmitter Holding Register (THR) and a Transmitter Shift Register (TSR). The THR is actually a 16-byte FIFO. Timing is supplied by the Baud Out (BAUDOUT) clock signal. Transmitter section control is a function of the ACE's Line Control Register.

The ACE THR receives data off the Internal Data Bus and, when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at the Serial Output (SOUT). In the TL16C450 mode, if the THR is empty and the Transmitter Holding Register Empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

interrupt enable register (IER)

The Interrupt Enable Register enables each of the five types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. The Interrupt Enable Register can also be used to disable the interrupt system by setting bits 0 through 3 to logic 0. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. This bit, when set to logic 1, enables the Received Data Available interrupt.
- Bit 1. This bit, when set to logic 1, enables the Transmitter Holding Register Empty interrupt.
- Bit 2. This bit, when set to logic 1, enables the Receiver Line Status interrupt.
- Bit 3. This bit, when set to logic 1, enables the Modern Status interrupt.
- Bits 4 thru 7. Bits 4 through 7 in the Interrupt Enable Register are not used and are always set to logic 0.

FIFO control register

The FIFO control register (FCR) is a write-only register at the same location as the IIR, which is a read-only register. The FCR is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

- Bit 0. FCR0, when set to logic 1, enables the transmit and receive FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed. Changing this bit clears the FIFOs.
- Bit 1. FCR1, when set to logic 1, clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 2. FCR2, when set to logic 1, clears all bytes in the transmit FIFO and resets its counter to 0. The shift register is not cleared. The 1 that is written to this bit position is self clearing.
- Bit 3. If FCR0 is a 1, setting FCR3 to a 1 causes the RXRDY and TXRDY to change from mode 0 to mode 1.



Bits 4 and 5. FCR4 and FCR5 are reserved for future use.

Bits 6 and 7. FCR6 and FCR7 are used to set the trigger level for the receiver FIFO interrupt.

| BIT 7 | BIT 6 | RECEIVER FIFO TRIGGER LEVEL (BYTES) |
|-------|-------|--|
| 0 | 0 | 01 |
| o | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

The ACE provides four prioritized levels of interrupts:

Priority 1 — Receiver line status (highest priority)

Priority 2 - Receiver data ready or Receiver character timeout

Priority 3 — Transmitter holding register empty

Priority 4 — Modem status (lowest priority)

When an interrupt is generated, the Interrupt Identification Register indicates that an interrupt is pending and the type of that interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4. Detail on each bit are as follows:

Bit 0. This bit can be used either in a hardwire-prioritized, or polled interrupt system. If this bit is a logic 0, an interrupt is pending. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2. These two bits are used to igentify the highest priority interrupt pending, as indicated in Table 4.

Bit 3. This bit is always 0 in the TL16C450 mode. In FIFO mode, this bit is set with bit 2 to indicate that a timeout interrupt is pending.

Bits 4 thru 5. These two bits are not used and are always set at logic 0.

Bits 6 and 7. These two bits are always 0 in the TL16C450 mode. They are set when bit 0 of the FIFO Control Register is equal to 1.

TABLE 4. INTERRUPT CONTROL FUNCTIONS

| ı | INTERRUPT IDENTIFICATION REGISTER | | ł | PRIORITY LEVEL | WITERRUST TYPE WITERRUST COURSE | | INTERRUPT RESET METHOD |
|-------|---|-------|-------|-------------------|------------------------------------|--|--|
| BIT 3 | BIT 2 | BIT 1 | BIT 0 | | | | |
| 0 | 0 | 0 | 1 | None | None | None | - |
| 0 | 1 | 1 | 0 | 1 | Receiver line status | Overrun error, parity error, framing error, or break interrrupt | Reading the Line Status register |
| 1 | 1 | 0 | 0 | 2 | Received data available | Receiver data available in the TL16C450 mode or trigger level reached in the FIFO mode. | Reading the Receiver buffer Buffer register |
| 1 | 1 | 0 | 0 | 2 | Character timeout indication | No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time | Reading the Receiver Buffer Register |
| 0 | 0 | 1 | 0 | 3 | Transmitter Holding register empty | Transmitter Holding register empty | Reading the Interrupt Identification register (if source of interrupt) or writing into the Transmitter Holding register |
| 0 | 0 | 0 | 0 | 4 | Modem status | Clear to Send, Data Set Ready, Ring Indicator, or Data Carrier Detect | Reading the Modem Status register |

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the Line Control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the Line Control register; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described below.

Bits 0 and 1. These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as follows:

| Bit 1 | Bit 0 | Word Length |
|-------|-------|-------------|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2. This bit specifies either one, one and one-half, or two Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the data. If bit 2 is a logic 1, the number of Stop bits generated is dependent on the word length selected with bits 0 and 1. The receive clocks the first stop bit only, regardless of the number of stop bits selected. The number of Stop bits generated, in relation to word length and bit 2, is shown in the following.

| Bit 2 | Word Length Selected by Bits 1 and 2 | Number of Stop Bits Generated |
|-------|---|----------------------------------|
| 0 | Any word length | 1 |
| 1 | 5 bits | 1 1/2 |
| 1 | 6 bits | 2 |
| 1 | 7 bits | 2 |
| 1 | 8 bits | 2 |

- Bit 3. This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is a logic 1, parity is checked. When bit 3 is a logic 0, no parity is generated or checked.
- Bit 4. Bit 4 is the Even Parity Select bit. When parity is enabled by bit 3: a logic 1 in bit 4 produces Even Parity (an even number of logic 1s in the data and parity bits) and a logic 0 in bit 4 produces Odd Parity (an odd number of logic 1s).
- Bit 5. This is the Stick parity bit. When bits 3, 4, and 5 are logic 1s, the Parity bit is transmitted and checked as a logic 0. When bits 3 and 5 are logic 1s and bit 4 is a logic 0, the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0, stick parity is disabled.
- Bit 6. This bit is the Break Control bit. Bit 6 is set to a logic 1 to force a break condition, i.e, a condition where the Serial Output (SOUT) pin is forced to the spacing (logic 0) state. When bit 6 is set to a logic 0, the break condition is disabled. The break condition has no effect on the transmitter logic; it only effects the serial output.
- Bit 7. This bit is the Divisor Latch Access bit (DLAB). Bit 7 must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or write. Bit 7 must be set to a logic 0 during a read or write to access the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

modem control register (MCR)

The Modem Control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modern. The contents of this register are summarized in Table 3 and are described below.

Bit 0. Bit 0 (DTR) controls the Data Terminal Ready (DTR) output, Setting this bit to a logic 1 forces the DTR output to its low state. When bit 0 is set to a logic 0, DTR goes high.

Bit 1. Bit 1 (RTS) controls the Request to Send (RTS) output in a manner identical to Bit 0's control over the DTR output.

Bit 2. Bit 2 (OUT 1) controls the Output 1 (OUT 1) signal, a user-designated output signal, in a manner identical to Bit 0's control over the DTR output.

Bit 3. Bit 3 (OUT 2) controls the Output 2 (OUT 2) signal, a user-designated output signal, in a manner identical to Bit 0's control over the DTR output.

Bit 4. Bit 4 provides a local loopback feature for diagnostic testing of the ACE. When this bit is set to a logic high, the following occurs:

- 1. The transmitter Serial Output (SOUT) is set high.
- 2. The receiver Serial Input (SIN) is disconnected.
- 3. The output of the Transmitter Shift register is looped back into the Receiver Shift register input.
- 4. The four modem control inputs (CTS, DSR, DCD, and RI) are disconnected.
- 5. The four modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs.
- 6. The four modem control output pins are forced to their inactive states (high).

In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit- and receive-data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt's sources are now the lower four bits of the Modem Control register instead of the four modem control inputs. All interrupts are still controlled by the Interrupt Enable register.

Bit 5 through 7. These bits are permanently set to logic 0.

line status register (LSR)†

The Line Status Register provides information to the CPU concerning the status of data transfers. The contents of this register are described below and summarized in Table 3.

Bit 0. Bit 0 is the Data Ready (DR) indicator for the receiver. This bit is set to a logic 1 condition whenever a complete incoming character has been received and transferred into the Receiver Buffer register or the FIFO and is reset to logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1[‡]. Bit 1 is the Overrun Error (OE) indicator. When this bit is set to logic 1, it indicates that before the character in the Receiver Buffer register was read, it was overwritten by the next character transferred into the register. The OE indicator is reset every time the CPU reads the contents of the Line Status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but is not transferred to the FIFO.

Bit 2[‡]. Bit 2 is the Parity Error (PE) indicator, When this bit is set to logic 1, it indicates that the parity of the received data character does not match the parity selected in the Line Control Register (bit 4). The PE bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is

[‡] Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.



[†] The Line Status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3[‡]. Bit 3 is the Framing Error (FE) indicator. When this bit is set to logic 1, it indicates that the received character did not have a valid (logic 1) Stop bit. The FE bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The ACE will try to resynchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit. The ACE then samples this start bit twice and then accepts the input data.

Bit 4[‡]. Bit 4 is the Break Interrupt (BI) indicator. When this bit is set to logic 1, it indicates that the received data input was held in the logic 0 state for longer than a full-word transmission time. A "full-word transmission time" is defined as the total time of the Start, Data, Parity, and Stop bits. The BI bit is reset every time the CPU reads the contents of the Line Status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs, only one 0 character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Bit 5. Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. This bit is set to logic 1 when the Transmitter Holding Register is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is a logic 1, then an interrupt is generated. THRE is set to a logic 1 when the contents of the Transmitter Holding Register are transferred to the transmitted Shift Register. This bit is reset to logic 0 concurrent with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

Bit 6. Bit 6 is the Transmitter Empty (TEMT) indicator. This bit is set to a logic 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. When either the Transmitter Holding register or the Transmitter Shift register contains a data character, the TEMT bit is reset to logic 0. In the FIFO mode, this bit is set to a 1 when the transmitter FIFO and shift register are both empty.

Bit 7. In the TL16C550A, this bit is always reset to logic 0. In the TL16C450 mode, this bit is always a 0. In the FIFO mode, LSR7 is set when there is at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.

[‡] Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt.

modem status register (MSR)

The Modem Status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state, the appropriate bit is set to logic 1. All four bits are reset to logic 0 when the CPU reads the Modem Status register. The contents of this register are summarized in Table 3 and are described below.

- Bit 0. Bit 0 is the change in Clear to Send (DCTS) indicator. This bit indicates that the CTS input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modern Status Interrupt is enabled, a Modern Status Interrupt is generated.
- Bit 1. Bit 1 is the change in Data Set Ready (DDSR) indicator. This bit indicates that the $\overline{\rm DSR}$ input has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modern Status Interrupt is enabled, a Modern Status Interrupt is generated.
- Bit 2. Bit 2 is the Trailing Edge of Ring Indicator (TERI) detector. This bit indicates that the $\overline{\rm RI}$ input to the chip has changed from a low to a high state. When this bit is a logic 1 and the Modern Status Interrupt is enabled, a Modern Status Interrupt is generated.



Bit 3. Bit 3 is the change in Data Carrier Detect (DDCD) indicator. This bit indicates that the \overline{DCD} input to the chip has changed state since the last time it was read by the CPU. When this bit is a logic 1 and the Modem Status Interrupt is enabled, a Modem Status Interrupt is generated.

Bit 4. Bit 4 is the compliment of the Clear to Send (CTS) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control register bit 1 (RTS).

Bit 5. Bit 5 is the compliment of the Data Set Ready (DSR) input. If Bit 4 (loop) of the Modern Control register is set to a logic 1, this bit is equivalent to the Modern Control register bit 0 (DTR).

Bit 6. Bit 6 is the compliment of the Ring Indicator (RI) input. If Bit 4 (loop) of the Modern Control register is set to a logic 1, this bit is equivalent to the Modern Control registers bit 2 (OUT 1).

Bit 7. Bit 7 is the compliment of the Data Carrier Detect (\overline{DCD}) input. If Bit 4 (loop) of the Modem Control register is set to a logic 1, this bit is equivalent to the Modem Control registers bit 3 (OUT 2).

scratch register (SCR)

The Scratch register is an 8-bit register that is intended for the programmer's use as a "scratchpad," in the sense that it will temporarily hold the programmer's data without affecting any other ACE operation.

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 8 MHz and divides it by a divisor in the range between 1 and $2^{16}-1$. The output frequency of the baud generator is sixteen times (16 X) the baud rate. The formula for the divisor is:

divisor # = XIN frequency input ÷ (desired baud rate X 16)

Two 8-bit registers, called divisor latches, are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 5 and 6, which follow, illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

FIFO interrupt-mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) receiver interrupts will occur as follows:

- The Receive Data Available interrupt will be issued to the microprocessor when the FIFO has reached its programmed trigger level. It will be cleared as soon as the FIFO drops below its programmed trigger level.
- The IIR Receive Data Available indication also occurs when the FIFO trigger level is reached, and, like the interrupt, it is cleared when the FIFO drops below the trigger level.
- 3. The Receiver Line Status interrupt (IIR = 06), as before, has higher priority than the Received Data Available (IIR = 04) interrupt.
- 4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts will occur as follows:

- 1. FIFO timeout interrupt will occur if the following conditions exist:
 - a. At least one character is in the FIFO.
 - b. The most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).



- The most recent microprocessor read of the FIFO was longer than 4 continuous character times ago.
- This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12-bit character.
- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
- When a timeout interrupt has occurred, it is cleared and the timer reset when the microprocessor reads one character from the receiver FIFO.
- 4. When a timeout interrupt has not occurred, the timeout timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts will occur as follows:

- 1. The Transmitter Holding Register interrupt (02) occurs when the transmit FIFO is empty. It is cleared as soon as the Transmitter Holding Register is written to (1 to 16 characters may be written to the transmit FIFO while servicing this interrupt) or the IIR is read.
- The Transmit FIFO Empty indications will be delayed 1 character time minus the last stop bit time
 when the following occurs: THRE = 1 and there have not been at least two bytes at the same time in
 the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be
 immediate, if it is enabled.

Character timeout and receiver FIFO trigger level interrupts have the same priority as the current Received Data Available interrupt; Transmit FIFO Empty has the same priority as the current Transmitter Holding Register Empty interrupt.

FIFO polled-mode operation

With FCR0 = 1, resetting IER0, IER1, IER2, IER3, or all four to 0 puts the ACE in the FIFO Polled Mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, the user program will check receiver and transmitter status via the LSR. As stated previously:

- 1. LSR0 will be set as long as there is one byte in the receiver FIFO.
- LSR1 through LSR4 will specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2 = 0.
- 3. LSR5 will indicate when the transmit FIFO is empty.
- 4. LSR6 will indicate that both the transmit FIFO and shift registers are empty.
- 5. LSR7 will indicate whether there are any errors in the receiver FIFO.

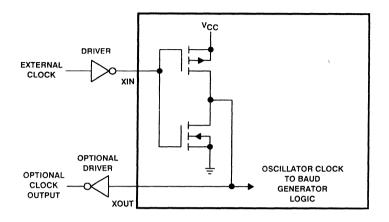
There is no trigger level reached or timeout conditions indicated in the FIFO Polled Mode. However, the receiver and transmit FIFOs are still fully capable of holding characters.

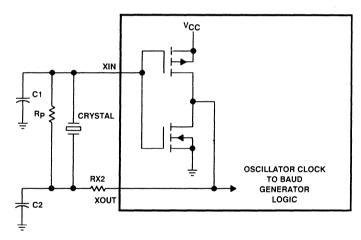
TABLE 5. BAUD RATES USING A 1.8432-MHz CRYSTAL

| DESIRED BAUD RATE | DIVISOR USED TO GENERATE 16 X CLOCK | PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL |
|----------------------|---|---|
| 50 | 2304 | |
| 75 | 1536 | |
| 110 | 1047 | 0.026 |
| 134.5 | 857 | 0.058 |
| 150 | 768 | |
| 300 | 384 | |
| 600 | 192 | |
| 1200 | 96 | |
| 1800 | 64 | |
| 2000 | 58 | 0.69 |
| 2400 | 48 | |
| 3600 | . 32 | |
| 4800 | 24 | |
| 7200 | 16 | |
| 9600 | 12 | |
| 19200 | 6 | |
| 38400 | 3 | |
| 56000 | 2 | 2.86 |

TABLE 6. BAUD RATES USING A 3.072-MHz CRYSTAL

| DESIRED BAUD RATE | DIVISOR USED TO GENERATE 16 X CLOCK | PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL |
|----------------------|---|---|
| 50 | 3840 | |
| 75 | 2560 | |
| 110 | 1745 | 0.026 |
| 134.5 | 1428 | 0.034 |
| 150 | 1280 | |
| 300 | 640 | |
| 600 | 320 | |
| 1200 | 160 . | |
| 1800 | 107 | 0.312 |
| 2000 | 96 | |
| 2400 | 80 | |
| 3600 | 53 | 0.628 |
| 4800 | 40 | |
| 7200 | 27 | 1.23 |
| 9600 | 20 | |
| 19200 | 10 | |
| 38400 | 5 | |





TYPICAL CRYSTAL OSCILLATOR NETWORK

| CRYSTAL | Rp | RX2 | C1 | C2 |
|---------|------|--------|----------|----------|
| 3.1 MHz | 1 ΜΩ | 1.5 kΩ | 10-30 pF | 40-60 pF |
| 1.8 MHz | 1 ΜΩ | 1.5 kΩ | 10-30 pF | 40-60 pF |

FIGURE 16. TYPICAL CLOCK CIRCUITS

uA9636AC DUAL LINE DRIVERS WITH ADJUSTABLE SLEW RATE

D2608, OCTOBER 1980-REVISED SEPTEMBER 1986

- Meets EIA Standards RS-423-A and RS-232-C and Federal Standard 1030
- Slew Rate Control
- Output Short-Circuit-Current Limiting
- Wide Supply Voltage Range
- 8-Pin Package
- Designed to Be Interchangeable With Fairchild 9636A

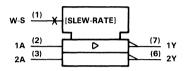
description

The uA9636AC is a dual single-ended line driver designed to meet EIA Standards RS-423-A and RS-232-C and Federal Standard 1030. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS} , connected between the wave-shape-control terminal and ground. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diodeprotected against negative transients. This device operates from $\pm\,12$ V and is supplied in an 8-pin package.

The uA9636AC is characterized for operation from 0°C to 70°C.

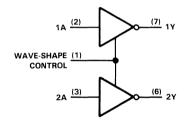
D, JG, OR P PACKAGE (TOP VIEW) W-S 1 0 8 VCC + 1A 2 7 1Y 2A 3 6 2Y GND 4 5 VCC -

logic symbol†

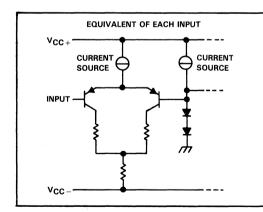


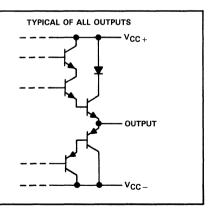
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Positive supply voltage range, V _{CC+} (see Note 1) V _{CC-} to 15 V |
|---|
| Negative supply voltage range, VCC |
| Output voltage ±15 V |
| Output current |
| Continuous total power dissipation (see Note 2) See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D and P packages |

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. In the JG package, uA9636AC chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| JG | 825 mW | 6.6 mW/°C | 528 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|--------|------|-------|------|
| Positive supply voltage, V _{CC+} | 10.8 | 12 | 13.2 | V |
| Negative supply voltage, V _{CC} _ | - 10.8 | - 12 | -13.2 | V |
| High-level input voltage, VIH | 2 | | | ٧ |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Wave-shaping resistor, RWS | 10 | | 1000 | kΩ |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended range of free-air temperature, supply voltage, and waveshaping resistance (unless otherwise noted)

| | PARAMETER | TEST COL | NDITIONS | MIN | TYP [†] | MAX | UNIT |
|----------------|---|------------------------------|-------------------------------------|-----|------------------|-------|-------|
| | TANAMETER | 1251 001 | NDITIONS | (S | ee Note | 3) | Oitii |
| VIK | Input clamp voltage | $I_i = -15 \text{ mA}$ | | | -1.1 | -1.5 | V |
| | | | R _L = ∞ | 5 | 5.6 | 6 | |
| Vон | High-level output voltage | V _I = 0.8 V | $R_L = 3 k\Omega$ to ground | 5 | 5.6 | 6 | V |
| | | | $R_L = 450 \Omega$ to ground | 4 | 5.4 | 6 | |
| | | | R _L = ∞ | -6 | - 5.7 | 5 | |
| VOL | Low-level output voltage | V _I = 2 V | $R_L = 3 k\Omega$ to ground | -6 | -5.6 | - 5 | V |
| | | | $R_L = 450^{\circ}\Omega$ to ground | -6 | - 5.4 | -4 | |
| 1 | High level in the summer | V ₁ = 2.4 V | | | | 10 | |
| ήн | High-level input current | $V_1 = 5.5 \text{ V}$ | | | | 100 | μΑ |
| 1 _L | Low-level input current | V _I = 0.4 V | | | - 20 | 80 | μА |
| lo | Output current (power off) | $V_{CC\pm}=0$, | V _O = ±6 V | | | ± 100 | μΑ |
| | Short-circuit output current [‡] | V ₁ = 2 V | | 15 | 25 | 150 | ^ |
| los | Short-circuit output current | V _I = 0 | | -15 | -40 | - 150 | mA |
| ro | Output resistance | $R_L = 450 \Omega$ | | | 25 | 50 | Ω |
| | D | $V_{CC} = \pm 12 \text{ V},$ | V _I = 0, | | 13 | 18 | |
| ICC+ | Positive supply current | $R_{WS} = 100 k\Omega$ | Output open | | 13 | 18 | mA |
| 1 | Nogative cumbic current | $V_{CC} = \pm 12 V$, | V _I = 0, | | -13 | - 18 | ^ |
| ICC - | Negative supply current | $R_{WS} = 100 k\Omega$ | Output open | | -13 | - 18 | mA |

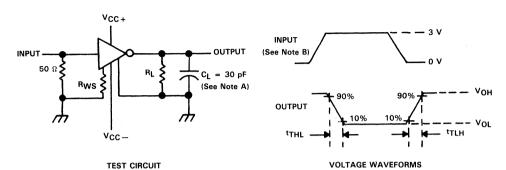
switching characteristics, $VCC \pm = 12 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$, see Figure 1

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------|---|----------------------|--------------------------------|-----|-----|-----|------|
| | | | $R_{WS} = 10 k\Omega$ | 0.8 | 1.1 | 1.4 | |
| tTLH | Transition time, low-to-high-level output | $R_L = 450 \Omega$, | $R_{WS} = 100 k\Omega$ | 8 | 11 | 14 | |
| | | $C_L = 30 pF$ | $R_{WS} = 500 k\Omega$ | 40 | 55 | 70 | μS |
| | | | $R_{WS} = 1 M\Omega$ | 80 | 110 | 140 | |
| | Transition time, high-to-low-level output | | $R_{WS} = 10 k\Omega$ | 0.8 | 1.1 | 1.4 | |
| | | $R_L = 450 \Omega$, | $R_{WS} = 100 \text{ k}\Omega$ | 8 | 11 | 14 | _ |
| tTHL | | $C_L = 30 pF$ | $R_{WS} = 500 \text{ k}\Omega$ | 40 | 55 | 70 | μS |
| | | | $R_{WS} = 1 \text{ m}\Omega$ | 80 | 110 | 140 | |

 $^{^{\}dagger}All$ typical values are at V_{CC} \pm 12 V, T_A = 25 °C. $^{\ddagger}Not$ more than one output should be shorted to ground at a time.

NOTE 3: The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when -5 V is the maximum, the minimum is a more-negative voltage.

PARAMETER MEASUREMENT INFORMATION

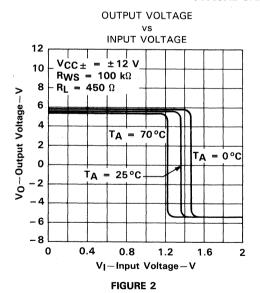


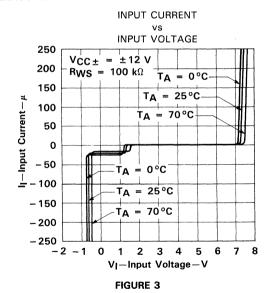
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_0 = 50 \Omega$, PRR ≤ 1 kHz, duty cycle = 50%.

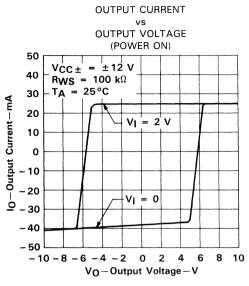
FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS



OUTPUT CURRENT OUTPUT VOLTAGE (POWER OFF) 100 Vcc± 80 $V_1 = 0$ 60 -Output Current−μA TA = 25°C 40 20 0 -- 20 -40 0 -60 -80-100 8 10 -10-8-6-4 2 0 2 4 Vo-Output Voltage-V

FIGURE 4

FIGURE 5

TRANSITION TIMES

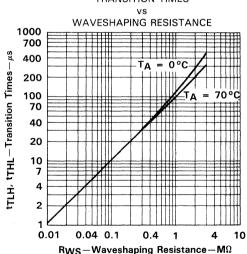


FIGURE 6

FIGURE 7. RS-423-A SYSTEM APPLICATION

uA9637AM, uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

D2609, SEPTEMBER 1980-REVISED NOVEMBER 1986

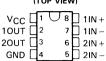
- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line and "Small Outline" Packages
- Similar to SN75157 except for Corner V_{CC} and Ground Pin Positions
- Designed to Be Interchangeable with Fairchild µA9637A

description

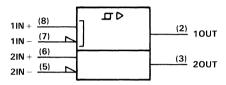
The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-inline package and small outline package.

The uA9637AM is characterized over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The uA9637AC is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

uA9637M . . . JG PACKAGE uA9637C . . . D, JG, OR P PACKAGE (TOP VIEW)

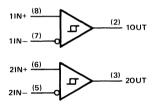


logic symbol†

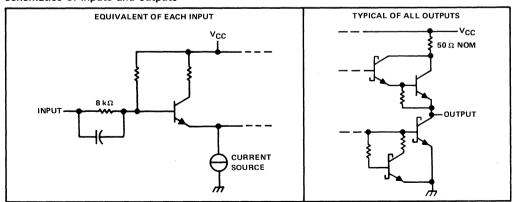


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



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uA9637AM, uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|---|
| Input voltage |
| Differential input voltage (see Note 2) |
| Output voltage (see Note 1) |
| Low-level output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| D package |
| JG package: uA9637AM |
| uA9637AC |
| P package |
| Operating free-air temperature range: uA9637AM55°C to 125°C |
| uA9637AC 0 °C to 70 °C |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or P package |

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.

- 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
- 3. For operation above 25°C free-air temperature, derate linearly at the following rates: 5.8 mW/°C for the D package, 8.4 mW/°C for uA9637AM in the JG package, 6.6 mW/°C for uA9637AC in the JG package, and 8.0 mW/°C for the P package.

recommended operating conditions

| | u. | A9637A | M | u/ | 9637A | С | UNIT | |
|--|------|--------|-----|------|-------|------|------|--|
| | MIN | NOM | MAX | MIN | NOM | MAX | UNIT | |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4,75 | 5 | 5.25 | V | |
| Common-mode input voltage, V _{IC} | | | ±7 | | | ± 7 | V | |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C | |

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

| | PARAMETER | TEST CONDI | TIONS | 1 | TYP [†] | | UNIT | |
|------------------------|--|---|-------------------------|------|------------------|--------|------|--|
| T PAIR TER | | ,, | | Se | See Note 4 | | | |
| VT | Threshold voltage (V _{T+} and V _{T-}) | | | -0.2 | | 0.2 | V | |
| v T I nresnoid voitage | Threshold voltage (V + and V =) | See Note 5 | | -0.4 | | 0.4 | l * | |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | | | | 70 | | mV | |
| VOH | High-level output voltage | $V_{ID} = 0.2 V$ | $I_0 = -1 \text{ mA}$ | 2.5 | 3.5 | | V | |
| VOL | Low-level output voltage | $V_{ID} = -0.2 V$, | I _O = 20 mA | | 0.35 | 0.5 | V | |
| l ₁ | Input current | $V_{CC} = 0 \text{ to } 5.5 \text{ V},$ | V _I = 10 V | | 1.1 | 3.25 | mA | |
| " | input current | See Note 6 | V _I = -10 V | | - 1.6 | - 3.25 | IIIA | |
| los | Short-circuit output current [‡] | V _O = 0, | V _{ID} = 0.2 V | -40 | - 75 | - 100 | mA | |
| Icc | Supply current | $V_{ID} = -0.5 V$, | No load | | 35 | 50 | mA | |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

- 5. The expanded threshold parameter is tested with a 500- Ω resistor in series with each input.
- 6. The input not under test is grounded.



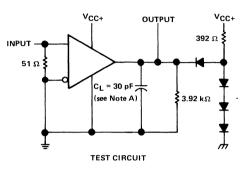
^{*}Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

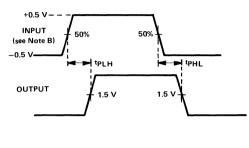
NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

switching characteristics, VCC = 5 V, TA = 25°C

| Γ | PARAMETER | TEST CONDITION | | TYP | MAX | UNIT |
|----|--|--------------------------------------|--|-----|-----|------|
| tı | PLH Propagation delay time, low-to-high-level output | C _I = 30 pF, See Figure 1 | | 15 | 25 | ns |
| ti | PHL Propagation delay time, high-to-low-level output | CL = 30 pr, See rigure r | | 13 | 25 | ns |

PARAMETER MEASUREMENT INFORMATION





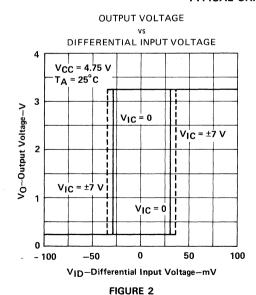
VOLTAGE WAVEFORM

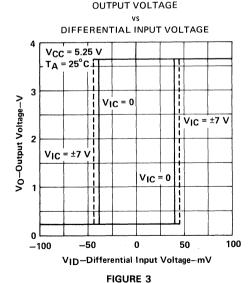
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_f \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

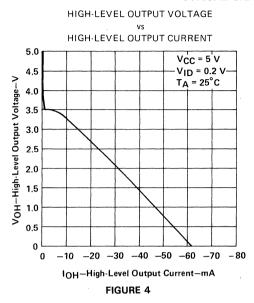
TYPICAL CHARACTERISTICS

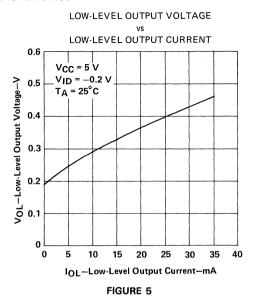




TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS





SUPPLY CURRENT SUPPLY VOLTAGE 100 No load 90 Inputs open $T_{\Delta} = 25^{\circ}C$ 80 CC-Supply Current-mA 70 60 40 30 20 10 0 0 1 2 3 4 7 8 V_{CC}-Supply Voltage-V FIGURE 6

TYPICAL APPLICATION DATA

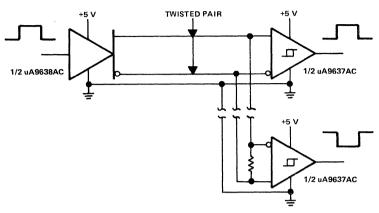


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

D2612, OCTOBER 1980-REVISED SEPTEMBER 1986

- Meets EIA Standard RS-422-A
- Operates From a Single 5-V Supply
- TTL-and CMOS-Input Compatibility
- Output Short-Circuit Protection
- Schottky Circuitry
- Designed to Be Interchangeable With Fairchild 9638

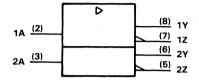
description

The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422-A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

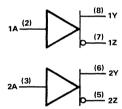
The uA9638C is characterized for operation from 0°C to 70°C.



logic symbol†

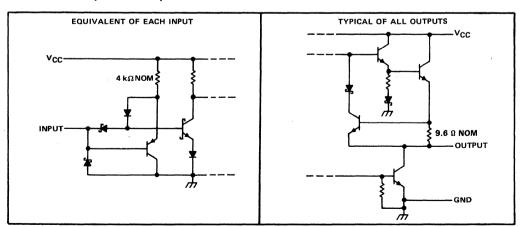


logic diagram



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range, VCC (see Note 1) | -0.5 V to 7 V |
|--|------------------|
| Input voltage range | -0.5 V to 7 V |
| Continuous total power dissipation (see Note 2) See Dissipat | ion Rating Table |
| Operating free-air temperature range | . 0°C to 70°C |
| Storage temperature range | 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package | 300°C |
| Lead temperature 1.6 mm (1/16 inch) from 10 seconds: D and P package | 260°C |

NOTES: 1. Voltage values except differential output voltages are with respect to network ground terminal.

2. In the JG package, uA9638C chips are glass mounted.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| JG | 825 mW | 6.6 mW/°C | 528 mW |
| Р | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| , | MI | N | NOM | MAX | UNIT |
|--|-----|-----|-----|------|------|
| Supply voltage, V _{CC} | 4.7 | 5 . | 5 | 5.25 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | | 0.8 | V |
| High-level output current, IOH | | | | - 50 | mA |
| Low-level output current, IOL | | | | 50 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over operating free-air temperature range (unless otherwise noted)

| P/ | RAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|----------|--|--|--------------------------------|------|------------------|------------------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 \text{ V}, \text{ I}_1 = -18 \text{ m/s}$ | 4 | | -1 | -1.2 | ٧ |
| V | High lavel autout valtage | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ | I _{OH} = -10 mA | 2.5 | 3.5 | | V |
| Vон | High-level output voltage | V _{IL} = 0.8 V | IOH = -40 mA | 2 | | | · · |
| VOL | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ | $V_{IL} = 0.8 V,$ | | | 0.5 | V |
| LVOL. | Low-level output voltage | I _{OL} = 40 mA | | | | 0.5 | |
| VOD1 | Differential output voltage | $V_{CC} = 5.25 \text{ V}, I_{O} = 0$ | | | 2 | V _{OD2} | ٧ |
| VOD2 | Differential output voltage | | | 2 | | | V |
| | Change in magnitude of ‡ | | | | | ±0.4 | V |
| △ VOD | $\frac{\text{VOD}}{\text{differential output voltage}}$ V _{CC} = 4.75 V to 5.25 V, R _I = 100 Ω, See Figure 1 | | - 100 0 Soo Figure 1 | | | 10.4 | |
| Voc | Common-mode output voltage§ | VCC = 4.75 V to 5.25 V, NL = 100 M, See Figure 1 | | | | 3 | > |
| A Voc | Change in magnitude of [‡] | | | | | ±0.4 | ν |
| A1 VOC 1 | common-mode output voltage | | | | | 10.4 | |
| | | | V _O = 6 V | | 0.1 | 100 | |
| 10 | Output current with power off | $V_{CC} = 0$, | $V_0 = -0.25 \text{ V}$ | | -0.1 | - 100 | μΑ |
| | | | $V_0 = -0.25 \text{ V to 6 V}$ | | | ±100 | |
| 11 | Input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$ | | | | 50 | μΑ |
| ΊΗ | High-level input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$ | | | | 25 | μΑ |
| IIL | Low-level input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 0.5 \text{ V}$ | | | | - 200 | μΑ |
| los | Short-circuit output current | $V_{CC} = 5.25 \text{ V}, V_{O} = 0$ | | - 50 | | - 150 | mA |
| Icc | Supply current (all drivers) | V _{CC} = 5.25 V, No load, | All inputs at 0 V | | 45 | 65 | mA |

switching characteristics, VCC = 5 V, TA = 25 °C

| | PARAMETER | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|-----|-------------------------------------|-------------------------|----------------------|-----|-----|-----|------|
| tDD | Differential-output delay time | C ₁ = 15 pF, | $R_{l} = 100 \Omega$ | | 10 | 15 | ns |
| tTD | Differential-output transition time | See Figure 2 | $H_{L} = 100 u$ | | 10 | 15 | ns |
| | Skew | See Figure 2 | | | 1 | | ns |

 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V and T_A = 25 °C. ‡ $^{\Delta}$ | V_{OD}| and $^{\Delta}$ | V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

In EIA Standard RS-422-A, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, VOS. Only one output at a time should be shorted and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

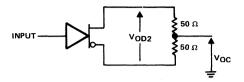
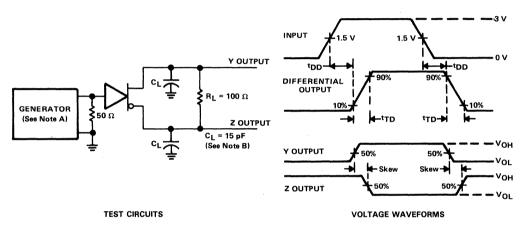


FIGURE 1. DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



NOTES: A. The input pulse generator has the following characteristics: $Z_0 = 50 \Omega$, PRR $\leq 500 \text{ kHz}$, $t_W = 100 \text{ ns}$, $t_\Gamma = \leq 5 \text{ ns}$. B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

D3009, OCTOBER 1986

- Meets EIA Standards RS-422-A and RS-423-A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line and "Small Outline" Packages
- Designed to be Interchangeable with Fairchild μA9639AC

description

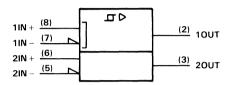
The uA9639C is a dual differential line receiver designed to meet EIA standards RS-422-A and RS-423-A and Federal Standards 1020 and 1030. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package and "small outline" package.

The uA9639C is characterized for operation from 0° C to 70° C.

D, JG, OR P PACKAGE (TOP VIEW)

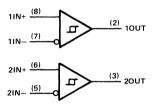
| Vcc 🗖 | U 8 | 🗎 1 IN + |
|----------|-----|----------|
| 10UT 🛚 2 | 7 | 🗌 1IN – |
| 20UT []3 | 6 | 🗌 21N + |
| GND □4 | 5 | 2IN - |

logic symbol†

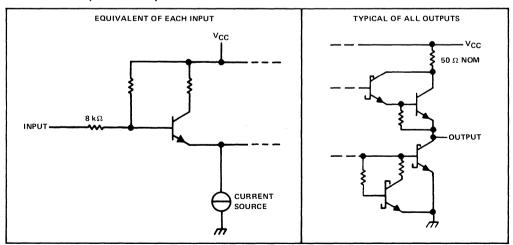


 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



Texas Instruments

Copyright © 1986, Texas Instruments Incorporated

uA9639C DUAL DIFFERENTIAL LINE RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Input voltage |
| Differential input voltage (see Note 2) |
| Output voltage (see Note 1) |
| Low-level output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3): |
| D package |
| JG package |
| P package |
| Operating free-air temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package 260 °C |

- NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
 - 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 - 3. For operation above 25 °C free-air temperature, derate the D package to 464 mW at 70 °C at the rate of 5.8 mW/°C, the JG package to 528 mW at 70 °C at the rate of 6.6 mW/°C, and the P package to 640 mW at 70 °C at the rate of 8.0 mW/°C.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V _{IC} | | | ±7 | V |
| Operating free-air temperature A | 0 | | 70 | °C |

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless othewise noted)

| PARAMETER | | TEST CONDITIONS | | 1 | MIN TYP [†] MAX See Note 4 | | UNIT |
|------------------|--|---|-------------------------|------|--|-------|------|
| VT | Threshold voltage (V _{T+} and V _{T-}) | | | -0.2 | | 0.2 | v |
| | | See Note 5 | | -0.4 | | 0.4 | i |
| V _{hys} | Hysteresis (V _{T+} - V _{T-}) | | | | 70 | | mV |
| Voн | High-level output voltage | $V_{ID} = 0.2 V$ | $I_0 = -1 \text{ mA}$ | 2.5 | 3.5 | | V |
| VOL | Low-level output voltage | $V_{1D} = -0.2 V$, | I _O = 20 mA | | 0.35 | 0.5 | V |
| I. | Input current | $V_{CC} = 0 \text{ to } 5.5 \text{ V},$ | V _I = 10 V | | 1.1 | 3.25 | mA |
| h | | See Note 6 | V _I = -10 V | | -1.6 | -3.25 | A |
| los | Short-circuit output current [‡] | V _O = 0, | V _{ID} = 0.2 V | -40 | - 75 | - 100 | mA |
| Icc | Supply current | $V_{ID} = -0.5 V$, | No load | | 35 | 50 | mA |

[†]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

- 5. The expanded threshold parameter is tested with a 500- Ω resistor in series with each input.
- 6. The input not under test is grounded.

switching characteristics, VCC = 5 V, TA = 0°C to 70°C

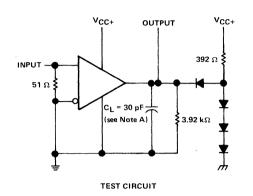
| PARAMETER | | TEST CONDITION | MIN | MAX | UNIT |
|-----------|--|--------------------------------------|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | C ₁ = 30 pF, See Figure 1 | | 85 | ns |
| tPHL | Propagation delay time, high-to-low-level output | CL = 30 pr, See rigure r | | 85 | ns |

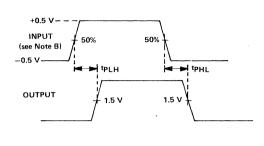


[‡]Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

PARAMETER MEASUREMENT INFORMATION





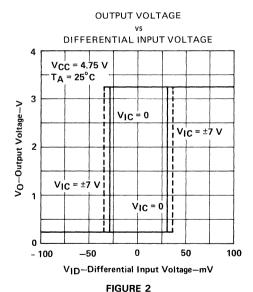
VOLTAGE WAVEFORM

NOTES: A. C. includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

FIGURE 1. TRANSITION TIMES

TYPICAL CHARACTERISTICS



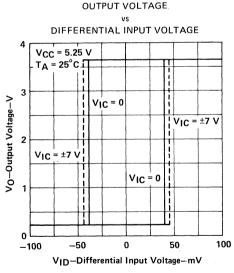
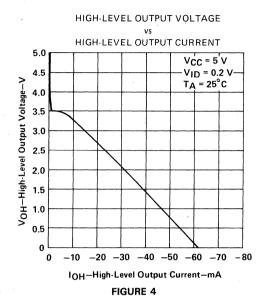
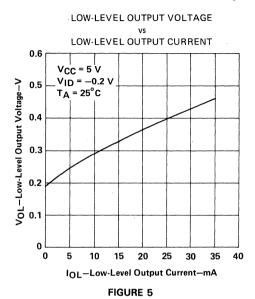


FIGURE 3

TYPICAL CHARACTERISTICS





SUPPLY CURRENT vs SUPPLY VOLTAGE 100 No load 90 Inputs open TA = 25°C 80 ICC-Supply Current-mA 70 60 50 40 30 20 10 0 0 1 7 8 VCC-Supply Voltage-V FIGURE 6

TYPICAL APPLICATION DATA

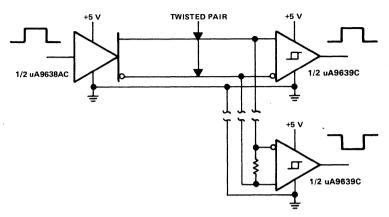


FIGURE 7. RS-422-A SYSTEM APPLICATIONS

| Gene | ral Information | ń | | | 1 |
|----------|-----------------|----------|-------------|----------|---|
| | | | | | |
| Data | Transmission | and Cont | rol Circult | S | 2 |
| | | | | | |
| Displ | ay Drivers | | | | 3 |
| | | | | | |
| Perio | heral Drivers/F | Power Ac | tuators | | 4 |
| April 18 | | | | | |
| | | | | | |
| Mech | nanical Data | | | Range of | 5 |
| | | | | | |
| | | | | | |

D2471, DECEMBER 1984-REVISED MAY 1990

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15 mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Dependable Texas Instruments Quality and Reliability
- Direct Replacement for SN55500D

description

The SN55500E is a monolithic BIDFET† integrated circuit designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

The outputs of the driver are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, SO, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuits standby power consumption. All outputs contain clamp diodes to the VCC2 and GND supply inputs.

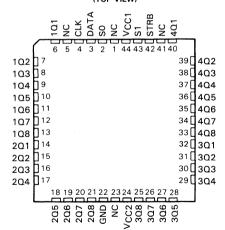
The SN55500E is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $\,^{\circ}\text{C}$.

| so□ | 1 | U40 | D _{VCC1} |
|-------|----|------|-------------------|
| DATA | 2 | 39 | ⊒ sı |
| с∟к□ | 3 | 38 | DSTRB |
| 101 | 4 | 37 | 1 401 |
| 102 | 5 | 36 | 1 402 |
| 103□ | 6 | 35 | 1 403 |
| 104□ | 7 | 34 |] 404 |
| 105 🗆 | 8 | 33 | 1 405 |
| 106 🗆 | 9 | 32 | 1 406 |
| 107 | 10 | 31 | 1 407 |
| 108 | 11 | 30 |] 4Q8 |
| 201 | 1: | 2 29 | 301 |
| 202 | 10 | 3 28 | 302 |
| 203 | 14 | 1 27 | 303 |
| 204 | 15 | 5 26 | 304 |
| 2Q5 | 16 | 25 | 305 |
| 206 🗆 | 17 | 7 24 | 306 |
| 207 🗆 | 18 | 3 23 | 307 |
| 208 | 19 | 22 | 308 |

JD PACKAGE (TOP VIEW)

FD PACKAGE (TOP VIEW)

□Vcc2



NC-No internal connection

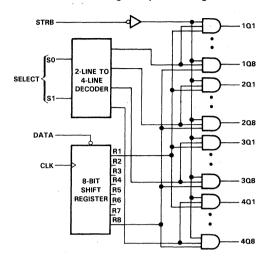
[†] BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.



logic symbol†

CMOS/PLASMA DISP STROBE (38) so (1) S1 (39) CLOCK (3) (4) 1Q1 DATA (2) 1,11 **Z**1 (<u>11)</u> 108 8,11 D (12) 201 1,12 D Z3 8,12 208 ٥ (29) 301 1,13 (22) 308 Z6 8.13 Ъ (37)401 δ 1.14 **Z**7 (30) 408 **Z**8 8 14

functional block diagram (positive logic)



 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the JD package.

FUNCTION TABLE

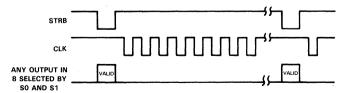
| | INPUTS | | | | | OUTPUTS | | | | | | | |
|----------|--------|-----|------------|-----|------|-----------------|-----------------|---------------------------------|---------|---------|---------|---------|--|
| FUNCTION | DATA | CLK | SEL | ECT | STRB | | SHIFT RE | GISTER | | | | | |
| | DATA | CLK | S 1 | S0 | SIND | R1 | R2 | R3 R8 | 1Q1 1Q8 | 201 208 | 3Q1 3Q8 | 401 408 | |
| LOAD | Н | 1 | Х | X | Н | L | R1 _n | R2 _n R7 _n | L L | L L | L L | L L | |
| LOAD | L | 1 | Х | Х | Н | Н | R1 _n | R2 _n R7 _n | L L | L L | L L | L L | |
| | Х | Х | Х | Х | Н | R1 _n | R2 _n | R3 _n R8 _n | L L | L L | L L | L L | |
| | X | н | L | L | L | R1 _n | R2n | R3 _n R8 _n | R1 R8 | L L | L L | L L | |
| STROBE | х | н | L | Н | L | R1 _n | R2 _n | R3 _n R8 _n | L L | R1 R8 | L L | L L | |
| | X | н | Н | L | L | R1 _n | R2 _n | R3 _n R8 _n | L L | L L | R1 R8 | L L | |
| | X | Н | Н | Н | L | R1 _n | R2 _n | R3 _n R8 _n | L L | L L | L L | R1 R8 | |

 $H = high level, L = low level, X = irrelevant, \uparrow = low-to-high transition.$

R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.

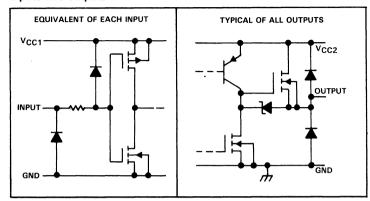
R1_n . . . R8_n = levels at outputs R1 through R8 respectively, before the most recent ↑ transition of the clock.

typical operating sequence





schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) |
|--|
| Supply voltage, V _{CC2} |
| Input voltage |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) 1825 mW |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Case temperature for 60 seconds: FD package |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JD package 300°C |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, see Dissipation Rating Table.

DISSIPATION RATING TABLE

| | PACKAGE | POWER RATING | DERATING FACTOR | ABOVE T _A | | |
|---|---------|-----------------|--------------------|-------------------------|--|--|
| ı | FD | 1825 mW | 14.6 mW/°C | 25°C | | |
| ١ | JD | 1825 mW | 22 mW/°C | 67°C | | |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|------|-----|------|------|
| Supply voltage, V _{CC1} | | 10.8 | 12 | 13.2 | V |
| Supply voltage, V _{CC2} | | 0 | | 100 | V |
| High-level input voltage | , V _{IH} , as a percentage of V _{CC1} | 75% | | | |
| Low-level input voltage, | , V _{IL} , as a percentage of V _{CC1} | | | 25% | |
| High-level output clamp | current | | | 20 | mA |
| Low-level output clamp current | | | | -20 | mA |
| Clock frequency, f _{clock} (see Figure 2) | | | | 8 | MHz |
| Duration of high or low clock pulse, t _w | | | | | ns |
| C-t ti t | Data inputs before clock↑ | , 20 | | | |
| Setup time, t _{SU} | Select inputs before strobe↓ . | 50 | | | ns |
| | Data inputs after clock1 (see Note 3) | 50 | | | |
| Hold time, th | Strobe input high after clock↑ | 50 | | | ns |
| Select inputs after strobe↑ | | 50 | | | |
| Operating free-air temper | -55 | | | °C | |
| Operating case temperature, T _C | | | | 125 | °C |

NOTE 3: For operation above 25 °C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

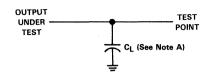
| | PARAMETER | TEST CON | TEST CONDITIONS | | | MAX | UNIT |
|--------------------------------|----------------------------|--|--------------------------------------|------|------|-------|------|
| VIK | Input clamp voltage | V _{CC1} = 12 V, | I _I = -12 mA | | - 1 | - 1.5 | V |
| | | V 12 2 V | $I_{OH} = -1 \text{ mA}$ | 94 | 97.5 | | |
| V_{OH} | High-level output voltage | $V_{CC1} = 13.2 \text{ V},$ | I _{OH} = -10 mA | 92 | 94.5 | | V |
| | | $V_{CC2} = 100 \text{ V}$ | I _{OH} = -15 mA | 90 | 93.5 | | |
| Voi Low-level output voltage I | V 12.2.V | I _{OL} = 1 mA | | 0.85 | 2 | | |
| | Low-level output voltage | V _{CC1} = 13.2 V, V _{CC2} = 100 V | I _{OL} = 10 mA | | 2 | 4 | \ \ |
| | İ | | I _{OL} = 15 mA | | 2.75 | 5 | i |
| \/-·· | Outros de alaman contra de | | I _O = 20 mA | | 1 | 2.5 | V |
| VOK | Output clamp voltage | $V_{CC2} = 0$ | $I_0 = -20 \text{ mA}$ | | -1.2 | -2.5 | V |
| ΊΗ | High-level input current | V _{CC1} = 13.2 V, | VI = VIH min | | | 1 | μΑ |
| IIL | Low-level input current | V _{CC1} = 13.2 V, | V _I = V _{IL} max | | | - 1 | μΑ |
| lcc1 | Supply current | $V_{CC1} = 13.2 \text{ V},$ | V _{CC2} = 100 V | | 0.05 | 1 | mA |
| ICC2 | Supply current | V _{CC2} = 100 V | | | 1 | 5 | mA |

 $^{^{\}dagger}AII$ typical values are at $V_{\mbox{\footnotesize CC}}~=~12$ V, $T_{\mbox{\footnotesize A}}~=~25\,^{o}C.$

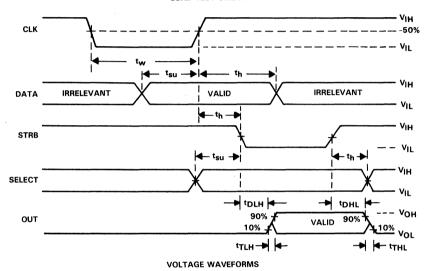
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|-----------------|-----|-----|------|
| ^t DHL | Delay time, high-to-low-level output from strobe input | | | 250 | ns |
| tDLH | Delay time, low-to-high-level output from strobe input | $C_L = 30 pF$, | | 450 | ns |
| tTHL | Transition time, high-to-low-level output | See Figure 1 | | 200 | ns |
| tTLH | Transition time, low-to-high-level output | | | 300 | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

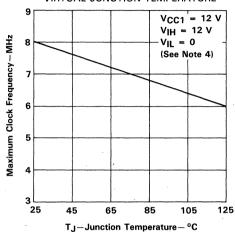


TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY

vs

VIRTUAL JUNCTION TEMPERATURE



NOTE 4: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta J A}$$

 $T_J = T_C + P_D R_{\theta J C}$

where

T_J = virtual junction temperature

T_A = free-air temperature

PD = average device power dissipation

 R_{θ} = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

| PACKAGE TYPE | $R_{\theta JA}$ | $R_{\theta JC}$ |
|-------------------|-----------------|-----------------|
| FD 44-pin ceramic | 68 °C/W | 20 °C/W |
| JD 40-pin ceramic | 45 °C/W | 12°C/W |



SN55501E AC PLASMA DISPLAY DRIVER

D2472, APRIL 1986-REVISED DECEMBER 1989

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN55501C, SN55501D

description

The SN55501E is a monolithic BIDFET[†] integrated circuit designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. This device has diode-clamped CMOS inputs.

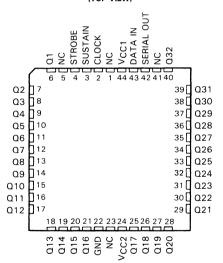
The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the SUSTAIN pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low stand-by power consumption. All outputs contain clamp diodes to the VCC2 and GND supply inputs.

The SN55501E is characterized for operation over the full military temperature range of -55 °C to 125 °C.

| - | | | |
|-----------------|------|---|------------|
| CLOCK 🗖 1 | U40 | D | VCC1 |
| SUSTAIN 2 | 39 | Ы | DATA IN |
| STROBE 3 | 38 | þ | SERIAL OUT |
| Ω1 🗖 4 | 37 | | Q32 |
| Ω2 □ 5 | 36 | þ | Q31 |
| 03 🗖 6 | 35 | Þ | Q30 |
| Q4 🗖 7 | 34 | Þ | Q29 |
| Q5 □ 8 | 33 | | Q28 |
| Ω6 □ 9 | 32 | Þ | Q27 |
| Q7 []1 | 0 31 | | Q26 |
| 08₫₁ | 1 30 | Ы | Q25 |
| Ω9 🗖 1 | 2 29 | Б | Q24 |
| Q10 _ 1 | 3 28 | Ь | Q23 |
| Q11 []1 | 4 27 | Ь | Q22 |
| Q12 []1 | 5 26 | Ь | Q21 |
| Q13 []1 | 6 25 | Ы | Q20 |
| 014 🗖 1 | 7 24 | Ь | Q19 |
| Q15 []1 | 8 23 | b | Q18 |
| Q16 []1 | 9 22 | Ь | Q17 |

J PACKAGE (TOP VIEW)

FD OR FJ PACKAGE (TOP VIEW)



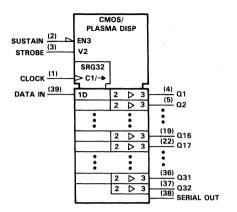
NC-No internal connection

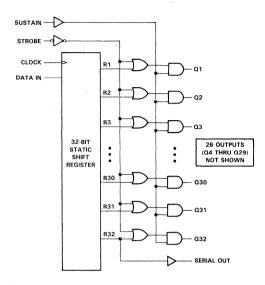
[†]BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip -- patented process.



logic symbol†

functional block diagram (positive logic)





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J package.

FUNCTION TABLE

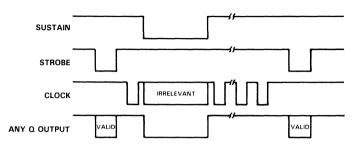
| | INPUTS | | | | OUTPUTS | | | | | | |
|----------|--------|-------|--------|---------|-----------------|-----------------|----------------------------------|------------------|----|----|--------|
| FUNCTION | DATA | СГОСК | STROBE | SUSTAIN | S | SHIFT REGISTER | | SERIAL | 01 | Q2 | 03032 |
| | DATA | CLUCK | SINUBE | SUSTAIN | R1 | R2 | R3R32 | DATA | u. | uz | ususz |
| LOAD | Н | 1 | Н | Н | Н | R1 _n | R2 _n R31 _n | R32 _n | Н | Н | НН |
| LUAD | L | 1 | н | н | L | R1 _n | R2 _n R31 _n | R32n | Н | Н | нн |
| STROBE | Х | Х | Н | Н | R1 _n | R2 _n | R3 _n R32 _n | R32 _n | Н | Н | НН |
| SINOBE | Х | н | L | ` н | R1 _n | R2n | R3 _n R32 _n | R32 _n | R1 | R2 | R3 R32 |
| SUSTAIN | Х | Х | X | L | R1 _n | R2 _n | R3 _n R32 _n | R32 _n | L | L | LL |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

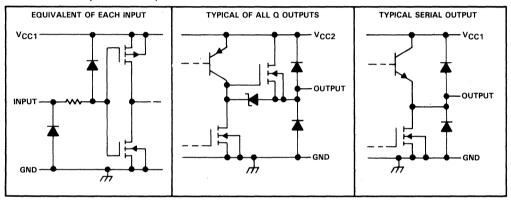
R1...R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.

R1n...R32n = levels at shift-register outputs R1 through R32 respectively, before the most recent † transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC1} (see Note 1) |
|---|
| Supply voltage, VCC2 |
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA55 °C to 125 °C |
| Storage temperature range |
| Case temperature for 60 seconds: FD or FJ package |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300°C |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR | DERATE ABOVE T _A | TA = 125°C POWER RATING | |
|----------|---------------------------------------|--------------------|--------------------------------|----------------------------|--|
| FD or FJ | 1825 mW | 14.6 mW/°C | 25 °C | 365 mW | |
| J | 1825 mW | 22.0 mW/°C | 67°C | 550 mW | |



SN55501E AC PLASMA DISPLAY DRIVER

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--------------------------------------|---|-----------------------|-----|-----------------------|------|
| Supply voltage, V | CC1 | 10.8 | 12 | 13.2 | V |
| Supply voltage, V | CC2 | 0 | | 100 | V |
| High-level input v | oltage, V _{IH} | 0.75 V _{CC1} | | | |
| Low-level input vo | oltage, V _{IL} | | | 0.25 V _{CC1} | |
| Peak high-level Q | output current, IOH | | | - 20 | mA |
| Peak low-level Q output current, IOL | | | | 20 | mA |
| High-level Q outp | ut clamp current, IOKH | | | 20 | mA |
| Low-level Q outpu | w-level Q output clamp current, I _{OKL} -20 | | | | mA |
| Clock frequency, | f _{clock} , at or below, 25 °C junction temperature (see Note 2) | 0 | 0 8 | | MHz |
| Duration of high of | or low clock pulse, t _w | 62 | | | ns |
| Setup time, t _{su} | Data inputs before CLOCK↑ | 20 | | | ns |
| | Data hold time after CLOCK↑ | 50 | | | |
| Hold time, th | STROBE high after CLOCK↑ | 150 | | | ns |
| | STROBE high after SUSTAIN1 | 250 | | | 1 |
| Operating free-air | temperature, TA | - 55 | | 125 | °C |
| Operating case te | mperature, T _C | | | 125 | ا 'ل |

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above $T_{\rm J}=25\,{\rm ^{o}C}$.

electrical characteristics over recommended operating temperature range

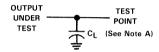
| PARAMETER | | | PARAMETER TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT |
|-----------|------------------------|----------------------------|--|--|------|------------------|------|------|
| Vik | Input clamp vol | tage | $V_{CC1} = 12 V$, | lj = 12 mA | | -1 | -1.5 | V |
| | | V _{CC1} = 13.2 V, | IOH = -1 mA | 94 | 97.5 | | | |
| VoH | High-level | Q outputs | $V_{CC1} = 13.2 \text{ V},$ $V_{CC2} = 100 \text{ V}.$ | IOH = -10 mA | 92 | 94.5 | |] v |
| νОН | output voltage | | VCC2 = 100 V | I _{OH} = -15 mA | 90 | 93.5 | |] ' |
| | | SERIAL OUT | $V_{CC1} = 10.8 V,$ | $I_{OH} = -100 \mu A$ | 9 | 10 | | |
| | | | $V_{CC1} = 13.2 \text{ V},$ | IOL = 1 mA | | 0.85 | 2 | |
| 1/01 | Low-level | Q outputs | $V_{CC2} = 100 \text{ V}$ | I _{OL} = 10 mA | | 2 | 4 |] v |
| VOL | output voitage | | VCC2 = 100 V | I _{OL} = 15 mA | | 2.75 | 5 |] ' |
| | | SERIAL OUT | $V_{CC1} = 10.8 V,$ | $I_{OL} = 100 \mu A$ | | 0.1 | 1 | |
| Var | Output clamp Q outputs | V _{CC2} = 0 | I _{OK} = 20 mA | | 1 | 2.5 | V | |
| Voк | voltage | a outputs | VCC2 = 0 | $I_{OK} = -20 \text{ mA}$ | | -1.2 | -2.5 | |
| 1 | High-level | | $V_{CC1} = 13.2 V,$ | $V_{IH} = V_{IH}min,$ | | | 1 | μΑ |
| ΉΗ | input current | | $V_{CC2} = 100 \text{ V}$ | | | | 1 | μΛ |
| 1 | Low-level | | $V_{CC1} = 13.2 V$ | V _{IL} = V _{IL} max, | | | - 1 | μΑ |
| ΙΙL | input current | | $V_{CC2} = 100 \text{ V}$ | | | | ' | μΑ |
| ICC1 | Supply current | from V _{CC1} | $V_{CC1} = 13.2 V,$ | V _{CC2} = 100 V [‡] | | 0.05 | 1 | mA |
| loon | Supply current | from Voca | $V_{CC1} = 13.2 V,$ | Outputs low | | 0.1 | 1 | mA |
| ICC2 | Supply current | nom vCC2 | $V_{CC2} = 100 V$ | Outputs high | | 1 | 5 | |

 $^{^{\}dagger}\text{Typical}$ values are at VCC1 = 12 V, TA = 25 °C. $^{\ddagger}\text{Measure}$ with inputs at VCC1 and again with inputs at GND.

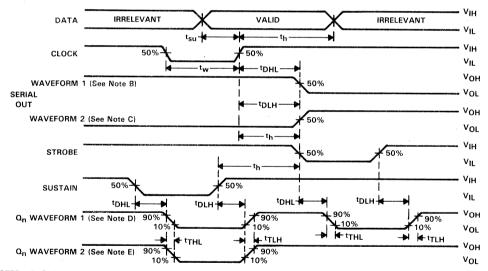
switching characteristics, VCC1 = 12 V, VCC2 = 100 V, TA = 25°C

| | PARA | METER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|----------------------|------------------------|-----|-----|-----|------|
| | Delay time, | STROBE to Q outputs | C _L = 30 pF | | | 250 | |
| tDHL | high-to-low- | SUSTAIN to Q outputs | $C_L = 30 pF$ | | | 250 | ns |
| | level outputs | CLOCK to SERIAL OUT | C _L = 20 pF | | | 147 | |
| | Delay time, | STROBE to Q outputs | C _L = 30 pF | | | 450 | |
| †DLH | low-to-high- | SUSTAIN to Q outputs | C _L = 30 pF | | | 450 | ns |
| | level outputs | CLOCK to SERIAL OUT | C _L = 20 pF | | | 147 | |
| ^t THL | t _{THL} Transition time, high-to-low-level Q output | | C _L = 30 pF | | | 200 | ns |
| tTLH | t _{TLH} Transition time, low-to-high-level Q output | | C _L = 30 pF | | | 300 | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



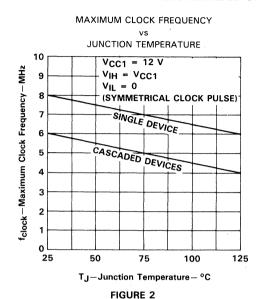
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Serial out waveform for internal conditions such that a low is registered in R32.
 - C. Serial out waveform for internal conditions such that a high is registered in R32.
 - D. Q_n output with a low stored in associated register R_n.
 - E. Q_n output with a high stored in associated register R_n.

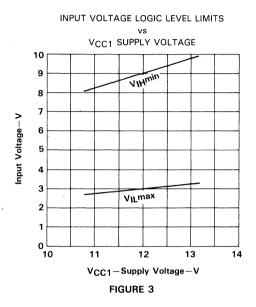
VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS





THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature

 $T_A = free-air temperature$

PD = average device power dissipation

 R_{θ} = thermal resistance (junction-to-air, $R_{\theta}JA$, or junction-to-case, $R_{\theta}JC$)

| PACKAGE | R _{OJA} | R _O JC |
|----------|------------------|-------------------|
| FD or FJ | 68 °C/W | 20 °C/W |
| J | 45 °C/W | 12°C/W |

D2743, APRIL 1986

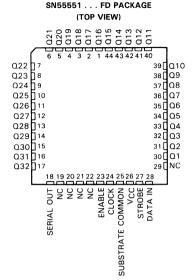
- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

description

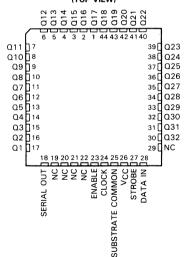
The SN55551 and SN55552 are monolithic BIDFET[†] integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN55552 output sequence has been reversed from the SN55551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the highto-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

The SN55551 and SN55552 are characterized for operation over the full military temperature range of -55 °C to 125 °C.



SN55552 . . . FD PACKAGE (TOP VIEW)



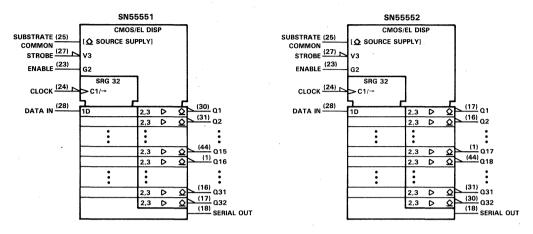
NC-No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.



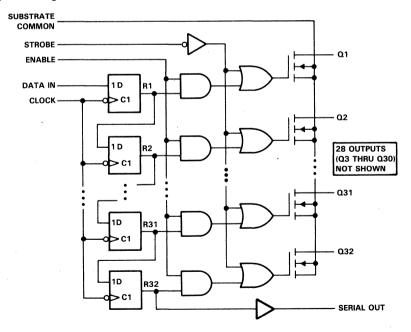
SN55551, SN55552 ELECTROLUMINESCENT ROW DRIVER

logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol **△** here indicates an n-channel open-drain output.

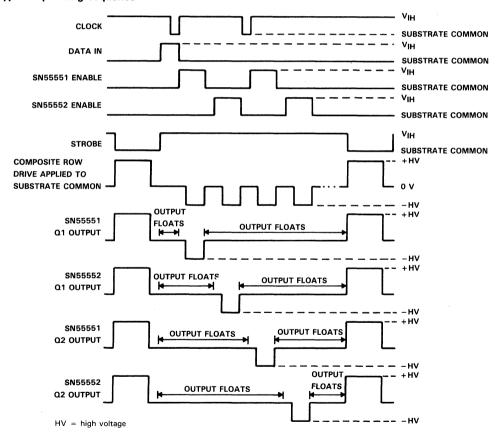
logic diagram (positive logic)



| | FUNCTION TABLE | | | | | | | | | | |
|----------|----------------|--------|--------|-----------------------------|---------|---------------------------------|--|--|--|--|--|
| FUNCTION | CONTROL INPUTS | | | SHIFT REGISTERS | OUTPUTS | | | | | | |
| | СГОСК | ENABLE | STROBE | R1 THRU R32 | SERIAL | Q1 THRU Q32 | | | | | |
| LOAD | ţ | Х | Х | Load and Shift [†] | R32 | Determined by Enable and Strobe | | | | | |
| LOAD | No.↓ | X | Х | No Change | R32 | Determined by Enable and Strobe | | | | | |
| ENABLE | Х | L | Н | As determined above | R32 | All Q outputs off | | | | | |
| LIVABLE | Х | Н | Н | As determined above | R32 | Determined by R1 through R32 | | | | | |
| STROBE | Х | Х | L | As determined above | R32 | All Q outputs on | | | | | |

H = high level, L = low level, X = irrelevant, L = high-to-low transition.

typical operating sequence



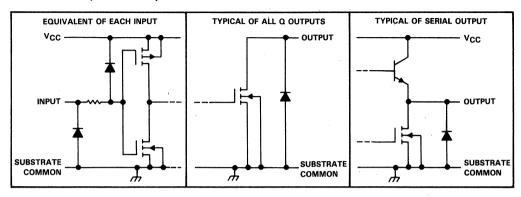
NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.



[†]Register R32 takes on the state of R31, R31 takes on the state of R30,...R2 takes on the state of R1, and R1 takes on the state of the data input.

SN55551, SN55552 **ELECTROLUMINESCENT ROW DRIVER**

schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Q off-state output voltage, VO(off) |
| Input voltage |
| Substrate common terminal current (see Note 2) |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 3) 1825 mW |
| Minimum operating free-air temperature |
| Operating case temperature |
| Storage temperature range |
| Case temperature for 60 seconds |

NOTES: 1. Voltage values are with respect to substrate common terminal.

- 2. Duty cycle is limited by package dissipation.
- 3. For operation above 25 °C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

| | | | | MIN | NOM MAX | UNIT |
|-----------------|---|----------------------------|--|---------------------|----------------------|------|
| Vcc | Supply voltage | | | 10.8 | 12 15 | V |
| VO(off) | Off-state Q output voltage | | | 0 | 200 | V |
| VIH | High-level input voltage | | | 0.75V _{CC} | V _{CC} +0.3 | V |
| VIL | Low-level input voltage | | | -0.3 | 0.25V _{CC} | ٧ |
| lo, | On state O output current | V _{DD} = 80 V, | $V_{CC} = 10.8 \text{ V},$ $T_{C} = 25 ^{\circ}\text{C}$ | | 50 | mA |
| (O(on) | IO(on) On-state Q output current | | $V_{CC} = 15 V$, $T_{C} = 25 ^{\circ}C$ | | 80 | |
| fclock | Clock frequency, TA = 25° | C | | | 6.25 | MHz |
| t _w | Clock pulse duration, high or | low, T _A = 25°C | | 80 | | ns |
| t _{su} | Setup time, data valid before clock\$\dagger\$, T_A = 25 °C | | | 20 | | ns |
| th | Hold time, data valid after clock↓, T _A = 25 °C | | | 110 | | ns |
| TA | Operating free-air temperature | | | - 55 | | °C |
| TC | Operating case temperature | | | | 125 | °C |

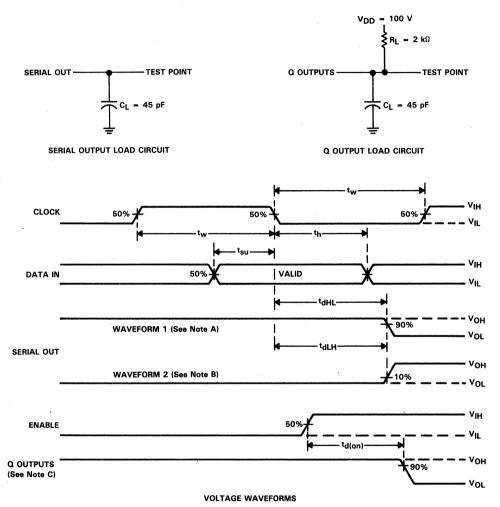
electrical characteristics over recommended operating temperature range, $V_{CC}=12~V$, substrate common at 0 V

| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------|----------------------------|----------------|-------------------------|-----|-----|------|
| Voн | High-level output voltage | Serial outputs | $I_{O} = -100 \mu A$ | 10 | · | V |
| 1/ | | Q outputs | IO = 50 mA | | 50 | V |
| v_{OL} | Low-level output voltage | Serial output | I _O = 100 μA | | 1.5 | 1 ° |
| ΊΗ | High-level input current | | V _I = 12 V | | 5 | μΑ |
| ll. | Low-level input current | | V ₁ = 0 | | - 5 | μΑ |
| IO(off) | Off-state Q output current | | V _O = 200 V | | 50 | μΑ |
| Icc | Supply current | | | | 500 | μΑ |

switching characteristics, VCC = 12 V, TC = $25\,^{\circ}$ C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---------------------------------|--|-----|------|------|
| tdLH | Delay time, clock↓ to serial↓ | $C_L = 45 pF to common,$ | | 200 | ns |
| tdHL | Delay time, clock↓ to serial↑ | See Figure 1 | | 200 | ns |
| ^t dHL | Delay time, enable to ℚ output↓ | $V_{DD}=100 \text{ V}, R_{L}=2 \text{ k}\Omega,$ $C_{L}=45 \text{ pF to common},$ See Figure 1 | | 500° | ns |

PARAMETER MEASUREMENT INFORMATION



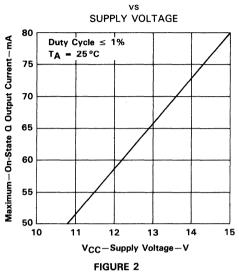
- NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
 - B. Waveform 2 is for internal conditions such that a high is clocked into R32.
 - C. To measure $t_{d(on)}$, a high is stored in the associated register.

FIGURE 1. SWITCHING CHARACTERISTICS

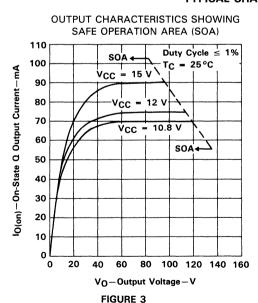


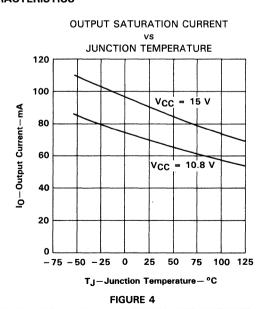
RECOMMENDED OPERATING CONDITIONS

MAXIMUM ON-STATE Q OUTPUT CURRENT



TYPICAL CHARACTERISTICS





D2744, APRII 1986

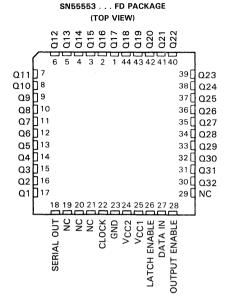
- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

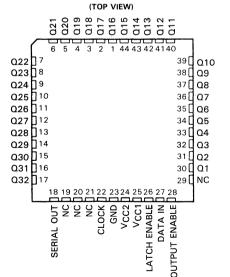
description

The SN55553 and SN55554 are monolithic BIDFET[†] integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence has been reversed from the SN55553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-tohigh transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of -55°C to 125°C.





SN55554 . . . FD PACKAGE

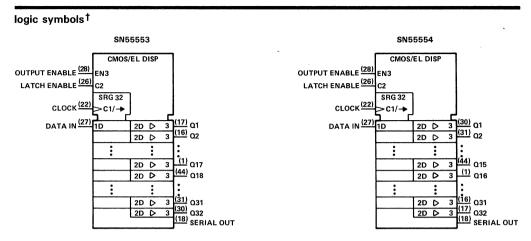
NC-No internal connection

SERIAL

 † BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip - patented process.

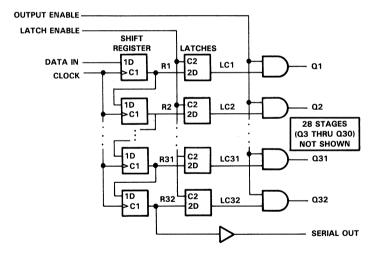


SN55553, SN55554 **ELECTROLUMINESCENT COLUMN DRIVERS**



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

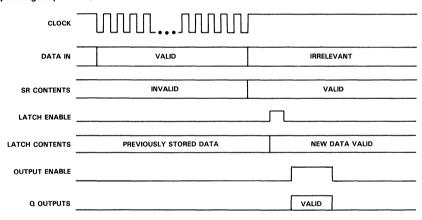


FUNCTION TABLE

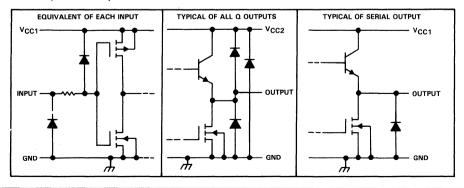
| | CONTROL INPUTS | | | SHIFT REGISTER | LATCHES | OUTPUTS | | | |
|----------|----------------|-----------------|------------------|---------------------------------------|---------------------------|---------|-----------------------------|--|--|
| FUNCTION | CLOCK | LATCH ENABLE | OUTPUT ENABLE | TPUT R1 THRU R32 LC1 THRU LC32 SERIAL | | | | | |
| 1040 | 1 | х | х | Load and shift [†] | Determined by | R32 | Determined by | | |
| LOAD | Not | х | Х | No change | Latch Enable [‡] | R32 | Output Enable | | |
| LATCH | Х | L | Х | As determined above | Stored data | R32 | Determined by | | |
| LATCH | Х | н | × | As determined above | New data | R32 | Output Enable | | |
| OUTPUT | Х | Х | L | As determined above | Determined by | R32 | All L | | |
| ENABLE | х | х | н | As determined above | Latch Enable [‡] | R32 | LC1 thru LC32, respectively | | |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

typical operating sequence



schematic of inputs and outputs



[†]R32 and the serial output take on the state of R31, R31 takes on the state of R30,...R2 takes on the state of R1, and R1 takes on the state of the data input.

^{*}New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

SN55553, SN55554 ELECTROLUMINESCENT COLUMN DRIVERS

absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) |
|--|
| Supply voltage, VCC2 |
| Input voltage VCC1 + 0.3 V |
| Ground current |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) 1825 mW |
| Minimum operating free-air temperature |
| Operating case temperature |
| Storage temperature range – 65 °C to 150 °C |
| Case temperature for 60 seconds 260 °C |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------|---|---------------------|-----|----------------------|------|
| V _{CC1} | Supply voltage | 10.8 | 12 | 13.2 | V |
| V _{CC2} | Supply voltage | 0 | | 60 | V |
| ViH | High-level input voltage | 0.75V _{CC} | | V _{CC} +0.3 | V |
| VIL | Low-level input voltage | -0.3 | | 0.25V _{CC} | |
| ЮН | High-level output current | - 15 | | | mA |
| lOL | Low-level output current | 15 | | | mA |
| Ток | Peak output clamp diode current | | | ± 20 | mA |
| fclock | Clock frequency, T _A = 25 °C | | | 6.25 | MHz |
| tw(CLK) | Clock pulse duration, high or low, $T_A = 25^{\circ}\text{C}$ | 80 | | | ns |
| tw(LE) | Latch enable pulse duration, T _A = 25 °C | 80 | | | |
| t _{su} | Setup time, data valid before clock1, T _A = 25 °C | 20 | | | ns |
| th | Hold time, data valid after clock ↑, T _A = 25 °C | 110 | | | ns |
| TA | Operating free-air temperature | - 55 | | | |
| TC | Operating case temperature | | | 125 | |

electrical characteristics over recommended operating temperature range, $V_{CC1} = 12 \text{ V}$, $V_{CC2} = 60 \text{ V}$

| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------|----------------------------------|---------------|-------------------------|-----|-----|------|
| | 11: | Q outputs | I _O = -15 mA | 55 | | V |
| Vон | High-level output voltage | Serial output | $I_0 = -100 \mu A$ | 10 | | v |
| VOL | | Q outputs | I _O = 15 mA | | 10 | V |
| | Low-level output voltage | Serial output | I _O = 100 μA | | 1.5 | 1 ° |
| ΙН | High-level input current (se | ee Note 3) | V _I = 12 V | | 5 | μΑ |
| ΙL | Low-level input current (se | e Note 3) | V _I = 0 | | -5 | μΑ |
| ICC1 | Supply current, V _{CC1} | | | | 7 | mA |
| lCC2 | | | Outputs high | | 20 | |
| | Supply current, V _{CC2} | Outputs low | | | | mA |

NOTE 3: I_{IH} and I_{IL} parameter performances are independent of V_{CC2} and need not be 60 V for this test.

switching characteristics, VCC1 = 12 V, VCC2 = 60 V, TC = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|-------------------------------|--------------------------|-----|------|------|
| tdLH | Delay time, clock↑ to serial↑ | $C_L = 45 pF to ground,$ | | 200 | ns |
| ^t dHL | Delay time, clock↑ to serial↓ | See Figures 1 and 2 | | 200 | ns |
| t _{dLH} | Delay time, LE to Q output↑ | $C_L = 45 pF to ground,$ | | 1000 | ns |
| ^t dHL | Delay time, LE to Q output↓ | See Figures 1 and 3 | | 500 | ns |

PARAMETER MEASUREMENT INFORMATION

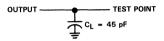


FIGURE 1. OUTPUT LOAD CIRCUIT

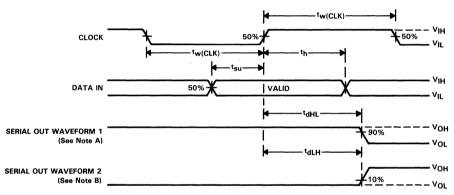


FIGURE 2. VOLTAGE WAVEFORMS FOR SERIAL OUTPUT

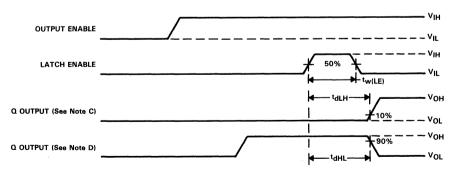


FIGURE 3. VOLTAGE WAVEFORMS FOR Q OUTPUTS

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.

- B. Waveform 2 is for internal conditions such that a high is clocked into R32.
- C. To measure $t_{\mbox{\scriptsize dLH}}$, initially a low is stored in the latch and a high is stored in the shift register.
- D. To measure t_{dHL}, initially a high is stored in the latch and a low is stored in the shift register.



SN55563A, SN55564A ELECTROLUMINESCENT ROW DRIVERS

D3313 OCTOBER 1989

- Each Device Drives 34 Electrodes
- Selectable Open-Source or Open-Drain Output
- Outputs Rated at 225 V
- Output Current Capability:
 -90 mA to 150 mA
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

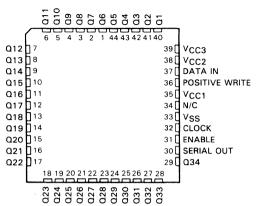
description

The SN55563A and SN55564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If the Positive Write input is high, the Q outputs act like opensource outputs and output data is not inverted with respect to input data. If the Positive Write input is low, the Q outputs act like opendrain outputs and output data is inverted with respect to input data. The SN55564A output sequence has been reversed from the SN55563A for ease in printed circuit board layout.

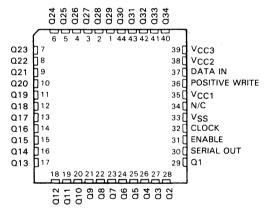
Typically, composite V_{CC2}, V_{CC3}, and V_{SS} signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when Positive Write is high or to V_{SS} when Positive Write is low. V_{CC3} may be tied to V_{CC2} or held 5 to 15 V above V_{CC2} for better V_{OH} characteristics. The Serial Output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Positive Write inputs.

The SN55563A and SN55564A are characterized for operation over the full military operating temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$.

SN55563A . . . FJ PACKAGE (TOP VIEW)



SN55564A . . . FJ PACKAGE (TOP VIEW)



NC-No internal connection

†BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process



SN55563A, SN55564A **ELECTROLUMINESCENT ROW DRIVERS**

LOAD FUNCTION TABLE

| | co | NTROL INP | UTS | SHIFT REGISTER | OUTPUTS | | |
|----------|-------|-----------|-------------------|-----------------------------|---------|---|--|
| FUNCTION | CLOCK | ENABLE | POSITIVE WRITE | R1 THRU R34 | SERIAL | Q1 THRU Q34 | |
| LOAD | 1 | Х | × | Load and Shift [†] | R34 | Determined by Enable and Positive Write | |
| LOAD | No↓ | X | × | No Change | R34 | Determined by Enable and Positive Write | |

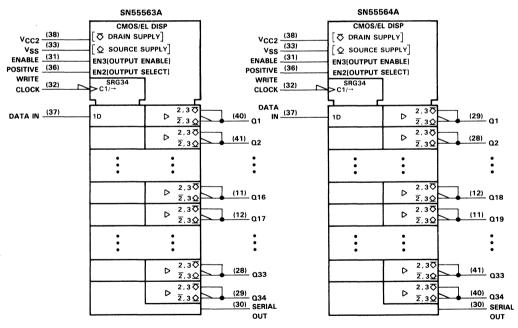
[†]Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

| | co | NTROL INP | UTS | SHIFT REGISTER CONTENTS Rn FOR | OUTPUTS | | |
|----------|-------|-----------|-------------------|-----------------------------------|---------|----------------|--|
| FUNCTION | СГОСК | ENABLE | POSITIVE WRITE | R1 THRU R34 (Determined Above) | SERIAL | Q1 THRU Q34 | |
| | × | L | Х | X | R34 | High-Impedance | |
| OUTPUT | × | н | н | н | R34 | н | |
| CONTROL | х | н | L | н | R34 | L | |
| | Х | х | X | L | R34 | High-Impedance | |

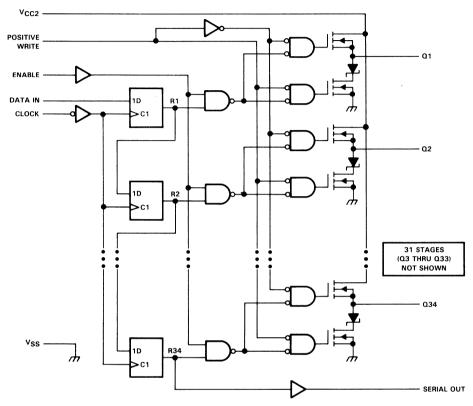
 $H = high, L = low, X = irrelevant, \downarrow = high-to-low transition$

logic symbols‡

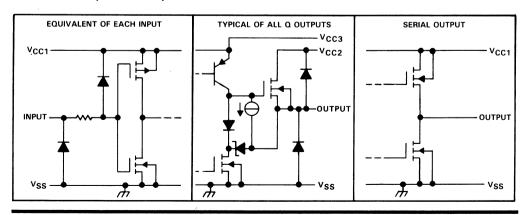


[‡]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

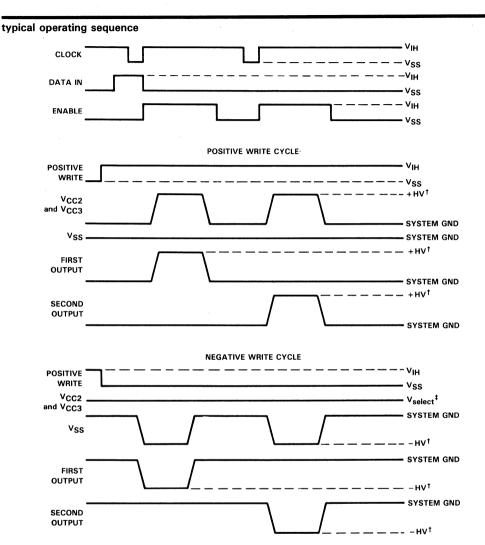
logic diagram (positive logic)



schematics of inputs and outputs



SN55563A, SN55564A **ELECTROLUMINESCENT ROW DRIVERS**



[†]HV = high voltage

[‡]V_{select} is a voltage level between V_{CC2} of the column driver and V_{SS}.

absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) |
|---|
| Supply voltage, VCC2 |
| Supply voltage, VCC3 |
| Supply voltage, VSS |
| Input voltage |
| Continuous total power dissipation at (or below) 25 °C free-air temperature |
| (see Note 2) |
| Operating free-air temperature range |
| Storage temperature range |
| Case temperature for 10 seconds 260°C |

NOTES: 1. Voltage values are with respect to VSS.

2. For operation above 25 °C free-air temperature, derate 365 mW at 125 °C at the rate of 14.6 mW/°C.

recommended operating conditions (see Figure 1 and Figure 2)

| | MIN | NOM | MAX | UNIT |
|--|-----------------------|-----|------------------------|------|
| Supply voltage, V _{CC1} | 10.8 | 12 | 13.2 | V |
| Supply voltage, V _{CC2} | V _{CC3} – 15 | | V _{CC3} | V |
| Supply voltage, V _{CC3} | 0 | | 225 | V |
| Supply voltage, V _{SS} | 0 | | - 225 | V |
| High-level input voltage, VIH | 0.75V _{CC1} | | V _{CC1} + 0.3 | V |
| Low-level input voltage, V _{IL} † | -0.3 | | 0.25V _{CC1} | V |
| High-level output current, IOH | | | - 90 | mA |
| Low-level output current, IOL | | | 150 | mA |
| Output clamp current, IOK | | | ±150 | mA |
| Clock frequency, f _{clock} | | | 1 | MHz |
| Pulse duration, Clock high or low, twCLK | 125 | | | ns |
| Setup time, data high or low before clock↓, t _{su1} | 100 | | | ns |
| Setup time, Clock low before V _{CC2} ↑ or V _{SS} ↓, t _{su2} | 300 [‡] | | | ns |
| Setup time, Enable high before V _{CC2} ↑ or V _{SS} ↓, t _{su3} | 300 [‡] | | | ns |
| Setup time, Positive Write high or low before VCC21 or VSS1, tsu4 | 300 [‡] | | | ns |
| Hold time, data high or low after clock↓, th1 | 100 | | | ns |
| Hold time, Clock high after V _{CC2} ↓ or V _{SS} ↑, th2 | 300 [‡] | | | ns |
| Hold time, Enable high after V _{CC2} ↓ or V _{SS} ↑, t _{h3} | 0 [‡] | | | ns |
| Hold time, Positive Write after V _{CC2} ↓ or V _{SS} ↑, t _{h4} | 0‡ | | | ns |
| Hold time, Enable low between successive VCC21, th5 | 12 [‡] | | | μS |
| Hold time, Enable low between successive V _{SS} ↓, t _{h6} | 300 [‡] | | | ns |
| Operating free-air temperature, TA | - 55 | | 125 | °C |

[†]The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.



[‡]These minimum recommendations are not tested during manufacturing. Performance is dependent on application voltage and temperature and must be validated by the user.

electrical characteristics over recommended operating ranges of VCC1 and free-air temperature range, $VCC2=225\ V,\ VCC3=225\ V,\ VSS=0$ (unless otherwise noted)

| | PARAMETE | R | TEST CONDITIONS | MIN | MAX | UNIT | |
|---------|--------------------------------------|------------------------|--|----------------------|-------|------|--|
| lov re | Off-state Q output current | | V _O = 225 V | | 150 | μΑ | |
| lO(off) | On-state & outp | ut current | V _O = 0 | | - 150 | μΑ | |
| | High-level | Q outputs | $I_0 = -70 \text{ mA}, V_{CC1} = 12 \text{ V}$ | V _{CC2} -40 | | | |
| Vон | output voltage | Q outputs | $I_0 = -90 \text{ mA}, V_{CC1} = 12 \text{ V}$ | V _{CC2} -45 | | V | |
| | output voitage | Serial Out | $I_{O} = -100 \mu\text{A}, V_{CC1} = 12 \text{V}$ | 10.5 | | | |
| Voi | Low-level | Q outputs | I _O = 150 mA | | 30 | V | |
| VOL | output voltage | Serial Out | $I_O = 100 \mu A$ | | 1 | _ `_ | |
| ΊΗ | High-level input | current | V _{IH} = V _{CC1} | | 100 | μΑ | |
| IIL | Low-level input of | current | V _{IL} = 0 | | 100 | μΑ | |
| | Supply current from V _{CC1} | | One Q output high | | 4 | mA | |
| ICC1 | Supply current in | om vCC1 | All Q outputs low or high impedance | | 2 | mA | |
| | | | One Q output high, V _{CC1} = 12 V | | 10 | mA | |
| Іссз | Supply current for | rom V _{CC3} ‡ | All Q outputs low or high impedance, | | 200 | | |
| | | | V _{CC1} = 12 V | | 200 | μΑ | |

switching characteristics over recommended operating range of VCC1, TA = 25°C

| | PARAMETER | TEST CONDITIONS | MIN | MIN MAX | |
|------------------|-------------------------------------|-------------------------|-----|---------|----|
| | Propagation delay time, low-to-high | | | 400 | |
| ^t PLH | level serial output from clock | $C_L = 50 pF to V_{SS}$ | | 400 | ns |
| | Propagation delay time, high-to-low | See Figures 3 and 4 | | 400 | |
| ^t PHL | level serial output from clock | | | 400 | ns |

[‡]I_{CC3} is measured with V_{CC2} and V_{CC3} shorted together.

PARAMETER MEASUREMENT INFORMATION

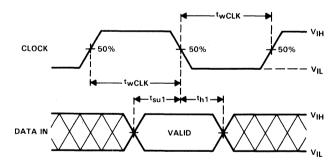
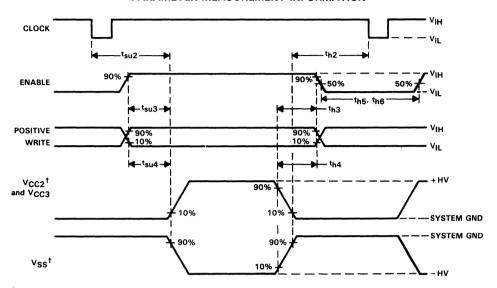


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



 $^{^{\}dagger}\text{Timing}$ waveforms are with respect to VCC2 or VSS, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

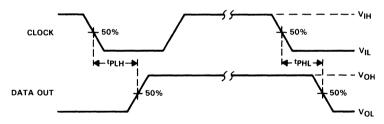
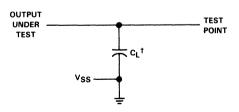


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT



[†]C_L includes probe and jig capacitance.

FIGURE 4. LOAD CIRCUIT



SN65500E, SN75500E AC PLASMA DISPLAY DRIVERS

D2471, DECEMBER 1985-REVISED JULY 1989



- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN75500A

description

The SN65500E and SN75500E are monolithic BIDFET[†] integrated circuits designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

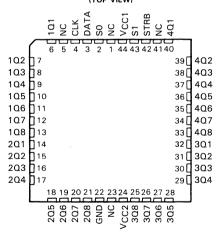
The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, SO, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the VCC2 and GND supply inputs.

The SN65500E is characterized for operation from $-40\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$. The SN75500E is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

| () | I UP V | IE VV | , |
|-------|--------|-------|--------------|
| so 🗖 | 1 U | 40 | J VCC1 |
| DATA | 2 | 39 |] s1 |
| CLK 🗆 | 3 | 38 | STRB |
| 101 | 4 | 37 |] 4Q1 |
| 102 | 5 | 36 |] 4Q2 |
| 103 🗖 | 6 | 35 |] 4Q3 |
| 104 | 7 | 34 |] 4Q4 |
| 105 | 8 | 33 |] 4Q5 |
| 106 | 9 | 32 |] 4Q6 |
| 107 | 10 | 31 |] 4Q7 |
| 108 | 11 | 30 | 3 4Q8 |
| 201 | 12 | 29 | 3 3Q1 |
| 202 | 13 | 28 | 302 |
| 203 | 14 | 27 | 303 |
| 204 | 15 | 26 | 304 |
| 205 | 16 | 25 | 3Q5 |
| 206 | 17 | 24 | 306 |
| 207 | 18 | 23 | 307 |
| 208 | 19 | 22 | 308 |
| GND [| 20 | 21 | J Vcc2 |

N PACKAGE

FN PACKAGE (TOP VIEW)

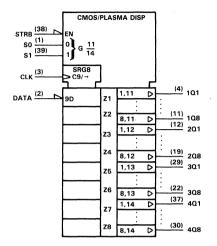


NC-No internal connection

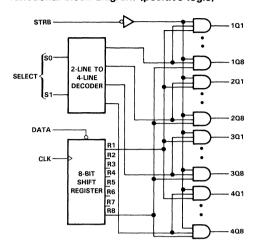
[†]BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.



logic symbol†



functional block diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the N package.

FUNCTION TABLE

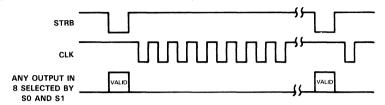
| | INPUTS | | | | | OUTPUTS | | | | | | | | |
|----------|----------|-----|-----|-----|------|-----------------|-----------------|---------------------------------|----------|---------|---------|---------|--|--|
| FUNCTION | DATA | CLK | CLK | CLK | SEL | ECT | STRB | : | SHIFT RI | EGISTER | | | | |
| | DATA CLI | | S1 | S0 | SIND | R1 | R2 | R3 R8 | 101 108 | 201 208 | 3Q1 3Q8 | 4Q1 4Q8 | | |
| LOAD | Н | 1 | Х | X | Н | L | R1 _n | R2 _n R7 _n | L L | L L | L L | L L | | |
| LOAD | L | 1 | Х | Χ | н | н | R1 _n | R2 _n R7 _n | L L | LL | L L | L L | | |
| | Х | Х | Х | Х | Н | R1 _n | R2 _n | R3 _n R8 _n | L L | L L | L L | L L | | |
| | × | Н | L | L | L | R1 _n | R2 _n | R3 _n R8 _n | R1 R8 | L L | L L | L L | | |
| STROBE | × | Н | L | Н | L | R1 _n | R2n | R3 _n R8 _n | L L | R1 R8 | L L | L L | | |
| | × | Н | н | L | L | R1 _n | R2 _n | R3 _n R8 _n | L L | L L | R1 R8 | L L | | |
| | X | Н | н | Н | L | R1 _n | R2 _n | R3 _n R8 _n | L L | LL | L L | R1 R8 | | |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high transition$.

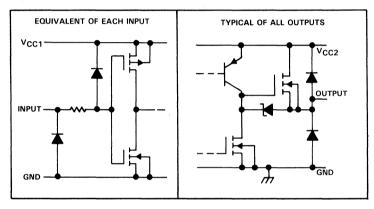
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.

R1_n . . . R8_n = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) | 15 V |
|--|-----------------------------|
| Supply voltage, VCC2 | |
| Input voltage | V _{CC1} +0.3 V |
| Continuous total power dissipation | ee Dissipation Rating Table |
| Operating free-air temperature range: SN65500E | 40°C to 85°C |
| SN75500E | 0°C to 70°C |
| Storage temperature | 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N packag | je 260°C |
| Case temperature for 10 seconds: FN package | 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| FN | 1775 mW | 14.2 mW/°C | 1136 mW | 923 mW |
| N | 1275 mW | 10.2 mW/°C | 816 mW | 663 mW |



SN65500E, SN75500E AC PLASMA DISPLAY DRIVERS

recommended operating conditions

| | | S | N65500 | E | SI | V75500I | Ė | LINUT |
|-----------------------------------|---|------|--------|------|------|---------|--|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 1 | 10.8 | 12 | 13.2 | 10.8 | 12 | 13.2 | V |
| Supply voltage, VCC | 2 | 0 | | 100 | 0 | | 100 | V |
| High-level input volta | ge, V _{IH} , as a percentage of V _{CC1} | 75% | | | 75% | | | |
| Low-level input voltage | ge, V _{IL} , as a percentage of V _{CC1} | | | 25% | | | 25% | |
| High-level output clar | np current | | | 20 | | | 20 | mA |
| Low-level output clan | np current | | | - 20 | | | - 20 | mA |
| Clock frequency, f _{clo} | ck (see Figure 2) | 0 | | 8 | 0 | | 8 | MHz |
| Duration of high or lo | w clock pulse, t _w | 62 | | | 62 | - | | ns |
| Catus time t | Data inputs before clock1 | 20 | | | 20 | | MAX 13.2 100 25% 20 -20 | |
| Setup time, t _{SU} | Select inputs before strobe↓ | 50 | | | 50 | | | ns |
| | Data inputs after clock1 (see Note 2) | 50 | | | 50 | | | |
| Hold time, th | Strobe input high after clock1 | 50 | | | 50 | | | ns |
| | Select inputs after strobe↑ | 50 | | | 50 | | | |
| Operating free-air tem | perature, T _A | -40 | | 85 | 0 | | 70 | °C |

NOTE 2: For operation above 25 °C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating free-air temperature range

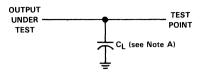
| | PARAMETER | TEST CO. | NOTIONS | SN65500E | | | SN75500E | | | UNIT |
|-------|---------------------------|-----------------------------|---------------------------------------|----------|------------------|-------|----------|------------------|-------|------|
| | PARAMETER | TEST CONDITIONS | | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | UNIT |
| VIK | Input clamp voltage | $V_{CC1} = 12 V$, | I _I = -12 mA | | - 1 | - 1.5 | | - 1 | - 1.5 | ٧ |
| | | V _{CC1} = 13.2 V, | $I_{OH} = -1 \text{ mA}$ | 94 | 97.5 | | 95 | 97.5 | | _ |
| ∨он | High-level output voltage | | $I_{OH} = -10 \text{ mA}$ | 92 | 94.5 | | 93 | 94.5 | | V |
| | | V _{CC2} = 100 V | I _{OH} = -15 mA | 90 | 93.5 | | 91 | 93.5 | | |
| | | V _{CC1} = 13.2 V, | I _{OL} = 1 mA | | 0.85 | 2 | | 0.85 | 2 | |
| VOL | Low-level output voltage | | I _{OL} = 10 mA | | 2 | 4 | | 2 | 4 | V |
| | | V _{CC2} = 100 V | I _{OL} = 15 mA | | 2.75 | 5 | | 2.75 | 5 | |
| Vari | Output clamp voltage | V 0 | I _O = 20 mA | | 1 | 2.5 | | 1 | 2.5 | V |
| VOK | Output clamp voltage | V _{CC2} = 0 | $I_0 = -20 \text{ mA}$ | | -1.2 | - 2.5 | | -1.2 | -2.5 | V |
| IIH · | High-level input current | $V_{CC1} = 13.2 \text{ V},$ | V _I = V _{IH} min | | | 1 | | | 1 | μΑ |
| IL | Low-level input current | $V_{CC1} = 13.2 \text{ V},$ | V _I = V _I L max | | | - 1 | | | - 1 | μΑ |
| ICC1 | Supply current | $V_{CC1} = 13.2 \text{ V},$ | V _{CC2} = 100 V | | 0.05 | 1 | | 0.05 | 1 | mA |
| ICC2 | Supply current | $V_{CC2} = 100 \text{ V}$ | | | 1 | 5 | | 1 | 3 | mA |

 $^{^{\}dagger}$ All typical values are at V_{CC1} = 12 V, T_A = 25 °C.

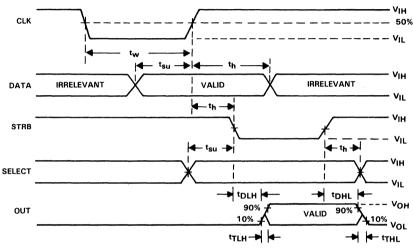
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25 °C

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|-------------------------|-----|-----|------|
| tDHL Delay time, high-to-low-level output from strobe input | | | 250 | ns |
| t _{DLH} Delay time, low-to-high-level output from strobe input | C _L = 30 pF, | | 450 | ns |
| t _{THL} Transition time, high-to-low-level output | See Figure 1 | | 200 | ns |
| t _{TLH} Transition time, low-to-high-level output | · | | 300 | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



VOLTAGE WAVEFORMS

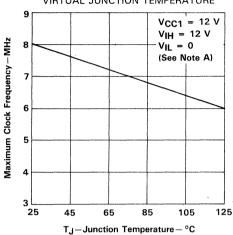
NOTE A. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY vs

VIRTUAL JUNCTION TEMPERATURE



NOTE A: This curve assumes a symmetrical clock pulse.

FIGURE 2

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta J A}$$

$$T_J = T_C + P_D R_{\theta J C}$$

where

T_J = virtual junction temperature

 T_A = free-air temperature

 $P_D = \mbox{average device power dissipation} \label{eq:pd}$

 R_{θ} = thermal resistance (junction-to-air, $R_{\theta}JA$, or junction-to-case, $R_{\theta}JC$)

| PACKAGE TYPE | $R_{\theta JA}$ | $R_{\theta JC}$ |
|-------------------|-----------------|-----------------|
| FN 44-pin plastic | 70°C/W | 22°C/W |
| N 40-pin plastic | 97°C/W | 27 °C/W |

SN65501E, SN75501E AC PLASMA DISPLAY DRIVERS

D2472, MARCH 1983-REVISED OCTOBER 1989

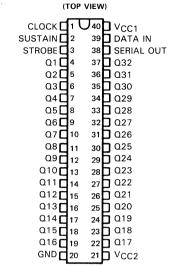
- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Standby Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN75501C

description

The SN65501E and SN75501E are monolithic BIDFET[†] integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

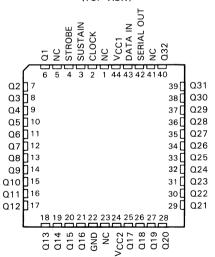
The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low will switch low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the sustain pulse required in the operation of an acplasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low standby power consumption. All outputs contain clamp diodes to the VCC2 and GND supply inputs.

The SN65501E is characterized for operation over the temperature range of $-40\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$. The SN75501E is characterized for operation over the temperature range of $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.



N PACKAGE

FN PACKAGE (TOP VIEW)



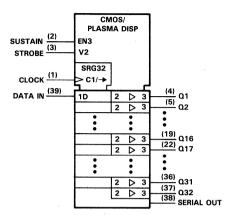
NC-No internal connection

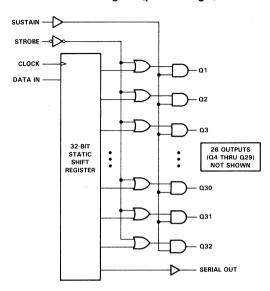
†BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip - patented process



logic symbol†

functional block diagram (positive logic)





 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the N package.

FUNCTION TABLE

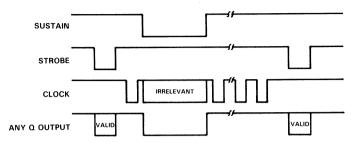
| | | INPUTS | | | OUTPUTS | | | | | | |
|----------|------|--------|--------|---------|-----------------|-----------------|----------------------------------|------------------|----|----|--------|
| FUNCTION | DATA | СГОСК | STROBE | SUSTAIN | R1 | SHIFT I | REGISTER R3 R32 | SERIAL DATA | Q1 | Q2 | Q3 Q32 |
| 1040 | Н | 1 | Н | Н | Н | | R2 _n R31 _n | R32 _n | Н | Н | НН |
| LOAD | L | 1 | н | н | L | R1 _n | R2 _n R31 _n | R32 _n | Н | Н | нн |
| STROBE | Х | Х | Н | Н | R1 _n | R2 _n | R3 _n R32 _n | R32 _n | Н | Н | нн |
| STRUBE | Х | Н | L | Н | R1 _n | R2n | $R3_n \dots R32_n$ | R32 _n | R1 | R2 | R3 R32 |
| SUSTAIN | Х | Х | Х | L | R1 _n | R2 _n | R3 _n R32 _n | R32 _n | L | L | L L |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

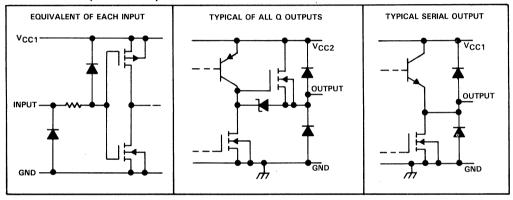
R1...R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.

R1_n . . . R32_n = levels at shift-register outputs R1 through R32 respectively, before the most recent † transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC1} (see Note 1) |
|---|
| Supply voltage, VCC2 |
| Input voltage |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA: SN65501E40°C to 85°C |
| SN75501E 0°C to 70°C |
| Storage temperature range – 65 °C to 150 °C |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| FN | 1775 mW | 14.2 mW/°C | 1136 mW | 923 mW |
| N | 1275 mW | 10.2 mW/°C | 816 mW | 663 mW |



SN65501E, SN75501E AC PLASMA DISPLAY DRIVERS

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT | |
|-----------------------------|--|--|-----------------------|-----|---|------|----|
| Supply voltage, V | CC1 | | 10.8 | 12 | 13.2 | ٧ | |
| Supply voltage, V | CC2 | | 0 | | 100 | | |
| High-level input vo | oltage, V _{IH} | | 0.75 V _{CC1} | | | | |
| Low-level input vo | Itage, V _{IL} | | | | 0.25 V _{CC1} | V | |
| High-level Q outpu | t clamp current, IOH | КН | | | 20 | mA | |
| Low-level Q outpu | Q output clamp current, I _{OKL} -20 | | | | I Q output clamp current, IOKL | | mA |
| Clock frequency, f | clock, at or below, | 25°C junction temperature (see Note 2) | 0 | | 8 | MHz | |
| Duration of high o | r low clock pulse, t _v | v | 62 | | | ns | |
| Cotum time t | Data inputs before | e CLOCK† | 20 | | | ns | |
| Setup time, t _{SU} | Data inputs after | CLOCK† | 50 | | 13.2 100 0.25 V _{CC1} 20 -20 | ns | |
| Hald since 4 | STROBE high after | er CLOCK† | 150 | | 13.2 100 0.25 V _{CC1} 20 - 20 8 | | |
| Hold time, th | STROBE high afte | r SUSTAIN† | 250 | | | ns | |
| Onesetina free six | SN65501E | | -40 | | 85 | °C | |
| Operating free-air | temperature, IA | SN75501E | 0 | | 20 -20 8 8 | | |

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above $T_J = 25\,^{\circ}\text{C}$.

electrical characteristics over recommended operating free-air temperature range

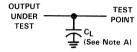
| | | | oo | UDITIONS | S | N65501 | E | s | N75501 | E | |
|------------------|--------------------------------|--------------------------------------|---|--|-----|------------------|-------|-----|------------------|-------|-------------|
| | PARAMET | EK | TEST CO | NDITIONS | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | UNIT |
| VIK | Input clamp vol | tage | V _{CC1} = 12 V, | I _I = 12 mA | | - 1 | - 1.5 | | - 1 | - 1.5 | > |
| | | | V12.2.V | I _{OH} = -1 mA | 94 | 97.5 | | 95 | 97.5 | | |
| \ _{\/=} | High-level | Q outputs | V _{CC1} = 13.2 V, | I _{OH} = -10 mA | 92 | 94.5 | | 93 | 94.5 | | v |
| Vон | output voltage | | V _{CC2} = 100 V | I _{OH} = -15 mA | 90 | 93.5 | | 91 | 93.5 | | V |
| | | SERIAL OUT | $V_{CC1} = 10.8 \text{ V},$ | $I_{OH} = -100 \mu A$ | 9 | 10 | | 9 | 10 | | |
| | | | V 12.2.V | I _{OL} =1 mA | | 0.85 | 2 | | 0.85 | 2 | - |
| ., | Low-level Q our output voltage | Q outputs | puts $V_{CC1} = 13.2 \text{ V},$ $V_{CC2} = 100 \text{ V}$ | I _{OL} = 10 mA | | 2 | 4 | | 2 | 4 | V |
| VOL | | put voltage | | I _{OL} = 15 mA | | 2.75 | 5 | | 2.75 | 5 | V |
| | | SERIAL OUT | , V _{CC1} = 10.8 V, | I _{OL} = 100 μA | - | 0.1 | 1 | | 0.1 | 1 | |
| | Output clamp | 0 | V0 | I _{OK} = 20 mA | | 1 | 2.5 | | 1 | 2.5 | 5 , |
| Voк | voltage | Q output | V _{CC2} =0 | I _{OK} = -20 mA | | -1.2 | -2.5 | | -1.2 | -2.5 | V |
| | High-level | | V _{CC1} = 13.2 V, | V _{IH} = V _{IH} min, | | | 1 | | | 1 | |
| ΉΗ | input current | | V _{CC2} = 100 V | | | | | | | ' | μΑ |
| t | Low-level | | V _{CC1} = 13.2 V, | V _{IL} = V _{IL} max, | | | 1 | | | -1 | ^ |
| l L | input current | | V _{CC2} = 100 V | | | | 1 | l | | - 1 | μΑ |
| | | | V _{CC1} = 13.2 V, | | | 0.05 | 1 | | 0.05 | | 4 |
| ICC1 | Supply current | Supply current from V _{CC1} | | | | 0.05 | ' | | 0.05 | ' | mA |
| lcc2 | Supply current | from V _{CC2} | V _{CC2} = 100 V | | | 1 | 5 | | 1 | 3 | mA |

 $^{^{\}dagger}$ Typical values are at VCC1 = 12 V, TA = 25 °C.

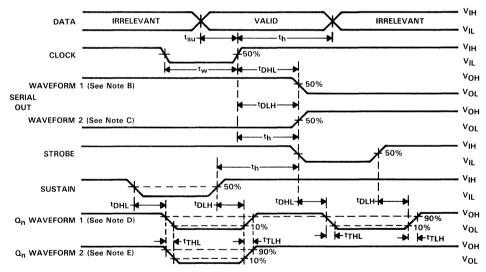
switching characteristics, VCC1 = 12 V, VCC2 = 100 V, TA = 25°C

| | | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|-----------------|-------------------------------|------------------------|-----|-----|-----|------|
| | Delay time, | STROBE to Q outputs | C _L = 30 pF | | | 250 | |
| tDHL | high-to-low- | SUSTAIN to Q outputs | C _L = 30 pF | | | 250 | ns |
| | level outputs | CLOCK to SERIAL OUT | C _L = 20 pF | | | 147 | |
| | Delay time, | STROBE to Q outputs | C _L = 30 pF | | | 450 | |
| tDLH | low-to-high- | SUSTAIN to Q outputs | C _L = 30 pF | | | 450 | ns |
| 1. | level outputs | CLOCK to SERIAL OUT | C _L = 20 pF | | | 147 | |
| tTHL | Transition time | e, high-to-low-level Q output | C _L = 30 pF | | | 200 | ns |
| tTLH | Transition time | e, low-to-high-level Q output | C _L = 30 pF | | | 300 | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD TEST CIRCUIT



NOTES: A. C_L includes probe and jig capacitance.

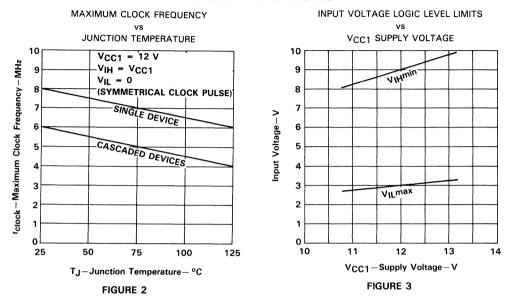
- B. Serial out waveform for internal conditions such that a low is registered in R32.
- C. Serial out waveform for internal conditions such that a high is registered in R32.
- D. \mathbf{Q}_n output with a low stored in associated register $\mathbf{R}_n.$
- E. Q_n output with a high stored in associated register R_n .

VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING CHARACTERISTICS







THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature

TA = free-air temperature

PD = average device power dissipation

 R_{θ} = thermal resistance (junction-to-air, $R_{\theta}JA$, or junction-to-case, $R_{\theta}JC$)

| PACKAGE | R _{OJA} | R _O JC |
|---------|------------------|-------------------|
| FN | 70°C/W | 22 °C/W |
| N | 100°C/W | 27 °C/W |

SN65512B. SN75512B VACUUM FLUORESCENT DISPLAY DRIVERS

D2654, DECEMBER 1985-REVISED OCTOBER 1989

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

description

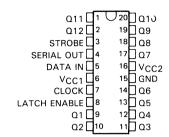
The SN65512B and SN75512B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when opencircuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

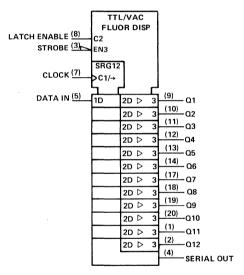
The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-tohigh transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from -40°C to 85°C. The SN75512B is characterized for operation from 0 °C to 70 °C.

DW OR N PACKAGE (TOP VIEW)



logic symbol‡

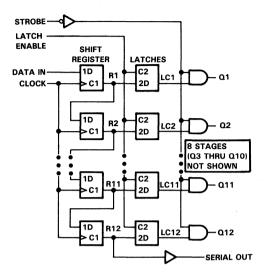


[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[†] BIDFET —Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.



logic diagram (positive logic)



FUNCTION TABLE

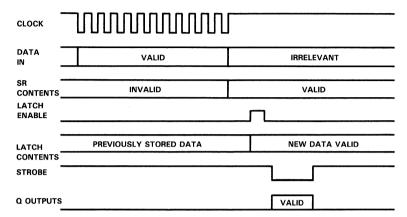
| | CONTROL INPUTS | | SHIFT REGISTER LATCHES | | OUTPUTS | | |
|----------|----------------|--------|------------------------|-----------------------------|---|---------------|-----------------------------|
| FUNCTION | | LATCH | | R1 THRU R12 | | LC1 THRU LC12 | |
| | CLOCK | ENABLE | STROBE | K1 IHRU K12 | LC1 THRU LC12 | SERIAL | Q1 THRU Q12 |
| LOAD | 1 | Х | Х | Load and shift [†] | Determined by LATCH ENABLE‡ | R12 | Determined by STROBE |
| LUAD | Not | х | X X No change | No change | Determined by LATCH ENABLE‡ | R12 | Determined by STROBE |
| LATCH | Х | L | Х | A - d-4 | Stored data | R12 | Determined by STROBE |
| LATCH | X | н | × | As determined above | New data | R12 | Determined by STROBE |
| STROBE | X | Х | Н | A | Determined by LATCH ENABLE‡ | R12 | All L |
| STROBE | x | х | L | As determined above | Determined by LATCH ENABLE [‡] | R12 | LC1 thru LC12, respectively |

 $H = high level, L = low level, X = irrelevant, \uparrow = low-to-high-level transition.$

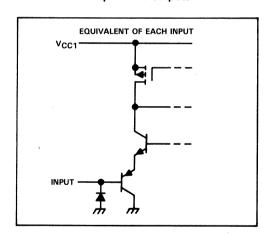
[†]R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

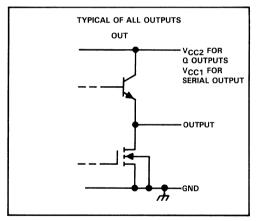
[‡] New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs





SN65512B, SN75512B **VACUUM FLUORESCENT DISPLAY DRIVERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) | 15 V |
|--|-------------------|
| Supply voltage, VCC2 | 70 V |
| Input voltage | V _C C1 |
| Continuous total power dissipation See Dissipation Rating | Table |
| Operating free-air temperature range: SN65512B | 85°C |
| SN75512B | 70°C |
| Storage temperature range | 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW | 585 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

recommended operating conditions

| | | SN65 | 512B | SN75512B | | UNIT |
|---|---|------|------|----------|------|--------|
| | | MIN | MAX | MIN | MAX | UNIT |
| Supply voltage, V _{CC1} | | 5 | 15 | 5 | 15 | V |
| Supply voltage, V _{CC2} | | 0 | 60 | 0 | 60 | V |
| High-level input voltage, VIH | | 2 | | 2 | | V |
| Low-level input voltage, VIL | | | 0.8 | | 0.8 | V |
| High-level output current, IOH | | | - 25 | | - 25 | mA |
| Low-level output current, IOL | V _{CC1} = 10 V | | 5 | | 5 | mA |
| Clock frequency, fclock | $V_{CC1} = 15 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | 0 | 4 | 0 | 4 | MHz |
| Clock frequency, iclock | $V_{CC1} = 5 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | 0 | 1 | 0 | 1 | IVITIZ |
| Pulse duration, CLOCK high or low, tw | $V_{CC1} = 15 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | 100 | | 100 | | ns |
| ruise duration, CLOCK high or low, t _W | V _{CC1} = 5 V, T _A = 25°C | 500 | | 500 | | ris |
| Setup time, DATA IN before CLOCK1, | V _{CC1} = 15 V, T _A = 25°C | 100 | | 100 | | |
| t _{SU} (see Figure 1) | $V_{CC1} = 5 \text{ V}, T_A = 25 ^{\circ}\text{C}$ | 250 | | 250 | | ns |
| Hold time, DATA IN after CLOCK1, th | V _{CC1} = 15 V, T _A = 25°C | 50 | | 50 | | |
| (see Figure 1) | V _{CC1} = 5 V, T _A = 25°C | 250 | | 250 | | ns |
| Operating free-air temperature, TA | | -40 | 85 | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range, VCC2 = 60 V (unless otherwise noted)

| | PARAMETER | | TEST CON | IDITIONS | MIN | TYP [†] | MAX | UNIT |
|--|--------------------------------------|---|--------------------------|-------------------------|------|------------------|-------|------|
| VIK | Input clamp voltage | | $l_1 = -12 \text{ mA}$ | | | | -1.5 | V |
| V | High-level output | Q outputs | I _{OH} = -25 mA | | 57.5 | 58 | | V |
| Vон | voltage Serial output | | $I_{OH} = -200 \mu A$ | $V_{CC1} = 10 V$ | 9 | 9.5 | | · |
| 1/ | Low-level output | Q outputs | $I_{OL} = 5 \text{ mA},$ | V _{CC1} = 10 V | | 2.6 | 5 | V |
| VoL | voltage | Serial output | $I_{OL} = 200 \mu A$, | V _{CC1} = 10 V | | 0.05 | 0.2 | · · |
| ΊΗ | High-level input current | | $V_{CC1} = 15 V_{r}$ | V _I = 5 V | | 0.01 | 1 | μΑ |
| ηL | Low-level input current | | $V_{CC1} = 15 V$, | $V_1 = 0.8 V$ | | - 25 | - 150 | μΑ |
| 1 | Summer to a very very | | Vac 15 V | V _I = 5 V | | 80 | 500 | μΑ |
| lcc1 | Supply current from V _{CC1} | | $V_{CC1} = 15 V$ | $V_1 = 0.8 \text{ V}$ | | 2 | 6 | mA |
| Complete and the Comple | | 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | V 15 V | All outputs high | | 10 | 100 | μΑ |
| lcc2 | Supply current from V _{CC2} | | V _{CC1} = 15 V | STROBE at 2 V | | 0.8 | 3 | mA |

 $^{^{\}dagger}AII$ typical values are at $V_{CC1}~=~10$ V, $T_{A}~=~25\,^{o}C.$



switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------|---|-----------------|-----|-----|------|
| tDHL | Delay time, high-to-low-level output | | | 300 | ns |
| tDLH | Delay time, low-to-high-level output | $C_L = 30 pF$, | | 300 | ns |
| tTHL | Transition time, high-to-low-level output | See Figure 2 | | 500 | ns |
| tTLH | Transition time, low-to-high-level output | | | 500 | ns |

PARAMETER MEASUREMENT INFORMATION

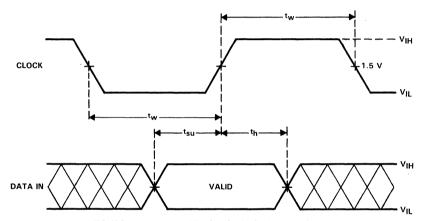


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

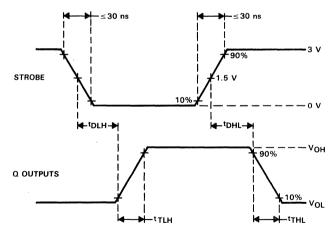
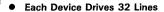


FIGURE 2. SWITCHING-TIME VOLTAGE WAVEFORMS

SN65518, SN75518 VACUUM FLUORESCENT DISPLAY DRIVERS

N PACKAGE

D2720, MARCH 1983-REVISED MAY 1990



- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- Latches on All Driver Outputs

description

The SN65518 and SN75518 are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

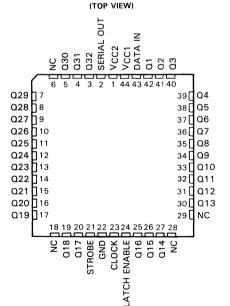
The devices each consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from $-40\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$ and the SN75518 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

| (| гор \ | /IEW | n |
|--|--|--|--------------------------|
| VCC2 C SERIAL OUT G 032 C 031 C 030 C 029 C 028 C 027 C | 1 2 3 4 5 6 7 8 9 10 11 | 40 39 38 37 36 35 34 33 32 31 30 29 28 | VCC1 DATA IN 01 02 03 04 |
| 001 | 13 | 28 | 012 |
| 020 | 15 | 26 | Q13 |
| Q19 [Q18 [| 16 17 | 25 24 | 014 1015 |
| Q17 [| 18 | 23 | |
| STROBE C | 19 20 | 22 21 | LATCH ENABLE |

FN PACKAGE

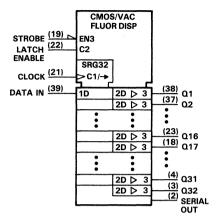


[†]BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

NC-No internal connection

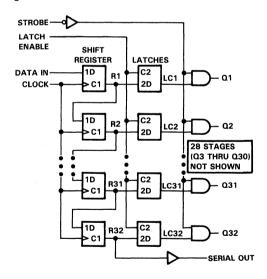


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the N package.

logic diagram (positive logic)

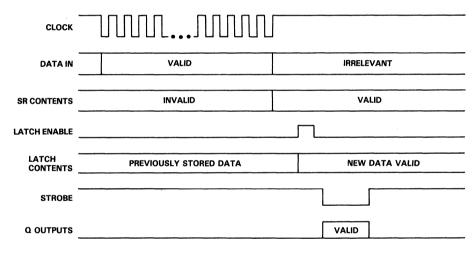


FUNCTION TABLE

| | CONTROL INPUTS | | | SHIFT REGISTERS | LATCHES | OUTPUTS | | |
|----------|----------------|-----------------|--------|--|--|---------|--------------------------------------|--|
| FUNCTION | CLOCK | LATCH ENABLE | STROBE | R1 THRU R32 | LC1 THRU LC32 | SERIAL | Q1 THRU Q32 | |
| LOAD | † No† | X X | X X | Load and shift [†] No change | Determined by LATCH ENABLE [‡] | R32 | Determined by STROBE | |
| LATCH | X X | L H | X X | As determined above | Stored data New Data | R32 | Determined by STROBE | |
| STROBE | X X | X X | H | As determined above | Determined by LATCH ENABLE [‡] | R32 | All L LC1 thru LC32, respectively | |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

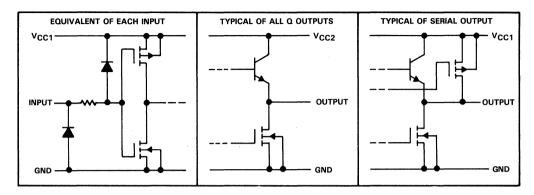
typical operating sequence



[†]R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

[‡]New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) |
|--|
| Supply voltage, VCC2 |
| Input voltage, V _I |
| Continuous total power dissipation |
| Operating free-air temperature range, TA: SN65518 |
| SN75518 |
| Storage temperature range65 °C to 150 °C |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package 260 °C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| | PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| I | FN | 1700 mW | 13.6 mW/°C | 1088 mW | 884 mW |
| ١ | N | 1250 mW | 10.0 mW/°C | 800 mW | 650 mW |

recommended operating conditions, T_A = 25 °C (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|---|---------------------------------|------|------|-------|--|
| Supply voltage, V _{CC1} | | 4.5 | 15 | V | |
| Supply voltage, V _{CC2} | 0 | 60 | V | | |
| High level input valtage Viv. (see Figure 1) | V _{CC1} = 4.5 V | 3.5 | | V | |
| High-level input voltage, V _{IH} (see Figure 1) | V _{CC1} = 15 V | 12 | | \ \ \ | |
| Low-level input voltage, V _{IL} (see Figure 1) | | -0.3 | 0.8 | ٧ | |
| High-level output current, IOH | | | - 25 | mA | |
| Low-level output current, IOL | | | 2 | mA | |
| Clock frequency, f _{clock} (see Figure 2) | V _{CC1} = 10 V to 15 V | 0 | 5 | MHz | |
| | V _{CC1} = 4.5 V | 0 | 1 | IVIHZ | |
| D. I 01.00K111 | V _{CC1} = 10 V to 15 V | 100 | | | |
| Pulse duration, CLOCK high, tw(CKH) | V _{CC1} = 4.5 V | 500 | | ns | |
| Bules duration CLOCK law to come | V _{CC1} = 10 V to 15 V | 100 | | | |
| Pulse duration, CLOCK low, tw(CKL) | V _{CC1} = 4.5 V | 500 | | ns | |
| Setum time DATA IN before CLOCKA t | V _{CC1} = 10 V to 15 V | 75 | | | |
| Setup time, DATA IN before CLOCK [†] , t _{SU} | V _{CC1} = 4.5 V | 150 | | ns | |
| Hold time DATA IN often CLOCKA A. | V _{CC1} = 10 V to 15 V | 75 | | | |
| Hold time, DATA IN after CLOCK1, th | V _{CC1} = 4.5 V | 150 | | ns | |
| Otititi | SN65518 | -40 | 85 | °C | |
| Operating free-air temperature, TA | SN75518 | 0 | 70 | ا ا | |

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1} (unless otherwise noted), $V_{CC2} = 60 \text{ V}$

| | PARAMETER | | TEST C | CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------|---------------------------|------------|--------------------------|-----------------------------|------|------------------|------|------|
| VIK | Input clamp voltage | | I ₁ = -12 mA | | | | -1.5 | V |
| Van | High-level output voltage | Q outputs | IOH ≈ -25 mA | | 57.5 | 58 | | V |
| Voн | High-level output voltage | SERIAL OUT | $V_{CC1} = 5 V$, | I _{OH} = -20 μA | 4.5 | 4.9 | 5 | V |
| \/a: | Law layer output valtage | Q outputs | IOL = 1 mA | | | | 5 | v |
| VOL | Low-level output voltage | SERIAL OUT | $I_{OL} = 20 \mu A$ | | | 0.06 | 0.8 | · |
| Ιн | High-level input current | | V _{CC1} = 15 V, | V ₁ = 15 V | | 0.1 | 1 | μΑ |
| I _I L | Low-level input current | | $V_{CC1} = 15 V$, | V _I = 0 V | | -0.1 | 1 | μΑ |
| | Summit aurent | | V _{CC1} = 4.5 V | | 1 | 1.8 | 4 | mA |
| ICC1 | Supply current | | V _{CC1} = 15 V | | } | 2 | 5 | mA |
| | | SN65518 | Outputs high, | $T_A = -40$ °C | | | 12 | |
| I _{CC2} | Supply current | SN65518, | Outputs high, | T _A = 0°C to MAX | | 7 | 10 | mA |
| | | SN75518 | Outputs low | | | 0.01 | 0.5 | |

 $^{^{\}dagger}$ All typical values are at $T_{A} = 25\,^{\circ}$ C.

switching characteristics, $V_{CC2} = 60 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25 \,^{\circ}\text{C}$ (unless otherwise noted)

| | PARA | | TEST CONDITIONS | MIN MAX | UNIT | |
|--|---|--------------------------|--------------------------|--------------|------|-----|
| • . | Delay time, CLOCK to DATA O | V _{CC1} = 4.5 V | C _L = 15 pF, | 600 | ns | |
| ^t d | Delay time, CLOCK to DATA O | 0.1 | V _{CC1} = 15 V | See Figure 4 | 150 | 115 |
| | t _{DHL} Delay time, high-to-low-level Q output | from LATCH ENABLE | V _{CC1} = 4.5 V | See Figure 5 | 1.5 | |
| †DHL | | from STROBE | | See Figure 6 | 1 | |
| | | from LATCH ENABLE | V _{CC1} = 15 V | See Figure 5 | 0.5 | μS |
| | | from STROBE | | See Figure 6 | 0.5 | |
| | Delay time, low-to-high-level | from LATCH ENABLE | V _{CC1} = 4.5 V | See Figure 5 | 1.5 | |
| tDLH | | from STROBE | | See Figure 6 | 1 | |
| | Q output | from LATCH ENABLE | V 15 V | See Figure 5 | 0.25 | μS |
| | | from STROBE | V _{CC1} = 15 V | See Figure 6 | 0.25 | |
| | T | | V _{CC1} = 4.5 V | See Figure 6 | 3 | |
| tthL Transition time, high-to-low-leve | | ei a output | V _{CC1} = 15 V | See Figure 6 | 1.5 | μS |
| | tti H Transition time, low-to-high-level Q output | | V _{CC1} = 4.5 V | See Figure 6 | 2.5 | |
| tTLH | Transition time, low-to-nigh-lev | er a output | V _{CC1} = 15 V | See rigure 6 | 0.75 | μS |

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS

vs SUPPLY VOLTAGE V_{CC1}

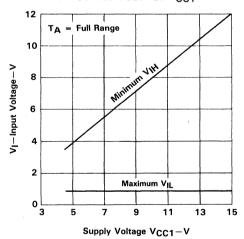


FIGURE 1

MAXIMUM INPUT DATA RATE

vs

SUPPLY VOLTAGE V_{CC1}

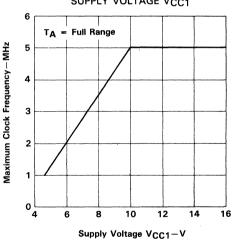


FIGURE 2

PARAMETER MEASUREMENT INFORMATION[†]

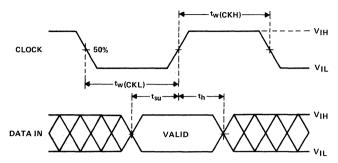


FIGURE 3. INPUT TIMING VOLTAGE WAVEFORMS

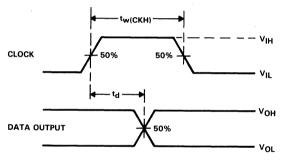


FIGURE 4. DATA OUTPUT SWITCHING TIMES

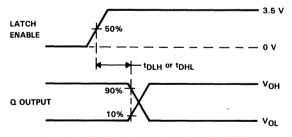


FIGURE 5. Q OUTPUT SWITCHING TIMES

 $^{^{\}dagger}\text{For testing purposes, all input pulses have maximum rise and fall times of 30 ns.$

PARAMETER MEASUREMENT INFORMATION[†]

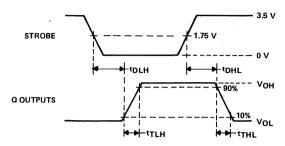


FIGURE 6. SWITCHING-TIME VOLTAGE WAVEFORMS

[†]For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

SN65551, SN65552, SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVERS

DUAL-IN-LINE-PACKAGES

(TOP VIEW)

D2743, MARCH 1983-REVISED OCTOBER 1989

- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

description

The SN65551, SN65552, SN75551, and SN75552 are monolithic BIDFET[†] integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence is reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65551 and SN65552 are characterized for operation from $-40\,^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$. The SN75551 and SN75552 are characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

| SN65! | 551, 9 | SN7! | 5551 |
|------------|--------|------|--------------|
| Q16 🗖 | 1 U | 40 |] 015 |
| Q17 🗖 | 2 | 39 |] Q14 |
| Q18 🗖 | 3 | 38 |] Q13 |
| 019 🗖 | 4 | 37 |] Q12 |
| 020 🗆 | 5 | 36 | 3 |
| 021 🛘 | 6 | 35 |] Q10 |
| 022 🗆 | 7 | 34 |] |
| 023 🗖 | 8 | 33 |] 08 |
| 024 🗖 | 9 | 32 |] Q7 |
| 0.25 🗖 | 10 | 31 |] Q6 |
| Q26 🗖 | 11 | 30 |] Q5 |
| 0.27 | 12 | 29 |] Q4 |
| 0.28 | 13 | 28 |] 03 |
| 0.29 | 14 | 27 |] Q2 |
| 030 □ | 15 | 26 |] Q1 |
| Q31 🗖 | 16 | 25 |] NC |
| Q32 🗖 | 17 | 24 | DATA IN |
| SERIAL OUT | 18 | 23 | STROBE |
| ENABLE 🕻 | 19 | 22 | □∨cc |
| сьоск П | 20 | 21 | SUBSTRATE |

SN65552, SN75552

COMMON

| 017 | 1 U | 40 | 1 018 |
|--------------|-----|----|--------------|
| Ω16 🗖 | 2 | 39 | 1 019 |
| Ω15 🗖 | 3 | 38 |] 020 |
| Q14 🗖 | 4 | 37 | 1 021 |
| Ω13 🗖 | 5 | 36 | D 022 |
| 012 | 6 | 35 | 1 023 |
| Q11 🗀 | 7 | 34 | D 024 |
| 010 □ | 8 | 33 |] Q25 |
| ⊙ 9 🗖 | 9 | 32 | D Q26 |
| 08 □ | 10 | 31 | D 027 |
| ۵7 ◘ | 11 | 30 | 1 028 |
| σ 6 ⊑ | 12 | 29 | Q29 |
| Q5 🗖 | 13 | 28 | _ 030 |
| Q4 [| 14 | 27 | Q 31 |
| σ3 ⊏ | 15 | 26 | 1 032 |
| Q2 [| 16 | 25 | □ NC |
| Q1 [| 17 | 24 | DATA IN |
| SERIAL OUT | 18 | 23 | STROBE |
| ENABLE 🗀 | 19 | 22 | □∨cc |
| CLOCK 🗀 | 20 | 21 | SUBSTRATE |
| , | | | COMMON |

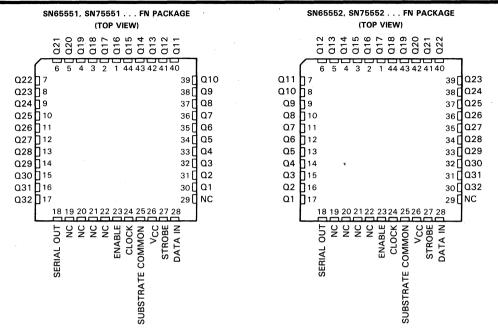
NC-No internal connection

†BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip - patented process.



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SN65551, SN65552, SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVERS



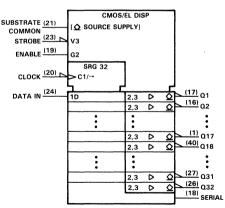
NC-No internal connection

logic symbols†

SN65551, SN75551

CMOS/EL DISP SUBSTRATE (21) SOURCE SUPPLY COMMON STROBE (23) V٦ ENABLE (19) SRG 32 CLOCK (20) DATA IN (24) (2<u>6)</u> Q1 1D ٥ (<u>27)</u> Q2 (4<u>0)</u> Q15 D (1) Q16 2,3 D (<u>16)</u> Q31 2,3 ٥ (17) Q32 2,3 D (18) SERIAL OUT

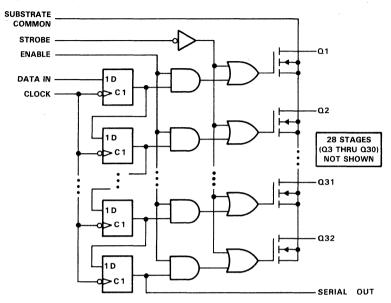
SN65552, SN75552



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol here indicates an n-channel open-drain output.

Pin numbers shown are for the N package.

logic diagram (positive logic)



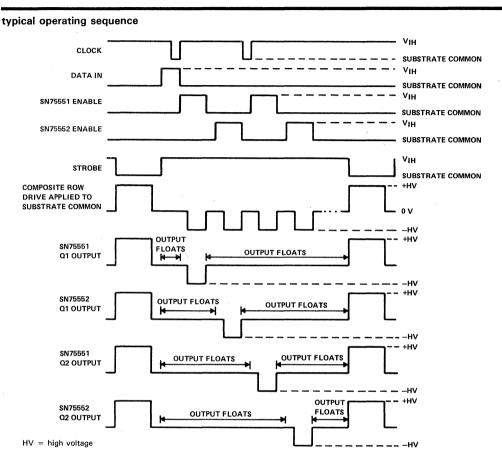
FUNCTION TABLE

| FUNCTION5 | CONTROL INPUTS | | | SHIFT REGISTERS | | OUTPUTS |
|-----------|----------------|--------|--------|-----------------------------|--------|---------------------------------|
| FUNCTIONS | CLOCK | ENABLE | STROBE | R1 THRU R32 | SERIAL | Q1 THRU Q32 |
| LOAD | + | X | Х | Load and Shift [†] | R32 | Determined by ENABLE and STROBE |
| LOAD | No ↓ | X | × | No Change | R32 | Determined by ENABLE and STROBE |
| ENABLE | X | L | Н | As determined above | R32 | All Q outputs off |
| ENABLE | × | н | н | As determined above | R32 | Determined by R1 through R32 |
| STROBE | Х | Х | L | As determined above | R32 | All Q outputs on |

 $H = high level, L = low level, X = irrelevant, \downarrow = high-to-low transition.$

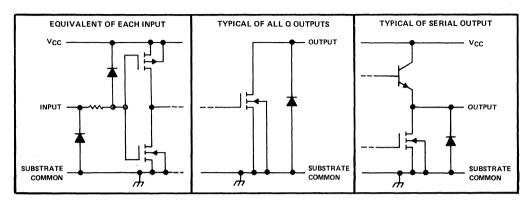
[†]Register R32 takes on the state of R31, R31 takes on the state of R30,...R2 takes on the state of R1, and R1 takes on the state of the data input.

SN65551, SN65552, SN75551, SN75552 **ELECTROLUMINESCENT ROW DRIVERS**



NOTE: During operation CLOCK, DATA IN, ENABLE, and STROBE are referenced to the Composite Row Drive signal received at the SUBSTRATE COMMON pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Off-state Q output voltage, VO(off) |
| Input voltage |
| Substrate common terminal current (see Note 2) |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN65551, SN6555240°C to 85°C |
| SN75551, SN75552 0 °C to 70 °C |
| Storage temperature range65 °C to 150 °C |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package 260 °C |

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.

2. Duty cycle is limited by package dissipation.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| FN | 1700 mW | 13.6 mW/°C | 1088 mW | 884 mW |
| N | 1250 mW | 10.0 mW/°C | 800 mW | 650 mW |

SN65551, SN65552, SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVERS

recommended operating conditions

| | | | | MIN | NOM | MAX | UNIT | |
|---------------------|--|------------------|---|-------|-----|------|------|--|
| Vcc | Supply voltage | | | 10.8 | 12 | 15 | ٧ | |
| V | 'IH High-level input voltage (see Figure 1) | | V _{CC} = 10.8 V | 8.1 | | 11.1 | V | |
| VIН | | | V _{CC} = 15 V | 11.25 | | 15.3 | v | |
| V 1 | | \ | V _{CC} = 10.8 V | -0.3 | | 2.7 | v | |
| VIL | Low-level input voltage (see Figure 1) | | V _{CC} = 15 V | -0.3 | | 3.75 | · · | |
| V _{O(off)} | Off-state Q output voltage | | | | | 200 | ٧ | |
| 1 | On-state output current, duty cycle \leq 1%, (see Figures 2, 3, and 4) | | V _{CC} = 10.8 V, T _A = 25°C | | | 50 | mA | |
| 'O(on) | | | V _{CC} = 15 V, T _A = 25 °C | T | | 80 | mA | |
| ОК | Output clamp current | | | | | 45 | mA | |
| fclock | Clock frequency | - | | 0 | | 4 | MHz | |
| t _W | Pulse duration, CLOCK high or low | | | 125 | | | ns | |
| t _{su} | Setup time, DATA IN before CLOCK (see Figure 5) | | | 50 | | | ns | |
| t _h | Hold time, DATA IN after CLOCK (see Figure 5) | | | 100 | | | ns | |
| т. | Operating free six temperature | SN65551, SN65552 | | -40 | | 85 | °C | |
| TA | Operating free-air temperature | SN75551, S | N75552 | 0 | | 70 | • | |

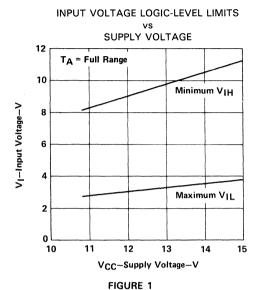
electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|-------------------------------------|----------------|---------------------------------------|-----------------------|-----|------|
| I _{O(off)} | Off-state Q output current | | V _O = 200 V | | 10 | μΑ |
| Vон | High-level output voltage | Serial outputs | $I_{O} = -100 \mu A$ | V _{CC} - 1.5 | | V |
| \/-· | landard and a second and the second | Q outputs | I _{OL} = 50 mA, See Figure 3 | | 30 | v |
| VOL | Low-level output voltage | Serial output | I _{OL} = 100 μA | | 1 | 1 ° |
| lн | High-level input current | | V _I @ V _{CC} | | 1 | μΑ |
| ΊL | Low-level input current | | V _I = 0 | | -1 | μΑ |
| Icc | Supply current from V _{CC} | | | | 250 | μΑ |

switching characteristics, $V_{CC} = 12 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

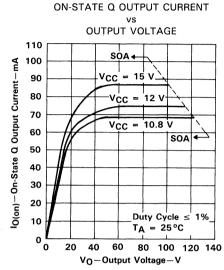
| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|-------------------------------------|--|-----|-----|------|
| + | Propagation delay time, high-to-low | | 200 | ns | |
| ^t PHL . | level SERIAL OUTPUT from CLOCK | C ₁ = 20 pF to ground, See Figure 6 | | 200 | 115 |
| 4 | Propagation delay time, low-to-high | CL = 20 pr to ground, See Figure 6 | | 200 | |
| tPLH | level SERIAL OUTPUT from CLOCK | | | 200 | ns |
| | Turn-on delay time, Q outputs | $I_{OL} = 50$ mA, STROBE at V_{CC} , | | 500 | ns |
| ^t d(on) | from ENABLE | $R_L = 1.4 \text{ k}\Omega$ to 100 V, See Figure 7 | 500 | | 115 |

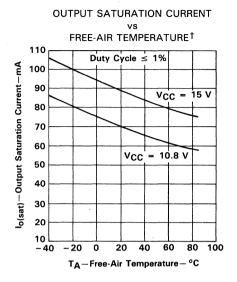
RECOMMENDED OPERATING CONDITIONS



MAXIMUM ON-STATE Q OUTPUT CURRENT SUPPLY VOLTAGE 80 Duty Cycle ≤ 1% Maximum On-State Q Output Current-mA $T_A = 25^{\circ}C$ 75 70 65 60 55 50 10 12 13 14 15 VCC-Supply Voltage-V FIGURE 2

TYPICAL CHARACTERISTICS





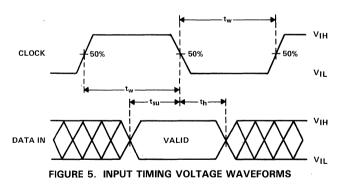
SOA = Safe Operating Area

FIGURE 3

FIGURE 4

[†] Data for temperatures below 0°C and above 70°C apply only for SN65551 and SN65552.

PARAMETER MEASUREMENT INFORMATION



PARAMETER MEASUREMENT INFORMATION

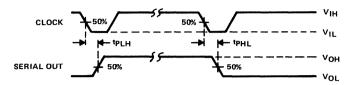


FIGURE 6. VOLTAGE WAVEFORMS, SERIAL OUTPUT

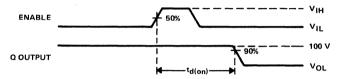


FIGURE 7. VOLTAGE WAVEFORMS, Q OUTPUT

N PACKAGE

D2744, MARCH 1983-REVISED DECEMBER 1989

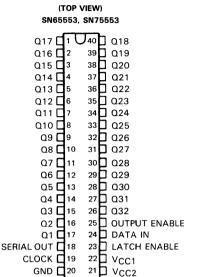
- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

description

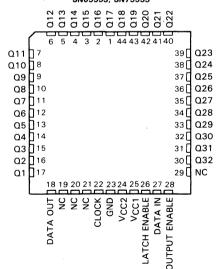
The SN65553, SN65554, SN75553, and SN75554 are monolithic BIDFET[†] integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65554 and SN75554 output sequence is reversed from the SN65553 and SN75553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The \$N65553 and \$N65554 are characterized for operation from -40°C to 85°C. The \$N75553 and \$N75554 are characterized for operation from 0°C to 70°C.



FN PACKAGE (TOP VIEW) SN65553, SN75553

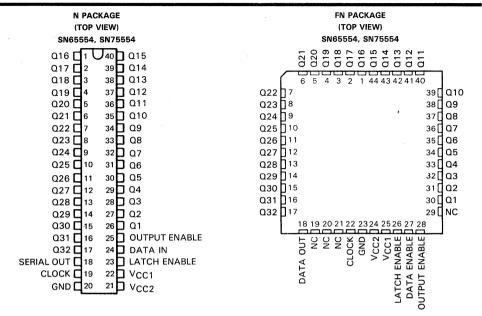


NC-No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

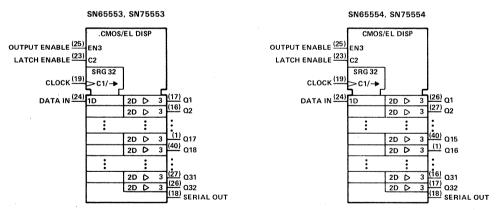


SN65553, SN65554, SN75553, SN75554 **ELECTROLUMINESCENT COLUMN DRIVERS**



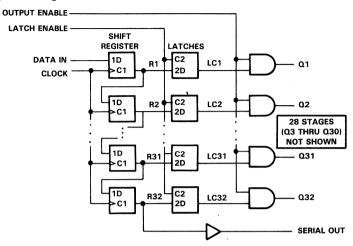
NC-No internal connection

logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for N packages.

logic diagram (positive logic)



FUNCTION TABLE

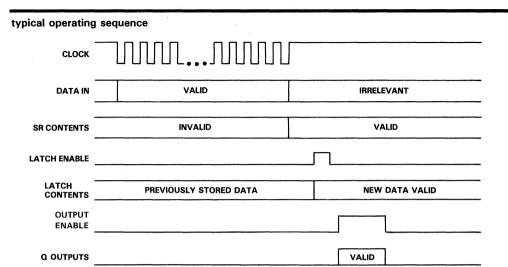
| FUNCTION | CONTROL INPUTS | | | SHIFT REGISTER | LATCHES | OUTPUTS | | |
|----------|----------------|-----------------|------------------|-----------------------------|---------------|---------|-----------------------------|--|
| | CLOCK | LATCH ENABLE | OUTPUT ENABLE | R1 THRU R32 | LC1 THRU LC32 | SERIAL | Q1 THRU Q22 | |
| LOAD | 1 | X | Х | Load and shift [†] | Determined by | R32 | Determined by | |
| | Not | × | x | No change | LATCH ENABLE‡ | R32 | OUTPUT ENABLE | |
| LATCH | Х | L | Х | As determined | Stored data | R32 | Determined by | |
| LATCH | × | н | x | above | New data | R32 | OUTPUT ENABLE | |
| OUTPUT | Х | X | L | As determined | Determined by | R32 | All L | |
| ENABLE | х | x | н | above | LATCH ENABLE‡ | R32 | LC1 thru LC32, respectively | |

H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

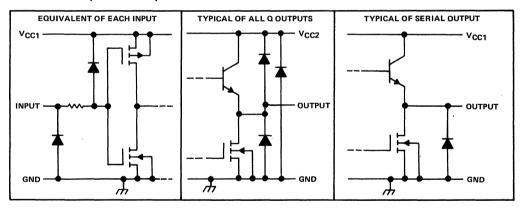
[†]R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

^{*}New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

SN65553, SN65554, SN75553, SN75554 ELECTROLUMINESCENT COLUMN DRIVERS



schematic of inputs and outputs



SN65553, SN65554, SN75553, SN75554 ELECTROLUMINESCENT COLUMN DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC1} (see Note 1) |
|--|
| Supply voltage, VCC2 |
| Input voltage VCC1 + 0.3 V |
| Ground current |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN65553, SN6555440°C to 85°C |
| SN75553, SN75554 0 °C to 70 °C |
| Storage temperature range65°C to 150°C |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package 260 °C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| FN | 1700 mW | 13.6 mW/°C | 1088 mW | 884 mW |
| N | 1250 mW | 10.0 mW/°C | 800 mW | 650 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---------------------------|-------|------|------------------|------|
| Supply voltage, V _{CC1} | | 10.8 | 12 | 15 | V |
| Supply voltage, V _{CC2} | | 0 | | 60 | V |
| High level input valence V (and Figure 1) | V _{CC1} = 10.8 V | 8.1 | | 11.1 | V |
| High-level input voltage, V _{IH} (see Figure 1) | V _{CC1} = 15 V | 11.25 | | 15.3 | V |
| Low-level input voltage, V _{II} (see Figure 1) | V _{CC1} = 10.8 V | -0.3 | | 15 60 11.1 | V |
| Low-level input voltage, VIL (see Figure 1) | -0.3 | | 3.75 | V | |
| High-level output current, IOH | | - 15 | | | mA |
| Low-level output current, IOL | | 15 | | | mA |
| Output clamp current, IOK | | | | 20 | mA |
| Clock frequency, f _{clock} | | 0 | | 6.25 | MHz |
| Pulse duration, CLOCK high or low, tw(CLK) (see Figur | e 2) | 80 | | | ns |
| Pulse duration, LATCH ENABLE, tw(LE) (see Figure 4) | | 80 | | | ns |
| Data setup time before CLOCK 1, t _{su} (see Figure 2) | | 20 | | | ns |
| Data hold time after CLOCK 1, th (see Figure 2) | | | | | ns |
| Operating free-air temperature, Τ _Δ | SN65553, SN65554 | - 40 | | 85 | °C |
| Operating free-air temperature, 1A | SN75553, SN75554 | 0 | | 70 | ٠.ر |

electrical characteristics over recommended ranges of V_{CC1} and operating free-air temperature, V_{CC2} = 60 V (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------|--------------------------------------|------------------|-----------------------------------|------------------------|-----|------|
| | High lavel autout valence | Q outputs | $I_0 = -15 \text{ mA}$ | 57 | | V |
| VOH | High-level output voltage | SERIAL OUT | $I_O = -100 \mu A$ | V _{CC1} - 1.5 | | _ v |
| VOL | Laurelaurelaurelaure | Q outputs | IOL = 15 mA | | 8 | V |
| | Low-level output voltage | SERIAL OUT | $I_{OL} = 100 \mu A$ | | 1 | ľ |
| ΊΗ | High-level input current | | V _I = V _{CC1} | | 1 | μΑ |
| IL | Low-level input current | | V ₁ = 0 | | -1 | μΑ |
| lCC1 | Supply current from V _{CC1} | | | | 5 | mA |
| 1 | Supply current from V _{CC2} | SN65553, SN65554 | | | 12 | ^ |
| ICC2 | | SN75553, SN75554 | | | 10 | mA |

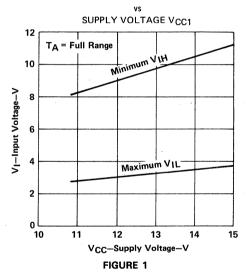
SN65553, SN65554, SN75553, SN75554 ELECTROLUMINESCENT COLUMN DRIVERS

switching characteristics, VCC1 = 12 V, VCC2 = 60 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|---|-----|-----|------|
| tPHL | Propagation delay time, high-to-low-level SERIAL OUT from CLOCK | $C_L = 20 pF to ground,$ | | 140 | ns |
| ^t PLH | Propagation delay time, low-to-high-level SERIAL OUT from CLOCK | C _L = 20 pF to ground, See Figure 3 C _L = 20 pF to ground, | | 140 | ns |
| ^t DHL | Delay time, high-to-low-level Q output from LATCH ENABLE | C _L = 20 pF to ground, See Figure 4 | | 500 | ns |
| ^t DLH | Delay time, low-to-high-level Q output from LATCH ENABLE | C _L = 20 pF to ground, See Figure 4 | | 1 | μS |

RECOMMENDED OPERATION CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS



PARAMETER MEASUREMENT INFORMATION

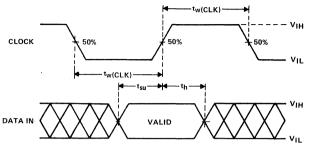


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

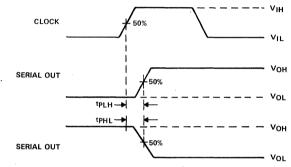


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

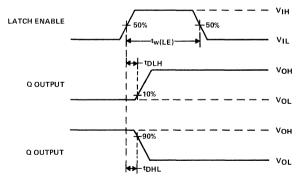


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS



D2744, APRIL 1985-REVISED JULY 1990

- Each Device Drives 32 Electrodes
- 90-V Output Voltage Swing Capability Using Ramped Supply
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

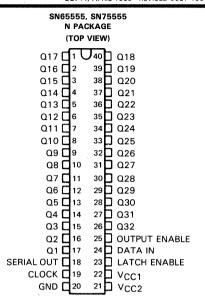
description

The SN65555, SN75555, SN65556, and SN75556 are monolithic BIDFET[†] integrated circuits designed to drive the column electrodes of an electro-luminescent display. The SN65556 and SN75556 output sequence is reversed from the SN65555 and SN75555 for ease in printed circuit board layout.

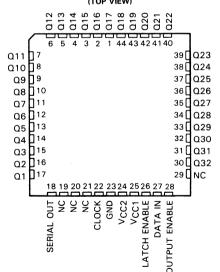
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Data must be loaded into the latches and OUTPUT ENABLE must be high before supply voltage VCC2 is ramped up.

Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65555 and SN65556 are characterized for operation from $-40\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$. The SN75555 and SN75556 are characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.



SN65555, SN75555 FN PACKAGE (TOP VIEW)

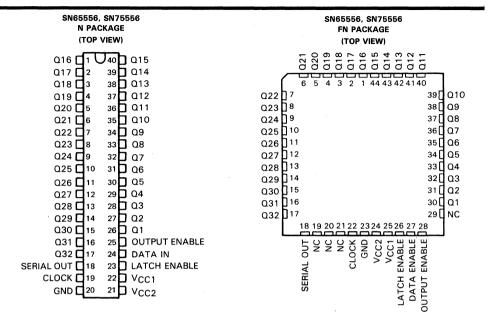


NC-No internal connection

†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

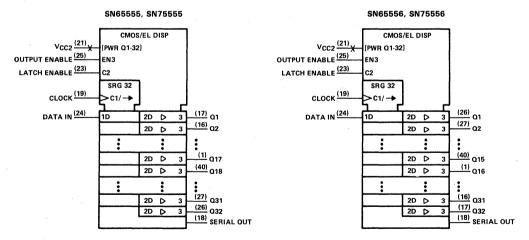


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NC-No internal connection

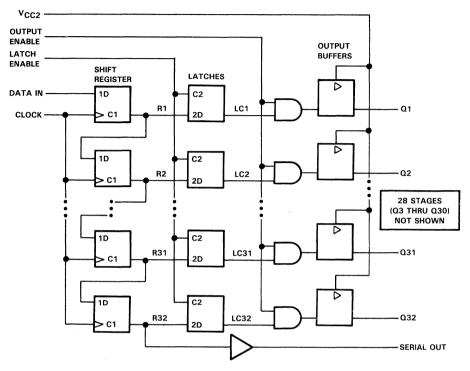
logic symbols†



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for N packages.



logic diagram (positive logic)



FUNCTION TABLE

| FUNCTION | CONTROL INPUTS | | | CHIET DECICTED | LATCHES | OUTPUTS | | | |
|----------|----------------|---|-------------------------|---|---|-----------------------------|-----------------------------|--|--|
| | CLOCK | | OUTPUT ENABLE | SHIFT REGISTER R1 THRU R32 | LC1 THRU LC32 | SERIAL | Q1 THRU Q32 | | |
| 1010 | 1 | Х | Х | Load and shift [†] | D | R32 | D | | |
| LOAD | No↑ | × | × | No change | Determined by LATCH ENABLE [‡] | R32 | Determined by OUTPUT ENABLE | | |
| LATOU | Х | L | Х | A - d-tid -t | Stored data | R32 | Data and the OUTBUT ENABLE | | |
| LATCH | х | н | × | As determined above | New data | R32 | Determined by OUTPUT ENABLE | | |
| OUTPUT | Х | Х | L | A - d-4id -b | Date de la TOU FNARIET | R32 | All L | | |
| ENABLE | × | Х | X H As determined above | Determined by LATCH ENABLE [‡] | R32 | LC1 thru LC32, respectively | | | |

H = high level, L = low level, X = irrelevant, 1 = low-to-high-level transition.

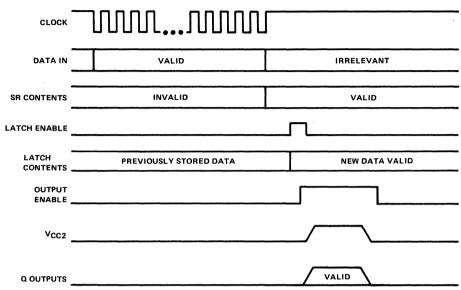


[†]R32 and the serial output take on the state of R31, R31 takes on the state of R30,...R2 takes on the state of R1, and R1 takes on the state of the data input.

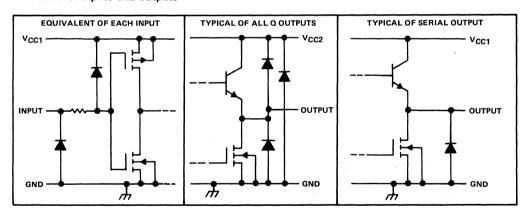
[‡]New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

SN65555, SN65556, SN75555, SN75556 ELECTROLUMINESCENT COLUMN DRIVER

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC1} (see Note 1) |
|---|
| Supply voltage, VCC2 (see Note 2) |
| Input voltage |
| Ground current |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range: SN65555, SN6555640°C to 85°C |
| SN75555, SN75556 0 °C to 70 °C |
| Storage temperature range |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. These devices have been designed to be used in applications in which the high-voltage supply, VCC2, is switched to ground before changing the state of the outputs.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| FN | 1700 mW | 13.6 mW/°C | 1088 mW | 884 mW |
| N | 1250 mW | 10.0 mW/°C | 800 mW | 650 mW |

recommended operating conditions

| | | | | MIN | NOM | MAX | UNIT |
|--|--------------------------|--|---------------------------|-------------------|-----|-------|------|
| V _{CC1} | Supply voltage | ř. | 10.8 | 12 | 15 | V | |
| V _{CC2} | Supply voltage | | | 0 | | 80 | V |
| VIH | High-level input voltage | go (noo Figure 1) | V _{CC1} = 10.8 V | 8.1 | | 11.1 | V |
| VIH. | | ge (see Figure 1) | V _{CC1} = 15 V | 11.25 | | 15.3 | L |
| V. Lauriania in the control in the c | no (soo Eiguro 1) | V _{CC1} = 10.8 V | -0.3 [†] | | 2.7 | V | |
| VIL | Low-level input voltag | ge (see Figure 1) | V _{CC1} = 15 V | -0.3 [†] | | 3.75 | |
| ЮН | High-level output curr | ent | | | | - 15 | mA |
| lOL | Low-level output current | | | | | 15 | mA |
| lok | Output clamp current | | | | | 20 | mA |
| fclock | Clock frequency | | | 0 | | 6.25 | MHz |
| tw(CLK) | Pulse duration, CLOC | ration, CLOCK high or low (see Figure 2) | | | | | ns |
| tw(LE) | Pulse duration, LATCI | H ENABLE . | | 80 | | | ns |
| | Setup time | DATA IN before CLOCK1 (see | Figure 2) | 20 | | | |
| t _{su} | Setup time | OUTPUT ENABLE before VCC | 2↑ (see Figure 4) | 500 | | | ns |
| +. | Hold time | DATA IN after CLOCK1 (see F | igure 2) | 80 | | | ns |
| th | Hold time | OUTPUT ENABLE after VCC2 | 100 | | | l iis | |
| dv/dt | Rate of rise for VCC2 | | | | 80 | V/μs | |
| T . | Onesetine free six tons | | SN65555, SN65556 | -40 | | 85 | °C |
| TA | Operating free-air tem | iperature | SN75555, SN75556 | 0 | | 70 |] - |

[†]The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended operating free-air temperature range, $V_{CC1} = 12 \text{ V}$, $V_{CC2} = 80 \text{ V}$

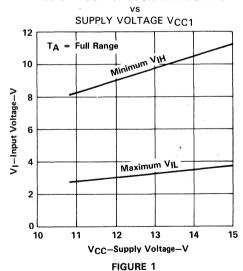
| | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT | |
|----------|--------------------------------------|------------|--------------------------|------|-----|------|--|
| V | High lavel autout valence | Q outputs | I _O = -15 mA | 77 | | V | |
| VOH | High-level output voltage | SERIAL OUT | $I_O = -100 \mu A$ | 10.5 | |) | |
| `` | Lavida al autorita caltaga | Q outputs | I _{OL} = 15 mA | | 8 | 8 V | |
| v_{OL} | Low-level output voltage | SERIAL OUT | I _{OL} = 100 μA | | 1 | | |
| ΊΗ | High-level input current | | V _I = 12 V | | 1 | μΑ | |
| IIL. | Low-level input current | | V ₁ = 0 | | - 1 | μΑ | |
| ICC1 | Supply current from V _{CC1} | | | | 2 | mA | |
| ICC2 | Supply current from VCC2 | | | | 5 | mA | |

switching characteristics, VCC1 = 12 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------|---|---|-----|-------|------|
| tou | Propagation delay time, high-to-low-level | | 140 | | ns |
| tPHL | SERIAL OUT from CLOCK | $C_L = 20 \text{ pF to ground, } V_{CC2} = 0,$ See Figure 3 | | | 113 |
| + | Propagation delay time, low-to-high-level | | | 140 | ns |
| tPLH | SERIAL OUT from CLOCK | | | 140 | 118 |
| td | Delay time, V _{CC2} to Q outputs | dv/dt = 80 V/μs, See Figure 4 | | . 100 | ns |

RECOMMENDED OPERATION CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS



PARAMETER MEASUREMENT INFORMATION

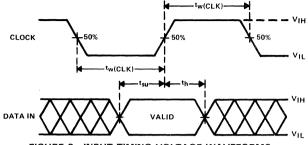


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

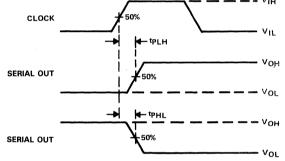


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

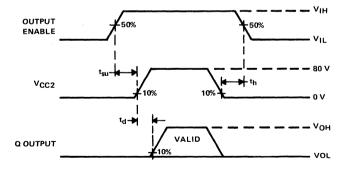


FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, VCC2 TO Q OUTPUTS

SN65557, SN65558, SN75557, SN75558 **ELECTROLUMINESCENT ROW DRIVERS**

D2999, DECEMBER 1985-REVISED OCTOBER 1989

- Each Device Drives 32 Electrodes
- High-Voltage Open-Collector N-P-N Outputs Using Ramped Supply
- 300-mA Output Current Capability
- **CMOS-Compatible Inputs**
- Very Low Steady-State Power Consumption

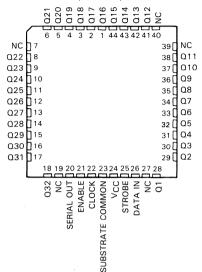
description

These devices are monolithic BIDFET[†] integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are highvoltage open-collector n-p-n transistors. The SN65558 and SN75558 output sequences are reversed from the SN65557 and SN75557 for ease in printed circuit board layout.

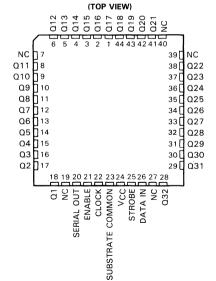
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the SUBSTRATE COMMON terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The Serial Data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65557 and SN65558 are characterized for operation from -40°C to 85°C. The SN75557 and SN75558 are characterized for operation from 0°C to 70°C.

SN65557, SN75557 . . . FN PACKAGE (TOP VIEW)



SN65558, SN75558 . . . FN PACKAGE



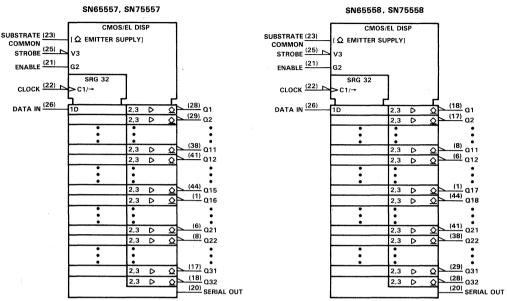
NC-No internal connection

 † BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip - patented process



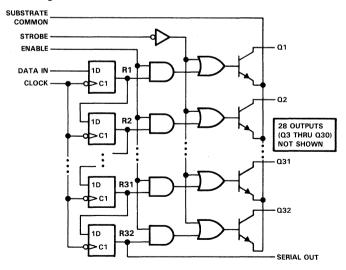
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logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

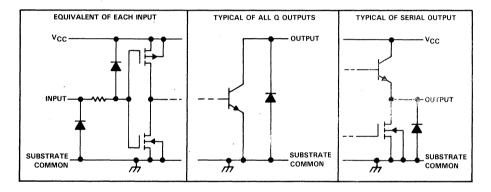


FUNCTION TABLE

| FUNCTION | CONTROL INPUTS | | | SHIFT REGISTERS | | OUTPUTS ` |
|----------|----------------|--------|--------|-----------------------------|--------|---------------------------------|
| FUNCTION | CLOCK | ENABLE | STROBE | R1 THRU R32 | SERIAL | Q1 THRU Q32 |
| LOAD | 1 | . X | Х | Load and Shift [†] | R32 | Determined by ENABLE and STROBE |
| LUAD | No ↓ | x | × | No Change | R32 | Determined by ENABLE and STROBE |
| ENABLE | Х | L | Н | As determined above | R32 | All Q outputs off |
| ENABLE | х | Н | н | As determined above | R32 | Determined by R1 through R32 |
| STROBE | Х | Х | L | As determined above | R32 | All Q outputs on |

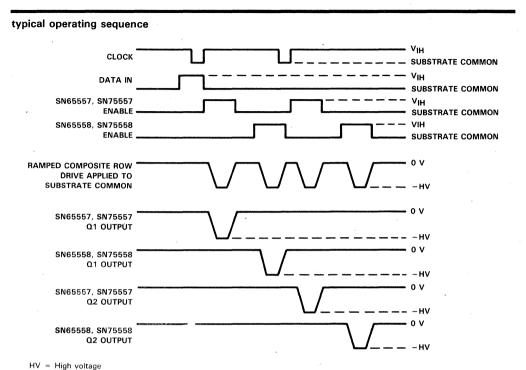
H = high level, L = low level, X = irrelevant, $\downarrow = high-to-low transition$.

schematics of inputs and outputs



[†]Register R32 takes on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

SN65557, SN65558, SN75557, SN75558 ELECTROLUMINESCENT ROW DRIVERS





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) |
|--|
| Off-state output voltage, VO(off) (see Note 2) |
| Input voltage |
| Substrate common terminal current (see Note 3) |
| Continuous total power dissipation at (or below) |
| 25°C free-air temperature (see Note 4) |
| Operating free-air temperature range: SN65557, SN6555840°C to 85°C |
| SN75557, SN75558 0 °C to 70 °C |
| Storage temperature range |
| Case temperature for 10 seconds |

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON terminal.

- Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to -HV (see typical operating sequence).
- 3. Duty cycle is limited by package dissipation.
- 4. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

| | | | MIN | NOM | MAX | UNIT | |
|---|---|--------------------------|-------|-----|------|------|--|
| Supply voltage, V | cc | | 10.8 | 12 | 15 | V | |
| High lavel innut v | oltogo V., (oco Figure 1) | V _{CC} = 10.8 V | 8.1 | | 11.1 | | |
| High-level input voltage, VIH (see Figure 1) | | V _{CC} = 15 V | 11.25 | | 15.3 |) v | |
| Low lovel input w | oltogo V., Jose Figure 1) | V _{CC} = 10.8 V | -0.3 | | 2.7 | V | |
| Low-level input voltage, V _{IL} (see Figure 1) | | V _{CC} = 15 V | -0.3 | | 3.75 | V | |
| Off-state Q output | t voltage, V _{O(off)} | -0.3 | | 100 | V | | |
| On-state Q output | t current, $I_{O(on)}$, duty cycle $\leq 1\%$ | , V _{CC} = 15 V | | | 300 | mA | |
| Rate of rise for SI | igure 4) | | | 100 | V/μs | | |
| Clock frequency, | f _{clock} | | 0 | | 4 | MHz | |
| Pulse duration, Cl | OCK high or low, t _w | | 125 | | | ns | |
| C-4 4: 4 | DATA IN before CLOCK↓ (see Fig | ure 2) | 50 | | | | |
| Setup time, t _{su} | ENABLE before SUBSTRATE COMMON ↓ (see Figure 4) | | 500 | | | ns | |
| Hold time, th, DA | 100 | | | ns | | | |
| O | 4 | SN65557, SN65558 | -40 | | 85 | 1 00 | |
| Operating free-air temperature, TA | | SN75557, SN75558 | 0 | | 70 | 1 °℃ | |

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | SN65557 SN65558 | | SN75557 SN75558 | | UNIT | |
|---------|-------------------------------------|------------------------|--------------------------|------|--------------------|------|------|----|
| | | CONDITIONS | MIN | MAX | MIN | MAX | | |
| IO(off) | Off-state Q output current | V _O = 100 V | | 20 | | 10 | μΑ | |
| Vон | High-level output voltage | Serial outputs | $I_0 = -100 \mu A$ | 10.5 | | 10.5 | | ٧ |
| V | Low-level output voltage | Q outputs | I _{OL} = 300 mA | | 20 | | 10 | V |
| VVOL | | Serial output | I _{OL} = 100 μA | | 1 | | 1 | |
| ΊΗ | High-level input current | V _I = 12 V | | 1 | | 1 | μΑ | |
| IL | Low-level input current | V ₁ = 0 | T T | - 1 | | -1 | μΑ | |
| lcc | Supply current from V _{CC} | | | | 250 | | 250 | μΑ |

SN65557, SN65558, SN75557, SN75558 ELECTROLUMINESCENT ROW DRIVERS

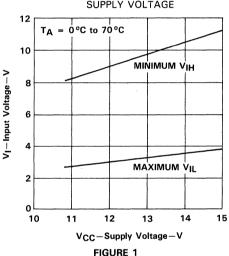
switching characteristics, VCC = 12 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|--|---|-----|-----|------|
| tPHL | Propagation delay time, high-to-low- level SERIAL OUTPUT from CLOCK | C _L = 20 pF to SUBSTRATE COMMON | | 200 | ns |
| tPLH | Propagation delay time, low-to-high- level SERIAL OUTPUT from CLOCK | (see Figure 3) | | 200 | ns |
| ^t d(on) | Turn-on delay time, Q outputs from ENABLE | $dV/dt = 100 V/μs$, STROBE at V_{CC} , $R_L = 2 kΩ$ to 60 V (see Figure 4) | | 500 | ns |

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS

SUPPLY VOLTAGE



PARAMETER MEASUREMENT INFORMATION

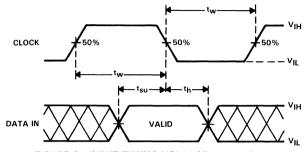


FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

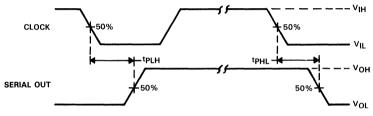


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

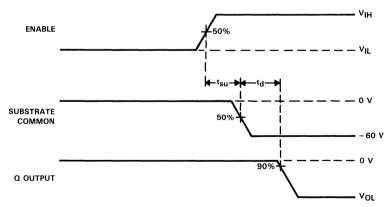
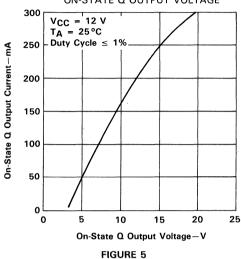


FIGURE 4. VOLTAGE WAVEFORMS FOR TURN ON DELAY TIME, SUBSTRATE COMMON TO Q OUTPUT

TYPICAL CHARACTERISTICS

ON-STATE Q OUTPUT CURRENT ON-STATE Q OUTPUT VOLTAGE



D3223, MAY 1986-REVISED DECEMBER 1989

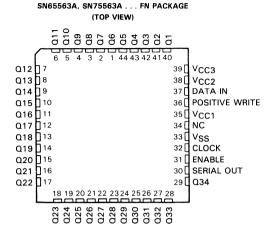
- Each Device Drives 34 Electrodes
- Selectable Open-Source or Open-Drain Output
- Outputs Rated at 240 V
- Output Current Capability:
 - 150 mA to 100 mA (SN65')
 - 150 mA to 120 mA (SN75')
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

description

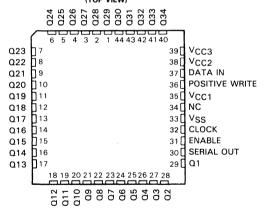
The SN65563A, SN65564A, SN75563A, and SN75564A are monolithic BIDFET[†] integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN65564A and SN75564A output sequences are reversed from the SN65563A and SN75563A for ease in printed circuit board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN65563A and SN65564A are characterized for operation over the full automotive operating temperature range of -40°C to 85°C. The SN75563A and SN75564A are characterized for operation from 0°C to 70°C.



SN65564A, SN75564A . . . FN PACKAGE (TOP VIEW)



NC-No internal connection

[†]BIDFET-Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — Patented Process



LOAD FUNCTION TABLE

| | C | ONTROL IN | PUTS | SHIFT REGISTER | OUTPUTS | | |
|----------|-------|-----------|-------------------|-----------------------------|---------|---|--|
| FUNCTION | сгоск | ENABLE | POSITIVE WRITE | R1 THRU R34 | SERIAL | Q1 THRU Q34 | |
| LOAD | + | Х | X. | Load and Shift [†] | R34 | Determined by ENABLE and POSITIVE WRITE | |
| LUAD | No↓ | X | X | No Change | R34 | Determined by ENABLE and POSITIVE WRITE | |

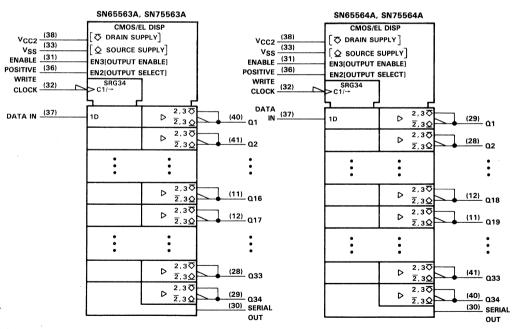
[†]Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

| | CONTROL INPUTS | | | SHIFT REGISTER CONTENTS Rn FOR | OUTPUTS | | |
|----------|----------------|--------|-------------------|-----------------------------------|---------|----------------|--|
| FUNCTION | СГОСК | ENABLE | POSITIVE WRITE | R1 THRU R34 (Determined Above) | SERIAL | Q1 THRU Q34 | |
| | X | L | Х | Х | R34 | High-Impedance | |
| OUTPUT | × | н | н | н | R34 | н | |
| CONTROL | x | н | L | н | R34 | L | |
| | х | Х | Х | L | R34 | High-Impedance | |

H = high, L = low, X = irrelevant, ↓ = high-to-low transition

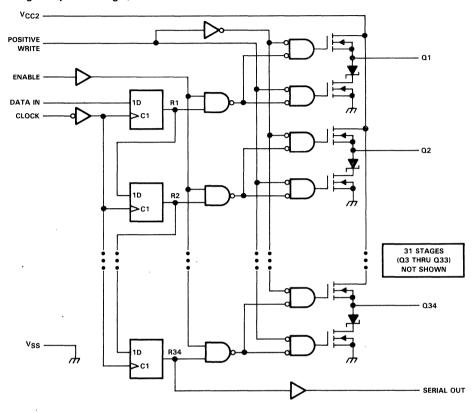
schematics of inputs and outputs



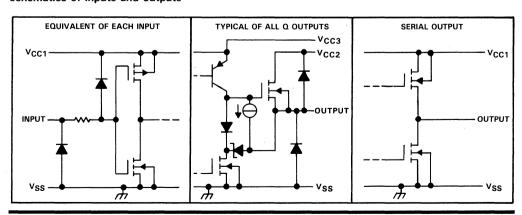
[‡]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



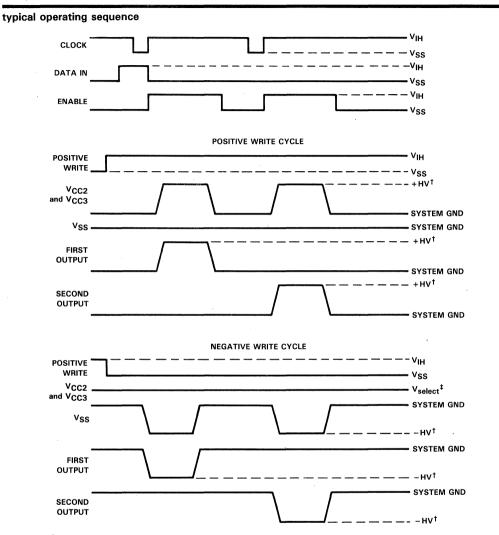
logic diagram (positive logic)



schematics of inputs and outputs







 $^{^{\}bar{1}}HV=$ high voltage $^{\ddagger}During$ the negative write cycle, the VCC2 and VCC3 supplies are in a high-impedance state.

absolute maximum ratings over operating free-air temperture range (unless otherwise noted)

| Supply voltage, VCC1 (see Note 1) 15 V Supply voltage, VCC2 240 V |
|---|
| Supply voltage, VCC3 240 V Supply voltage, VSS -240 V |
| Input voltage |
| Continuous total power dissipation at (or below) 25 °C free-air temperature |
| (see Note 2) |
| Operating free-air temperature range: SN65563A, SN65564A |
| SN75563A, SN75564A 0°C to 70°C |
| Storage temperature range40°C to 125°C |
| Case temperature for 10 seconds |

NOTES: 1. Voltage values are with respect to VSS.

2. For operation above 25 °C free-air temperature, derate to 1088 mW at 70 °C or 884 mW at 85 °C at the rate of 13.6 mW/ °C.

recommended operating conditions (see Note 1, Figure 1, and Figure 2)

| | | MIN | NOM | MAX | UNIT | |
|---|--|------------------------|------|-----------------------|------|--|
| Supply voltage, V _{CC1} | 7.5 | 12 | 13.2 | V | | |
| Supply voltage, V _{CC2} | | VCC3 - 15 | | V _{CC3} | V | |
| Supply voltage, V _{CC3} | | 0 | | 235 | ٧ | |
| Supply voltage, VSS | | 0 | | - 235 | V | |
| High-level input voltage, VIH | | 0.75V _{CC1} | | V _{CC1} +0.3 | V | |
| Low-level input voltage, V _{IL} † | | -0.3 | | 0.25V _{CC1} | ٧ | |
| High-level output current, IOH | SN65563A, SN65564A | | | 100 | m A | |
| nigh-level output current, IOH | SN75563A, SN75564A | | | - 120 | mA | |
| Low-level output current, IOL | | | | 150 | mA | |
| Output clamp current, IOK | | | | ± 150 | mA | |
| Clock frequency, f _{clock} | | | | 4 | MHz | |
| Pulse duration, CLOCK high or low, t | wCLK | 125 | | | ns | |
| Setup time, DATA IN high or low bef | ore CLOCK↓, t _{su1} | 100- | | | ns | |
| Setup time, CLOCK low before VCC2 | ∱ or V _{SS} ∮, t _{su2} | 300 | | | ns | |
| Setup time, ENABLE high before VCC | 2 [↑] or V _{SS} ↓, t _{su3} | 300 | | | ns | |
| Setup time, POSITIVE WRITE high or | low before V _{CC2} † or V _{SS} ↓, t _{su4} | 300 | | | ns | |
| Hold time, DATA IN high or low after | CLOCK↓, th1 | 100 | | | ns | |
| Hold time, CLOCK high after V _{CC2} ↓ of | or VSS [†] , th2 | 300 | | | ns | |
| Hold time, ENABLE high after VCC2↓ | | 0 | | | ns | |
| Hold time, POSITIVE WRITE after VC | C2 [↓] or VSS [↑] , th4 | 0 | | | ns | |
| Hold time, ENABLE low between | SN65563A, SN65564A | 12 | | | _ | |
| successive V _{CC2} [↑] , t _{h5} SN75563A, SN75564A | | 10 | | | μS | |
| Hold time, ENABLE low between such | 300 | | | ns | | |
| Operating free six temperature T. | SN65563A, SN65564A | SN65563A, SN65564A -40 | | 85 | °C | |
| Operating free-air temperature, TA | SN75563A, SN75564A | 0 | | 70 | 1 30 | |

[†]The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, $V_{CC2} = 235 \text{ V}$, $V_{CC3} = 235 \text{ V}$, $V_{SS} = 0$ (unless otherwise noted)

| | PARAMETER | ł | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------------------------|--------------------------------------|------------|--|-----------------------|-------|------|
| IO(off) Off-state Q output current | | ıt ourront | V _O = 235 V | | 50 | μΑ |
| lO(off) | On-state & outpo | it current | $V_0 = 0$ | | - 50 | μΑ |
| V | High-level | Q outputs | $I_0 = -70 \text{ mA}$ | V _{CC2} - 30 | | V |
| ∨он | output voltage | SERIAL OUT | $I_{O} = -100 \mu\text{A}, V_{CC1} = 12 \text{V}$ | 10.5 | | V |
| Vai | Low-level | Q outputs | I _O = 150 mA | | 30 | V |
| VOL | output voltage | SERIAL OUT | I _O = 100 μA | | 1 | V |
| ΊΗ | High-level input o | urrent | V _{IH} = V _{CC1} | | 100 | μΑ |
| Ιμ | Low-level input c | urrent | V _{IL} = 0 | | - 100 | μΑ |
| lane | Supply current from V _{CC1} | | One Q output high | | 4 | mA |
| ICC1 | | | All Q outputs low or high impedance | | 2 | ША |
| lana | Supply current from | om Voca | One Q output high | | 10 | mA |
| _I CC3 | Supply Current In | om ACC3 | All Q outputs low or high impedance | | 200 | μΑ |

switching characteristics operating range of VCC1, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|-------------------------------------|---------------------------------|-----|-----|------|
| + | Propagation delay time, low-to-high | | | 400 | |
| tPLH ie | level serial output from clock | $C_L = 50 \text{ pF to V}_{SS}$ | | 400 | ns |
| | Propagation delay time, high-to-low | See Figures 3 and 4 | | 400 | |
| ^t PHL | level serial output from clock | | | 400 | ns |

PARAMETER MEASUREMENT INFORMATION

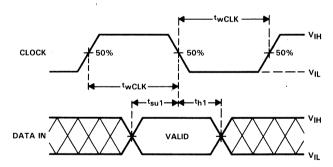
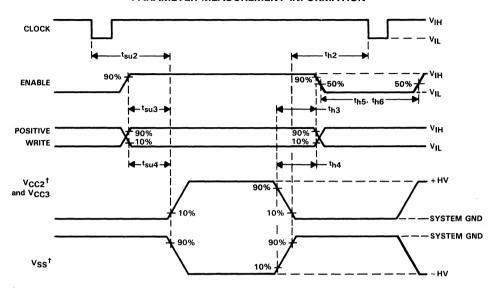


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



 $^{^{\}dagger}\text{Timing}$ waveforms are with respect to VCC2 or VSS, as appropriate.

FIGURE 2. CONTROL INPUT TIMING VOLTAGE WAVEFORMS

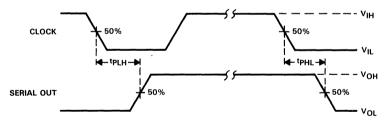


FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, CLOCK TO DATA OUT

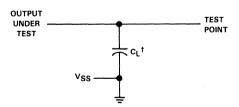


FIGURE 4. LOAD CIRCUIT

[†]C_L includes probe and jig capacitance.



SN751506, SN751516 DC PLASMA DISPLAY DRIVERS

D3005, DECEMBER 1986-REVISED JULY 1989

SN751506 . . . FT PACKAGE (TOP VIEW)

- Each Device Drives 32 Lines
- 180-V Open-Drain Parallel Outputs
- 220-mA Parallel Output Sink Current Capability
- CMOS-Compatible Inputs
- Strobe Input Provided
- Serial Data Output for Cascade Operation
- Inputs Have Built-in Electrostatic Discharge Protection

description

The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed circuit board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off-state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0 °C to 70 °C.

| Q32 | 38 Q11 2 37 Q12 3 36 Q13 4 35 Q14 5 33 Q16 7 32 QNC 3 1 QND |
|--|---|
| NC 20 | 29 STROBE |
| CLOCK 22 | |
| NC 🗖 23 | 3 26 🗖 NC |
| SERIAL OUT 2 | DATA IN |
| SN751516 . | FT PACKAGE |
| | VIEW) |
| 01 | 48 Q 032 47 Q 031 046 Q 030 |
| Q4 🔲 4 Q5 🔲 5 | 45 Q29 44 Q28 |
| Q6 ☐ 6 | 43 🖸 027 |
| Ω7 □ 7 Ω8 □ 8 | 42 026 41 025 |
| 09 🗖 9 | 40 024 |
| 010 🗖 10 | E |
| Q11 [] 1 ¹ Q12 [] 1 ² | E |
| 013 1 | |
| 014 🗖 14 | 1 35 O19 |

NC-No internal connection

DATA IN 24

Q15 🗖 15

Q16 🗖 16

NC 17

NC 19 STROBE 20

NC 721

VCC 22 NC 23

GND [] 18

Texas Instruments

34 018

33 017

31 GND 30 NC

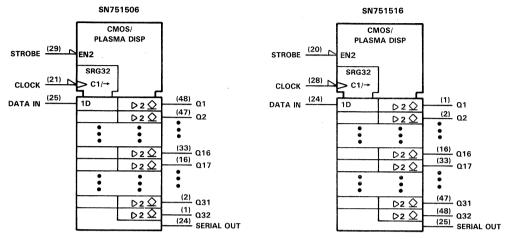
32 NC

29 NC

26 NC 25 SERIAL OUT

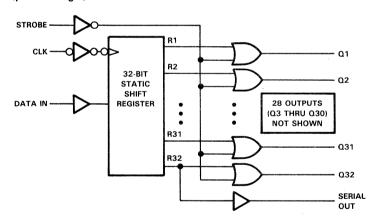
28 CLOCK

logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

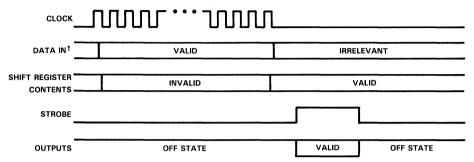
| FUNCTION | CONTROL INPUTS | | SHIFT REGISTERS | OUTPUTS | | |
|----------|----------------|---------------------|-----------------------------|--------------------|----------------------|--|
| PUNCTION | CLOCK | STROBE | R1 THRU R32 | SERIAL | Q1 THRU Q32 | |
| LOAD | ↓ | Х | Load and shift [‡] | R32 | Determined by STROBE | |
| LUAD | No↓ | X | No change | R32 | Determined by STROBE | |
| CTROPE | X L | As determined above | R32 | All high impedance | | |
| STROBE | Х | Н | As determined above | R32 | R1 thru R32 | |

 $H = high level, L = low level, X = irrelevant, \downarrow = high to low transition.$

[‡] R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

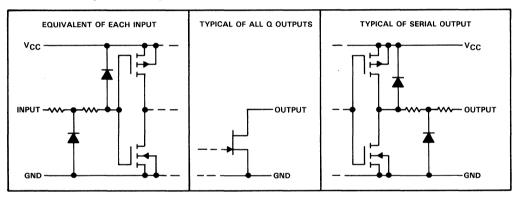


typical operating sequence



[†]Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| - · · · · · · · · · · · · · · · · · · · |
|---|
| Supply voltage, VCC (see Note 1)0.4 V to 7 V |
| On-state Q output voltage, Vo0.4 V to 125 V |
| Off-state Q output voltage, VO0.4 V to 180 V |
| Input voltage |
| Serial output voltage |
| Q output on-state time duration (see Note 2) |
| Q output duty cycle (see Note 2) |
| Continuous total power dissipation at (or below) 25 °C free-air |
| temperature (see Note 3) |
| Operating free-air temperature range, TA |
| Storage temperature range – 55 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

- NOTES: 1. Voltage values are with respect to GND.
 - 2. Only one Q output should be on at a time.
 - 3. For operation above 25 °C free-air temperature, derate linearly to 656 mW at 70 °C at the rate of 8.2 mW/°C.

SN751506, SN751516 DC PLASMA DISPLAY DRIVERS

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-----------------------|------------------|-----|-----|------|
| Supply voltage, V _{CC} | | 4 | 5 | 6 | ٧ |
| Peak on-state Q output voltag | e, V _{O(on)} | | | 110 | V |
| High-level input voltage, VIH | $V_{CC} = 4 V$ | 3.2 | | | V |
| | V _{CC} = 6 V | 4.8 | | | |
| Low-level input voltage, VII | $V_{CC} = 4 V$ | | | 0.8 | V |
| Low-level input voltage, v L | $V_{CC} = 6 V$ | | | 1.2 | · · |
| Output current, IO (TA = 25°C) | | | | 220 | mA |
| Clock frequency, f _{clock} | | | | 200 | kHz |
| Pulse duration, CLOCK high or low, twCLK | | 1.5 [†] | | | μS |
| Pulse duration, DATA, t _{WD} | | 5 | | | μs |
| Pulse duration, STROBE, twSTRB | | 2 | | | μs |
| Setup time, DATA IN before CLOCK↓, t _{SU} | | 1 | | | μS |
| Hold time, DATA IN after CLOCKI, th 1.2 | | | μs | | |
| Operating free-air temperature, T _A | | 0 | | 70 | °C |

 $^{^{\}dagger}$ The minimum clock period is 5 μs .

electrical characteristics, VCC = 5 V, TA = 25 °C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|---------------------------|------------|--------------------------|-----|-----|-----|------|
| Vон | High-level output voltage | SERIAL OUT | IOH = −0.1 mA | 4.5 | | | V |
| VOL | Low-level output voltage | Q outputs | I _{OL} = 180 mA | | 6 | 10 | V |
| | | SERIAL OUT | I _{OL} = 0.1 mA | | | 0.5 | · · |
| IO(off) | Off-state output current | Q outputs | V _{OH} = 110 V | | | 1 | μΑ |
| lOL | Low-level output current | Q outputs | V _{OL} = 16 V | 220 | | | mA |
| lн | High-level input current | | $V_I = V_{CC}$ | | | 1 | μΑ |
| IIL Low-level input current | | | V _I = 0 | | | - 1 | μΑ |
| Ci | Input capacitance | | | | | 15 | pF |
| Icc | Summit and | | All Q outputs off | | | 1 | ^ |
| | Supply current | | One Q output on | | 20 | 40 | , mA |

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-----|-------|-----|------|
| t _{pd} | Propagation delay time, CLOCK to SERIAL OUT | C _L = 15 pF | | 0.2 | 0.5 | μs |
| †DHL | Delay time, high-to-low-level Q output from STROBE or CLOCK inputs | C _I = 150 pF, | | 0.2‡ | 0.6 | μS |
| tDLH | Delay time, low-to-high-level Q output from STROBE or CLOCK inputs | $C_L = 150 \text{pr},$ $R_1 = 470 \Omega,$ | | 0.35‡ | 1 | μs |
| tTHL | Transition time, high-to-low-level Q output | See Figures 2 and 3 | | 0.1 | 0.3 | μS |
| tTLH | Transition time, low-to-high-level Q output | 3ee rigules 2 and 3 | | 0.35 | 1 | μS |

[‡] Typical values are for clock inputs. Typical from strobe inputs will be less.

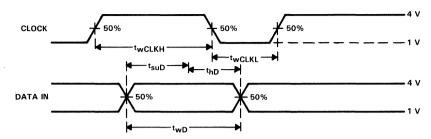


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

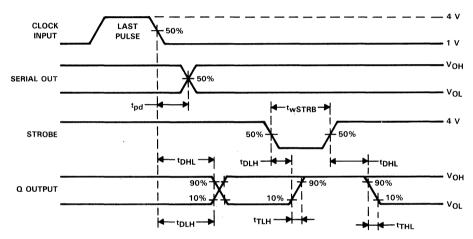
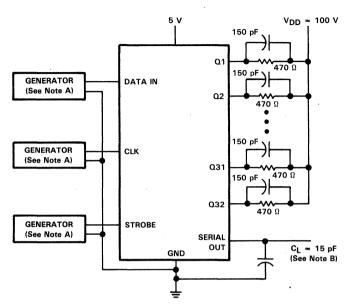


FIGURE 2. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

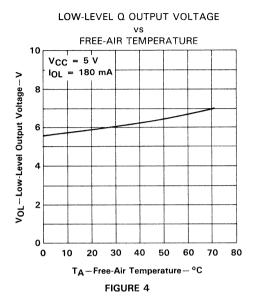


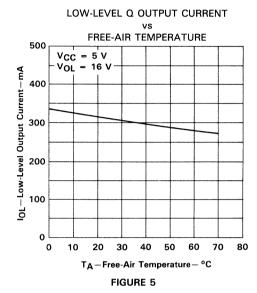
NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_W = 1.25~\mu s$, PRR $\leq 200~kHz$, $t_f \leq 30~ns$, $t_f \leq 30~ns$, $Z_0 = 50~\Omega$.

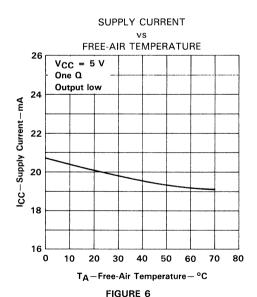
B. C_L includes probe and jig capacitance.

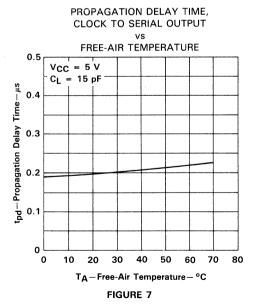
FIGURE 3. TEST CIRCUIT

TYPICAL CHARACTERISTICS

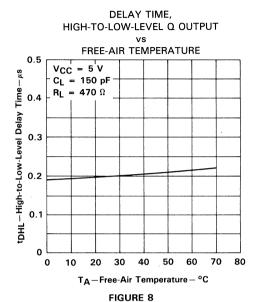








TYPICAL CHARACTERISTICS



LOW-TO-HIGH-LEVEL Q OUTPUT FREE-AIR TEMPERATURE 0.5 VCC = 5 V :DLH-Low-to-High-Level Delay Time-µs $C_L = 150 pF$ $R_L = 470 \Omega$ 0.4 0.3 0.2 0.1 0 30 40 50 60 70 . 0 10 20 TA-Free-Air Temperature-°C FIGURE 9

DELAY TIME,

TRANSITION TIME, HIGH-TO-LOW-LEVEL Q OUTPUT

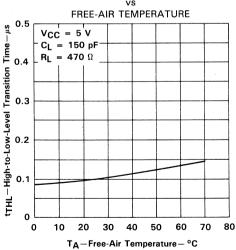


FIGURE 10

TRANSITION TIME, LOW-TO-HIGH-LEVEL Q OUTPUT VS

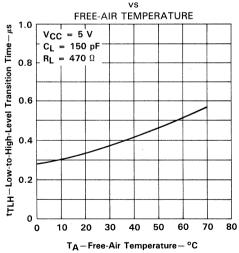


FIGURE 11

D2984, JANUARY 1987-REVISED NOVEMBER 1989

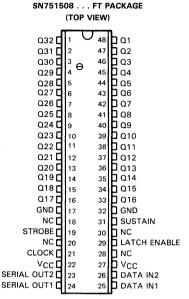
- Each Device Drives 32 Lines
- 120-V P-N-P Open-Collector Parallel Outputs
- High-Speed Serially Shifted Data Inputs
- CMOS-Compatible Inputs
- Strobe and Sustain Inputs Provided
- Serial Data Output for Cascade Operation

description

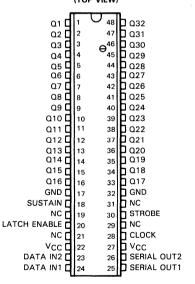
The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed circuit board layout.

Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 P-N-P open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal, A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high will be placed on the data input of the output AND gates. When STROBE is low, and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN will force all outputs to their off state. Drivers may be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.



SN751518 . . . FT PACKAGE (TOP VIEW)

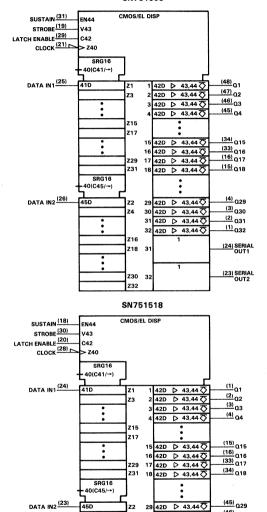


NC-No internal connection



logic symbols†

SN751508



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Z16 Z18 31

Z30 32 Z32 (46) Q30

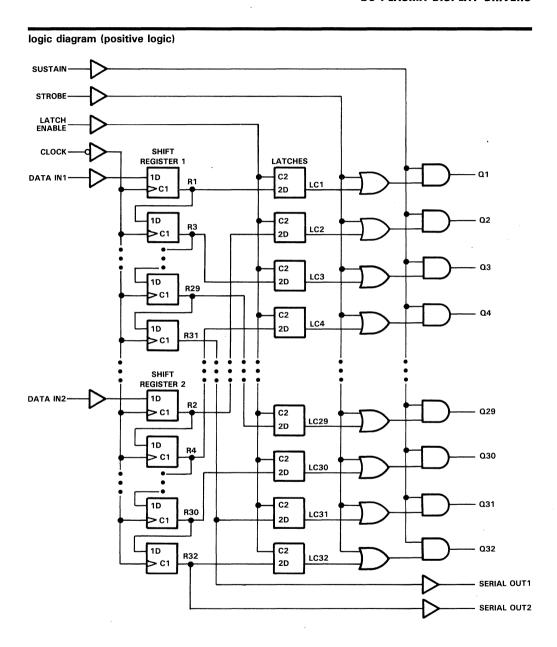
(<u>47)</u> Q31

(48) Q32

30 42D ▷ 43,44 ♦

31 42D ▷ 43,44 ♦

32 42D ▷ 43,44 ♡



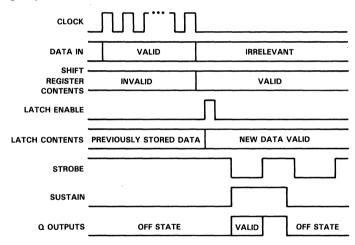


SN751508, SN751518 DC PLASMA DISPLAY DRIVERS

| | | CONTRO | L INPUTS | | SHIFT REGISTERS | LATCHES | OUTPUTS | | | |
|----------|-------|--------------|----------|----------------|------------------|---------------------------|---------|-----|--------------------|--|
| FUNCTION | сьоск | LATCH OTDORE | | STROBE SUSTAIN | R1 THRU R32 | LC1 THRU LC32 | SERIAL | | Q1 THRU Q32 | |
| | CLUCK | ENABLE | STRUBE | SUSTAIN | III IIIIO IIGZ | LCT THRU LC32 | S01 | S02 | u i inno usz | |
| LOAD | 4 | Х | Х | Х | Load and shift † | Determined by | R31 | R32 | Determined by | |
| LUAD | No↓ | Х | X | Х | No change | LATCH ENABLE‡ | noı | noz | SUSTAIN and STROBE | |
| LATCH | Х | L | Х | Х | As determined | Stored data | R31 | R32 | Determined by | |
| ENABLE | X | н | Х | Х | above | New data | noı | noz | SUSTAIN and STROBE | |
| STROBE | Х | Х | L | Н | As determined | Determined by | R31 | R32 | LC1 thru LC32 | |
| SINOBE | х | Х | Н | Н | above | LATCH ENABLE [‡] | noi | noz | All on (high) | |
| SUSTAIN | х | Х | х | | As determined | Determined by | R31 | R32 | All off | |
| SUSTAIN | ^ | ^ ^ | | _ | above | LATCH ENABLE‡ | n31 | n32 | All Oli | |

H = high level, L = low level, X = irrelevant, \downarrow = high-to-low transition

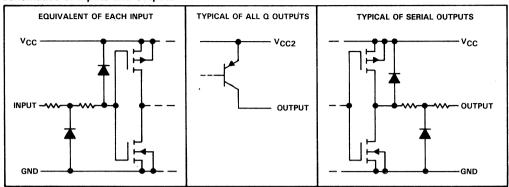
typical operating sequence



[†] Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, . . . R4 takes on the state of R2, R2 takes on the state of R29, R29 takes on the state of R27, . . . R3 takes on the state of R1, and R1 takes on the state of R27, . . . R3 takes on the state of R3, and R1 takes on the state of R3, and R1 takes on the state of R3, and R1 takes on the state of R3, and R1 takes on the state of R3, and R1 takes on the state of R3, and R3 takes on

^{*}New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) −0.4 to 7 V On-state Q output voltage, V _Q −120 V to V _{CC} +0.4 V |
|---|
| |
| Input voltage |
| Serial output voltage |
| Continuous total power dissipation at (or below) 25 °C free-air temperature |
| (see Note 2) |
| Operating free-air temperature range, TA |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. Voltages values are with respect to GND.

2. For operation above 25 °C free-air temperature, derate linearly to 656 mW at 70 °C at the rate of 8.2 mW/°C.

SN751508, SN751518 DC PLASMA DISPLAY DRIVERS

recommended operating conditions

| | | ************************************** | MIN | NOM | MAX | UNIT | | |
|---|--------------------------------|--|-------|---|------|------|--|--|
| Supply voltage, VCC | | | 4.5 | 5 | 5.5 | V | | |
| Output voltage, VO | | | | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, | - 75 | V | | |
| High-level input voltage, VIH | | V _{CC} = 4.5 \ | / 3.6 | | | v | | |
| High-level input voltage, VIH | | V _{CC} = 5.5 \ | / 4.4 | | | ı v | | |
| Low-level input voltage, VII | | $V_{CC} = 4.5$ | / | | 0.9 | V | | |
| Low-level input voltage, VIL | | $V_{CC} = 5.5$ | / | | 1 | | | |
| Output current, IO (TA = 25°C) | | | | | | mA | | |
| Clock frequency, f _{clock} | | | | | 5 | MHz | | |
| | CLOCK | | 75 | | | | | |
| | DATA IN | | | | | ns | | |
| Pulse duration, tw (see Figure 1) | LATCH ENABLE | | | | | | | |
| Pulse duration, t _W (see Figure 1) | STROBE | STROBE | | | | 0 | | |
| | SUSTAIN | | 2 | | | μS | | |
| | DATA IN before CLOCK↓ | | 20 | | | | | |
| | CLOCK low before LATCH ENABLE | ≣↑ | 50 | | | ns | | |
| Setup time, t _{SU} (see Figure 1) | LATCH ENABLE low before CLOCK | (↓ | 0 | | | | | |
| | LATCH ENABLE high before STRO | LATCH ENABLE high before STROBE↓ | | | | | | |
| | LATCH ENABLE high before SUST. | AIN† | 0 | | | 1 | | |
| Hold time, DATA IN after CLOCK↓, t _↑ | (see Figure 1) | | 50 | | | μS | | |
| Operating free-air temperature, TA | | | 0 | | 70 | °C | | |

electrical characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 0 \,^{\circ}\text{C}$ to $70 \,^{\circ}\text{C}$ (unless otherwise noted)

| | PARAMETER | | TEST CO | NDITIONS | MIN | TYP [†] | MAX | UNIT | |
|-----|-----------------------------|-----------|---|--------------------------|----------------------|------------------|------|------|--|
| | | Q outputs | $I_{OH} = -0.5 \text{ mA}$ | | 4 | 4.5 | | | |
| | | | V F F V | $I_{OH} = -100 \mu A$ | 4.3 | 4.6 | | | |
| νон | High-level output voltage | Serial | $V_{CC} = 5.5 V$ | $I_{OH} = -20 \mu A$ | 4.4 | | | V | |
| | | Outputs | V _{CC} = 4.5 V | $I_{OH} = -100 \mu A$ | 3.4 | 3.6 | | | |
| | | | | $I_{OH} = -20 \mu A$ | 3.6 | | | 1 | |
| | Low-level output voltage | | | V F F V | $I_{OL} = 100 \mu A$ | | 0.9 | 1.2 | |
| | | Serial | $V_{CC} = 5.5 V$ | I _{OL} = 20 μA | | | 1.1 | v | |
| VOL | | Outputs | V _{CC} = 4.5 V | I _{OL} = 100 μA | | 0.9 | 1.1 | | |
| | | | | $I_{OL} = 20 \mu A$ | | | 0.9 | | |
| Іон | High-level Q output current | | T _A = 25°C, | V _O = 3 V | -1.2 | | | mA | |
| loL | Low-level Q output current | | T _A = 25°C, | $V_0 = -75 \text{ V}$ | | | -500 | μΑ | |
| ΊΗ | High-level input current | | T _A = 25°C, | $V_I = V_{CC}$ | | | 1 | μΑ | |
| IL | Low-level input current | | T _A = 25°C, | V ₁ = 0 | | | - 1 | μΑ | |
| | | | All Q outputs high, V _{CC} = 5.5 V | | | 17 | 25 | ^ | |
| Icc | Supply current | | All Q outputs low | | | | 3 | mA | |
| Ci | Input capacitance | | | | | | 15 | pF | |

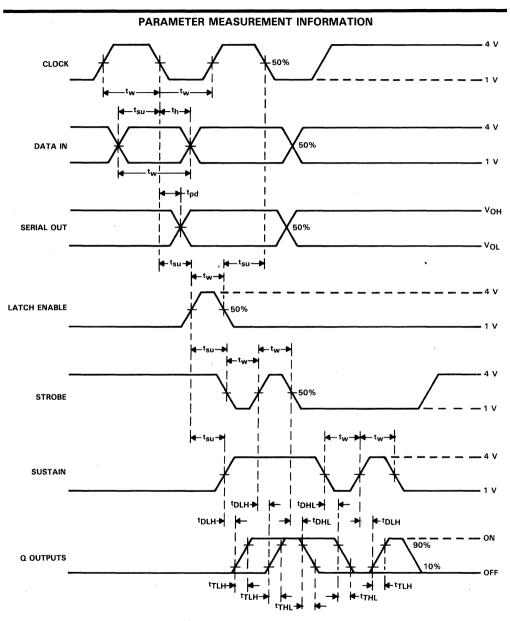
 $^{^{\}dagger}AII$ typical values are at $T_{\mbox{\scriptsize A}}~=~25\,^{\rm o}\mbox{\scriptsize C}.$

switching characteristics $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$ (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|---|--|-----|----------------|-----|------|
| tpd | Propagation delay time, CLOCK to Serial Outputs | C _L = 15 pF | | 100 | 150 | nš |
| tDLH | Delay time, low-to-high-level Q output from SUSTAIN or STROBE | CL = 15 pF, | | 0.3‡ | 1 | μS |
| †DHL | Delay time, high-to-low-level Q output from SUSTAIN or STROBE | $C_L = 15 \text{ pr},$ $R_1 = 91 \text{ k}\Omega,$ | | 1 [‡] | 2.5 | μS |
| tTLH | Transition time, low-to-high-level Q output | See Figures 1 and 2 | | 2 | 5 | μs |
| tTHL | Transition time, high-to-low-level Q output | See Figures 1 and 2 | | 11 | 18 | μS |

[‡]Typical values for delay times are measured from the SUSTAIN input.



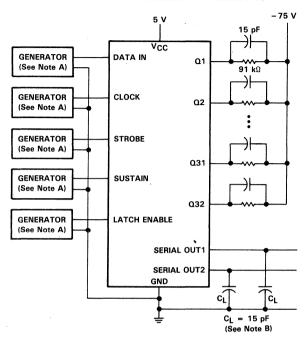


NOTE: Input t_r and t_f are less than or equal to 10 ns.

FIGURE 1. INPUT TIMING AND SWITCHING TIME VOLTAGE WAVEFORMS



PARAMETER MEASUREMENT INFORMATION



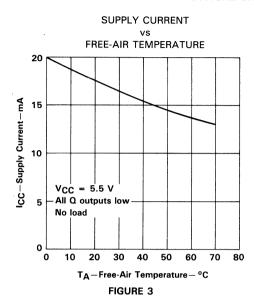
TEST CIRCUIT

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_W = 100 \text{ ns}$, PRR $\leq 5 \text{ MHz}$, $t_r \leq 10 \text{ ns}$, $t_f \, \leq \, 10 \, \, \text{ns, Z}_O \, = \, 50 \, \, \Omega.$

B. CL includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS



DELAY TIME, SUSTAIN INPUT TO Q OUTPUT, LOW TO HIGH

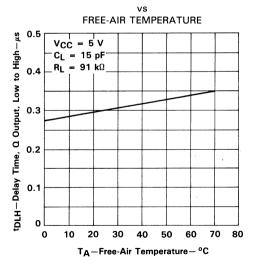
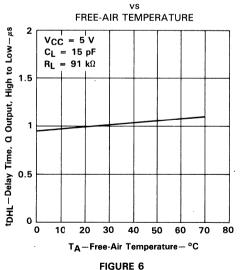


FIGURE 5

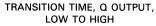
DELAY TIME, CLOCK TO SERIAL OUTPUT VS FREE-AIR TEMPERATURE 125 tpd-Delay Time, Clock to Serial Output-ns 100 75 50 $V_{CC} = 5 V$ 25 $C_L = 15 pF$ 0 0 40 50 70 80 10 20 30 60 TA-Free-Air Temperature-°C

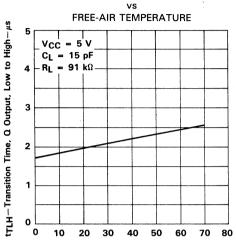
DELAY TIME, SUSTAIN INPUT TO Q OUTPUT, HIGH TO LOW

FIGURE 4



TYPICAL CHARACTERISTICS





TA-Free-Air Temperature - °C FIGURE 7

TRANSITION TIME, Q OUTPUT. HIGH TO LOW

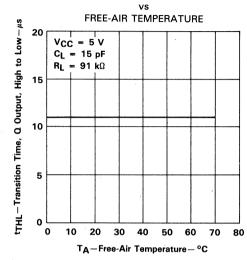


FIGURE 8

TL4810BI, TL4810B VACUUM FLUORESCENT DISPLAY DRIVERS

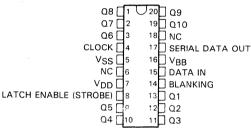
| | D2715, DECEMBER 1984—REVISED OCTOBER 198 |
|--|---|
| Each Device Drives 10 Lines | N PACKAGE |
| 60-V Output Voltage Rating | (TOP VIEW) |
| 40-mA Output Source Current | Q8 |
| High-Speed Serially-Shifted Data Input | Q6 3 16 SERIAL DATA OUT |
| CMOS-Compatible Inputs | CLOCK |
| Latches on All Driver Outputs | VDD 6 13 BLANKING |
| Improved Direct Replacement for UCN4810A and TL4810A | LATCH ENABLE (STROBE) |
| description | |
| The TL4810BI and TL4810B are monolithic BIDFET [†] integrated circuits designed to drive a | DW SMALL OUTLINE PACKAGE (TOP VIEW) |
| dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large | Q8 |

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

display arrays.

Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and 40 mA source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to VDD when driven by TTL logic.

The TL4810BI is characterized for operation from -40°C to 85°C. The TL4810B is characterized for operation from 0°C to 70°C.



NC-No internal connection

[†] BIDFET - Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip - patented process.



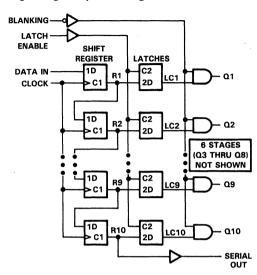
TL4810BI, TL4810B VACUUM FLUORESCENT DISPLAY DRIVERS

logic symbol†

CMOS/ LATCH ENABLE (7) VAC FLUOR BLANKING (13) DISP >C1/→ (12)_Q1 DATA IN (14) 11D 2D Þ (11)2D Þ 3 (10) 2D Þ 3 (9) 2D Þ (8) .05 2D Þ (3) 2D D (2) 07 2D Þ (1) 2D Þ -08 (18) 2D Þ (17)-010 2D D 3 - SERIAL DATA OUT

Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

| | CO | NTROL IN | PUTS | SHIFT REGISTERS | LATCHES | OUTPUTS | | | |
|----------|-------|-----------------|---------------|-----------------------------|---------------|---------|----------------------------|--|--|
| FUNCTION | сьоск | LATCH ENABLE | BLANK- ING | R1 THRU R10 [‡] | LC1 THRU LC10 | SERIAL | Q1 THRU Q10 | | |
| LOAD | 1 | X | Х | Load and shift [‡] | Determined by | R10 | Determined by DLANKING | | |
| LUAD | Not | × | x | No change | LATCH ENABLE§ | RIU | Determined by BLANKING | | |
| LATCH | Х | L | Х | As determined above | Stored data | R10 | Determined by BLANKING | | |
| LAICH | Х | Н | х | As determined above | New data | I NIU | Determined by BLANKING | | |
| BLANK | Х | X | Н | As determined above | Determined by | R10 | All L | | |
| BLAINK | х | X | L | As determined above | LATCH ENABLE§ | NIO | LC1 thru LC10 respectively | | |

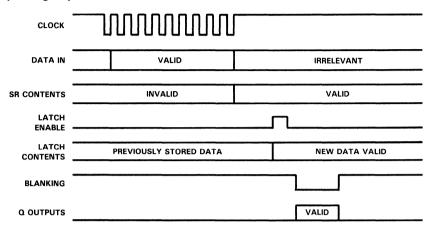
H = high level, L = low level, X = irrelevant, $\uparrow = low-to-high-level transition$.

 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

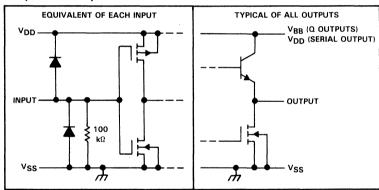
[‡] Register R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

[§] New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



TL4810BI, TL4810B VACUUM FLUORESCENT DISPLAY DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Logic supply voltage, VDD (see Note 1) | 18 \ | ٧ |
|--|-------|---|
| Driver supply voltage, VBB | 70 ١ | ٧ |
| Output voltage | 70 ١ | ٧ |
| Input voltage | 0.3 \ | ٧ |
| Continuous total power dissipation See Dissipation Rating | Tabl | е |
| Operating free-air temperature range: TL4810BI40°C to | 85°0 | С |
| TL4810B 0°C to | 70°0 | С |
| Storage temperature range65 °C to 1 | 50°0 | С |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260° | С |

NOTE 1: Voltage values are with respect to VSS.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|---------------------------------------|
| DW | 1125 mW | 9.0 mW/°C | 720 mW | 585 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

recommended operating conditions

| DADA | METER | • | TL48101 | BI | TL4810B | | | UNIT | |
|---|----------------------------|-------------------|---------|-------|---------|-----|-------|------|--|
| PARA | METER | MIN | NOM | MAX | MIN | NOM | MAX | UNIT | |
| Supply voltage, V _{DD} | | 4.75 | | 15.75 | 4.75 | | 15.75 | ٧ | |
| Supply voltage, V _{BB} | | 5 | | 60 | 5 60 | | | V | |
| Supply voltage, VSS | | | 0 | | | 0 | | V | |
| High level inner valence V | for V _{DD} = 5 V | 3.5 | | 5.3 | 3.5 | | 5.3 | v | |
| High-level input voltage, V _{IH} | for V _{DD} = 15 V | 13.5 | | 15.3 | 13.5 | | 15.3 | · | |
| Low-level input voltage, VIL | | -0.3 [†] | | 0.8 | -0.3 | | 0.8 | V | |
| Continuous high-level output c | urrent, IOH | | | - 25 | | | - 25 | mA | |
| Operating free-air temperature, TA | | -40 | | 85 | 0 | | 70 | °C | |

[†] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.

electrical characteristics over recommended operating free-air temperature range, VDD = 5 V to 15 V, VBB = 60 V, VSS = 0 (unless otherwise noted)

| | PARAM | | 7507 | CONDITIONS | | TL4810 | 31 | | TL4810 | В | UNIT |
|--------|---|---------------------------|--------------------------|--------------------------|------|------------------|------|----------|--------|-----|------|
| | PAKAM | EIEK | TEST | CONDITIONS | MIN | TYP [‡] | MAX | MIN | TYP‡ | MAX | UNII |
| • | High-level | Q outputs | I _{OH} = -25 mA | | 57.5 | 58 | | 57.5 | 58 | | |
| Voн | output | Serial output | $V_{DD} = 5 V$, | $I_{OH} = -100 \mu A$ | 4 | 4.5 | | 4 | 4.5 | | V |
| | voltage | Condi odipat | $V_{DD} = 15 V$, | $I_{OH} = -100 \mu A$ | 14 | 14.7 | | 14 | 14.7 | | |
| | Low-level | Q outputs | $I_{OH} = 1 \mu A$, | BLANKING at VDI |) | 0.5 | 1 | | 0.5 | 1 | |
| VOL | output | Serial output | $V_{DD} = 5 V$, | $I_{OL} = 100 \mu A$ | | 0.05 | 0.1 | | 0.05 | 0.1 | V |
| | voltage | ochai output | $V_{DD} = 15 V$, | $I_{OL} = 100 \mu A$ | | 0.02 | 0.1 | | 0.02 | 0.1 | |
| | Low-level Q output current OL (pull-down current) | | $V_0 = 60 V$, | BLANKING at VDI | D, | | | | 0.7 | | |
| i . | | | TA = MIN to 7 | o°C | 2.5 | 3.7 | | 2.5 | 3.7 | | |
| lOF | | | V _O = 60 V, | BLANKING at VDI |), | | | | | | mA |
| | | | T _A = 85°C | | , 2 | | | | | | |
| | 044 | | $V_0 = 0,$ | BLANKING at VDI |), | – 1 | | | -1 | 15 | |
| ¹O(off | Off-State o | utput current | $T_A = MAX$ | | į | -1 | - 15 | -15 -1 | | 15 | μΑ |
| ΙΗ | High-level i | nput current | $V_I = V_{DD}$ | | | 30 | 50 | | 30 | 50 | μΑ |
| | | | All outputs low | | | 0.5 | 1 | | 0.5 | 1 | |
| IBB | Supply curr | rent from V _{BB} | All outputs high | $T_A = 0$ °C to MA | X | 2.7 | 4 | | 2.7 | 4 | mA |
| | | | All outputs high | $T_{A} = -40^{\circ}C$ | | | 5 | | | | |
| | | | ' All inputs at 0 \ | /, V _{DD} = 5 V | | 10 | 50 | | 10 | 50 | |
| | Cumply ave | rant from \/ | One Q output hi | gh $V_{DD} = 15 V$ | | 10 | 100 | | 10 | 100 | |
| IDD | Supply cur | rent from V _{DD} | All inputs at 0 \ | /, V _{DD} = 5 V | | 10 | 50 | | 10 | 50 | μΑ |
| | | | All outputs low | $V_{DD} = 15 \text{ V}$ | | 10 | 100 | | 10 | 100 | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

timing requirements over recommended operating free-air temperature range

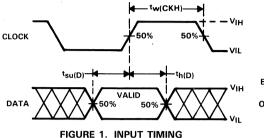
| | PARAMETER | , V _{DD} | = 5 V | V _{DD} | UNIT | |
|--------------------|---|-------------------|-------|-----------------|------|------|
| | FANAIVIETEN | MIN | MAX | MIN | MAX | UNII |
| tw(CKH) | Pulse duration, CLOCK high | 250 | | 50 | | ns |
| tw(LEH) | Pulse duration, LATCH ENABLE high | 250 | | 50 | | ns |
| t _{su(D)} | Setup time, DATA IN before CLOCK↑ | 125 | | 25 | | ns |
| th(D) | Hold time, DATA IN after CLOCK1 | 125 | | 25 | | ns |
| tCKH-LEH | Delay time, CLOCK↑ to LATCH ENABLE high | 125 | | 25 | | ns |

switching characteristics, $V_{BB} = 60 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|--|--|------------------------|-----|-----|-----|------|
| A December delegation of ATCH FMADIF As a second | | $V_{DD} = 5 V$ | 1 | | | |
| 1 | t _{pd} Propagation delay time, LATCH ENABLE to output | V _{DD} = 15 V | | 0.5 | | μS |

[‡] All typical values are at $T_A = 25$ °C, except for I_O .

PARAMETER MEASUREMENT INFORMATION



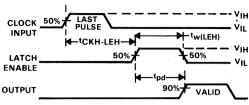
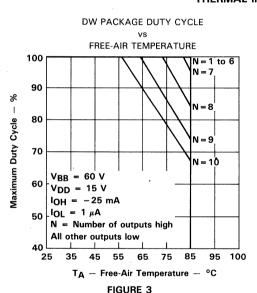


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION



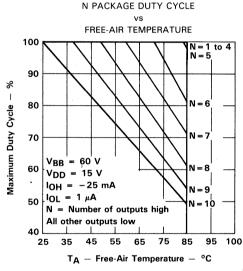


FIGURE 4

TL5812I, TL5812 VACUUM FLUORESCENT DISPLAY DRIVERS

D2914, OCTOBER 1985-REVISED OCTOBER 1989

- Drives Up to 20 Lines
- 70-V Output Voltage Swing Capability
- 40-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Direct Replacement for Sprague UCN5812A

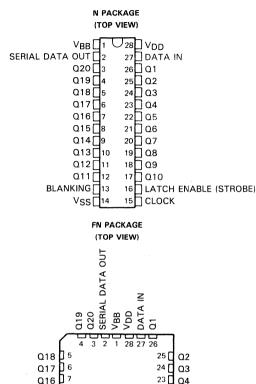
description

The TLC5812I and TLC5812 are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of CLOCK. Parallel data is transferred to the output buffers through a 20-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

The outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and a source-current capability of 40 mA. All inputs are CMOS compatible.

The TLC5812I is characterized for operation from -40°C to 85°C. The TLC5812 is characterized for operation from 0°C to 70°C.



Q15 D8

11

Q14 D9

Q13 D10

Q12

†BIDFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip - patented process.



22 🏻 Q5

21 D Q6

20 Q Q7

19 □

12 13 14 15 16 17 18

010

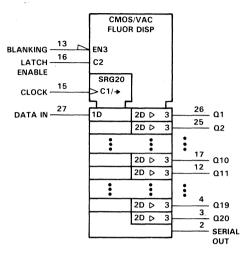
ATCH ENABLE (STROBE)

VSS

BLANKING

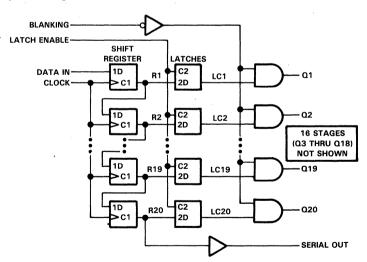
Ω8

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

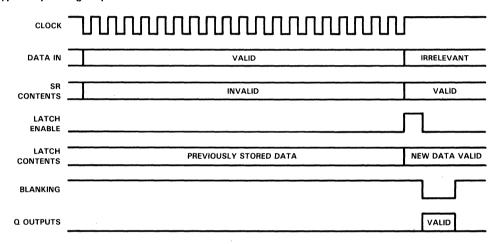


FUNCTION TABLE

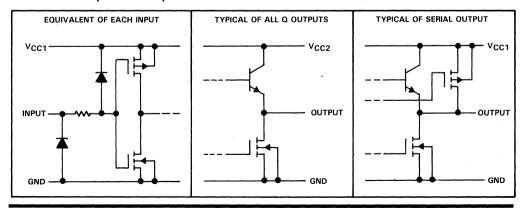
| | CC | NTROL INF | UTS | SHIFT REGISTER | LATCHES | | OUTPUTS |
|----------|-------|-----------------|----------|-----------------------------|---------------|--------|-----------------------------|
| FUNCTION | СГОСК | LATCH ENABLE | BLANKING | R1 THRU R20 | LC1 THRU LC20 | SERIAL | Q1 THRU Q20 |
| 1045 | † | Х | X | Load and shift [†] | Determined by | R20 | Determined by DLANKING |
| LOAD | No† | × | × | No change | LATCH ENABLE‡ | R20 | Determined by BLANKING |
| LATCU | Х | L | Х | As determined above | Stored data | R20 | Determined by BLANKING |
| LATCH | Х | н | х | As determined above | New data | R20 | Determined by BLANKING |
| BLANK | Х | X | Н | As determined above | Determined by | R20 | All L |
| BLANK | Х | × | L | As determined above | LATCH ENABLE‡ | R20 | LC1 thru LC20, respectively |

H = high level, L = low level, $\dot{X} = irrelevant$, $\uparrow = low-to-high-level transition$.

typical operating sequence



schematics of inputs and outputs



[†]R20 takes on the state of R19, R19 takes on the state of R18, . . . R2 takes on the state of R1, and R1 takes on the state of the data input. ‡New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

TL5812I, TL5812 VACUUM FLUORESCENT DISPLAY DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VDD (see Note 1) |
|--|
| Supply voltage, VBB |
| Output voltage, VO |
| Input voltage, V _I |
| Output current, IO |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range: TL5812I40°C to 85°C |
| TL5812 0°C to 70°C |
| Storage temperature range |
| Case temperature for 10 seconds: FN package |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package 260 °C |

NOTE 1. All voltage values are with respect to Vss.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|---------------------------------------|
| FN | 1400 mW | 11.2 mW/°C | 896 mW | 728 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

recommended operating conditions.

| | | | MIN | NOM | MAX | UNIT |
|--|-----------|-----------------------|-----|----------------------|-----|------|
| Supply voltage, V _{DD} | | | 4.5 | | 15 | V |
| Supply voltage, VBB | | | 0 | | 60 | V |
| Supply voltage, VSS | | | | 0 | | ٧ |
| High-level input voltage, VIH | | V _{DD} - 1.5 | | V _{DD} +0.3 | V | |
| Low-level input voltage, V _{IL} | | -0.3 [†] | | 0.8 | V | |
| High-level output current, IOH | | | | | -40 | mA |
| Operating free six temperature T | * TL5812I | | -40 | | 85 | °C · |
| Operating free-air temperature, TA | TL5812 | | 0 | | 70 | -,0 |

[†]The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

| PARAMETER | | | TEST C | ONDITIONS | MIN | TYP [‡] | MAX | UNIT |
|-----------------------------|-------------------------------------|-------------------|--------------------------|-----------------------------|------|------------------|------|------|
| | | Q outputs | I _{OH} = -25 mA | | 57.5 | 58.2 | | |
| ∨он | High-level output | Serial outputs | $V_{DD} = 5 V$, | I _{OH} = -20 μA | 4.5 | 4.9 | | V |
| | | Serial outputs | $V_{DD} = 15 V$, | $I_{OH} = -20 \mu A$ | 14.5 | 14.9 | | |
| | | Q outputs | $I_{OL} = 1 \text{ mA},$ | BLANKING at V _{DD} | | 0.7 | 1.5 | .3 V |
| v_{OL} | Low-level output voltage | Carial autouta | $V_{DD} = 5 V$, | IOL = 20 μA | | 0.06 | 0.3 | |
| | | Serial outputs | $V_{DD} = 15 V$, | I _{OL} = 20 μA | | 0.03 | 0.3 | |
| ΊΗ | High-level input current | | $V_I = V_{DD}$ | | | 0.3 | 1 | μΑ |
| ΊL | Low-level input current | | V ₁ = 0 | | | -0.3 | - 1 | μΑ |
| loL | Low-level output current (pr | ull down current) | $V_0 = 60 V$, | BLANKING at V _{DD} | 2.5 | 3.2 | | μΑ |
| IO(off) | Off-state output current | | $V_0 = 0$, | BLANKING at V _{DD} | | < - 1 | - 15 | μΑ |
| 1 | Complete account from Man | | Outputs high | | | 3.5 | 8 | mA |
| IBB Supply current from VBB | | | Outputs low | | | 0.02 | 0.5 | mA |
| l | Cumply augrent from V | | V _{DD} = 5 V | | | 1.5 | 3 | m A |
| IDD | Supply current from V _{DD} | | V _{DD} = 15 V | | | 1.7 | 4 | mA |

 $^{^{\}ddagger}AII$ typical characteristics are at $T_{\mbox{\scriptsize A}}=~25\,^{\circ}\mbox{\scriptsize C}.$



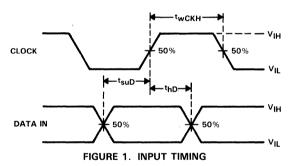
timing requirements over operating free-air temperature range

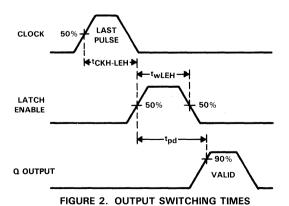
| | PARAMETER | | MIN | MAX | UNIT | 1 |
|--|---|------------------------|-----|-----|------|---|
| | Pulse duration, CLOCK high | V _{DD} = 5 V | 500 | | | 7 |
| twCKH | Fulse duration, CLOCK high | V _{DD} = 15 V | 100 | | ns | ١ |
| | Pulse duration, LATCH ENABLE high | $V_{DD} = 5 V$ | 500 | | | 1 |
| twLEH | Fulse duration, LATCH ENABLE high | V _{DD} = 15 V | 100 | | ns | 1 |
| | Setup time, data before CLOCK† | $V_{DD} = 5 \text{ V}$ | 150 | | | 1 |
| tsuD | Setup time, data before CLOCK | V _{DD} = 15 V | 75 | | ns | |
| | Hold time, data after CLOCK1 | V _{DD} = 5 V | 150 | | ns | 7 |
| thD | Hold time, data after CLOCK | V _{DD} = 15 V | 75 | | 115 | |
| tCKH-LFH Delay time, CLOCKT to LATCH ENABLE high | $V_{DD} = 5 V$ | 150 | | 200 | 1 | |
| tCKH-LEH | belay time, CLOCK! to LATCH ENABLE high | V _{DD} = 15 V | 75 | | ns | ١ |

switching characteristics, $V_{BB} = 60 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | | | TYP | MAX | UNIT |
|-----------------|-------------------------|------------------------|---|-----|-----|------|
| | Propagation delay time, | $V_{DD} = 5 V$ | 2 | | | |
| ^t pd | LATCH ENABLE to output | V _{DD} = 15 V | | 0.8 | | μS |

PARAMETER MEASUREMENT INFORMATION





THERMAL INFORMATION



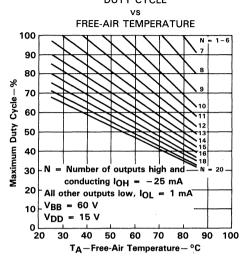


FIGURE 3

| | General Information | 1 |
|---|--|---|
| | | |
| | | |
| | | _ |
| | Data Transmission and Control Circuits | 2 |
| | | |
| | | |
| | Display Drivers | 3 |
| | | |
| | | |
| , | | |
| | Peripheral Drivers/Power Actuators | 4 |
| L | | |
| | | |
| | | |
| | Mechanical Data | 5 |
| | | |
| | | |
| | | |

Explanation of Logic Symbols

D2758, MARCH 1986-REVISED MARCH 1990

- Designed for -52-V Battery Operation
- 50-mA Output Current Capability
- Input Compatible with TTL and CMOS
- High Common-Mode Input Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-In Output Clamp Diode
- Direct Replacement for National DS3680 and Fairchild µA3680

| (TOP VIEW) | | | | | |
|---|---------------------|--|--|--|--|
| AMPL #1 \ IN + | 1 U14 BAT GND | | | | |
| | | | | | |
| AMPL #2 \(\begin{aligned} IN - \bigcup \\ IN + \bigcup \end{aligned} | 3 12 OUTPUT AMPL #2 | | | | |
| ~"" | 4 11 OUTPUT AMPL #3 | | | | |
| AMPL #3 {IN + [] | 5 10 OUTPUT AMPL #4 | | | | |
| ^\\\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | 6 9∏ BAT NEG | | | | |
| AMPL #4 IN - | 7 8 N+ AMPL #4 | | | | |

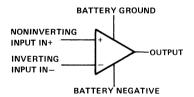
D OR N PACKAGE

description

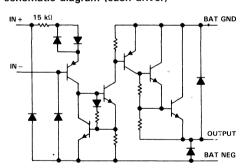
The DS3680I telephone relay driver is a monolithic integrated circuit designed to interface -48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard -52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ± 20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output will be ''off'' as a fail-safe condition when either output is open.

The DS3680I is characterized for operation from -40°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range at BAT NEG, V _B = (see Note 1) |
|---|
| Input voltage range with respect to BAT GND |
| Input voltage range with respect to BAT NEG |
| Differential input voltage, V _{ID} (see Note 2) ±20 V |
| Output current: resistive load |
| inductive load – 50 mA |
| Inductive output load |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA40°C to 85°C |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltages are with respect to the BAT GND terminal unless otherwise specified.

2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN-.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

recommended operating conditions

| | MIN | MAX | UNIŢ |
|---|------------------|-----|------|
| Supply voltage, V _B _ | -10 | -60 | V |
| Input voltage, either input | -20 [†] | 20 | ٧ |
| High-level differential input voltage, VIDH | 2 | 20 | V |
| Low-level differential input voltage, VIDL | -20 [†] | 0.8 | V |
| Operating free-air temperature, TA | - 40 | 85 | °C |

[†]The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage

electrical characteristics over recommended operating free-air temperature range, $V_{B-} = -52 \text{ V}$ (unless otherwise noted)

| | PARAMETER | TEST COND | DITIONS | MIN TYP‡ | MAX | UNIT |
|---------------------|--------------------------------------|-------------------------|--------------------------|----------|-------|---------------------------------------|
| 1 | High-level input current (into IN+) | $V_{ID} = 2 V$ | | 40 | 100 | μΑ |
| Iн | High-level input current (into in +) | $V_{ID} = 7 V$ | | 375 | 1000 | μΑ |
| 1 | Low-level input current (into IN+) | $V_{ID} = 0.4 V$ | | 0.01 | 5 | |
| ΙΙL | Low-lever input current (into in +) | $V_{ID} = -7 \text{ V}$ | | -1 | -100 | μΑ |
| VO(on) | On-state output voltage | $I_0 = -50 \text{ mA},$ | V _{ID} = 2 V | -1.6 | -2.1 | V. |
| 1 | Off-state output current | V V- | $V_{ID} = 0.8 \text{ V}$ | -2 | - 100 | |
| 'O(off) | | $VO = VB^-$ | Inputs open | -2 | -100 | μΑ |
| IR | Clamp diode reverse current | V _O = 0 | | 2 | 100 | μΑ |
| Vok | Output clamp voltage | $I_O = 50 \text{ mA}$ | | 0.9 | 1.2 | v |
| VOK | Output clamp voltage | $I_0 = -50 \text{ mA},$ | $V_{B-}=0$ | -0.9 | -1.2 | \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ |
| IB(on) | On-state battery current | All drivers on | | -2 | -4.4 | mA |
| I _{B(off)} | Off-state battery current | All drivers off | | -1 | - 100 | μΑ |

 $^{^{\}ddagger}$ All typical values are at $T_{A} = 25$ °C.



| switching | characteristics | $V_{R-} =$ | -52 V | . TΔ = | 25°C |
|-----------|-----------------|------------|-------|--------|------|
|-----------|-----------------|------------|-------|--------|------|

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------|---------------|------------------------------|---------------------|-----|-----|-----|------|
| ton | Turn-on time | V _{ID} = 3-V pulse, | $R_L = 1 k\Omega$, | | 1 | 10 | μS |
| toff | Turn-off time | L = 1 H, | See Figure 2 | | 1 | 10 | μS |

PARAMETER MEASUREMENT INFORMATION

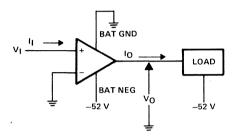
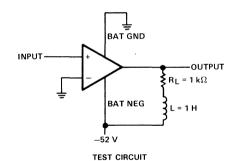


FIGURE 1. GENERALIZED TEST CIRCUIT, EACH DRIVER



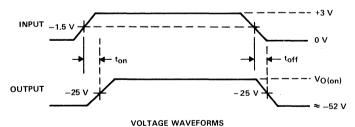


FIGURE 2. SWITCHING CHARACTERISTICS, EACH DRIVER



APPLICATION INFORMATION

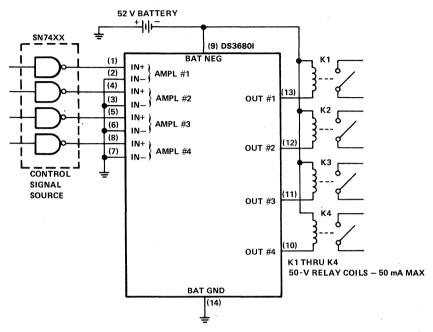


FIGURE 3. RELAY DRIVER

D2942, SEPTEMBER 1986-REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Pulsed Current 2-A Driver
- Wide Supply Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- NE Package Designed for Heat Sinking
- Thermal Shutdown
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Functional Replacement for SGS L293

description

The L293 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

NE PACKAGE (TOP VIEW)

| 1,2EN 1 1 16 VCC1 1A 2 15 4A 1Y 3 14 4Y HEATSINK AND 14 13 HEATSINK AND GROUND 5 12 GROUND 2Y 6 11 3Y 2A 7 10 3A VCC2 8 9 3,4EN |
|--|
|--|

FUNCTION TABLE (EACH DRIVER)

| INP | JTS† | OUTPUT |
|-----|------|--------|
| Α | EN | Y |
| Н | Н | Н |
| L | Н | L |
| x | L | z |

H = high-level L = low-level

X = irrelevant

Z = high-impedance

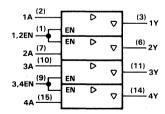
(off)

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal , separate from V_{CC2} , is provided for the logic inputs to minimize device power dissipation.

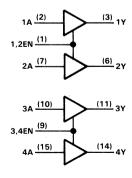
The L293 is designed for operation from 0°C to 70°C.

logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

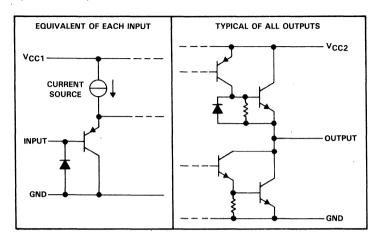
logic diagram





[†]In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Logic supply voltage, V _{CC1} (see Note 1). 36 V Output supply voltage, V _{CC2} . 36 V |
|--|
| Input voltage |
| Output voltage range |
| Peak output current (nonrepetitive, t \leq 5 ms) |
| Continuous output current |
| Continuous total dissipation at (or below) 25 °C free-air temperature |
| (see Notes 2 and 3) |
| Continuous total dissipation at 80 °C case temperature (see Note 3) |
| Operating case or virtual junction temperature range40°C to 150°C |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

- NOTES: 1. All voltage values are with respect to the network ground terminal.
 - 2. For operation above 25 °C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
 - 3. For operation above 25 °C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|------------------------|-------------------|-----|------|
| Logic supply voltage, V _{CC1} | | 4.5 | 7 | V |
| Output supply voltage, VCC2 | | | 36 | ٧ |
| High level in the college Mark | V _{CC1} ≤ 7 V | 2.3 | | ., |
| High-level input voltage, VIH | V _{CC1} ≥ 7 V | 2.3 | 7 | 1 ° |
| Low-level input voltage, VIL | | -0.3 [†] | 1.5 | V |
| Operating free-air temperature | TA | 0 | 70 | °C |

[†]The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.



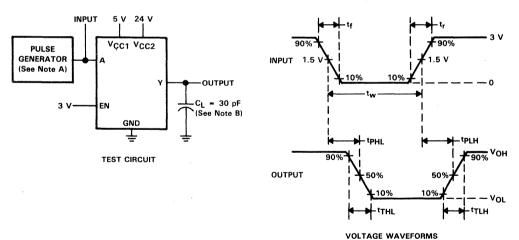
electrical characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 24 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | | TEST CONDITIONS | | TYP | MAX | UNIT | |
|------|--|-----------------------|-------------------------------|------------------------|-----------------------|-------|------|--|
| Vон | High-level output voltage I _{OH} = −1 A | | 1 A | V _{CC2} - 1.8 | V _{CC2} -1.4 | | ٧ | |
| VOL | Low-level output voltage | I _{OL} = 1 A | 4 | | 1.2 | 1.8 | V | |
| 1 | High-level input current | V ₁ = 7 V | | | 0.2 | 100 | ^ | |
| ΉΗ | EN | V-1 = 7 V | | | 0.2 | ±10 | μΑ | |
| 1 | Low level input current A | V ₁ = 0 | | | 3 | - 10 | ^ | |
| IJĽ | Low-level input current EN | V1 = 0 | | | - 2 | - 100 | μΑ | |
| | | | All outputs at high level | | 13 | 22 | | |
| ICC1 | Logic supply current | Io = 0 | All outputs at low level | | 35 | 60 | mA | |
| | • | | All outputs at high impedance | | 8 | 24 | | |
| | | | All outputs at high level | | 14 | 24 | | |
| ICC2 | Output supply current | Io = 0 | All outputs at low level | | 2 | 6 | mA | |
| | | | All outputs at high impedance | | 2 | 4 | ŀ | |

switching characteristics, VCC1 = 5 V, VCC2 = 24 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---------------------------------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output from A input | · · · · · · · · · · · · · · · · · · · | | ns | | |
| tPHL | Propagation delay time, high-to-low-level output from A input | | | ns | | |
| t _{TLH} Transition time, low-to-high-level output | | See Figure 1 | | 300 | | ns |
| tTHL | Transition time, high-to-low-level output | | | 300 | | ns |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 10$ μ s, PRR = 5 kHz, $Z_0 = 50$ Ω . B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



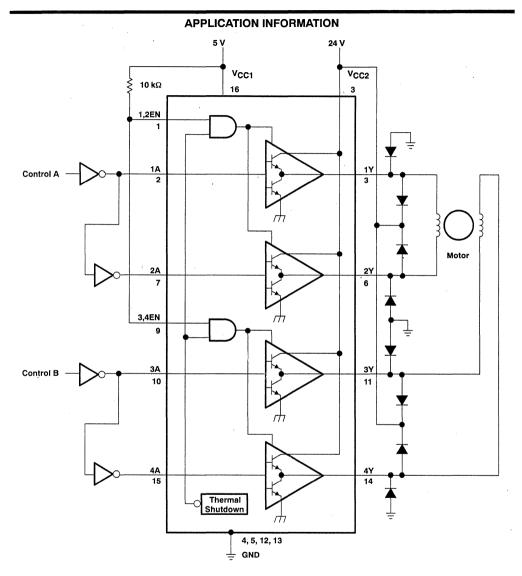


Figure 2. Two-Phase Motor Driver

- 600-mA Output Current Capability Per Driver
- Pulsed Current 1.2-A Per Driver
- Output Clamp Diodes for Inductive Transient Suppression
- Wide Supply Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Functional Replacement for SGS L293D

description

The L293D is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 600 mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

10 3A

a∏ 3.4EN

NE PACKAGE

FUNCTION TABLE (EACH DRIVER)

2A [

VCC2

| INPU | JTS [†] | OUTPUT |
|------|------------------|--------|
| Α | EN | Υ |
| Н | Н | Н |
| L | Н | L |
| х | i | 7 |

H = high-level

_ = low-level

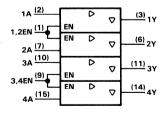
X = irrelevant

Z = high-impedance

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

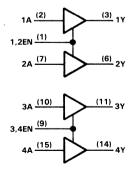
A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation. The L293D is designed for operation from 0° C to 70° C.

logic symbol[‡]



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

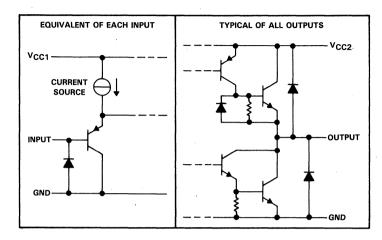




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[†]In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Logic supply voltage, V _{CC1} (see Note 1) |
|--|
| Input voltage |
| Output voltage range |
| Peak output current (nonrepetitive, t \leq 100 μ s) |
| Continuous output current |
| Continuous total dissipation at (or below) 25°C free-air temperature |
| (see Notes 2 and 3) |
| Continuous total dissipation at 80 °C case temperature (see Note 3) |
| Operating case or virtual junction temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

- NOTES: 1. All voltage values are with respect to the network ground terminal.
 - 2. For operation above 25 °C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
 - 3. For operation above 25 °C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

| | · | MIN | MAX | UNIT |
|---|------------------------|-------------------|------------------|------|
| Logic supply voltage, V _{CC1} | | 4.5 | 7 | ٧. |
| Output supply voltage, V _{CC2} | | V _{CC1} | 36 | ٧ |
| High-level input voltage, V _{IH} | V _{CC1} ≤ 7 V | 2.3 | V _{CC1} | V |
| | V _{CC1} ≥ 7 V | 2.3 | 7 | |
| Low-level input voltage, V _{IL} | | -0.3 [†] | 1.5 | ٧ |
| Operating free-air temperature, TA | | 0 | . 70 | °C |

[†]The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.



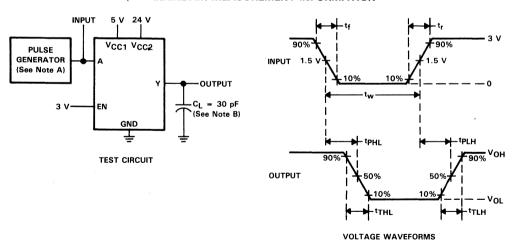
electrical characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 24 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|------|-----------------------------|------------|-------------------------------|-------------------------------|---------------------------|-------------------------|-------|------|--|
| Voн | High-level output voltage | | I _{OH} = -0 |).6 A | V _{CC2} - 1.8 | 3 V _{CC2} -1.4 | | V | |
| VOL | Low-level output voltage | | $I_{OL} = 0.6$ | Α | | 1.2 | 1.8 | ٧ | |
| Vокн | High-level output clamp v | oltage | I _{OK} = 0.6 | 6 A | | V _{CC2} + 1.3 | | ٧ | |
| VOKL | Low-level output clamp v | oltage | 10K = -0 |).6 A | | 1.3 | | ٧ | |
| 1 | High-level input current | Α | V _I = 7 V | | | 0.2 | 100 | μΑ | |
| ΊΗ | riigii-level iliput current | EN | V - / V | | | 0.2 | ±10 | μΑ | |
| 1 | Low-level input current | Α | V _I = 0 | | | -3 | 10 | μΑ | |
| 'IL | Low-level input current | EN | VI - 0 | - 0 | | -2 | - 100 | μΑ | |
| | | | | All outputs at high level | | 13 | 22 | | |
| ICC1 | Logic supply current | | $I_0 = 0$ | All outputs at low level | | 35 | 60 | mA | |
| | | | | All outputs at high impedance | | 8 | 24 | | |
| | | | | | All outputs at high level | | 14 | 24 | |
| ICC2 | Output supply current | | $I_0 = 0$ | All outputs at low level | | 2 | 6 | mA | |
| | | All output | All outputs at high impedance | | 2 | 4 | | | |

switching characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 24 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output from A input | | | 800 | | ns |
| tpHL Propagation delay time, high-to-low-level output from A input | | $C_L = 30 pF$, | | 400 | | ns |
| tTLH | Transition time, low-to-high-level output | See Figure 1 | | 300 | | ns |
| tTHL | Transition time, high-to-low-level output | | | 300 | | ns |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 10~\mu s$, PRR = 5 kHz, $Z_0 = 50~\Omega$. B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



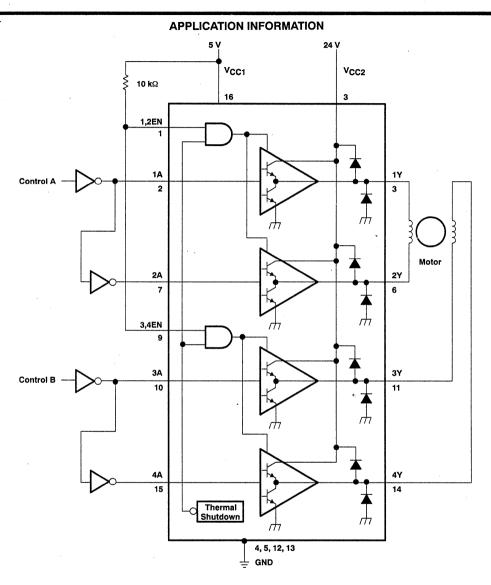


Figure 2. Two-Phase Motor Driver

- 2-A Output Current Capability per Full-H Driver
- Wide Range of Output Supply Voltage . . . 5 V to 46 V
- Separate Input-Logic Supply Voltage
- Thermal Shutdown
- Internal Electrostatic Discharge Protection
- High Noise Immunity
- Functional Replacement for SGS L298

description

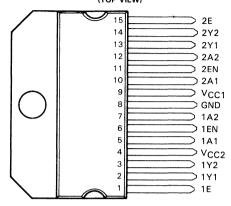
The L298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totempole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2} , is provided for the logic inputs.

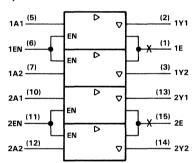
The L298 is designed for operation from 0° C to 70° C.

(TOP VIEW)



The tab is electrically connected to pin 8.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH CHANNEL)

| INPL | JTS‡ | OUTPUT |
|------|------|--------|
| Α | EN | Υ |
| Н | Н | Н |
| L | н | Ĺ |
| Х | L | z |

[†]In the thermal shutdown mode, the outputs are in the high-impedance state regardless of the input levels.

H = high-level

L = low-level

X = irrelevant

Z = high-impedance (off)



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logic diagram (positive logic) V_{CC2} 2Y1 (3) (4)(13) (14) V_{CC1}(9) (12) 2A2 (1<u>0)</u> 2A1 1A2 (7) (<u>11)</u> 2EN 1EN_(6) (15) (1) (8) GŃD

absolute maximum ratings over operating temperature range (unless otherwise noted)

| Logic supply voltage, VCC1, (see Note 1) |
|---|
| Output supply voltage, VCC2 50 V |
| Input voltage range at A or EN, V _I |
| Output voltage range, VO |
| Emitter terminal (1E and 2E) voltage range |
| Emitter terminal (1E and 2E) voltage (nonrepetitive, t _W ≤ 50 µs) |
| Peak output current, I _{OM} , (nonrepetitive, t _W ≤ 0.1 ms) |
| (repetitive, $t_W \le 10$ ms, duty cycle $\le 80\%$) ± 2.5 A |
| Continuous output current, Io |
| Peak combined output current for each full-H driver (see Note 2) |
| (nonrepetitive, $t_W \le 0.1 \text{ ms}$) |
| (repetitive, $t_W \le 10$ ms, duty cycle $\le 80\%$) ± 2.5 A |
| Continuous combined output current for each full-H driver (see Note 2) 3.575 W |
| Continuous dissipation at (or below) 25 °C free-air temperature (see Note 3) |
| Continuous dissipation at (or below) 75 °C case temperature (see Note 3) 25 W |
| Operating free-air, case, or virtual junction temperature range40°C to 150°C |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.

- Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
- 3. For operation above 25 °C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75 °C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

| | | MIN | MAX | UNIT | |
|--|----|-------------------|------------------------|------|--|
| Logic supply voltage, V _{CC1} | | 4.5 | 7 | V | |
| Output supply voltage, V _{CC2} | | 5 | 46 | V | |
| , | | -0.5 [†] | 2 | | |
| Emitter terminal (1E or 2E) voltage, V _E (see Note 4) | | | V _{CC1} - 3.5 | V | |
| | | | V _{CC2} - 4 | | |
| | A | 2.3 | V _{CC1} | | |
| High-level input voltage, VIH (see Note 4) | | | V _{CC2} -2.5 | v | |
| High-lever input voltage, VIH (see Note 4) | EN | 2.3 | 7 | ľ | |
| | EN | | V _{CC1} | | |
| Low-level input voltage at A or EN, V _{IL} | | -0.3 [†] | 1.5 | V | |
| Output current, IO | | | ± 2 | Α | |
| Commutation frequency, f _C | | | 40 | kHz | |
| Operating free-air temperature, TA | | 0 | 70 | °C | |

[†]The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 4: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_J = 25 °C (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | | | |
|------------------------------|-------------------------------|------------------------|-----------------------|---|-------------------------------|-------------------------|----------------------|----------------------|----|--|
| Va High lovel output voltage | | I _{OH} = -1 A | | V _{CC2} -1.8 V _{CC2} -1.2 | | | V | | | |
| ۷ОН | VOH High-level output voltage | | | 2 A | | V _{CC2} -2.8 V | CC2-1.8 | | V | |
| Va | Low-level output voltage | | IOL = 1 A | 4 | | | V _E + 1.2 | V _E + 1.8 | V | |
| VOL | Low-level output voltage | | IOL = 2 / | 4 | | | V _E + 1.7 | V _E + 2.6 | V | |
| v. | Total source plus sink | | IOH = - | A, I _{OL} = 1 A See Note 5 | | | 2.4 | 3.4 | | |
| V _{drop} | output voltage drop | | loh = - | | | 3.5 | | 5.2 | V | |
| 1 | A High level input surrent | | VI = VIH | | | | 30 | 100 | μΑ | |
| ΉΗ | High-level input current | ΕN | $V_I = V_{IH}$ | ≤ V _{CC1} -0.6 V | | | 30 | 100 | μΑ | |
| IIL | Low-level input current | | V _I = 0 to | 1.5 V | | | | - 10 | μΑ | |
| | | | | All outputs at hig | h level | | 7 | 12 | | |
| ICC1 | Logic supply current | | lo = 0 | All outputs at lov | v level | | 24 | 32 | mA | |
| | | | | All outputs at hig | All outputs at high impedance | | 4 | 6 | ĺ | |
| | | | | All outputs at high level | | | 38 | 50 | | |
| ICC2 | Output supply current | | 10 = 0 | All outputs at lov | v level | | 13 | 20 | mA | |
| | | | | All outputs at hig | h impedance | | | 2 | | |

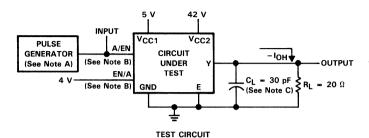
NOTE 5. The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels. $V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_{E}$

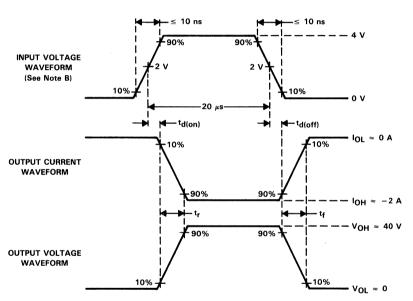
L298 DUAL FULL-H DRIVER

switching characteristics, VCC1 = 5 V, VCC2 = 42 V, VE = 0, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN TYP MAX | UNIT |
|--------------------|--|-------------------------|-------------|------|
| t _{d(on)} | Source current turn-on delay time from A input | | 2.5 | μs |
| td(off) | Source current turn-off delay time from A input | | 1.7 | μs |
| t _r | Source current rise time (turning on) | C _L = 30 pF, | 0.4 | μs |
| tf | Source current fall time (turning off) | See Figure 1 | 0.2 | μs |
| td(on) | Source current turn-on delay time from EN input | | 2.5 | μs |
| td(off) | Source current turn-off delay time from EN input | | 1.7 | μS |
| td(on) | Sink current turn-on delay time from A input | | 1.5 | μS |
| td(off) | Sink current turn-off delay time from A input | | 0.7 | μS |
| t _r | Sink current rise time (turning on) | C _L = 30 pF, | 0.2 | μS |
| tf | Sink current fall time (turning off) | See Figure 2 | 0.2 | μs |
| td(on) | Sink current turn-on delay time from EN input | | 1.5 | μS |
| td(off) | Sink current turn-off delay time from EN input | | 0.7 | μs |

PARAMETER MEASUREMENT INFORMATION





VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_0 = 50 Ω .

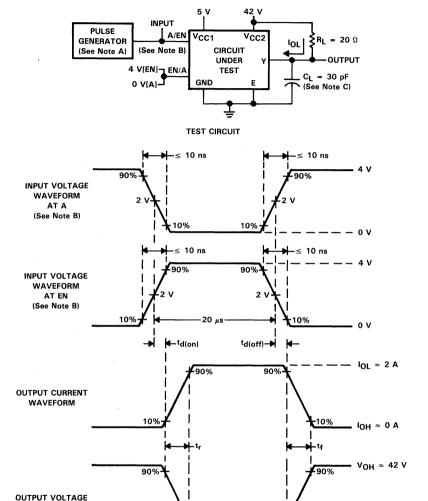
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.

C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS



PARAMETER MEASUREMENT INFORMATION



VOLTAGE AND CURRENT WAVEFORMS

VOL ≈ 2 V

10%

- NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_0 = 50 Ω .
 - B. EN is at 4 $^{\circ}$ V if A is used as the switching input. A is at 0 V if EN is the switching input.
 - C. C_L includes probe and jig capacitance.

WAVEFORM

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS



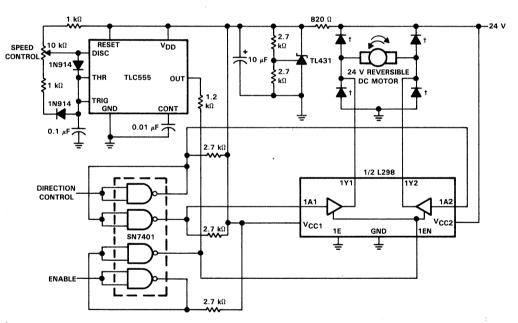
APPLICATION INFORMATION

This circuit shows one half of an L298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the L298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

| ENABLE | NABLE DIRECTION CONTROL | | 1Y2 |
|--------|-------------------------|----------|----------|
| Н | Н | source | sink |
| н | L | sink | source |
| L | x | disabled | disabled |

X = don't care H = high level L = low level



[†]Diodes are 1N4934 or equivalent.

FIGURE 3. L298 AS BIDIRECTIONAL DC MOTOR DRIVER

SN55451B THRU SN55454B SN75451B THRU SN75454B DUAL PERIPHERAL DRIVERS

D2217, DECEMBER 1976-REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

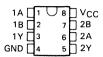
- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SUMMARY OF SERIES 55451B/75451B

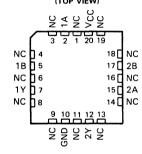
| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|----------|------------------------------|----------|
| SN55451B | AND [†] | FK,JG |
| SN55452B | NAND | FK,JG |
| SN55453B | OR | FK,JG |
| SN55454B | NOR | FK,JG |
| SN75451B | AND | D,P |
| SN75452B | NAND | D,P |
| SN75453B | OR | D,P |
| SN75454B | NOR | D,P |

[†]With output transistor base connected externally to output of gate.

SN55451B, SN55452B, SN55453B, SN55454B . . . JG PACKAGE SN75451B, SN75452B, SN75453B, SN75454B . . . D OR P PACKAGE (TOP VIEW)



SN55451B, SN55452B, SN55453B, SN55454B, . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

description

Series SN55451B/75451B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the SN55451B/SN75451B family is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latchup. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN55451B drivers are characterized for operation over the full military range of -55 °C to 125 °C. Series SN75451B drivers are characterized for operation from 0 °C to 70 °C.

SN55451B THRU SN55454B, SN75451B THRU SN75454B **DUAL PERIPHERAL DRIVERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | , | SN55451B SN55452B SN55453B SN55454B | SN75451B SN75452B SN75453B SN75454B | UNIT |
|---|---------------------------------------|--|--|------|
| Supply voltage, V _{CC} (see Note 1) | | 7 | 7 | V |
| Input voltage | 5.5 | 5.5 | V | |
| Interemitter voltage (see Note 2) | 5.5 | 5.5 | ٧ | |
| Off-state output voltage | 30 | 30 | V | |
| Continuous collector or output current (see Note 4) | 400 | 400 | mA | |
| Peak collector or output current (t _w ≤ 10 ms, duty cycle ≤ 50%, see Note 4) | | | 500 | mA |
| Continuous total power dissipation | · · · · · · · · · · · · · · · · · · · | See Dissipation Rating Table | | |
| Operating free-air temperature range, TA | | -55 to 125 | 0 to 70 | °C |
| Storage temperature range | | | -65 to 150 | °C |
| Case temperature for 60 seconds | FK package | 260 | | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | JG package | 300 | | °C |
| Lead temperature 1,6 mm (1,16 inch) from case for 10 seconds | D or P package | | 260 | °C |

NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.

2. This is the voltage between two emitters of a multiple-emitter transistor.

3. This value applies when the base-emitter resistance (RBE) is equal to or less than 500 Ω .

4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

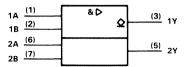
DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | TA = 125°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|----------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW | - |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | |

recommended operating conditions

| | SEF | IES 554 | 51B | SERIES 75451B | | | UNIT |
|------------------------------------|-----|---------|-----|---------------|-----|------|------|
| • | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, VCC | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | 2 | | | ٧ |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | ٧ |
| Operating free-air temperature, TA | -55 | | 125 | 0 | | 70 | °C |

logic symbol†



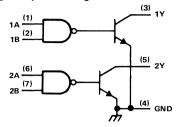
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH DRIVER)

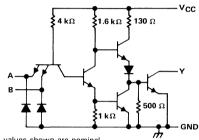
| Α | В | Υ |
|---|---|---------------|
| L | L | L (on state) |
| L | Н | L (on state) |
| Н | L | L (on state) |
| н | Н | H (off state) |

positive logic: $Y = AB \text{ or } \overline{A} + \overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

Pin numbers shown are for D, JG, and P packages.

electrical characteristics over recommended operating free-air temperature range

| | DADAMETED | TEST COM | Dirionet | SI | V5545 | 1B | S | N7545 | 1B | LIBUT |
|------|--|--|--------------------------|----|-------|------|-----|-------|-------|-------|
| | PARAMETER | TEST CON | TEST CONDITIONS‡ | | TYP§ | MAX | MIN | TYP§ | MAX | UNIT |
| VIK | Input clamp voltage | V _{CC} = MIN, | I _I = -12 mA | | -1.2 | -1.5 | | -1.2 | - 1.5 | V |
| Іон | High-level output current | $V_{CC} = MIN,$ $V_{OH} = 30 V$ | V _{IH} = MIN, | | | 300 | | | 100 | μΑ |
| VOL | Low-level output voltage | $V_{CC} = MIN,$ $I_{OL} = 100 \text{ mA}$ | V _{IL} = 0.8 V, | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| VOL | | V _{CC} = MIN, I _{OL} = 300 mA | V _{IL} = 0.8 V, | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| Ιį | Input current at maximum input voltage | V _{CC} = MAX, | $V_1 = 5.5 V$ | | | 1 | | | 1 | mA |
| ΊΗ | High-level input current | V _{CC} = MAX, | V _I = 2.4 V | | | 40 | | | 40 | μΑ |
| IIL | Low-level input current | V _{CC} = MAX, | V _I = 0.4 V | | - 1 | -1.6 | | - 1 | -1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | V _I = 5 V | | 7 | 11 | | 7 | 11 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 0 | | 52 | 65 | | 52 | 65 | mA |

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25 °C

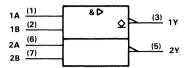
| PARAMETER | | TEST CO | MIN | TYP | MAX | UNIT | |
|--|--------------------------|-----------------|--------------------------|---------------------|--------|------|-------|
| tpLH Propagation delay time, low-to-high-level or | utput | | | | 18 | 25 | ns |
| tphL Propagation delay time, high-to-low-level or | I _O ≈ 200 mA, | $C_L = 15 pF$, | | 18 | 25 | ns | |
| t _{TLH} Transition time, low-to-high-level output | $R_L = 50 \Omega$ | See Figure 1 | | 5 | 8 | ns | |
| t _{THL} Transition time, high-to-low-level output | | | | | 7 | 12 | ns |
| VOH High-level output voltage after switching | SN55451B | $V_S = 20 V$, | I _O ≈ 300 mA, | | Vs-6.5 | 5 | mV |
| VOH Inigri-level output voltage after switching | SN75451B | See Figure 2 | | V _S -6.5 | 5 | | III V |



 $^{^{\}S}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

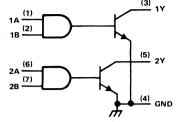
SN55452B. SN75452B **DUAL PERIPHERAL POSITIVE NAND DRIVERS**

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

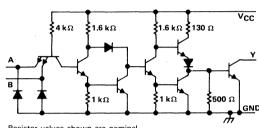


FUNCTION TABLE (EACH DRIVER)

| Α | В | Y |
|---|---|---------------|
| L | L | H (off state) |
| L | Н | H (off state) |
| Н | L | H (off state) |
| Н | Н | L (on state) |

positive logic: $Y = \overline{AB} \text{ or } \overline{A} + \overline{B}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CON | DITIONET | S | N55452 | 2B | S | N75452 | 2B | UNIT |
|------|--|--|-------------------------|-----|--------|-------|-----|--------|-------|------|
| | PARAMETER | TEST CON | DITIONS | MIN | TYP§ | MAX | MIN | TYP§ | MAX | ONLI |
| VIK | Input clamp voltage | V _{CC} = MIN, | I _I = -12 mA | | -1.2 | - 1.5 | | -1.2 | - 1.5 | ٧ |
| Іон | High-level output current | $V_{CC} = MIN,$ $V_{OH} = 30 V$ | V _{IL} = 0.8 V | | , | 300 | | | 100 | μΑ |
| | Low-level output voltage | V _{CC} = MIN, I _{OL} = 100 mA | V _{IH} = MIN | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| VOL | | V _{CC} = MIN, I _{OL} = 300 mA | V _{IH} = MIN, | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| lą | Input current at maximum input voltage | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| ΉΗ | High-level input current | V _{CC} = MAX, | $V_1 = 2.4 V$ | | | 40 | | | 40 | μΑ |
| HL | Low-level input current | V _{CC} = MAX, | V _I = 0.4 V | | -1.1 | -1.6 | | -1.1 | -1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | V ₁ = 0 | | 11 | 14 | | 11 | 14 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 5 V | | 56 | 71 | | 56 | 71 | mA |

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

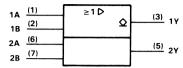
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PARAMETER | | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------|-------------------------|--------------|--------|-----|-----|------|
| tPLH Propagation delay time, low-to-high-level or | utput | | | | 26 | 35 | ns |
| tpHL Propagation delay time, high-to-low-level or | I _O ≈ 200 mA, | C _L = 15 pF, | | 24 | 35 | ns | |
| tTLH Transition time, low-to-high-level output | $R_L = 50 \Omega$, | See Figure 1 | | 5 | 8 | ns | |
| tTHL Transition time, high-to-low-level output | | | | | 7 | 12 | ns |
| Va. High lovel output valtage often avritahing | SN55452B | V _S = 20 V, | IO ≈ 300 mA, | Vs-6.5 | | 5 | mV |
| VOH High-level output voltage after switching | SN75452B | See Figure 2 | | Vs-6. | 5 | | 1110 |



 $^{^{\}S}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

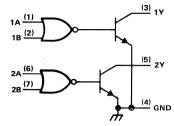
FUNCTION TABLE

| Α | В | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | Н | H (off state) |
| Н | L | H (off state) |
| Н | н | H (off state) |

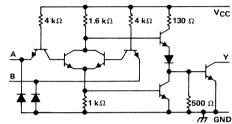
positive logic:

 $Y = A + B \text{ or } \overline{\overline{AB}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

Pin numbers shown are for D, JG, and P packages.

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CON | DITIONE [‡] | S | N55453 | В | S | N75453 | B | UNIT |
|------|--|--|--------------------------|-----|--------|-------|-----|--------|-------|------|
| | PARAMETER | IESI CON | יפאטוווכ | MIN | TYP§ | MAX | MIN | TYP§ | MAX | UNIT |
| VIK | Input clamp voltage | V _{CC} = MIN, | $I_1 = -12 \text{ mA}$ | | - 1.2 | - 1.5 | | 1.2 | - 1.5 | > |
| ЮН | High-level output current | $V_{CC} = MIN,$ $V_{OH} = 30 V$ | V _{IH} = MIN, | | | 300 | | | 100 | μΑ |
| \/ | Low-level output voltage | V _{CC} = MIN, I _{OL} = 100 mA | V _{IL} = 0.8 V, | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| VOL | | V _{CC} = MIN, I _{OL} = 300 mA | V _{IL} = 0.8 V, | | 0.5 | 0.8 | | 0.5 | 0.7 | ľ |
| lį. | Input current at maximum input voltage | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| ЧН | High-level input current | V _{CC} = MAX, | V _I = 2.4 V | | | 40 | | | 40 | μΑ |
| IIL | Low-level input current | V _{CC} = MAX, | $V_1 = 0.4 V$ | | - 1 | - 1.6 | | - 1 | - 1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | V _I = 5 V | | 8 | 11 | | 8 | 11 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 0 | | 54 | 68 | | 54 | 68 | mA |

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

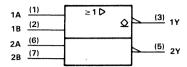
switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------------------------|--------------|-------|-------|-----|-------|
| tpLH Propagation delay time, low-to-high-level or | ıtput | | | | 18 | 25 | ns |
| tpHL Propagation delay time, high-to-low-level or | l _O ≈ 200 mA, | $C_L = 15 pF$, | | 16 | 25 | ns | |
| tTLH Transition time, low-to-high-level output | $R_L = 50 \Omega$, | See Figure 1 | | 5 | 8 | ns | |
| tTHL Transition time, high-to-low-level output | tTHL Transition time, high-to-low-level output | | | | 7 | 12 | ns |
| V High level common veltage often contacting | SN55453B | V _S = 20 V, | IO ≈ 300 mA, | | Vs-6. | 5 | mV |
| VOH High-level output voltage after switching | SN75453B | See Figure 2 | | Vg-6. | 5 | | 111.0 |

[§] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

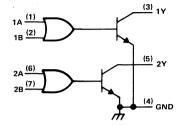
SN55454B, SN75454B **DUAL PERIPHERAL POSITIVE NOR DRIVERS**

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

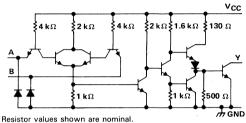


FUNCTION TABLE (EACH DRIVER)

| Α | В | Υ |
|---|---|---------------|
| L | L | H (off state) |
| L | Н | L (on state) |
| Н | L | L (on state) |
| Н | Н | L (on state) |

positive logic: $Y = \overline{A + B} \text{ or } \overline{AB}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CON | DITIONS t | S | N55454 | IB | S | N75454 | B | UNIT |
|----------------|--|--|-------------------------|------|--------|------|-----|--------|-------|------|
| | PARAMETER | IESI COM | DITIONS | MIN. | TYP§ | MAX | MIN | TYP§ | MAX | UNII |
| VIK | Input clamp voltage | V _{CC} = MIN, | I _I = -12 mA | | -1.2 | -1.5 | | -1.2 | - 1.5 | ٧ |
| ЮН | High-level output current | $V_{CC} = MIN,$ $V_{OH} = 30 V$ | V _{IL} = 0.8 V | | | 300 | | | 100 | μΑ |
| V | Low level output voltage | V _{CC} = MIN, I _{OL} = 100 mA | V _{IH} = MIN | | 0.25 | 0.5 | | 0.25 | 0.4 | 4 V |
| VOL | Low-level output voltage | $V_{CC} = MIN,$ $I_{OL} = 300 \text{ mA}$ | V _{IH} = MIN, | | 0.5 | 0.8 | | 0.5 | 0.7 | V |
| l _l | Input current at maximum input voltage | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| ΊΗ | High-level input current | V _{CC} = MAX, | $V_{J} = 2.4 V$ | | | 40 | | | 40 | μΑ |
| ЦL | Low-level input current | V _{CC} = MAX, | $V_1 = 0.4 V$ | | - 1 | -1.6 | | -1 | - 1.6 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = MAX$, | $V_1 = 0$ | | 13 | 17 | | 13 | 17 | mA |
| ICCL. | Supply current, outputs low | V _{CC} = MAX, | $V_I = 5 V$ | | 61 | 79 | | 61 | 79 | mA |

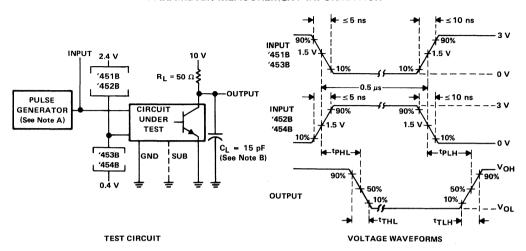
[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | CONTRACTOR OF THE STATE OF THE | TEST CO | NDITIONS | MIN | ГҮР | MAX | UNIT |
|--|---|------------------------|--------------|--------|-------|-----|------|
| tpLH Propagation delay time, low-to-high-level ou | utput | | | | 27 | 35 | ns |
| tpHL Propagation delay time, high-to-low-level or | I _O ≈ 200 mA, | $C_L = 15 pF$, | | 24 | 35 | ns | |
| tTLH Transition time, low-to-high-level output | tTLH Transition time, low-to-high-level output | | | | 5 | 8 | ns |
| t _{THL} Transition time, high-to-low-level output | | | *** | | 7 | 12 | ns |
| VOH High-level output voltage after switching | SN55454B | V _S = 20 V, | Io ≈ 300 mA, | V | s-6.5 | 5 | mV |
| VOH High-level output voltage after switching | SN75454B | See Figure 2 | | Vg-6.5 | | | 1110 |

 $^{^{\}S}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.

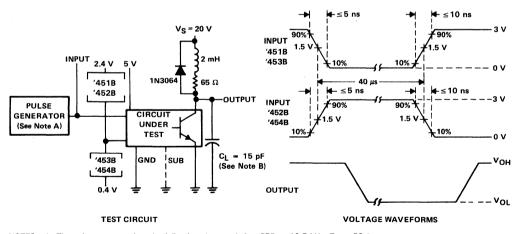
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, Z $_{0}$ \approx 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES OF COMPLETE DRIVERS



NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, Z $_{0}$ = 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE

COLLECTOR CURRENT VCE (sat) -Collector-Emitter Saturation Voltage-V 0.6 0.5 See Note 5 0.4 0.3 0.2 0.1 10 20 40 70 100 200 400 IC-Collector Current-mA

NOTE 5: These parameters must be measured using pulse techniques, $t_W = 300 \mu s$, duty cycle $\leq 2\%$.

FIGURE 3

SN55461 THRU SN55464 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

D2218, DECEMBER 1976-REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

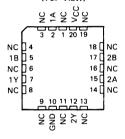
SUMMARY OF SERIES 55461/75461

| DEVICE | LOGIC | PACKAGES |
|---------|-------|----------|
| SN55461 | AND | FK,JG |
| SN55462 | NAND | FK,JG |
| SN55463 | OR | FK,JG |
| SN55464 | NOR | FK,JG |
| SN75461 | AND | D,P |
| SN75462 | NAND | D,P |
| SN75463 | OR | D,P |

SN55461, SN55462, SN55463, SN55464 . . . JG PACKAGE SN75461, SN75462, SN75463 . . . D OR P PACKAGE (TOP VIEW)



SN55461, SN55462, SN55463, SN55464, . . . FK PACKAGE



NC-No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55454B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the gates internally connected to the bases of the n-p-n output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C; Series SN75461 drivers are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.



SN55461 THRU SN55464 SN75461 THRU SN75463 DUAL PERIPHERAL DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55461 SN55462 SN55463 SN55464 | SN75461 SN75462 SN75463 | UNIT | | |
|---|----------------|--|-------------------------------|------|--|--|
| Supply voltage, V _{CC} (see Note 1) | | 7 | 7 | ٧ | | |
| Input voltage | 5.5 | 5.5 | V | | | |
| Interemitter voltage (see Note 2) | 5.5 | 5.5 | ٧ | | | |
| Off-state output voltage | 35 | 35 | | | | |
| Continuous collector or output current (see Note 3) | 400 | 400 | mA | | | |
| Peak collector or output current $(t_W \le 10 \text{ ms, duty cycle} \le 50\%, \text{ see Note 3})$ | 500 | 500 | mA | | | |
| Continuous total power dissipation | | See Dissipation Rating Table | | | | |
| Operating free-air temperature range, TA | | -55 to 125 | 0 to 70 | °C | | |
| Storage temperature range | | -65 to 150 | -65 to 150 | °C | | |
| Case temperature for 60 seconds | FK package | 260 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | JG package | 300 | | °C | | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or P package | | 260 | °C | | |

- NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
 - 2. This is the voltage between two emitters of a multiple-emitter transistor.
 - 3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | _ |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 210 mW |
| , Р | 1000 mW | 8.0 mW/°C | 640 mW | |

recommended operating conditions

| | 1 | SN55461 THRU SN55464 | | | SN75461 THRU SN75463 | | | |
|------------------------------------|------|-------------------------|-----|------|-------------------------|------|----|--|
| · | MIN | NOM | MAX | MIN | NOM | MAX | | |
| Supply voltage, V _{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | |
| High-level input voltage, VIH | 2 | | | 2 | | | ٧ | |
| Low-level input voltage, VIL | | | 0.8 | | | 0.8 | ٧ | |
| Operating free-air temperature, TA | - 55 | | 125 | 0 | | 70 | °C | |

logic symbol † 1A $\frac{(1)}{(2)}$ 2B $\frac{(6)}{(7)}$ (3) 1Y (5) 2Y

Pin numbers shown are for D, JG, and P packages.

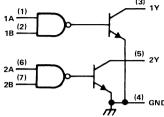
FUNCTION TABLE (EACH DRIVER)

| Α | В | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | Н | L (on state) |
| Н | L | L (on state) |
| Н | Н | H (off state) |

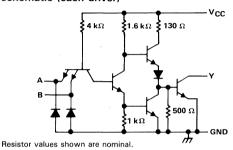
positive logic:

 $Y = AB \text{ or } \overline{\overline{A} + \overline{B}}$

logic diagram (positive logic)



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST SON | DITIONAT | | SN5546 | 1 | SN75461 | | | UNIT |
|------|------------------------------|---------------------------|--------------------------|------|------------------|------|---------|------|-------|-------|
| | PARAMETER | IEST CON | TEST CONDITIONS† | | TYP [‡] | MAX | MIN | TYP‡ | MAX | UNII |
| VIK | Input clamp voltage | V _{CC} = MIN, | I _I = -12 mA | | -1.2 | -1.5 | | -1.2 | -1.5 | V |
| lон | High-level output current | V _{CC} = MIN, | $V_{IH} = MIN,$ | | | 300 | | | 100 | μА |
| 701 | | $V_{OH} = 35 V$ | | | | | | | | μ., . |
| | | V _{CC} = MIN, | $V_{IL} = 0.8 V$ | | 0.25 | 0.5 | | 0.25 | 0.4 | |
| VOL | Low-level output voltage | $I_{OL} = 100 \text{ mA}$ | | 0.20 | | | J | 0.20 | 0. 1 | V |
| VOL | | V _{CC} = MIN, | $V_{IL} = 0.8 V$ | | 0.5 | 0.8 | | 0.5 | 0.7 |) |
| | | $I_{OL} = 300 \text{ mA}$ | | | 0.0 | 0.0 | | 0.0 | 0.7 | |
| 1. | Input current at maximum | VCC = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| l lı | input voltage | VCC - MAX, | VI - 5.5 V | | | ' | | | ' | IIIA |
| ΊΗ | High-level input current | $V_{CC} = MAX$, | V _I = 2.4 V | | | 40 | | | 40 | μΑ |
| IIL | Low-level input current | $V_{CC} = MAX$, | $V_{ } = 0.4 \text{ V}$ | | - 1 | -1.6 | | - 1 | - 1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | V _I = 5 V | | 8 | 11 | | 8 | 11 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 0 | | 56 | 76 | | 56 | 76 | mA |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditons.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

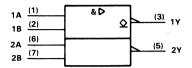
| | PARAMETER | | TEST COM | MIN | TYP | MAX | UNIT | |
|------------------|---|--------------------------|------------------------|--------------------------|--------------------|---------------------|------|------|
| tPLH | Propagation delay time, low-to-high-level | | | | 30 | 55 | ns | |
| ^t PHL | Propagation delay time, high-to-low-level | l _O ≈ 200 mA, | $C_L = 15 pF$, | | 25 | 40 | ns | |
| tTLH | Transition time, low-to-high-level output | $R_L = 50 \Omega$, | See Figure 1 | | 8 | 20 | ns | |
| tTHL | Transition time, high-to-low-level output | | | | 10 | 20 | ns | |
| V | High-level output voltage after switching | SN55461 | V _S = 30 V, | I _O ≈ 300 mA, | | V _S - 10 |) | mV |
| Vон | VOH High-level output voltage after switching | | See Figure 2 | | V _S -10 | | | 1110 |

 $^{^\}dagger$ This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

SN55462, SN75462 DUAL PERIPHERAL POSITIVE NAND DRIVERS

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, JG, and P packages.

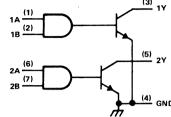
FUNCTION TABLE (EACH DRIVER)

| Α | В | Υ |
|---|---|---------------|
| L | L | H (off state) |
| L | Н | H (off state) |
| Н | L | H (off state) |
| Н | Н | L (on state) |

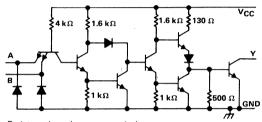
positive logic:

 $Y = \overline{AB} \text{ or } \overline{A} + \overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| 1 | DADAMETED | TEST CONDITIONS† | | 1 | SN55462 | | | SN75462 | | |
|------------------|--|--|------------------------|------------------|---------|------|------|---------|-------|----|
| ŀ | PARAMETER | IEST CON | MIN | TYP [‡] | MAX | MIN | TYP‡ | MAX | UNIT | |
| VIK | Input clamp voltage | V _{CC} = MIN, | lj = -12 mA | | -1.2 | -1.5 | | 1.2 | - 1.5 | ٧ |
| ЮН | High-level output current | V _{CC} = MIN, V _{OH} = 35 V | $V_{IL} = 0.8 V$, | | | 300 | | | 100 | μΑ |
| | | V _{CC} = MIN, I _{OL} = 100 mA | V _{IH} = MIN, | | 0.25 | 0.5 | | 0.25 | 0.4 | |
| VOL | Low-level output voltage | V _{CC} = MIN, I _{OL} = 300 mA | V _{IH} = MIN, | | 0.5 | 0.8 | | 0.5 | 0.7 | V |
| l _l | Input current at maximum input voltage | V _{CC} = MAX, | V _I = 5.5 V | | | 1 | | | 1 | mA |
| lін | High-level input current | V _{CC} = MAX, | V _I = 2.4 V | | | 40 | | | 40 | μΑ |
| I _I L | Low-level input current | V _{CC} = MAX, | V _I = 0.4 V | | -1.1 | 1.6 | | -1.1 | -1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | V ₁ = 0 | | 13 | 17 | | 13 | 17 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 5 V | | 61 | 76 | | 61 | 76 | mA |

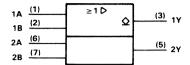
 $^{^{\}dagger}$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

| PAF | PARAMETER | | | TEST CONDITIONS | | | MAX | UNIT |
|---|--|-------|--------------------------|--------------------------|--------------------|--------------------|-----|------|
| tpLH Propagation delay ti | PLH Propagation delay time, low-to-high-level output | | | | | 45 | 65 | ns |
| tpHL Propagation delay time, high-to-low-level output | | | l _O ≈ 200 mA, | $C_L = 15 pF$, | | 30 | 50 | ns |
| t _{TLH} Transition time, low | tTLH Transition time, low-to-high-level output | | | See Figure 1 | | 13 | 25 | ns |
| tTHL Transition time, high | n-to-low-level output | | | | | 10 | 20 | ns |
| Va.: High lovel output ve | SN5 | 55462 | V _S = 30 V, | I _O ≈ 300 mA, | | V _S -10 |) | mV |
| VOH High-level output voltage after switching | | 75462 | See Figure 2 | | V _S -10 | | | my |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, JG, and P packages.

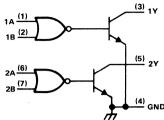
FUNCTION TABLE (EACH DRIVER)

| Α | В | Υ |
|---|---|---------------|
| L | L | L (on state) |
| L | Н | H (off state) |
| Н | L | H (off state) |
| Н | Н | H (off state) |

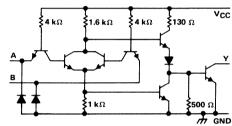
positive logic:

 $Y = A + B \text{ or } \overline{\overline{A}} \, \overline{\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CON | DITIONET | SN55463 | | | SN75463 | | | UNIT |
|------|------------------------------|--------------------------|-----------------------|---------|------------------|-------|---------|------------------|-------|------|
| | PARAMETER | TEST CONDITIONS† | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | UNIT |
| VIK | Input clamp voltage | V _{CC} = MIN, | lj = -12 mA | | -1.2 | - 1.5 | | -1.2 | - 1.5 | > |
| lou | High-level output current | V _{CC} = MIN, | VIH = MIN, | | | 300 | | | 100 | μА |
| ЮН | riigii-iever output current | V _{OH} = 35 V | | | 300 | | | 100 | μΛ | |
| | | V _{CC} = MIN, | $V_{IL} = 0.8 V$, | | 0.25 | 0.5 | | 0.25 | 0.4 | |
| VOL | Low-level output voltage | I _{OL} = 100 mA | | | 0.25 | 0.0 | 0.2 | 0.25 | 0.4 | v |
| VOL | | V _{CC} = MIN, | $V_{IL} = 0.8 V$ | | 0.5 | 0.8 | | 0.5 | 0.7 | · |
| | | I _{OL} = 300 mA | | | 0.5 | | | 0.0 | 0.7 | |
| h | Input current at maximum | V _{CC} = MAX, | $V_1 = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| '' | input voltage | VCC - WAX, | V1 = 0.5 V | | | | | | | |
| ΊΗ | High-level input current | $V_{CC} = MAX,$ | $V_1 = 2.4 V$ | | | 40 | | | 40 | μΑ |
| ηL | Low-level input current | V _{CC} = MAX, | $V_1 = 0.4 V$ | | -1 | -1.6 | | – 1 | - 1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = MAX, | $V_I = 5 V$ | | 8 | 11 | | 8 | 11 | mA |
| ICCL | Supply current, outputs low | V _{CC} = MAX, | V _I = 0 | | 58 | 76 | | 58 | 76 | mA |

 $^{^{\}dagger}$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C

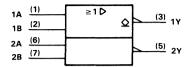
| PARAMETER | | | TEST CON | IDITIONS | MIN , TYP | MAX | UNIT |
|------------------|--|------------------------|--------------------------|-----------------|--------------------|-----|------|
| tPLH | PLH Propagation delay time, low-to-high-level output | | | | 30 | 55 | ns |
| ^t PHL | tPHL Propagation delay time, high-to-low-level output | | lo ≈ 200 mA, | $C_L = 15 pF$, | 25 | 40 | ns |
| tTLH | TLH Transition time, low-to-high-level output | | $R_L = 50 \Omega$, | See Figure 1 | 8 | 25 | ns |
| tTHL | t _{THL} Transition time, high-to-low-level output | | | | 10 | 25 | ns |
| SN55463 | | V _S = 30 V, | I _O ≈ 300 mA, | Vs-1 | 10 | m∨ | |
| Vон | High-level output voltage after switching | SN75463 | See Figure 2 | | V _S -10 | | |



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

SN55464 DUAL PERIPHERAL POSITIVE-NOR DRIVER

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the JG package.

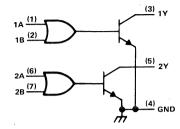
FUNCTION TABLE (EACH DRIVER)

| АВ | Y |
|-----|---------------|
| LL | H (off state) |
| LH | L (on state) |
| H L | L (on state) |
| нн | L (on state) |

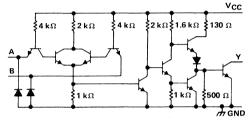
positive logic:

 $Y = \overline{A + B} \text{ or } \overline{A} \overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CONDITIONS† | SN55464 | | 4 | UNIT |
|------|--|---|---------|------|------|------|
| | PARAMETER | TEST CONDITIONS | MIN | TYP‡ | MAX | UNII |
| VIK | Input clamp voltage | $V_{CC} = MIN$, $I_I = -12 \text{ mA}$ | | -1.2 | -1.5 | V |
| ЮН | High-level output current | $V_{CC} = MIN$, $V_{IL} = 0.8 V$, $V_{OH} = 35 V$ | | | 300 | μΑ |
| ., | | $V_{CC} = MIN, V_{IH} = MIN,$ $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.5 | v |
| VOL | Low-level output voltage | $V_{CC} = MIN$, $V_{IH} = MIN$, | | 0.5 | 0.8 | V |
| lį | Input current at maximum input voltage | $V_{CC} = MAX$, $V_I = 5.5 V$ | | | 1 | mA |
| ΊΗ | High-level input current | $V_{CC} = MAX$, $V_{I} = 2.4 V$ | | | 40 | μΑ |
| IIL | Low-level input current | $V_{CC} = MAX$, $V_{I} = 0.4 V$ | | 1 | -1.6 | mA |
| ССН | Supply current, outputs high | $V_{CC} = MAX, V_I = 0$ | | 14 | 19 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = MAX$, $V_I = 5 V$ | | 67 | 85 | mA |

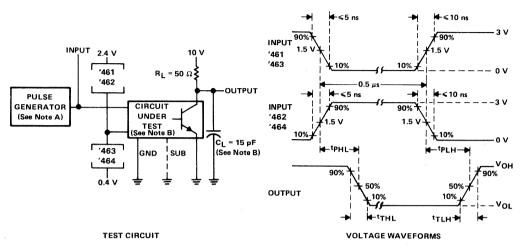
[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25 °C

| | PARAMETER | | TEST CON | IDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|---------|--------------------------|--------------------------|--------------------|--------------------|-----|------|
| t _{PLH} | tpLH Propagation delay time, low-to-high-level output | | | | | 40 | 65 | ns |
| ^t PHL | tpHL Propagation delay time, high-to-low-level output | | I _O ≈ 200 mA, | $C_L = 15 pF$, | | 30 | 50 | ns |
| tTLH | tTLH Transition time, low-to-high-level output | | $R_L = 50 \Omega$, | See Figure 1 | | 8 | 20 | ns |
| ^t THL | tTHL Transition time, high-to-low-level output | | | | | 10 | 20 | ns |
| Si Si | | SN55464 | $V_S = 30 V_{,}$ | I _O ≈ 300 mA, | | V _S -10 |) | mV |
| VOH | High-level output voltage after switching | SN75464 | See Figure 2 | | V _S -10 | | | 1110 |

 $^{^{\}ddagger}$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \,^{\circ}\text{C}$.

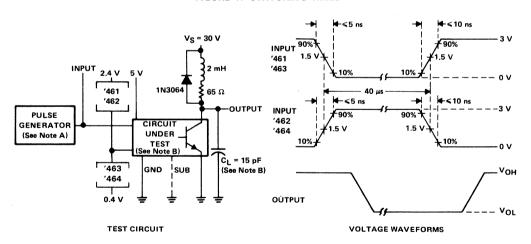
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHZ, Z $_{\rm out}$ \approx 50 $\Omega.$

B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, Z $_0$ = 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST



D3004, JULY 1986

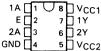
- Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range Up to 24 V
- Low Standby Power Dissipation

description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

The SN75372 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE (TOP VIEW)

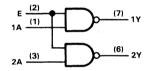


logic symbol†

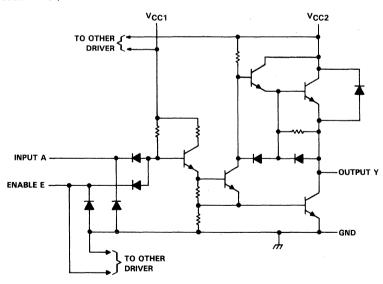


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



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SN75372 DUAL MOSFET DRIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range of VCC1 (see Note 1) | -0.5 V to 7 V |
|--|---------------------|
| Supply voltage range of VCC2 | $-0.5\ V$ to 25 V |
| Input voltage | 5.5 V |
| Peak output current (t _W < 10 ms, duty cycle < 50%): Sink | 500 mA |
| Source | 500 mA |
| Continuous total power dissipation See Dissipa | tion Rating Table |
| Operating free-air temperature range, TA | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|------------------------------------|---|------|-----|------|------|
| Supply voltage, VCC1 | 1 | 4.75 | 5 | 5.25 | V |
| Supply voltage, VCC2 | | 4.75 | 20 | 24 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, VIL | | | | 0.8 | V |
| High-level output current, IOH | | | | -10 | mA |
| Low-level output current, IOL | | | | 40 | mA |
| Operating free-air temperature, TA | | 0 | | 70 | °C |

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

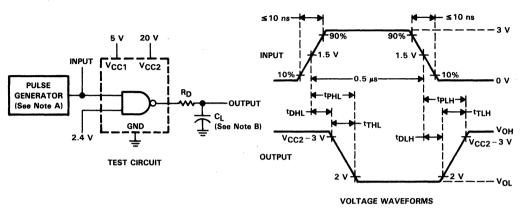
| | PARAMETER | | TEST CONDI | rions | MIN | TYP [†] | MAX | UNIT |
|---------------------|---|----------------|---|-------------------------------------|-----------------------|-----------------------|----------------|------|
| VIK | Input clamp voltage | | I _I = -12 mA | | | | - 1.5 | V |
| Vон | High-level output voltage | | $V_{IL} = 0.8 V$, | $I_{OH} = -50 \mu A$ | | V _{CC2} -0.8 | | V |
| VOH | | | $V_{IL} = 0.8 V,$ | $I_{OH} = -10 \text{ mA}$ | V _{CC2} -2.5 | V _{CC2} -1.8 | | |
| | | | $V_{IH} = 2 V$, | $I_{OL} = 10 \text{ mA}$ | | 0.15 | 0.3 | |
| VOL | Low-level output voltage | | $V_{CC2} = 15 \text{ V to } 24 \text{ V},$ $I_{OL} = 40 \text{ mA}$ | V _{IH} = 2 V, | | 0.25 | 0.5 | ٧ |
| VF | Output clamp diode forward voltage | | $V_{I} = 0,$ | I _F = 20 mA | | | 1.5 | V |
| 11 | Input current at maximus input voltage | m | V _I = 5.5 V | | | | 1 | mA |
| ΊΗ | High-level input current | Any A Any E | V _I = 2.4 V | | | | 40 80 | μΑ |
| ŊĻ | Low-level input current | Any A Any E | V _I = 0.4 V | | | - 1 - 2 | - 1.6 - 3.2 | mA |
| ICC1(H) | Supply current from V _C (both outputs high | 01, | V _{CC1} = 5.25 V, | V _{CC2} = 24 V, | | 2 | 4 | mA |
| I _{CC2(H)} | Supply current from V _C (both outputs high | C2, | All inputs at 0 V, | No load | | | 0.5 | mA |
| ICC1(L) | Supply current from V _C (both outputs low | C1, | V _{CC1} = 5.25 V, | V _{CC2} = 24 V, | | 16 | 24 | mA |
| ICC2(L) | Supply current from V _C both outputs low | 02, | All inputs at 5 V, | No load | | 7 | 13 | mA |
| ICC2(S) | Supply current from V _{C0} standby condition | 02, | $V_{CC1} = 0$, All inputs at 5 V, | V _{CC2} = 24 V, No load | | | 0.5 | mA |

 $^{^{\}dagger}AII$ typical values are at VCC1 $\,=\,5$ V, VCC2 $\,=\,$ 20 V, and TA $\,=\,25\,^{\circ}C.$

switching characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 20 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------|-----|-----|-----|------|
| tDLH Delay time, low-to-high-level output | | | 20 | 35 | ns |
| tDHL Delay time, high-to-low-level output | C _L = 390 pF, | | 10 | 20 | ns |
| t _{TLH} Transition time, low-to-high-level output | $R_{D} = 10 \Omega$ | | 20 | 30 | ns |
| t _{THL} Transition time, high-to-low-level output | See Figure 1 | | 20 | 30 | ns |
| tPLH Propagation delay time, low-to-high-level output | -to-high-level output | | 40 | 65 | ns |
| tpHL Propagation delay time, high-to-low-level output | | 10 | 30 | 50 | ns |

PARAMETER MEASUREMENT INFORMATION

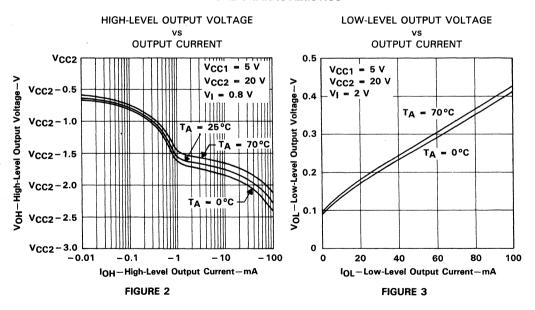


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z $_{out}$ \approx 50 $\Omega.$

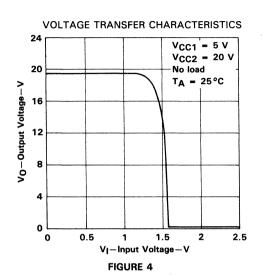
B. C_L includes probe and jig capacitance.

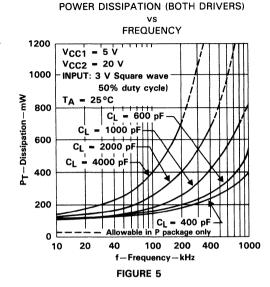
FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

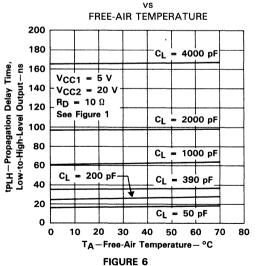


TYPICAL CHARACTERISTICS

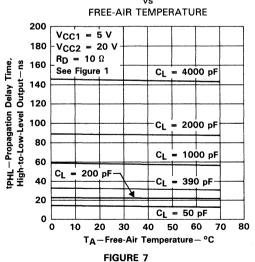




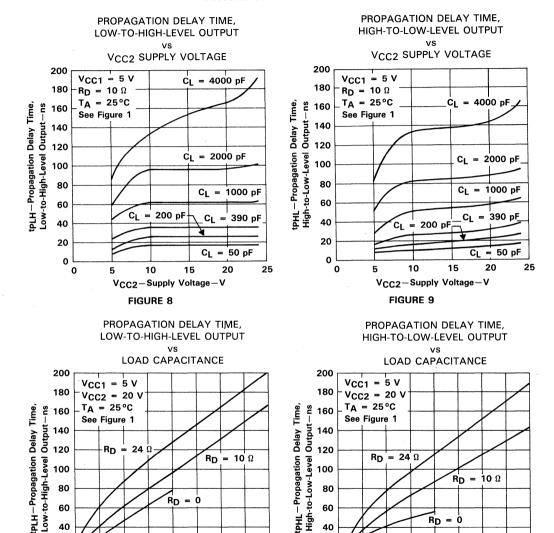
PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT



PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT



TYPICAL CHARACTERISTICS



NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

3000

2000

 $C_L-Load\ Capacitance-pF$

FIGURE 10

1000



4000

20

0

1000

 $R_D = 0$

2000

C_L-Load Capacitance-pF

FIGURE 11

3000

4000

40 20

0

0

APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470- Ω pull-up resistor. The input capacitance (Ciss) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of Ciss and the pull-up resistor is shown in Figure 12(b).

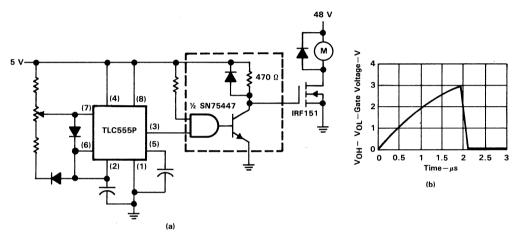


FIGURE 12. POWER MOSFET DRIVE USING SN75447

APPLICATIONS INFORMATION

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

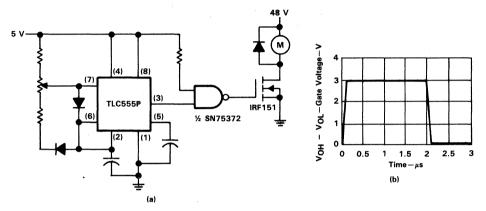


FIGURE 13. POWER MOSFET DRIVE USING SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = VOH - VOL$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$IPK = \frac{(3-0)4(10-9)}{100(10-9)} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a VCC of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 QUAD MOSFET driver should be used.



THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$PT(AV) = PDC(AV) + PC(AV) + PS(AV)$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_{H}t_{H} + P_{L}t_{L}}{T}$$

$$P_{C(AV)} \approx C V_{C}^{2} f$$

$$P_{S(AV)} = \frac{p_{L}t_{L}H + P_{H}L}{T}$$

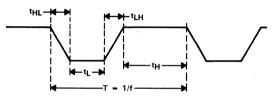


FIGURE 14. OUTPUT VOLTAGE WAVEFORM

where the times are as defined in Figure 14.

 P_L , P_H , P_{LH} , and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$VC = VOH - VOL$$

PS(AV) may be ignored for power calculations at low frequencies.

THERMAL INFORMATION

In the following power calculation, both channels are operating under identical conditions: $V_{OH}=19.2\ V$ and $V_{OL}=0.15\ V$ with $V_{CC1}=5\ V$, $V_{CC2}=20\ V$, $V_{C}=19.05\ V$, $C=1000\ pF$, and the duty cycle =60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values

$$P_{DC(AV)} = \left[(5 \text{ V}) \left(\frac{2 \text{ mA}}{2} \right) + (20 \text{ V}) \left(\frac{0 \text{ mA}}{2} \right) \right] (0.6) + \left[(5 \text{ V}) \left(\frac{16 \text{ mA}}{2} \right) + (20 \text{ V}) \left(\frac{7 \text{ mA}}{2} \right) \right] (0.4)$$

PDC(AV = 47 mW per channel

Power during the charging time of the load capacitance is

$$PC(AV) = (1000 \text{ pF}) (19.05 \text{ V})^2 (0.5 \text{ MHz}) = 182 \text{ mW per channel}$$

Total power for each driver is

$$PT(AV) = 47 \text{ mW} + 182 \text{ mW} = 229 \text{ mW}$$

and total package power is

$$PT(AV) = (229)(2) = 458 \text{ mW}.$$

D3004, SEPTEMBER 1986

- Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range from 5 V to 24 V
- Low Standby Power Dissipation
- V_{CC3} Supply Maximizes Output Source Voltage

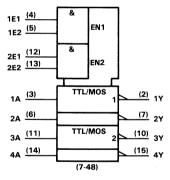
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. The V_{CC3} pin can also be tied directly to V_{CC2} when the source voltage requirements are lower.

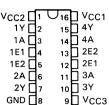
The SN75374 is characterized for operation from 0°C to 70°C.

logic symbol†

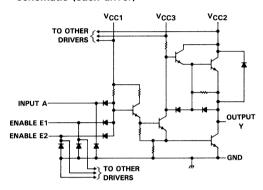


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

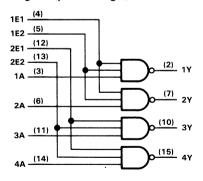
D OR N PACKAGE (TOP VIEW)



schematic (each driver)



logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range of VCC1, (see Note 1) |
|---|
| Supply voltage range of VCC2 |
| Supply voltage range of VCC3 |
| Input voltage |
| Peak output current (tw < 10 ms, duty cycle < 50%): Sink |
| Source 500 mA |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65 °C to 150 °C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------------------|-----|------|------|
| Supply voltage, V _{CC1} | 4.75 | 5 | 5.25 | V |
| Supply voltage, V _{CC2} | 4.75 | 20 | 24 | V |
| Supply voltage, VCC3 | V _{CC2} | 24 | 28 | V |
| Voltage difference between supply voltages: V _{CC3} - V _{CC2} | 0 | 4 | 10 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| High-level output current, IOH | | | - 10 | mA |
| Low-level output current, IOL | | | 40 | mA |
| Operating free-air temperature, T _A | 0 | | 70 | °C |

electrical characteristics over recommended ranges of VCC1, VCC2, VCC3, and operating free-air temperature (unless otherwise noted)

| F | PARAMETER | TEST (| CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|---------------------|--|--|--|-----------------------|-----------------------|----------------|------|
| VIK | Input clamp voltage | $I_{\parallel} = -12 \text{ mA}$ | | | | -1.5 | V |
| Voн | High-level | $V_{CC3} = V_{CC2} + 3 V$ | $V_{IL} = 0.8 \text{ V}, \ I_{OH} = -100 \ \mu\text{A}$ $V_{IL} = 0.8 \text{ V}, \ I_{OH} = -10 \text{ mA}$ | V _{CC2} -1.3 | V _{CC2} -0.1 | | V |
| | output voltage | | $V_{IL} = 0.8 \text{ V}, I_{OH} = -50 \mu\text{A}$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -10 \text{ mA}$ | | V _{CC2} -0.7 | | |
| VOL | Low-level | V _{IH} = 2 V, | I _{OL} = 10 mA | COZ | 0.15 | 0.3 | v |
| VOL | output voltage | $V_{CC2} = 15 \text{ V to } 28 \text{ V},$ | $V_{IH} = 2 V$, $I_{OL} = 40 \text{ mA}$ | | 0.25 | 0.5 | . " |
| VF | Output clamp diode forward voltage | V ₁ = 0, | I _F = 20 mA | | | 1.5 | V |
| lj | Input current at maximum input voltage | V _I = 5.5 V | | | www. | 1 | mA |
| ۱н | High-level Any A input current Any E | V _I = 2.4 V | | | | 40 80 | μА |
| IIL | Low-level Any A input current Any E | V _I = 0.4 V | 4-1 | | - 1 - 2 | - 1.6 - 3.2 | mA |
| ICC1(H) | Supply current from | V _{CC1} = 5.25 V, | V 24 V | | 4 | 8 | |
| I _{CC2(H)} | VCC2, all outputs high | $V_{CC3} = 28 \text{ V},$ No load | | | -2.2 | 0.25 | mA |
| ICC3(H) | Supply current from VCC3, all outputs high | | | | 2.2 | 3.5 | |
| ICC1(L) | Supply current from V _{CC1} , all outputs low | V _{CC1} = 5.25 V, | Voca - 24 V | | 31 | 47 | |
| ICC2(L) | VCC2, all outputs low | $V_{CC3} = 28 \text{ V},$ No load | | | | 2 | mA |
| ICC3(L) | VCC3, all outputs low | 110 1000 | | | 16 | 27 | |
| I _{CC2(H)} | Supply current from VCC2, all outputs high | $V_{CC1} = 5.25 \text{ V},$ $V_{CC3} = 24 \text{ V},$ | V _{CC2} = 24 V, All inputs at 0 V, | | | 0.25 | mA |
| ICC3(H) | Supply current from V _{CC3} , all outputs high | No load | All illputs at 0 V, | | | 0.5 | |
| ICC2(S) | Supply current from V _{CC2} , standby condition | V _{CC1} = 0, V _{CC3} = 24 V, | V _{CC2} = 24 V, All inputs at 0 V, | | | 0.25 | mA |
| ICC3(S) | Supply current from VCC3, standby condition | VCC3 = 24 V, No load | All lilputs at U V, | | | 0.5 | mA |

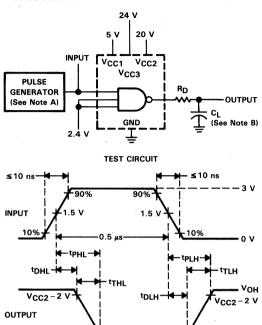
 $^{^{\}dagger}$ All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25 °C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

switching characteristics, VCC1 = 5 V, VCC2 = 20 V, VCC3 = 24 V, $T_A = 25 ^{\circ}\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|-----|-----|-----|------|
| tDLH Delay time, low-to-high-level output | | | 20 | 30 | ris |
| tDHL Delay time, high-to-low-level output | $C_L = 200 pF$, | | 10 | 20 | ns |
| t _{TLH} Transition time, low-to-high-level output | $R_D = 24 \Omega$ | | 20 | 30 | ns |
| t _{THL} Transition time, high-to-low-level output | See Figure 1 | | 20 | 30 | ns |
| tpLH Propagation delay time, low-to-high-level output | See Figure 1 | 10 | 40 | 60 | ns |
| tpHL Propagation delay time, high-to-low-level output | | 10 | 30 | 50 | ns |



PARAMETER MEASUREMENT INFORMATION



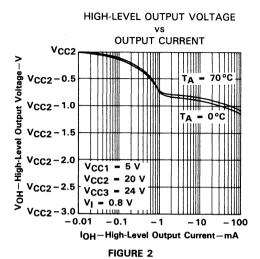
VOLTAGE WAVEFORMS

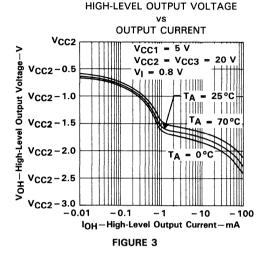
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50~\Omega$. B. C_L includes probe and jig capacitance.

2

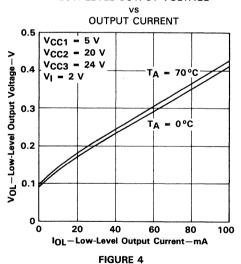
FIGURE 1. SWITCHING TIMES, EACH DRIVER

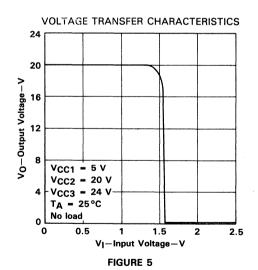
TYPICAL CHARACTERISTICS



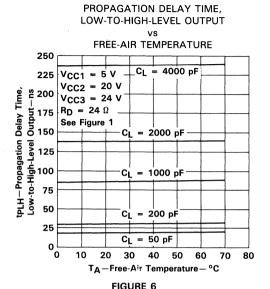


LOW-LEVEL OUTPUT VOLTAGE



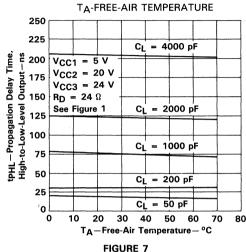


TYPICAL CHARACTERISTICS



HIGH-TO-LOW-LEVEL OUTPUT

PROPAGATION DELAY TIME.



PROPAGATION DELAY TIME.

LOW-TO-HIGH-LEVEL OUTPUT vs VCC2 SUPPLY VOLTAGE

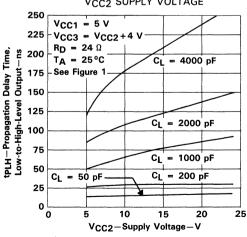
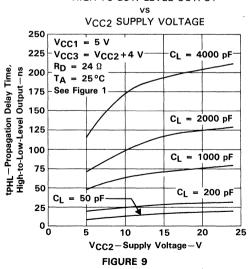
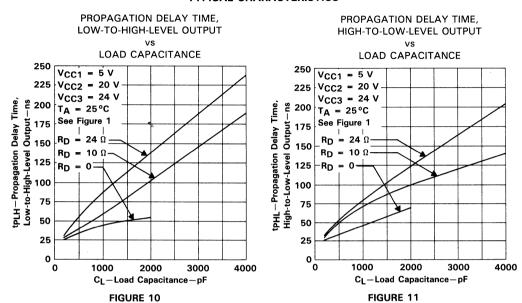


FIGURE 8

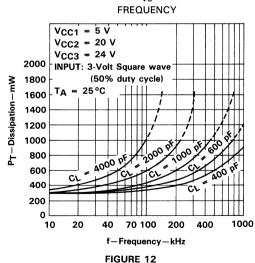
PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT



TYPICAL CHARACTERISTICS



POWER DISSIPATION (ALL DRIVERS)



NOTE: For $R_D = 0$, operation with $C_L > 2000 \ pF$ violates absolute maximum current rating.

APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470- Ω pull-up resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pull-up resistor is shown in Figure 13(b).

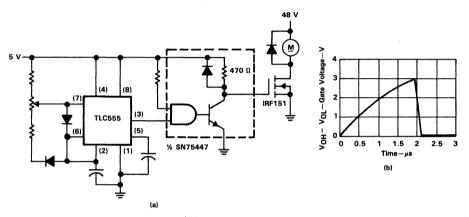


FIGURE 13. POWER MOSFET DRIVE USING SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

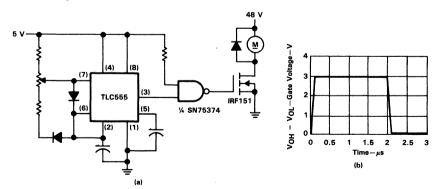


FIGURE 14. POWER MOSFET DRIVE USING SN75374



APPLICATIONS INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{T_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = VOH - VOL$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

$$IPK = \frac{(3-0)4(10-9)}{100(10-9)} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a VCC of 5 V, and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$PT(AV) = PDC(AV) + PC(AV) + PS(AV)$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_{H}t_{H} + P_{L}t_{L}}{T}$$

$$PC(AV) \approx C V^2C f$$

$$P_{S(AV)} = \frac{p_{LH}t_{LH} + P_{HL}t_{HL}}{T}$$

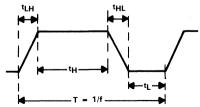


FIGURE 15. OUTPUT VOLTAGE WAVEFORM

where the times are as defined in Figure 15.

THERMAL INFORMATION

PL, PH, PLH, and PHL are the respective instantaneous levels of power dissipation, C is the load capacitance. VC is the voltage across the load capacitance during the charge cycle shown by the equation

$$VC = VOH - VOL$$

PS(AV) may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, $V_{OH} = 19.9 \text{ V}$ and $V_{OL} = 0.15 \text{ V}$ with $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 20 \text{ V}$, $V_{CC3} = 24 \text{ V}$, $V_{C} = 19.75 \text{ V}$, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for $C_{L} < 2000 \text{ pF}$, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, ICC2 is negligible and can be ignored.

On a per-channel basis using data sheet values

$$\begin{split} P_{DC(AV)} = & \left[(5 \text{ V}) \left(\frac{4 \text{ mA}}{4} \right) + (20 \text{ V}) \left(\frac{-2.2 \text{ mA}}{4} \right) + (24 \text{ V}) \left(\frac{2.2 \text{ mA}}{4} \right) \right] (0.6) + \\ & \left[(5 \text{ V}) \left(\frac{31 \text{ mA}}{4} \right) + (20 \text{ V}) \left(\frac{0 \text{ mA}}{4} \right) + (24 \text{ V}) \left(\frac{16 \text{ mA}}{4} \right) \right] (0.4) \end{split}$$

PDC(AV = 58.2 mW per channel)

Power during the charging time of the load capacitance is

$$PC(AV) = (1000 \text{ pF}) (19.75 \text{ V})^2 (0.2 \text{ MHz}) = 78 \text{ mW per channel}$$

Total power for each driver is

$$PT(\Delta V) = 58.2 \text{ mW} + 78 \text{ mW} = 136.2 \text{ mW}$$

The total package power is

$$PT(\Delta V) = (136.2) (4) = 544.8 \text{ mW}$$

D2848, FEBRUARY 1985-REVISED NOVEMBER 1989

- Saturating Outputs With Low On Resistance
- Very Low Standby Power . . . 53 mW Max
- High-Impedance MOS- or TTL-Compatible Inputs
- Standard 5-V Supply Voltage
- No Output Glitch During Power-Up or Power-Down
- Output Clamp Diodes for Transient Suppression
- 2-W Power Package . . . 60 °C/W R_{θ,IA}
- 600-mA Output Current
- 35-V Switching Voltage

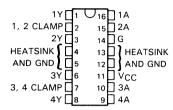
description

The SN75435 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. It features four inverting open-collector drivers with a common enable input that, when taken low, disables all four outputs. Each driver is protected against load shorts with its own latching over-current shutdown circuitry, which will turn the output off when a load short is detected. A short on one load will not affect operation of the other three drivers. The latch for the shutdown will hold the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the overcurrent shutdown to allow load capacitance of up to 5 nF at 35 V.

Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

The SN75435 is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

NE DUAL-IN-LINE PACKAGE (TOP VIEW)



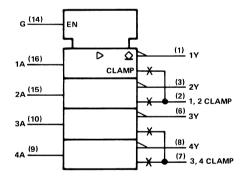
FUNCTION TABLE (EACH NAND DRIVER)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | G | Y |
| L | Х | Н |
| X | L | н |
| н | Н | L |

H = high level, L = low level

X = irrelevant

logic symbol†

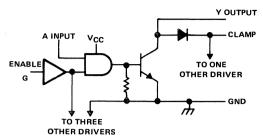


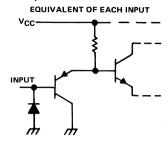
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)

schematic of inputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage range of VCC (see Note 1) | 7 | ٧ |
|--|------|---|
| Input voltage | 5.5 | ٧ |
| Output supply voltage | 70 | ٧ |
| Output diode clamp current | | |
| Continuous total power dissipation | | |
| at (or below) 25 °C free-air temperature (see Note 2) | j m\ | Ν |
| Operating free-air temperature range, TA | 70° | С |
| Storage temperature range – 65 °C to 1! | 50° | С |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 60° | С |

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25 °C free-air temperature, derate linearly at the rate of 16.6 mW/ °C.

recommended operating conditions

| , | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | ٧ |
| Output voltage | | | 35 | ٧ |
| Output current | | | 600 | mA |
| Load capacitance (See Figure 3) | | | 35 | nF |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|---|--|-----|--------------|----------|------|
| VIK | Input clamp voltage | V _{CC} = 4.75 V, | I _I = -12 mA | | -0.9 | -1.5 | V |
| ЮН | High-level output current | V _{CC} = 4.75 V, V _{IL} = 0.8 V, | V _{IH} = 2 V, V _{OH} = 70 V | | | 100 | μΑ |
| VOL | Low-level output voltage | V _{CC} = 4.75 V, V _{IH} = 2 V | I _{OL} = 300 mA I _{OL} = 600 mA | | 0.25 0.55 | 0.5 1 | V |
| VR | Output clamp diode reverse voltage | V _{CC} = 4.75 V, | I _R = 100 μA | 70 | 100 | | V |
| ٧F | Output clamp diode forward voltage | IF = 600 mA | | 1 | 1.2 | 1.6 | V |
| liH. | High-level input current | V _{CC} = 5.25 V, | V ₁ = 5.25 V | | 0.01 | 10 | μΑ |
| IIL | Low-level input current | $V_{CC} = 5.25 \text{ V},$ | V _I = 0.8 V | | -0.5 | - 10 | μΑ |
| | Over-current shutdown current | V _{CC} = 4.75 V to 5.25 V | | 650 | 850 | | mA |
| ІССН | Supply current, outputs high | V _{CC} = 5.25 V, | V _I = 0 | | 6 | 10 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 \text{ V},$ | V _I = 5 V | | 55 | 75 | mA |

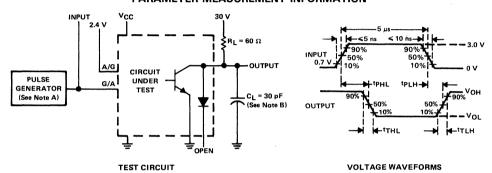
 $^{^{\}dagger}$ All typical values are at V_{CC} = 5 V, T_{A} = 25 °C.



switching characteristics, VCC = 5 V, TA = 25°C

| | PARAMETER | TEST CONDITIONS | MIN TYP MAX | UNIT |
|------------------|--|---------------------------------|---------------------|------|
| tPLH | Propogation delay time, low-to-high-level output | | 750 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $C_L = 30 pF, R_L = 60 \Omega,$ | 750 | ns |
| ^t TLH | Transition time, low-to-high-level output | See Figure 1 | 200 | ns |
| tTHL | Transition time, high-to-low-level output | | 200 | ns |
| Voн | High-level output voltage after switching | See Figure 2 | V _S - 10 | mV |

PARAMETER MEASUREMENT INFORMATION

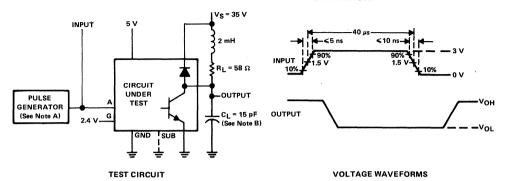


NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω . B. C_L include probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

RECOMMENDED OPERATING CONDITIONS

MAXIMUM OUTPUT SUPPLY VOLTAGE

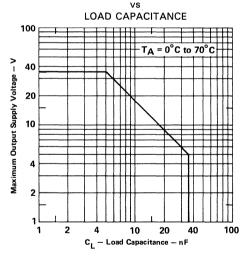
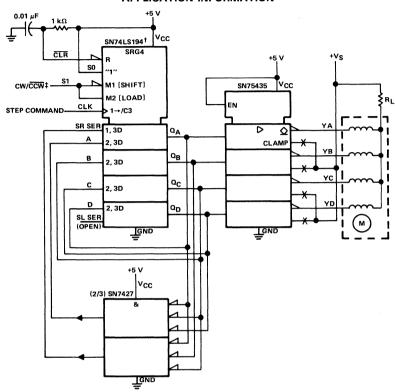
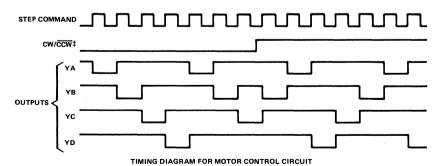


FIGURE 3

APPLICATION INFORMATION



4-WINDING STEPPER MOTOR CONTROL CIRCUIT



[†]The SN74LS194 is a universal shift register with both shift-right and shift-left capability. In this application SO (pin 9) is wired high and only the shift-right and parallel-load modes are utilized. The logic symbol shown above has been simplified to show only the utilized modes.

[‡]This signal is CW/CCW or CW/CCW depending on motor winding.



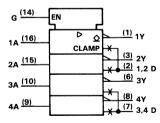
D2806, DECEMBER 1986

- Saturating Outputs With Low On-State Resistance
- High-Impedance Inputs Compatible With CMOS. MOS. and TTL Levels
- Very Low Standby Power . . . 21 mW Maximum
- High-Voltage Outputs . . . 70 V Min
- No Output Glitch During Power Up or Power Down
- No Latch-Up Within Recommended Operating Conditions
- Output Clamp Diodes for Transient Suppression
- 2-W Power Package

description

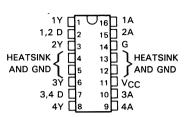
The SN75436, SN75437A, and SN75438 quadruple peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each device features four inverting open-collector outputs with a common enable input that, when taken low, disables all four outputs. The envelope of I-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NE PACKAGE (TOP VIEW)

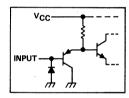


FUNCTION TABLE (each NAND driver)

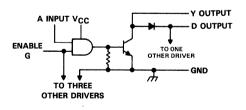
| INPUTS | | OUTPUT |
|--------|---|--------|
| Α | G | Υ |
| Н | Н | L |
| L | Х | Н |
| х | Ł | 1 н |

H = high level, L = low level, X = irrelevant

equivalent schematic of each input



logic diagram (positive logic, each driver)



SELECTION GUIDE

| FEATURE | SN75436 | SN75437A | SN75438 | UNIT |
|---|---------|----------|---------|------|
| Maximum recommended output current | 0.5 | 0.5 | 1 | Α |
| Maximum VOL at maximum IOL | 0.5 | 0.5 | 1 | ٧ |
| Maximum recommended output supply voltage in an inductive switching circuit, Vs | 50 | 35 | 35 | ٧ |

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN75436, SN75437A, SN75438 QUADRUPLE PERIPHERAL DRIVERS

absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage, VCC |
|---|
| Input voltage |
| Output current: SN75436, SN75437A (see Note 1) |
| SN75438 |
| Output clamp diode current |
| Output voltage (off-state) |
| Continuous total power dissipation at (or below) 25 °C free-air temperature |
| (see Note 2) |
| Operating free-air temperature range, T _A |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds |

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation ratings.

2. For operation above 25 °C free-air temperature, derate linearly to 1328 mW at 70 °C at the rate of 16.6 mW/°C.

recommended operating conditions

| D. D. L. L. L. L. L. L. L. L. L. L. L. L. L. | ; | SN75436 | | SN75437A | | SN75438 | | | UNIT | |
|---|------|---------|------|----------|-----|---------|------|-----|------|------|
| PARAMETER | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | 4.75 | 5 | 5.25 | ٧ |
| Output current, IOL | | | 0.5 | | | 0.5 | | | 1 | Α |
| Output supply voltage in inductive switching circuit (see Figure 2), V _S | | | 50 | | | 35 | | | 35 | ٧ |
| High-level input voltage, VIH | 2 | | | 2 | | | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | | | 0.8 | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CO | ONDITIONS | | SN75436 SN75437A | | | SN75438 | | |
|-------------------|------------------------------------|--|--|-----|---------------------|-------|-----|------------------|------|-----|
| | | | | MIN | TYP [†] | MAX | MIN | TYP [†] | MAX | |
| VIK | Input clamp | $V_{CC} = 4.75 V$, | I _I = -12 mA | | -0.9 | - 1.5 | | -0.9 | -1.5 | ٧ |
| Іон, | High-level output current | $V_{CC} = 4.75 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | V _{IH} = 2 V, V _{OH} = 70 V | | 1 | 100 | | 1 | 100 | μΑ |
| | | | I _{OL} = 250 mA | | 0.14 | 0.25 | | 0.14 | 0.25 | |
| V - | Landana and and and and | $V_{CC} = 4.75 V$, | I _{OL} = 500 mA | | 0.28 | 0.5 | | 0.28 | 0.5 | ·v |
| VOL | Low-level output voltage | V _{IH} = 2 V | I _{OL} = 750 mA | | | | | 0.42 | 0.75 | \ \ |
| | | | I _{OL} = 1 A | | | | | 0.60 | 1 | |
| V _{R(K)} | Output clamp diode reverse voltage | V _{CC} = 4.75 V, | I _R = 100 μA | 70 | 100 | | 70 | 100 | | ٧ |
| 1/ | Output clamp diode | IF = 500 mA | | | 1 | 1.6 | 1 | 1 | 1.6 | |
| V _{F(K)} | forward voltage | I _F = 1 A | | | | | | 1.2 | 2 | V |
| ΊΗ | High-level input current | $V_{CC} = 5.25 \text{ V},$ | V _I = 5.25 V | | 0.1 | 10 | | 0.1 | 10 | μΑ |
| IL | Low-level input current | $V_{CC} = 5.25 \text{ V},$ | V _I = 0.8 V | | -0.25 | - 10 | | -0.25 | - 10 | μΑ |
| Іссн | Supply current, outputs high | V _{CC} = 5.25 V, | V _I = 0 | | 1 | 4 | , | 1 | 4 | mA |
| ICCL | Supply current, outputs low | V _{CC} = 5.25 V, | V _I = 5 V | | 45 | 65 | | 45 | 65 | mA |

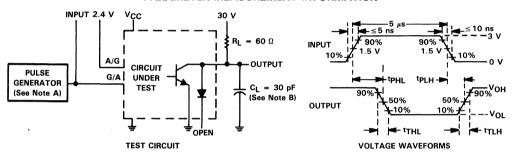
 $^{^{\}dagger}$ All typical values are at VCC = 5 V, TA = 25 °C.



switching characteristics, VCC = 5 V, TA = 25 °C

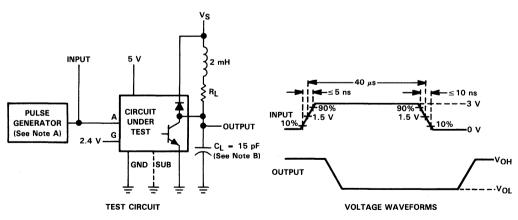
| | PARAMETE | R | TEST CO | NDITIONS | MIN | TYP | MAX | UNIT |
|------|---|------------------------|---|--|---------------------|------|------|------|
| tPLH | Propagation delay time, lov | v-to-high-level output | | | | 1950 | 5000 | ns |
| tPHL | Propagation delay time, hig | h-to-low-level output | $C_L = 30 pF$, | $R_L = 60 \Omega$, | | 150 | 500 | ns |
| tTLH | TLH Transition time, low-to-high-level output | | See Figure 1 | | | 40 | | ns |
| tTHL | Transition time, high-to-lov | v-level output | | | | 36 | | ns |
| | High-level output voltage, after switching | SN75436 | $V_S = 50 \text{ V},$ $R_L = 100 \Omega,$ | I _O ≈ 500 mA, See Figure 2 | V _S - 10 | | | mV |
| Vон | | SN75437A | $V_S = 35 \text{ V},$ $R_L = 70 \Omega,$ | I _O ≈ 500 mA, See Figure 2 | V _S -10 | | | mV |
| | | SN75438 | $V_S = 35 \text{ V},$ $R_L = 35 \Omega,$ | l _O ≈ 1 A, See Figure 2 | V _S - 10 | | | mV |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_0 = 50 Ω .
 - B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS



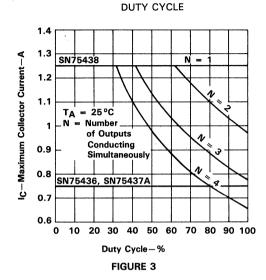
- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_0 = 50 Ω .
 - B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

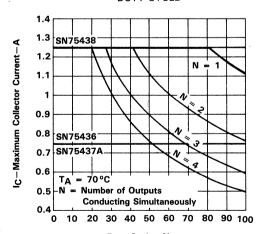


PARAMETER MEASUREMENT INFORMATION

MAXIMUM COLLECTOR CURRENT vs



MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE



Duty Cycle—%
FIGURE 4

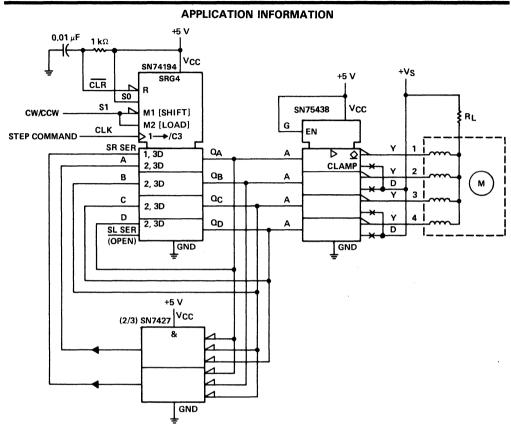
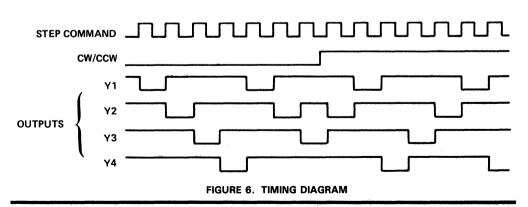


FIGURE 5. 4-WINDING STEPPER MOTOR CONTROL CIRCUIT





D3116. MAY 1988 - REVISED NOVEMBER 1989

- 1.3-A Current Capability Each Channel
- Saturating Outputs With Low On-State Resistance
- Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input
- Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors
- High-Impedance Inputs Compatible With TTL or CMOS Levels
- Very Low Standby Power . . . 10 mW Typ
- 50-V Noninductive Switching Voltage Capability
- 40-V Inductive Switching Voltage Capability
- Output Clamp Diodes for Inductive Transient Protection
- 2-W Power Package

description

The SN75439 quadruple peripheral driver is designed for use in systems requiring high current. high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

The SN75439 is characterized for operation from 0°C to 70°C.

NE PACKAGE (TOP VIEW)

| 1Y [| ſī | U16 1A |
|------------|----|------------------|
| 1, 2D | 2 | 15 2A |
| 2Y 🗀 | 3 | 14 🗍 \overline G |
| HEATSINK) |]4 | 13 \ HEATSINK |
| AND GND (| 5 | 12 AND GND |
| 3Y 🗀 | 6 | 11 🗆 VCC |
| 3, 4D 🗀 | 7 | 10∏ 3A |
| 4Y [| 8 | 9∏ 4A |

FUNCTION TABLES

(Each Channel 1 or Channel 4 Driver)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | G | Y |
| Н | L | L |
| L | Х | н |
| x | н | н |

(Each Channel 2 or Channel 3 Driver)

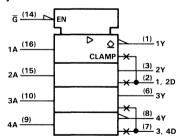
| ſ | INP | UTS | OUTPUT |
|---|-----|-----|--------|
| ľ | Α | G | Y |
| ľ | L | L | L |
| | Н | Х | н |
| | Х | Н | Н |

H = high level

L = low level

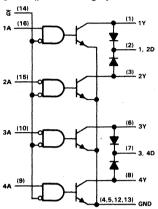
X = irrelevant

logic symbol†

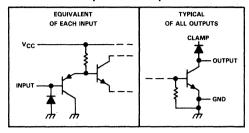


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage range, V _{CC} (see Note 1) |
|---|
| Input voltage, V _I |
| Output voltage range, VO0.3 V to 52 V |
| Output voltage, VO (inductive load) |
| Output clamp-diode terminal voltage range, VOK |
| Input current, I ₁ |
| Peak sink output current, I _{OM} (nonrepetitive, t _W ≤ 0.1 ms) (see Note 2) 1.5 A |
| (repetitive, t _w ≤ 10 ms, duty cycle ≤ 50%) 1.4 A |
| Continuous sink output current, IO (see Note 2) |
| Peak output clamp diode current, I _{OKM} (nonrepetitive, t _W ≤ 0.1 ms) (see Note 2) 1.5 A |
| (repetitive, $t_W \le 10$ ms, duty cycle $\le 50\%$) 1.3 A |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) 2075 mW |
| Continuous total dissipation at (or below) 65°C case temperature (see Note 3) 5000 mW |
| Operating case or virtual junction temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. All voltage values are with respect to the network ground terminal (unless otherwise specified).

- 2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
- 3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

| | MI | NO! | M MAX | UNIT |
|---|------|-----|--------|------|
| Supply voltage, V _{CC} | 4.7 | 5 | 5 5.25 | V |
| Output supply voltage in inductive switching circuit, VS (see Figure 2) | | | 40 | V |
| High-level input voltage, VIH | | 2 | 5.25 | V |
| Low-level input voltage, V _{IL} | -0.3 | j† | 0.8 | V |
| Low-level output current, IOL | | | 1.3 | Α |
| Operating free-air temperature, TA | | 0 2 | 5 70 | °C |

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.



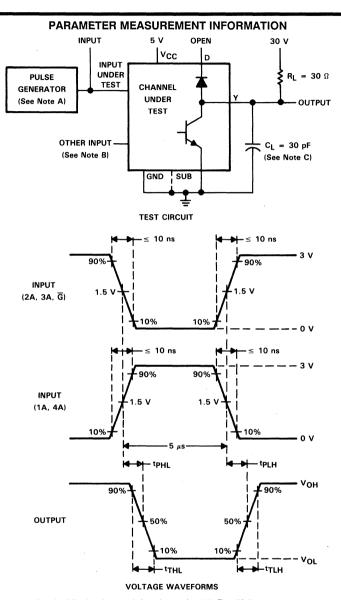
electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

| | PARAMETER | TEST CONDITION | S | MIN | TYP | MAX | UNIT |
|-------------------|--|-------------------------------------|---------------------------------|-----|------|------|------|
| VIK | Input clamp voltage | I _I = -12 mA | | | -0.9 | -1.5 | V |
| | | I _{OL} = 0.5 A | | | 0.2 | 0.35 | |
| VOL | Low-level output voltage | I _{OL} = 1 A | See Note 4 | | 0.4 | 0.7 | ٧ |
| | | I _{OL} = 1.3 A | | | 0.5 | 0.9 | |
| | | IF = 0.5 A | | | 1.1 | 1.9 | |
| V _{F(K)} | Output clamp diode forward voltage | IF = 1 A | See Note 4 | | 1.3 | 2.2 | ٧ |
| , , | | IF = 1.3 A | | | 1.4 | 2.4 | |
| Юн | High-level output current | VOH = 50 V, | V _{OK} = 50 V | | | 100 | μА |
| ΊΗ | High-level input current | VI = VIH | | | | 10 | μА |
| IIL | Low-level input current | $V_1 = 0 \text{ to } 0.8 \text{ V}$ | | | | -10 | μΑ |
| I _{R(K)} | Output clamp-diode reverse current (at Y output) | V _R = 50 V, | V _O = 0 | | | 100 | μΑ |
| | \$2 \tag{2.000} | All outputs at high level (off) | | | 2 | 8 | |
| loo. | Supply current | All outputs at low level (on) | | | 140 | 200 | mA |
| Icc | Supply current | Two outputs at high level (off) and | outputs at high level (off) and | | | 110 | IIIA |
| | | two outputs at low level (on) | | | 70 | . 10 | |

† All typical values are at $V_{CC}=5$ V, $T_{A}=25^{\circ}$ C. NOTE 4: These parameters must be measured using pulse techniques, $t_{W}=1$ ms, duty cycle $\leq 10\%$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

| PARAMETER | | TEST CO | NDITIONS | MIN TYP | MAX | UNIT |
|------------------|--|--|---------------------------|---------------------|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | | 1500 | | ns |
| tPHL | Propagation delay time, high-to-low-level output | lo∟≈1 A, | C _L = 30 pF, | 100 | | ns |
| tTLH | Transition time, low-to-high-level output | $R_L = 30 \Omega$, | See Figure 1 | 170 | | ns |
| [†] THL | Transition time, high-to-low-level output | | | 50 | | ns |
| Vон | High-level output voltage (after switching inductive load) | $V_S = 40 \text{ V},$ $R_L = 31 \Omega,$ | lo≈1.3 A, See Figure 2 | V _S -100 | | mV |



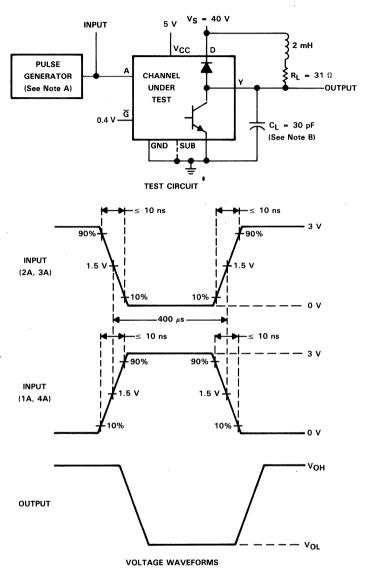
NOTES: A. The pulse generator has the following characteristics: duty cycle $\leq 1\%, Z_0 = 50 \Omega$.

- B. Enable input \overline{G} is at 0 V if input A is used as the switching input. When \overline{G} is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
- C. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS



PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: duty cycle \leq 1%, Z_0 = 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 2. OUTPUT LATCH-UP TEST



APPLICATION INFORMATION SN75439 G I (14)FOUR-1A (16) PHASE STEPPER MOTOR (2) 11, 2D DATA LINES (3) 2Y FROM (15) MICROPROCESSOR (6) 3Y (10)(8) 4A (9) (4,5,12,13) GND **WAVEFORMS**

FIGURE 3. FULL-STEP FOUR-PHASE STEPPER MOTOR DRIVER

SN75446 THRU SN75449 **DUAL PERIPHERAL DRIVERS**

D2481, DECEMBER 1978-REVISED DECEMBER 1989

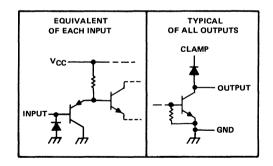
- **Very Low Power Requirements**
- **Very Low Input Current**
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- **Output Clamp Diodes for Transient** Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

description

Series SN75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diodeclamped inputs as well as high-current, highvoltage inductive-clamp diodes on the outputs.

Series SN75446 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



D OR P PACKAGE (TOP VIEW)

| s□ | 1 | U 8 | □vcc |
|-------|---|------------|-------|
| 1A 🗌 | 2 | 7 |] 2A |
| 1Y 🗌 | 3 | |] 2Y |
| GND [| 4 | 5 | CLAMP |

FUNCTION TABLES

SN75446 (EACH AND DRIVER)

| INP | JTS | OUTPUT | | |
|-----|-----|--------|--|--|
| A S | | Y | | |
| Н | Н | Н | | |
| L | Х | L | | |
| Х | L | L | | |

SN75447 (EACH NAND DRIVER)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | S | Y |
| Н | Н | L |
| L | Х | н |
| x | L | н |

SN75448 (EACH OR DRIVER)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | S | Y |
| Н | Х | Н |
| Х | Н | н |
| L | L | L |

SN75449 (EACH NOR DRIVER)

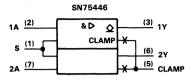
| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | S | Υ |
| Н | Х | L |
| Х | Н | L |
| L. | L | H |

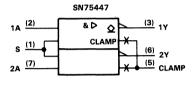
H = high level

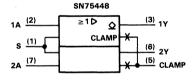
L = low level X = irrelevant

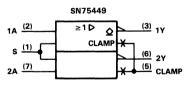
SN75446 THRU SN75449 DUAL PERIPHERAL DRIVERS

logic symbols†



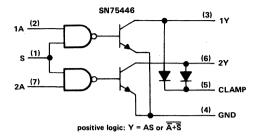


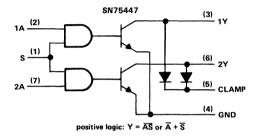


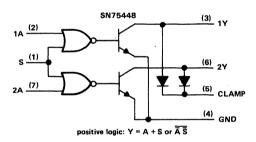


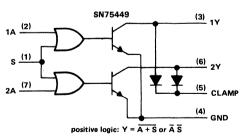
[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) | ٧ |
|---|----|
| Input voltage | ٧ |
| Output current (see Note 2) | ıA |
| Output clamp diode current | ıA |
| Continuous total power dissipation See Dissipation Rating Tab | le |
| Operating free-air temperature range, T _A | ,C |
| Storage temperature range | ,C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | ,C |

NOTES: 1. Voltage values are with respect to network ground terminal.

 Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING | |
|---------|---------------------------------------|---------------------------------|---------------------------------------|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | |
| P | 1000 mW | 8.0 mW/°C | 640 mW | |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, V _{IL} | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

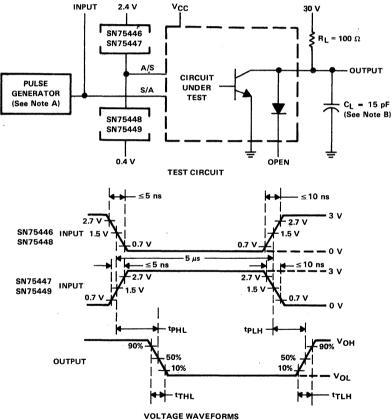
electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | | TEST C | ONDITIONS | MIN | TYP [†] | MAX | UNIT |
|---------------------|------------------------------------|--|--|--------------------------|-----|------------------|------|------|
| VIK | Input clamp voltage | | I₁ = −12 mA | | | 0.9 | -1.5 | ٧ |
| ЮН | High-level output current | $V_{CC} = 4.75 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | V _{IH} = 2 V, V _{OH} = 70 V | | 1 | 100 | μΑ | |
| | | | V _{CC} = 4.75 V, | I _{OL} = 100 mA | | 0.10 | 0.3 | |
| VOL | Low-level output voltage | | $V_{IH} = 2 V$ | I _{OL} = 200 mA | | 0.22 | 0.45 | v |
| \ VOL | Low-level output voltage | | V _{II} = 0.8 V | I _{OL} = 300 mA | | 0.45 | 0.65 | · |
| | | | VIL = 0.8 V | I _{OL} = 350 mA | | 0.55 | 0.75 | |
| V _(BR) C | Output breakdown voltage | | $V_{CC} = 4.75 V$, | $I_{OH} = 100 \mu A$ | 70 | 100 | | V |
| V _{R(K)} | Output clamp diode reverse voltage | | $V_{CC} = 4.75 V,$ | I _R = 100 μA | 70 | 100 | | ٧ |
| V _{F(K)} | Output clamp diode forward voltage | | $V_{CC} = 4.75 V$, | I _F = 350 mA | 0.6 | 1.2 | 1.6 | V |
| ΊΗ | High-level input current | | $V_{CC} = 5.25 \text{ V},$ | V _I = 5.25 V | | 0.01 | 10 | μΑ |
| 1 | Low-level input current | A input | $V_{CC} = 5.25 V,$ | V: - 0 9 V | | -0.5 | - 10 | |
| l IIL | | Strobe S | | V = 0.6 V | | - 1 | - 20 | μΑ |
| | | SN75446 | | V _I = 5 V | | 11 | 18 | mA |
| , | Supply current, outputs high | SN75447 | 1,, 505,4 | V _I = 0 | | 11 | 18 | |
| Іссн | Supply current, outputs high | SN75448 | $V_{CC} = 5.25 \text{ V}$ | V _I = 5 V | | 18 | 25 | |
| | | SN75449 | | V ₁ = 0 | | 18 | 25 | |
| | | SN75446 | | V ₁ = 0 | | 11 | 18 | |
| | Summits assument assets the last | SN75447 | V F 25 V | V _I = 5 V | | 11 | 18 | mA |
| CCL | Supply current, outputs low | SN75448 | V _{CC} = 5.25 V | V _I = 0 | | 18 | 25 | |
| | | SN75449 | | V _I = 5 V | | 18 | 25 | |

switching characteristics, VCC = 5 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|--|-----------------------|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | | 300 | 750 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $C_{L} = 15 \text{ pF, } R_{L} = 100 \Omega,$ | | 200 | 500 | ns |
| [†] TLH | Transition time, low-to-high-level output | See Figure 1 | | 50 | 100 | ns |
| tTHL | Transition time, high-to-low-level output | | | 50 | 100 | ns |
| Vон | High-level output voltage after switching | V _S = 55 V, I _O ≈300 mA, See Figure 2 | V _S -0.018 | | | V |

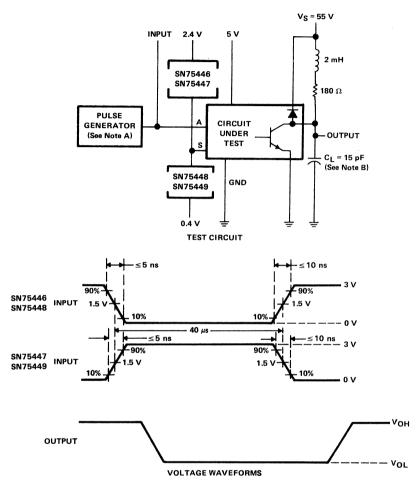
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics; PRR = 100 kHz, Z_{out} = 50 Ω . B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω .

B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

SN75465 THRU SN75469 DARLINGTON TRANSISTOR ARRAYS

D2625, DECEMBER 1976-REVISED SEPTEMBER 1986

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2005A, ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively, for Commercial Temperature Range

| (TOP VIEW) | | | | | | |
|------------|---|---|-----------------|---|-----|--|
| 1B | П | 1 | U ₁₆ | D | 1C | |
| 2B | ₫ | 2 | 15 | Б | 2C | |
| 3В | D | 3 | 14 | Б | 3C | |
| 4B | | 4 | 13 | D | 4C | |
| 5B | Ц | 5 | 12 | D | 5C | |
| 6В | | 6 | 11 | | 6C | |
| 7B | Ц | 7 | 10 | þ | 7C | |
| Ε | | 8 | 9 | | СОМ | |

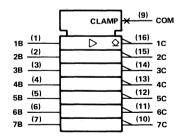
D OR N PACKAGE

description

The SN75465, SN75466, SN75467, SN75468, and SN75469 are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

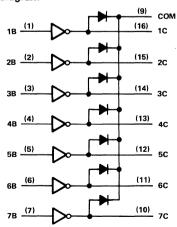
The SN75465 has a $1050-\Omega$ series base resistor and is especially designed for use with TTL where higher current is required and loading of the driving source is not a concern. The SN75466 is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The SN75467 is specifically designed for use with 14- to 25-V P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a $2700-\Omega$ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a $10.5-k\Omega$ series base resistor to allow its operation directly from CMOS or P-MOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468 and the required voltage is less than that required by the SN75467.

logic symbol†

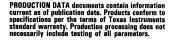


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

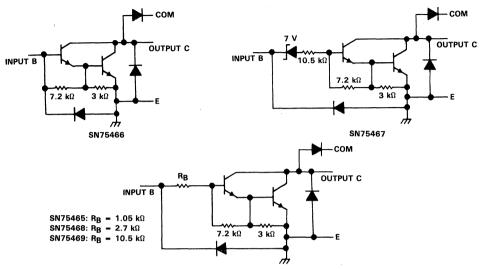


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schematics (each Darlington pair)



SN75465, SN75468, SN75469

All resistor values shown are nominal.

absolute maximum ratings at 25 °C free-air temperature (unless otherwise noted)

| Collector-emitter voltage |
|---|
| Input voltage (see Note 1): SN75465 |
| SN75467, SN75468, SN75469 |
| Peak collector current (see Figures 14 and 15) |
| Output clamp diode current |
| Total emitter-terminal current |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, T _A |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| , | DADAMETED | TEST | | TEGT CONDITIONS | | | N7546 | 5 | UNIT |
|----------------------|--------------------------|--------|---------------------------------|-------------------------|------------------------|-----|-------|-----|----------|
| | PARAMETER | FIGURE | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
| 1 | Collector cutoff current | 1 | V _{CE} = 100 V, | I _I = 0 | | | | 50 | μΑ |
| ICEX | Collector cutori current | | V _{CE} = 100 V, | lլ = 0, | T _A = 70 °C | | | 100 | μΑ |
| I(off) | Off-state input current | 3 | V _{CE} = 100 V, | $I_C = 500 \mu A$, | T _A = 70 °C | 50 | 65 | | μΑ |
| l _į | Input current | 4 | V _I =3 V | | | | 1.5 | 2.4 | mA |
| V _{I(on)} | On-state input voltage | 5 | V _{CE} = 2 V, | I _C = 350 mA | | | | 2.4 | V |
| | Collector-emitter | | $I_1 = 250 \mu A$, | I _C = 100 mA | | | 0.9 | 1.1 | |
| V _{CE(sat)} | saturation voltage | 6 | $I_1 = 350 \ \mu A$, | I _C = 200 mA | | | 1 | 1.3 | V |
| | saturation voitage | | $I_{\parallel} = 500 \ \mu A$, | I _C = 350 mA | | | 1.2 | 1.6 | |
| i_ | Clamp diode reverse | 7 | V _R = 100 V | | | | | 50 | μΑ |
| ^I R | current | | V _R = 100 V, | T _A = 70 °C | | | | 100 | μΑ |
| VF | Clamp diode forward | 8 | I _F = 350 mA | | | | 1.7 | 2 | V |
| Ϋ́F | voltage | | 1F = 330 IIIA | | | | 1.7 | | <u> </u> |
| Ci | Input capacitance | | V _I =0, | f=1 MHz | | | 15 | 25 | pF |

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| | ARAMETER | TEST | TEST CON | TEST CONDITIONS | | N7546 | 6 | 5 | N7546 | 7 | UNIT |
|----------------------|---------------------------------------|------|---|-------------------------|------|-------|-----|-----|-------|------|------|
| r | FIG | | TEST CONDITIONS | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| | | 1 | V _{CE} = 100 V, | 11=0 | | | 50 | | | 50 | |
| ICEX | Collector cutoff current | • | V _{CE} = 100 V, | I _I = 0 | | | 100 | | | 100 | μΑ |
| | | 2 | T _A = 70 °C | V _I =6 V | | | | | | 500 | |
| I _{I(off)} | Off-state input current | 3 | V _{CE} = 50 V, T _A = 70 °C | $I_C = 500 \mu A$, | 50 | 65 | | 50 | 65 | | μΑ |
| l ₁ | Input current | 4 | V _I = 17 V | | | | | | 0.82 | 1.25 | mA |
| hFE | Static forward current transfer ratio | 6 | V _{CE} =2 V, | I _C = 350 mA | 1000 | | ,, | | | | |
| V _{I(on)} | On-state input voltage | 5 | V _{CE} = 2 V, | I _C = 300 mA | | | | | | 13 | ٧ |
| | Collector-emitter | | $I_1 = 250 \mu A$, | I _C = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | |
| V _{CE(sat)} | saturation voltage | 6 | $I_{\parallel} = 350 \ \mu A$, | I _C = 200 mA | | 1 | 1.3 | | 1 | 1.3 | V |
| | saturation voltage | | $I_1 = 500 \mu A$, | $I_C = 350 \text{ mA}$ | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| 1 | Clamp diode | 7 | V _R = 100 V | | | | 50 | | | 50 | μΑ |
| I _R | forward voltage | , | V _R = 100 V, | T _A = 70 °C | | | 100 | | | 100 | μΑ |
| VF | Clamp diode forward voltage | 8 | I _F = 350 mA | | | 1.7 | 2 | | 1.7 | 2 | > |
| Ci | Input capacitance | | V _I = 0, | f=1 MHz | | 15 | 25 | | 15 | 25 | pF |

SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| | DADAMETED | TEST | TEAT OOM | DITIONS | | N7546 | В | S | N7546 | 9 | UNIT | | | | |
|---------------------------------------|--------------------------|--------|--------------------------|-------------------------|-----|-------|------|-----|-------------------------|------|------|---|--|--|--|
| ' | PARAMETER | FIGURE | TEST CON | DITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNII | | | | |
| | | 1 | V _{CE} = 100 V, | I _I =0 | | | 50 | | | 50 | | | | | |
| ICEX | Collector cutoff current | ' | V _{CE} = 100 V, | l ₁ = 0 | | | 100 | | | 100 | μΑ | | | | |
| | | 2 | T _A = 70°C | V _I = 1 V | | | | | | 500 | | | | | |
| 1 | Off-state input current | 3 | V _{CE} = 50 V, | $I_C = 500 \ \mu A$, | 50 | 65 | | 50 | 65 | | μΑ | | | | |
| l(off) | On-state input current | 3 | T _A = 70°C | | 50 | 00 | | 50 | 05 | | μΑ | | | | |
| | | | V _I =3.85 V | | | 0.93 | 1.35 | | | | | | | | |
| l _i | Input current | 4 | V _I = 5 V | | | | | | 0.35 | 0.5 | mA | | | | |
| | | | V _I = 12 V | | | | | | 1 | 1.45 | | | | | |
| | | | | I _C = 125 mA | | | | | | 5 | | | | | |
| | | 5 | V _{CE} = 2 V | I _C = 200 mA | | | 2.4 | | | 6 | | | | | |
| V | | | | I _C = 250 mA | | | 2.7 | | | | | | | | |
| V _{I(on)} | On-state input voltage | | | I _C = 275 mA | | | | | | 7 | ٧ | | | | |
| | | | | | | | | - | I _C = 300 mA | | | 3 | | | |
| | | | | I _C = 350 mA | | | | | | 8 | | | | | |
| | Collector-emitter | | $I_1 = 250 \mu A$, | I _C = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | | | | | |
| V _{CE(sat)} | saturation voltage | 6 | $I_1 = 350 \mu A$, | I _C = 200 mA | | 1 | 1.3 | | 1 | 1.3 | V | | | | |
| | saturation voitage | | $I_{I} = 500 \mu A$, | I _C = 350 mA | | 1.2 | 1.6 | | 1.2 | 1.6 | | | | | |
| 1- | Clamp diode | 7 | V _R = 100 V | | | | 50 | | | 50 | | | | | |
| İR | reverse current | ' | V _R = 100 V, | $T_A = 70 ^{\circ}C$ | | | 100 | | | 100 | μΑ | | | | |
| · · · · · · · · · · · · · · · · · · · | Clamp diode | | J- 250 A | | | 1 7 | 2 | | 1 7 | 2 | ٧ | | | | |
| ٧ _F | forward voltage | 8 | I _F = 350 mA | | | 1.7 | 2 | | 1.7 | 2 | V | | | | |
| Ci | Input capacitance | | V ₁ = 0, | f=1 MHz | | 15 | 25 | | 15 | 25 | pF | | | | |

switching characteristics at 25 °C free-air temperature

| | PARAMETER | | TEST CONDITIONS | | | MAX | UNIT |
|------|--|---|----------------------------|--------------------|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | Vs=50 V, | $R_L \approx 163 \Omega$, | | 0.25 | 1 | μS |
| tPHL | Propagation delay time, high-to-low-level output | C _L = 15 pF, | See Figure 9 | | 0.25 | 1 | μS |
| Vон | High-level output voltage after switching | V _S = 50 V, See Figure 10 | I _O ≈ 300 mA, | V _S -20 | | | mV |

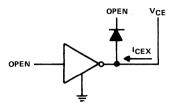


FIGURE 1. ICEX

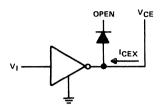


FIGURE 2. ICEX

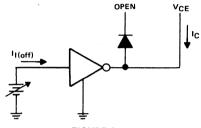


FIGURE 3. II(off)

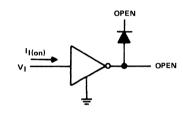


FIGURE 4. II

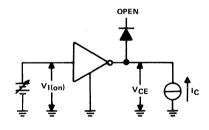
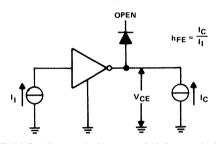
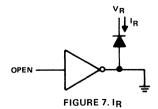


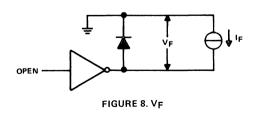
FIGURE 5. VI(on)



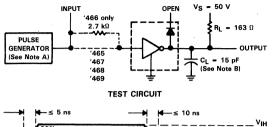
NOTE: I_I is fixed for measuring $V_{\text{CE(sat)}}$, variable for measuring h_{FE} .

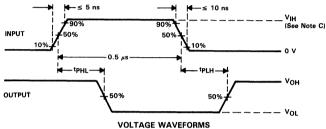
FIGURE 6. hFE, VCE(sat)









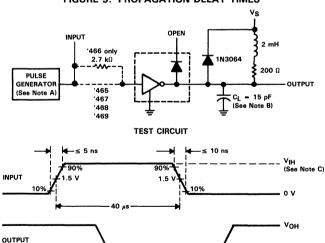


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_0 = 50 \Omega$.

B. C_L includes probe and jig capacitance.

C. For testing the '465, '466, and '468, $V_{IH} = 3 \text{ V}$; for the '467, $V_{IH} = 13 \text{ V}$; for the '469, $V_{IH} = 8 \text{ V}$.

FIGURE 9. PROPAGATION DELAY TIMES



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_0 = 50 \Omega$.

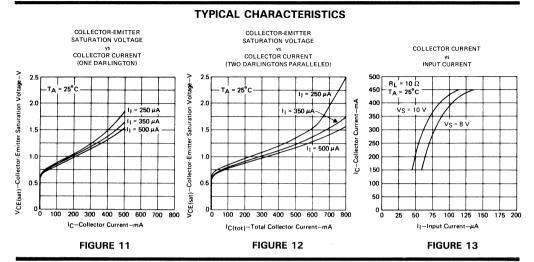
B. C_L includes probe and jig capacitance.

C. For testing the '465, '466, and '468, $V_{IH}=3~V$; for the '467, $V_{IH}=13~V$; for the '469, $V_{IH}=8~V$.

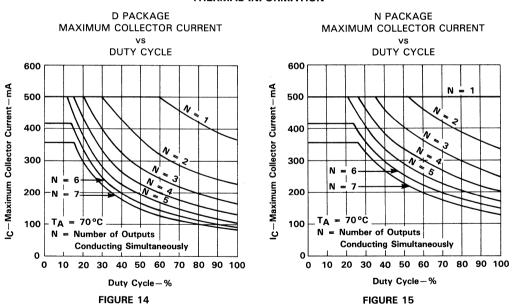
FIGURE 10. LATCH-UP TEST

VOLTAGE WAVEFORMS

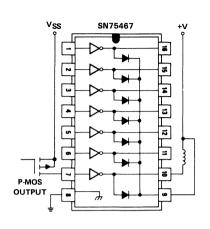




THERMAL INFORMATION



TYPICAL APPLICATION DATA



SN75465

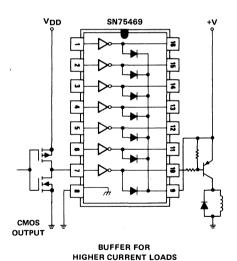
VCC SN75466, SN75468

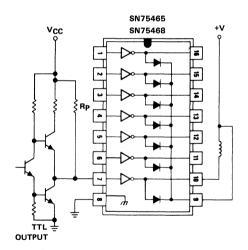
+V

LAMP
TEST
OUTPUT

P-MOS TO LOAD

TTL TO LOAD





USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

SN75471 THRU SN75473 DUAL PERIPHERAL DRIVER

D2130, DECEMBER 1976-REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability

D OR P PACKAGE (TOP VIEW)



SUMMARY OF SERIES SN75471

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---------|------------------------------|----------|
| SN75471 | AND | D,P |
| SN75472 | NAND | D,P |
| SN75473 | OR | D,P |

description

Series SN75471 dual peripheral drivers are functionally interchangeable with Series SN75451B and Series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 75451B (limits are the same as Series SN75461). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, and OR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

SN75471 THRU SN75473 **DUAL PERIPHERAL DRIVERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | 7 V |
|---|-----------|
| Input voltage | |
| Interemitter voltage (see Note 2) | . 5.5 V |
| Off-state output voltage | 70 V |
| Continuous collector or output current (see Note 3) | 400 mA |
| Peak collector or output current ($t_W \le 10$ ms, duty cycle $\le 50\%$, see Note 3) | 500 mA |
| Continuous total power dissipation See Dissipation Rati | ing Table |
| Operating free-air temperature range, TA | to 70°C |
| Storage temperature range65°C to | o 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260°C |

- NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.
 - 2. This is the voltage between two emitters of a multiple-emitter transistor.
 - 3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

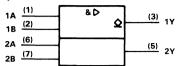
DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | TA = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|------------------------------------|------|-----|------|------|
| Supply voltage, V _{CC} | 4.75 | 5 | 5.25 | V |
| High-level input voltage, VIH | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |





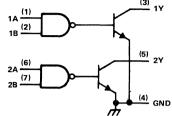
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH DRIVER)

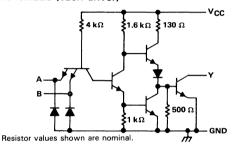
| Α | В | Y |
|---|---|---------------|
| L | L | L (on state) |
| L | Н | L (on state) |
| Н | L | L (on state) |
| н | Н | H (off state) |

positive logic: $Y = AB \text{ or } \overline{A} + \overline{B}$

logic diagram (positive logic)



schematic (each driver)



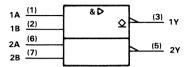
electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CONDITIONS | MIN | TYP [‡] | MAX | UNIT |
|------|--|--|-----|------------------|-------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 \text{ V}, \text{ I}_{I} = -12 \text{ mA}$ | | -1.2 | - 1.5 | V |
| ЮН | High-level output current | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{OH} = 70 V | | | 100 | μΑ |
| Vol | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{ L} = 0.8 \text{ V},$ $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.4 | V |
| VOL | cow-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V}$ $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.7 | V |
| 11 | Input current at maximum input voltage | V _{CC} = 5.25 V, V _I = 5.5 V | | | 1 | mA |
| ЧΗ | High-level input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 2.4 \text{ V}$ | | | 40 | μΑ |
| IIL | Low-level input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 0.4 \text{ V}$ | | - 1 | -1.6 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = 5.25 \text{ V}, V_1 = 5 \text{ V}$ | | 8 | 11 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 \text{ V}, V_{I} = 0$ | | 56 | 76 | mA |

 $^{^{\}ddagger}All$ typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---------|-----|-----|------|
| tpLH Propagation delay time, low-to-high-level output | | | 30 | 55 | ns |
| tpHL Propagation delay time, high-to-low-level output | $I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF},$ | | 25 | 40 | ns |
| tTLH Transition time, low-to-high-level output | $R_L = 50 \Omega$, See Figure 1 | | 8 | 20 | ns |
| tTHL Transition time, high-to-low-level output | | | 10 | 20 | ns |
| Va. High level output voltage ofter quitching | $V_S = 55 \text{ V}, I_O \approx 300 \text{ mA}$ | Vs - 18 | | | mV |
| VOH High-level output voltage after switching | See Figure 2 | VS-16 | | _ | mv |



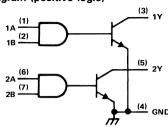
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH DRIVER)

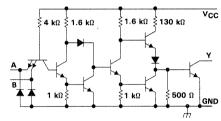
| Α | В | Y |
|---|---|---------------|
| L | L | H (off state) |
| L | н | H (off state) |
| н | L | H (off state) |
| н | Н | L (on state) |

positive logic: $Y = \overline{AB} \text{ or } \overline{A} + \overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

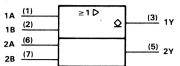
electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CONDITIONS | MIN | TYP [‡] | MAX | UNIT |
|------|--|--|-----|------------------|------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 \text{ V}, \text{ I}_{I} = -12 \text{ mA}$ | | -1.2 | -1.5 | ٧ |
| ЮН | High-level output current | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{OH} = 70 V | | | 100 | μΑ |
| Vai | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V},$ $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.4 | V |
| VOL | | $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V}$ $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.7 | • |
| h | Input current at maximum input voltage | V _{CC} = 5.25 V, V _I = 5.5 V | | | 1 | mA |
| ΊΗ | High-level input current | $V_{CC} = 5.25 \text{ V}, V_{I} = 2.4 \text{ V}$ | | | 40 | μΑ |
| IIL | Low-level input current | $V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.4 \text{ V}$ | | -1 | -1.6 | mA |
| Іссн | Supply current, outputs high | V _{CC} = 5.25 V, V _I = 5 V | | 13 | 17 | mA |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 \text{ V}, V_{I} = 0$ | | 61 | 76 | mA |

 $^{^{\}ddagger}AII$ typical values are at VCC = 5 V, TA = 25 °C.

switching characteristics, VCC = 5 V, TA = 25 °C

| PARAMETER | TEST CONDITIONS | | TYP | MAX | UNIT |
|--|---|-------|---------------------|-----|-------|
| tpLH Propagation delay time, low-to-high-level output | | | 45 | 65 | ns |
| tpHL Propagation delay time, high-to-low-level output | $I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF},$ | | 30 | 50 | ns |
| t _{TLH} Transition time, low-to-high-level output | $R_L = 50 \Omega$, See Figure 1 | | 13 | 25 | ns |
| t _{THL} Transition time, high-to-low-level output | | | 10 | 20 | ns |
| VOH High-level output voltage after switching | $V_S = 55 \text{ V}, I_O \approx 300 \text{ mA},$ | V- 10 | | | mV |
| VOH High-level output voltage after switching | See Figure 2 | VS-10 | V _S – 18 | | ····V |



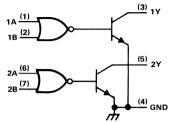
 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH DRIVER)

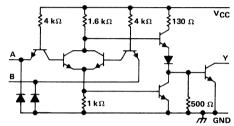
| Α | В | Υ |
|----|---|---------------|
| L | L | L (on state) |
| L | Н | H (off state) |
| н | L | H (off state) |
| ĺн | н | H (off state) |

positive logic: $Y = A + B \text{ or } \overline{\overline{A}}\overline{\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

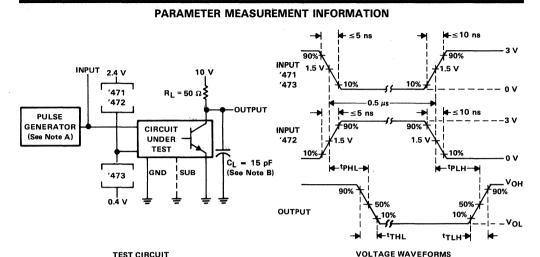
| | PARAMETER | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|------|--|--|-----|------|------|------|
| VIK | Input clamp voltage | $V_{CC} = 4.75 \text{ V}, I_{\parallel} = -12 \text{ mA}$ | | -1.2 | -1.5 | ٧ |
| ЮН | High-level output current | $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ $V_{OH} = 70 \text{ V}$ | | | 100 | μΑ |
| VOL | Low-level output voltage | $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V},$ $I_{OL} = 100 \text{ mA}$ | | 0.25 | 0.4 | V |
| VOL | | $V_{CC} = 4.75 \text{ V}, V_{IL} = 0.8 \text{ V}$ $I_{OL} = 300 \text{ mA}$ | | 0.5 | 0.7 | V |
| lı | Input current at maximum input voltage | $V_{CC} = 5.25 \text{ V}, V_{I} = 5.5 \text{ V}$ | | | 1 | mA |
| ΊΗ | High-level input current | $V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 2.4 \text{ V}$ | | | 40 | μΑ |
| IIL | Low-level input current | V _{CC} = 5.25 V, V _I = 0.4 V | | - 1 | -1.6 | mA |
| Іссн | Supply current, outputs high | $V_{CC} = 5.25 \text{ V}, V_{I} = 5 \text{ V}$ | | 8 | 11 | mA . |
| ICCL | Supply current, outputs low | $V_{CC} = 5.25 \text{ V}, V_{I} = 0$ | | 58 | 76 | mA |

 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$

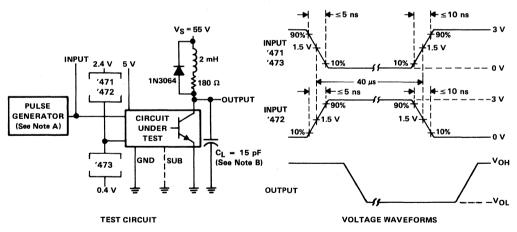
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--------------------|-----|-----|------|
| tpLH Propagation delay time, low-to-high-level output | | | 30 | 55 | ns |
| tpHL Propagation delay time, high-to-low-level output | $I_0 \approx 200 \text{ mA}, C_L = 15 \text{ pF},$ | | 25 | 40 | ns |
| t _{TLH} Transition time, low-to-high-level output | $R_L = 50 \Omega$, See Figure 1 | | 8 | 25 | ns |
| t _{THL} Transition time, high-to-low-level output | | | 10 | 25 | ns |
| IOH High-level output voltage after switching | $V_S = 55 \text{ V}, \qquad I_O \approx 300 \text{ mA},$ See Figure 2 | V _S -18 | | | mV |





NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, Z₀ \approx 50 Ω . B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, Z₀ \approx 50 Ω . B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST



SN75476 THRU SN75479 DUAL PERIPHERAL DRIVERS

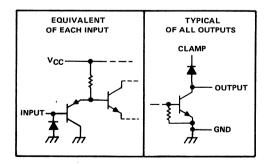
D2284, DECEMBER 1976-REVISED DECEMBER 1989

- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typical)
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability

description

Series SN75476 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diodeclamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, SN75478, and SN75479 drivers are characterized for operation from 0°C to 70°C .



D OR P PACKAGE (TOP VIEW)

| s∐ī | U 8 | □vcc |
|--------|------------|-------|
| 1A 🔲 2 | 7 |] 2A |
| 1Y 🛚 3 | 6 |] 2Y |
| GND □4 | 5 | CLAMP |

FUNCTION TABLES

SN75476 (EACH AND DRIVER)

| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | S | Υ |
| Н | Н | Н |
| L | Х | L |
| x | L | L |

SN75477 (EACH NAND DRIVER)

| į | INP | UTS | OUTPUT |
|---|-----|-----|--------|
| | Α | S | Υ |
| | Н | Η | L |
| | L | Х | Н |
| | х | L | н |

SN75478 (EACH OR DRIVER)

| I | INP | UTS | OUTPUT |
|---|-----|-----|--------|
| | Α | S | Υ |
| | Н | Х | Н |
| | х | Н | н |
| ı | L | L | L |

SN75479 (EACH NOR DRIVER)

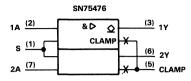
| INP | UTS | OUTPUT |
|-----|-----|--------|
| Α | S | Y |
| Н | Х | L |
| x | Н | L |
| L | L | н |

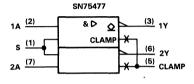
H = high level L = low level

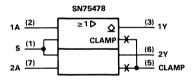
L = low level X = irrelevant

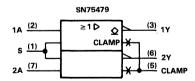
SN75476 THRU SN75479 DUAL PERIPHERAL DRIVERS

logic symbols†

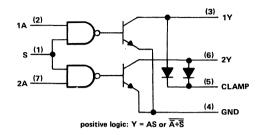


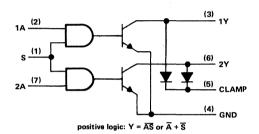


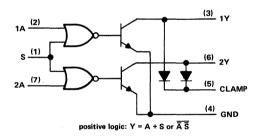


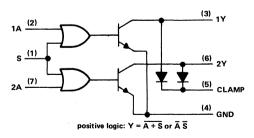


logic diagrams (positive logic)









[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, V _{CC} (see Note 1) |
|---|
| Input voltage |
| Continuous output current (see Note 2) |
| Peak output current: $t_W \le 10$ ms, duty cycle $\le 50\%$ |
| $t_W \le 30$ ns, duty cycle $\le 0.002\%$ |
| Output clamp diode current |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range, TA |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTES: 1. Voltage values are with respect to network ground terminal.

Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 70°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-----|------|
| Supply voltage, VCC | 4.5 | 5 | 5.5 | V |
| High-level input voltage, V _{IH} | 2 | | | V |
| Low-level input voltage, VIL | | | 0.8 | V |
| Operating free-air temperature, TA | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range

| | PARAMETER | TEST CO | ONDITIONS | MIN | TYPt | MAX | UNIT | |
|--|------------------------------------|----------|--|--|------|-------|-------|------|
| VIK | Input clamp voltage | | l _j = -12 mA | | - | -0.95 | - 1.5 | V |
| ЮН | High-level output current | | $V_{CC} = 4.5 \text{ V},$ $V_{IL} = 0.8 \text{ V},$ | V _{IH} = 2 V, V _{OH} = 70 V | | 1 | 100 | μΑ |
| V _{OL} Low-level output voltage | | | $V_{CC} = 4.5 V$, | I _{OL} = 100 mA | | 0.16 | 0.3 | |
| | | | V _{IH} = 2 V, | I _{OL} = 175 mA | | 0.22 | 0.5 | V |
| ĺ | | | V _{IL} = 0.8 V | I _{OL} = 300 mA | | 0.33 | 0.6 | |
| V _{(BR)O} | /(BR)O Output breakdown voltage | | $V_{CC} = 4.5 V,$ | IOH = 100 μA | 70 | 100 | | V |
| V _{R(K)} | | | $V_{CC} = 4.5 V,$ | $I_R = 100 \mu A$ | 70 | 100 | | V |
| V _{F(K)} | Output clamp diode forward voltage | | $V_{CC} = 4.5 V$, | I _F = 300 mA | 0.8 | 1.15 | 1.6 | V |
| lн | High-level input current | | $V_{CC} = 5.5 V,$ | $V_{I} = 5.5 \text{ V}$ | | 0.01 | 10 | μΑ |
| | Low-level input current | A input | V _{CC} = 5.5 V, V _I = | V _I = 0.8 V | | -80 | -110 | |
| IIL | Low-level input current | Strobe S | VCC = 5.5 V, | VI - 0.6 V | | - 160 | -220 | μΑ |
| | | SN75476 | | V _I = 5 V | | 10 | 17 | |
| l | Supply current, outputs high | SN75477 | V 5 5 V | V _I = 0 | | 10 | 17 | mA |
| ICCH | Supply current, outputs high | SN75478 | $V_{CC} = 5.5 V$ | V _I = 5 V | | 10 | 17 | IIIA |
| | | SN75479 | | V _I = 0 | | 10 | 17 | |
| | | SN75476 | | V _I = 0 | | 54 | 75 | |
| , | Complete account accounts lave | SN75477 |] V 5 5 V | V _I = 5 V | | 54 | 75 | |
| CCL | Supply current, outputs low | SN75478 | V _{CC} = 5.5 V | V _I = 0 | | 54 | 75 | mA |
| | | SN75479 | | V _I = 5 V | | 54 | 75 | |

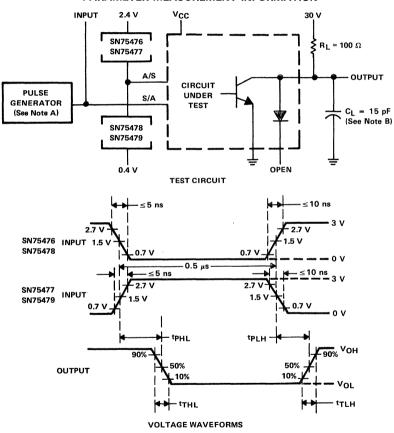
 $^{^{\}dagger}AII$ typical values are at $V_{CC}\,=\,5$ V, $T_{A}\,=\,25\,^{o}C.$



switching characteristics, VCC = 5 V, TA = 25°C

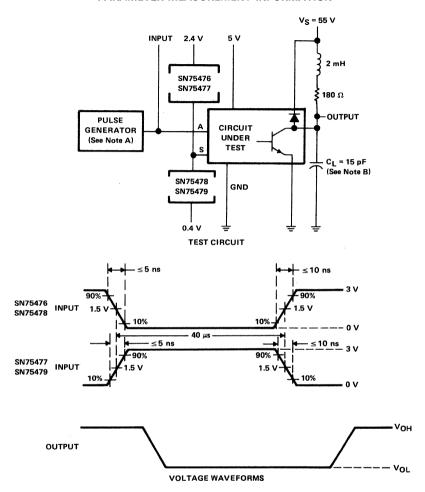
| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|---|---------|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | | , | 200 | 350 | ns |
| tPHL | Propagation delay time, high-to-low-level output | $C_{L} = 15 \text{ pF, } R_{L} = 100 \Omega,$ | | 200 | 350 | ns |
| [†] TLH | Transition time, low-to-high-level output | See Figure 1 | | 50 | 125 | ns |
| [†] THL | Transition time, high-to-low-level output | · | | 90 | 125 | ns |
| Vall | High-level output voltage after switching | $V_S = 55 \text{ V, I}_O \approx 300 \text{ mA,}$ | Vs-18 | | | mV |
| VOH H | riigii-level output voltage arter switching | See Figure 2 | 1 15-10 | | | |

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω . B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω .

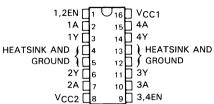
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

D2942, NOVEMBER 1986-REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- **Output Clamp Diodes for Inductive Transient** Suppression
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance **Diode-Clamped Inputs**
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the **SGS L293D**

NE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

| INPUTS† | | OUTPUT |
|---------|---|--------|
| A EN | | Y |
| Н | Н | н |
| L | Н | L |
| Х | L | Z |

H = high-level

L = low-level

X = irrelevant

Z = high-impedance (off)

†In the thermal shutdown mode, the output is in highimpedance state regardless of the input levels.

description

The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

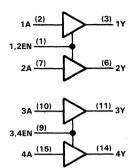
A separate supply voltage (VCC1) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (VCC2) is used for the output circuits.

The SN754410 is designed for operation from -40 °C to 85 °C.

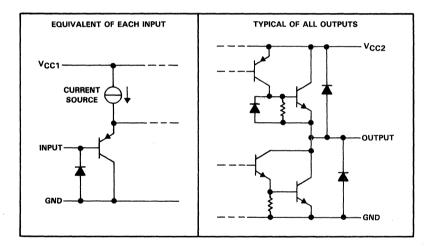
SN754410 QUADRUPLE HALF-H DRIVER

logic symbol†

logic diagram



schematics of inputs and outputs



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Logic supply voltage range, VCC1 (see Note 1) | V to 36 V |
|--|-----------|
| Output supply voltage range, V _{CC2} 0.5 \ | V to 36 V |
| Input voltage | 36 V |
| Output voltage range, VO | CC2+3 V |
| Peak output current (nonrepetitive, $t_W \le 5$ ms), IPK | ±2 A |
| Continuous output current, IO | ± 1.1 A |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) | 2075 mW |
| Operating free-air temperature range40°C | C to 85°C |
| Operating case or virtual junction temperature range40°C | to 150°C |
| Storage temperature range65°C | to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | . 260°C |

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

| | MIN | MAX | UNIT |
|--|-------------------|-----|------|
| Logic supply voltage, V _{CC1} | 4.5 | 5.5 | ٧ |
| Output supply voltage, V _{CC2} | 4.5 | 36 | > |
| High-level input voltage, VIH | 2 | 5.5 | V |
| Low-level input voltage, VIL | -0.3 [†] | 0.8 | ٧ |
| Operating virtual junction temperature, TJ | 40 | 125 | °C |
| Operating free-air temperature, TA | -40 | 85 | °C |

[†] The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

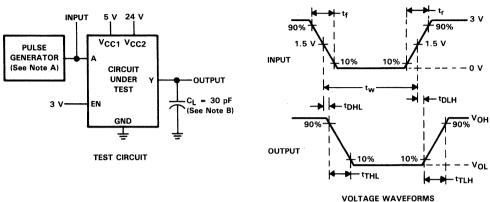
electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating virtual junction temperature (unless otherwise noted)

| | PARAMETER TEST CONDITIONS | | MIN | TYP [†] | MAX | UNIT | |
|------|----------------------------------|---------------------|-------------------------------|-----------------------|-----------------------|-----------------------|----|
| VIK | Input clamp voltage | I ₁ = -1 | 2 mA | | -0.9 | -1.5 | V |
| | | IOH = | -0.5 A | V _{CC2} -1.5 | V _{CC2} -1.1 | | |
| Vон | High-level output voltage | IOH = | -1 A | V _{CC2} -2 | | | V |
| L | | IOH = | -1 A, T _J = 25°C | V _{CC2} -1.8 | VCC2-1.4 | | |
| | | IOL = 0 | .5 A | | 1 | 1.4 | |
| VOL | Low-level output voltage | I _{OL} = 1 | Α | | | 2 | V |
| | I _{OL} = 1 | A, $T_J = 25$ °C | | 1.2 | 1.8 | | |
| V | High-level output clamp voltage | IOK = C |).5 A | | V _{CC2} +1.4 | V _{CC2} +2 | |
| VOKH | High-level output clamp voltage | IOK = 1 | Α | | V _{CC2} +1.9 | V _{CC2} +2.5 | |
| V | Low-level output clamp voltage | $I_{OK} = -0.5 A$ | | | -1.1 | - 2 | V |
| VOKL | Low-level output clamp voltage | IOK = - | -1 A | | -1.3 | - 2 <i>.</i> 5 | V |
| 10- | Off-state (high-impedance state) | V ₀ = V | CC2 1 | | | 500 | ^ |
| loz | output current | $V_0 = 0$ | | | | - 500 | μΑ |
| ήн | High-level input current | $V_I = 5$. | 5 V | | | | μΑ |
| IL | Low-level input current | $V_i = 0$ | | | | - 10 | μΑ |
| | | | All outputs at high level | | | 38 | |
| ICC1 | Logic supply current | 10 = 0 | All outputs at low level | | | 70 | mA |
| | | | All outputs at high impedance | | | 25 | |
| | | | All outputs at high level | | | 33 | |
| ICC2 | Output supply current | 10 = 0 | All outputs at low level | 20 | | 20 | mA |
| | | | All outputs at high impedance | | | 5 | |

 $^{^{\}dagger} All$ typical values are at VCC1 = 5 V, VCC2 = 24 V, TA = 25 °C.

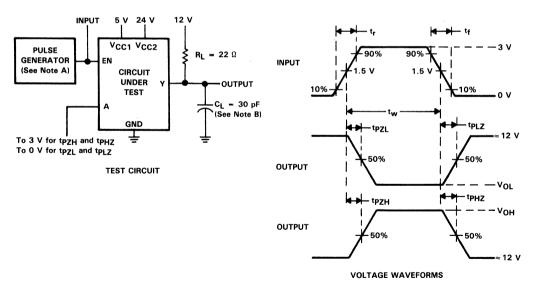
switching characteristics, VCC1 = 5 V, VCC2 = 24 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|---|--------------------------------------|-----|-----|-----|------|
| tDLH | Delay time, low-to-high-level output from A input | | | 800 | | ns |
| tDHL | Delay time, high-to-low-level output from A input | 400 | | | ns | |
| tTLH | Transition time, low-to-high-level output | C _L = 30 pF, See Figure 1 | 300 | | ns | |
| tTHL | Transition time, high-to-low-level output | | | 300 | | ns |
| tPZH | Enable time to the high level | | | 700 | | ns |
| tPZL | Enable time to the low level | C ₁ = 30 pF, See Figure 2 | | 400 | | ns |
| tPHZ | Disable time from the high level | CL = 30 pr, See rigule 2 | | 900 | | ns |
| tPLZ | Disable time from the low level | | | 600 | | ns |



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 10 \,\mu s$, PRR = 5 kHz, $Z_0 = 50 \,\Omega$. B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 10~\mu s$, PRR = 5 kHz, $Z_0 = 50~\Omega$. B. C₁ includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS



APPLICATION INFORMATION

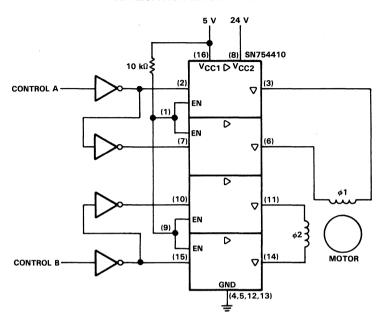


FIGURE 3. TWO-PHASE MOTOR DRIVER

QUADRUPLE HALF-H DRIVER

D2942 NOVEMBER 1986-REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- **Designed for Positive-Supply Applications**
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance **Diode-Clamped Inputs**
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the **SGS L293**

NE PACKAGE (TOP VIEW) 1,2EN 1 U₁₆D V_{CC1} 1A 🛮 2 15 4A 1Y 🛚 14 4Y 3 HEATSINK AND 1 1 4 13 HEATSINK AND GROUND 1 12 ☐ ∫ GROUND 5 27 □6 11 3Y 2A 🛮 7 10 3A 9 3,4EN Vcc2 ∏8

FUNCTION TABLE (EACH DRIVER)

| INPL | JTS [†] | OUTPUT |
|------|------------------|--------|
| A EN | | Υ |
| Н | Н | Н |
| L | Н | L |
| Х | L | z |

H = high-level

L = low-level

X = irrelevant

7 = high-impedance (off)

†In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

The SN754411 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

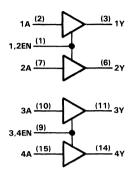
All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive-transient suppression. A separate supply voltage (VCC1) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (VCC2) is used for the output circuits.

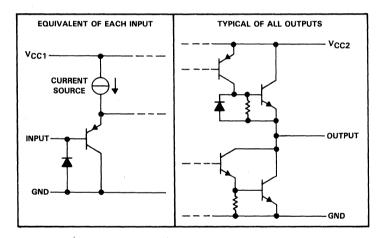
The SN754411 is designed for operation from -40°C to 85°C.

1A (2) (3) 1Y Δ V 1,2EN (1) ΕN EN (6) 2Y V 2A (7) 3A (10) (11) 3Y D V 3,4EN (9) EN (14)₄Y V

logic diagram



schematics of inputs and outputs



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Logic supply voltage range, VCC1 (see Note 1) | -0.5 V to 36 V |
|--|----------------|
| Output supply voltage range, VCC2 | -0.5 V to 36 V |
| Input voltage | 36 V |
| Output voltage range, Vo | V to VCC2+3 V |
| Peak output current (nonrepetitive, $t_W \le 5$ ms), IPK | ±2 A |
| Continuous output current, IO | ± 1.1 A |
| Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) | 2075 mW |
| Operating free-air temperature range | -40°C to 85°C |
| Operating case or virtual junction temperature range | -40°C to 150°C |
| Storage temperature range | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. For operation above 25 °C free-air temperature, derate linearly at the rate of 16.6 mW/ °C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

| | MIN | MAX | UNIT |
|--|-------------------|-----|------|
| Logic supply voltage, V _{CC1} | 4.5 | 5.5 | V |
| Output supply voltage, V _{CC2} | 4.5 | 36 | V |
| High-level input voltage, VIH | 2 | 5.5 | V |
| Low-level input voltage, V _{IL} | -0.3 [†] | 0.8 | V |
| Operating virtual junction temperature, TJ | -40 | 125 | °C |
| Operating free-air temperature, TA | -40 | 85 | °C |

[†] The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

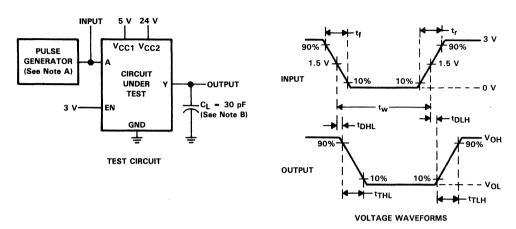
electrical characteristics over recommended ranges of VCC1, VCC2, and operating virtual junction temperature (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-------------------|----------------------------------|----------------------|-----------------------------------|-----------------------|-----------------------|-------|-------|
| VIK | Input clamp voltage | I _I = -1 | 2 mA | | -0.9 | -1.5 | V |
| | | IOH = · | -0.5 A | V _{CC2} -1.5 | V _{CC2} -1.1 | | |
| V _{OH} I | High-level output voltage | IOH = - | –1 A | V _{CC2} -2 | | | V |
| | | IOH = · | -1 A, T」= 25°C | V _{CC2} -1.8 | V _{CC2} -1.4 | | |
| | | IOL = 0 | .5 A | | 1 | 1.4 | |
| VOL | Low-level output voltage | IOL = 1 | A | | | 2 | \ \ \ |
| | | I _{OL} = 1 | A, T _J = 25°C | | 1.2 | 1.8 |] |
| la- | Off-state (high-impedance state) | $V_0 = V$ | V _O = V _{CC2} | | | 500 | μΑ |
| loz | output current | V _O = 0 | V _O = 0 | | | - 500 | |
| Ιн | High-level input current | $V_{\parallel} = 5.$ | 5 V _ | | | 10 | μΑ |
| ήL | Low-level input current | $V_{\parallel} = 0$ | | | | - 10 | μΑ |
| | | | All outputs at high level | | | 38 | |
| ICC1 | Logic supply current | 10 = 0 | All outputs at low level | | | | mA |
| | | | All outputs at high impedance | | | 25 | |
| | Output supply current | | All outputs at high level | | | 33 | |
| ICC2 | | 10 = 0 | All outputs at low level | | | 20 | mA |
| | | | All outputs at high impedance | | | 5 |] |

 $^{^{\}dagger}$ All typical values are at V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25 °C.

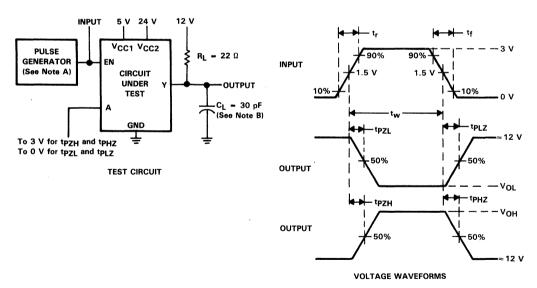
switching characteristics, VCC1 = 5 V, VCC2 = 24 V, TA = 25 °C

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|--------------------------------------|-----|-----|-----|------|
| ^t DLH | Delay time, low-to-high-level output from A input | | 800 | | ns | |
| tDHL | Delay time, high-to-low-level output from A input | C: - 30 pE Son Figure 1 | 400 | | ns | |
| tTLH | Transition time, low-to-high-level output | C _L = 30 pF, See Figure 1 | | 300 | | ns |
| ^t THL | Transition time, high-to-low-level output | | | 300 | | ns |
| tPZH | Enable time to the high level | | | 700 | | ns |
| tPZL | Enable time to the low level | | | 400 | | ns |
| tPHZ | Disable time from the high level | C _L = 30 pF, See Figure 2 | | 900 | | ns |
| tPLZ | Disable time from the low level | | | 600 | | ns |



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 10$ μ s, PRR = 5 kHz, $Z_0 = 50$ Ω . B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 10$ μ s, PRR = 5 kHz, $Z_0 = 50$ Ω . B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS



APPLICATION INFORMATION 16 8 SN754411 10 kΩ ≷ V_{CC1} ▷ V_{CC2} 2 CONTROL A ΕN 7 10 ▽ EN 15 CONTROL B MOTOR GND ALL DIODES: 1N4935 (4,5,12,13)

FIGURE 3. TWO-PHASE MOTOR DRIVER

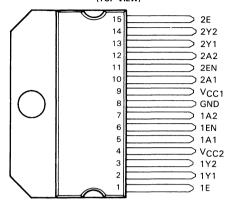
- Formerly TLP298
- 2-A Output Current Capability per Full-H Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Wide Range of Output Supply Voltage . . . 5 V to 46 V
- Separate Input-Logic Supply Voltage
- Thermal Shutdown
- Internal Electrostatic Discharge Protection
- High Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- Improved Functional Replacement for the SGS L298

description

The TPIC0298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totempole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

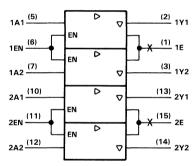
Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

KV PACKAGE (TOP VIEW)



The tab is electrically connected to pin 8.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE (EACH CHANNEL)

| INP | UTS | OUTPUT |
|------|-----|--------|
| A EN | | Υ |
| Н | Н | Н |
| L | Н | Ł |
| Х | L | z |

H = high-level

L = low-level

X = irrelevant

Z = high-impedance (off)

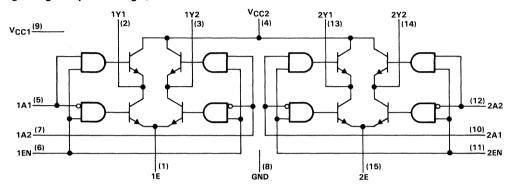
Texas VI

description (continued)

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a VCC1 supply voltage, separate from VCC2, is provided for the logic inputs.

The TPICO298 is designed for operation from 0°C to 70°C.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

| Logic supply voltage range, VCC1, (see Note 1) | -0.3~V to $7~V$ |
|--|---------------------|
| Output supply voltage range, VCC2 | |
| Input voltage range at A or EN, V _I (see Note 2) | $-1.6\ V$ to $7\ V$ |
| Output voltage range, Vo | to VCC2+2 V |
| Emitter terminal (1E and 2E) voltage range, VE | 0.5 V to 2.3 V |
| Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_W \le 50 \mu s$) | 1 V |
| Input current at A or EN, I _I | |
| Peak output current, I_{OM} , (nonrepetitive, $t_W \le 0.1 \text{ ms}$) | ±3 A |
| (repetitive, $t_W \le 10$ ms, duty cycle $\le 80\%$) | ±2.5 A |
| Continuous output current, IO | ±2 A |
| Peak combined output current for each full-H driver (see Note 3) | |
| (nonrepetitive, $t_W \leq 0.1 \text{ ms}$) | ±3 A |
| (repetitive, $t_W \le 10$ ms, duty cycle $\le 80\%$) | ±2.5 A |
| Continuous combined output current for each full-H driver (see Note 3) | ±2 A |
| Continuous dissipation at (or below) 25 °C free-air temperature (see Note 4) | 3.575 W |
| Continuous dissipation at (or below) 75 °C case temperature (see Note 4) | 25 W |
| Operating free-air, case, or virtual junction temperature range | 40°C to 150°C |
| Storage temperature range6 | 35°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| | |

- NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
 - The maximum current limitation at this terminal generally occurs at a voltage of lower magnitude than the voltage limit, Neither the maximum current nor the maximum voltage for this terminal should be exceeded.
 - 3. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
 - 4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.



recommended operating conditions

| | | | MIN | MAX | UNIT |
|--|--|-----|-------------------|------------------------|------|
| Logic supply voltage, V _{CC1} | | | 4.5 | 7 | ٧ |
| Output supply voltage, V _{CC2} | | | 5 | 46 | ٧ |
| | | | -0.5† | 2 | |
| Emitter terminal (1E or 2E) voltage, V _E (see Note 5) | | | | V _{CC1} - 3.5 | V |
| | | | | V _{CC2} -4 | |
| | | А | 2.3 | V _{CC1} | |
| High-level input voltage, V _{IH} (see Note 5) | | | | V _{CC2} -2.5 | v |
| High-level input voltage, VIH (see Note 5) | | EN | 2.3 | 7 | V |
| | | EIN | | V _{CC1} | |
| Low-level input voltage at A or EN, V _{IL} | | | -0.3 [†] | 1.5 | V |
| Output current, IO | | | | ± 2 | Α |
| Commutation frequency, f _C | | | | 40 | kHz |
| Operating free-air temperature, TA | | | 0 | 70 | °C |

[†] The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 5: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than VCC2, the maximum recommended voltage at any EN input is VCC1, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than VCC1 and 4 V lower than VCC2.

TPIC0298 DUAL FULL-H DRIVER

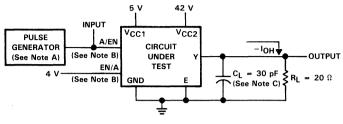
electrical characteristics over recommended ranges of VCC1, VCC2, and VE, TJ = 25 °C (unless otherwise noted)

| | PARAMETER | | | TEST CONDITIO | NS | MIN | TYP [†] | MAX | UNIT |
|-------------------|----------------------------|--|--|----------------------------------|---------------|-------------------------|----------------------|----------------------|------|
| VIK | Input clamp voltage | | I _I = -12 mA | | | | -0.9 | -1.5 | V |
| V | High-level output voltage | | IOH = -1 | I A | | V _{CC2} -1.8 \ | /CC2-1.2 | | V |
| VOH | | | I _{OH} = −2 A | | VCC2-2.8 V | /CC2-1.8 | | v | |
| | Low-level output voltage | | I _{OL} = 1 A | \ | | | V _E +1.2 | V _E + 1.8 | V |
| VOL | | | IOL = 2 A | \ | | | V _E + 1.7 | V _E + 2.6 | • |
| ٧. | Total source plus sink | | IOH = -1 | I A, I _{OL} = 1 A | See Note 6 | | 2.4 | 3.4 | V |
| V _{drop} | output voltage drop | | I _{OH} = -2 | 2 A, I _{OL} = 2 A | | | 3.5 | 5.2 | · · |
| | Off-state (high-impedane | ce state) | | | | | | | |
| lozh | output current, high-leve | el | $V_0 = V_{CC2}$ | | | . | | 500 | μΑ |
| | voltage applied | | | | | | | | |
| | Off-state (high-impedane | ce state) | | | | ŀ | | | |
| OZL | output current, low-leve | l | $V_0 = 0 V, V_E = 0 V$ | | ļ | | - 500 | μΑ | |
| | voltage applied | | | | | L | | | |
| | High-level input current A | ۸ | VI = VIH | | EN = H | | 20 | 100 | |
| ΉΗ | | High-level input current | VI - VIH | VI – VIH EN = L | | | | 10 | μΑ |
| | EN | | $V_I = V_{IH}$ | \leq V _{CC1} -0.6 V | | | 6 | 100 | |
| ΊL | Low-level input current | | V _I = 0 V to 1.5 V | | | | | - 10 | μΑ |
| | Logic supply current | All outputs at high All outputs at low All outputs at high All out | | igh level | | 7 | 12 | | |
| ICC1 | | | | ow level | | 20 | 32 | mA | |
| | | | | igh impedance | | 4 | 6 | | |
| | Output supply current | | IO = 0 All outputs at high leverage All outputs at low leverage All outputs at high im | | igh level | | 25 | 50 | |
| ICC2 | | | | | ow level | | 6 | 20 | mA |
| | | | | | igh impedance | | | 2 | |

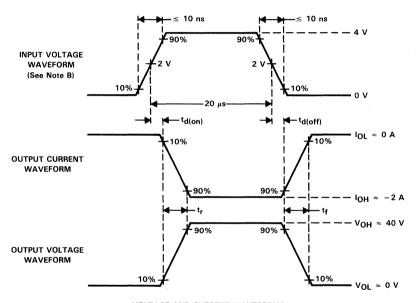
 $^{^{\}dagger}$ All typical values are at V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0 V, T_J = 25 °C (unless otherwise noted). NOTE 6: The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels. V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E.

switching characteristics, $V_{CC1} = 5 \text{ V}$, $V_{CC2} = 42 \text{ V}$, $V_E = 0$, $T_A = 25 ^{\circ}\text{C}$

| | PARAMETER | TEST CONDITIONS | MIN TYP MAX | UNIT |
|---------------------|--|-----------------|-------------|------|
| t _{d(on)} | Source current turn-on delay time from A input | | 0.6 | μs |
| td(off) | Source current turn-off delay time from A input | | 0.8 | μS |
| t _r | Source current rise time (turning on) | $C_L = 30 pF$, | 0.8 | μS |
| tf | Source current fall time (turning off) | See Figure 1 | 0.2 | μs |
| t _{d(on)} | Source current turn-on delay time from EN input | | 0.5 | μs |
| ^t d(off) | Source current turn-off delay time from EN input | | 2.5 | μS |
| t _{d(on)} | Sink current turn-on delay time from A input | | 1.3 | μS |
| ^t d(off) | Sink current turn-off delay time from A input | | 0.5 | μs |
| t _r | Sink current rise time (turning on) | $C_L = 30 pF$, | 0.2 | μS |
| tf | Sink current fall time (turning off) | See Figure 2 | 0.2 | μs |
| t _{d(on)} | Sink current turn-on delay time from EN input | | 0.3 | μs |
| td(off) | Sink current turn-off delay time from EN input | | 1 | μS |



TEST CIRCUIT



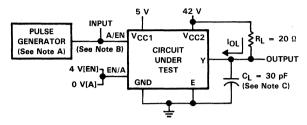
VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_0 = 50 Ω .

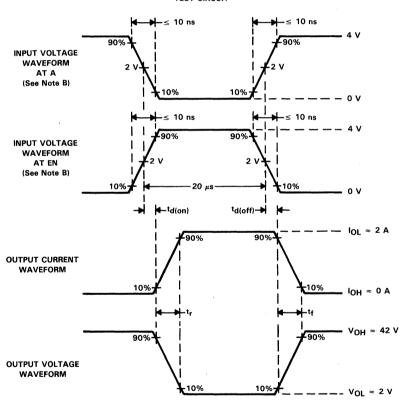
- B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
- C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS





TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z $_{0}$ = 50 $\Omega.$

B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.

C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS



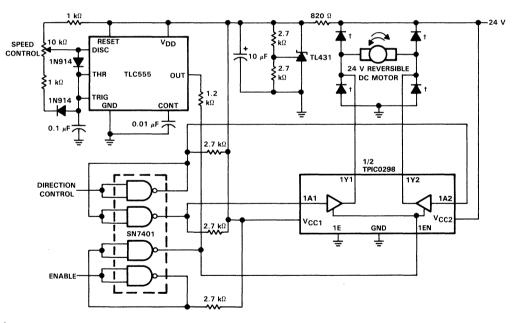
TYPICAL APPLICATION DATA

This circuit shows one half of a TPICO298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the TPICO298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 short regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

| ENABLE | DIRECTION CONTROL | 1Y1 | 1Y2 |
|--------|-------------------|----------|----------|
| н | Н | source | sink |
| Н | L | sink | source |
| L | X | disabled | disabled |

X = don't care H = high level L = low level



[†]Diodes are 1N4934 or equivalent.

FIGURE 3. TPIC0298 AS BIDIRECTIONAL DC MOTOR DRIVER



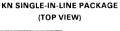
TPIC2404 INTELLIGENT-POWER QUAD LOW-SIDE SWITCH

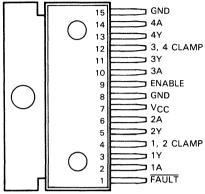
D3299, AUGUST 1989 - REVISED NOVEMBER 1989

- 1-A Current Capability Per Channel
- 45-V Inductive Switching Voltage Capability
- Current Sink Inputs Compatible with TTL or CMOS Devices
- Output Clamp Diodes for Inductive Transient Protection
- Independent Thermal Shutdown Protection
- Overvoltage Shutdown Protection
- Independent Channel Current Limit
- Error Sensing
- Extended Temperature Range of −40°C to 125°C

description

The TPIC2404 is a monolithic high-voltage highcurrent quadruple low-side switch especially designed for driving from low-level logic to peripheral loads such as relays, solenoids, motors, lamps, and other high-voltage highcurrent loads. The high-efficiency power switch is optimized for applications where a very rugged power switch is required. The device will tolerate power supply transients and reverse battery conditions up to 13 V.





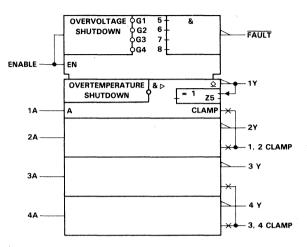
The tab is electrically connected to the GND pins.

The TPIC2404 features four inverting open-collector outputs controlled by a common-enable input. When ENABLE is low, the outputs are disabled. An error sensing circuit monitors load and device faults. When an error is sensed, the FAULT output goes to a low state. In addition, the device features on-board VCC overvoltage and thermal overload protection circuits, and the outputs are current-limit protected.

FUNCTION TABLE

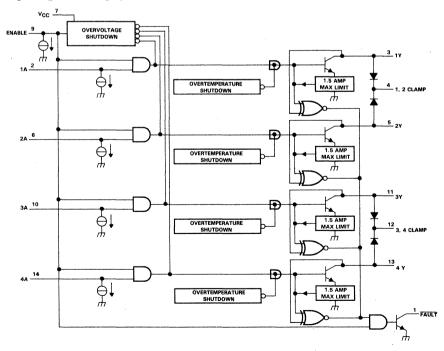
| | ENABLE | Α | Y | FAULT |
|--------------------------|-------------|-------------|-------------|-------------|
| Normal operation | H H L | H L X | L H H | H H H |
| Open load | ы | | | |
| Short to GND | 7 " | - | _ | _ |
| Overvoltage shutdown | П | | П | |
| Thermal shutdown | 7 " | ^ | " | _ |
| Short to V _{CC} | Н | Н | Н | L |

logic symbol†

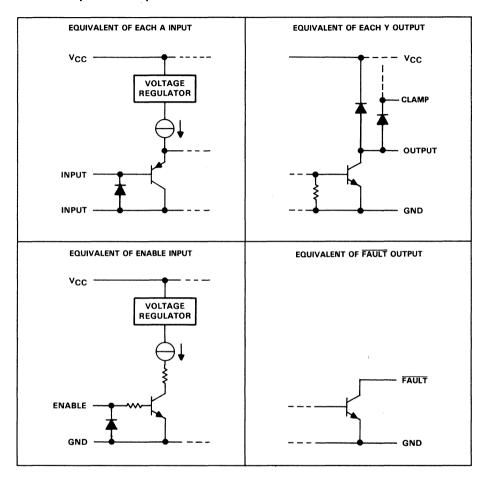


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage range, VCC (see Note 1) |
|--|
| Input voltage range, V ₁ |
| Output voltage range, VO |
| Output sustaining voltage, VO(sust) |
| Continuous output sink current (repetitive, tw < 8 ms), IOL (see Note 2) |
| Output clamp-diode voltage, VOK45 V |
| Continuous total dissipation at (or below) 25°C case temperature (see Note 3) 50 W |
| Operating case or virtual junction temperature range |
| Storage temperature range |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 s |

- NOTES: 1. All voltage values are with respect to the network ground terminal.
 - 2. Output sink current is limited by the overcurrent limit.
 - 3. For operation above 25°C free-air or case temperature refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below rated dissipation.

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

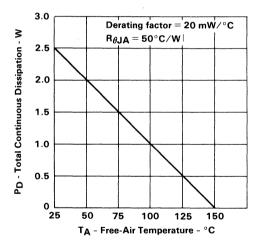


FIGURE 1

CASE TEMPERATURE DISSIPATION DERATING CURVE

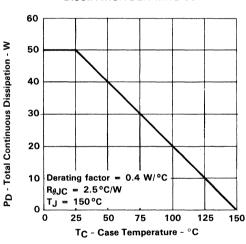


FIGURE 2

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|-------|-----|-----|------|
| Supply voltage, VCC | 9 | 12 | 16 | ٧ |
| High-level input voltage, VIH | 2 | | 5.5 | V |
| Low-level input voltage, V _{IL} | -0.3† | | 0.8 | V |
| Peak output voltage from external inductive kickback | | | 45 | V |
| Continuous output sink current | | | 1 | Α |
| Fault output sink current | | | 75 | μΑ |
| Operating free-air temperature, TA | -40 | | 125 | °C |

[†] The algebraic convention in which the least positive (most negative) value is designated minimum is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

| | PARAMETER | ************************************** | TEST CONDITIONS | MIN | TYP ‡ | MAX | UNIT | |
|--------------------|-----------------------------|--|---------------------------------------|-----|-------|------|----------|--|
| | | | V _O = 12 V, ENABLE low | | 15 | 100 | μΑ | |
| IO(off) | Off-state output current | | VO = 45 V, ENABLE high | | 0.6 | 2 | mA | |
| | | | VO = 12 V, ENABLE high | 200 | 400 | 600 | μΑ | |
| կլ | Low-level input current | | V _I = 0 to 0.8 V | -10 | 25 | 40 | μΑ | |
| | Lligh lovel input evenent | A inputs | | 10 | 25 | 60 | μΑ | |
| ΉΗ | High-level input current | ENABLE | | | 0.2 | 1 | mA | |
| | | | I _{OL} = 100 mA | | 0.1 | 0.15 | | |
| \/a. | Low-level output voltage | | I _{OL} = 500 mA | | 0.3 | 0.55 | V | |
| VOL | | | IOL = 1 A | | 0.8 | 1.3 | | |
| 1 | | | FAULT output, I _{OL} = 30 μA | | 0.2 | 0.4 | | |
| lOL | Low-level output current | | FAULT output, VOL = 1 V to 5.5 V | 50 | 90 | 125 | μΑ | |
| I _R (K) | Clamp diode reverse current | | $V_r = 50 \text{ V}, V_O = 0$ | | | 100 | μΑ | |
| V | Clamp diada farrand valtage | | lf = 1 A | | | 2 | V | |
| VF(K) | Clamp diode forward voltage | | I _f = 1.5 A | | | 2.5 | v | |
| | Supply current | | Outputs off, ENABLE low | | | 0.25 | | |
| Icc | | | Outputs on, T _A = -40°C | | | 120 | mA | |
| | | | Outputs on, TA = 25° C to 125°C | | | 100 | | |

operating characteristics over recommended operating free-air temperature and supply voltages (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|--------------------------------|------|------|------|------|
| High-level output sense voltage threshold | | | | 7 | V |
| Low-level output sense voltage threshold | | 3 | | | ٧ |
| Overcurrent limiting | $T_A = -40^{\circ}C$ | | | 1.85 | ۸ |
| Overcurrent infilting | T _A = 25°C to 125°C | | 1.2 | 7 | Α |
| V _{CC} Overvoltage shutdown | | 25.5 | | 31 | ٧ |
| V _{hvs} Overvoltages shutdown hysteresis | | | 0.25 | | ٧ |
| Thermal shutdown | | | 155 | | °C |
| Thermal shutdown hysteresis | | | 15 | | °C |
| Turn-on time | | | 8 | | μs |
| Turn-off time | | | 8 | | μs |

[‡] All typical values are at V_{CC} = 12 V, T_A = 25 °C.



TPIC2406 INTELLIGENT-POWER QUAD MOSFET LATCH

D3378, FEBRUARY 1990

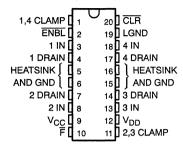


- 4 Output Channels of 700-mA Nominal Current Per Channel
- Pulsed Current 3 A Per Channel
- Low r_{DS(on)} . . . 0.5 Ω Typ
- Avalanche Energy . . . 50 mJ
- Thermal Shutdown Protection with Fault (Overtemperature) Output
- NE Package Designed for Heat Sinking
- Integral Output Clamp Diodes
- Input Transparent Latches for Data Storage
- Asynchronous Clear to Turn Off All Outputs
- Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current

description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The

NE PACKAGE (TOP VIEW)



FUNCTION TABLE (each channel)

| | (ea | nnei) | | | |
|---------------------|------|-------|----|----------------|-------|
| FUNCTION | IN | PUTS | | OUTPUT | FAULT |
| FUNCTION | ENBL | CLR | IN | Υ | F |
| NORMAL OPERATION | Х | L | Х | Н | Н |
| | L | Н | L | Н | Н |
| | L | Н | Н | L | н |
| | Н | Н | Х | Q ₀ | н |
| THERMAL SHUTDOWN | х | х | х | н | L |

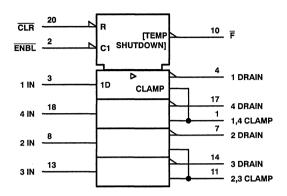
H = high-level, L = low-level, X = irrelevant

device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

Each device features four inverting open-drain outputs each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The $\overline{\text{CLR}}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{\text{ENBL}}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs will be held off while $\overline{\text{CLR}}$ is low, but will return to the stages on the data inputs when $\overline{\text{CLR}}$ goes high. When $\overline{\text{ENBL}}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If the $\overline{\text{CLR}}$ input is taken low, the data in the latches is cleared, turning all outputs off. If $\overline{\text{CLR}}$ is taken high again, $\overline{\text{ENBL}}$ must be cycled low to read new data into the latch.

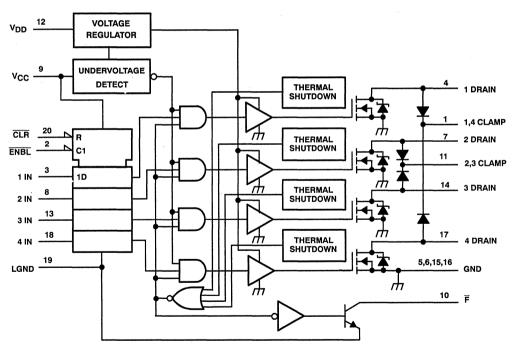
TPIC2406 INTELLIGENT-POWER QUAD MOSFET LATCH

logic symbol†

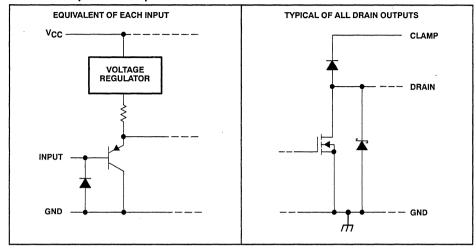


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over - 40°C to 125°C case temperature range (unless otherwise noted)

| Logic supply voltage, V _{CC} (see Note 1) |
|---|
| Power MOSFET driver supply voltage, V _{DD} |
| Logic input voltage, V ₁ |
| Power MOSFET drain-source voltage, V _{DS} |
| Foutput voltage |
| Clamp diode voltage |
| Continuous source-drain diode anode current |
| Pulsed source-drain diode anode current |
| Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, |
| T _A = 25°C (see Note 2 and Figures 5 through 8) |
| Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $I_{A} = 25^{\circ}C$ 770 mA |
| Peak drain current, single output, I _{DM} , T _A = 25°C (see Note 3) |
| Single-pulse avalanche energy, EAS |
| Continuous total dissipation at or below 25°C free-air temperature (see Note 4) |
| Continuous total dissipation at or below 100°C case temperature (see Note 4) |
| Operating junction temperature range, T _J – 40°C to 150°C |
| Storage temperature range |
| Lead temperature |
| 200 O |

- NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
 - 2. Pulse duration = 10 ms, duty cycle = 6%.
 - 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
 - 4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

TPIC2406 INTELLIGENT-POWER QUAD MOSFET LATCH

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|---|------|-----|-----|------|
| Logic supply voltage, VCC | | 4.5 | | 5.5 | V |
| Output supply voltage, VDD | | 10 | | 35 | V |
| High-level input voltage, VIH | | 2 | | | V |
| Low-level input voltage, VIL | | | | 0.6 | V |
| Setup time, t _{SU} , data before ENBL † | Setup time, t _{SU} , data before ENBL ↑ (see Figure 1) | | | | ns |
| Hold time, th, data after ENBL ↑ (see | Figure 1) | 100 | | | ns |
| Pulse duration, tw (see Figure 1) | ENBL low | low | | | |
| Fulse duration, tw (see Figure 1) | CLR low | .300 | | | ns |
| Operating case temperature, TC | | - 40 | | 125 | °C |

electrical characteristics, V_{CC} = 5 V, V_{DD} = 14 V, T_{C} = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---|--|--|-----|------|-------|------|
| V _{(BR)DSX} | Drain-source breakdown voltage | I _D = 1 mA | | 60 | | | ٧ |
| V _{F(K)} | Clamp diode forward voltage | IF = 1.25 A, | See Notes 5 and 6 | | | 1.6 | V |
| V _{SD} | Source-drain diode forward voltage | Is = 1.25 A, | See Notes 5 and 6 | | | 1.5 | ٧ |
| VIK | Input clamp voltage | V _{CC} = MIN, | lj = ~ 12 mA | | | - 1.5 | V |
| VOL | F low-level output voltage | IOL = 4 mA | | | 0.4 | | V |
| ¹IH . | High-level input current | V _{CC} = 5.5 V, | V _I = 2.7 V | | | 20 | μΑ |
| ΊL | Low-level input current | V _{CC} = 5.5 V, | V _I = 0.4 V | | | 0.1 | mA |
| Icc | Logic supply current | I _O = 0, | All outputs off | | | 10 | mA |
| IN | Nominal current | V _{DS(on)} = 0.5 V, T _C = 85°C, | I _N = I _D , See Notes 5, 6, and 7 | | 700 | | mA |
| IDD | Output supply current | IO = 0, | All outputs off | | | 6 | mA |
| | Olemen die de monerat | V _{DS} = 55 V, | V _O = 0 | | | 1 | |
| ^I R(K) | Clamp-diode reverse current | V _{DS} = 55 V, | $V_O = 0$, $T_C = 125$ °C | | | 10 | μΑ |
| 1 | 0"-1-1-1-1-1-1-1-1 | V _R = 55 V | | T | | 1 | |
| IDSX | Off-state drain current | V _R = 55 V, | T _C = 125°C | | | 10 | μΑ |
| 10(F) | High-level fault leakage current | V _{OH} = 5.5 V | | | | 1 | μА |
| | Static drain-source on-state resistance | I _D = 1.25 A | | | 0.5 | 0.6 | |
| rDS(on) | | I _D = 1.25 A, T _C = 125°C | See Notes 5 and 6 | | 0.8 | 1 | Ω |
| | | I _D = 3 A | | | 0.55 | 0.65 | |

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

^{7.} Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C at case temperature.

TPIC2406 INTELLIGENT-POWER QUAD MOSFET LATCH

switching characteristics, $V_{CC} = 5 \text{ V}$, $V_{DD} = 24 \text{ V}$, $T_{C} = 25 ^{\circ}\text{C}$

| | PARAMETER | TEST CON | MIN TYP | MAX | UNIT | |
|------------------|---|---------------------------------|-----------------------------------|-----|------|----|
| tPLH | Propagation delay time, low-to-high-level drain output from clock | | | 450 | | ns |
| tPHL | Propagation delay time, high-to-low-level drain output from clock | C _L = 30 pF, | See Figure 1 | 550 | | ns |
| tTLH | Transition time, low-to-high-level of source-drain output | 1 | | 35 | | ns |
| tTHL | Transition time, high-to-low-level of source-drain output | | | 30 | | ns |
| ^t DLH | Delay time, low-to-high-level drain output from input | | | 380 | | ns |
| tDHL | Delay time, high-to-low-level drain output from input | C _L = 30 pF, | See Figure 2, | 380 | | ns |
| tRLH | Rise time, low-to-high-level of source-drain output | $I_D = I_N = 700 \text{ mA}$ | | 35 | | ns |
| tFHL | Fall time, high-to-low-level of source-drain output | 7 | | 70 | | ns |
| ta | Reverse-recovery-current rise time | IF = 3 A, See Notes 5 and 6, | di/dt = 100 A/μs, See Figure 3 | 45 | | ns |

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.

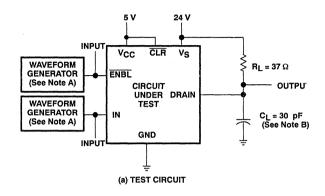
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

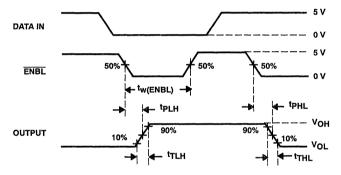
thermal resistance

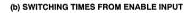
| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|-----------------------------------|-----|-----|------|------|
| R ₀ JC | Junction-to-case thermal resistance | All four outputs with equal power | | | 8.33 | °C/W |
| ReJA | Junction-to-ambient thermal resistance | All four outputs with equal power | | | 50 | °C/W |

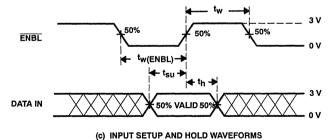
operating characteristics over - 40°C to 125°C case temperature range

| | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|------------------------------|-----|-----|-----|------|
| Vcc | Undervoltage shutdown | 3 | | 4.5 | V |
| | Thermal shutdown temperature | | 155 | | °C |
| | Thermal shutdown hysteresis | | 15 | | °C |





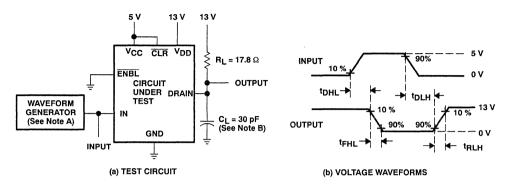




NOTES: A.The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 300$ ns, PRR = 5 kHz, $Z_0 = 50 \Omega$. B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES





NOTES: A.The pulse generator has the following characteristics: $t_f \le 10$ ns, $t_f \le 10$ ns, $t_W = 5$ ms, PRR = 5 kHz, $Z_0 = 50 \Omega$. B.C₁ includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

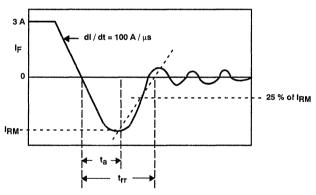
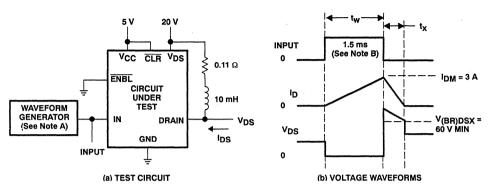


FIGURE 3. REVERSE-RECOVERY-CURRENT WAVEFORMS OF SOURCE-DRAIN DIODE

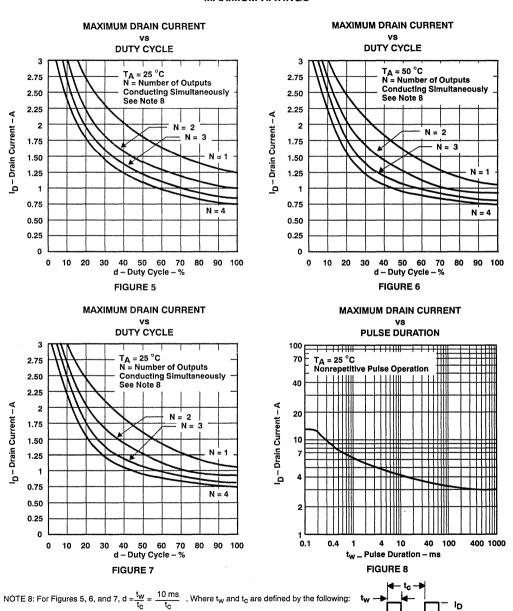


NOTES: A.The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_W = 1$ ms, PRR = 5 kHz, $Z_0 = 50 \Omega$. B. Input pulse duration is increased until peak current $I_{DM} = 3$ A.

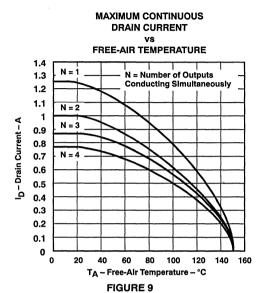
Energy test level is defined as
$$E_{AS} = \frac{I_{DM} \times V_{(BR)DSX} \times t_{X}}{2} = 50 \text{ mJ min.}$$

FIGURE 4. SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT AND WAVEFORMS

MAXIMUM RATINGS



MAXIMUM RATINGS



DISSIPATION DERATING CURVE 3 Derating factor = 20 mW/°C R_ΘJA = 50°C/W 1.5 1.5 0.5 0.5

FREE-AIR TEMPERATURE

TRANSIENT THERMAL IMPEDANCE vs

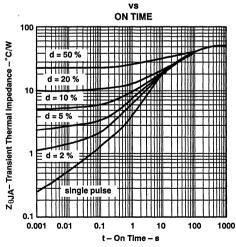


FIGURE 11

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

FIGURE 10

75

TA - Free-Air Temperature - °C

100

125

150

$$\begin{split} Z_{\theta JA} \; &= \left| \begin{array}{c} t_{\mathrm{W}} \\ t_{\mathrm{c}} \end{array} \right| \, R_{\theta JA} \; + \; \left| \begin{array}{c} 1 \; - \; t_{\mathrm{w}} \\ t_{\mathrm{c}} \end{array} \right| \, Z_{\theta (t_{\mathrm{w}} \; + \; t_{\; c})} \\ &+ \; Z_{\theta (t_{\mathrm{w}})} \; - \; Z_{\theta (t_{\mathrm{c}})} \end{split}$$

Where:

0

0

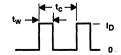
25

 $Z_{\theta}(t_w) = \text{the single-pulse thermal impedance}$ for $t = t_w \text{ seconds}$

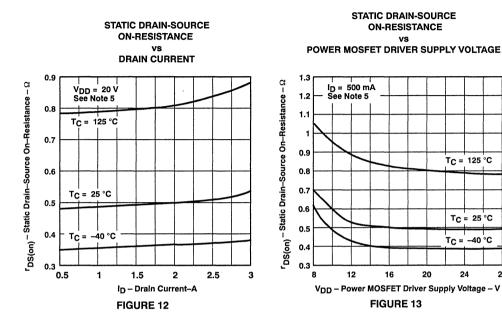
 $Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = t_c seconds

 $Z_{\theta(t_W + t_C)} = \text{ the single-pulse thermal impedance} \\ \text{ for } t = t_W + t_C \text{ seconds}$

 $d = t_w/t_c$



TYPICAL CHARACTERISTICS



NOTE 5: Technique should limit $T_{\dot{l}}$ – $T_{\dot{C}}$ to 10°C maximum.

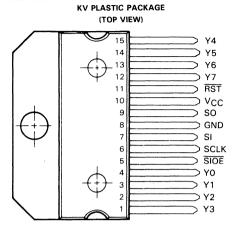
24

28

OCTAL INTELLIGENT-POWER SWITCH WITH SERIAL INPUT

D3282 AUGUST 1989 - REVISED JUNE 1990

- 8-Bit Serial-In Parallel-Out Driver
- 1-A Output Current Capability per Channel or 8-A Total Current
- Over-Current Limiting and Out-of-Saturation Voltage Protection on Driver Outputs
- Contains Eight Open-Collector Saturating Sink Outputs with Low On-State Voltage
- High-Impedance Inputs with Hysteresis are Compatible with TTL or CMOS Levels
- Very Low Standby Power . . . 20 mW Typical
- Status of Output Drivers May Be Monitored at Serial Output
- 3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections
- 25-V Transient Clamping with Inductive Switching on Outputs, 40-mJ Rating per **Driver Output**



The tab is electrically connected to pin 8.

description

The TPIC2801 is a monolithic BIDFET[†] integrated circuit that is designed to sink currents up to 1 A at 30 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

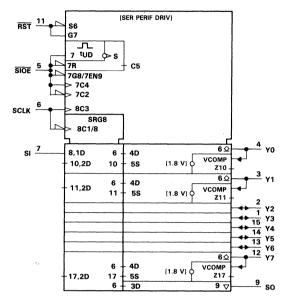
Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic high bit at SI_n turns the corresponding output driver (Y_n) off. A logic low bit at SI_n turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of serial clock (SCLK) input in 8-bit bytes with data for Y7 output (MSB) first and data for Y0 output (LSB) last. Both SI and SCLK are active when serial input-output enable (SIOE) input is low and are disabled when SIOE is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. An activated driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of SIOE transfers the logic state of the comparator output to the shift register.

[†] BIDFET – Bipolardouble-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

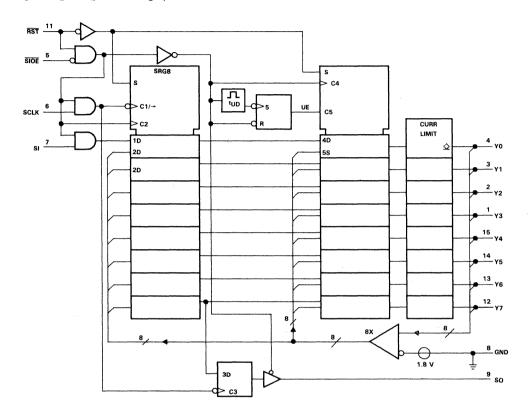


logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TPIC2801 OCTAL INTELLIGENT-POWER SWITCH WITH SERIAL INPUT

| PI | N | 1/0 | DESCRIPTION |
|--|------------------------------------|-----|---|
| NAME | NO. | 1/0 | DESCRIPTION |
| GND | 8 | | Ground. Common return for entire chip. The current out of this pin is potentially as high as 4 A if all outputs are on. This ground is used for both logic and power circuits |
| RST | 11 | 1 | Reset. An asynchronous reset is provided for the shift register and the parallel latches. This pin is active when low and has no internal pulllup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to VCC. |
| SCLK | 6 | 1 | Serial Clock. This pin clocks the shift register. The serial output (SO) will change state on the rising edge of this clock and serial input (SI) data will be accepted on the falling edge. |
| SI | 7 | ı | Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be off and a low will turn it on. |
| SIOE | 5 | ı | Serial Input-Output Enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver for the serial output (SO) pin is enabled when this pin is low, provided RST is high. |
| so | 9 | 0 | Serial Output. This pin is the serial 3-state output from the shift register and is in a high-impedance state when \overline{SIOE} is high or \overline{RST} is low. A high for a data bit on this pin indicates that the corresponding power output (Y_n) is high. This could mean that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage sense indicator. A low on this pin for a data bit indicates that the corresponding power output (Y_n) is low (an "on" output stage or open-circuit condition). |
| Vcc | 10 | | 5-V supply voltage |
| Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 | 4 3 2 1 15 14 13 | o | Power Outputs. The outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, but the current limiting is set to a minimum of 1.2 Å. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-K\(\Omega\) pull-down resistors are provided at each output. These resistors hold the output low during an open-circuit condition. |

PRINCIPLES OF OPERATION

timing data transfer

Figure 1 shows the overall 8-bit data-byte transfer to and from the TPIC2801 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t₀ on the high-to-low transition of SIOE. Therefore, the SO output data (DY0, DY1...) represents the conditions at the Y-driver outputs at time t₀. The data at SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 1 on the SI input, input data DI7 is clocked in at time t_1 , DI6 is clocked in at time t_2 , etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of $\overline{\text{SIOE}}$ parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO) and this allows other devices to be cascaded in a daisy chain with the TPIC2801. Once the last data bit has been shifted into the TPIC2801, the SIOE input should be pulled high. The clock (SCLK) input should be low at both transitions of the SIOE input to avoid any false clocking of the shift register. The SCLK input is gated by the SIOE input, so the SCLK input is ignored whenever the SIOE is high. At the rising edge of the SIOE input, the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs will be protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions will be inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay has ended, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.



PRINCIPLES OF OPERATION

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the the device. If the diagnostic bit for that output comes back as a low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte should be clocked into the TPIC2801. The diagnostic bit clocked back from the TPIC2801 in the subsequent data transfer should indicate a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte. After a sufficient time delay, another control byte (same byte can be used) is clocked in. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high will result.

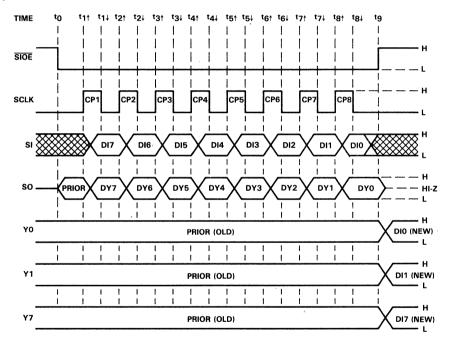
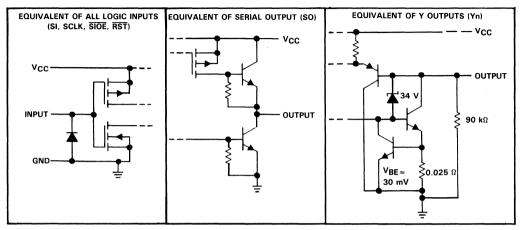


FIGURE 1. DATA-BYTE TRANSFER TIMING

TPIC2801 OCTAL INTELLIGENT-POWER SWITCH WITH SERIAL INPUT

schematics of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

| Supply voltage range, V _{CC} (see Note 1) |
|---|
| Input voltage, V _I |
| Output voltage range at SO |
| Input current, I ₁ |
| Peak output sink current at Y, IO repetitive, t _W = 10 ms, |
| duty cycle = 50%, see Notes 2 and 3 |
| Continuous output current at Y, IO (see Note 3) |
| Peak current through GND terminal: |
| Nonrepetitive t _W = 0.2 ms |
| Repetitive, t _W = 10 ms, duty cycle = 50% |
| Continuous current through GND terminal |
| Output clamp energy, EOK (after turning off IO(on) = 0.5 A) |
| Continuous dissipation at (or below) 25°C free-air temperature (see Note 4) 3.575 W |
| Continuous dissipation at (or below) 75°C case temperature (see Note 4) |
| Operating case or virtual-junction temperature range |
| Storage temperature range – 65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260°C |
| |

- NOTES: 1. All voltage values are with respect to network ground terminal.
 - 2. Each Y output is individually current limited with a typical over-current limit of about 1.4 A.
 - 3. Multiple Y outputs of this device may conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND current must fall within the GND-terminal current range.
 - For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case
 temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings
 must not be exceeded.

recommended operating conditions

| | , N | IIN | NOM | MAX | UNIT |
|---|-------|-----|-----|---------------------|------|
| Supply voltage, VCC | 4 | .75 | 5 | 5.25 | ٧ |
| High-level input voltage, V _{IH} | 0.7 V | CC | | 5.25 | ٧ |
| Low-level input voltage, V _{IL} | _ | 0.3 | | 0.2 V _{CC} | ٧ |
| Output voltage, VO(off) | | | | 30 | ٧ |
| Continuous output current, IO(on) | | | | 1 | Α |
| Operating case temperature, TC | - | -40 | 25 | 105 | °C |

timing requirements (see Figure 2)

| | PARAMETER | FROM | то | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|----------------------------|------|-------|-----------------|------|-----|------|
| fSCLK | Clock frequency | | | | 0 | 500 | kHz |
| twsclkh | Pulse duration, SCLK high | | | | 840 | | ns |
| twsclkl | Pulse duration, SCLK low | | | | 840 | | ns |
| twRST | Pulse duration, RST low | | | | 1000 | | ns |
| t _{su1} | Setup time | SIOE | SCLK† | | 1000 | | ns |
| t _{su2} | Setup time | SCLK | SIOE↑ | | 1000 | | ns |
| t _{su3} | Setup time | SI | SCLK | | 500 | | ns |
| t _{h1} | Hold time | SCLK | SI | | 500 | | ns |
| t _r | Rise time (SCLK, SI, SIOE) | | | | | 2 | μs |
| tf | Fall time (SCLK, SI, SIOE) | | | | | 2 | μs |

electrical characateristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

driver array outputs (Y0 to Y7)

| | PARAMETER | TEST CONDI | TEST CONDITIONS | | | MAX | UNIT |
|------------------|-------------------------------------|--|---|-----|-----|-----|------|
| VOK. | Output clamp voltage | IO = 0.5 A, output programmed to ground | I _O = 0.5 A, output programmed off and current shunted to ground | | | 40 | ٧ |
| IO(off) | Off-state output current | VO = 24 V with output programr | VO = 24 V with output programmed off | | | | mA |
| IO(CL) | Output current limit | V _O = 3 V with output programmed on | | | 1.4 | | Α |
| | On-state output voltage | With output programmed on | I _{OL} = 0.5 A | | 0.4 | 0.5 | V |
| V0() | | | I _{OL} = 0.75 A | | 0.6 | 1 | V |
| VO(on) | | I _{OL} = 1 A, During unlatch disable | | | 0.8 | 1.5 | ٧ |
| v _{tos} | Out of saturation threshold voltage | With output programmed on and condition | an over-current fault | 1.6 | 1.8 | 2 | V |

shift register (inputs SI, SIOE, SCLK, and RST)

| | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|---------------------------------------|---------------------|---------------------|------|
| V _{T+} | Positive-going threshold voltage | | | 0.7 V _{CC} | V |
| V _T _ | Negative-going threshold voltage | | 0.2 V _{CC} | | V |
| V _{hys} | Hysteresis voltage (V _{T+} V _{T-}) | | 0.85 | 2.25 | V |
| lj. | Input current | V _I = 0 to V _{CC} | | ±10 | μΑ |
| Ci | Inpout capacitance | V _I = 0 to V _{CC} | | 20 | pF |

[†] All typical values are at V_{CC} = 5 V, T_J = 25°C.

TPIC2801 OCTAL INTELLIGENT-POWER SWITCH WITH SERIAL INPUT

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

shift register (output SO)

| | PARAMETER | TEST CONDITION | TEST CONDITIONS | | | MAX | UNIT |
|-----|---------------------------|---|-------------------------|--|---|-----|------|
| VOL | Low-level output voltage | I _O = 1.6 mA | I _O = 1.6 mA | | | 0.4 | ٧ |
| Vон | High-level output voltage | $I_{O} = -0.8 \text{ mA}$ | V _{CC} -1.3 | | | ٧ | |
| 10 | Output current | V _O = 0 to V _{CC} , SIOE input high | | | | ±10 | μΑ |
| lcc | Supply current | All outputs on, I _O = 0.5 A at all outputs | T _J = 105°C | | | 150 | |
| | | | T _J = 25°C | | | 200 | mA |
| | | | $T_J = -40^{\circ}C$ | | | 250 | 1 |
| lcc | Supply current | All outputs off | T _J = 25°C | | 4 | 10 | mA |
| CO | Output capacitance | V _O = 0 to V _{CC} , SIOE input high | | | | 20 | pF |

[†] All typical values are at V_{CC} = 5 V, T_J = 25°C.

thermal characteristics

| | PARAMETER | MIN MAX | UNIT |
|-------------------|---|---------|--------|
| R ₀ JC | Thermal resistance, junction-to-case temperature | | °C/W |
| R ₀ JA | Thermal resistance, junction-to-ambient temperature | 3: | 5 °C/W |

switching characteristics over recommended ranges of supply voltage and operating case temperatures (unless otherwise noted)

| | PARAMETER | FROM | то | TEST CO | NDITIONS | MIN | MAX | UNIT |
|---------------------|--|-------|----|--|--|-----|------|------|
| t _{en} | Enable time | SIOE | so | CL = 20 pF,See Figure 3 | $R_L = 2 k\Omega$, | | 1000 | ns |
| ^t dis | Disable time | SIOE↑ | so | C _L = 20 pF,See Figure 3 | $R_L = 2 k\Omega$, | | 1000 | ns |
| t _{d1} | Delay time, valid data | SCLK† | so | C _L = 200 pF, | See Figure 4 | | 740 | ns |
| t _{d2} | Delay time, unlatch disable | SIOE† | Yn | CL = 20 pF,See Figure 5 | $R_L = 5 \Omega$, | 75 | 250 | μs |
| t _{r(so)} | Rise time, SO | | | C _L = 200 pF, | See Figure 4 | | 150 | ns |
| t _f (so) | Fall time, SO | | | C _L = 200 pF, | See Figure 4 | | 150 | ns |
| ^t d(on) | Delay time, turn-on | SIOE↑ | Yn | $I_{OL} = 500 \text{ mA},$ $R_L = 28 \Omega,$ | C _L = 20 pF,See Figure 6 | | 10 | μs |
| ^t d(off) | Delay time, turn-off | SIOE↑ | Yn | $I_{OL} = 500 \text{ mA},$ $R_L = 28 \Omega,$ | C _L = 20 pF,See Figure 6 | | 10 | μs |
| t _V | Valid time, SO output data remains valid after SCLK high | SCLK† | so | CL = 200 pF, | See Figure 4 | 0 | | ns |

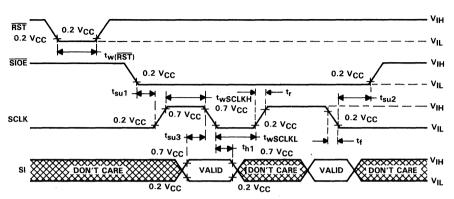
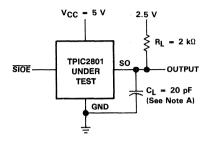
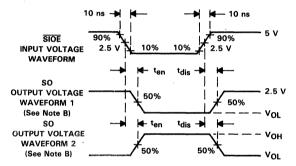


FIGURE 2. INPUT TIMING WAVEFORMS



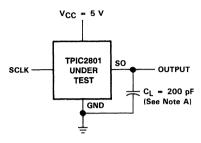
TEST CIRCUIT FOR ENABLE AND DISABLE TIMES



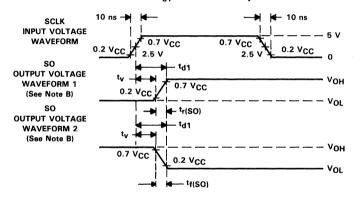
NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when SIOE is high. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control when SIOE is high.

FIGURE 3. VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



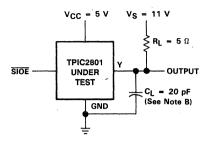
TEST CIRCUIT FOR VALID DATA
DELAY TIME t_{d1} AND VALID TIME t_v



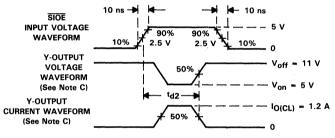
NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from low to high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES



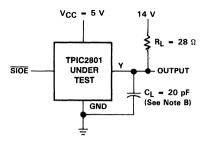
TEST CIRCUIT FOR UNLATCH DISABLE DELAY TIME t_{d2} (See Note A)



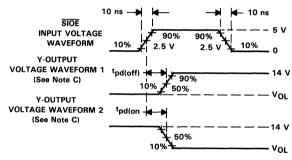
NOTES: A. t_{d2} = delay until Y-output current goes off under fault condition.

- B. C_L includes probe and jig capacitance.
- C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of SIOE causes the output to switch from being off to being on.
- D. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{OR} is greater than the maximum out-of-saturation threshold voltage, V_{TOS}. Thus, V_{OL} = V_{on} > V_{TOS(max)} = 1.98 V.

FIGURE 5. VOLTAGE AND CURRENT WAVEFORMS FOR UNLATCH DISABLE DELAY



TEST CIRCUIT FOR TURN-OFF td(off) AND TURN-ON td(on) DELAY TIMES (See Note A)

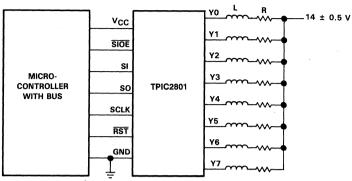


NOTES: A. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$. B. CL includes probe and jig capacitance.

C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SIOE causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such the low-to-high transition of SIOE causes the output to switch from off to on.

FIGURE 6. VOLTAGE WAVEFORMS FOR TURN-OFF AND TURN-ON DELAY TIMES

TYPICAL APPLICATION DATA



 $V_{CC} = 5 V \pm 5\%$ $R = 30 \Omega \pm 5\%$ $L = 10 \text{ mH} \pm 10\%$

8 LOADS UP TO 0.5 A EACH

FIGURE 7. MICROCONTROLLER DRIVING EIGHT LOADS USING A TPIC2801 FOR LOAD INTERFACE

ULN2001A THRU ULN2005A DARLINGTON TRANSISTOR ARRAYS

D2624, DECEMBER 1976-REVISED SEPTEMBER 1986

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series

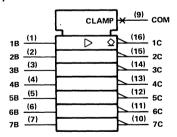
| D OR N PACKAGE (TOP VIEW) | | | | | | | |
|------------------------------|------------|-----------------|-------|--|--|--|--|
| 1B [| ſī | U ₁₆ |]1C | | | | |
| 2B [| 2 | 15 | 2C | | | | |
| 3B [|]3 | 14 |]3C | | | | |
| 4B [|]4 | 13 |] 4C | | | | |
| 5B [| 1 5 | 12 |] 5C | | | | |
| 6B [| 6 | 11 |] 6C | | | | |
| 7B [| 17 | 10 |] 7C | | | | |
| E [| [8 | 9 | 🛚 сом | | | | |

description

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

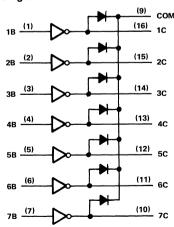
The ULN2001A is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-k Ω series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A. The ULN2005A has a 1050- Ω series base resistor and is specifically designed for use with TTL devices where higher output current is required and loading of the driving source is not a concern.

logic symbol†



 $^{^{\}dagger}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

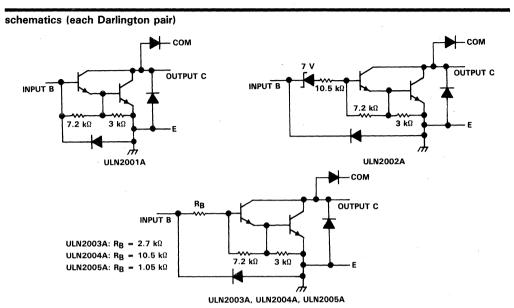




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ULN2001A THRU ULN2005A DARLINGTON TRANSISTOR ARRAYS



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

| Collector-emitter voltage |
|---|
| Input voltage (see Note 1): ULN2002A, ULN2003A, ULN2004A |
| ULN2005A |
| Peak collector current (see Figures 14 and 15) |
| Output clamp diode current |
| Total emitter-terminal current |
| Continuous total power dissipation See Dissipation Rating Table |
| Operating free-air temperature range |
| Storage temperature range65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

| PACKAGE | T _A = 25°C POWER RATING | DERATING FACTOR ABOVE TA = 25°C | T _A = 85°C POWER RATING |
|---------|---------------------------------------|---------------------------------|---------------------------------------|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| N | 1150 mW | 9.2 mW/°C | 598 mW |



electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| | DADAMETED | TEST | TEST CONDITIONS | U | LN200 | 1A | U | LN200 | 2A | UNIT |
|--------------------|-----------------------------|---------------------------------------|--|------|-------|-----|-----|-------|------|------|
| | PARAMETER | FIGURE | 1EST CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | ONL |
| | | 1 | VCE = 50 V, II = 0 | | | 50 | | | 50 | |
| ICEX | Collector cutoff current | ' ' | V _{CE} = 50 V, I _I = 0 | | | 100 | | | 100 | μΑ |
| | | 2 | $T_A = 70^{\circ}C V_I = 6 \text{ V}$ | | | | | | 500 | |
| lu en | Off-state input current | 3 | $V_{CE} = 50 \text{ V}, I_{C} = 500 \mu\text{A}$ | 50 | 65 | | 50 | 65 | | μΑ |
| l(off) | On-state input current | , , , , , , , , , , , , , , , , , , , | T _A = 70°C | | | | | | | μ., |
| lj | Input current | 4 | V _I = 17 V | | | , | | 0.82 | 1.25 | mA |
| bee | Static forward current | 5 | V _{CF} = 2 V, I _C = 350 mA | 1000 | | | | | | |
| hFE | transfer ratio | J 3 | VCE = 2 V, IC = 350 III | 1000 | | | | | | |
| V _{I(on)} | On-state input voltage | 6 | V _{CE} = 2 V, I _C = 300 mA | | | | | | 13 | ٧ |
| | Collector-emitter | | $I_1 = 250 \mu\text{A}, \ I_C = 100 \text{mA}$ | \ \ | 0.9 | 1.1 | | 0.9 | 1.1 | |
| VCE(sat) | saturation voltage | 5 | $I_1 = 350 \mu A$, $I_C = 200 \text{mA}$ | | 1 | 1.3 | | 1 | 1.3 | V |
| | saturation voltage | | $I_1 = 500 \mu A$, $I_C = 350 \text{mA}$ | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| 1- | Clamp diada revenes evenest | 7 | V _R = 50 V | | | 50 | | | 50 | |
| I'R | Clamp diode reverse current | / | $V_R = 50 \text{ V}, T_A = 70 ^{\circ}\text{C}$ | | | 100 | | | 100 | μΑ |
| VF | Clamp diode forward voltage | 8 | I _F = 350 mA | | 1.7 | 2 | | 1.7 | 2 | V |
| Ci | Input capacitance | | $V_{\parallel} = 0$, $f = 1 \text{ MHz}$ | | 15 | 25 | | 15 | 25 | pF |

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| | PARAMETER | TEST | TEST CO | NDITIONS | U | LN200 | 3 A | UI | LN200 | 4A | UNIT |
|----------------------|------------------------------|--------|--|-------------------------|----|-------|------------|-----|-------|------|------|
| | PARAMETER | FIGURE | 1251 CO | TEST CONDITIONS | | TYP | MAX | MIN | TYP | MAX | UNII |
| | | 1 | $V_{CE} = 50 \text{ V},$ | 11 = 0 | | | 50 | | | 50 | |
| ICEX | Collector cutoff current | ' | $V_{CE} = 50 V$ | I _I = 0 | | | 100 | | | 100 | μΑ |
| | - | 2 | $T_A = 70$ °C | V ₁ = 1 V | | | | | | 500 | |
| l _{l(off)} | Off-state input current | 3 | $V_{CE} = 50 \text{ V},$ $T_{A} = 70 ^{\circ}\text{C}$ | $I_C = 500 \mu A$, | 50 | 65 | | 50 | 65 | | μΑ |
| | | | $V_{I} = 3.85 V$ | | | 0.93 | 1.35 | | | | |
| կ | Input current | 4 | V _I = 5 V | | | | | | 0.35 | 0.5 | mA |
| | | | V _I = 12 V | | | | | | 1 | 1.45 | |
| | | | | $I_C = 125 \text{ mA}$ | | | | | | 5 | |
| | | | | $I_C = 200 \text{ mA}$ | | | 2.4 | | | 6 | |
| V _{I(on)} | On-state input voltage | 6 | V _{CE} = 2 V | $I_C = 250 \text{ mA}$ | | | 2.7 | | | | v |
| VI(ON) | On-state input voitage | " | VCE - 2 V | $I_C = 275 \text{ mA}$ | | | | | | 7 | |
| | | | | $I_C = 300 \text{ mA}$ | | | 3 | | | | |
| | | | | I _C = 350 mA | | | | | | 8 | |
| | Collector-emitter | Ì | $I_{\parallel} = 250 \mu A$ | $I_C = 100 \text{ mA}$ | | 0.9 | 1.1 | | 0.9 | 1.1 | |
| V _{CE(sat)} | saturation voltage | 5 | | $I_C = 200 \text{ mA}$ | | 1 | 1.3 | | 1 | 1.3 | V |
| | | | | $I_C = 350 \text{ mA}$ | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| I _R | Clamp diode reverse current | 7 | $V_R = 50 V$ | | | | 50 | | | 50 | μΑ |
| 'n | Statis diede tovelee duiteit | | $V_R = 50 V$, | $T_A = 70$ °C | | | 100 | | | 100 | |
| ٧ _F | Clamp diode forward voltage | 8 | $I_F = 350 \text{ mA}$ | | | 1.7 | 2 | | 1.7 | 2 | V |
| Ci | Input capacitance | | $V_{\parallel} = 0$, | f = 1 MHz | | 15 | 25 | | 15 | 25 | рF |

ULN2001A THRU ULN2005A DARLINGTON TRANSISTOR ARRAYS

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| 22 | PARAMETER | TEST CONDITIONS | | | | A | |
|----------------------|-----------------------------|-----------------|---|---------|-----|-----|------|
| | ranawe i en | | TEST CONDITIONS | MIN TYP | | MAX | UNIT |
| I | Collector cutoff current | 1 | V _{CE} = 50 V, I _I = 0 | | | 50 | |
| CEX | Collector cutoff current | ' ' | $V_{CE} = 50 \text{ V}, I_{I} = 0, T_{A} = 70 ^{\circ}\text{C}$ | | | 100 | μΑ |
| l(off) | Off-state input current | 3 | $V_{CE} = 50 \text{ V}, I_{C} = 500 \mu\text{A}, T_{A} = 70 ^{\circ}\text{C}$ | 50 | 65 | | μΑ |
| lį . | Input current | 4 | V _I = 3 V | | 1.5 | 2.4 | mA |
| V _{I(on)} | On-state input voltage | 6 | $V_{CE} = 2 \text{ V}, I_{C} = 350 \text{ mA}$ | | | 2.4 | ٧ |
| | Collector-emitter | | l _I = 250 μA, l _C = 100 mA | | 0.9 | 1.1 | |
| V _{CE(sat)} | saturation voltage | 5 | $I_1 = 350 \mu\text{A}, I_C = 200 \text{mA}$ | | · 1 | 1.3 | ٧ |
| | saturation voltage | | $I_1 = 500 \mu A$, $I_C = 350 \text{mA}$ | | 1.2 | 1.6 | |
| | Oleman die de | T - | V _R = 50 V | | | 50 | |
| ^I R | Clamp diode reverse current | 7 | $V_{R} = 50 \text{ V}, T_{A} = 70 ^{\circ}\text{C}$ | | | 100 | μΑ |
| ., | Clamp diode forward | | L 250 A | | | 2 | ٧ |
| ٧F | voltage | 8 | IF = 350 mA | 1 | 1.7 | 2 | V |
| Ci | Input capacitance | 1 | V _I = 0, f = 1 MHz | | 15 | 25 | pF |

switching characteristics at 25 °C free-air temperature

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|--|--|--------------------|------|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | See Figure 9 | | 0.25 | 1 | μS |
| tPHL | Propagation delay time, high-to-low-level output | See rigure 9 | | 0.25 | 1 | μs |
| Voн | High-level output voltage after switching | $V_S = 50 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 10 | V _S -20 | | | mV |

PARAMETER MEASUREMENT INFORMATION

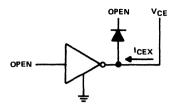


FIGURE 1. ICEX

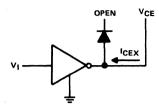


FIGURE 2. ICEX

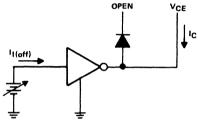


FIGURE 3. II(off)

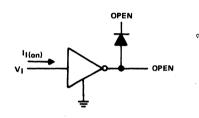
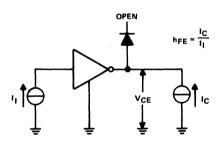


FIGURE 4. I



NOTE: II is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

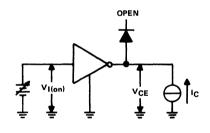
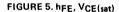
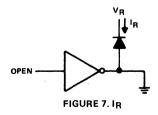
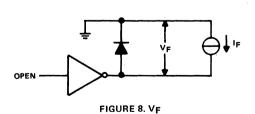


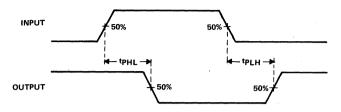
FIGURE 6. VI(on)





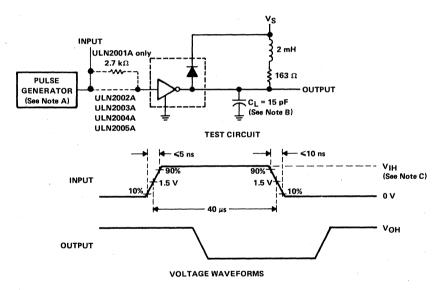


PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 9. PROPAGATION DELAY TIMES



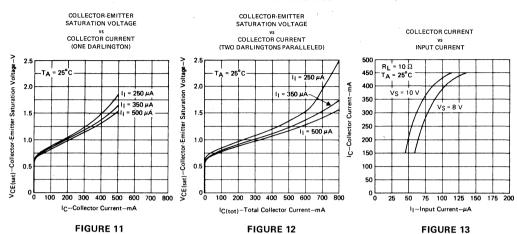
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_0 = 50 \Omega$.

B. C_L includes probe and jig capacitance.

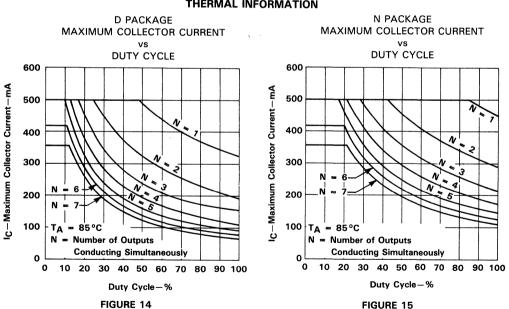
C. For testing the ULN2001A, ULN2003A, and the ULN2005A, $V_{IH}=3$ V; for the ULN2002A, $V_{IH}=13$ V; for the ULN2004A, $V_{IH}=8$ V.

FIGURE 10. LATCH-UP TEST

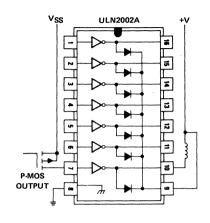
TYPICAL CHARACTERISTICS



THERMAL INFORMATION



APPLICATION INFORMATION

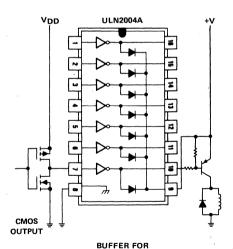


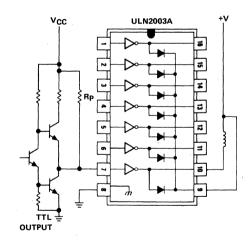
Vcc ULN2005A LAMP TEST OUTPUT

ULN2003A

P-MOS TO LOAD

TTL TO LOAD





HIGHER CURRENT LOADS

USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

ULN2064, ULN2065, ULN2066, ULN2067 OUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

D2528, DECEMBER 1979-REVISED SEPTEMBER 1986

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- ULN2064 and ULN2065 Have TTL Compatible Inputs
- ULN2066 and ULN2067 Have CMOS- and PMOS-Compatible Inputs
- Designed for Interchangeability With Sprague ULN2064 thru ULN2067, Respectively

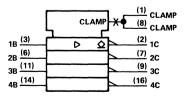
description

The ULN2064, ULN2065, ULN2066, and ULN2067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The ULN2064 and ULN2065 are intended for use with TTL and 5-V MOS logic. The ULN2066 and ULN2067 are intended for use with PMOS and higher-voltage CMOS logic.

The ULN2064, ULN2065, ULN2066, and ULN2067 are characterized for operation from -20 °C to 85 °C.

logic symbol†

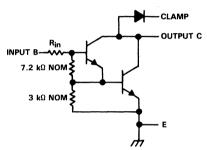


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NE PACKAGE (TOP VIEW) CLAMP 1 U16 14C 15 11C 1C∏2 1B∏3 14 🗌 4B HEAT SINK, E, ∫ 14 13 HEAT SINK, E, AND SUBSTRATE 1 5 12 AND SUBSTRATE Дзв 2В∏6 11 2C∏7 10 NC CLAMP 8 9∏3C

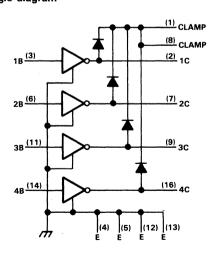
NC-No internal connection

schematic (each darlington pair)



ULN2064, ULN2065: $R_{in} = 350 Ω$ NOM ULN2066, ULN2067: $R_{in} = 3 kΩ$ NOM

logic diagram





Copyright © 1986, Texas Instruments Incorporated

ULN2064, ULN2065, ULN2066, ULN2067 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

absolute maximum ratings at 25 °C free-air temperature for each switch (unless otherwise noted)

| | ULN2064 | ULN2065 | ULN2066 | ULN2067 | UNIT |
|---|------------|------------|------------|------------|------|
| Collector-emitter voltage | 50 | 80 | 50 | 80 | V |
| Input voltage (see Note 1) | 15 | 15 | . 30 | 30 | ٧ |
| Peak collector current (see Figures 12, 13, and 14) | 1.5 | 1.5 | 1.5 | 1.5 | Α |
| Input current | 25 | 25 | 25 | 25 | mA |
| Total power dissipation at (or below) 25 °C free-air temperature (see Note 2) | 2075 | 2075 | 2075 | 2075 | mW |
| Operating free-air temperature range | - 20 to 85 | -20 to 85 | -20 to 85 | -20 to 85 | °C |
| Storage temperature range | -55 to 150 | -55 to 150 | -55 to 150 | -55 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260 | 260 | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.

2. For operation above 25 °C free-air temperature, derate total power linearly to 1079 mW at 85 °C at the rate of 16.6 mW/°C.

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| | PARAMETER | TEST | TEST CONDITIONS | 1 | 2064 | ULN2 | | ULN | | 1 | 2067 | UNIT |
|----------------------|------------------------------------|--------|---|----------|------|----------|-------------|-----|------|-----|------|--------------|
| | ANAMETER | FIGURE | 1201 00101110110 | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | VIII. |
| V _{CEX(sus} | Collector sustaining voltage | 1 | V _I = 0.4 V, I _C = 100 mA | 35 | | 50 | | 35 | | 50 | | v |
| | | | V _{CE} = 50 V | | 100 | | | | 100 | | | |
| CEX | Collector output | 2 | $V_{CE} = 50 \text{ V}, T_{A} \approx 70 ^{\circ}\text{C}$ | | 500 | | | | 500 | | | μΑ |
| CEX | cutoff current | | V _{CE} = 80 V | | | | 100 | | | | 100 | μ |
| | | | $V_{CE} = 80 \text{ V}, T_{A} = 70 ^{\circ}\text{C}$ | 1 | | <u> </u> | 500 | | | | 500 | |
| | | } | V _I = 2.4 V | 1.4 | 4.3 | 1.4 | 4.3 | | | ļ | | |
| (I(on) | On-state | 3 | $V_1 = 3.75 \text{ V}$ | 3.3 | 9.6 | 3.3 | 9.6 | | | | | mΑ |
| 1(011) | input current | | V ₁ = 5 V | 1 | | | | 0.6 | 1.8 | 0.6 | 1.8 | |
| | | | V ₁ = 12 V | <u> </u> | | <u> </u> | | 1.7 | 5.2 | 1.7 | 5.2 | |
| | On-state | | V _{CE} = 2 V, I _C = 1 A | | 2 | <u> </u> | 2 | | 6.5 | | 6.5 | |
| V _{I(on)} | input voltage | 4 | V _{CE} = 2 V, I _C = 1.5 A, See Note 3 | | 2.5 | | 2.5 | | 10 | | 10 | ٧ |
| | | | $I_1 = 625 \mu\text{A}, I_C = 500 \text{m/s}$ | | 1.1 | | 1.1 | | 1.1 | | 1.1 | |
| | | 1 | $I_1 = 935 \mu\text{A}, I_C = 750 \text{m/s}$ | \ | 1.2 | | 1.2 | | 1.2 | | 1.2 | |
| | Collector-emitter | | $I_1 = 1.25 \text{ mA}, I_C = 1 \text{ A}$ | | 1.3 | | 1.3 | | 1.3 | | 1.3 | |
| V _{CE(sat)} | saturation voltage | 5 | $I_I = 2 \text{ mA}, \qquad I_C = 1.25 \text{ A}$ See Note 3 | | 1.4 | | | | 1.4 | | | V |
| | | | $I_1 = 2.25 \text{ mA}, I_C = 1.5 \text{ A},$ See Note 3 | | | | 1.5 | | | | 1.5 | |
| | | | V _R = 50 V | 1 | 50 | | | | 50 | | | |
| 1- | Clamp-diode | | $V_R = 50 \text{ V}, T_A = 70 ^{\circ}\text{C}$ | 1 | 100 | | *********** | | 100 | | | 1, |
| ¹ R | reverse current | 6 | V _R = 80 V | T | | | 50 | | | | 50 | μΑ |
| | | | $V_R = 80 \text{ V}, T_A = 70 ^{\circ}\text{C}$ | | | | 100 | | | | 100 |] |
| VF | Clamp-diode | 7 | I _F = 1 A | | 1.75 | | 1.75 | | 1.75 | | 1.75 | V |
| ٧F | forward voltage | 1 | I _F = 1.5 A, See Note 3 | 1 | 2 | 1 | 2 | | 2 | | 2 |] |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, VCC = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|-----------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | See Figure 8 | | | 1 | μS |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 6 | | | 1.5 | μS |

PARAMETER MEASUREMENT INFORMATION

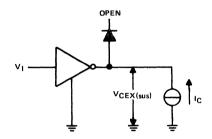


FIGURE 1. VCEX(sus)

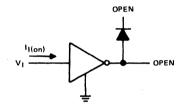
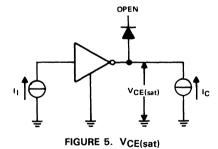


FIGURE 3. II(on)



OPEN VCE

FIGURE 2. ICEX

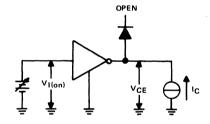


FIGURE 4. VI(on)

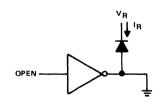


FIGURE 6. IR

PARAMETER MEASUREMENT INFORMATION

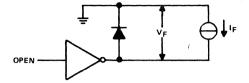
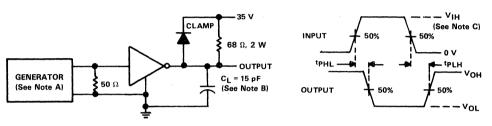


FIGURE 7. VF



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_0 = 50\,\Omega$.

B. C_L includes all probe and stray capacitance.

C. $V_{IH} = 2.5 \text{ V}$ for ULN2064 and ULN2065. $V_{IH} = 10 \text{ V}$ for ULN2065 and ULN2067.

FIGURE 8. SWITCHING TIMES

ELECTRICAL CHARACTERISTICS

COLLECTOR CURRENT vs



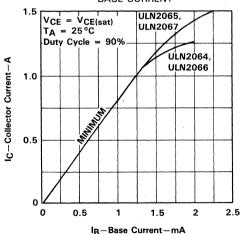


FIGURE 9

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT

VS **DUTY CYCLE** 2.0 = 25°C = Number of Outputs IC-Maximum Collector Current-A Conducting Simultaneously 1.5 1.0 0.5 30 40 50 60 70 80 90 100 10 20

MAXIMUM COLLECTOR CURRENT

DUTY CYCLE 2.0 $T_A = 50$ °C = Number of Outputs IC-Maximum Collector Current-A Conducting Simultaneously 1.5 1.0 0.5 10 20 30 40 50 60 70 80 90 100 Duty Cycle-%

FIGURE 10

Duty Cycle-%

FIGURE 11

MAXIMUM COLLECTOR CURRENT

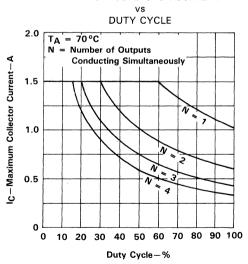


FIGURE 12

ULN2064, ULN2065, ULN2066, ULN2067 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

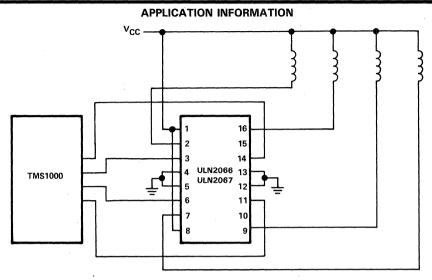


FIGURE 13. RELAY DRIVER INTERFACE

ULN2068, ULN2069 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

D2579, MAY 1980-REVISED SEPTEMBER 1986

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible With TTL and 5-V CMOS
- Designed for Interchangeability With Sprague ULN2068 and ULN2069

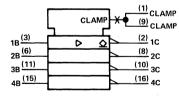
description

The ULN2068 and ULN2069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-V CMOS signal levels. The second and third stages form uncommitted-collector outputs with commoncathode clamp diodes for switching inductive loads.

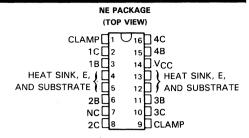
The ULN2068 and ULN2069 can sink up to 1.5 A per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge).

The ULN2068 and ULN2069 are characterized for operation from $-20\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$.

logic symbol1

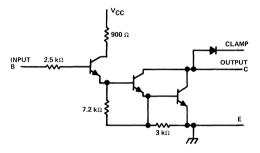


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



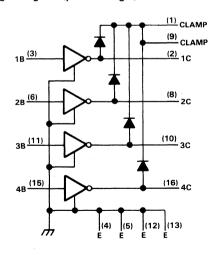
NC-No internal connection

schematic (each switch)



Resistor values shown are nominal.

logic diagram (positive logic)





ULN2068, ULN2069 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

absolute maximum ratings at 25 °C free-air temperature for each switch (unless otherwise noted)

| | ULN2068 | ULN2069 , | UNIT |
|---|------------|------------|------|
| Collector-emitter voltage | 50 | 80 | ٧ |
| Supply voltage, V _{CC} (see Note 1) | 10 | 10 | V |
| Input voltage | 15 | 15 | V |
| Peak collector current (see Figures 10, 11, and 12) | 1.5 | 1.5 | Α |
| Total power dissipation at (or below) 25 °C free-air temperature (see Note 2) | 2075 | 2075 | mW |
| Operating free-air temperature range | -20 to 85 | -20 to 85 | °C |
| Storage temperature range | -55 to 150 | -55 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.

2. For operation above 25 °C free-air temperature, derate total power linearly to 1079 mW at 85 °C at the rate of 16.6 mW/°C.

electrical characteristics at 25 °C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

| | 0.0.0.1.5555 | TEST | TEGT COMPLETIONS | ULN | 2068 | ULN: | 2069 | UNIT |
|-----------------------|---|--------|--|----------|------|----------|------|------|
| | PARAMETER | FIGURE | TEST CONDITIONS | MIN | MAX | MIN | MAX | UNIT |
| V _{CEX(sus)} | Collector sustaining voltage | 1 | $V_{I} = 0.4 \text{ V}, I_{C} = 100 \text{ mA}$ | 35 | | 50 | | ٧ |
| | | | V _{CE} = 50 V | | 100 | | | |
| loev | Collector output cutoff current | 2 | V _{CE} = 50 V, T _A = 70°C | | 500 | | | μΑ |
| ICEX | Conector output cutori current | | V _{CE} = 80 V | | | | 100 | μ |
| | | | V _{CE} = 80 V, T _A = 70°C | | | | 500 | |
| 1 | On-state input current | 3 | V _I = 2.4 V | | 250 | | 250 | μА |
| l(on) | On-state input current | 3 | V _j = 3.75 V | | 1000 | | 1000 | μΑ |
| V., . | On-state input voltage | 4 | V _{CE} = 2 V, I _C = 1.5 A, | 1 | 2.4 | | 2.4 | ν |
| V _{I(on)} | On-state input voltage | | See Note 3 | | 2.4 | | 2.4 | |
| | | | $V_1 = 2.4 \text{ V}, I_C = 500 \text{ mA}$ | | 1.1 | | 1.1 | |
| | Collector-emitter | | $V_{I} = 2.4 \text{ V}, I_{C} = 750 \text{ mA}$ | | 1.2 | | 1.2 | |
| | | | $V_1 = 2.4 \text{ V}, I_C = 1 \text{ A}$ | | 1.3 | | 1.3 | |
| V _{CE(sat)} | saturation voltage | 5 | $V_1 = 2.4 \text{ V}, I_C = 1.25 \text{ A},$ | | 1.4 | | | V |
| | saturation voitage | | See Note 3 | <u> </u> | 1.4 | <u> </u> | | |
| | | | $V_1 = 2.4 \text{ V}, I_C = 1.5 \text{ A},$ | | | | 1.5 | l |
| | | | See Note 3 | İ | | | 1.5 | |
| | | | V _R = 50 V | ľ | 50 | | | |
| 1- | Clamp-diode reverse current | 6 | $V_{R} = 50 \text{ V}, T_{A} = 70 ^{\circ}\text{C}$ | | 100 | | | μΑ |
| ^I R | Clamp-diode reverse current | " | V _R = 80 V | | | | 50 | μ^ |
| | | | $V_{R} = 80 \text{ V}, T_{A} = 70 ^{\circ}\text{C}$ | | | | 100 | } |
| VF | Clamp-diode forward voltage | 7 | lp = 1 A | | 1.75 | | 1.75 | V |
| νF | Clamp-diode forward voltage | | IF = 1.5 V, See Note 3 | | 2 | | 2 | L |
| lcc | Supply current (only one switch conducting) | 8 | V _I = 2.4 V, I _C = 500 mA | | 6 | | 6 | mA |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, $t_W = 10$ ms, duty cycle $\leq 10\%$.

switching characteristics at 25 $^{\circ}$ C free-air temperature, V_{CC} = 5 V

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|--|-----------------|-----|-----|-----|------|
| ^t PLH | Propagation delay time, low-to-high-level output | See Figure 9 | | | 1 | μS |
| tPHL | Propagation delay time, high-to-low-level output | See i iguie 9 | | | 1.5 | μS |

PARAMETER MEASUREMENT INFORMATION

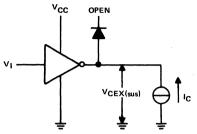


FIGURE 1. VCEX(sus)



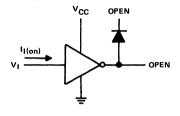
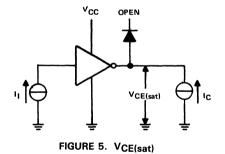


FIGURE 3. II(on)



OPEN V_F V_F

FIGURE 7. VF

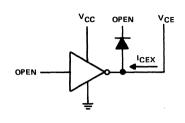


FIGURE 2. ICEX

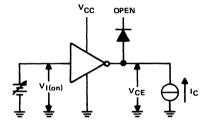


FIGURE 4. VI(on)

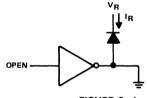


FIGURE 6. IR

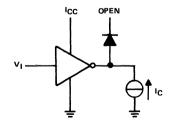
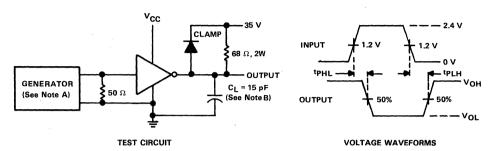


FIGURE 8. ICC



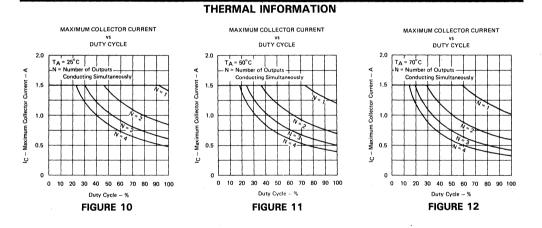
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_0 = 50 Ω .

B. C_1 includes all probe and stray capacitance.

FIGURE 9. SWITCHING TIMES



APPLICATION INFORMATION

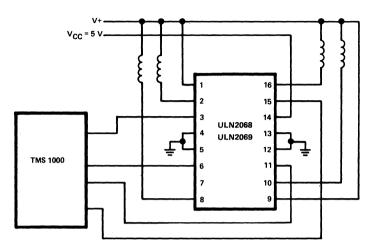


FIGURE 13. RELAY DRIVER INTERFACE

ULN2074, ULN2075 OUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

D2580, MAY 1980-REVISED SEPTEMBER 1986

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible with TTL or 5-V CMOS
- Designed for Interchangeability with Sprague ULN2074 and ULN2075

description

The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 A for each Darlington pair.

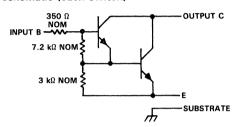
The ULN2074 and ULN2075 are unique generalpurpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

For proper operation, the substrate must be connected to the most negative voltage.

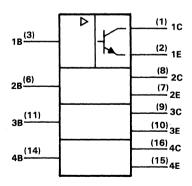
The ULN2074 and ULN2075 are characterized for operation from -20°C to 85°C.

NE PACKAGE (TOP VIEW) 1E [7 4E 15 1B [] 4B 14 **HEATSINK** HEATSINK AND AND 12日子 SUBSTRATE SUBSTRATE 28 ∏6 11 🗌 3B 2E [10 7 3E 7 зс 2C ∏8 9[

schematic (each switch)



logic symbol†



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



ULN2074, ULN2075 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

absolute maximum ratings at 25 °C free-air temperature for each switch (unless otherwise noted)

| | ULN2074 | ULN2075 | UNIT |
|---|------------|------------|------|
| Collector-emitter voltage | 50 | 80 | V |
| Input voltage with respect to substrate | 30 | 60 | V |
| Peak collector current (see Figures 9, 10, and 11) | 1.5 | 1.5 | Α |
| Input current | 25 | 25 | mA |
| Total power dissipation at (or below) 25 °C free-air temperature (see Note 1) | 2075 | 2075 | mW |
| Operating free-air temperature range | -20 to 85 | - 20 to 85 | °C |
| Storage temperature range | -55 to 150 | -55 to 150 | °C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260 | 260 | °C |

NOTE 1: For operation above 25 °C free-air temperature, derate total power linearly to 1079 mW at 85 °C at the rate of 16.6 mW/°C.

electrical characteristics at 25 °C free-air temperature (unless otherwise noted)

| i | PARAMETER | TEST | TEST COL | IDITIONS | ULN | 2074 | ULN | 2075 | LINUT |
|-----------------------|---------------------------------|--------|---------------------------|--------------------------|----------|------|-----|------|-------|
| | PARAMETER | FIGURE | TEST CON | IDITIONS | MIN | MAX | MIN | MAX | UNIT |
| V _{CEX(sus)} | Collector sustaining voltage | 1 | $V_1 = 0.4 V$, | I _C = 100 mA | 35 | | 50 | | ٧ |
| | | | V _{CE} = 50 V | | | 100 | | | |
| lory | Collector output cutoff current | 2 | $V_{CE} = 50 \text{ V},$ | $T_A = 70$ °C | | 500 | | | μΑ |
| CEX | Collector output cutori current | 2 | V _{CE} ≈ 80 V | | | | | 100 | μΑ |
| İ | | | V _{CE} ≈ 80 V, | $T_A = 70$ °C | | | | 500 | |
| lu , | On-state input current | 3 | $V_1 = 2.4 \text{ V}$ | | 2 | 4.3 | 2 | 4.3 | mA |
| l(on) | On-state input current | 3 | $V_1 = 3.75 \text{ V}$ | 1 | 4.5 | 9.6 | 4.5 | 9.6 | IIIA |
| , | | 1 | $V_{CE} = 2 V$, | I _C = 1 A | | 2 | | 2 | |
| V _{I(on)} | On-state input voltage | 4 | $V_{CE} = 2 V$, | $I_{C} = 1.5 A,$ | ł | 2.5 | ł | 2.5 | V |
| | | | See Note 2 | | | 2.5 | L | 2.5 | |
| | | | $I_1 = 625 \mu A$, | $I_C = 500 \text{ mA}$ | <u> </u> | 1.1 | ļ | 1.1 | |
| • | | 1 | $I_1 = 935 \mu A$, | $I_C = 750 \text{ mA}$ | | 1.2 | | 1.2 | |
| | Collector-emitter | | $I_1 = 1.25 \text{ mA},$ | I _C = 1 A | T | 1.3 | | 1.3 | |
| V _{CE(sat)} | | 5 | l ₁ = 2 mA, | I _C = 1.25 A, | | 1.4 | | | V |
| , | saturation voltage | | See Note 2 | | | 1.4 | | | |
| | | | l _j = 2.25 mA, | I _C = 1.5 A, | | | | 1.5 | |
| | | | See Note 2 | | | | | 1.5 | |

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, $t_W = 10$ ms, duty cycle $\leq 10\%$.

switching characteristics at 25 °C free-air temperature, $V_{CC} = 5$ V

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------|--|-----------------|-----|-----|-----|------|
| tPLH | Propagation delay time, low-to-high-level output | See Figure 6 | | | 1 | μs |
| tPHL | Propagation delay time, high-to-low-level output | See Figure 0 | | | 1.5 | μS |

PARAMETER MEASUREMENT INFORMATION

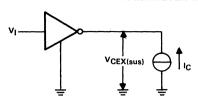


FIGURE 1. VCEX(sus)

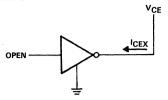


FIGURE 2. ICEX

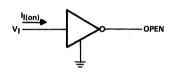


FIGURE 3. II(on)

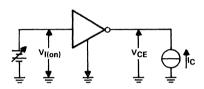


FIGURE 4. VI(on)

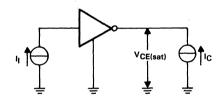
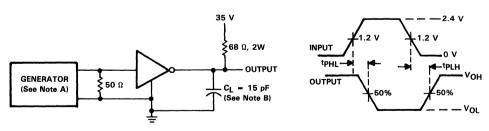


FIGURE 5. VCE(sat)



TEST CIRCUITS

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_0 = 50 \Omega$.

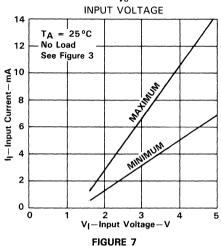
B. C_L includes all probe and stray capacitance.

FIGURE 6. SWITCHING CHARACTERISTICS



ELECTRICAL CHARACTERISTICS

INPUT CURRENT vs
INPUT VOLTAGE



COLLECTOR CURRENT

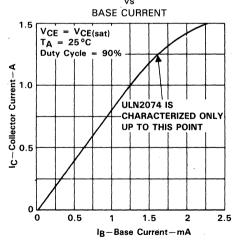
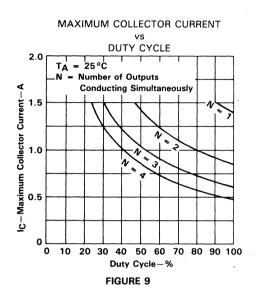
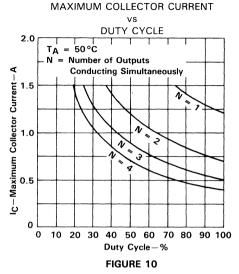


FIGURE 8

THERMAL INFORMATION





MAXIMUM COLLECTOR CURRENT

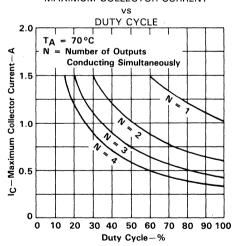


FIGURE 11

APPLICATION INFORMATION

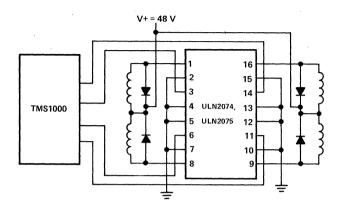


FIGURE 12. RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES

| General Information | 1 |
|--|-----------------------------------|
| | |
| Data Transmission and Control Circuits | 2 |
| | |
| Display Drivers | 3 |
| | Manufacture and American American |
| Peripheral Drivers/Power Actuators | 4 |
| | overalisma |
| Mechanical Data | 5 |

Explanation of Logic Symbols

Contents

| | Page |
|-----------------------|------|
| Ordering Instructions | 5-3 |
| Mechanical Data | 5-5 |

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

| EXAMPLE: SN 75189 N -00 |
|--|
| Prefix — / / |
| MUST CONTAIN TWO, THREE, OR FOUR LETTERS |
| SN TI Special Functions or Interface Products TCM TI Telecommunication Products TL TI Linear Products TPIC TI Intelligent Power Products |
| STANDARD SECOND-SOURCE PREFIXES |
| AM, DP, or DS National MC Motorola LT Linear Technology N8T Signetics MAX Maxim Integrated Products uA Fairchild/National |
| Unique Circuit Description |
| MUST CONTAIN THREE TO EIGHT CHARACTERS (From Individual Data Sheets) |
| Examples: 232 75160B 3695 75C1154 75115 75ALS180 |
| Package ———————————————————————————————————— |
| MUST CONTAIN ONE OR TWO LETTERS |
| D, DB, DW, FD, FK, FN, FT, HA, HB, J, JD, JG, KN, KV, N, NE, NT, P, W (From Pin-Connection Diagrams on Individual Data Sheet) |
| Instructions (Dash No.) |
| MUST CONTAIN TWO NUMBERS |
| -00 No special instructions -10 Solder-dipped leads (N, NE, and NT packages only) |

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

Dual-In-Line (D, DB, DW, J, JD, JG, N, NE, NT, P)

Slide Magazines

- A-Channel Plastic Tubing - Sectioned Cardboard Box

Individual Cardboard Box

Chip Carrier (FD, FK, FN, FT)

- Anti-Static Plastic Tubing

Flat (HA, HB, W)

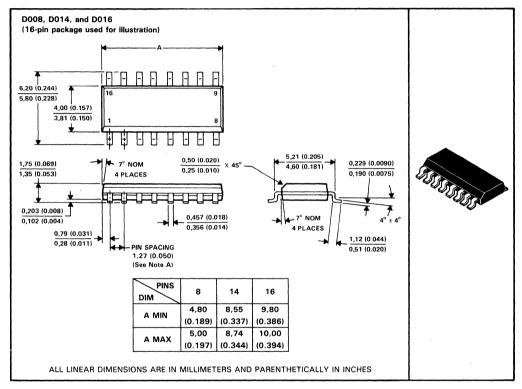
Power Tab (KN, KV) - Sleeves

- Wells Carrier



D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

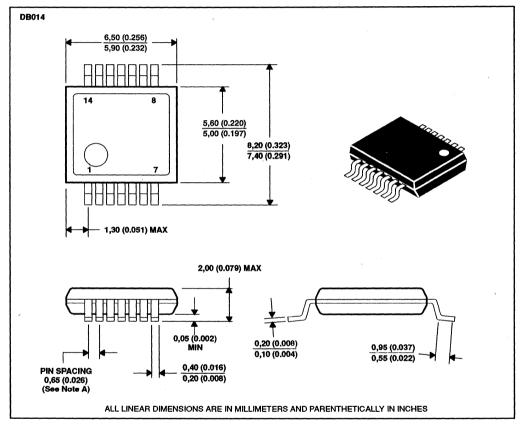


- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
 - B. Body dimensions do not include mold flash or protrusion.
 - C. Mold flash or protrusion shall not exceed 0,15 (0.006).
 - D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.



DB014 "shrunk small outline" package

This "shrunk small outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

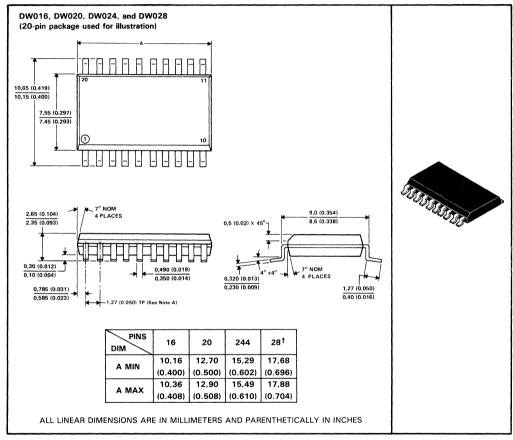


NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0.15 (0.006).
- D. Lead tips to be planar within ± 0.051 (0.002) exclusive of solder.

DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



[†]The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

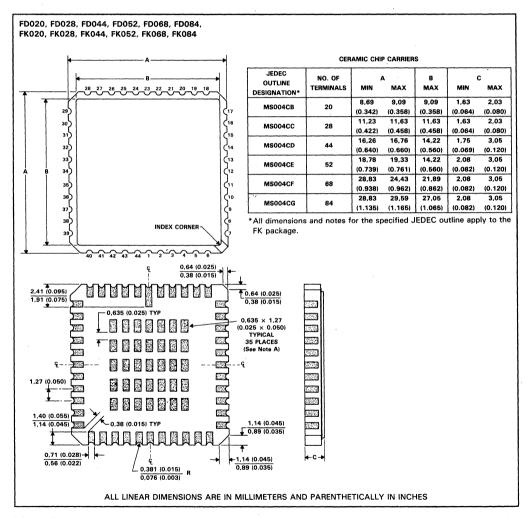
- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0,15 (0.006).
- D. Lead tips to be planar within $\pm 0,051$ (0.002) exclusive of solder.



FD020, FD028, FD044, FD052, FD068, FD084, and FK020, FK028, FK044, FK052, FK068, FK084 leadless ceramic chip carrier packages

Each of these hermetically sealed chip charrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder leads on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC standards, 1, 2, and 11.

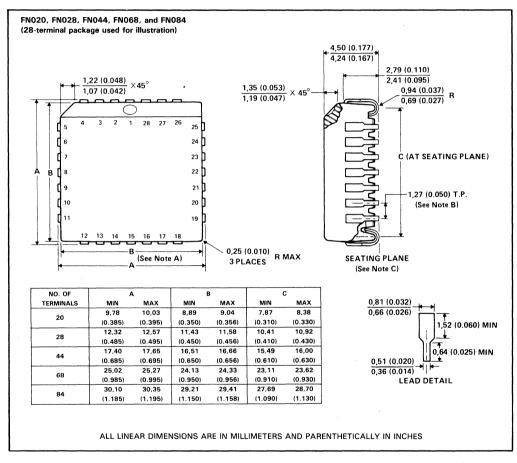


NOTE A: The checkerboard pattern is aligned vertically with the contact pads and is symmetrical horizontally as shown; it is applicable to some 44-terminal packages only.



FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.

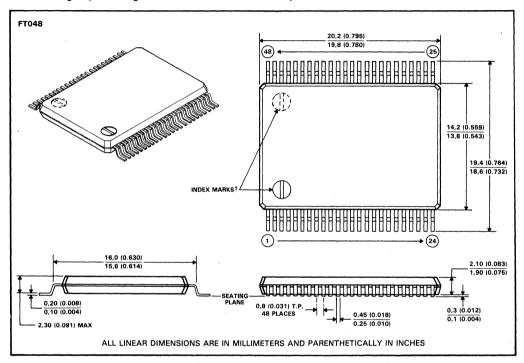
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

C. The lead contact points are planar within 0,10 (0.004).



FT048

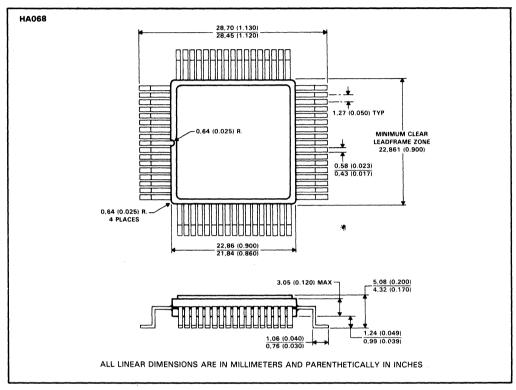
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



[†]There are two versions of the 48-lead FT package that differ in the position of the index mark in the top view. In one version, the mark is near lead 3, in the other version, it is near lead 46. Consult the individual data sheet to see which applies for a particular device type.

HA068 quadriform flat package

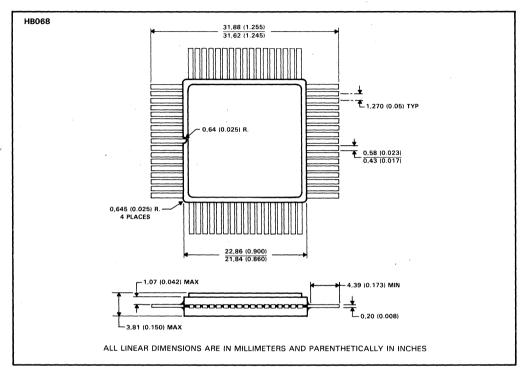
The 68-pin HA package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with gull-wing bent leads for surface mounting capability.





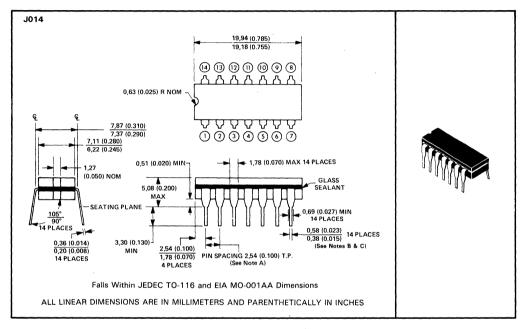
HB068 quadriform flat package

The 68-pin HB package is housed in a quadriform flat package. It is hermetically sealed with 0.05-inch-lead spacing configured with straight leads for surface mounting capability.



J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

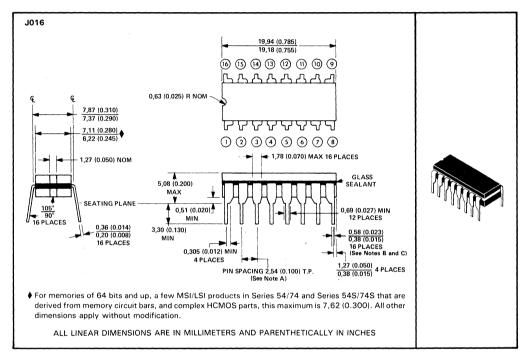


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

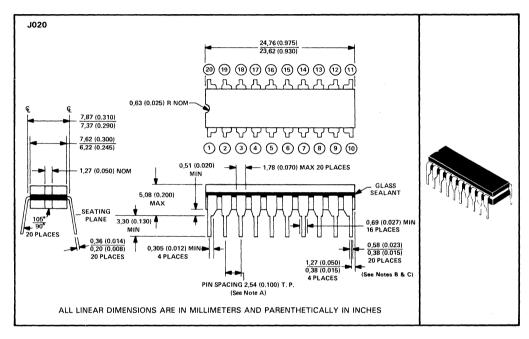


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J020 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

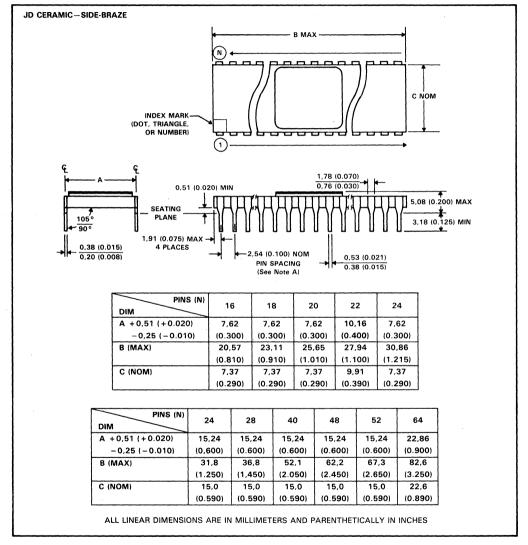


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

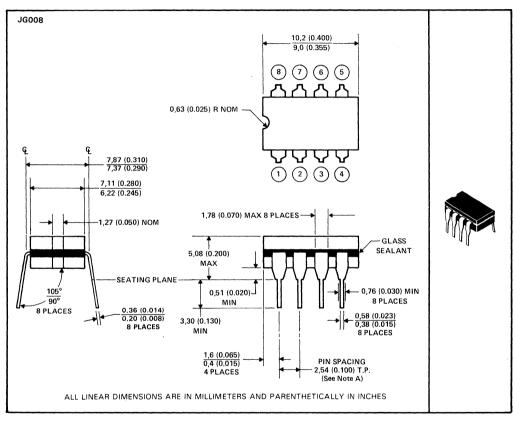


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



JG008 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-pin lead frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

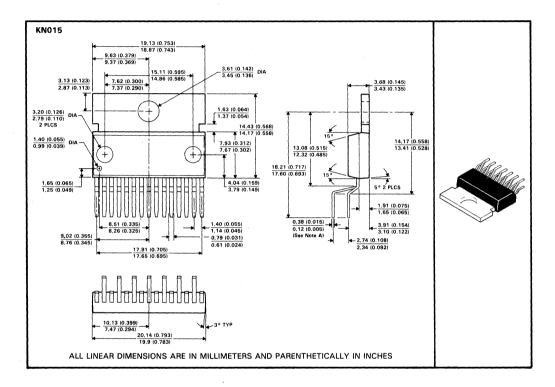


NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.



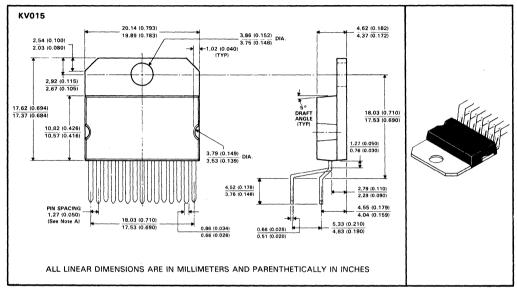
KN015 plastic flange-mount package

This package comprises a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



KV015 plastic package

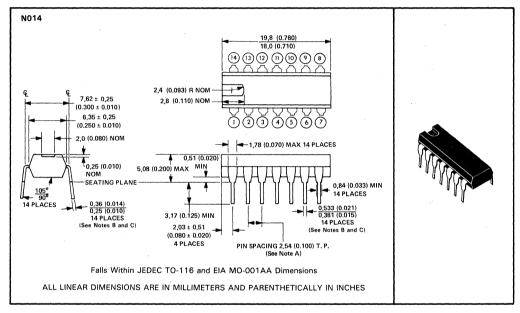
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



NOTE A: Leads are within 0,36 (0.014) radius of true position (T.P.) at maximum material conditions.

NO14 plastic dual-in-line package

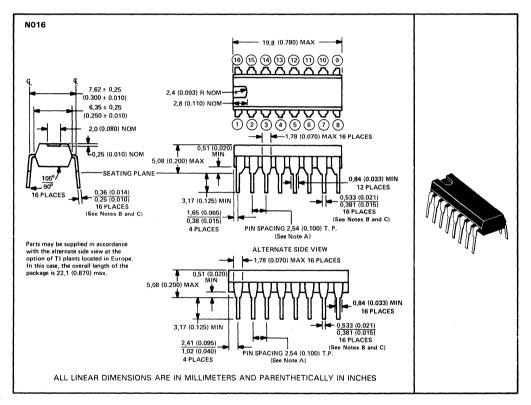
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 - B. This dimension does not apply for solder-dipped leads.
 - C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NO16 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



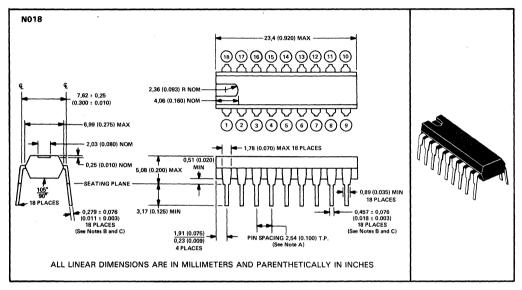
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.



NO18 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

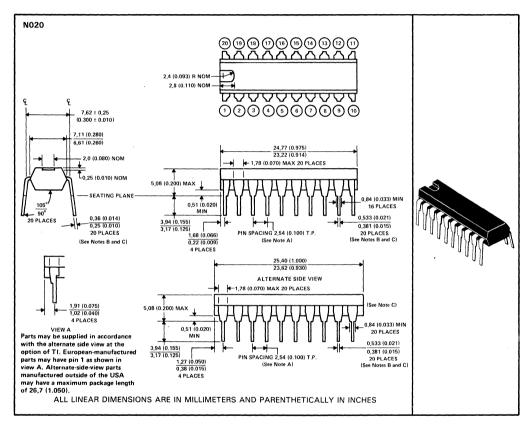


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

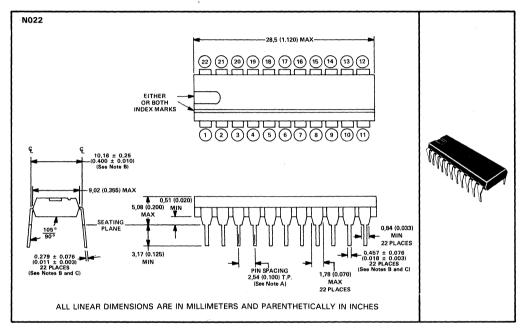


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N022 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

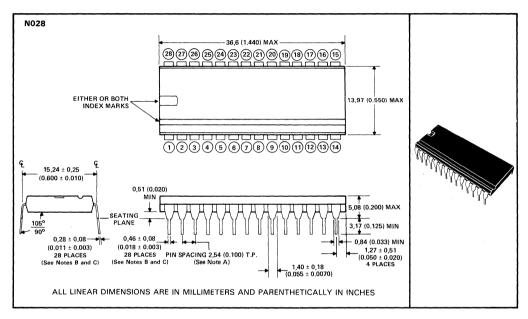


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028 plastic dual-in-line package

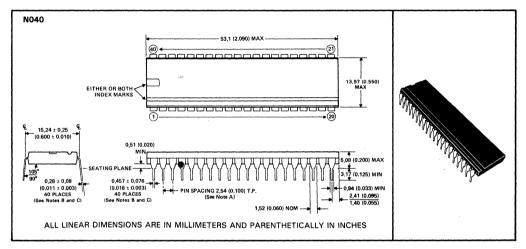
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 - B. This dimension does not apply for solder-dipped leads.
 - C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NO40 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



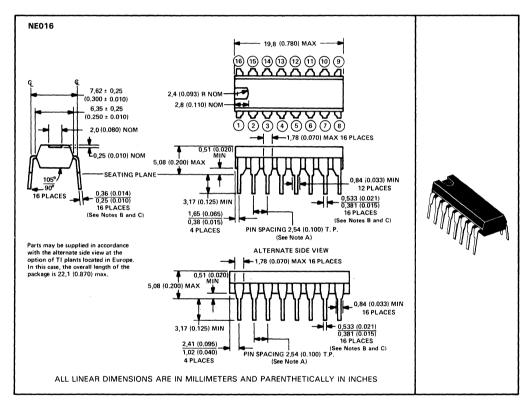
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

B. This dimension does not apply for solder-dipped leads.

C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NE016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a 16-pin lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. For better heat dissipation there are internal tabs connecting the two central leads on each side of the 16-pin package. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



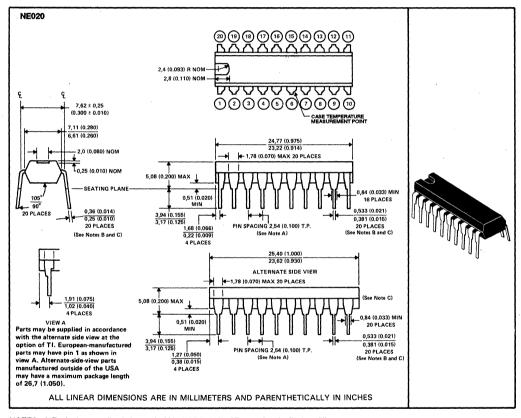
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.



NE020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. For better heat dissipation there are internal tabs connecting the two central leads on each side of the 20-pin package. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



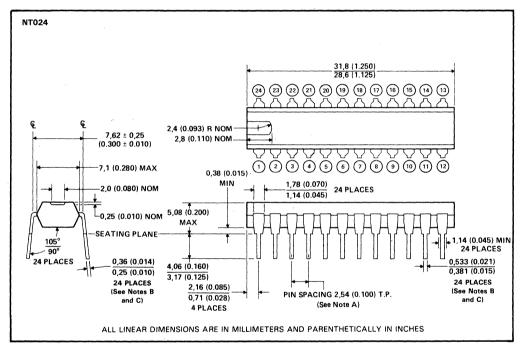
NOTES: A.Each pin centerline is located within 0,25 (0.010) of ilts true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



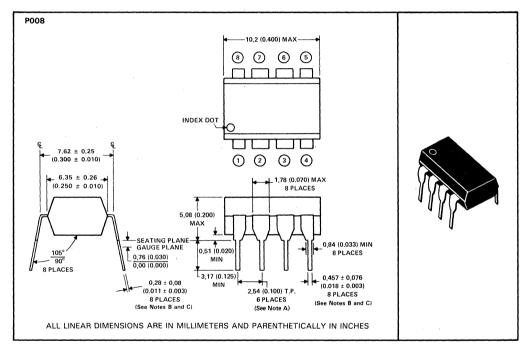
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.



P008 dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

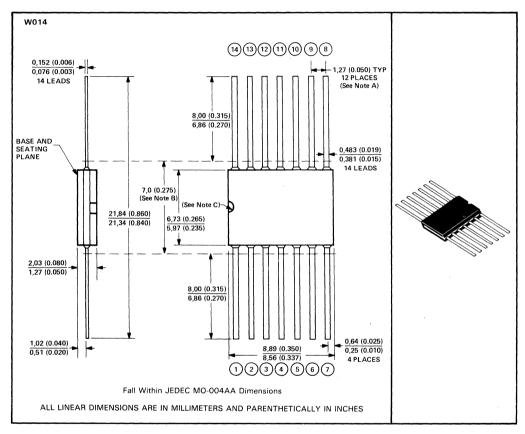


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

W014 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.

- B. This dimension determines a zone within which all body and lead irregularities lie.
- C. Index point is provided on cap for terminal identification only.

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Explanation of Logic Symbols

by F.A. Mann

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C (Control) Dependency

If you have questions on this Explanation of Logic Symbols, please contact:

Cumbala for Internal Connections

F.A. Mann, MS 3684 Texas Instruments Incorporated P.O. Box 655303 Dallas, Texas 75265 Telephone (214) 997-2489 IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc. IEEE Standards Office 345 East 47th Street New York, N.Y. 10017

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International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc. 1430 Broadway New York, N.Y. 10018

Table

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1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

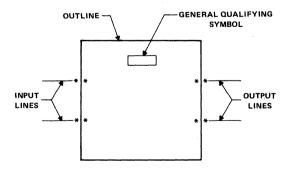
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that consolidates the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply ANSI/IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this data book and is somewhat briefer than the explanation that appears in several of TI's data books on digital logic. However, it includes a new section (6.0) that explains several symbols for actual devices in detail. This has proven to be a powerful learning aid.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 9.



^{*}Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by ANSI/IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

X/Y is the general qualifying symbol for identifying coders, code converters, and level converters. X and Y may be used in their own right to stand for some code or either or both may be replaced by some other indication of the code or level such as BCD or TTL. As might be expected, interface circuits make frequent use of this set of qualifying symbols.

Table 1. General Qualifying Symbols

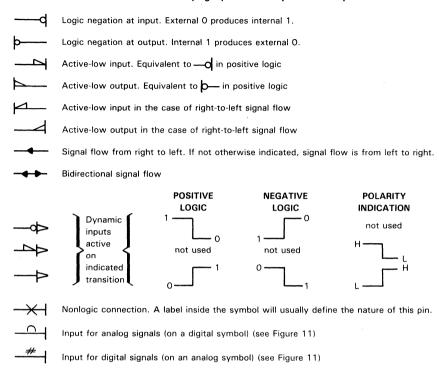
| SYMBOL | DESCRIPTION | | |
|----------------------|---|---|--|
| & | AND gate or function | | |
| ≥1 | OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output. | | |
| = 1 | Exclusive OR. One and only one input must be active to activate the output. | | |
| 1 | A simple 1-input gate or element | | |
| ▷ or ◁ | A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow). | | |
| ┲ | Schmitt trigger; element with hysteresis | | |
| X/Y | Coder, code converter, level converter | | |
| | The following are examples of subsets of this general class of qualifying symbol used in this book. | | |
| | BCD/7-SEG | BCD to 7-segment display driver | |
| | TTL/MOS | TTL to MOS level converter | |
| | CMOS/PLASMA DISP | Plasma-display driver with CMOS-compatible inputs | |
| | MOS/LED | Light-emitting-diode driver with MOS-compatible inputs | |
| | CMOS/VAC FLUOR DISP | Vacuum-fluorescent display driver with CMOS-compatible inputs | |
| | CMOS/EL DISP | Electroluminescent display driver with CMOS-compatible inputs | |
| | TTL/GAS DISCH DISPLAY | Gas-discharge display driver with TTL-compatible inputs | |
| SRGm | Shift register. m = number of bits | | |

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2 and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangle polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 2. Qualifying Symbols for Inputs and Outputs



3.3 Symbols Inside the Outline

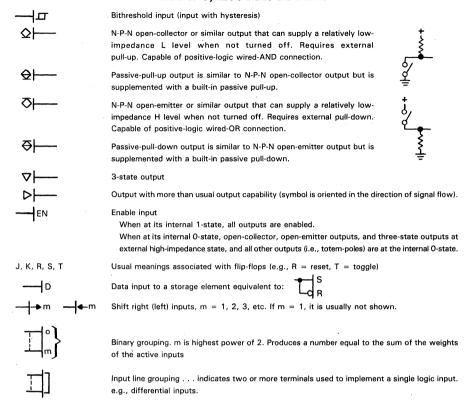
Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the element and has no effect on inputs. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 6.11. Binary-weighted inputs are arranged in order and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. This number is the sum of the weights (1, 2, 4...2n) of those input standing at their 1 states. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Table 3. Symbols Inside the Outline



3.4 Combinations of Outlines and Internal Connections

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

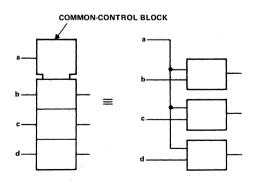


Figure 2. Common-Control Block

The outlines of elements may be embedded within one another or abutted to form complex elements, in which case the following rules apply. There is no logic connection between elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection when the line common to two outlines is perpendicular to the direction of signal flow. If no indications are shown on either side of the common line, it is assumed that there is only one logic connection. If more than one internal connection exists between adjacent elements, the number of connections will be clarified by the use of one or more of the internal connection symbols from Table 4 and/or appropriate qualifying symbols or dependency notation.

Table 4. Symbols for Internal Connections

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Dynamic internal connection. Transition from 1 to 0 on left produces transitory 1 state on right.

Table 4 shows symbols that are used to represent internal connection with specific characteristics. The first is a simple noninverting connection, the second is inverting, the third is dynamic. As with this symbol and an external input line, the transition from 0 to 1 on the left produces a momentary 1-state on the right. The fourth symbol is similar except that the active transition on the left is from 1 to 0.

Only logic states, not levels, exist inside symbols. The negation symbol () is used internally even when direct polarity indication () is used externally.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN75163B symbol (see 6.5) illustrates this principle.

4 Dependency Notation

Some readers will find it more to their liking to skip this section and proceed to the explanation of the symbols for a few actual devices in 6.0. Reference will be made there to various parts of this section as it is needed. If this procedure is followed, it is recommended that 5.0 be read after 6.0 and then all of 4.0 be reread.

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined but only the eight used in this book are explained. They are listed below in the order in which they are presented and are summarized in Table 5 following 4.10.2.

| Section | Dependency Type or Other Subject | | |
|---------|---------------------------------------|--|--|
| 4.2 | G, AND | | |
| 4.3 | General Rules for Dependency Notation | | |
| 4.4 | V, OR | | |
| 4.5 | N, Negate (Exclusive-OR) | | |
| 4.6 | Z, Interconnection | | |
| 4.7 | X, Transmission | | |
| 4.8 | C, Control | | |
| 4.9 | EN, Enable | | |
| 4.10 | M. Mode | | |

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 3 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

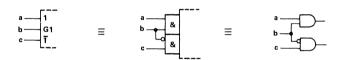


Figure 3. G Dependency Between Inputs

In Figure 4, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 5 shows input **a** to be ANDed with a dynamic input **b**.

Figure 4. G Dependency Between Outputs and Inputs

Figure 5. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

When a Gm input or output (m is a number) stands at its internal 1 state, all inputs and outputs affected by Gm stand at their normally defined internal logic states. When the Gm input or output stands at its 0 state, all inputs and outputs affected by Gm stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

- Labeling the input (or output) affecting other inputs or outputs with the letter symbol indicating
 the relationship involved (e.g., G for AND) followed by an identifying number, appropriately
 chosen, and
- 2. Labeling each input or output affected by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 3).

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other (Figure 6).

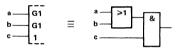


Figure 6. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 12).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 12).

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 7).

When a Vm input or output stands at its internal 1 state, all inputs and outputs affected by Vm stand at their internal 1 states. When the Vm input or output stands at its internal 0 state, all inputs and outputs affected by Vm stand at their normally defined internal logic states.

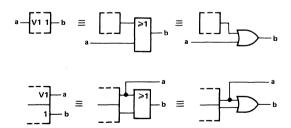


Figure 7. V (OR) Dependency

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 8). Each input or output affected by an Nm input or output stands in an Exclusive-OR relationship with the Nm input or output.

When an Nm input or output stands at its internal 1 state, the internal logic state of each input and each output affected by Nm is the complement of what it would otherwise be. When an Nm input or output stands at its internal 0 state, all inputs and outputs affected by Nm stand at their normally defined internal logic states.

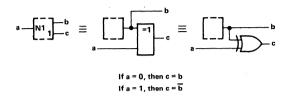


Figure 8. N (Negate) (Exclusive-OR) Dependency

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Zm input or output will be the same as the internal logic state of the Zm input or output, unless modified by additional dependency notation (Figure 9).

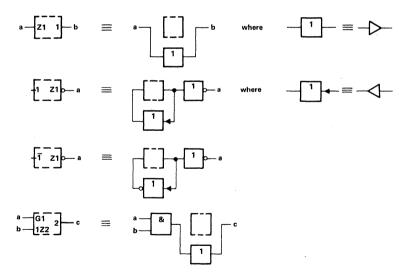


Figure 9. Z (Interconnection) Dependency

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 10).

When an Xm input or output stands at its internal 1 state, all input-output ports affected by this Xm input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an Xm input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

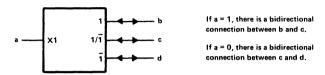


Figure 10. X (Transmission) Dependency

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 10 and 11 would be omitted.

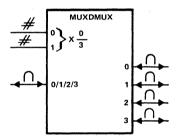


Figure 11. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the second example of Figure 12.

When a Cm input or output stands at its internal 1 state, the inputs affected by Cm have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a Cm input or output stands at its internal 0 state, the inputs affected by Cm are disabled and have no effect on the function of the element.

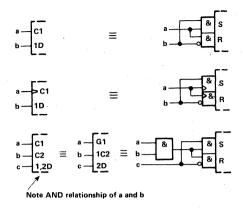


Figure 12. C (Control) Dependency

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An ENm input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number m. It also affects those inputs labeled with the identifying number m. By contrast, an EN input affects all outputs and no inputs. The effect of an ENm input on an affected input is identical to that of a Cm input (Figure 13).

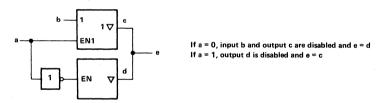


Figure 13. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.

When an ENm input stands at its internal 0 state, the inputs affected by ENm are disabled and have no effect on the function of the element, and the outputs affected by ENm are also disabled. Open-collector outputs are turned off, three-state outputs stand at their high-impedance state, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

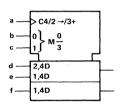
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting Mm inputs will appear in the label of that affected input or output between parentheses and separated by solidi, e.g., $(1/2)CT = 0 \equiv 1CT = 0/2CT = 0$ where 1 and 2 refer to M1 and M2.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an Mm input or Mm output stands at its internal 1 state, the inputs affected by this Mm input or Mm output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an Mm input or Mm output stands at its internal 0 state, the inputs affected by this Mm input or Mm output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., $C4/2 \rightarrow /3 +)$, any set in which the identifying number of the Mm input or Mm output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 14 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 14. M (Mode) Dependency Affecting Inputs

4.10.2 M Dependency Affecting Outputs

When an Mm input or Mm output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an Mm input or Mm output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that Mm input or Mm output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this Mm input or Mm output appears are to be ignored.

Figure 15 shows a symbol for a device whose output can behave like either a 3-state output or an open-collector output depending on the signal applied to input a. Mode 1 exists when input a stands at its internal 1 state and, in that case, the three-state symbol applies and the open-element symbol has no effect. When $\mathbf{a}=0$, mode 1 does not exist so the three-state symbol has no effect and the open-element symbol applies.

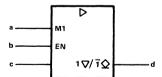


Figure 15. Type of Output Determined by Mode

Table 5. Summary of Dependency Notation

| TYPE OF | LETTER | AFFECTING INPUT | AFFECTING INPUT |
|-----------------|---------|---------------------------------|---|
| DEPENDENCY | SYMBOL* | AT ITS 1-STATE | AT ITS 0-STATE |
| Control | С | Permits action | Prevents action |
| | EN | Permits action | Prevents action of inputs |
| Enable | | | outputs turned off |
| Enable | | | outputs at external high impedance |
| | | | Other outputs at internal 0 state |
| AND | G | Permits action | Imposes 0 state |
| Mode | M | Permits action (mode selected) | Prevents action (mode not selected) |
| Negate (Ex-NOR) | N | Complements state | No effect |
| OR | V | Imposes 1 state | Permits action |
| Transmission | × | Bidirectional connection exists | Bidirectional connection does not exist |
| Interconnection | Z | Imposes 1 state | Imposes 0 state |

^{*}These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output)
AFFECTED by that input is labeled with that same number.

5 Bistable Elements

The dynamic input symbol and dependency notation provide the tools to identify different types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 16).

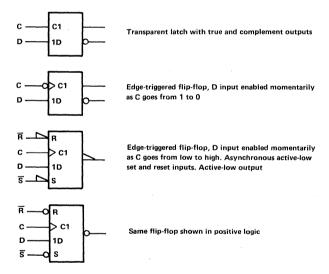


Figure 16. Latches and Flip-Flops

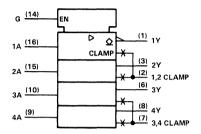
Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C.

Notice that synchronous inputs can be readily recognized by their dependency labels (a number preceding the functional label, 1D in these examples) compared to the asynchronous inputs (S and R), which are not dependent on the C inputs. Of course if the set and reset inputs were dependent on the C inputs, their labels would be similarly modified (e.g., 1S, 1R).

6 Examples of Actual Device Symbols

The symbols explained in this section include some of the most complex in this book. These were chosen, not to discourage the reader, but to illustrate the amount of information that can be conveyed. It is likely that if one reads these explanations and follows them reasonably well, most of the other symbols will seem simple indeed. The explanations are intended to be independent of each other so they may seem somewhat repetitious. However each illustrates new principles. They are arranged more or less in the order of complexity.

6.1 SN75437A Quadruple Peripheral Driver

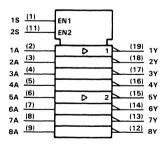


There are four identical sections. The symbology is complete for the first element; the absence of any symbology for the other elements indicates they are identical. The top two elements share a common output clamp, pin 2. This is shown to be a nonlogic connection by the superimposed X on the line. The function for this type of connection is indicated briefly and not necessarily exactly by a small amount of text within the symbol. The bottom two elements likewise share a common clamp.

Each element is shown to be an inverter with amplification (indicated by \triangleright). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case. The output is shown by \bigcirc to be open collector.

All the outputs share a common EN input, pin 14. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 14 is low), the outputs, being open-collector types, are turned off and would be pulled high by an external pullup resistor.

6.2 SN75128 8-Channel Line Receiver

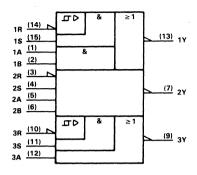


There are eight identical sections. The symbology is complete for the first element; the absence of any symbology for the next three elements indicates they are identical. Likewise the symbology is complete for the fifth element; the absence of any symbology for the next three elements indicates they are identical to the fifth.

Each element is shown to be an inverter with amplification (indicated by \triangleright). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The former applies in this case. Since neither the symbol for open-collector (\bigcirc) or 3-state (\bigcirc) outputs is shown, the outputs are of the totem-pole type.

The top four outputs are shown to be affected by affecting input number 1, which is EN1, meaning they will be enabled if EN1 = 1 (pin 1 is high). See 4.9 for an explanation of EN dependency. If pin 1 is low, EN1 = 0 and the affected outputs will go to their inactive (high) levels. Similarly, the lower four outputs are controlled by pin 11.

6.3 SN75122 Triple Line Receivers

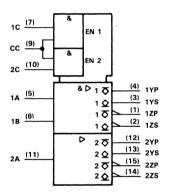


There are two identical sections. The symbology is complete for the first section; the absence of any symbology for the next section indicates it is identical. Likewise the symbology is complete for the third section, which is similar, but not identical, to the first and second.

The top section may be considered to be an OR element (\geq 1) with two embedded ANDs (&), one of which has an active-low amplified input (\triangleright) with hysteresis (\perp 7), pin 14. This is ANDed with pin 15 and the result is ORed with the AND of pins 1 and 2. The output of the OR, pin 13, is active-low.

The third section is identical to the first except that pin 12 has no input ANDed with it. Since neither the symbol for open-collector (Ω) or 3-state (∇) outputs is shown, the outputs are of the totem-pole type.

6.4 SN75113 Differential Line Drivers with Split 3-State Outputs



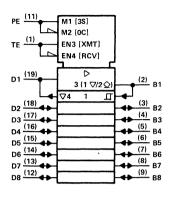
There are two similar elements in the array. The first is a 2-input AND element (indicated by &); the second has only a single input. Both elements are shown to have special amplification (indicated by \triangleright). Taking TTL as a reference, this means that either the input is sensitive to lower level signals, or the output has greater drive capability than usual. The latter applies in this case.

Each element has four outputs. Pins 4 and 3 are a pair consisting of one open-emitter output (♥) and one open-collector output (♠). Relative to the AND function, both are active high. Pins 1 and 2 are a similar pair but relative to the AND function, both are active low. All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated symbol or label inside the element. Here there is no such contrary indication. All four outputs are shown to be affected by affecting input number 1, which is EN1,

meaning they will all be enabled if EN1 = 1. See 4.9 for an explanation of EN dependency. If EN1 = 0, all the affected outputs will be turned off. EN1 is the output of an AND gate (indicated by &) whose active-high inputs are pins 7 and 9. Both pins 7 and 9 must be high to enable the outputs of the top element. Assuming they are enabled and that pins 5 and 6 are both high, the internal state of all four outputs will be a 1. Pins 4 and 3 will both be high, pins 1 and 2 will both be low. The part is designed so that pins 3 and 4 may be connected together creating an active-high 3-state output. Likewise pins 1 and 2 may be connected together to create an active-low 3-state output.

All that has been said about the first element regarding its outputs and their enable inputs also applies to the second element. Pins 9 and 10 are the enable inputs in this case.

6.5 SN75163B Octal General-Purpose Interface Bus Transceiver



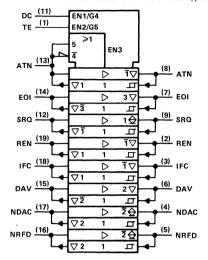
There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. There are eight identical channels. The symbology is complete for the first channel; the absence of any symbology for the other channels indicates they are identical. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by \triangleright), and the inputs on the right all have hysteresis (indicated by \square).

The outputs on the left are shown to be 3-state outputs by the ∇ . They are also shown to be affected by affecting input number 4, which is EN4, meaning they will be enabled if EN4 = 1 (pin 1 is low). See 4.9 for an explanation of EN dependency. If EN4 = 0 (pin 1 is high), the affected outputs will go to their high-impedance (off) states.

The labeling at pin 2, which applies to all the outputs on the right, is unusual because the outputs themselves have an unusual feature. The label includes both the symbol for a 3-state output (∇) and for an open-collector output (Ω), separated by a slash indicating that these are alternatives.

The symbol for the 3-state output is shown to be affected by affecting input number 1, which is M1, meaning the ∇ label is valid when M1 = 1 (pin 11 is high), but is to be ignored when M1 = 0 (pin 11 is low). See 4.10 for an explanation of M (mode) dependency. Likewise the symbol for the open-collector output is shown to be affected by affecting input number 2, which is M2, meaning the Ω label is valid when M2 = 1 (pin 11 is low), but is to be ignored when M2 = 0 (pin 11 is high). These labels are enclosed in parentheses (used as in algebra); the numeral 3 indicates that in either case the output is affected by EN3. Thus the right-hand outputs will be off if pin 1 is low. It can now be seen that pin 1 is the direction control and pin 11 is used to determine whether the outputs are of the 3-state or open-collector variety.

6.6 SN75161B Octal IEEE Std 488 Interface Bus Transceiver



There are eight I/O ports on each side, pins 2 through 9 and 12 through 19. Pin 13 is not only an I/O port; the line running into the common-control block (see Figure 2) indicates that it also has control functions. Pins 1 and 11 are also controls. The eight bidirectional channels each have amplification from left to right, that is, the outputs on the right have increased drive capability (indicated by ▷), and the inputs on the right all have hysteresis (indicated by □). All of the outputs are shown to be of the 3-state type by the ∇ symbol except for the outputs at pins 9, 4, and 5, which are shown to have passive pullups by the ⇔ symbol.

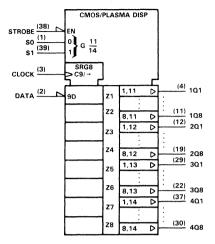
Starting with a typical I/O port, pin 18, the output portion is identified by an arrow indicating right-to-left signal flow and the three-state output symbol (∇). This output is shown to be affected by affecting input number 1, which is EN1, meaning it will be enabled as an output if EN1 = 1 (pin 11 is high). See 4.9 for an explanation of EN dependency. If pin 11 is low, EN1 = 0 and the output at pin 18

will be in its high-impedance (off) state. This also applies to the 3-state outputs at pins 13 and 19 and to the passive-pullup output at pin 9. On the other hand, the outputs at pins 8, 2, 3, and 12 all are affected by the complement of EN1. This is indicated by the bar over the 1 at each of those outputs. They are enabled only when pin 11 is low. Thus one function of pin 11 is to serve as direction control for the first, third, fourth, and fifth channels.

Similarly it can be seen that pin 1 serves as direction control for the sixth, seventh, and eighth channels. If pin 1 is high, transmission will be from left to right in the sixth channel, right to left in the seventh and eighth. These transmissions are reversed if pin 1 is low.

The direction control for the second channel, EN3, is more complex. EN3 is the output of an OR (\geq 1) function. One of the inputs to this OR is the active-high signal on pin 13. This signal is shown to be affected at the input to the OR gate by affecting input number 5, which is G5, meaning that pin 13 is ANDed with pin 1 before entering the OR gate. See 4.2 for an explanation of G (AND) dependency. The other input to the QR is the active-low signal on pin 13. This signal is ANDed with the complement of pin 11 before entering the OR gate. This is indicated by the G4 at pin 1 and the 4 with a bar over it at pin 13. Thus for EN3 to stand at the 1 state, which would enable transmission from pin 14 to pin 7, both pins 13 and 1 must be high or both pins 13 and .11 must be low.

6.7 SN75500E AC Plasma Display Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is an 8-bit shift register. It has a single D input, pin 2, which is shown to be affected by affecting input number 9, which is C9, meaning it will be enabled if C9=1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C9=1, which in this case will occur on the transition of pin 3 from low to high, the state of the D input will be stored. Pin 2 is shown to be active low so to store a 1, pin 2 must be low.

In addition to controlling the D input, pin 3 is shown by $/\rightarrow$ to have an additional function. As pin 3 goes from low to high, data stored in the shift register is shifted one position. The right-pointing arrow means that the data is shifted away from the control block (down).

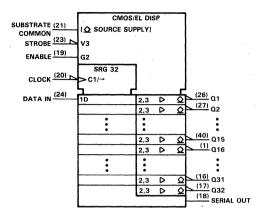
On the right side of the symbol an abbreviation technique has been used that is practical only when

the internal labels and the pin numbers are both consecutive. Thus it should be clear that the input of the element whose output is pin 5 is affected by affecting input number 2, just as the input of the element whose output is pin 4 is affected by affecting input number 1. Affecting inputs 1 through 8 are Z inputs (Z1 through Z8), which means their signals are transferred directly to the output elements. See 4.6 for an explanation of Z dependency.

The inputs of the 32 implicitly shown output elements are also shown to be affected by affecting inputs numbers 11, 12, 13, and 14 in four blocks of eight each. These inputs will be found in the common control block preceded by a letter G and a brace. The brace is called the binary grouping symbol. It is equivalent to a decoder with outputs in this case driving four G inputs (G11, G12, G13, and G14). The weights of the inputs to the coder are shown to be 2^0 and 2^1 for pins 1 and 39, respectively. The decoder has four outputs corresponding to the four possible sums of the weights of the activated decoder inputs. If pins 1 and 39 are both low, the sum of the weights = 0 and G11 = 1. If pin 1 is low while pin 39 is high, the sum = 2 and G13 = 1 and so forth. G indicates AND dependency, see 4.2. Only one of the four affecting G inputs at a time can take on the 1 state. The block of eight output elements affected by that G input are enabled; the 0 state is imposed on the other 24 output elements and externally those output pins are low.

Because of their high-current, high-voltage characteristics, the outputs are labeled with the amplification symbol \triangleright . All the outputs share a common EN input, pin 38. See Figure 2 for an explanation of the common control block. When EN = 0 (pin 38 is high), the outputs take on their internal 0 states. Being active high, that means they are forced low.

6.8 SN75551 Electroluminescent Row Driver with CMOS-Compatible Inputs



The heart of this device and its symbol is a 32-bit shift register. It has a single D input, pin 24, which is shown to be affected by affecting input number 1, which is C1, meaning it will be enabled if C1 = 1. See 4.8 for an explanation of C dependency and 5.0 for a discussion of bistable elements. Since the C input is dynamic, the storage elements are edge-triggered flip-flops. While C1 = 1, which in this case will occur on the transition of pin 20 from high to low, the state of the D input will be stored. Pin 24 is shown to be active high so to store a 1, pin 24 must be high.

In addition to controlling the D input, pin 20 is shown by /→ to have an additional function. As pin 20 goes from high to low, data stored in the shift register is shifted one position. The

right-pointing arrow means that the data is shifted away from the control block (down). The internal inputs of the output buffers are all shown to be affected by affecting inputs 2 and 3. Affecting input 2 is G2, meaning that pin 19 is ANDed with each of the internal register outputs, which are the buffer inputs. If pin 19 is high, the affected buffer inputs are enabled. If pin 19 is low, the 0 state is imposed on the affected buffer inputs. See 4.2 for an explanation of G (AND) dependency. Affecting input 3 is V3, meaning that pin 23 (active low) is ORed with each of the internal register outputs. If pin 23 is high, V3 = 0 and the affected buffer inputs are enabled. If pin 23 is low, V3 = 1 and the 1 state is imposed on the affected buffer inputs. See 4.4 for an explanation of V (OR) dependency. The effect of V3 is taken into account after that of G2 because of the order in which the labels appear. This means that the imposition of the 1 state on the internal buffer inputs by pin 23 would take precedence over the imposition of the 0 state by pin 19 in case both inputs were active. Pin 18 is shown to be an output directly from the thirty-second stage of the shift register. Pins 19 and 23 do not affect this output.

An abbreviation technique has been used for the shift register elements and associated the output lines. This technique is practical only when the pin numbers and pin names are both consecutive.

The symbol Ω designates an n-p-n open-collector or similar output. In this device, the outputs are actually open-drain n-channel field-effect transistors. Instead of being grounded, the sources of these transistors are all connected to pin 21. This pin is used as an input to control the output voltage.

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