TEXAS INSTRUMENTS

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Linear Circuits

Voltage Regulators/Supervisors, Comparators, Special Functions, and Building Blocks

Data Book
Volume 3

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Volume 3

Linear Circuits
Voltage Regulators/Supervisors, Comparators, Special Functions, and Building Blocks

1992

1992

Linear Products

Linear Products Quick Reference Guide

Data Book	Contents	Document No.
• Optoelectronics and Image Sensors	Optocouplers CCD Image Sensors and Support Phototransistors IR-Emitting Diodes Hybrid Displays	SOYD002A, 1990
• Speech System Manuals	TSP50C4X Family TSP50C10/11 Synthesizer TSP53C30 Synthesizer	SPSS010, 1990 SPSS011, 1990 SPSV006, 1991
• Interface Circuits	Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers	SLYD006, 1991
• Telecommunications Circuits	Transmission, Switching, Subscriber, Transient Suppressors	SCTD001B, 1991
• Linear and Interface Circuits Applications	Op Amps/Comparators, Video Amps, VRegs, Power Supply Design, Timers, Display Drivers, Datran, Peripheral Drivers, Data Acq., Special Functions	SLYA005, 1991
• Mass Storage ICs Designer's Reference Guide	Disk Drivers: Read/Write, Servo/System Control, Interface/Linear, Digital ASIC, LinASIC™, Applications	SSCA001, 1992
• Macromodel Data Manual	Level I: Operational Amplifiers, Voltage Comparators, Building Blocks Level II: Selected Operational Amplifiers, Buildilng Blocks	SLOS047B, 1992

January 1992

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Linear Circuits Data Book 1992

Volume 3
Voltage Regulators/Supervisors, Comparators, Special Functions, and Building Blocks

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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed to provide highly reliable power supply regulators, supervisors, comparators, special functions, and building blocks. These circcuits represent processes from standard bipolar through BIDFET, BIFET, IMPACT™, LinCMOS™, Advanced LinCMOS™, and Schottky technologies.

This data book (Volume 3 of 3) provides information on the following types of products:

- Supervisory Circuits
- Switch-Capacitance Voltage Converters
- Shunt Voltage Regulators and Voltage References
- Adjustable Series-Pass Voltage Regulators
- Switching Power Supply and Pulse-Width-Modulated (PWM) Controllers and Regulators
- Fixed Output Series-Pass Voltage Regulators (Positive and Negative)
- Voltage Comparators, Timers, Disk Drive Circuits
- Current Mirrors, Sonar Circuits, Sound Generators
- Video Amplifiers

These products provide critical functions in analog and digital systems that:

- Utilize a wide range of voltages
- Require a constant output voltage regardless of changes in input voltage, output current, and ambient temperature
- Demand high input-output isolation where analog circuitry must be connected independently of digital ground
- Need low voltage (i.e., battery) regulation

New surface-mount packages (3 to 20 leads) include the thin, small-outline packages (PW) and SOT-89 (PK) plastic packages that optimize board density with minimum impact of power dissipation capabilities. Test equipment with handlers and automated assembly bonders strengthen the production capabilities that provide a lower cost-to-performance ratio. TI continues to enhance quality and reliability of integrated circuits by improvements in materials, processes, test methods, and test equipment. In addition, specifications and programs are continuously updated. Qualilty and performance are monitored throughout all phases of manufacturing.

The alphanumeric listing in this data book includes all devices contained in Volumes 1, 2, and 3. Products in this book are shown in **BOLD** type. Thus, the reader can easily find the particular volume for a given device. Also included are those new products added to this volume as indicated by a dagger(†). The selection guide includes a functional description of each device by providing key parametric information and packaging options. Ordering information and mechanical data are in the last section of the book.

Complete technical data for all TI semiconductor products are available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
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P.O. BOx 809066
Dallas, Texas 75380-9066

We sincerely feel that this new 1992 Linear Circuits Data Book, Volume 3, will be a significant addition to your technical literature from Texas Instruments.

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uA79M12M 2–465
uA79M15C 2–465
uA79M20C 2–465
uA79M24C 2–465
†UC2842 2–475
†UC2843 2–475
†UC2844 2–475
†UC2845 2–475
†UC3842 2–475
†UC3843 2–475
†UC3844 2–475
†UC3845 2–475

†New devices added to this volume.

power supply supervisors

(values specified for T_A = 25°C)

FUNCTION	SENSE INPUT SUPPLY		SENSE INPUT THRESHOLD	THRESHOLD TOLERANCE	OUTPUT	TYPE	PACKAGE	PAGE NO.
	S1	S2	(V TYP)	(%)				
Overvoltage Monitor	†	–	2.6	5	Open Emitter	MC3423	D, JG, P	2–147
Undervoltage Monitor	† 5 V 9 V 12 V 15 V	– – – – –	2.53 4.55 7.6 10.8 13.5	1	Open Collector	TL7702A TL7705A TL7709A TL7712A TL7715A	D, P	2–343
Undervoltage Monitor	† 5 V	–	7.53 4.55	1	Open Collector	TL7702B TL7705B	D, P	2–351
Undervoltage Monitor	5 V	–	4.55	2.6	Open Collector	TL7757 TL7759C	D, LP, PK, Y‡ D, P	2–359 2–373
Dual Undervoltage/ Overvoltage	5 V 12 V 15 V	† † †	4.55 10.9 13.64	1	Open Collector	TL7770-5 TL7770-12 TL7770-15	DW, N	2–377

† Programmable
‡ Y package is in chip form

switched-capacitor voltage converters

(values specified for T_A = 25°C)

CONTROL TOPOLOGY	OUTPUT SWITCH	SUPPLY VOLTAGE RANGE (V)	QUIESCENT CURRENT (NO LOAD)	MAXIMUM CONTINUOUS I/O	MAXIMUM FREQUENCY (kHz)	TYPICAL CONVERSION EFFICIENCY (%)	TYPE	PACKAGE	PAGE NO.
Voltage Mode	Single	3.5 – 15	150 μA	300 mA	35	90	LT1054	DW, JG, P	2–55

shunt voltage regulators/references

(values specified for T_A = 25°C)

REGULAR VOLTAGE RANGE (V)	MINIMUM SHUNT CURRENT TO MAINTAIN REG	MAXIMUM SHUNT CURRENT	TOLERANCE (%)	TEMPERATURE COEFFICIENT (TYP)	DEVICE	PACKAGE	PAGE NO.
1.2 Typ	10 μA	20 mA	1	20 PPM/°C	LM185-1.2 LM285-1.2 LM385B-1.2	D, LP	2–3
			2		LM385-1.2		
2.5 Typ			1		LT1004-2.5		2–35
	20 μA		1.5		LM185-2.5 LM285-2.5 LM385B-2.5		2–9
			3		LM385-2.5		
	400 μA Typ	10 mA	2		LM236 LM336		2–17
			1		LM236A LM336B		
	400 μA		0.2	15 PPM/°C	LT1009		2–47
2.5 to 30	500 μA Typ	150 mA	4	120 PPM/°C	TL430	LP	2–185
2.5 to 36	400 μA Typ		2	25 PPM/°C	TL431	D, JG, LP, P, PK	2–189
			1		TL431A		
2.5 to 36	450 μA Typ		0.4	25 PPM/°C	TL1431	D, LP, PK, Y‡	2–303

‡ Y package is in chip form

adjustable series-pass voltage regulators (values specified over operating temperature range)

OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT VOLTAGE RANGE (V)	TOLERANCE (%)	MAXIMUM ($V_I - V_O$) DIFFERENCE	DEVICE	PACKAGE	PAGE NO.
Positive Output	100 mA	1.2 to 32	5	35 V	TL317	D, JG, LP	2–173
	750 mA	1.25 to 125	5	125 V	TL783	KC	2–291
Positive Output	5 A	1.25 to 35	2	30 V	LT1084		2–133
Negative Output	1.5 A	−1.2 to −37	4	−40 V	LM337		2–21
Positive or Negative Output	150 mA	2 to 37	5	38 V	uA723	D, J, N, U	2–417

virtual grounds (values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)	OUTPUT IMPEDANCE (Ω)	TOLERANCE (%)	TEMPERATURE COEFFICIENT (TYP)	DEVICE	PACKAGE	PAGE NO.
2.5	±20	0.0075	0.8	20 PPM/°C	TLE2425	D, LP, Y†	2–385
1.5 V_I		0.025			TLE2426		2–399

† Y package is in chip form

switching power supply controllers and regulators

(values specified for T_A = 25°C)

CONTROL TOPOLOGY	SINGLE ENDED	FIXED PUSH-PULL	SINGLE SWITCH OUTPUTS	TOTEM-POLE OUTPUTS	OUTPUT CURRENT PER SWITCH (mA)	MAXIMUM FREQUENCY (kHz)	VOLTAGE REFERENCE TOLERANCE (%)	PULSE-BY-PULSE CURRENT LIMITING	OUTPUT STEERING CONTROL	PROGRAMMABLE OUTPUTS	DEAD-TIME CONTROL	UNDERVOLTAGE LOCKOUT	SOFT START	ON-BOARD AMPLIFIERS	CURRENT-SENSE AMPLIFIERS	50% MAXIMUM DUTY CYCLE	TYPE	PKGS	PAGE NO.
Voltage-Mode Pulse-Width Modulated Controllers	X	–	X	–	250	200	5	–	–	–	X	–	–	2	–	–	MC34060	D, N	2–149
	–	–	X			300				X	X						TL494	D, FK, J, N	2–207
		X	–							–	–			1	1		SG2524 SG3524	D, N	2–161
		–	X				1										TL594		2–241
		X	–	X	±250					X	X	X		2	–		TL598	D, FK, J, N	2–251
	X	–	Dual	–	21	500	4			–	X	X		–	X		TL1451A	D, N	2–319
Current-Mode Pulse-Width Modulated Controllers	X	–	–	X	±1000	500	1	X	–	–	–	X	–	1	X	–	UC2842 UC2843 UC3842 UC3843	D, P	2–475
																X	UC2844 UC2845 UC3844 UC3845		2–475
	X	–	X	–	5000	40	2	X	–	–	–	–	–	1	X	–	LT1070	KC, KV	2–77
					2500												LT1071		2–101
					1250												LT1072	KC, KV, P	2–117
Fixed On-Time Voltage Mode	X	–	X	–	1200	40	10	–	–	–	–	–	–	1	–	–	TL496	D, P	2–223
							5	–	–	–	–	–	–	1	–	–	TL499A	D, P	2–35
					700	50	5	–	–	–	–	–	–	1	–	–	TL497A	D, J, N	2–227

X Applicable data
– Nonapplicable data

positive fixed output series-pass voltage regulators

(values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
2	1.5 A	3	2.5	TL782	KC	2–87
2.6	100 mA	5	2	uA78L02A	D, LP	2–437
		10		uA78L02		
5	100 mA	5		uA78L05A	D, JG, LP	
		10		uA78L05		
	150 mA	10	0.6	LM2930-5	KC, LP	2–25
		5		TL750L05	D, KC, LP, P	2–267
				TL751L05	D, P	2–267
	500 mA		2	uA78M05	JG, KC	2–447
	750 mA	1	0.6	TL750M05	KC	2–273
				TL751M05		
	1.5 A	2	2	TL780-5		2–281
		5		uA7805		2–427
6	500 mA			uA78M06		2–447
6.2	100 mA			uA78L06A	D, LP	2–437
		10		uA78L06		
	1.5 A	5		uA7806	KC	2–427
8	100 mA			uA78L08A	D, LP	2–437
		10		uA78L08		
	150 mA		0.6	LM2930-8	KC, LP	2–25
		5		TL750L08	D, KC, LP, P	2–267
				TL751L08	D, P	2–267
	500 mA		2	uA78M08	KC	2–447
	750 mA	1	0.6	TL750M08		2–273
				TL751M08		
8.5	1.5 A	5	2	uA7808		2–427
				uA7885		
9	100 mA			uA78L09A	D, LP	2–437
		10		uA78L09		
	500 mA	5		uA78M09	KC	2–447
10	100 mA			uA78L10A	D, LP	2–437
		10		uA78L10		
	150 mA	5	0.6	TL750L10	K, KC, LP, P	2–267
				TL751L10	D, P	
	500 mA		2	uA78M10	KC	2–447
	750 mA	1	0.6	TL750M10		2–273
				TL751M10		
	1.5 A	5	2	uA7810		2–427
12	100 mA			uA78L12A	D, JG, LP	2–437
		10		uA78L12		

positive fixed output series-pass voltage regulators (continued)

(values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
12	150 mA	5	0.6	TL750L12	D, KC, LP, D	2–267
				TL751L12	D, P	
	500 mA		2	uA78M12	JG, KC	2–447
	750 mA	1	0.6	TL750M12	KC	2–273
				TL751M12		
	1.5 A	2	2	TL780-12		2–281
		5		uA7812		2–427
15	100 mA			uA78L15A	D, LP	2–437
		10		uA78L15		
	500 mA	5		uA78M15	JG, KC	2–447
	1.5 A	2		TL780-15	KC	2–281
		5		uA7815		2–427
18				uA7818		
20	500 mA			uA78M20		2–447
24				uA78M24		
	1.5 A			uA7824		2–427
2.85	620 mA	1	0.6	TLSCSI285	KC, N, PW	2–179
	500 mA	1.5	1	TL2217-285		2–337

negative fixed output series-pass voltage regulators

(values specified over operating temperature range)

OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	MINIMUM DIFFERENTIAL VOLTAGE (V)	TYPE	PACKAGE	PAGE NO.
5	100 mA	5	1.7	MC79L05A	D, LP	2–157
		10		MC79L05		
	500 mA	5	2	uA79M05	JG, KC	2–465
	1.5 A			uA7905	KC	2–457
5.2				uA7952		
6	500 mA			uA79M06		2–465
	1.5 A			uA7906		2–457
8	500 mA			uA79M08	JG, KC	2–465
	1.5 A			uA7908	KC	2–457
12	100 mA		1.7	MC79L12A	D, LP	2–157
		10		MC79L12		
	500 mA	5	2	uA79M12	JG, KC	2–465
	1.5 A			uA7912	KC	2–457
15	100 mA		1.7	MC79L15A	D, LP	2–157
		10		MC79L15		
	500 mA	5	2	uA79M15	KC	2–465
	1.5 A			uA7915	KC	2–457
18				uA7918		
20	500 mA			uA79M20		2–465
24				uA79M24		
	1.5 A			uA7924		2–457

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM185-2.5	LM185-2.5		2–9
LM285-2.5	LM285-2.5		2–9
LM336-2.5	LM336-2.5		2–17
LM337	LM337		2–21
LM385-2.5	LM385-2.5		2–9
LT1004-2.5	LT1004-2.5		2–35
LT1009	LT1009		2–47
LT1070 (HV)	LT1070 (HV)		2–77
LT1071 (HV)	LT1071 (HV)		2–101
LT1072 (HV)	LT1072 (HV)		2–117
LT1004-1.2	LT1004-1.2		2–35
LT1054	LT1054		2–55
LT1084	LT1084		2–133
LT1117-285		TL2217-285	2–337
LT1431		TL1431	2–303
SG3524	SG3524		2–161

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM237, LM337	LM237, LM337		2–21
MC1723	uA723		2–417
MC3423	MC3423		2–147
MC34060	MC34060		2–149
MC34063	TL497		2–227
MC34064		TL7757	2–359
MC34164		TL7757	2–359
MC78L00 Series	uA78L00 Series		2–437
MC78M00 Series	uA78M00 Series		2–447
MC79L00 Series	MC79L00 Series		2–157
TL431	TL431		2–189
TL431A	TL431A		2–189
TL494	TL494		2–207
TL780-5	TL780-5		2–281
TL780-12	TL780-12		2–281
TL780-15	TL780-15		2–281

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NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM237, LM337	LM237, LM337		2–21
LM317L	TL317		2–173
LM336-2.5	LM336-2.5	LT1009	2–17 / 2–47
LM385-2.5	LM385-2.5	LT1004-2.5	2–9 / 2–35
LM723	uA723		2–417
LM2930-5	LM2930-5		2–25
LM2930-8	LM2930-8		2–25
LM3524	SG3524		2–161
LM7800 Series	uA7800 Series		2–427
LM78L00 Series	uA78L00 Series		2–437
LM78M00 Series	uA78M00 Series		2–447
LM7900 Series	uA7900 Series		2–457
LM79L00 Series	MC79L00 Series		2–157
LM79M00 Series	uA79M00 Series		2–465

SILICON GENERAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
SG3524	SG3524		2–161
SG3842/3/4/5	UC3842/3/4/5		2–475

SPRAGUE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
ULN8194	TL594		2–241

UNITRODE	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
TL431	TL431		2–185
UC337	LM337		2–21
UC494	TL494		2–207
UC494A	TL594		2–241
UC2842/3/4/5	UC2842/3/4/5		2–475
UC3842/3/4/5	UC3842/3/4/5		2–475
UC7800 Series	uA7800 Series		2–427
UC7800A Series		TL780-00 Series	2–281
UC7900 Series	uA7900 Series		2–457

SERIES REGULATORS

Bias Current

The difference between input and output currents.
NOTE: This is sometimes referred to as quiescent current.

Current-Limit Sense-Voltage

The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry. This is the current-sense voltage at which current limiting occurs.

Dropout Voltage

The low input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage

The voltage that is a function of the output voltage and is used for feedback control of the regulator.

Input Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in input voltage from one level to another level.
NOTE: Sometimes this characteristic is normalized with respect to the input voltage change.

Output Noise Voltage

The rms output noise voltage, sometimes expressed as a percentage of the dc output voltage, with constant load and no input ripple.

Output Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in load current from one level to another level.

Output Voltage Change With Temperature

The percentage change in the output voltage for a change in temperature. This is the net change over the total temperature range.

Output Voltage Long-Term Drift

The change in the output voltage over a long period of time.

Peak Output Current

The maximum output current that can be obtained from the regulator due to limiting circuitry within the regulator.

Reference Voltage

The voltage that is compared with the feedback sense voltage to control the regulator.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
NOTE: This is the reciprocal of ripple sensitivity.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage, sometimes expressed as a percentage of output voltage, to the peak-to-peak input ripple voltage.
NOTE: This is the reciprocal of ripple rejection.

Short-Circuit Output Current

The output current of the regulator with the output shorted to ground.

Standby Current

The input current drawn by the regulator with no output load and no reference voltage load.

Temperature Coefficient of Output Voltage (α_{VO})

The ratio of the change in output voltage, usually expressed as a percentage of output voltage, to the change in temperature. This is the average value for the total temperature change.

$$\alpha_{VO} = \pm \left[\frac{V_O \text{ at } T_2 - V_O \text{ at } T_1}{V_O \text{ at } 25°C} \right] \left[\frac{100\%}{T_2 - T_1} \right]$$

SHUNT REGULATORS

NOTE: These terms and symbols are based on JEDEC and IEC standards for voltage regulator diodes.

Anode
The electrode to which the regulator current flows within the regulator when it is biased for regulation.

Cathode
The electrode from which the regulator current flows within the regulator when it is biased for regulation.

Dynamic Impedance $|z_{KA}|$
The quotient of a change in voltage across the regulator and the corresponding change in current through the regulator when it is biased for regulation.

Noise Voltage (V_{nz})
The rms noise voltage with the regulator biased for regulation and with no input ripple.

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)
The voltage at the reference input terminal with respect to the anode terminal.

Regulator Current (I_Z)
The dc current through the regulator when it is biased for regulation.

Regulator Current near Lower Knee of Regulation Range (I_{ZK})
The regulator current near the lower limit of the region within which regulation occurs; this corresponds to the breakdown knee of a regulator diode.

Regulator Current at Maximum Limit of Regulation Range (I_{ZM})
The regulator current above which the differential resistance of the regulator significantly increases.

Regulator Voltage (V_Z)
The dc voltage across the regulator.

Shunt Regulator
A device having a voltage-current characteristic similar to that of a voltage-regulator diode. It is normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) and develops across its terminals an essentially constant voltage throughout a specified current range.

Temperature Coefficient of Reference Voltage (α_{Vref})
The ratio of the change in reference voltage to the change in temperature. This is the average value for the total temperature change.

To obtain a value in ppm/°C:

$$\alpha V_{ref} = \left[\frac{V_{ref \text{ at } T_2} - V_{ref \text{ at } T_1}}{V_{ref \text{ at } 25°C}}\right]\left[\frac{10^6}{T_2 - T_1}\right]$$

SWITCHING REGULATORS

Current-Mode PWM Control

A PWM control technique in which a second feedback loop is incorporated to accomplish pulse-by-pulse switch current control.

Dead Time

A fixed, load independent off time between output pulses of a switching regulator.
NOTE: This is sometimes referred to as blanking time.

Duty Cycle

The ratio of on time to off time of a switching output, usually expressed as a percentage equal to: $\frac{\text{On Time}}{\text{On Time + Off Time}}$

Parallel Operation

A dual output switching configuration in which both output stages conduct simultaneously.

Pulse-Width-Modulation (PWM) Control

A switching regulation technique in which a fixed frequency is maintained, and regulation is accomplished by changing the output pulse width to vary the duty cycle.

Push-Pull Operation

A dual output switching configuration in which each output stage conducts alternately.

Single-Ended Operation

A single output switching configuration.

Soft Start

A protection circuit that prevents current surges during power up and protects against false signals that might be generated by the control circuit when power is applied.

Undervoltage Lockout (UVLO)

A protection circuit that prevents switching outputs from turning on until a certain supply voltage threshold is reached.

Variable Frequency Control

A switching regulation technique in which a fixed output on time or off time is maintained. Regulation is accomplished by changing the output frequency to vary the duty cycle.

commercial temperature range

(values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (μA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
single channel									
Strobe	12	−6	5	40	100	28	LM306	D, P	3–33
Strobe	4–30	0	7.5	0.25	8	115	LM311	D, P, Y‡	3–3
Low-Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP311	D, P	3–45
Output Enable	5	0	±1	–	Max 16	25	TL712	D, P	3–53
High-Speed	5	0	–	–	Max 16	7	TL714C	D, P	3–57
High-Speed	0	−5.2	±1	–	Max 16	Max 12	TL721	D, P	3–61
High-Speed, LinCMOS	3–16	0	3	†	6	200	TLC371C	D, P	3–97
dual channel									
Low-Power, Bipolar	4–30	0	5	0.25	6	300	LM393	D, DB, P, PW, Y‡	3–27
Precision Input	4–30	0	2	0.25	6	300	LM393A	D, P	
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352C	D, P	3–81
High-Speed, LinCMOS	3–16	0	5	†	6	200	TLC372C	D, P	3–109
Ultra Low-Power, Open-Drain Output, CMOS	3–18	0	5	†	6	1100	TLC393C	D, P	3–129
Ultra Low-Power, Push-Pull Output, CMOS	3–18	0	5	†	4	1300	TLC3702C	D, P	3–145
quad channel									
Low-Power, Bipolar	4–30	0	5	−0.25	6	300	LM339	D, DB, N, PW, Y‡	3–19
Precision Input	4–30	0	2	−0.25	6	300	LM339A	D, N	
Ultra Low-Power, Bipolar	4–30	0	±5	−0.025	6	8000	LP339	D, N	3–49
Ultra Low-Power, Open-Drain Output, CMOS	3–18	0	5	†	6	1100	TLC339C	D, N	3–65
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354C	D, N	3–89
High-Speed, CMOS	3–18	0	10	†	6	200	TLC374C	D, N	3–119
Ultra Low-Power, Push-Pull Output, CMOS	3–18	0	5	†	4	1300	TLC3704C	D, N	3–167

† Typically 5 pA
‡ Y package is in chip form

industrial temperature range

(values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (μA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
single channel									
Strobe	4–30	0	3	0.1	8	115	LM211	D, P	3–3
Low-Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP211	D, P	3–45
dual channel									
Industrial LM393	4–30	0	5	0.25	6	300	LM293	D, P	3–27
Industrial LM393, Low Offset	4–30	0	2	0.25	6	300	LM293A	D, P	
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352I	D, P	3–81
High-Speed, LinCMOS	3–16	0	5	†	6	200	TLC371I	D, P	3–97
High-Speed, LinCMOS	3–16	0	5	†	6	200	TLC372I	D, P	3–109
Ultra Low-Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC393I	D, P	3–129
Ultra Low-Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3702I	D, P	3–145
quad channel									
Industrial LM339	4–30	0	5	−0.25	6	300	LM239	D, N	3–19
Industrial LM339, Low Offset	4–30	0	2	−0.25	6	300	LM239A	D, N	
Ultra Low-Power, Industrial LP339, Bipolar	4–30	0	±5	−0.025	20	8000	LP239	D, N	3–49
Ultra Low-Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC339I	D, N	3–65
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354I	D, N	3–89
High-Speed, LinCMOS	3–18	0	10	†	6	200	TLC374I	D, N	3–119
Ultra Low-Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3704I	D, N	3–167

† Typically 5 pA

automotive temperature range

(values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (μA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
dual channel									
Automotive LM393	4–30	0	7	0.25	6	300	LM2903, LM2903Q	D, DB, P, PW	3–27
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352I	D, P	3–81
High-Speed, LinCMOS	3–16	0	5	†	6	200	TLC372Q	D, P	3–109
Ultra Low-Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC393I	D, P	3–129
Ultra Low-Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3702Q	JG	3–145
quad channel									
Automotive LM339	4–30	0	7	−0.25	6	300	LM2901, LM2901Q	D, DB, N, PW	3–19
Low-Cost LM2901	4–26	0	20	0.5	6	300	LM3302	D, N	3–41
Ultra Low-Power, Automotive LP339, Bipolar	5	0	±5	−0.025	20	8000	LP2901	D, N	3–49
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354I	D, N	3–89
Open-Drain Output	3–18	0	5	†	6	1100	TLC339Q	D, N	3–65
High-Speed, LinCMOS	3–18	0	10	†	6	200	TLC374Q	D, N	3–119
Push-Pull Output	3–18	0	5	†	4	1300	TLC3704Q	J	3–167

† Typically 5 pA

military temperature range

(values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (μA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
single channel									
Strobe	4–30	0	3	0.1	8	115	LM111	FK, J, JG, U	3–3
Low-Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP111	FK, JG	3–45
dual channel									
Low-Power, Bipolar	4–30	0	5	0.1	6	300	LM193	D, FK, JG, P	3–27
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352M	FK, JG	3–81
High-Speed, LinCMOS	4–16	0	5	†	6	200	TLC371M	D, P	3–97
High-Speed, LinCMOS	4–16	0	5	†	6	200	TLC372M	FK, JG	3–109
Ultra Low-Power, Open-Drain Output	4–18	0	5	†	6	1100	TLC393M	FK, JG	3–129
Ultra Low-Power, Push-Pull Output	4–18	0	5	†	4	1300	TLC3702M	FK, JG	3–145
quad channel									
Low-Power, Bipolar	4–30	0	5	−0.1	6	300	LM139	D, FK, J, N	3–19
Precision Input	4–30	0	2	−0.1	6	300	LM139A	D, FK, J, N	
Ultra Low-Power, Open-Drain Output	4–18	0	5	†	6	1100	TLC339M	D, FK, J, N	3–65
Ultra Low-Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354M	FK, J	3–89
High Speed, LinCMOS	4–18	0	10	†	6	200	TLC374M	FK, J	3–119
Ultra Low-Power, Push-Pull Output	4–18	0	5	†	4	1300	TLC3704M	FK, J	3–167

† Typically 5 pA

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

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Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY	SUGGESTED TI REPLACEMENT	PAGE NO.
LT1017	TLC352 or TLC3702	3–81 / 3–145
LT1018	TLC352, or TLC3702	3–81 / 3–145

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM311	LM311		3–3
LM339	LM339	TLC339	3–19 / 3–65
LM393	LM393	TLC393	3–27 / 3–129
LM2901	LM2901	TLC339	3–19 / 3–65
LM3302	LM3302		3–41
LP339	LP339	TLC339	3–49 / 3–65

PMI	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
CMP04F		LM339, LM3302, LM2901, or TLC339	3–19 / 3–41 / 3–65

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha I_{IO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha V_{IO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the comparator to cease functioning properly.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.

NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Differential Input Voltage Range (V_{ID})

The range of voltage between the two input terminals that if exceeded will cause the comparator to cease functioning properly.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant.

High-Level Output Current (I_{OH})

The current into an output with input conditions applied that according to the product specification will establish a high level at the output.

High-Level Output Voltage (V_{OH})

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

High-Level Strobe Current ($I_{IH(S)}$)

The current flowing into or out of† the strobe at a high-level voltage.

High-Level Strobe Voltage ($V_{IH(S)}$)

For a device having an active-low strobe, a voltage within that range is guaranteed not to interfere with the operation of the comparator.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at the specified level.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at the specified level.

† Current out of a terminal is given as a negative value.

Input Offset Voltage (V_{IO})
The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to the specified level.

Input Voltage Range (V_I)
The range of voltage that if exceeded at either input terminal will cause the comparator to cease functioning properly.

Low-Level Output Current (I_{OL})
The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

Low-Level Output Voltage (V_{OL})
The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

Low-Level Strobe Current ($I_{IL(S)}$)
The current flowing out of† the strobe at a low-level voltage.

Low-Level Strobe Voltage ($V_{IL(S)}$)
For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

Output Resistance (r_o)
The resistance between an output terminal and ground.

Response Time
The interval between the application of an input step function and the instant the output crosses the logic threshold voltage.

NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time
The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

Supply Current (I_{CC+}, I_{CC-})
The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit.

Total Power Dissipation (P_D)
The total dc power supplied to the device less any power delivered from the device to a load.

NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$.

† Current out of a terminal is given as a negative value.

precision timers

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	10 µs	Hours	NE555	D, P, Y†	4–11
Dual Timer, Bipolar	±200 mA	10 µs	Hours	NE556	D, N	4–33
LinCMOS, Single HIgh-Speed Timer, 1-V Operation	100 mA −10 mA	1 µs	Hours	TLC551	D, P, Y†	4–123
LinCMOS, Dual HIgh-Speed Timer, 1-V Operation	100 mA −10 mA	1 µs	Hours	TLC552C	D, N	4–135
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC555C	D, P	4–143
				TLC555Y	Y†	
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC556C	D, N	4–153
Programmable Timer/Counter	4 mA	10 µs	Days	uA2240C	N	4–173

† Y package is in chip form

automotive temperature range

(values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	10 µs	Hours	SA555	D, P	4–11
Dual Timer, Bipolar	±200 mA	10 µs	Hours	SA556	D, N	4–33
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC555I	D, P	4–143
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC556I	D, N	4–153

military temperature range

(values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	1 µs	Hours	SE555	D, FK, JG, P	4–11
Single Timer, Bipolar	±200 mA	1 µs	Hours	SE555C	D, FK, JG, P	
Dual Timer, Bipolar	±200 mA	1 µs	Hours	SE556	D, FK, J, N	4–33
Dual Timer, Bipolar	±200 mA	1 µs	Hours	SE556C	D, FK, J, N	
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC555M	D, FK, JG, P	4–143
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 µs	Hours	TLC556M	D, FK, J, N	4–153

current mirrors

(values specified for T_A = 25°C)

DESCRIPTION	TEMPERATURE RANGE	CURRENT RATIO INPUT TO OUTPUT	INPUT CURRENT RANGE	TYPE	PACKAGES	PAGE NO.
Programmable	0°C to 70°C	3:1 to 1:15	Variable	TL010C	P	4–45
Programmable	−40°C to 85°C	3:1 to 1:15	Variable	TL010I	P	
Fixed	0°C to 70°C	1:1	1 μA to 1 mA	TL011C	LP	4–49
Fixed	−40°C to 85°C	1:1	1 μA to 1 mA	TL011I	LP	
Fixed	0°C to 70°C	1:2	1 μA to 1 mA	TL012C	LP	
Fixed	−40°C to 85°C	1:2	1 μA to 1 mA	TL012I	LP	
Fixed	0°C to 70°C	1:4	1 μA to 1 mA	TL014AC	LP	
Fixed	0°C to 70°C	1:2	2 μA to 2 mA	TL021C	LP	
Fixed	−40°C to 85°C	1:2	2 μA to 2 mA	TL021I	LP	

sonar ranging functions

(values specified for T_A = 25°C)

DESCRIPTION		TYPE	PACKAGES	PAGE NO.
Controller Circuit	Control integrated circuit for use in a sonar ranging module, capable of driving 50-kHz transducers with a simple interface	TL851	N	4–109
Receiver Circuit	Receiver integrated circuit for use in a sonar ranging module	TL852	N	4–113
Control Circuit	Control integrated circuit for use in a sonar ranging module, capable of driving 40-kHz transducers With a simple interface	TL853	N	4–119

floppy-disk control circuits

(values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
Tape-Read Signal Conditioner	TL041AC	DW, NT	4–77
Disk-Memory Read-Chain Data Comparator	TL712	D, JG, P	3–53
Disk-Memory Read-Chain Data Comparator With MECL III and MECL 1000	TL721	D, JG, P	3–61

differential video amplifiers

commercial temperature range

(values specified for T_A = 25°C)

DESCRIPTION	BANDWIDTH (MHz)	GAIN	TYPICAL NOISE, V_n	TYPE	PACKAGES	PAGE NO.
Amplifier With 2 Multiplexed Inputs and Wide AGC Range	60	100 Max	25 μV	MC1445	J, N	4–9
Amplifier With Internal Frequency Compensation and Adjustable/Selectable Gain Options	90	600 Max	12 μV	NE592	D, N	4–25
Amplifier With a Wide AGC Range	50	100	12 μV	TL026C	D, P	4–55
Amplifier With a Wide AGC Range	50	400 Max	12 μV	TL027C	D, J, N	4–63
2-Channel Multiplexed Video Amp	20	600 Max	<5 μV	TL040C	D, N	4–71
Similar to NE592 but in an 8-Pin Package	90	600 Max	12 μV	TL592	D, P	4–99
Low-Noise Version of NE592 and TL592	90	600 Max	3 μV	TL592B	D, N, P	4–103
Amplifier With Internal Frequency Compensation	200	10, 100, 400	12 μV	uA733C	D, N	4–165

military temperature range

(values specified for T_A = 25°C)

DESCRIPTION	BANDWIDTH (MHz)	GAIN	TYPICAL NOISE, V_n	TYPE	PACKAGES	PAGE NO.
Amplifier With Internal Frequency Compensation and Adjustable/Selectable Gain Options	90	600 Max	12 μV	SE592	J	4–25
Amplifier With Internal Frequency Compensation	200	10, 100, 400	12 μV	uA733M	J, U	4–165

logarithmic amplifiers

(values specified for military temperature range)

DESCRIPTION	BANDWIDTH	GAIN	TYPE	PACKAGES	PAGE NO.
Logarithmic Amplifier	40 MHz	Logarithmic Curve	TL441AM	J, FK	4–85

programmable tone/noise generators

(values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
Complex Sound Generators Designed to Provide Low-Cost Digital Tones or Noise Programmable White-Noise and Attenuation Functions, and Simultaneous Sounds Under Microprocessor Control TTL Compatible	SN76494/ SN76494A SN76496/ SN76496A	N	4–37

frequency-to-voltage-converters

(values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
Output Swings to Ground for Zero-Frequency Input Only One RC Network Provides Frequency Doubling for Low Ripple 8-Pin Version Interfaces Directly to Variable Reluctance Magnetic Pickups	LM2907 LM2917	D, N, P	4–3

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Manufacturers are arranged in alphabetical order.

INTERSIL		SUGGESTED TI REPLACEMENT	PAGE NO.
ICM7555		TLC555	4–143

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1445	MC1445		4–9
MC1733		uA733	4–165
NE555	NE555		4–11
NE592	NE592		4–25

SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
NE555	NE555	TLC555	4–11 / 4–143
NE556	NE556	TLC556	4–33 / 4–153
NE592	NE592		4–25
SA555	SA555	TLC555	4–11 / 4–143
SA556	SA556	TLC556	4–33 / 4–153
SE555	SE555	TLC555	4–11 / 4–143
SE555C	SE555C	TLC555	4–11 / 4–143
SE5556	SE556	TLC556	4–33 / 4–153
SE556C	SE556C	TLC556	4–33 / 4–153
uA733	uA733	uA733	4–165

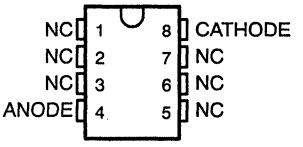
General Information 1
VRegs/Supervisors and Bldg Blocks 2
Comparators 3
Special Functions 4
Thermal Design Considerations 5
Mechanical Data 6

2 VRegs/Supervisors and Bldg Blocks

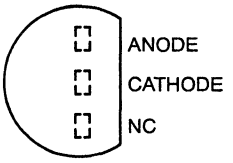
D3268, APRIL 1989–REVISED AUGUST 1991

- **Operating Current Range . . . 10 μA to 20 mA**
- **1% and 2% Initial Voltage Tolerance**
- **Reference Impedance**
  LM185 . . . 0.6 Ω Max at 25°C
  LM385 . . . 1 Ω Max at 25°C
  All Devices . . . 1.5 Max Over Full Temperature Range
- **Very Low Power Consumption**
- **Applications:**
  Portable Meter References
  Portable Test Instruments
  Battery-Operated Systems
  Current-Loop Instrumentation
  Panel Meters
- **Designed to Be Interchangeable With National LM185-1.2, LM285-1.2, and LM385-1.2**

D PACKAGE
(TOP VIEW)

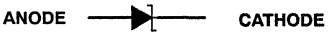


LP PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



description

These micropower terminal band-gap voltage references operate over a 10-μA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The LM185-1.2 series band-gap reference has low noise and good long-term stability.

Careful design of the LM185-1.2 series has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating temperature range allows its use with widely varying supplies with excellent regulation.

The extremely low-power drain of the LM185-1.2 series makes it useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current range allows them to replace older references with a tighter tolerance part.

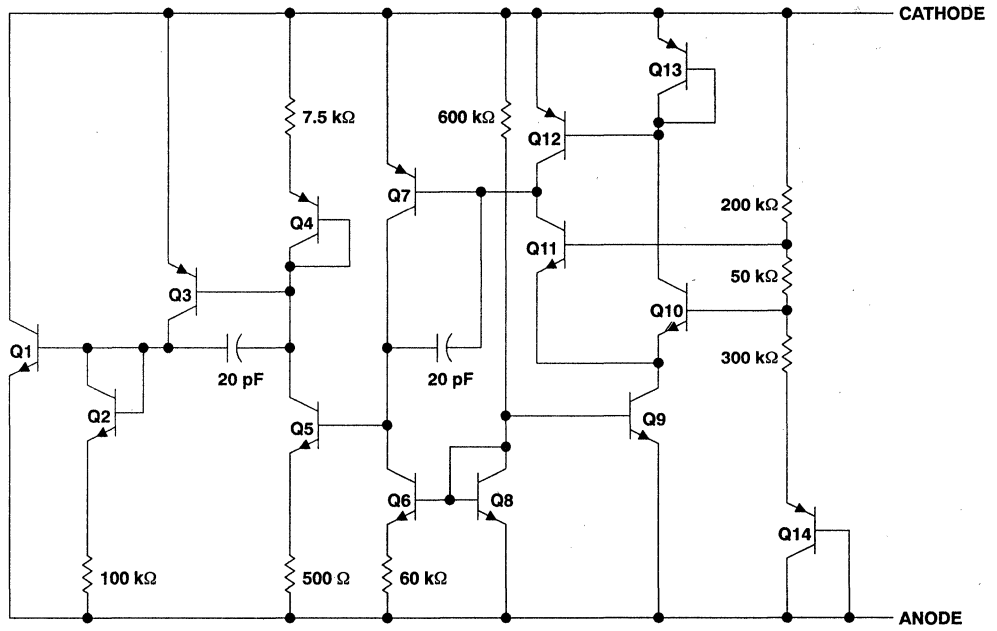
The LM185-1.2 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM285-1.2 is characterized for operation from −40°C to 85°C. The LM385-1.2 and LM385B-1.2 are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_Z TOLERANCE	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC (LP)
0°C to 70°C	2%	LM385D-1.2	LM385LP-1.2
	1%	LM385BD-1.2	LM385BLP-1.2
−40°C to 85°C	1%	LM285D-1.2	LM285LP-1.2
−55°C to 125°C	1%	LM185D-1.2	LM185LP-1.2

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM385DR-1.2).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current, I_R ..... 30 mA
Forward current, I_F ..... 10 mA
Operating free-air temperature range: LM185-1.2 ..... −55°C to 125°C
LM285-1.2 ..... −40°C to 85°C
LM385-1.2, LM385B-1.2 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

recommended operating conditions

		MIN	MAX	UNIT
Reference current, I_Z		10	20000	μA
Operating free-air temperature range, T_A	LM185-1.2	−55	125	°C
	LM285-1.2	−40	85	
	LM385-1.2, LM385B-1.2	0	70	

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LM185-1.2 LM285-1.2			LM385-1.2			LM385B-1.2			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 10 μA to 20 mA	25°C	1.223	1.235	1.247	1.210	1.235	1.260	1.223	1.235	1.247	V
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 10 μA to 20 mA	25°C		±20			±20			±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 10 μA to 1 mA	25°C			1			1			1	mV
			Full range			1.5			1.5			1.5	
		I_Z = 1 mA to 20 mA	25°C			10			20			20	
			Full range			20			25			25	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 μA	25°C		±20			±20			±20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range		8	10		8	15		8	15	μA
Z_Z	Reference impedance	I_Z = 100 μA	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 μA, f = 10 Hz to 10 kHz	25°C		60			60			60		μV

† Full range is −55°C to 125°C for the LM185-1.2, −40°C to 85°C for the LM285-1.2, and 0°C to 70°C for the LM385-1.2 and LM385B-1.2.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REVERSE CURRENT
vs
REVERSE VOLTAGE

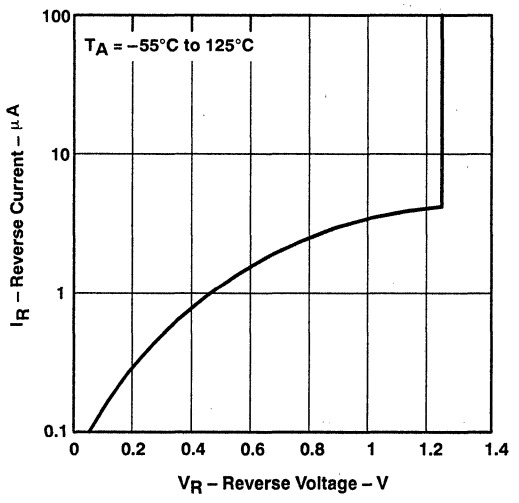


Figure 1

REFERENCE VOLTAGE CHANGE
vs
REVERSE CURRENT

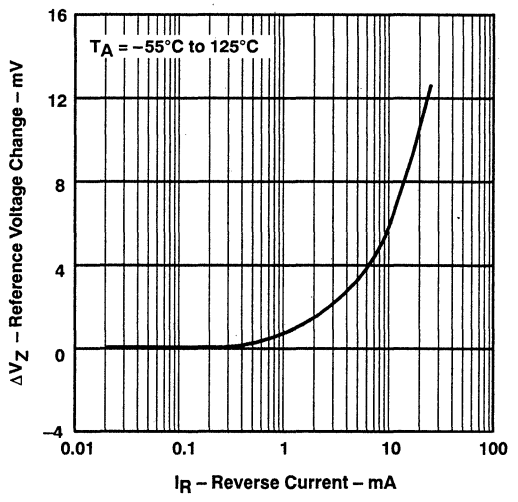


Figure 2

FORWARD VOLTAGE
vs
FORWARD CURRENT

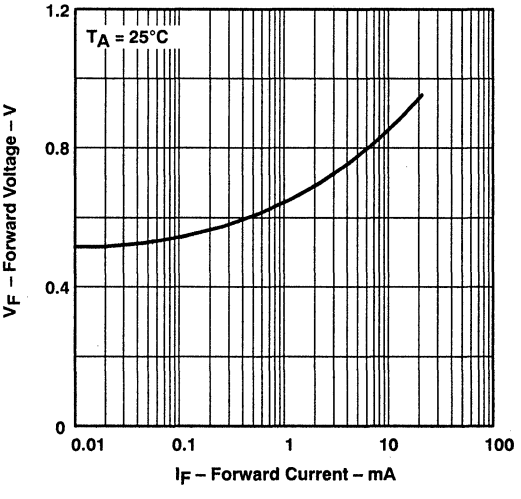


Figure 3

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

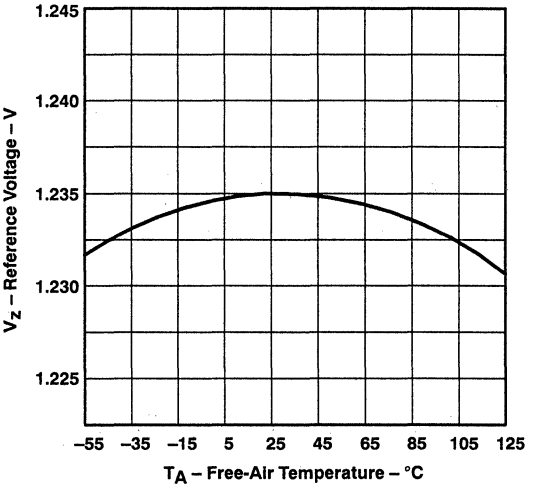


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

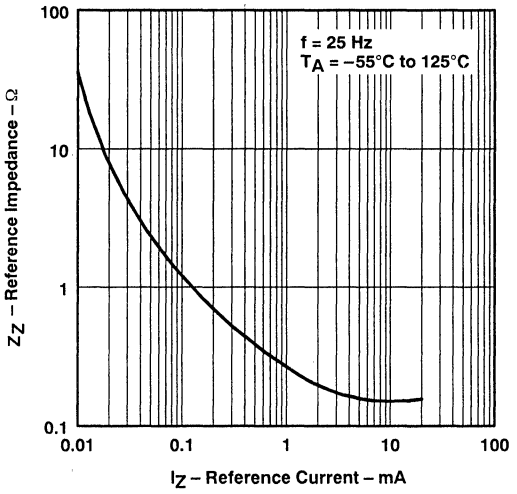


Figure 5

NOISE VOLTAGE
vs
FREQUENCY

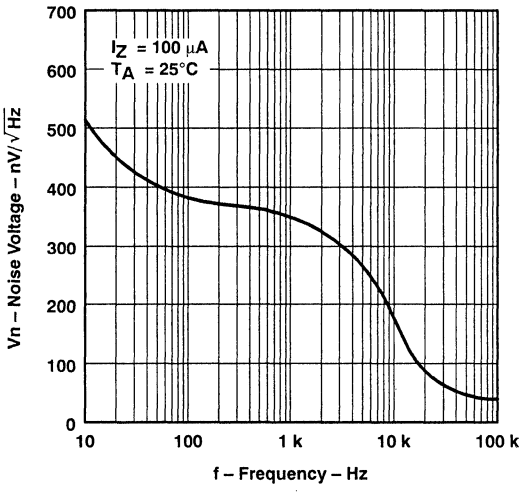


Figure 6

OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

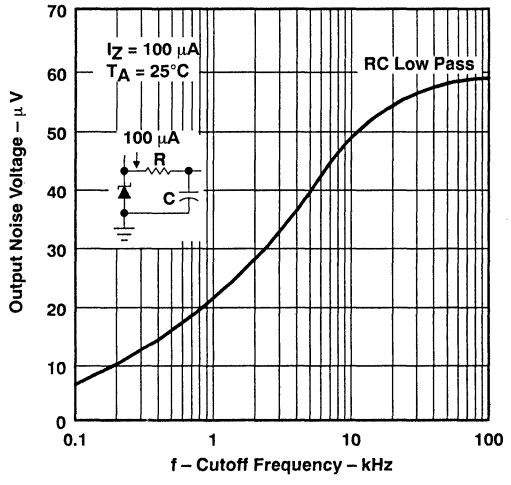


Figure 7

TRANSIENT RESPONSE

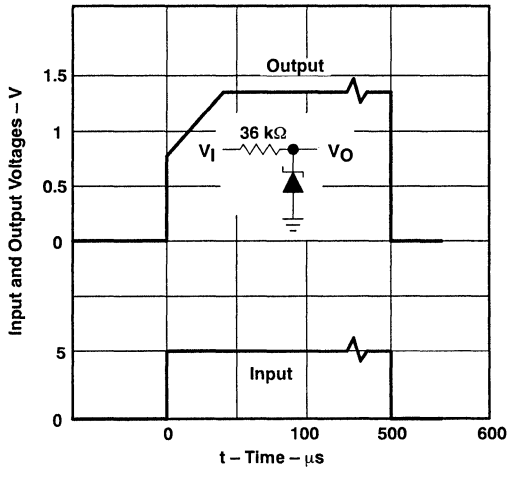


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

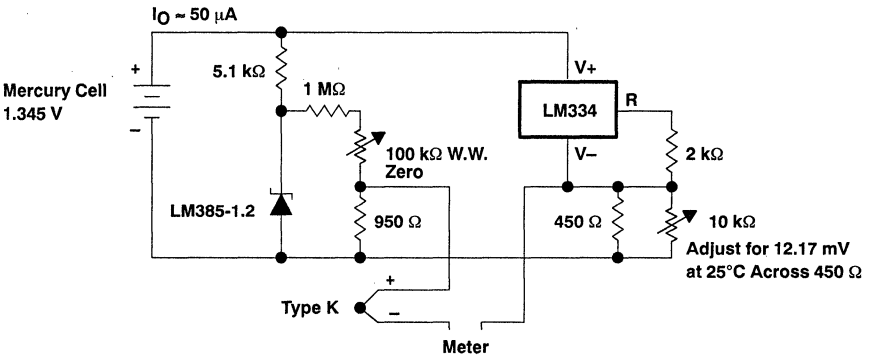


Figure 9. Thermocouple Cold-Junction Compensator

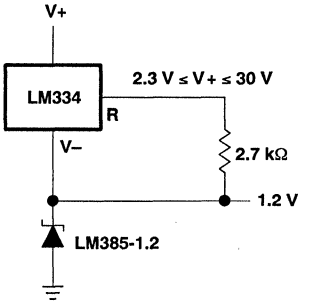


Figure 10. Operation Over a Wide Supply Range

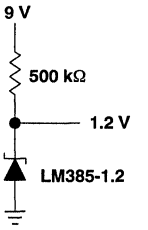
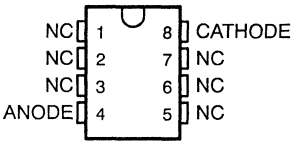


Figure 11. Reference From a 9-V Battery

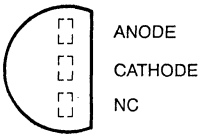
D3189, JANUARY 1989–REVISED JANUARY 1992

- **Operating Current Range . . . 20 μA to 20 mA**
- **1.5% and 3% Initial Voltage Tolerance**
- **Reference Impedance**
  - **LM185 . . . 0.6 Ω Max at 25°C**
  - **LM385 . . . 1 Ω Max at 25°C**
  - **All Devices . . . 1.5 Ω Max Over Full Temperature Range**
- **Very Low Power Consumption**
- **Applications:**
  - **Portable Meter References**
  - **Portable Test Instruments**
  - **Battery-Operated Systems**
  - **Current-Loop Instrumentation**
  - **Panel Meters**
- **Designed to Be Interchangeable With National LM185-2.5, LM285-2.5, and LM385-2.5**

D PACKAGE
(TOP VIEW)

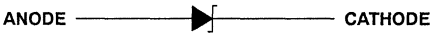


LP PACKAGE
(TOP VIEW)



NC–No internal connection

symbol



description

These micropower terminal band-gap voltage references operate over a 10-μA to 20-mA current range and feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming provides tight voltage tolerance. The LM185-2.5 series band-gap reference has low noise and good long-term stability.

Careful design of the LM185-2.5 series has made these devices exceptionally tolerant of capacitive loading, making them easy to use in almost any reference application. The wide dynamic operating temperature range allows their use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 series makes it useful for micropower circuitry. These voltage references can be used to make portable meters, regulators, or general-purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current range allows them to replace older references with a tighter tolerance part.

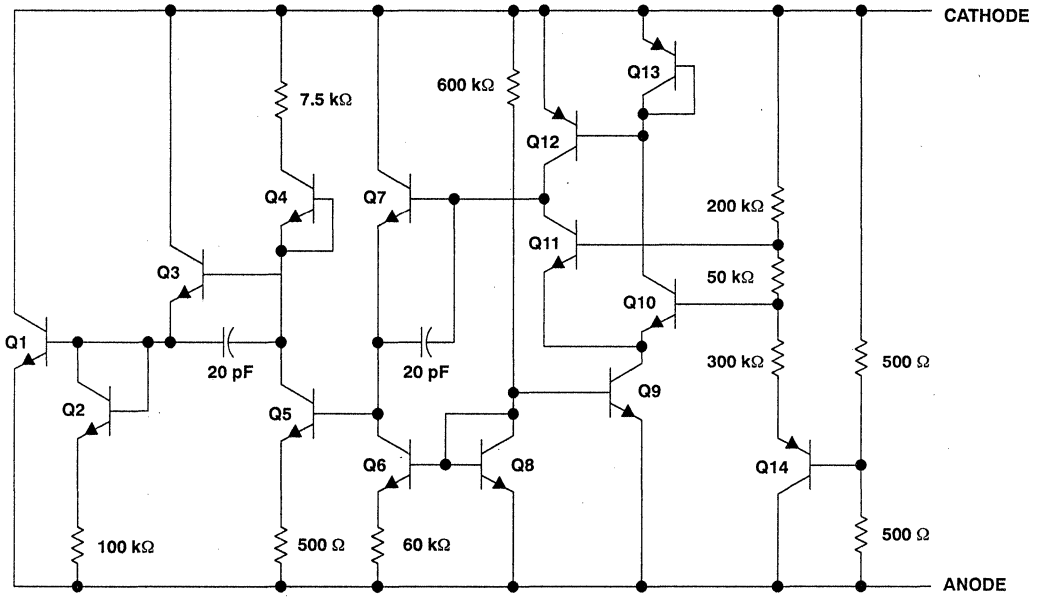
The LM385-2.5 and LM385B-2.5 are characterized for operation from 0°C to 70°C. The LM285-2.5 is characterized for operation from −40°C to 85°C. The LM185-2.5 is characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_Z TOLERANCE	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC (LP)
0°C to 70°C	3%	LM385D-2.5	LM385LP-2.5
	1.5%	LM385BD-2.5	LM385BLP-2.5
−40°C to 85°C	1.5%	LM285D-2.5	LM285LP-2.5
−55°C to 125°C	1.5%	LM185D-2.5	LM185LP-2.5

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM385DR-2.5).

schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current, I_R ..... 30 mA
Forward current, I_F ..... 10 mA
Operating free-air temperature range: LM185-2.5 ..... −55°C to 125°C
LM285-2.5 ..... −40°C to 85°C
LM385-2.5, LM385B-2.5 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds ..... 260°C

recommended operating conditions

		MIN	MAX	UNIT
Reference current, I_Z		20	20000	μA
Operating free-air temperature range, T_A	LM185-2.5	−55	125	°C
	LM285-2.5	−40	85	
	LM385-2.5, LM385B-2.5	0	70	

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	LM185-2.5 LM285-2.5			LM385-2.5			LM385B-2.5			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 20 μA to 20 mA	25°C	2.462	2.5	2.538	2.425	2.5	2.575	2.462	2.5	2.538	V
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 20 μA to 20 mA	25°C		±20			±20			±20		ppm/°C
ΔV_Z	Change in reference voltage with current	I_Z = 20 μA to 1 mA	25°C			1			2			2	mV
			Full range			1.5			2			2	
		I_Z = 1 μA to 20 mA	25°C			10			20			20	
			Full range			20			25			25	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 100 μA	25°C		±20			±20			±20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range		8	20		8	20		8	20	μA
Z_Z	Reference impedance	I_Z = 100 μA	25°C		0.2	0.6		0.4	1		0.4	1	Ω
			Full range			1.5			1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 μA, f = 10 Hz to 10 kHz	25°C		120			120			120		μV

† Full range is 0°C to 70°C for the LM385-2.5 and LM385B-2.5, −40°C to 85°C for the LM285-2.5, and −55°C to 125°C for the LM185-2.5.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REVERSE CURRENT
vs
REVERSE VOLTAGE

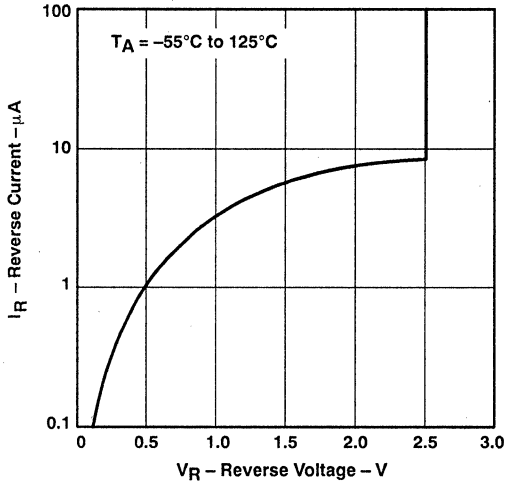


Figure 1

REFERENCE VOLTAGE CHANGE
vs
REVERSE CURRENT

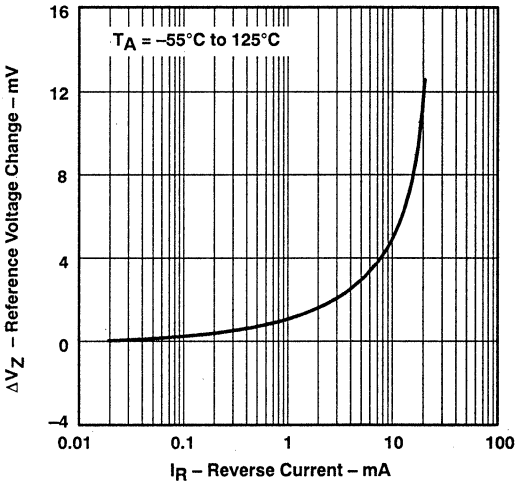


Figure 2

FORWARD VOLTAGE
vs
FORWARD CURRENT

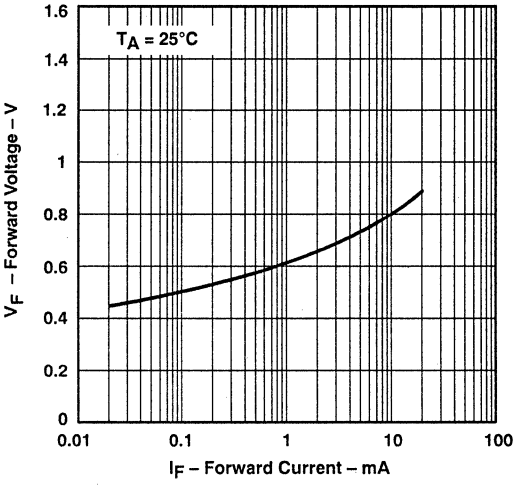


Figure 3

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

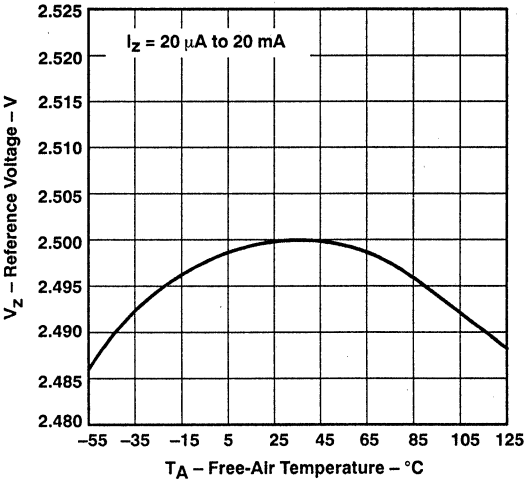


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

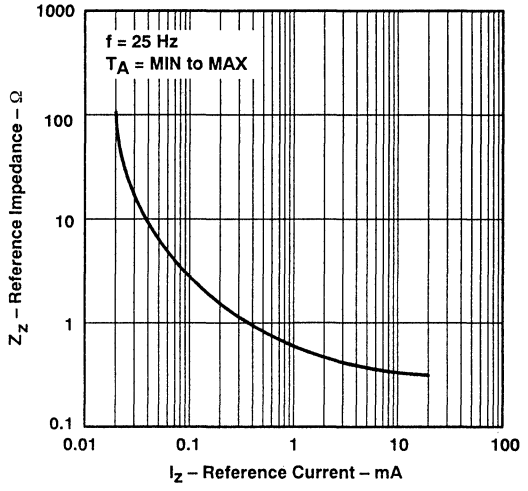


Figure 5

REFERENCE IMPEDANCE
vs
FREQUENCY

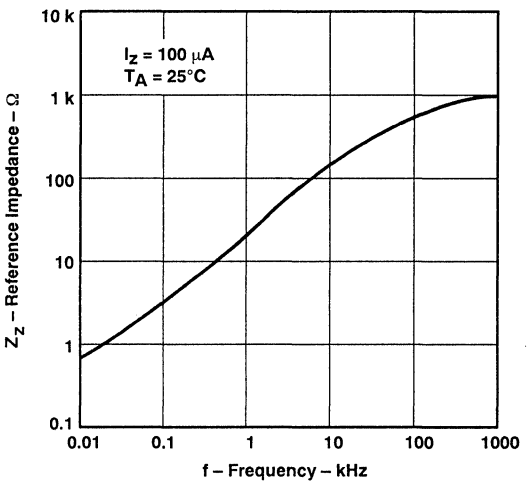


Figure 6

NOISE VOLTAGE
vs
FREQUENCY

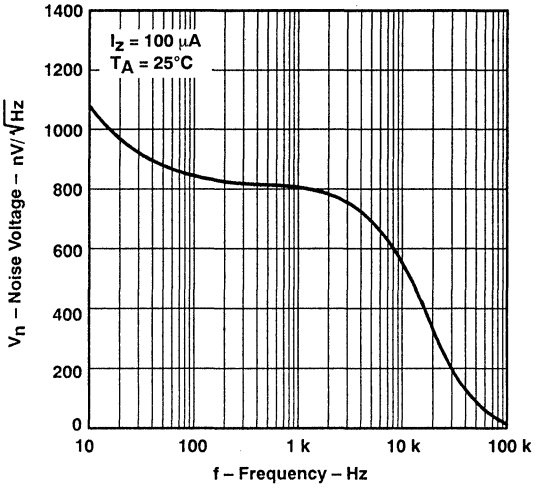


Figure 7

FILTERED RMS OUTPUT NOISE VOLTAGE
vs
FREQUENCY

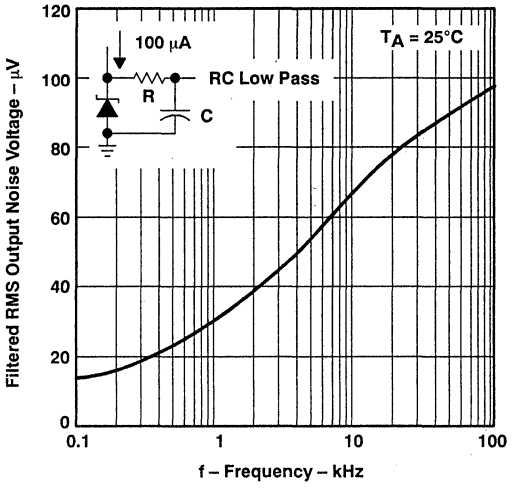


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

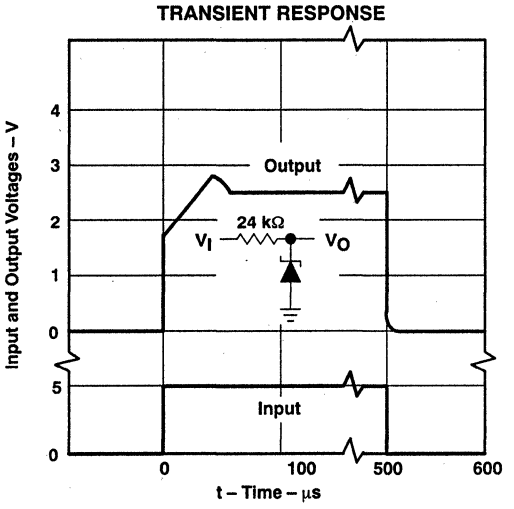


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

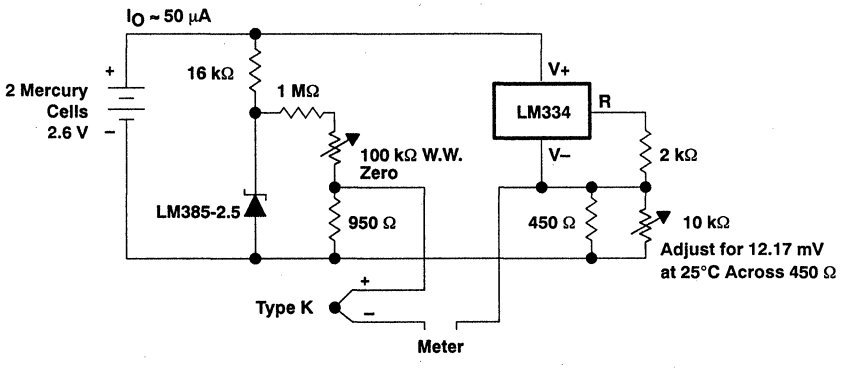


Figure 10. Thermocouple Cold-Junction Compensator

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

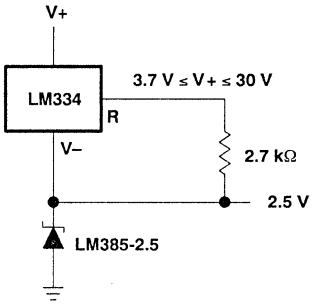


Figure 11. Operation Over a Wide Supply Range

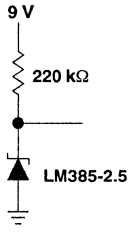
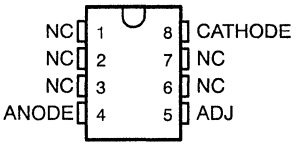


Figure 12. Reference From a 9-V Battery

D3289, NOVEMBER 1988–REVISED AUGUST 1991

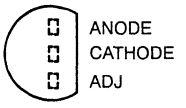
- **Low Temperature Coefficient**
- **Wide Operating Current . . . 400 μA to 10 mA**
- **0.2-Ω Dynamic Impedance**
- **±1% Tolerance Available**
- **Specified Temperature Stability**
- **Easily Trimmed for Minimum Temperature Drift**
- **Fast Turn-On**
- **Three-Lead Transistor Package**

D PACKAGE
(TOP VIEW)



NC-No internal connection

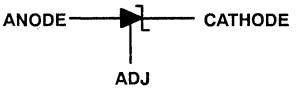
LP PACKAGE
(TOP VIEW)



description

The LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5-V shunt regulator diodes. These monolithic references operate as a low-temperature coefficient 2.5-V zener with a 0.2-Ω dynamic impedance. A third terminal provided on the circuits allows the reference voltage and temperature coefficient to be easily trimmed.

symbol



The series are useful as a precision 2.5-V low-voltage reference (V_Z) for digital voltmeters, power supplies, or operational amplifier circuitry. The 2.5-V voltage reference makes it convenient to obtain a stable reference from 5-V logic supplies. Since the series operate as shunt regulators, they can be used as either positive or negative voltage references.

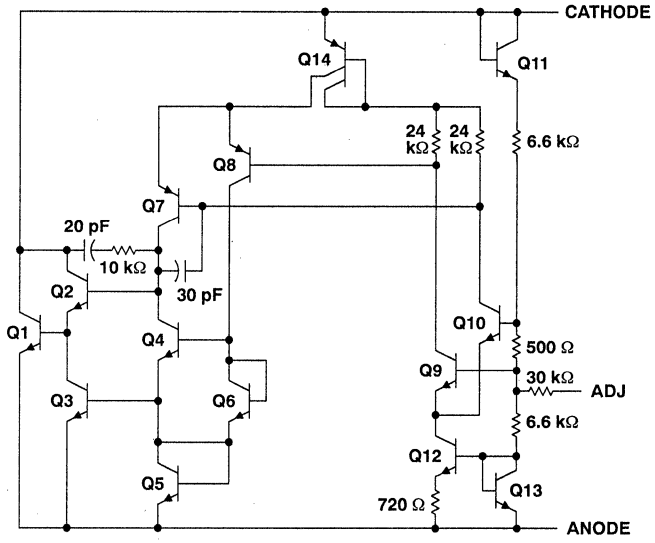
The LM236-2.5 is characterized for operation from –25°C to 85°C. The LM336-2.5 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC (LP)
0°C to 70°C	LM336D-2.5	LM336LP-2.5
–25°C to 85°C	LM236D-2.5	LM236LP-2.5

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LM336DR-2.5).

schematic diagram



All component values are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Reverse current ..... 20 mA
Forward current ..... 10 mA
Operating free-air temperature range: LM236-2.5 ..... −25°C to 85°C
LM336-2.5 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or LP package ..... 260°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LM236-2.5			LM336-2.5			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	LM236, LM336	25°C	2.44	2.49	2.54	2.39	2.49	2.59	V
			LM236A, LM336B		2.465	2.49	2.515	2.44	2.49	2.54	
$\Delta V_{Z(\Delta T)}$	Change in reference voltage with temperature‡	V_Z adjusted to 2.490 V, I_Z = 1 mA		Full range		3.5	9		1.8	6	mV
$\Delta V_{Z(\Delta I)}$	Change in reference voltage with current	I_Z = 400 μA to 10 mA		25°C		2.6	6		2.6	10	mV
				Full range		3	10		3	12	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 1 mA		25°C		20			20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA, f = 1 kHz		25°C		0.2	0.6		0.2	1	Ω
				Full range		0.4	1		0.4	1.4	

† Full range is −25°C to 85°C for the LM236-2.5 and 0°C to 70°C for the LM336-2.5.
‡ Temperature stability (change in reference voltage with temperature) for these devices is ensured by design. Design limits are specified over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

TYPICAL CHARACTERISTICS

CHANGE IN REFERENCE VOLTAGE
vs
REFERENCE CURRENT

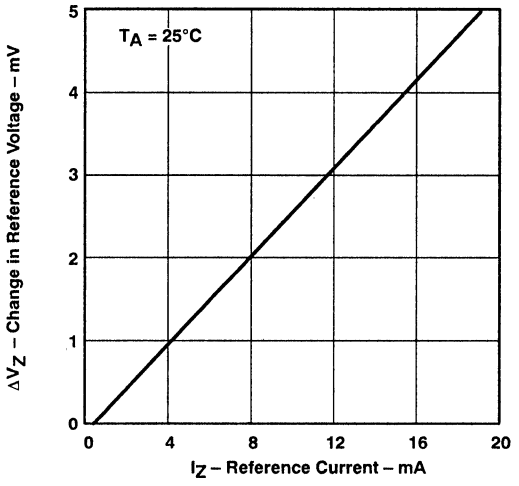


Figure 1

NOISE VOLTAGE
vs
FREQUENCY

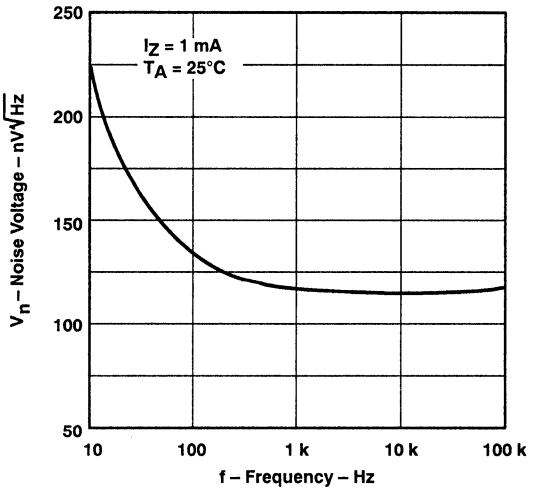


Figure 2

REFERENCE IMPEDANCE
vs
FREQUENCY

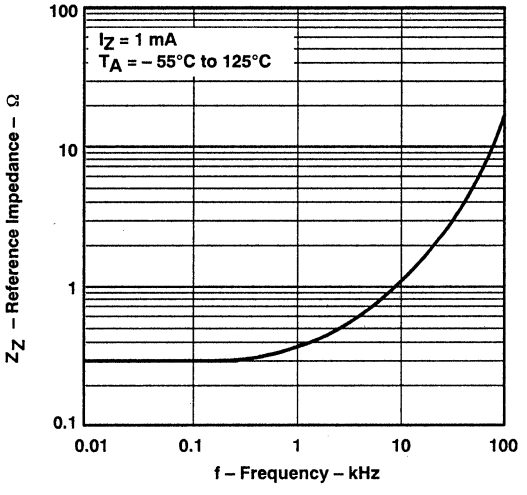
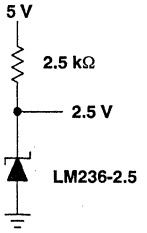


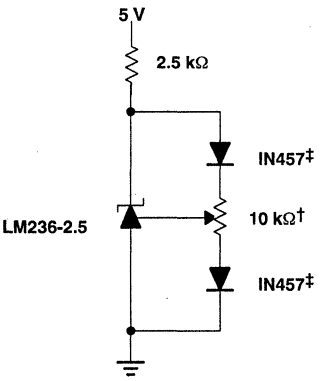
Figure 3

APPLICATION INFORMATION

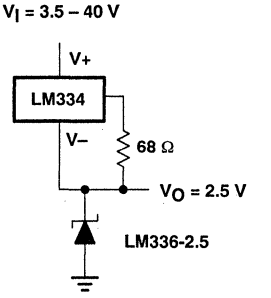
2.5-V REFERENCE



2.5-V REFERENCE WITH MINIMUM TEMPERATURE COEFFICIENT



WIDE INPUT RANGE REFERENCE

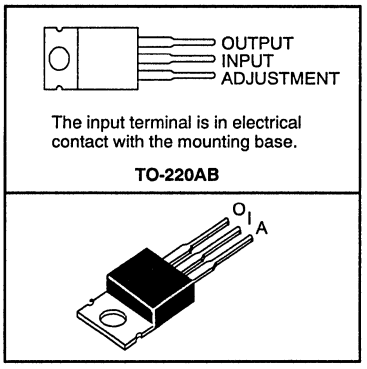


† Adjust to 2.49 V
‡ Any silicon signal diode

D2640, NOVEMBER 1981–REVISED NOVEMBER 1991

- **Output Voltage Range Adjustable From –1.2 V to –37 V**
- **I_O Capability of 1.5 A Max**
- **Input Regulation Typically 0.01% Per Input-Voltage Change**
- **Output Regulation Typically 0.3%**
- **Peak Output Current Constant Over Temperature Range of Regulator**
- **Ripple Rejection Typically 77 dB**
- **Direct Replacement for National Semiconductor LM237, LM337**

LM237, LM337 . . . KC PACKAGE
(TOP VIEW)

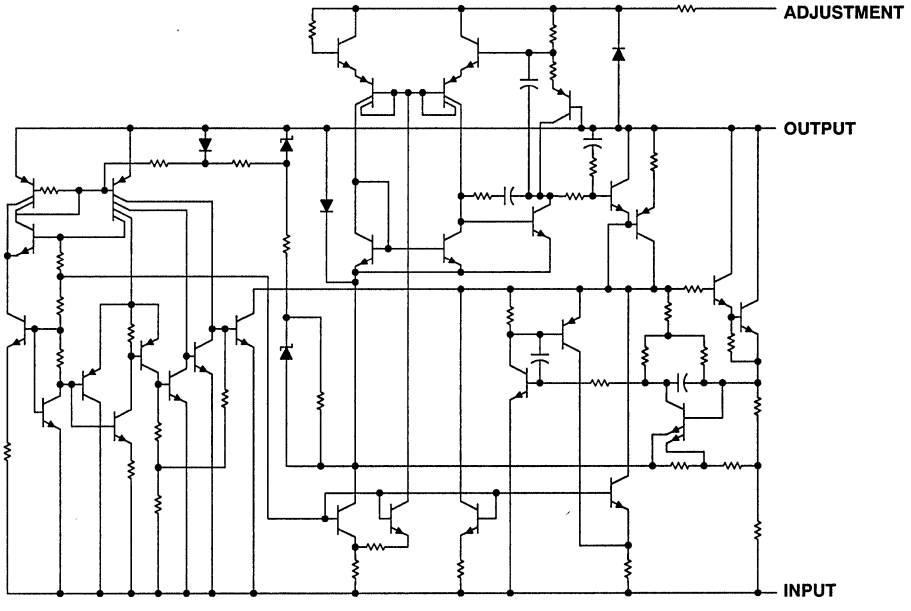


description

The LM237 and LM337 are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of –1.5 A over an output voltage range of –1.2 V to –37 V. They are exceptionally easy to use, requiring only two external resistors to set the output voltage and one output capacitor for frequency compensation. The current design has been optimized for excellent regulation and low thermal transients. In addition, the LM237 and LM337 feature internal current limiting, thermal shutdown, and safe-area compensation, making them virtually immune to blowout by overloads.

The LM237 and LM337 serve a wide variety of applications including local on-card regulation, programmable output voltage regulation, or precision current regulation.

schematic diagram



absolute maximum ratings over operating temperature ranges (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ ..... −40 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 2 W
Continuous total dissipation at (or below) 90°C case temperature (see Note 1) ..... 15 W
Operating free-air, case, or virtual junction temperature range: LM237 ..... −25°C to 150°C
LM337 ..... 0°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: For operation above 25°C operating free-air or 90°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

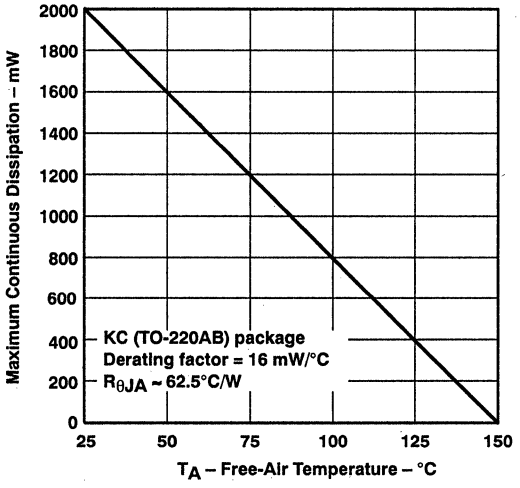


Figure 1

CASE TEMPERATURE DISSIPATION DERATING CURVE

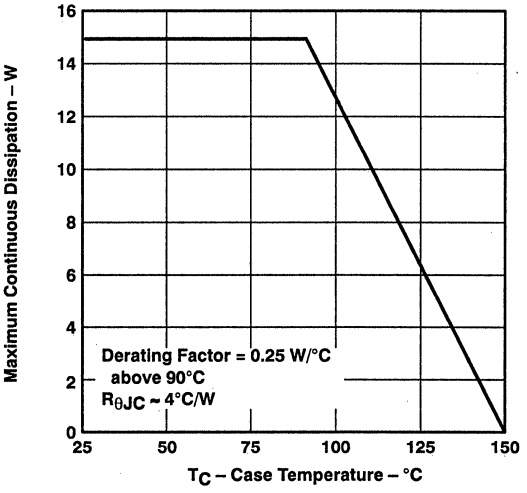


Figure 2

recommended operating conditions

		LM237		LM337		UNIT
		MIN	MAX	MIN	MAX	
Output current, I_O	$\lvert V_I - V_O \rvert \le 40$ V, $P \le 15$ W	10	1500	10	1500	mA
	$\lvert V_I - V_O \rvert \le 10$ V, $P \le 15$ W	6	1500	6	1500	
Operating virtual junction temperature, T_J		−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

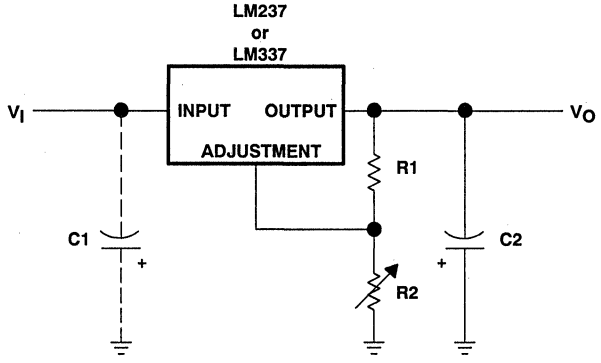
PARAMETER	TEST CONDITIONS†		LM237			LM337			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation‡	$V_I - V_O = -3$ V to −40 V	$T_J = 25°C$		0.01	0.02		0.01	0.04	%/V
		T_J = MIN to MAX		0.02	0.05		0.02	0.07	
Ripple rejection	$V_O = -10$ V,	f = 120 Hz		60			60		dB
	$V_O = -10$ V, $C_{ADJ} = 10\ \mu F$	f = 120 Hz	66	77		66	77		
Output regulation	I_O = 10 mA to 1.5 A, $T_J = 25°C$	$\lvert V_O \rvert \le 5$ V			25			50	mV
		$\lvert V_O \rvert \ge 5$ V		0.3%	0.5%		0.3%	1%	
	I_O = 10 mA to 1.5 A	$\lvert V_O \rvert \le 5$ V			50			70	mV
		$\lvert V_O \rvert \ge 5$ V			1%			1.5%	
Output voltage change with temperature	T_J = MIN to MAX			0.6%			0.6%		
Output voltage long-term drift (see Note 2)	After 1000 h at T_J = MAX and $V_I - V_O = -40$ V			0.3%	1%		0.3%	1%	
Output noise voltage	f = 10 Hz to 10 kHz,	$T_J = 25°C$		0.003%			0.003%		
Minimum output current to maintain regulation	$\lvert V_I - V_O \rvert \le 40$ V			2.5	5		2.5	10	mA
	$\lvert V_I - V_O \rvert \le 10$ V			1.2	3		1.5	6	
Peak output current	$\lvert V_I - V_O \rvert \le 15$ V		1.5	2.2		1.5	2.2		A
	$\lvert V_I - V_O \rvert \le 40$ V,	$T_J = 25°C$	0.24	0.4		0.15	0.4		
Adjustment-terminal current				65	100		65	100	μA
Change in adjustment-terminal current	$V_I - V_O = -2.5$ V to −40 V, I_O = 10 mA to MAX	$T_J = 25°C$,		2	5		2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O = -3$ V to −40 V, I_O = 10 mA to 1.5 A, $P \le$ rated dissipation	$T_J = 25°C$	−1.225	−1.250	−1.275	−1.213	−1.25	−1.287	V
		T_J = MIN to MAX	−1.2	−1.25	−1.3	−1.2	−1.25	−1.3	
Thermal regulation	Initial $T_J = 25°C$,	10-ms pulse		0.002	0.02		0.003	0.04	%/W

† Unless otherwise noted, these specifications apply for the following test conditions $\lvert V_I - V_O \rvert = 5$ V and $I_O = 0.5$ A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTE 2: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

APPLICATION INFORMATION



R1 is typically 120 Ω.

$$R2 = R1\left(\frac{-V_O}{-1.25} - 1\right)$$ where V_O is the output in volts.

C1 is a 1-μF solid tantalum capacitor required only if the regulator is more than 10 cm (4 in.) from the power supply filter capacitor.
C2 is a 1-μF solid tantalum or 10-μF aluminum electrolytic capacitor required for stability.

Figure 3. Adjustable Negative-Voltage Regulator

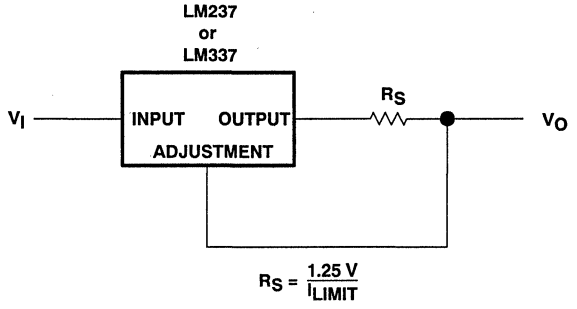
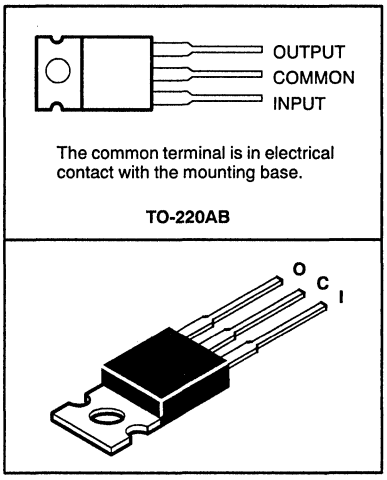


Figure 4. Current-Limiting Circuit

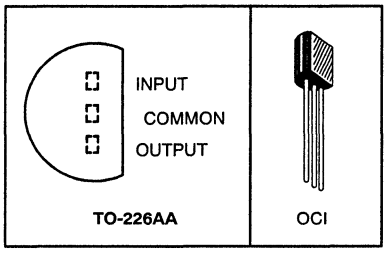
D2733, APRIL 1983–REVISED AUGUST 1991

- **Input-Output Differential Less Than 0.6 V**
- **Output Current of 150 mA**
- **Reverse Battery Protection**
- **Line Transient Protection**
- **40-V Load-Dump Protection**
- **Internal Short Circuit Current Limiting**
- **Internal Thermal Overload Protection**
- **Mirror-Image Insertion Protection**
- **Direct Replacement for National LM2930 Series**

KC PACKAGE
(TOP VIEW)



LP
SILECT PACKAGE
(TOP VIEW)



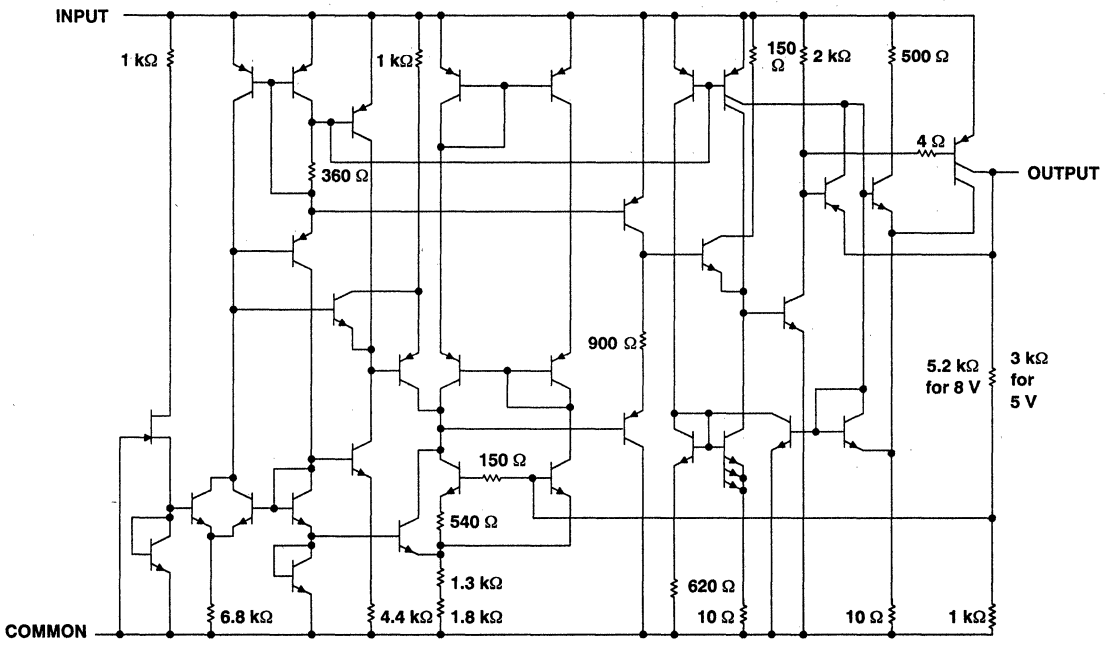
description

The LM2930-5 and LM2930-8 are 3-terminal positive regulators that provide fixed 5-V and 8-V regulated outputs. Each features the ability to source 150 mA of output current with an input-output differential of 0.6 V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

The LM2930 series has low voltage dropout, making it useful for certain battery applications. For example, the low voltage dropout feature allows a longer battery discharge before the output falls out of regulation; the battery supplying the regulator input voltage may discharge to 5.6 V and still properly regulate the system and load voltage. Supporting this feature, the LM2930 series protects both itself and the regulated system from reverse battery installation or 2-battery jumps.

Other protection features include line transient protection for load dump of up to 40 V. In this case, the regulator shuts down to avoid damaging internal and external circuits. The LM2930 series regulator cannot be harmed by temporary mirror-image insertion.

schematic diagram



All component values are nominal.

absolute maximum ratings over operating free-air temperature ranges (unless otherwise noted)

Continuous input voltage ..... 26 V
Transient input voltage: t = 1 s ..... 40 V
Continuous reverse input voltage ..... −6 V
Transient reverse input voltage: t = 100 ms ..... −12 V
Continuous total dissipation (see Note 1) ..... See Dissipation Rating Tables 1 and 2
Operating free-air, case, or virtual junction temperature ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
KC	2000 mW	16 mW/°C	25°C	1280 mW
LP	775 mW	6.2 mW/°C	25°C	496 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
KC	20 W	0.25 W/°C	70°C	6.25 W
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
I_O	Output current		150	mA
T_J	Operating virtual junction temperature	−40	125	°C

LM2930-5 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	4.5	5	5.5	V
Input regulation	I_O = 5 mA	V_I = 9 V to 16 V		7	25	mV
		V_I = 6 V to 26 V		30	80	
Ripple rejection	f = 120 Hz			56		dB
Output regulation	I_O = 5 mA to 150 mA			14	50	mV
Output voltage long-term drift‡	After 1000 hours at T_J = 125°C			20		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			60		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		5.5	V
Output impedance	I_O = 100 mA, I_O = 10 mA (rms), 100 Hz to 10 kHz			200		mΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor across the output.

‡ Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is intended to be an engineering estimate of the average drift to be expected from lot to lot.

LM2930-8 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 150 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, T_J = −40°C to 125°C	I_O = 5 mA to 150 mA,	7.2	8	8.8	V
Input regulation	I_O = 5 mA	V_I = 9.4 V to 16 V		12	50	mV
		V_I = 9.4 V to 26 V		50	100	
Ripple rejection	f = 120 Hz			52		dB
Output regulation	I_O = 5 mA to 150 mA			25	50	mV
Output voltage long-term drift‡	After 1000 h at T_J = 125°C			30		mV
Dropout voltage	I_O = 150 mA			0.32	0.6	V
Output noise voltage	f = 10 Hz to 100 kHz			90		μV
Output voltage during line transients	V_I = −12 V to 40 V,	R_L = 100 Ω	−0.3		8.8	V
Output impedance	I_O = 100 mA, I_O = 10 mA (rms), f = 100 Hz to 10 kHz			300		mΩ
Bias current	I_O = 10 mA			4	7	mA
	I_O = 150 mA			18	40	
Peak output current			150	300	700	mA

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor across the output.

‡ Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is intended to be an engineering estimate of the average drift to be expected from lot to lot.

TYPICAL CHARACTERISTICS

table of graphs

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Bias Current vs Input Voltage	16

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

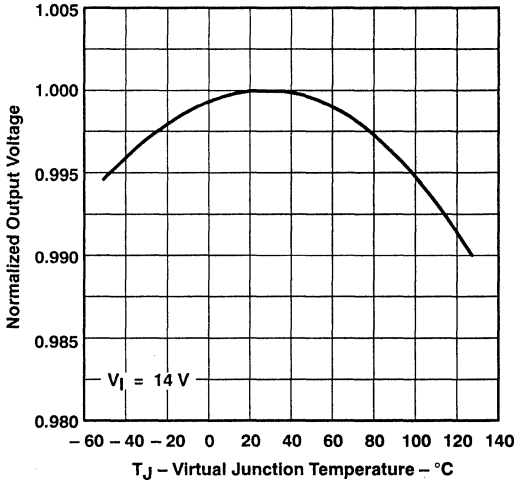

Figure 1

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

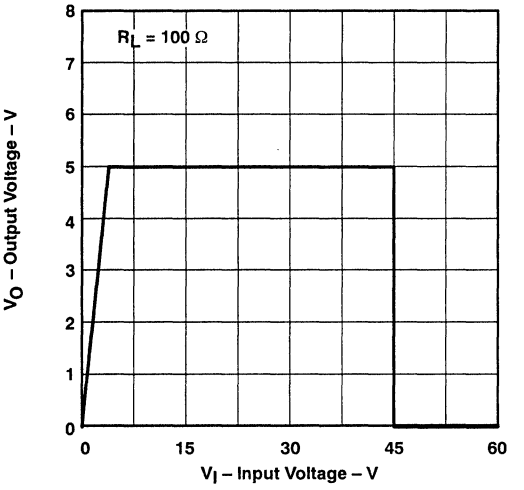

Figure 2

LM2930-5
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

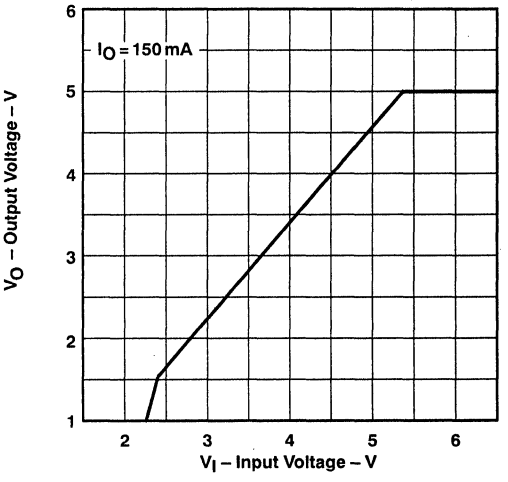

Figure 3

RIPPLE REJECTION
vs
FREQUENCY

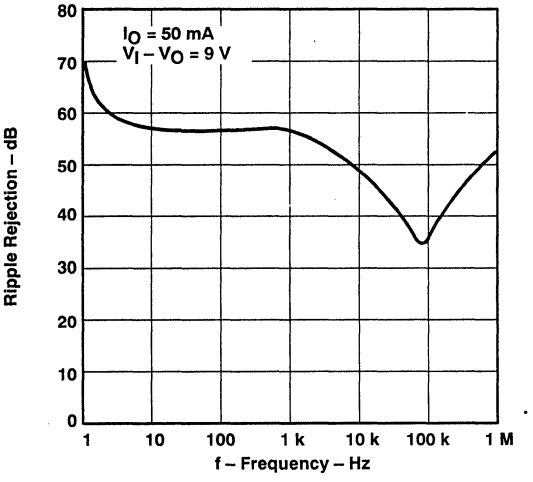

Figure 4

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
OUTPUT CURRENT

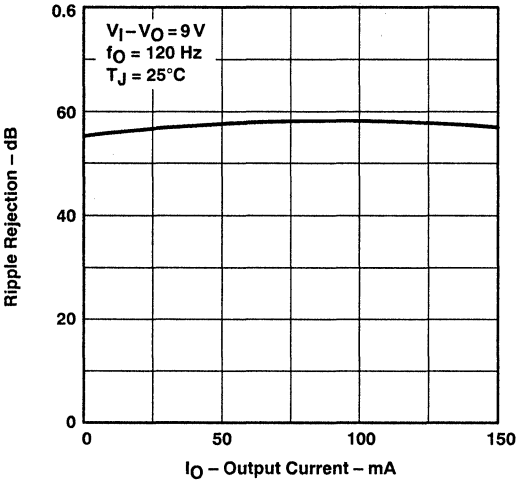

Figure 5

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

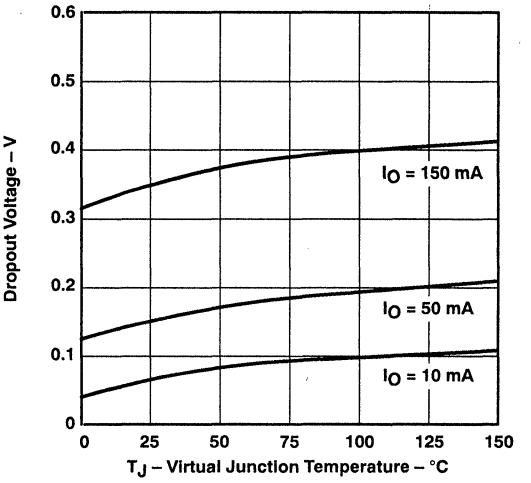

Figure 6

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

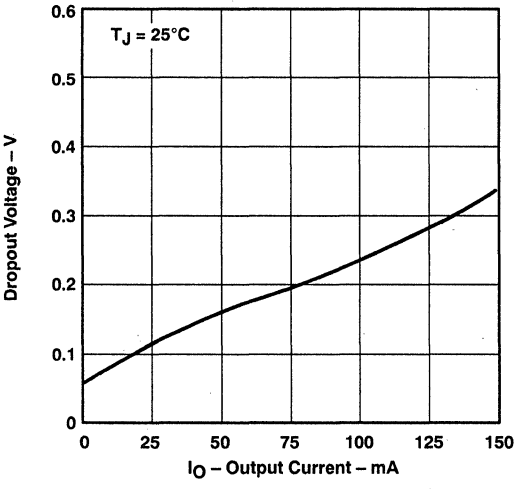

Figure 7

OUTPUT IMPEDANCE
vs
FREQUENCY

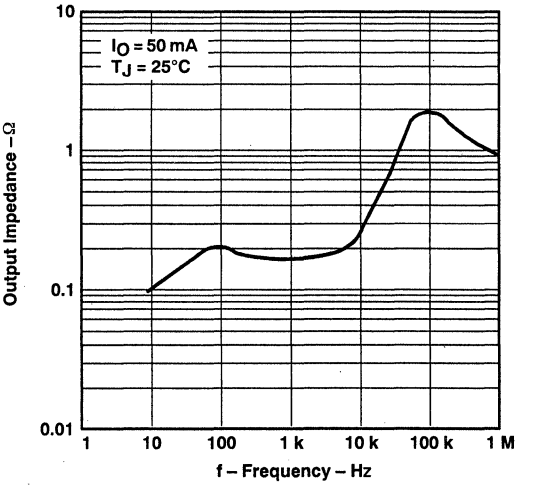

Figure 8

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TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

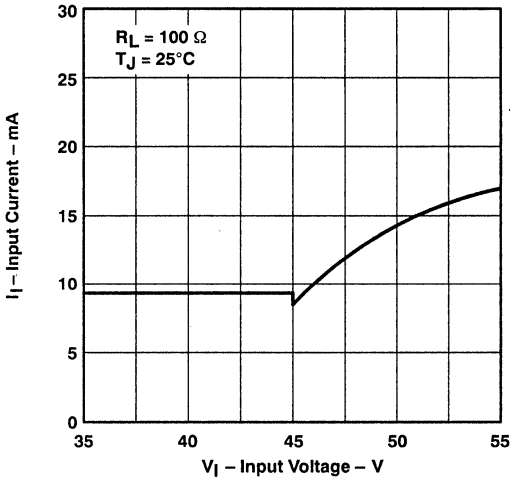


Figure 9

LINE TRANSIENT RESPONSE

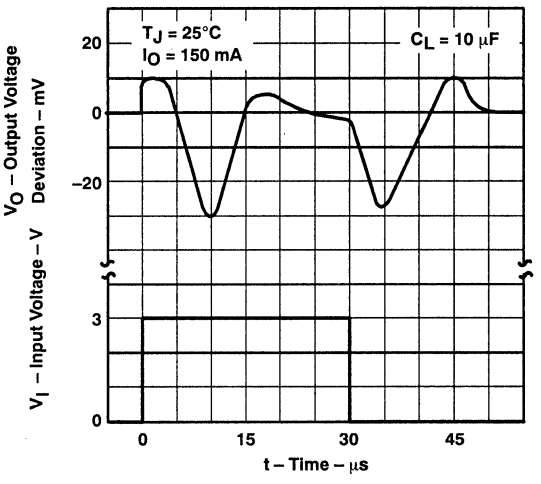


Figure 10

INPUT CURRENT vs REVERSE INPUT VOLTAGE

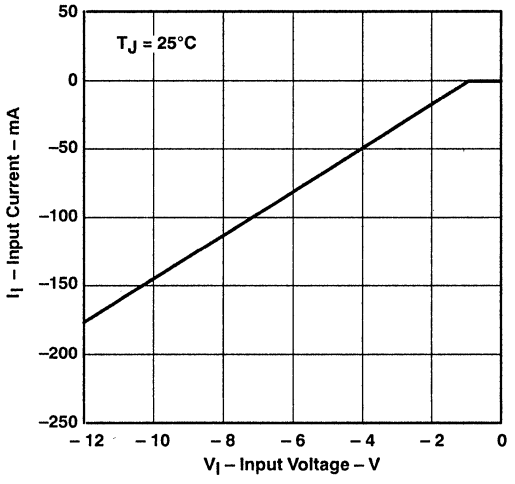


Figure 11

OUTPUT VOLTAGE vs REVERSE INPUT VOLTAGE

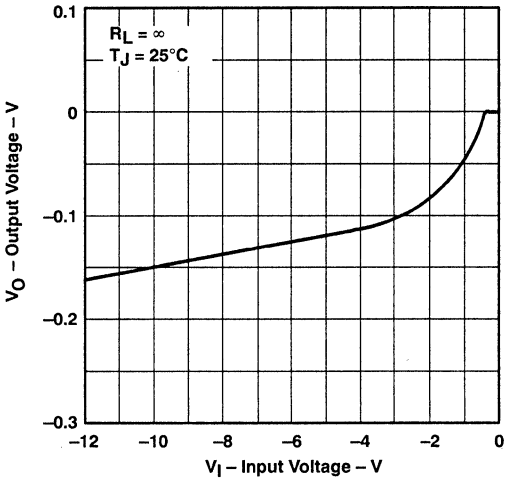


Figure 12

TYPICAL CHARACTERISTICS

LOAD TRANSIENT RESPONSE

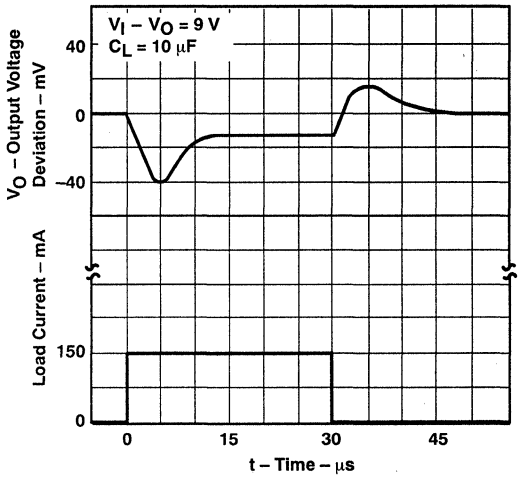


Figure 13

BIAS CURRENT
vs
OUTPUT CURRENT

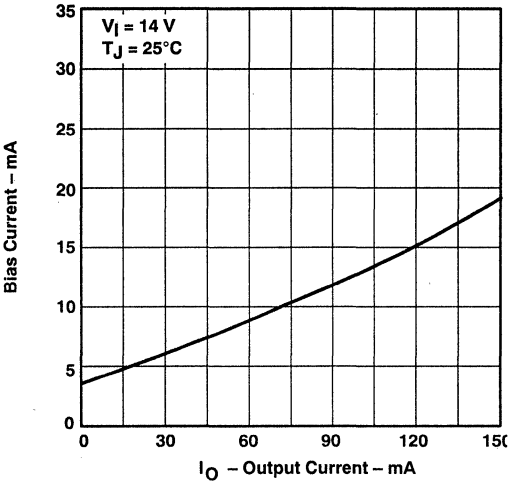


Figure 14

BIAS CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

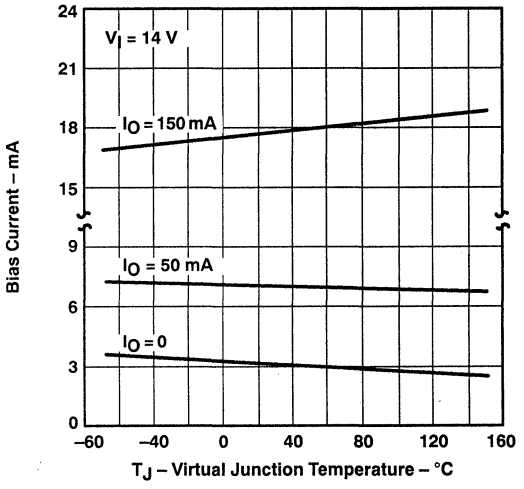


Figure 15

LM2930-5
BIAS CURRENT
vs
INPUT VOLTAGE

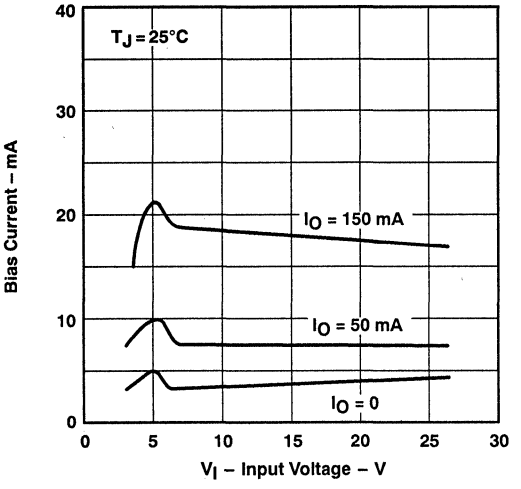
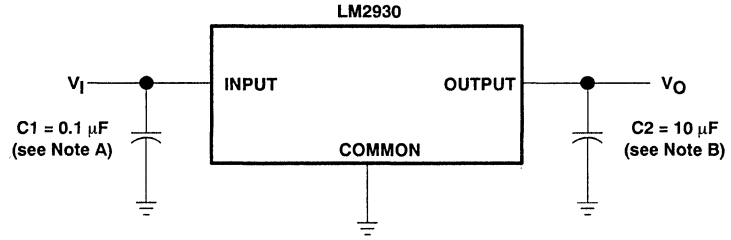


Figure 16

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION



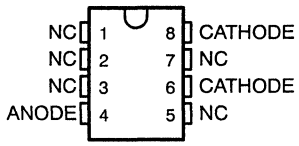
NOTES: A. Use of C1 is required if the regulator is not located in close proximity to the supply filter.
B. Capacitor C2 must be located as close as possible to the regulator and may be an aluminum or tantalum-type capacitor. The minimum value required for stability is 10 μF. The capacitor must be rated for operation at −40°C to guarantee stability to that extreme.

Figure 17

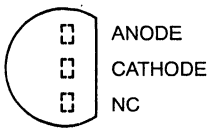
D3190, JANUARY 1989–REVISED JULY 1991

- **Initial Accuracy**
  - **±4 mV for LT1004-1.2**
  - **±20 mV for LT1004-2.5**
- **Micropower Operation**
- **Operates Up to 20 mA**
- **Very Low Reference Impedance**
- **Applications:**
  - **Portable Meter Reference**
  - **Portable Test Instruments**
  - **Battery-Operated Systems**
  - **Current-Loop Instrumentation**

LT1004C . . . D PACKAGE
(TOP VIEW)



LT1004C . . . LP PACKAGE
(TOP VIEW)

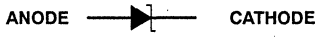


NC–No internal connection

description

The LT1004 micropower voltage reference is a 2-terminal band-gap reference diode designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimizing the key parameters in the design, processing and testing of the device results in specifications previously attainable only with selected units.

symbol



The LT1004 is a pin-for-pin replacement for the LM185 series of references with improved specifications. The LT1004 is an attractive device for use in systems in which accuracy was previously attained at the expense of power consumption and trimming.

The LT1004C is characterized for operation from 0°C to 70°C. The LT1004M is characterized for operation over the full military temperature range of −55°C to 125°C.

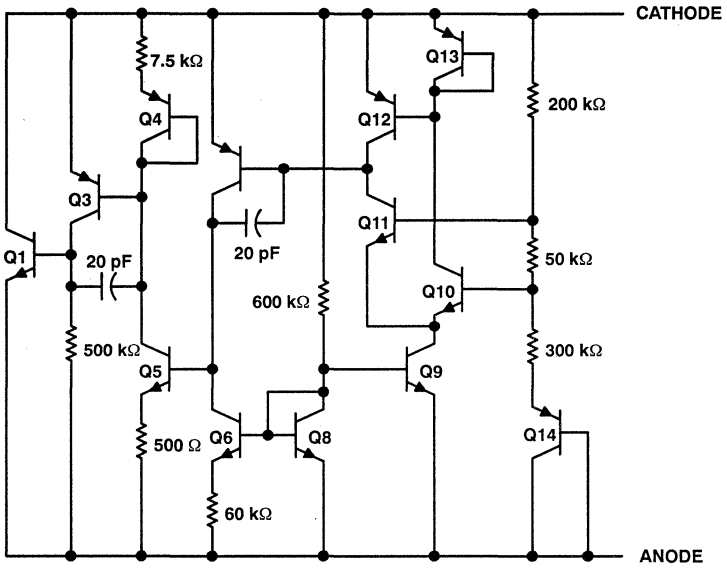
AVAILABLE OPTIONS

T_A	NOM V_Z	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC (LP)
0°C to 70°C	1.2 V	LT1004CD-1.2	LT1004CLP-1.2
	2.5 V	LT1004CD-2.5	LT1004CLP-2.5
−55°C to 125°C	1.2 V	LT1004MD-1.2	LT1004MLP-1.2
	2.5 V	LT1004MD-2.5	LT1004MLP-2.5

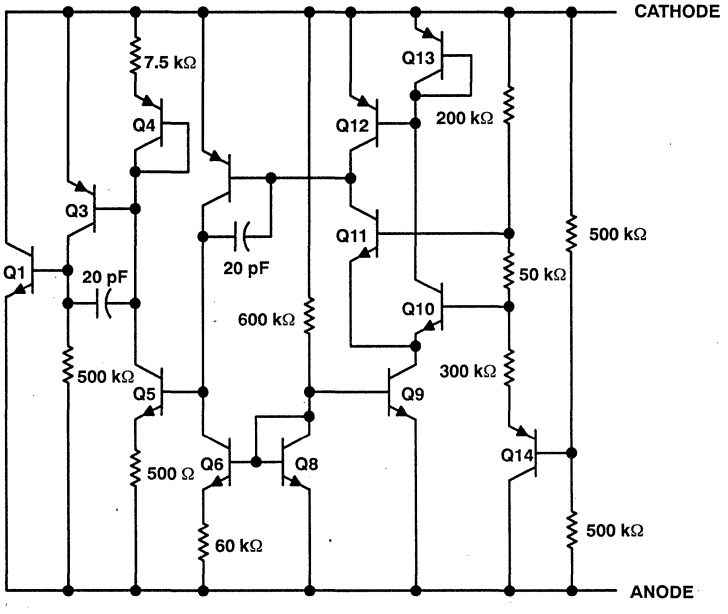
The D and LP packages are available taped and reeled. Add suffix R to the device type (i.e., LT1004CDR).

schematic

LT1004-1.2



LT1004-2.5



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Reverse current, I_R ..... 30 mA
Forward current, I_F ..... 10 mA
Operating free-air temperature range: LT1004C ..... 0°C to 70°C
LT1004M ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†		LT1004-1.2			LT1004-2.5			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 100 μA	25°C		1.231	1.235	1.239	2.48	2.5	2.52	V
			Full range	LT1004C	1.225		1.245	2.47		2.53	
				LT1004M	1.22		1.245	2.46		2.535	
α_{VZ}	Average temperature coefficient of reference voltage‡	I_Z = 10 μA	25°C			20					ppm/°C
		I_Z = 20 μA							20		
ΔV_Z	Change in reference voltage with current	$I_Z = I_{Z(min)}$ to 1 mA	25°C				1			1	mV
			Full range				1.5			1.5	
		I_Z = 1 mA to 20 mA	25°C				10			10	
			Full range				20			20	
$\Delta V_Z/\Delta_t$	Long-term change in reference voltage	I_Z = 100 μA	25°C			20			20		ppm/khr
$I_{Z(min)}$	Minimum reference current		Full range			8	10		12	20	μA
Z_Z	Reference impedance	I_Z = 100 μA	25°C			0.2	0.6		0.2	0.6	Ω
			Full range				1.5			1.5	
V_n	Broadband noise voltage	I_Z = 100 μA, f = 10 Hz to 10 kHz	25°C			60			120		μV

† Full range is 0°C to 70°C for the LT1004C and −55°C to 125°C for the LT1004M.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REVERSE CURRENT
vs
REVERSE VOLTAGE

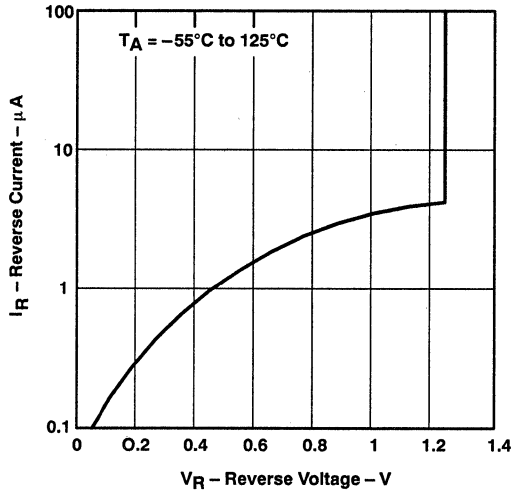


Figure 1

REFERENCE VOLTAGE CHANGE
vs
REVERSE CURRENT

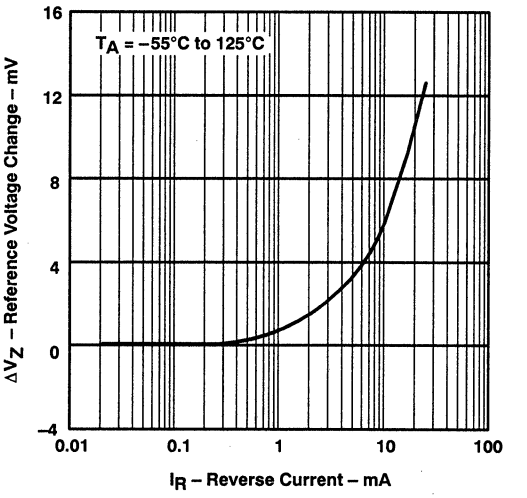


Figure 2

FORWARD VOLTAGE
vs
FORWARD CURRENT

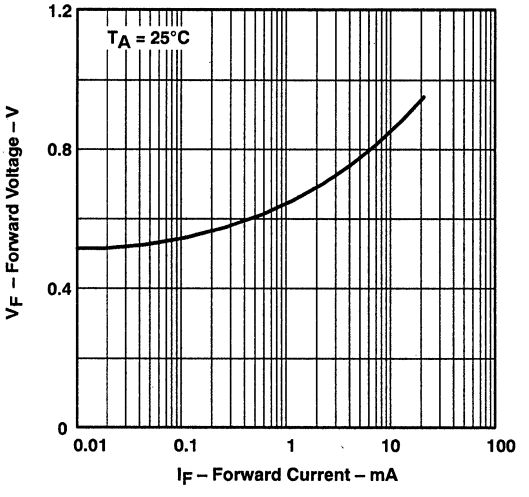


Figure 3

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

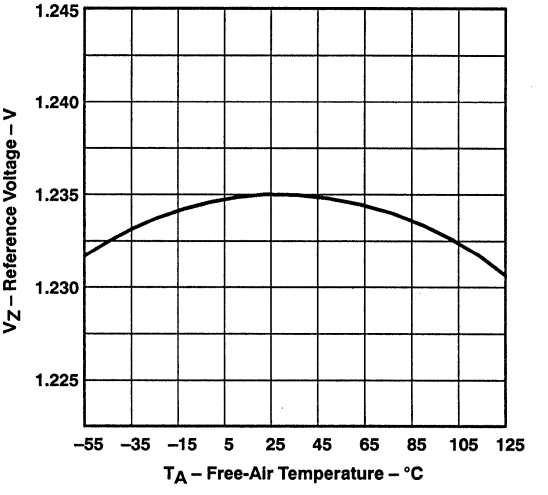


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

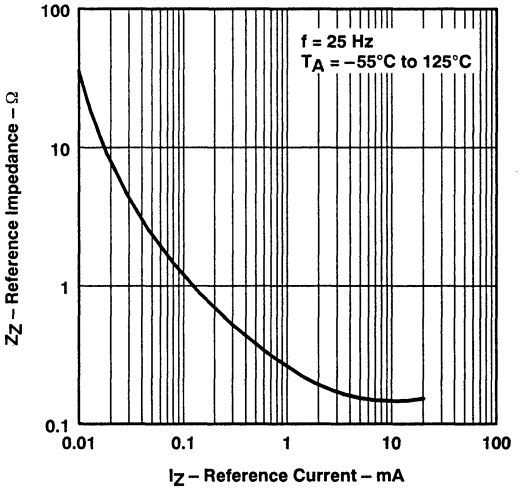


Figure 5

NOISE VOLTAGE
vs
FREQUENCY

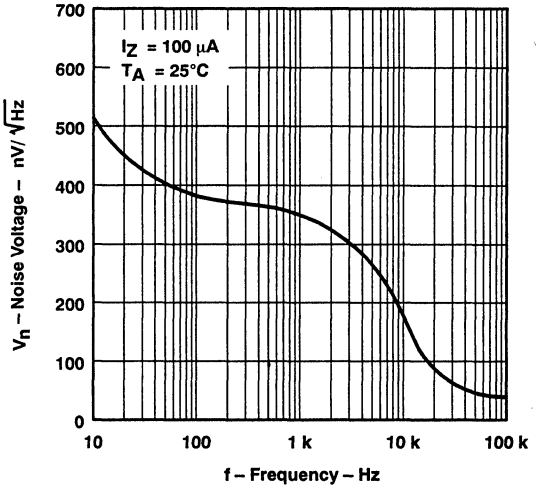


Figure 6

OUTPUT NOISE VOLTAGE
vs
CUTOFF FREQUENCY

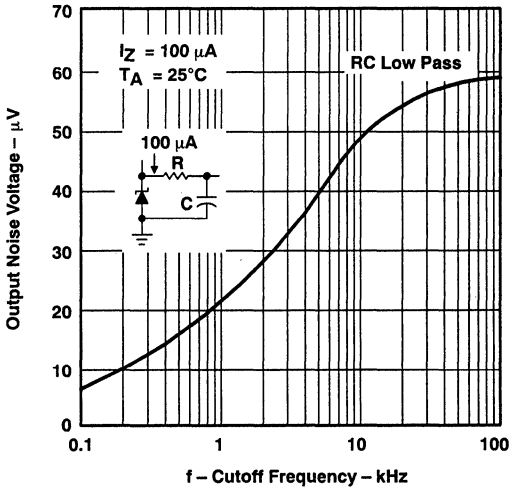


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REVERSE CURRENT
vs
REVERSE VOLTAGE

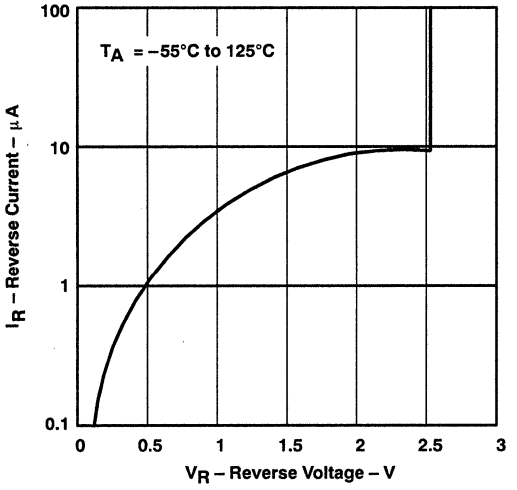


Figure 8

FORWARD VOLTAGE
vs
FORWARD CURRENT

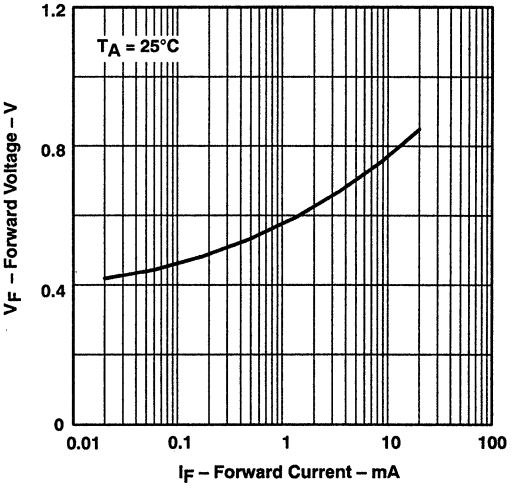


Figure 9

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

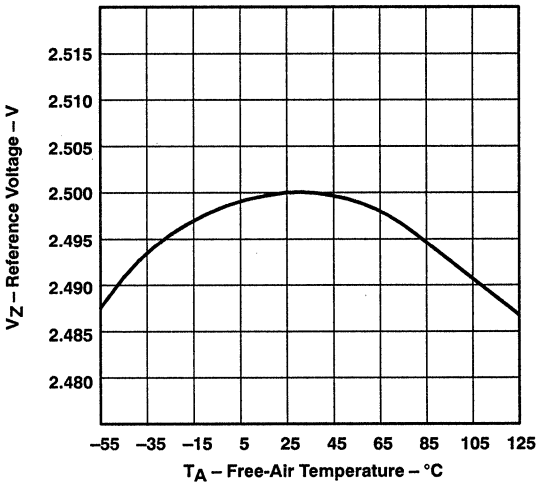


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

REFERENCE IMPEDANCE
vs
REFERENCE CURRENT

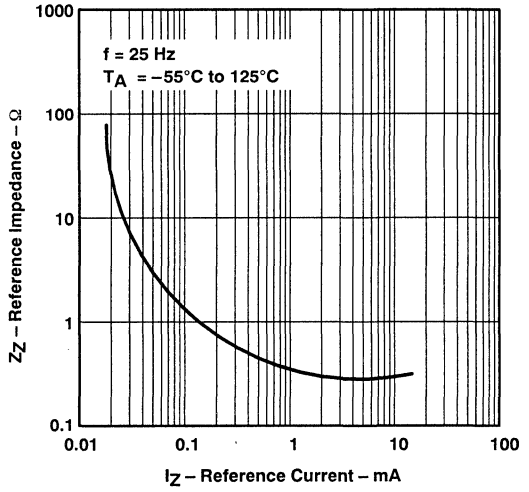


Figure 11

NOISE VOLTAGE
vs
FREQUENCY

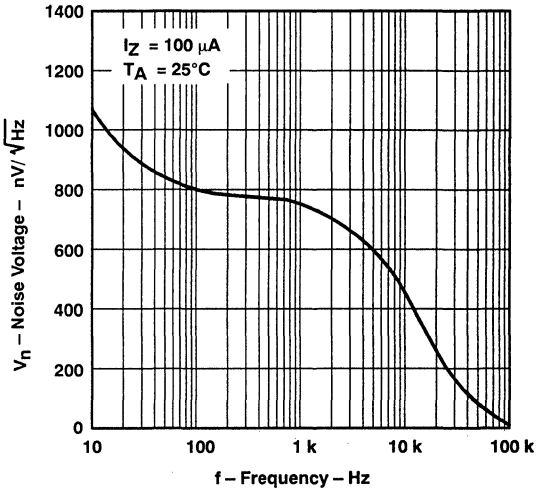


Figure 12

FILTERED OUTPUT NOISE VOLTAGE
vs
OUTPUT FREQUENCY

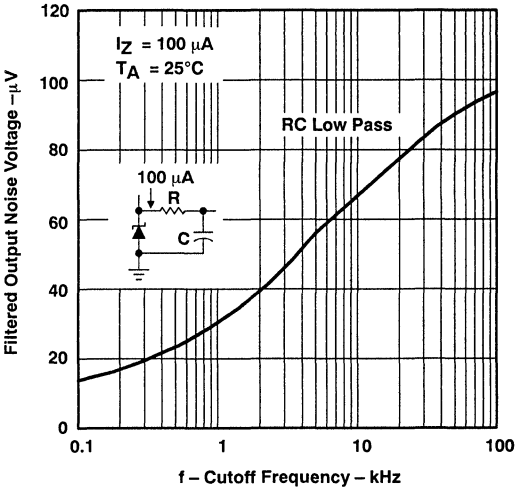


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LT1004-1.2
TRANSIENT RESPONSE

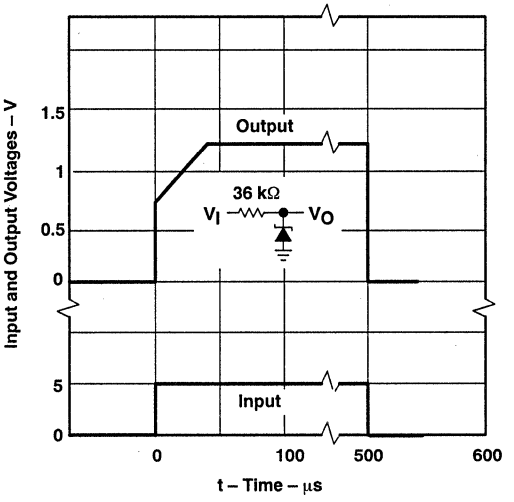


Figure 14

LT1004-2.5
TRANSIENT RESPONSE

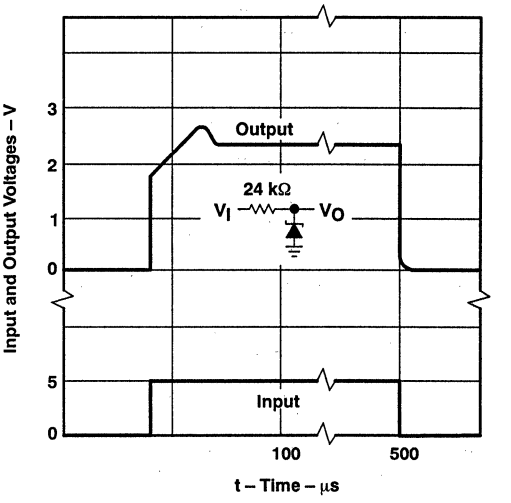
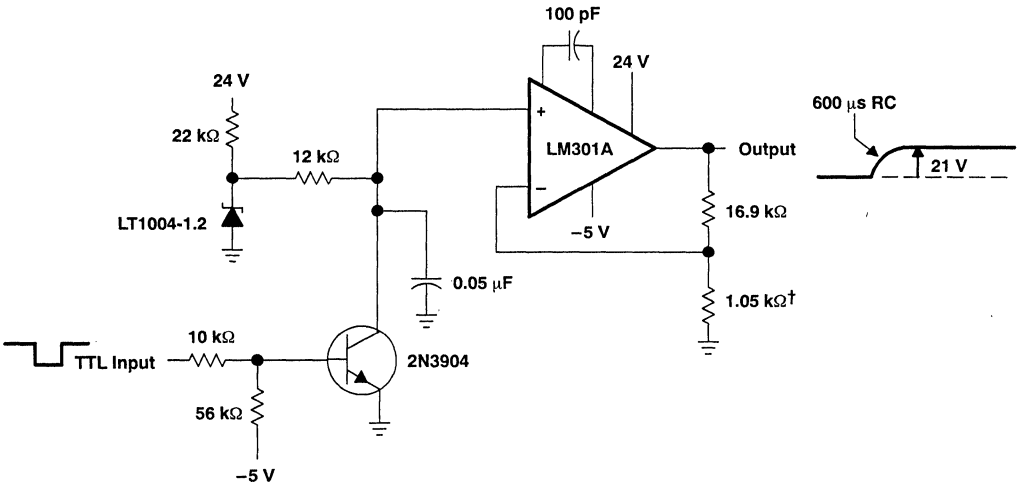


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



† 1% metal film resistors

Figure 16. V_{PP} Generator for EPROMs (no trim required)

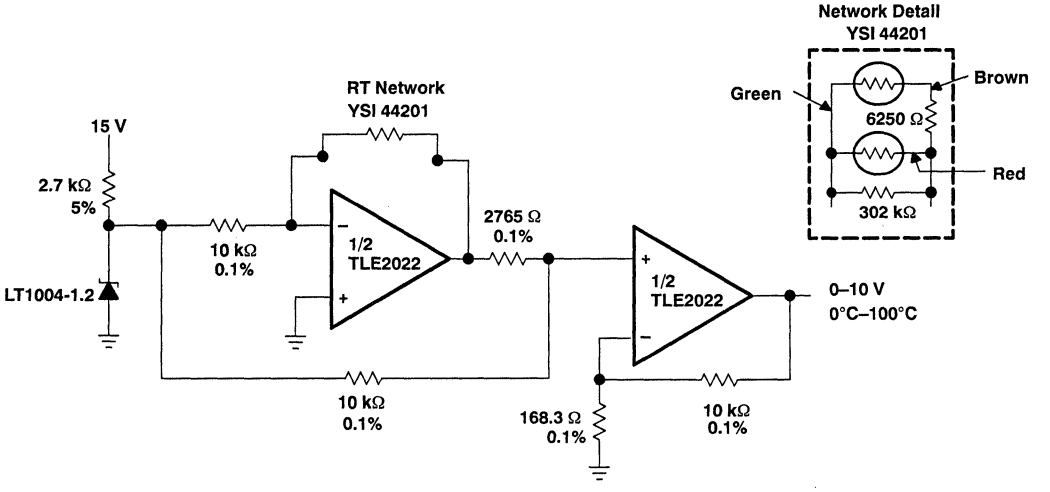


Figure 17. 0°C to 100°C Linear Output Thermometer

APPLICATION INFORMATION

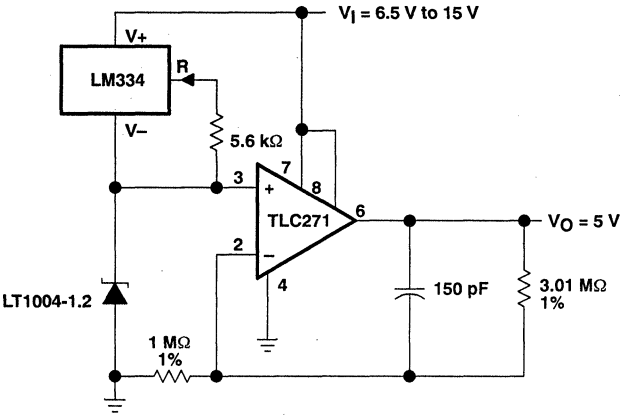


Figure 18. Micropower 5-V Reference

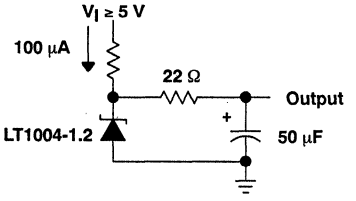


Figure 19. Low-Noise Reference

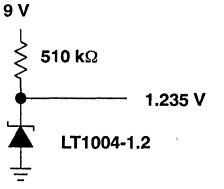
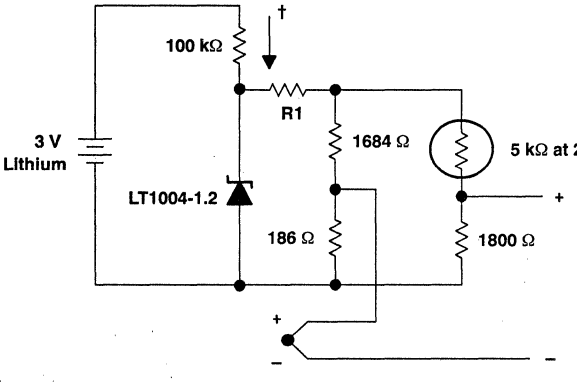


Figure 20. Micropower Reference From 9-V Battery



Thermocouple Type	R1
J	233 kΩ
K	299 kΩ
T	300 kΩ
S	2.1 MΩ

† Quiescent current ≈ 15 μA
‡ Yellow Springs Inst. Co., Part #44007
NOTE: This application compensates within ±1°C from 0°C to 60°C.

Figure 21. Micropower Cold-Junction Compensation for Thermocouples

APPLICATION INFORMATION

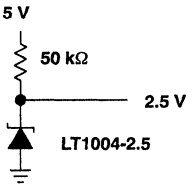


Figure 22. 2.5-V Reference

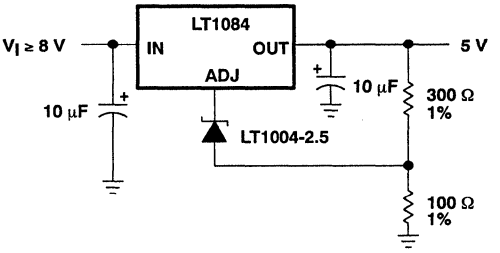
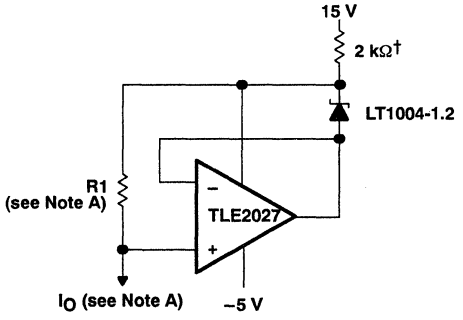


Figure 23. High-Stability 5-V Regulator



† May be increased for small output currents.

NOTE A: $R1 \approx \frac{2\ V}{I_O + 10\ \mu A}$, $I_O = \frac{1.235\ V}{R1}$.

Figure 24. Ground-Referenced Current Source

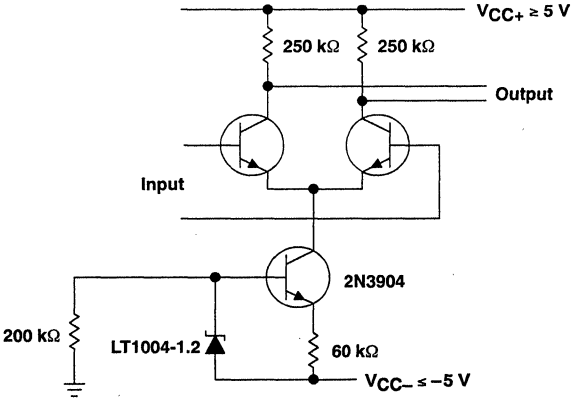
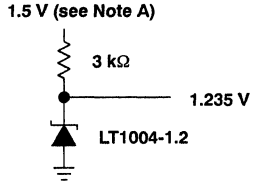


Figure 25. Amplifier With Constant Gain Over Temperature



NOTE A: Output regulates down to 1.285 V for $I_O = 0$.

Figure 26. 1.2-V Reference From 1.5-V Battery

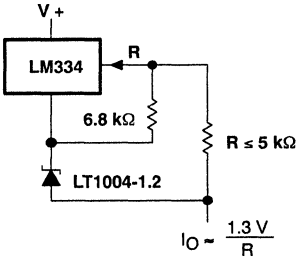
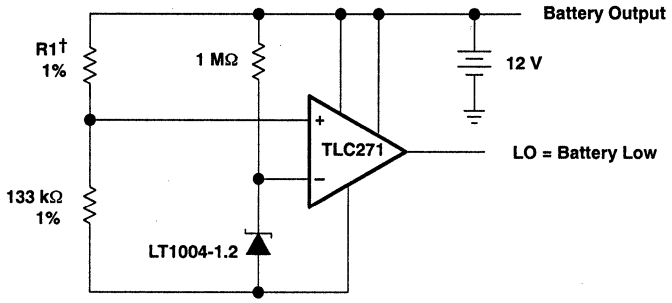


Figure 27. Terminal Current Source With Low Temperature Coefficient

APPLICATION INFORMATION



†R1 sets trip point, 60.4 kΩ per cell for 1.8 V per cell.

Figure 28. Lead-Acid Low-Battery-Voltage Detector

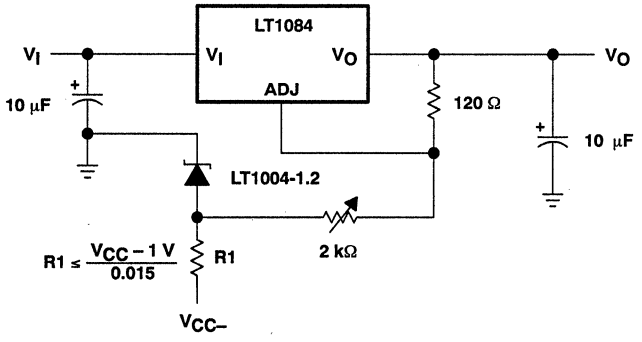


Figure 29. Variable-Voltage Supply

D3191, MAY 1987–REVISED AUGUST 1991

- **Excellent Temperature Stability**
- **Initial Tolerance . . . 0.2% Max**
- **Dynamic Impedance . . . 0.6 Ω Max**
- **Wide Operating Current Range**
- **Directly Interchangeable With LM136**
- **Needs No Adjustment for Minimum Temperature Coefficient**

description

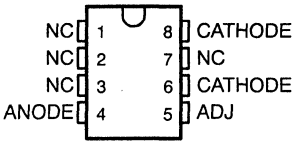
The LT1009 is a precision trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. A maximum initial tolerance of ±5 mV is available in the FK, JG, or LP package and ±10 mV in the D package. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient α_{VZ}.

Even though the LT1009 needs no adjustments, a third terminal allows the reference voltage to be adjusted ±5% to eliminate system errors. In many applications, the LT1009 can be used as a pin-for-pin replacement for the LM136-2.5, which eliminates the external trim network.

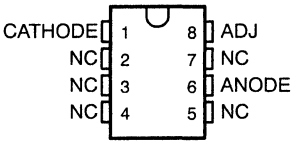
The uses of the LT1009 include a 5-V system reference, an 8-bit ADC and DAC reference, or a power supply monitor. The LT1009 can also be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from −40°C to 85°C. The LT1009M is characterized for operation over the full military temperature range of −55°C to 125°C.

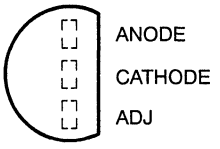
LT1009C, LT1009I . . . D PACKAGE
(TOP VIEW)



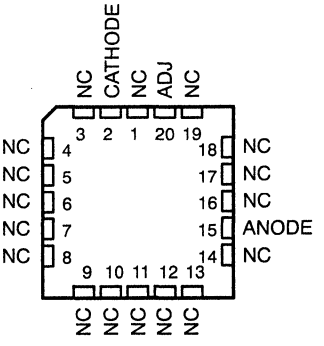
LT1009M . . . JG PACKAGE
(TOP VIEW)



LT1009C, LT1009I . . . LP PACKAGE
(TOP VIEW)

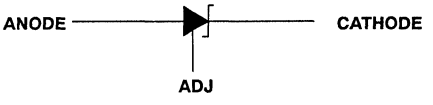


FK PACKAGE
(TOP VIEW)

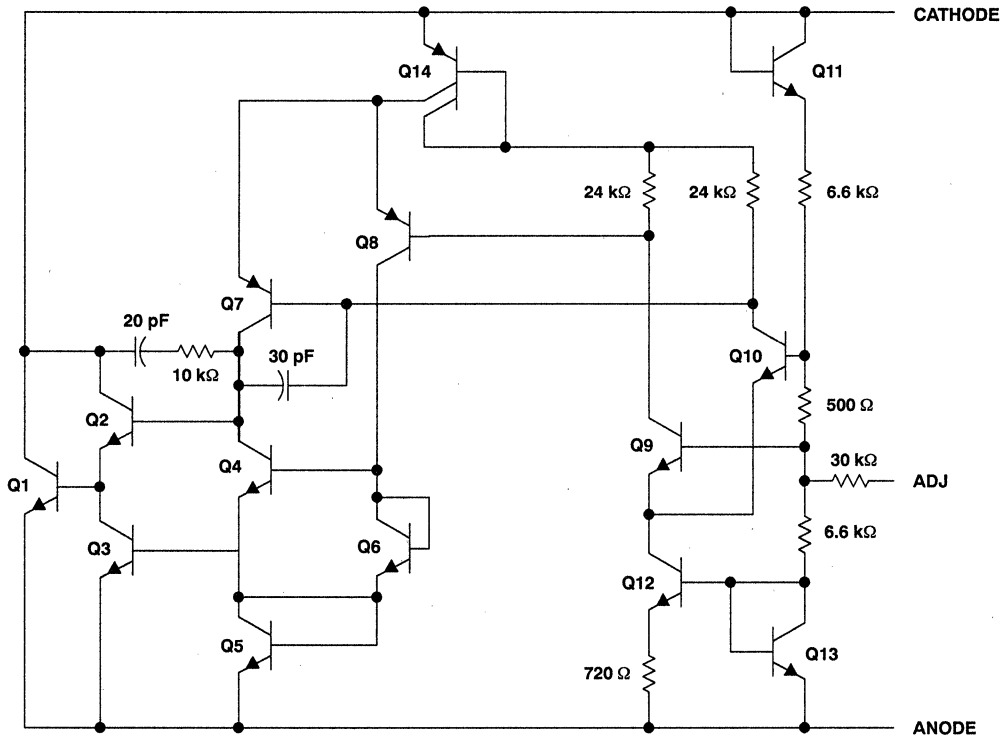


NC–No internal connection

symbol



schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range

Reverse current		20 mA
Forward current		10 mA
Operating free-air temperature range:	LT1009C	0°C to 70°C
	LT1009I	−40°C to 85°C
	LT1009M	−55°C to 125°C
Storage temperature range		−65°C to 150°C
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and LP package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package		300°C

DISSIPATION RATING TABLE

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	5.8 mW/°C	725 mW	464 mW	377 mW	145 mW
FK	11.0 mW/°C	1375 mW	880 mW	715 mW	275 mW
JG	8.4 mW/°C	1050 mW	672 mW	546 mW	210 mW
LP	6.2 mW/°C	775 mW	496 mW	403 mW	155 mW

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A†	LT1009C			LT1009I			LT1009M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reference voltage	I_Z = 1 mA	FK, JG, LP package	25°C	2.495	2.5	2.505	2.495	2.5	2.505	2.495	2.5	2.505	V
			D package		2.49	2.5	2.51	2.49	2.5	2.51				
			FK, JG, LP package	Full range	2.491		2.509	2.480		2.520	2.460		2.535	
			D package		2.486		2.514	2.475		2.525				
V_F	Forward voltage	I_F = 2 mA		25°C	0.4		1	0.4		1	0.4		1	V
	Adjustment range	I_Z = 1 mA, V_{ADJ} = GND to V_Z		25°C	125			125						mV
		I_Z = 1 mA, V_{ADJ} = 0.6 V to V_Z –0.6 V			45			45			15			
$\Delta V_{Z(temp)}$	Change in reference voltage with temperature		FK, JG, LP package	Full range			4			15			15*	mV
			D package				5			15				
α_{VZ}	Average temperature coefficient of reference voltage‡			0°C to 70°C		15	25							ppm/°C
				–40°C to 85°C					20					
				–55°C to 125°C								25	35	
ΔV_Z	Change in reference voltage with current	I_Z = 400 μA to 10 mA		25°C		2.6	10		2.6	6		2.6	6	mV
				Full range			12			10			10	
$\Delta V_Z/\Delta t$	Long-term change in reference voltage	I_Z = 1 mA		25°C		20			20			20		ppm/khr
Z_Z	Reference impedance	I_Z = 1 mA		25°C		0.3	1		0.3	1		0.3	0.6*	Ω
				Full range			1.4			1.4			1*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is 0°C to 70°C for the LT1009C, –40°C to 85°C for the LT1009I, and –55°C to 125°C for the LT1009M.
‡ The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.

TYPICAL CHARACTERISTICS†

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

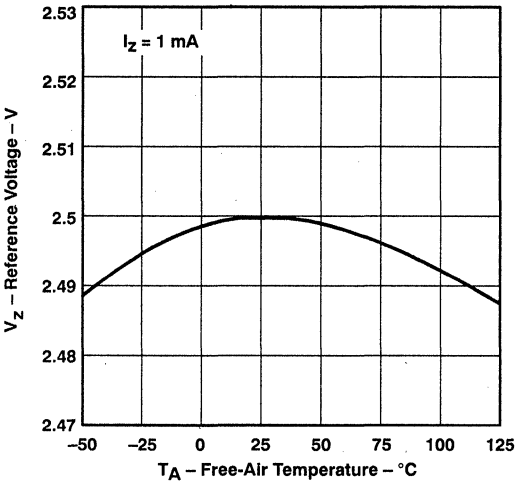


Figure 1

CHANGE IN REFERENCE VOLTAGE
vs
REFERENCE CURRENT

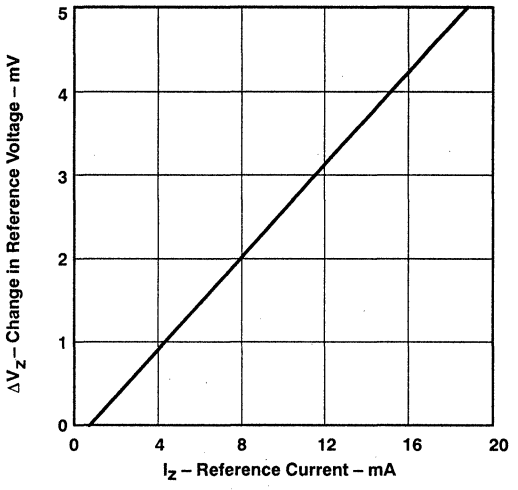


Figure 2

REVERSE CHARACTERISTICS

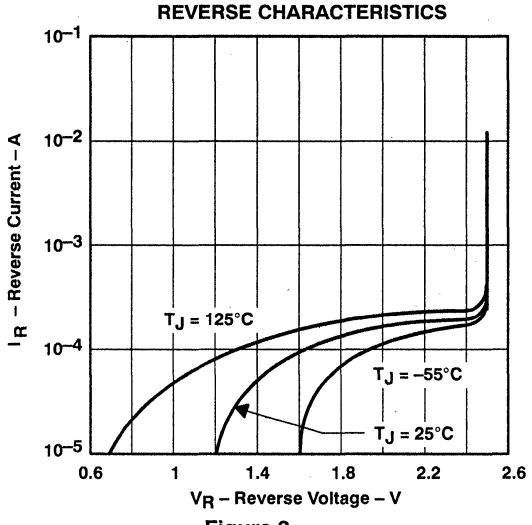


Figure 3

FORWARD CHARACTERISTICS

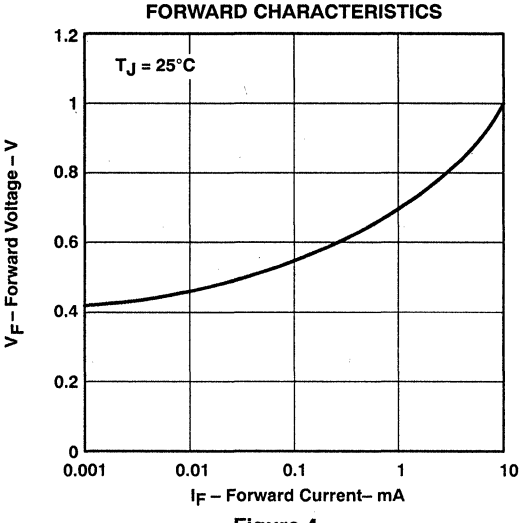


Figure 4

† Data at the high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

REFERENCE IMPEDANCE
vs
FREQUENCY

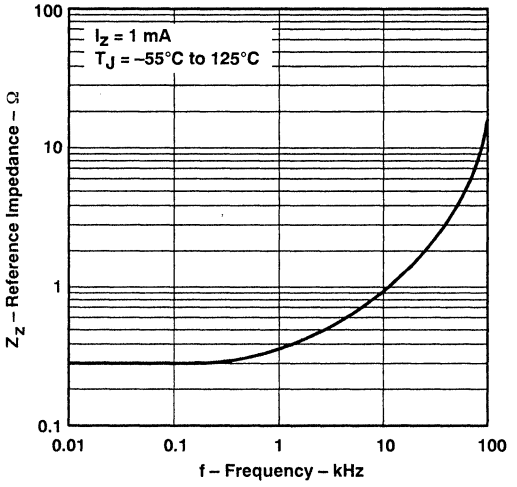


Figure 5

NOISE VOLTAGE
vs
FREQUENCY

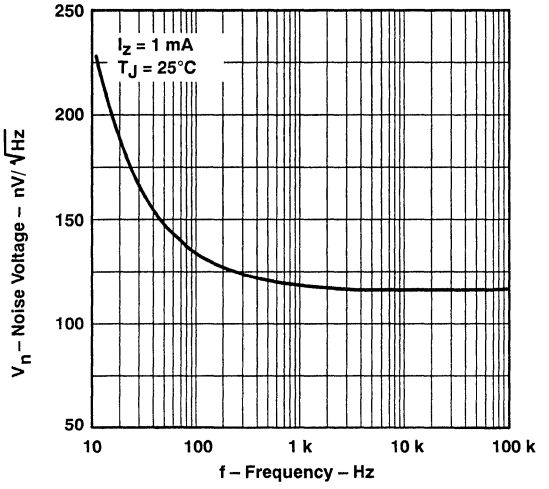


Figure 6

TRANSIENT RESPONSE

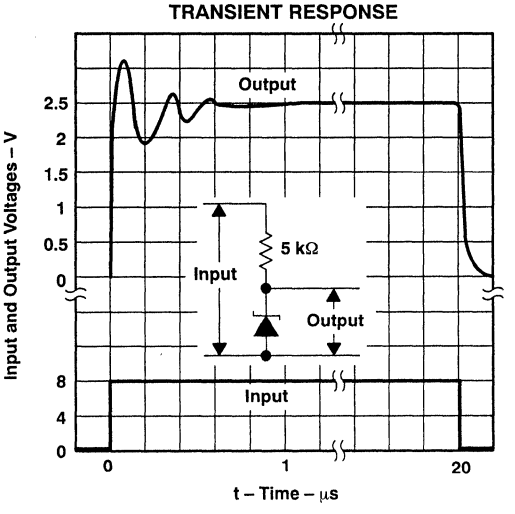
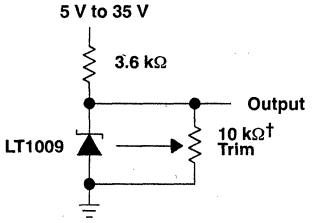


Figure 7

APPLICATION INFORMATION



†Does not affect temperature coefficient. Provides ±5% trim range.

Figure 8. 2.5-V Reference

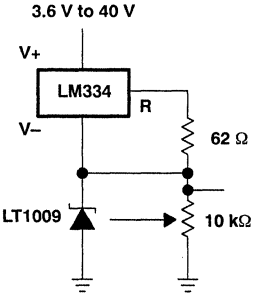


Figure 9. Adjustable Reference With Wide-Supply Range

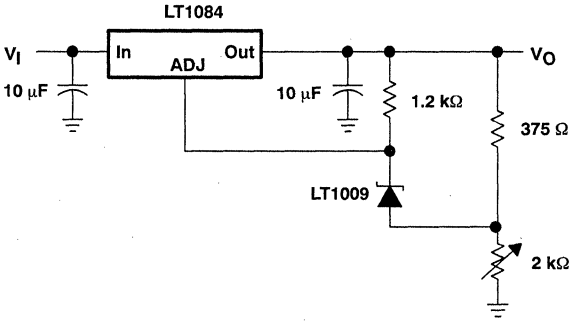


Figure 10. Power Regulator With Low Temperature Coefficient

APPLICATION INFORMATION

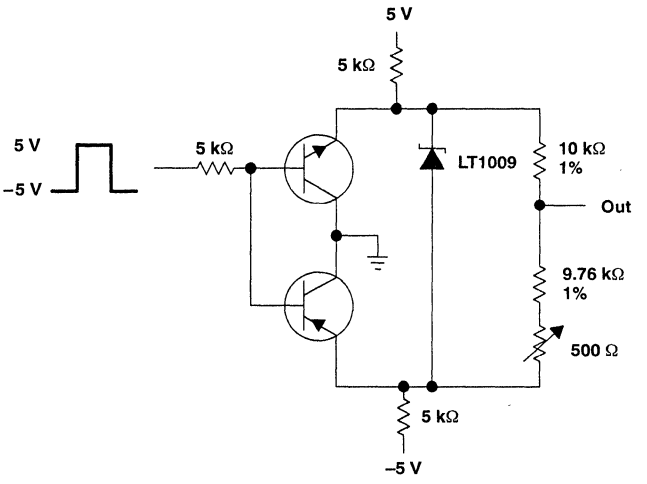


Figure 11. Switchable ±1.25-V Bipolar Reference

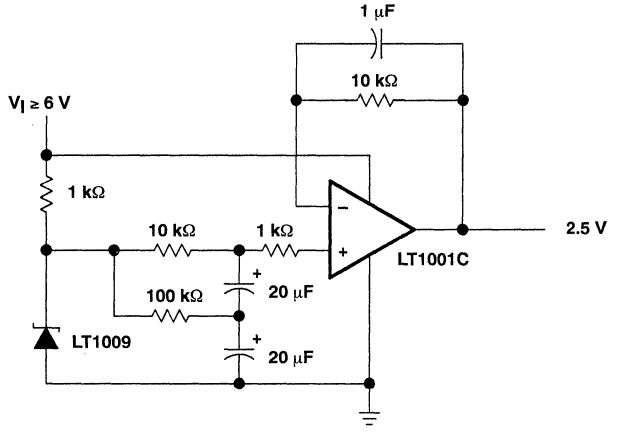


Figure 12. Low-Noise 2.5-V Buffered Reference

D3202, FEBRUARY 1990–REVISED AUGUST 1991

- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin Compatible With the LTC1044/7660**

description

The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current is typically 1.1 V. This holds true over the full supply voltage range of 3.5 V to 15 V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shut-down is typically 100 μA.

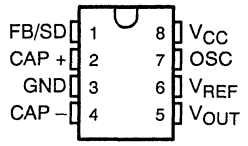
The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator pin can be used to adjust the switching frequency or to externally synchronize the LT1054.

AVAILABLE OPTIONS

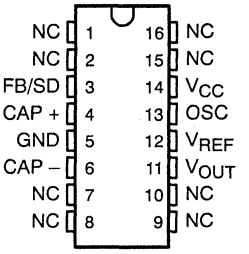
T_A	PACKAGE	
	SMALL OUTLINE (DW)	PLASTIC DIP (P)
0°C to 70°C	LT1054CDW	LT1054CP
−40°C to 85°C	LT1054IDW	LT1054IP

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., LT1054CDWR).

P PACKAGE
(TOP VIEW)

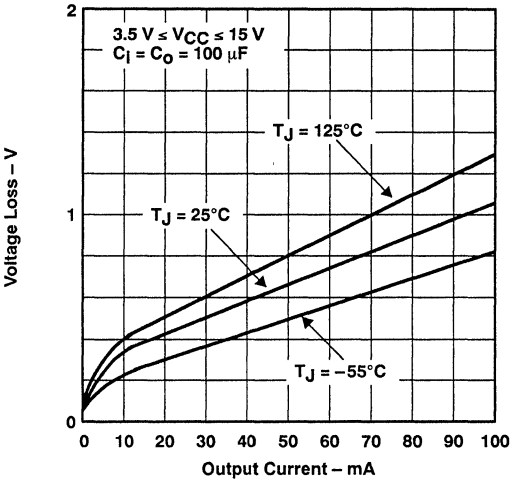


DW PACKAGE
(TOP VIEW)

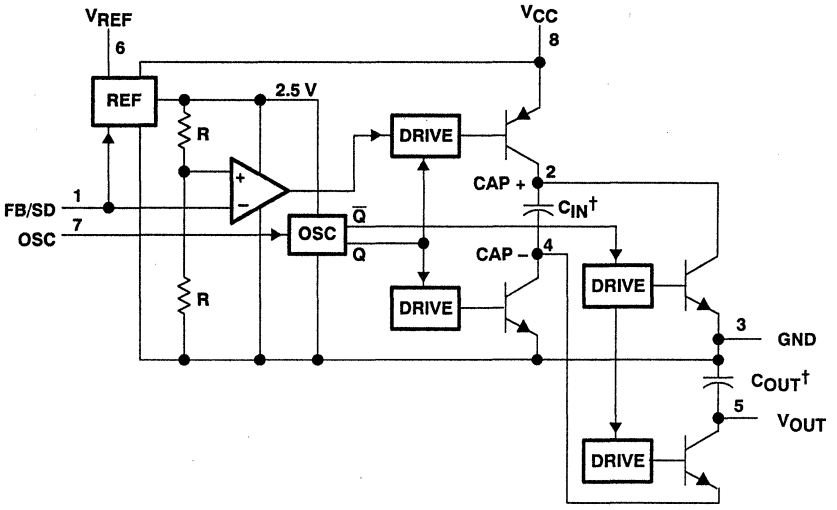


NC – No internal connection

VOLTAGE LOSS
vs
OUTPUT CURRENT



functional block diagram



† External capacitors

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 16 V
Input voltage range, FB/SD terminal ..... 0 V to V_{CC}
Input voltage range, OSC terminal ..... 0 V to V_{ref}
Junction temperature (see Note 2): LT1054C ..... 125°C
LT1054I ..... 135°C
Operating free-air temperature range: LT1054C ..... 0°C to 70°C
LT1054I ..... −40°C to 85°C
Storage temperature range ..... −55°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. The absolute maximum supply voltage rating of 16 V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \leq 15$ V, this rating may be increased to 20 V.
2. The devices are functional up to the absolute maximum junction temperature.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	15	V
Operating free-air temperature range, T_A	LT1054C	0	70	°C
	LT1054I	−40	85	

electrical characteristics

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP‡	MAX	UNIT
Regulated output voltage, V_O	V_{CC} = 7 V, TJ = 25°C, R_L = 500 Ω, See Note 3		25°C	−4.7	−5	−5.2	V
Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 3		Full range		5	25	mV
Output regulation	V_{CC} = 7 V, R_L = 100 Ω to 500 Ω, See Note 3		Full range		10	50	mV
Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = 100 μF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
		I_O = 100 mA	Full range		1.1	1.6	
Output resistance	ΔI_O = 10 mA to 100 mA, See Note 5		Full range		10	15	Ω
Oscillator frequency	V_{CC} = 3.5 V to 15 V		Full range	15	25	35	kHz
Reference voltage, V_{ref}	I_{ref} = 60 μA		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
Maximum switch current			25°C		300		mA
Supply current, I_{CC}	I_O = 0	V_{CC} = 3.5 V	Full range		2.5	3.5	mA
		V_{CC} = 15 V	Full range		3	4.5	
Supply current in shutdown	$V_{FB/SD}$ = 0 V		Full range		100	150	μA

† Full range is 0°C to 70°C for the LT1054C and −40°C to 85°C for the LT1054I.

‡ All typical values are at T_A = 25°C.

NOTES: 3. All regulation specifications are for a device connected as a positive to negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, C_I = 10 μF (tantalum), C_O = 100 μF (tantalum) and C1 = 0.002 μF.

4. For voltage-loss tests, the device is connected as a voltage inverter, with pins 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations.

5. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents less than 10 mA due to the characteristics of the switch transistors.

TYPICAL CHARACTERISTICS

table of graphs

				FIGURE
	Shutdown Threshold	vs T_A	Free-Air Temperature	1
I_{CC}	Supply Current	vs V_{CC}	Input Voltage	2
I_{OSC}	Oscillator Frequency	vs T_A	Free-Air Temperature	3
	Supply Current in Shutdown	vs V_{CC}	Input Voltage	4
I_{avg}	Average Supply Current	vs I_O	Output Current	5
	Output Voltage Loss	vs C_I	Input Capacitance	6
	Output Voltage Loss	vs f_{osc}	Oscillator Frequency (10 μF)	7
	Output Voltage Loss	vs f_{osc}	Oscillator Frequency (100 μF)	8
V_O	Regulated Output Voltage	vs T_A	Free-Air Temperature	9
ΔV_{ref}	Reference Voltage Change	vs T_A	Free-Air Temperature	10

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Motor Speed Servo	17
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TYPICAL CHARACTERISTICS†

SHUTDOWN THRESHOLD
vs
FREE-AIR TEMPERATURE

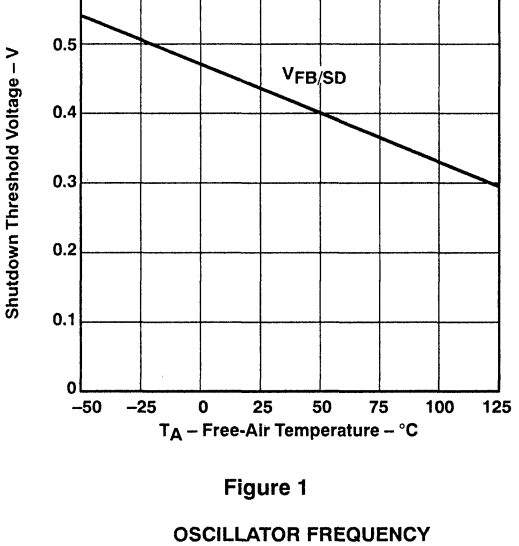


Figure 1

SUPPLY CURRENT
vs
INPUT VOLTAGE

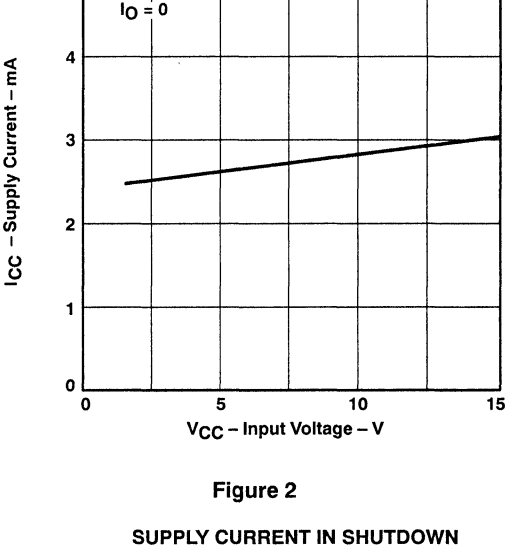


Figure 2

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

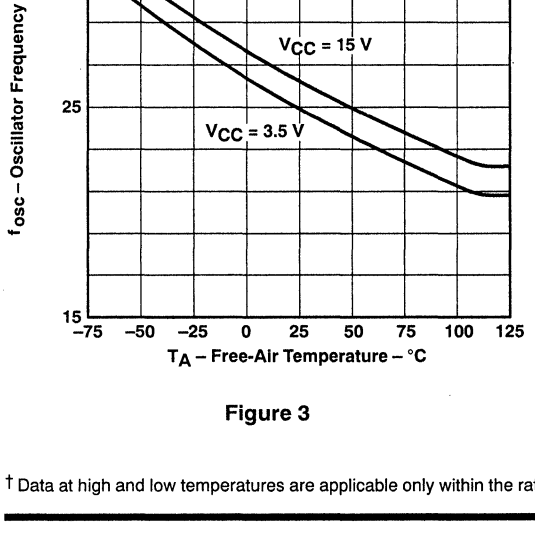


Figure 3

SUPPLY CURRENT IN SHUTDOWN
vs
INPUT VOLTAGE

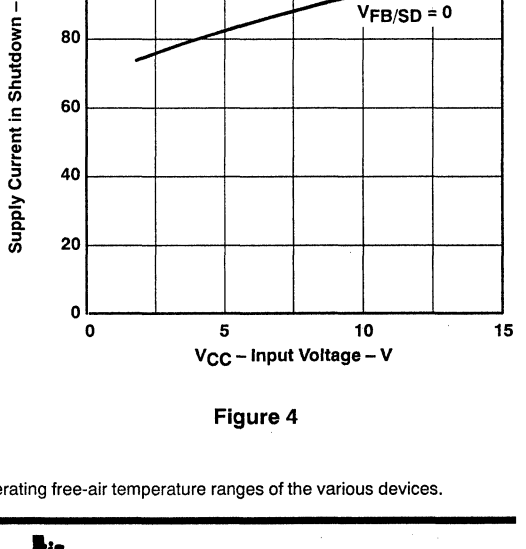


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
OUTPUT CURRENT

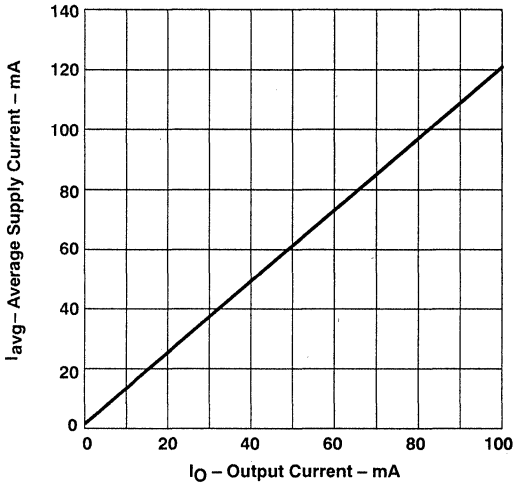


Figure 5

OUTPUT VOLTAGE LOSS
vs
INPUT CAPACITANCE

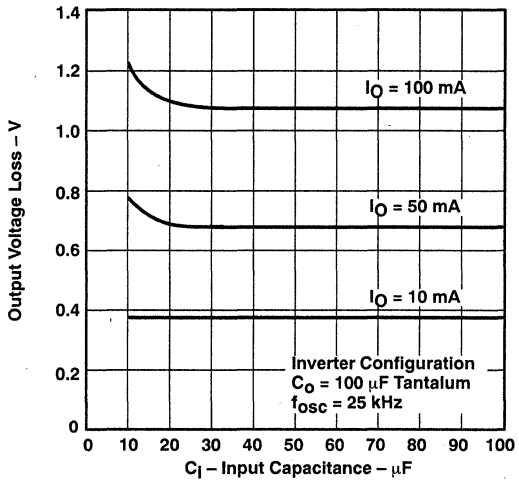


Figure 6

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

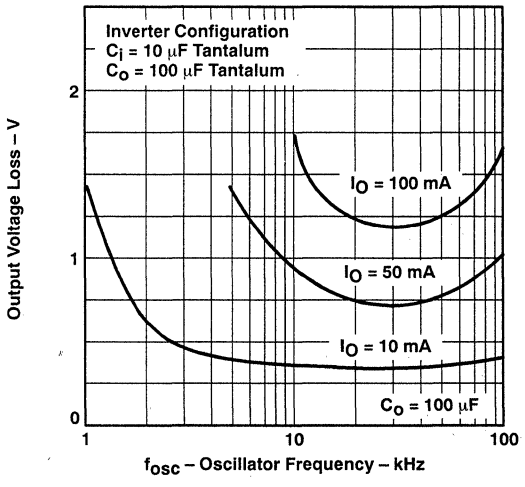


Figure 7

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

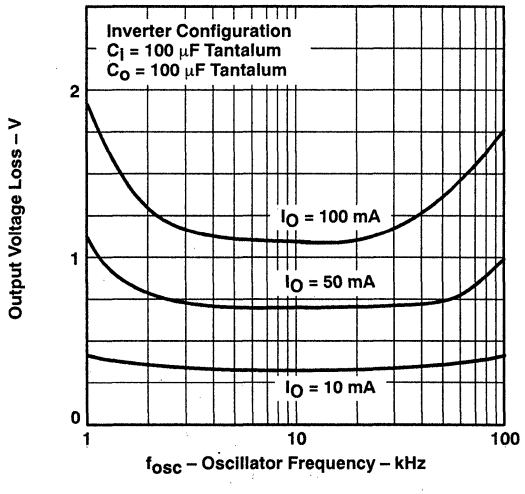


Figure 8

TYPICAL CHARACTERISTICS†

REGULATED OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

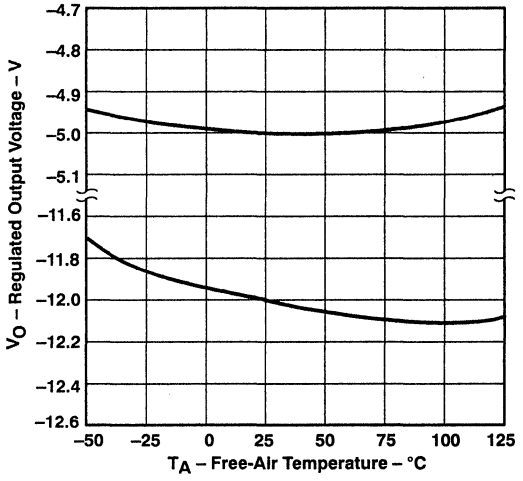


Figure 9

REFERENCE VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

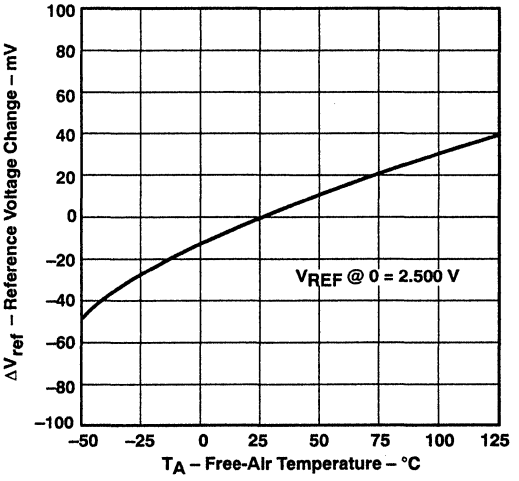


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PRINCIPLES OF OPERATION

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 11 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is as shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

PRINCIPLES OF OPERATION

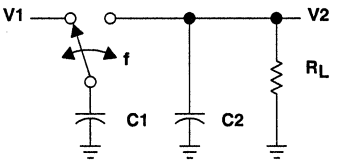


Figure 11. Switched-Capacitor Building Block

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is as shown in Figure 12. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

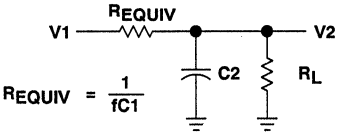


Figure 12. Switched-Capacitor Equivalent Circuit

APPLICATION INFORMATION

pin functions (see functional block diagram)

Supply voltage V_{CC} (pin 8) alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply, and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the LT1054, and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 μF, preferably tantalum or some other low-ESR type, is recommended. A larger capacitor is desirable in some cases. An example is when the actual input supply is connected to the LT1054 through long leads or when the pulse currents drawn by the LT1054 might affect other circuits through supply coupling.

In addition to being the output pin, V_{OUT} (pin 5) is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other pins. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 13). This transistor prevents V_{OUT} from being pulled above the GND pin (pin 3) during start-up. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{(|V_{OUT}|)\,\beta}{I_{OUT}} \tag{4}$$

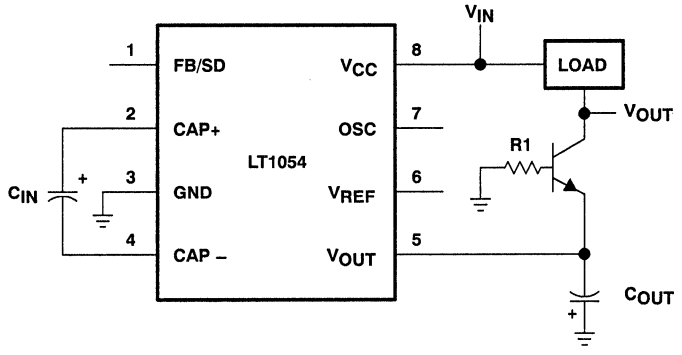


Figure 13. Circuit with Load Connected from V_{CC} to V_{OUT}

APPLICATION INFORMATION

The voltage reference (V_{ref}) output (pin 6) provides a 2.5-V reference point for use in LT1054-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 μA. V_{ref} draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This pin can also be used as a pullup for LT1054 circuits that require synchronization.

CAP+ (pin 2) is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– (Pin 4) is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional, as should be expected when using bipolar switches.

The OSC (pin 7) can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 μA, so that the duty cycle is approximately 50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 14) in the range of 5 pF - 20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{ref}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an NPN transistor can then be used to drive OSC at the external clock frequency as shown in Figure 14.

The frequency can be lowered by adding an external capacitor (C_1 in Figure 14) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

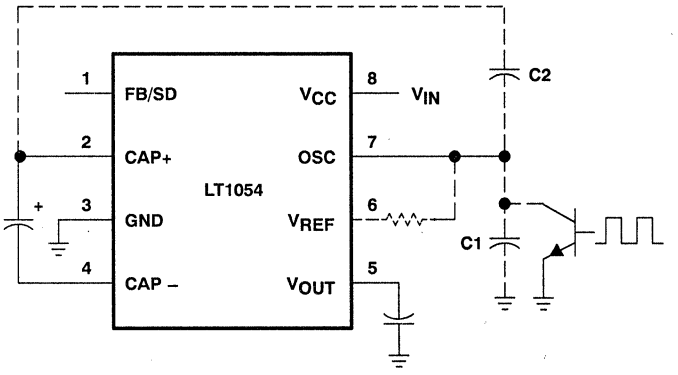
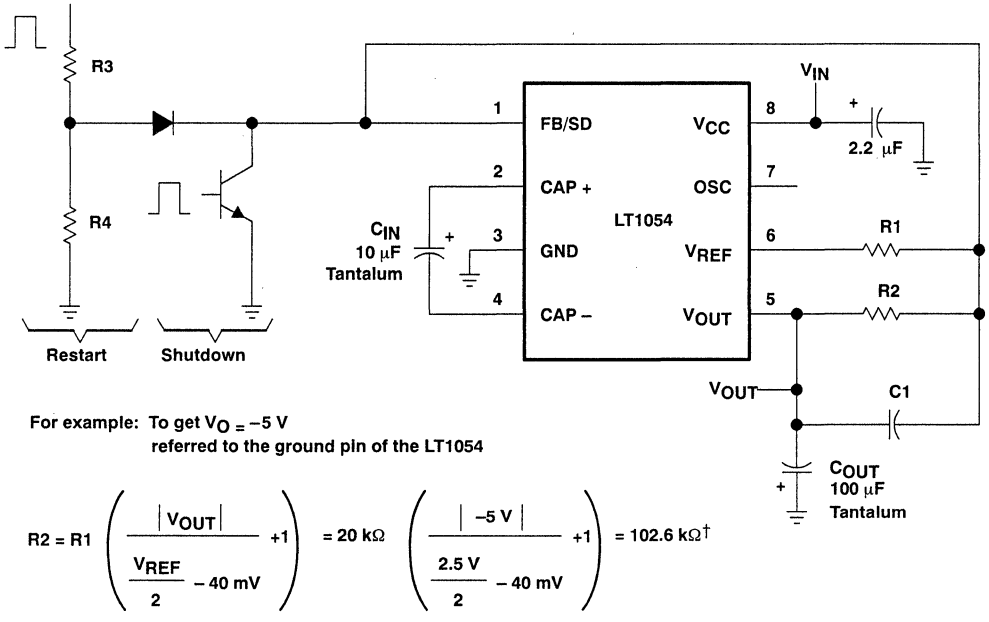


Figure 14. External Clock System

APPLICATION INFORMATION

The feedback/shutdown (FB/SD) pin has two functions. Pulling FB/SD below the shutdown threshold (≈0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 μA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 15, the restart signal can be either a pulse (t_p > 100 μs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 15 should be chosen to provide a signal level at FB/SD of 0.7 V - 1.1 V.

FB/SD is also the inverting input of the LT1054 error amplifier, and as such can be used to obtain a regulated output voltage.



For example: To get V_O = −5 V referred to the ground pin of the LT1054

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|-5\text{ V}|}{\frac{2.5\text{ V}}{2} - 40\text{ mV}} + 1\right) = 102.6\text{ k}\Omega^{\dagger}$$

Where: R1 = 20 kΩ
V_{REF} = 2.5 V Nominal

† Choose the closest 1% value

Figure 15. Basic Regulation Configuration

APPLICATION INFORMATION

regulation

The error amplifier of the LT1054 drives the PNP switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 is used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 15 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 μA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 μF for all output voltages.

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054, must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler can provide higher voltages at reduced output currents.

capacitor selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good-quality low-ESR capacitors, such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the equivalent series resistance (ESR) of the capacitor is multiplied by four, since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique is used to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown:

$$\Delta V = \frac{I_{OUT}}{2\, fC_{OUT}} \tag{5}$$

where:

ΔV = p-p ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (ESR\ of\ C_{OUT}) \tag{6}$$

power dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 is calculated as shown.

APPLICATION INFORMATION

$$P \approx (V_{CC} - |V_{OUT}|)\, I_{OUT} + (V_{CC})\,(I_{OUT})\,(0.2) \quad (7)$$

where both V_{CC} and V_{OUT} refer to the ground pin. The power dissipation is equivalent to that of a linear regulator. Limited power handling capability of the LT1054 packages causes limited output current requirements or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 16. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown.

$$R_X = V_X/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - [(LT1054\ voltage\ loss)\ (1.3) + |V_{OUT}|] \quad (8)$$

and I_{OUT} = maximum required output current. The factor of 1.3 allows some operating margin for the LT1054. When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ V - |-5\ V|)\ (100\ mA) + (12\ V)\ (100\ mA)\ (0.2)$$

$$P = 700\ mW + 240\ mW = 940\ mW$$

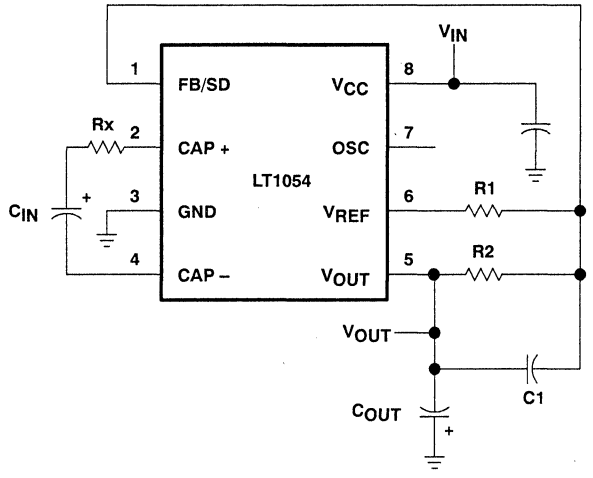


Figure 16. Power-Dissipation-Limiting Resistor in Series with C_{IN}

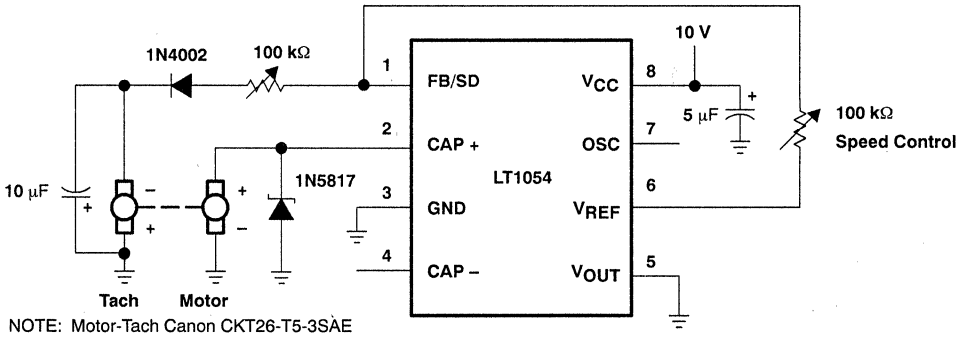
At θ_{JA} of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external-resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

$$V_X = 12\ V - [(1.6\ V)\ (1.3) + |-5\ V|] = 4.9\ V \quad \text{and}$$

$$R_X = 4.9\ V/(4.4)\ (100\ mA) = 11\ \Omega$$

APPLICATION INFORMATION

The resistor reduces the power dissipated by the LT1054 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the LT1054 leads helps to remove heat from the device. This is especially true for plastic packages.



NOTE: Motor-Tach Canon CKT26-T5-3SAE

Figure 17. Motor Speed Servo

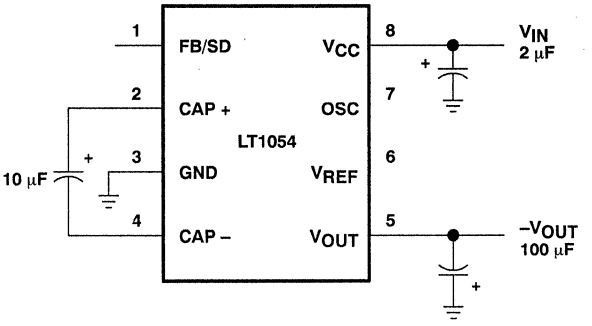


Figure 18. Basic Voltage Inverter

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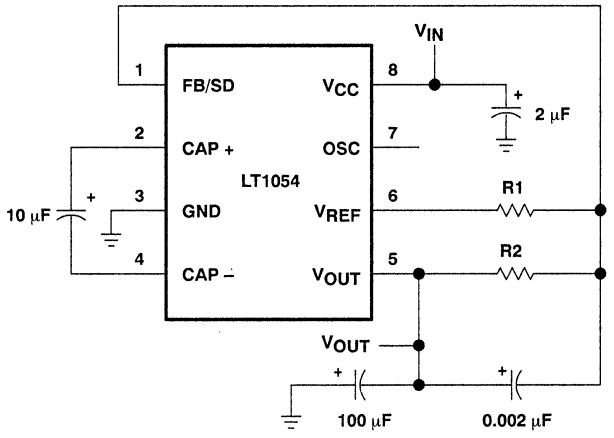
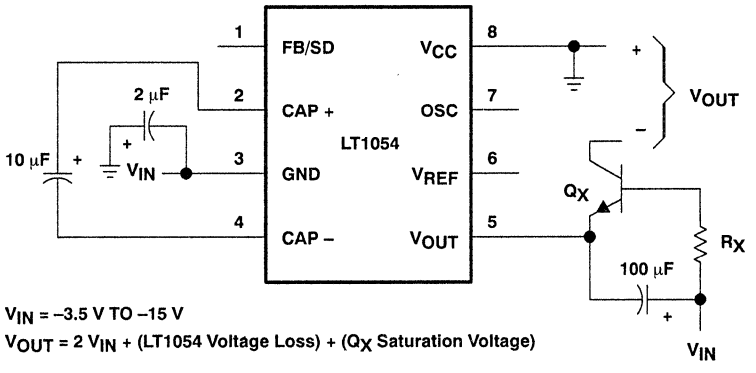
APPLICATION INFORMATION



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = 20\text{ k}\Omega\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 19. Basic Voltage Inverter/Regulator



V_{IN} = –3.5 V TO –15 V

$V_{OUT} = 2\ V_{IN}$ + (LT1054 Voltage Loss) + (Q_X Saturation Voltage)

Figure 20. Negative Voltage Doubler

APPLICATION INFORMATION

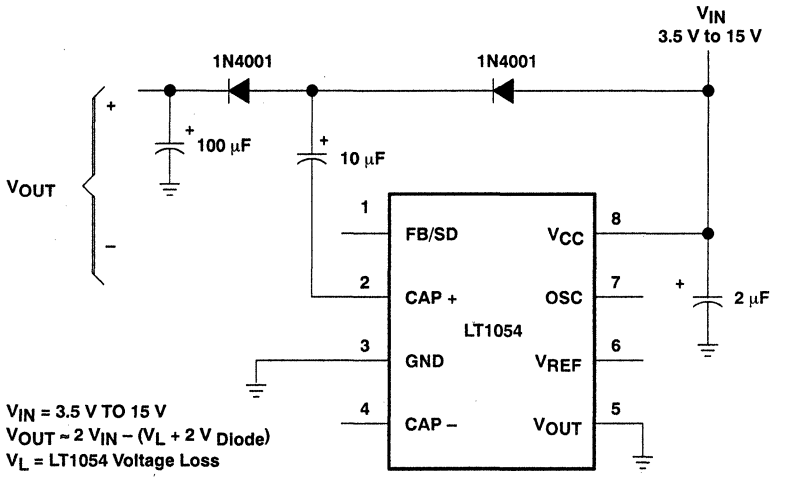


Figure 21. Positive Doubler

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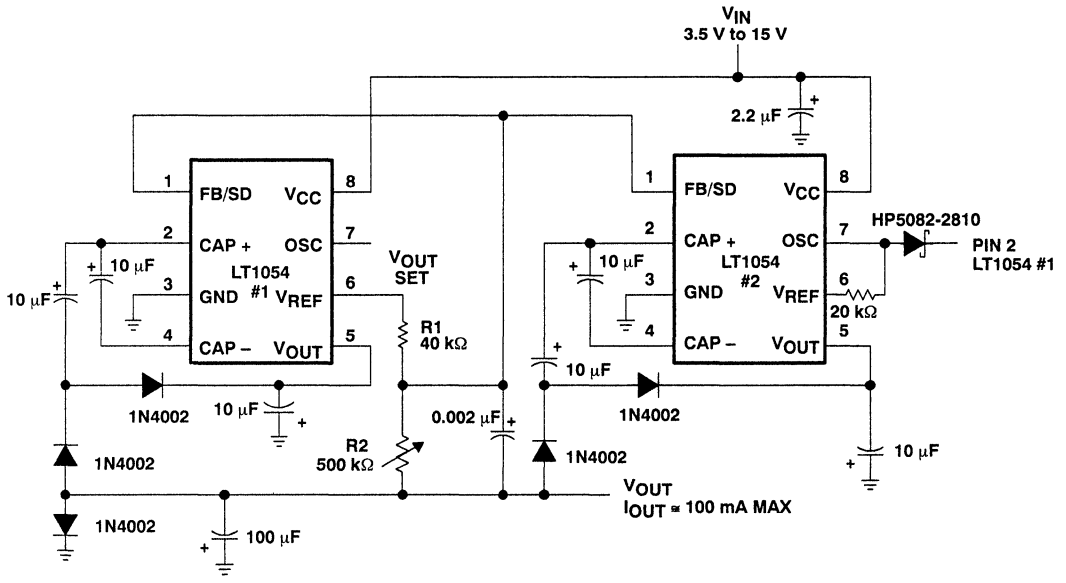
APPLICATION INFORMATION



V_{IN} = 3.5 to 15 V
V_{OUT} MAX ≈ −2 V_{IN} + [LT1054 Voltage Loss +2 (V_{Diode})]

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 22. 100-mA Regulating Negative Doubler

APPLICATION INFORMATION

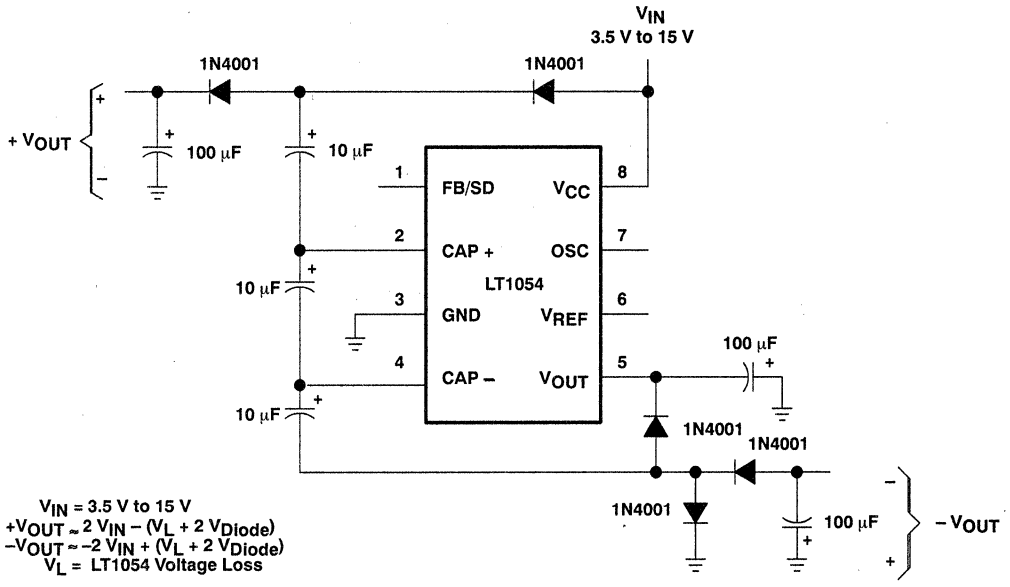


Figure 23. Dual Output Voltage Doubler

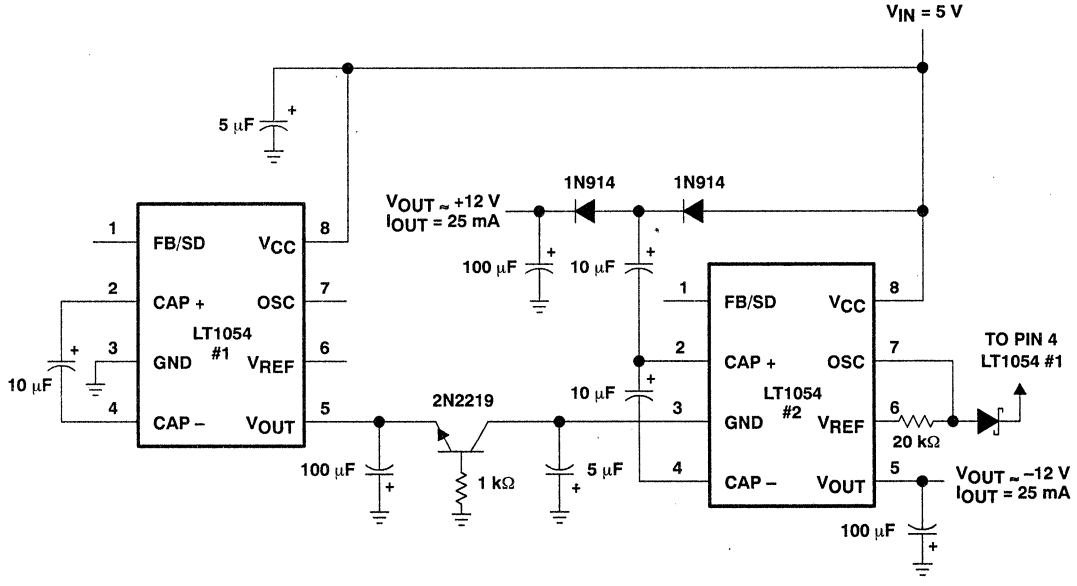


Figure 24. 5-V to ±12-V Converter

APPLICATION INFORMATION

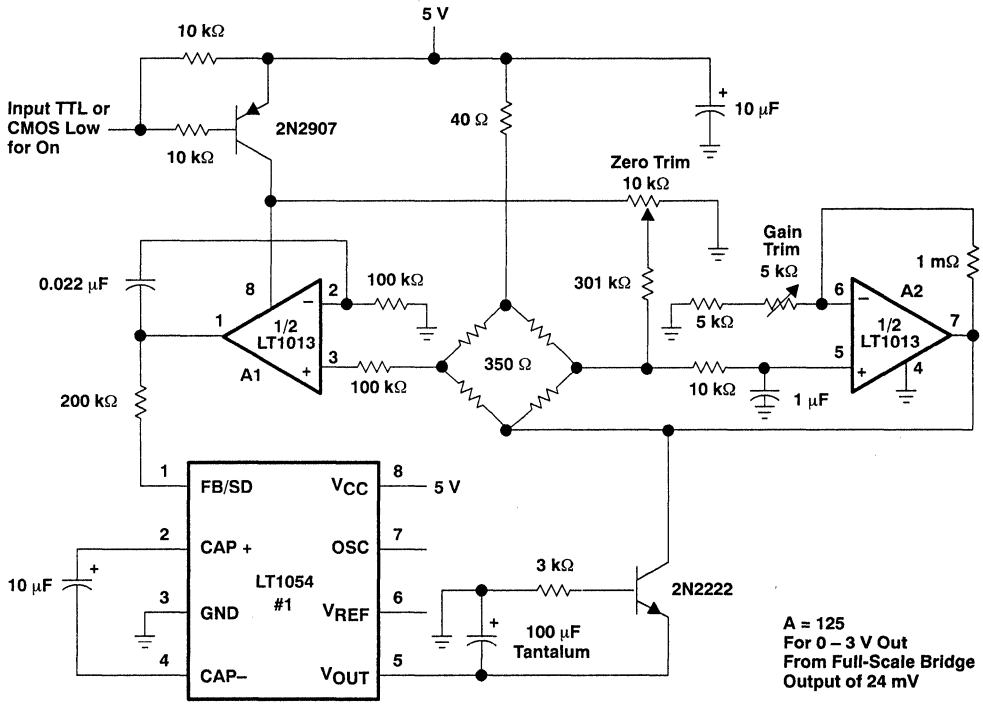
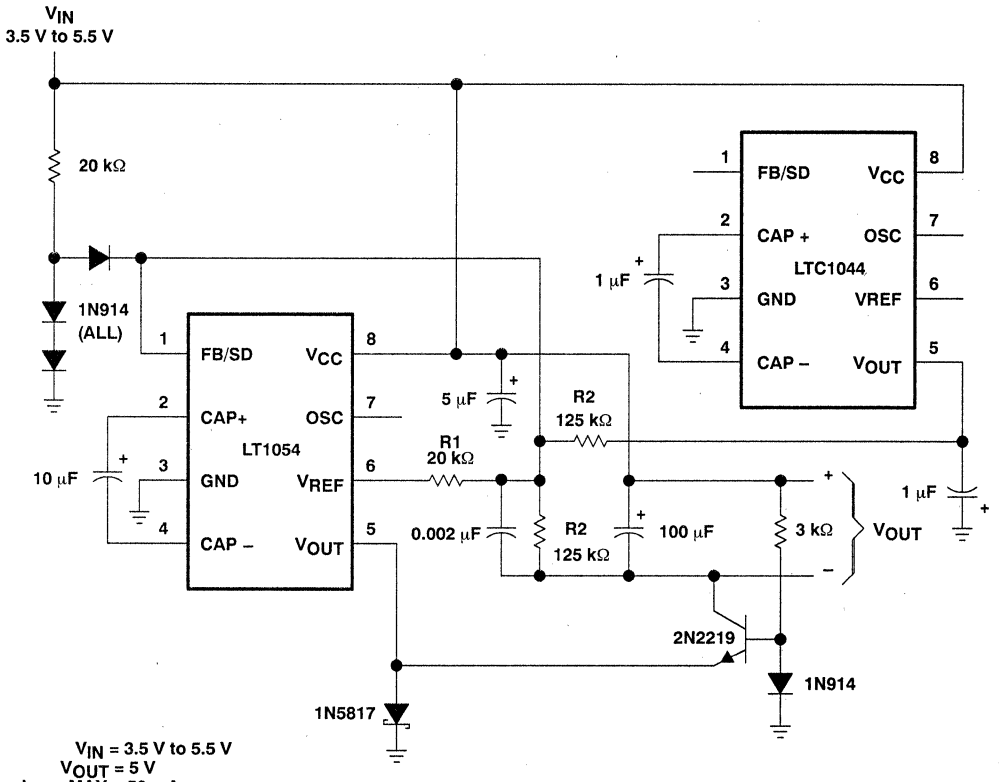


Figure 25. Strain Gage Bridge Signal Conditioner

APPLICATION INFORMATION



V_{IN} = 3.5 V to 5.5 V
V_{OUT} = 5 V
I_{OUT} MAX = 50 mA

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 26. 3.5-V to 5-V Regulator

APPLICATION INFORMATION

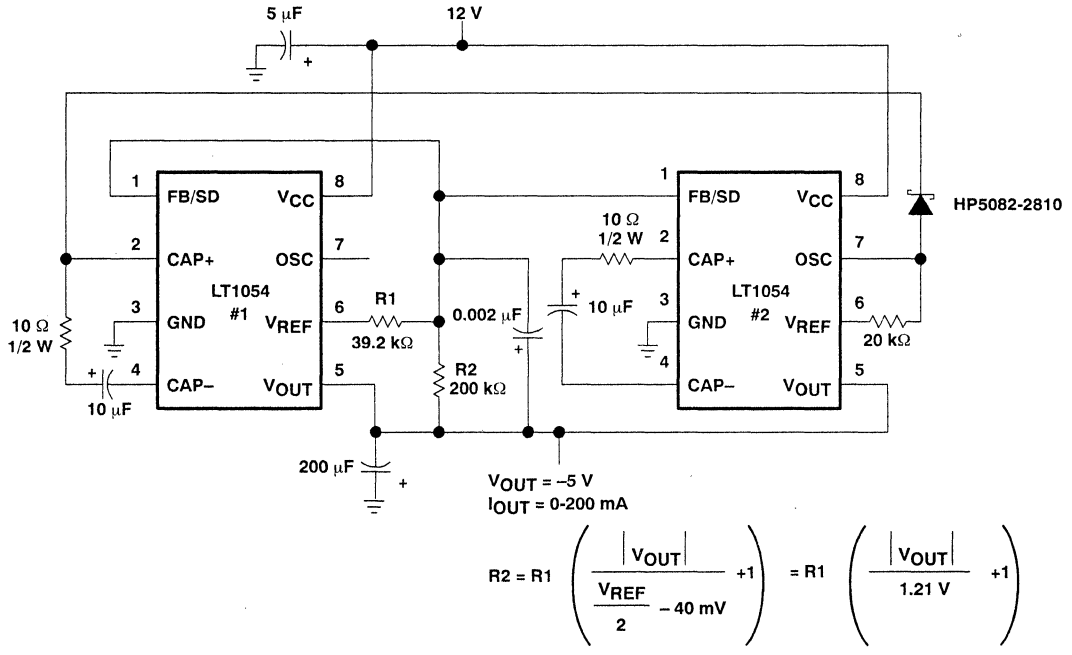


Figure 27. Regulating 200-mA + 12-V to –5-V Converter

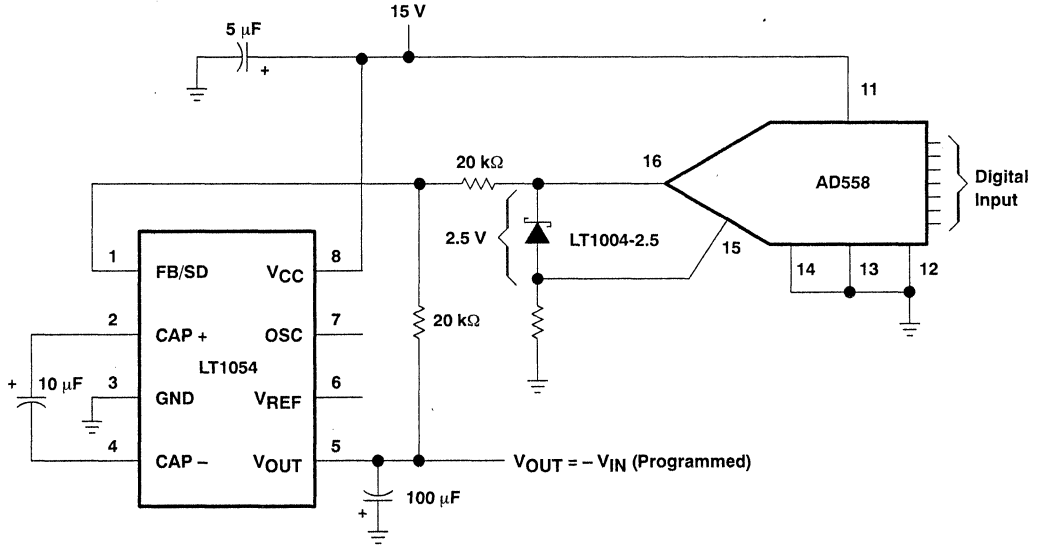


Figure 28. Digitally Programmable Negative Supply

APPLICATION INFORMATION

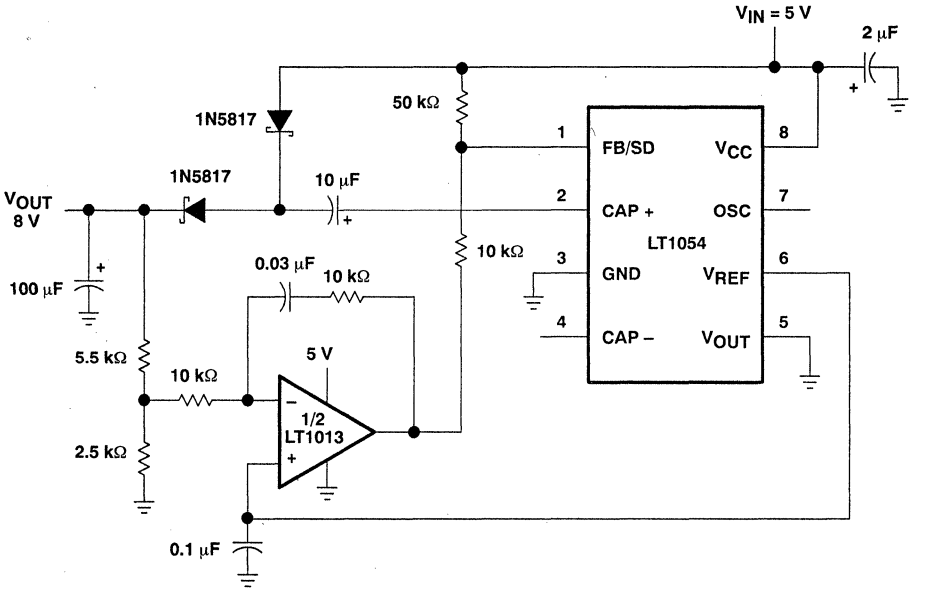
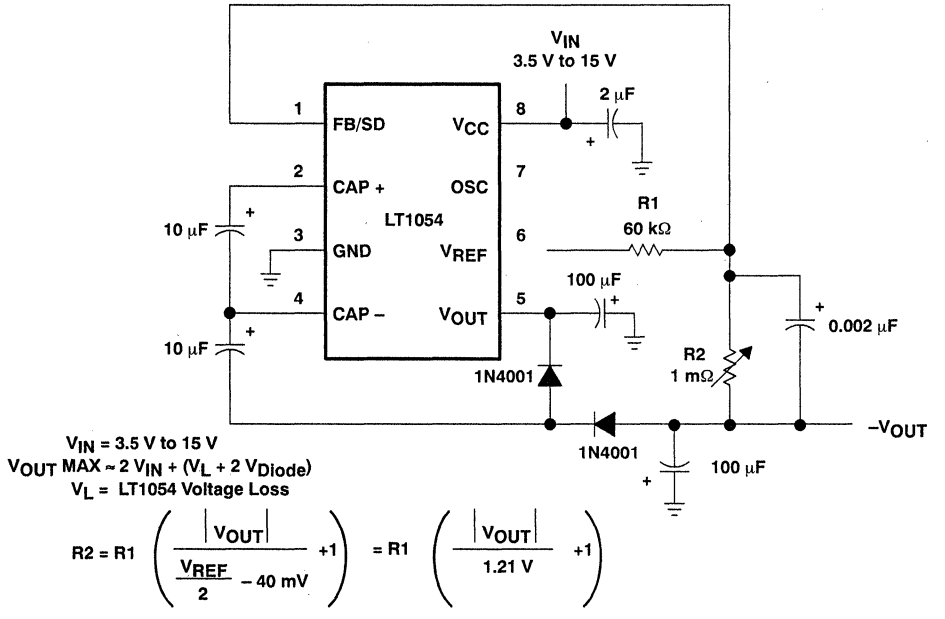


Figure 29. Positive Doubler with Regulation (5-V to 8-V Converter)



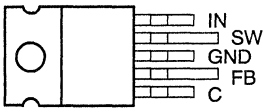
$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

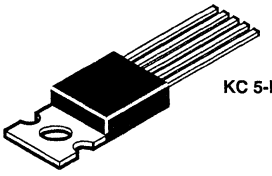
Figure 30. Negative Doubler with Regulator

D3222, OCTOBER 1988–REVISED OCTOBER 1991

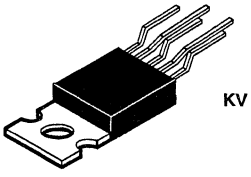
- **Wide Supply Voltage Range:**
  LT1070HV . . . 3 V to 60 V
  LT1070 . . . 3 V to 40 V
- **Low Quiescent Current . . . 6 mA Typ**
- **Self-Protected Against Overloads**
- **Operates in Most Switching Configurations**
- **Low Shutdown-Mode Supply Current**
- **Floating Outputs in Flyback-Regulated Mode**
- **Available in Standard KC and KV Packages**
- **Can Be Externally Synchronized**

KC AND KV PACKAGE
(KV Package Used for Illustration)
(TOP VIEW)





KC 5-LEAD



KV 5-LEAD

AVAILABLE OPTIONS

T_J	MAX INPUT VOLTAGE	KC PACKAGE	KV PACKAGE
0°C to 100°C	60 V	LT1070HVCKC	LT1070HVCKV
	40 V	LT1070CKC	LT1070CVKV
−40°C to 125°C	60 V	LT1070HVIKC	LT1070HVIKV
	40 V	LT1070IKC	LT1070IKV

description

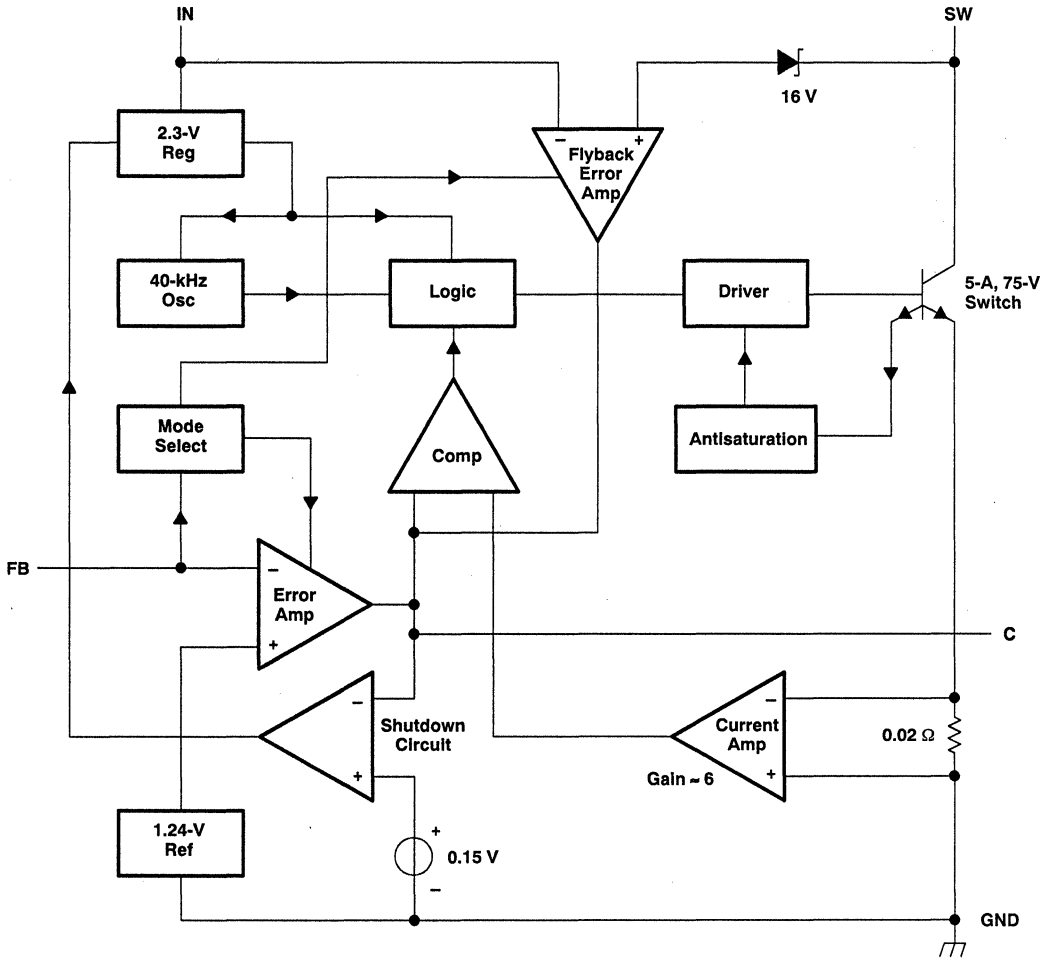
The LT1070 is a monolithic, high-efficiency switching regulator. It can be operated in all standard switching configurations including: step-down (buck), step-up (boost), flyback, forward, inverting, and Cuk†. A high-current, high-efficiency switch is included in the package along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070 to be built in a standard 5-pin KC or KV package. This makes it extremely easy to use and provides reliable operation similar to that obtained with 3-pin linear regulators.

The LT1070 operates with supply voltages from 3 V to 40 V. The LT1070HV, a high-voltage version of the LT1070, operates with supply voltages from 3 V to 60 V. These devices draw only 6 mA of quiescent current, deliver load power up to 100 W with no external power devices, and by utilizing current-mode switching techniques, they provide excellent ac and dc input and output regulation.

The LT1070 is much easier to use than the low-power control chips that are presently available and has many unique features that are not found on these chips. It uses an adaptive saturation-preventing switch drive to allow very-wide-ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional flyback-regulation mode built into the LT1070 without the need for optocouplers or extra transformer windings.

†A boost-buck-derived regulator circuit patented by Slobodan Ćuk.

functional block diagram



Resistor value shown is nominal.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Supply voltage, V_{IN} (see Note 1): LT1070 ..... 40 V
LT1070HV ..... 60 V
Switch output voltage: LT1070 ..... 65 V
LT1070HV ..... 75 V
Feedback input voltage, V_{FB} (transient, 1 ms) ..... ±15 V
Continuous total dissipation ..... See Dissipation Rating Tables 1 and 2
Operating virtual-junction temperature range:
LT1070C, LT1070HVC (normal operation) ..... 0°C to 100°C
LT1070C, LT1070HVC (short-circuit operation) ..... 0°C to 125°C
LT1070I, LT1070HVI ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

NOTE 1: Minimum switch-on time for the LT1070 in current limit is ≈ 1 μs. This limits the maximum input voltage during short-circuit conditions, in the step-down and inverting modes only, to ≈ 35 V. Normal (unshorted) conditions are not affected. If the LT1070 is being operated in the step-down or inverting mode at high input voltages and short-circuit conditions are expected, a resistor must be placed in series with the inductor.

DISSIPATION RATING TABLE 1
FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 100°C$ POWER RATING	$T_A = 125°C$ POWER RATING
KC and KV	2000 mW	16 mW/°C	800 mW	400 mW

DISSIPATION RATING TABLE 2
CASE TEMPERATURE

PACKAGE	$T_C \le 70°C$ POWER RATING	OPERATING FACTOR ABOVE $T_C = 70°C$	$T_C = 125°C$ POWER RATING
KC and KV	20 mW	250 mW/°C	6.25 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_{IN}	LT1070C, LT1070I	3	40	V
	LT1070HVC, LT1070HVI	3	60	
Virtual-junction temperature, T_J	LT1070C, LT1070HVC	0	100	°C
	LT1070I, LT1070HVI	−40	125	

electrical characteristics at specified virtual-junction temperature, V_{IN} = 15 V, $V_{FB} = V_{ref}$, with SW output open (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
V_{ref}	Reference voltage	Measured at FB input,	V_C = 0.6 V	25°C	1.224	1.244	1.264	V
				Full range	1.214		1.274	
	Reference voltage input regulation	V_{IN} = 3 V to MAX,	V_C = 0.6 V	Full range			0.03	%/V

error amplifier section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
I_{FB}	Feedback input current	$V_{FB} = V_{ref}$		25°C		380	750	nA
				Full range			1100	
g_m	Transconductance	ΔI_C = ±25 μA		25°C	3000	4200	6000	μmho
				Full range	2400		7000	
	Source current	V_C = 1.5 V,	V_{FB} = 0.8 V	25°C	150	200	350	μA
				Full range	120		400	
	Sink current	V_C = 1.5 V,	V_{FB} = 1.5 V	25°C	150	200	350	μA
				Full range	120		400	
$V_{O(C)}$	Output voltage	High state,	V_{FB} = 1 V	25°C	1.8		2.3	V
		Low state,	V_{FB} = 1.5 V		0.25	0.38	0.52	
A_V	Voltage amplification	V_C = 0.7 V to 1.4 V		Full range	500	800	2000	V/V
$V_{T(C)}$	Control threshold voltage	Duty cycle = 0		25°C	0.8	0.9	1.08	V
				Full range	0.6		1.25	

flyback amplifier section

PARAMETER		TEST CONDITIONS†			T_J‡	MIN	TYP§	MAX	UNIT
$V_{T(FB)}$	Normal-/flyback-mode threshold voltage	I_{FB} = 50 μA			25°C	0.4	0.45	0.54	V
V_Z	Flyback reference voltage	V_C = 0.6 V, I_{FB} = 50 μA	I_C = −1 μA to 1 μA,		25°C	15	16.3	17.6	V
					Full range	14		18	
ΔV_Z	Change in flyback reference	V_C = 0.6 V I_{FB} = 0.05 to 1 mA	I_C = −1 μA to 1 μA,		25°C	4.5	6.8	8.5	V
	Flyback reference voltage input regulation	V_C = 0.6 V, I_{FB} = 50 μA,	I_C = −1 μA to 1 μA, V_{IN} = 3 V to MAX		25°C		0.01	0.03	%/V
g_m	Transconductance	$\Delta I_C \le \pm 10$ μA,	I_{FB} = 50 μA		25°C	150	300	500	μmho
	Source or sink current	V_C = 1.5 V, $V_{(SW)} = V_Z + V_{IN} \pm 1$ V	I_{FB} = 50 μA,	Source	Full range	15	32	50	μA
				Sink		25	40	70	

† .For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1070C and LT1070HVC and −40°C to 125°C for LT1070I and LT1070HVI
§ All typical values are T_A = 25°C.

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electrical characteristics at specified virtual junction temperature, V_{IN} = 15 V, V_{FB} = V_{ref} with SW output open (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$V_{(BR)SW}$	Switch breakdown voltage	V_{FB} = 1.5 V, V_{IN} = 3 V to MAX, I_{SW} = 5 mA	LT1070	Full range	65			V
			LT1070HV		75			
Ron	Switch on-state resistance	V_{FB} = 0.8 V, I_{SW} = 5 A		Full range		0.15	0.24	Ω
g_m	Control-to-switch transconductance			25°C		8		mho
$I_{SW(lim)}$	Switch current limit	Duty cycle = 50%, V_{FB} = 0.8 V		Full range	5		13	A
		Duty cycle = 80%, V_{FB} = 0.8 V						
$\Delta I_{IN}/\Delta I_{SW}$	Input current increase during switch turn-on	V_{FB} = 0.8 V		25°C		25	35	mA/A
f	Frequency			25°C	35	40	45	kHz
				Full range	33		47	
	Maximum duty cycle	V_{FB} = 1 V		25°C	90%	92%	97%	
t_d	Flyback sense delay time			25°C		1.5		μs

shutdown section

PARAMETER		TEST CONDITIONS†	T_J‡	MIN	TYP§	MAX	UNIT
$I_{IN(off)}$	Input current	V_{IN} = 3 V to MAX, V_C = 50 mV	25°C		100	250	μA
$V_{T(off)}$	Control threshold voltage	V_{IN} = 3 V to MAX	25°C	100	150	250	mV
			Full range	50		300	

total device

PARAMETER		TEST CONDITIONS†	T_J‡	MIN	TYP§	MAX	UNIT
$V_{IN(min)}$	Minimum input voltage		Full range		2.6	3	V
I_{IN}	Input current	V_{IN} = 3 V to MAX, V_C = 0.6 V	25°C		6	9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1070C and LT1070HVC and −40°C to 125°C for LT1070I and LT1070HVI.
§ All typical values are T_A = 25°C.

theory of operation

The LT1070 is a current-mode switcher. This means that the switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the functional block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when the switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set the current trip level. This technique has several advantages. First, it has immediate response to input-voltage variations, which is unlike ordinary switchers that have poor input transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy-storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input-voltage or output-load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3-V supply for all internal circuitry on the LT1070. This low-dropout design allows input voltage to vary from 3 V to 60 V with virtually no change in device performance. A 40-kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn off of the switch.

A 1.2-V band-gap reference biases the positive input of the error amplifier. The negative input is brought out for output-voltage sensing. This feedback pin has a second function when pulled low with an external resistor. It programs the LT1070 to disconnect the main error-amplifier output and connects the output pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback-topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation, this pin sits at a voltage between 0.9 V (low output current) and 2 V (high output current). The error amplifiers are current-output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft start. Switch duty cycle goes to zero if the C pin is pulled to ground through a diode. This places the LT1070 in an idle mode. Pulling the C pin below 0.15 V causes total regulator shutdown, with only 50-μA supply current for shutdown-circuitry biasing.

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TYPICAL CHARACTERISTICS

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V_{ref}	Reference voltage	vs	Junction temperature	2
ΔV_{ref}	Reference voltage change	vs	Input voltage	3
I_{FB}	Feedback input current	vs	Junction temperature	4
g_m	Error amplifier transconductance	vs	Junction temperature	5
I_C	Control current	vs	Control voltage	6
$V_{T(FB)}$	Normal-/flyback-mode threshold voltage	vs	Junction temperature	7
I_{FB}	Feedback input current	vs	Junction temperature	7
V_Z	Flyback-mode reference voltage	vs	Junction temperature	8
t_d	Flyback sense delay time	vs	Junction temperature	9
$I_{O(SW)}$	Switch output current (with switch off)	vs	Switch voltage	10
	Driver base current	vs	Switch output current	11
$V_{sat(SW)}$	Switch saturation voltage	vs	Switch output current	12
$I_{O(SW)}$	Switch output current limit	vs	Duty cycle	13
	Maximum duty cycle	vs	Junction temperature	14
$I_{IN(off)}$	Shutdown-mode input current	vs	Control voltage	15
$I_{IN(off)}$	Shutdown-mode input current	vs	Input voltage	16
$V_{T(off)}$	Shutdown-mode control threshold voltage	vs	Junction temperature	17
$V_{T(off)}$	Shutdown-mode control threshold current	vs	Junction temperature	17
V_{FB}	Feedback input voltage	vs	Feedback input current	18
$V_{IN(min)}$	Minimum input voltage	vs	Junction temperature	19
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External current limit	38
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TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT POWER
vs
INPUT VOLTAGE

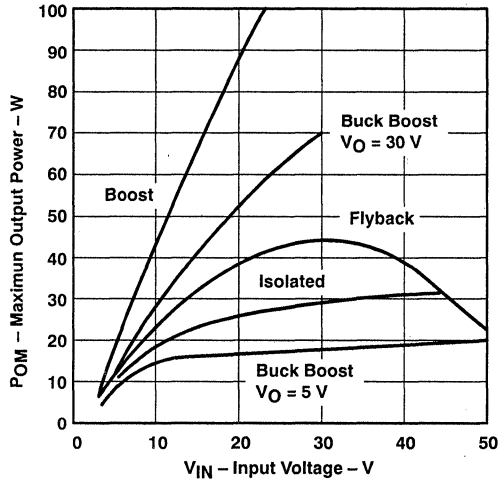

Figure 1

REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

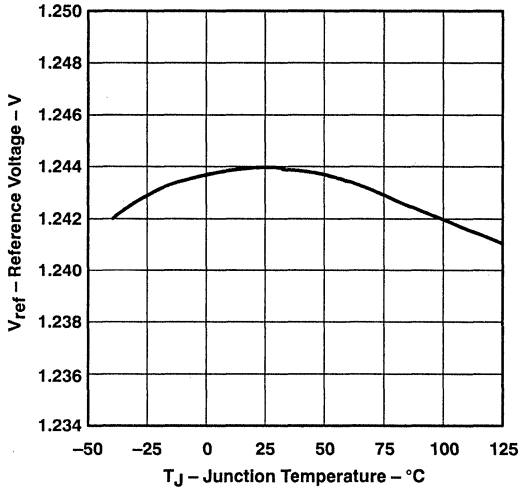

Figure 2

REFERENCE VOLTAGE INPUT REGULATION

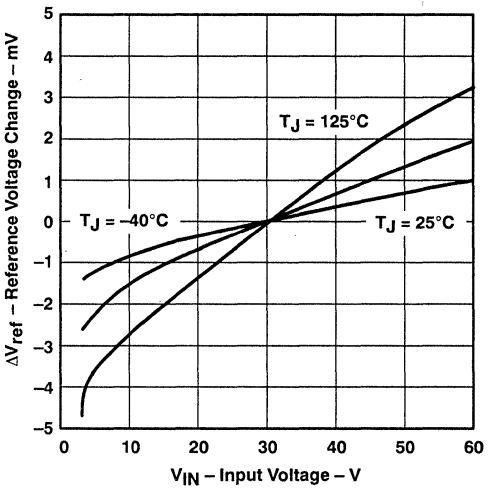

Figure 3

FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

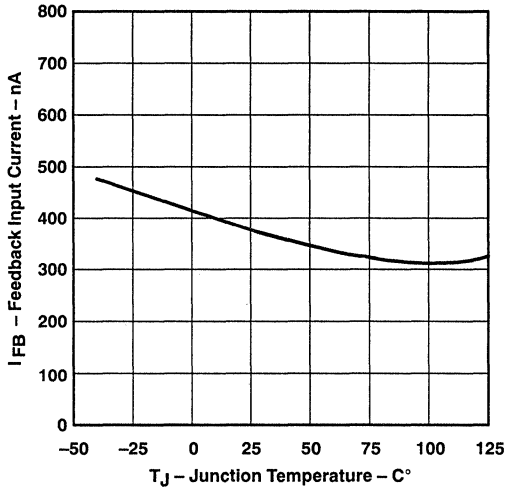

Figure 4

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER TRANSCONDUCTANCE
vs
JUNCTION TEMPERATURE

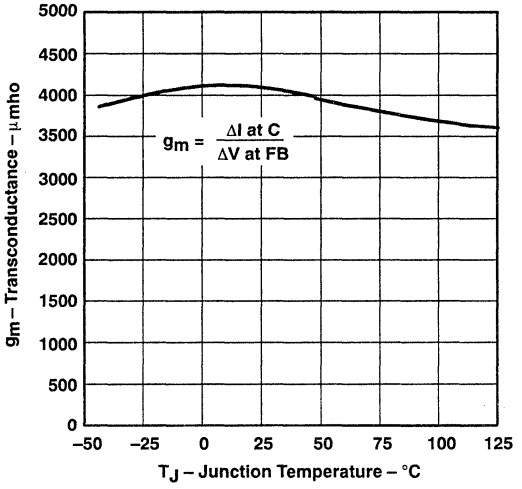

Figure 5

CONTROL CURRENT
vs
CONTROL VOLTAGE

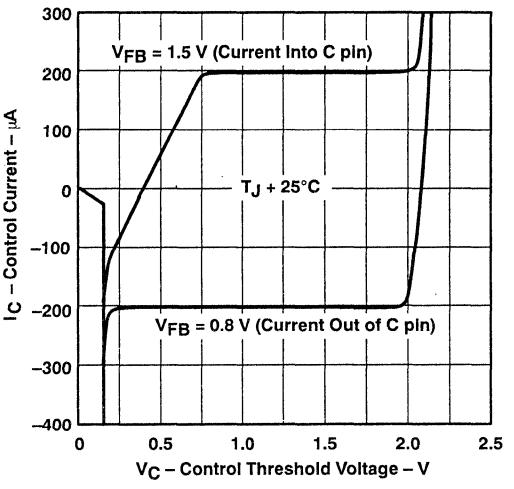

Figure 6

NORMAL/FLYBACK-MODE THRESHOLD VOLTAGE
AND FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

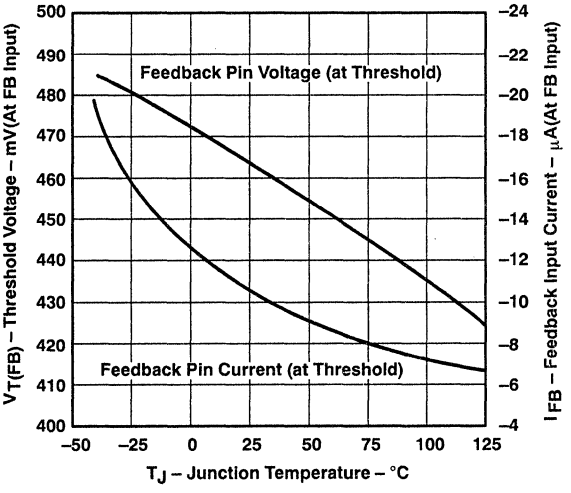

Figure 7

FLYBACK-MODE REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

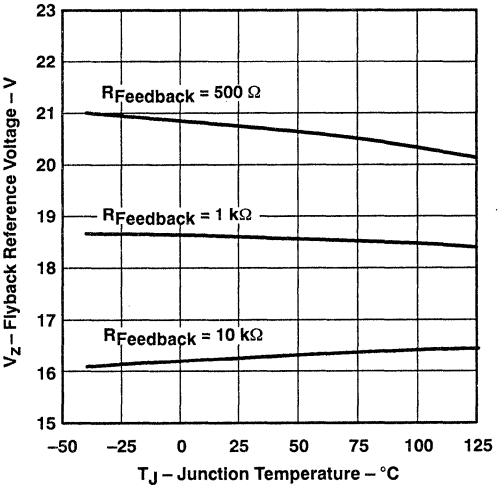

Figure 8

TYPICAL CHARACTERISTICS

FLYBACK SENSE DELAY TIME
vs
JUNCTION TEMPERATURE

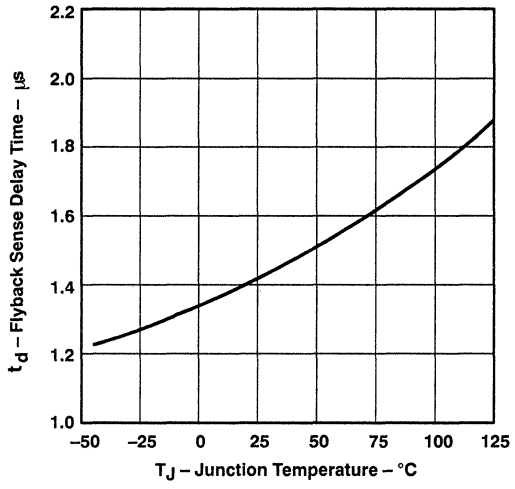

Figure 9

SWITCH OUTPUT CURRENT
vs
SWITCH VOLTAGE and INPUT VOLTAGE
(WITH SWITCH OFF)

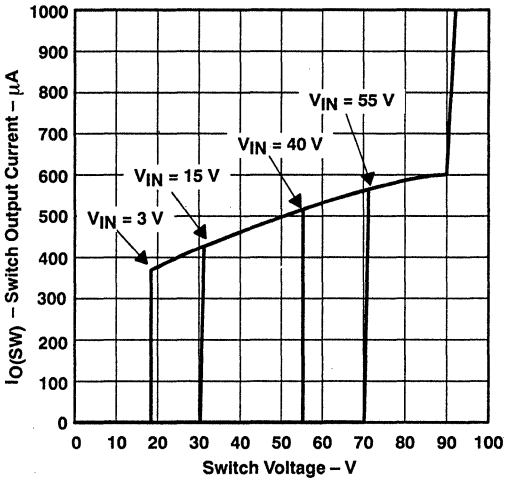

Figure 10

DRIVER BASE CURRENT†
vs
SWITCH OUTPUT CURRENT

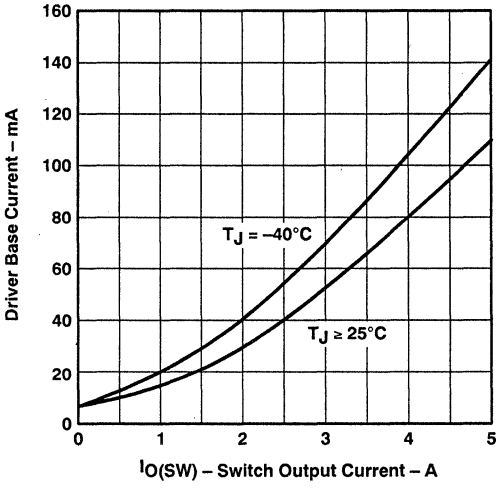

Figure 11

SWITCH SATURATION VOLTAGE
vs
SWITCH CURRENT

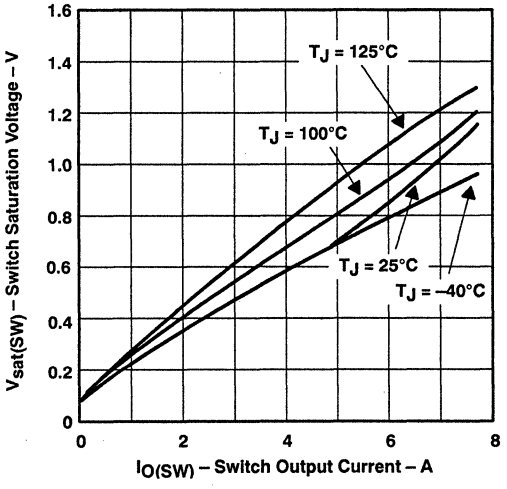

Figure 12

† Average input current is found by multiplying driver base current by duty cycle plus quiescent current.

TYPICAL CHARACTERISTICS

SWITCH OUTPUT CURRENT LIMIT
vs
DUTY CYCLE

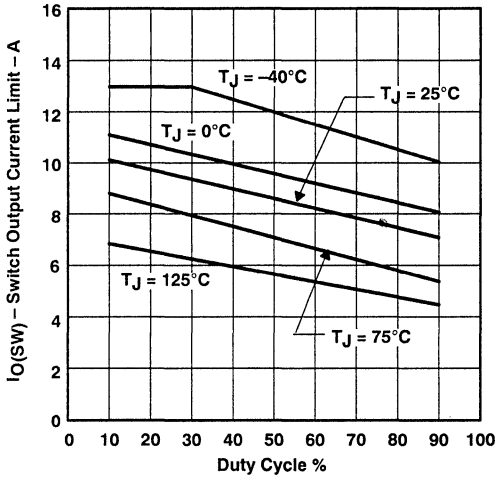

Figure 13

MAXIMUM DUTY CYCLE
vs
JUNCTION TEMPERATURE

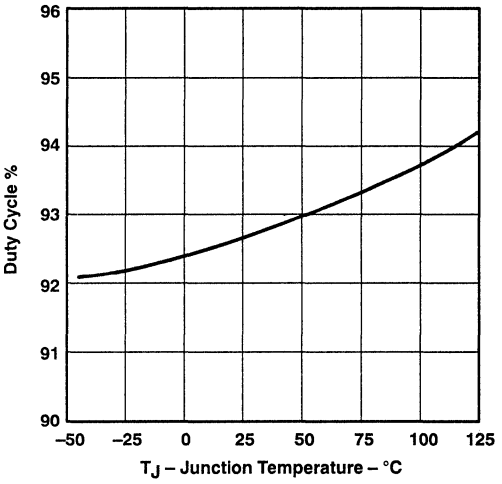

Figure 14

SHUTDOWN-MODE INPUT CURRENT
vs
CONTROL VOLTAGE

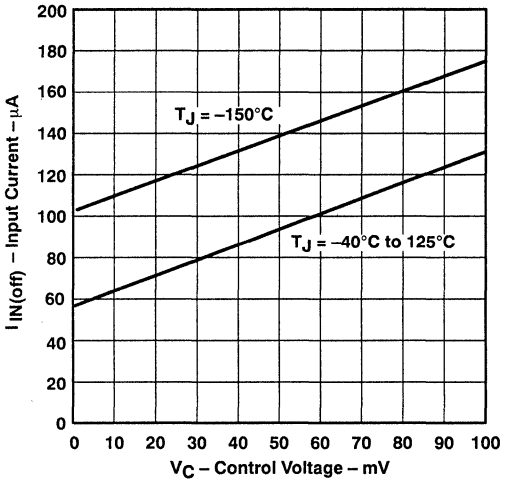

Figure 15

SHUTDOWN-MODE INPUT CURRENT
vs
INPUT CURRENT

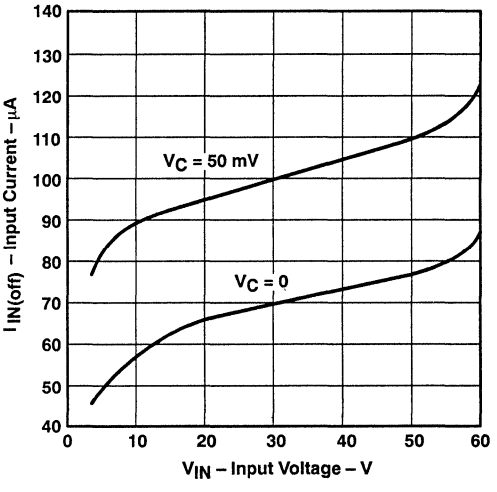

Figure 16

TYPICAL CHARACTERISTICS

CONTROL THRESHOLD VOLTAGE AND CURRENT
vs
JUNCTION TEMPERATURE
(SHUTDOWN MODE)

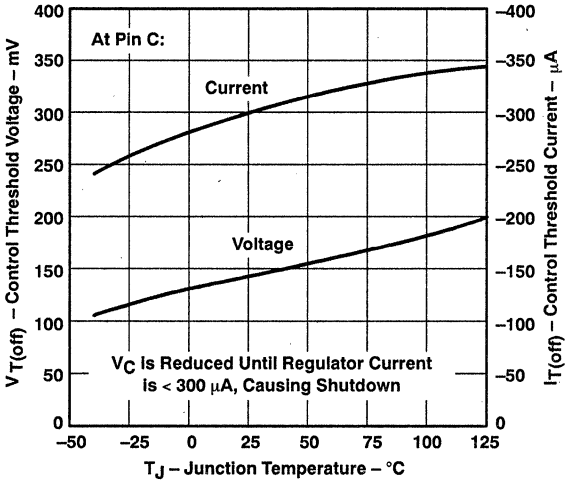

Figure 17

FEEDBACK INPUT VOLTAGE
vs
FEEDBACK INPUT CURRENT

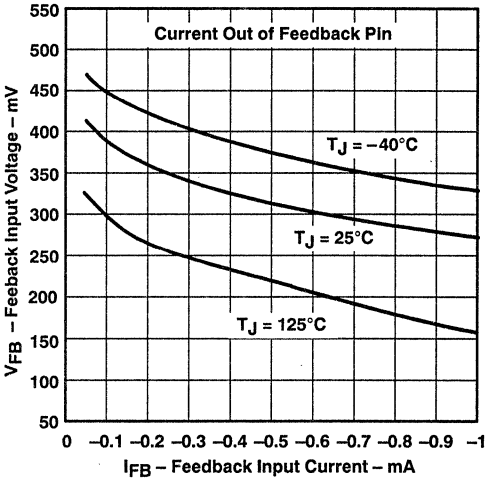

Figure 18

MINIMUM INPUT VOLTAGE
vs
JUNCTION TEMPERATURE

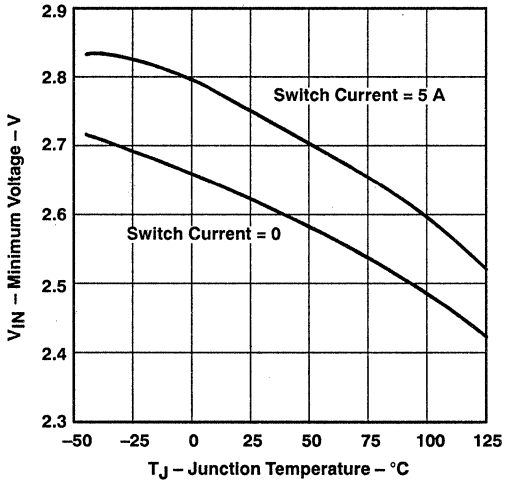

Figure 19

INPUT CURRENT
vs
JUNCTION TEMPERATURE
(SW OUTPUT OPEN)

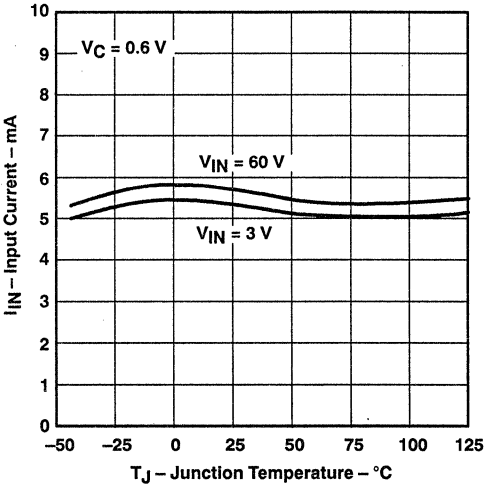

Figure 20

TEXAS INSTRUMENTS
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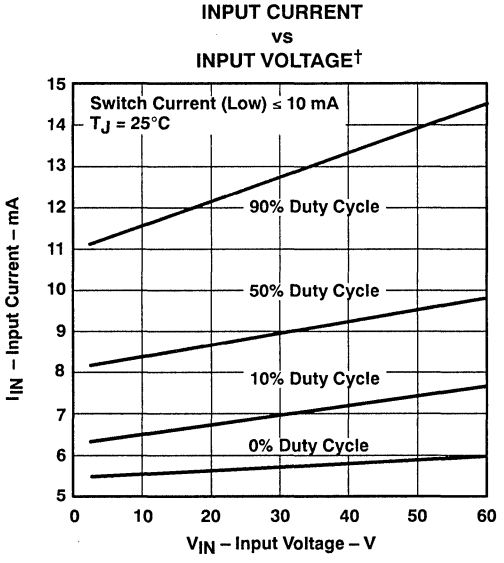
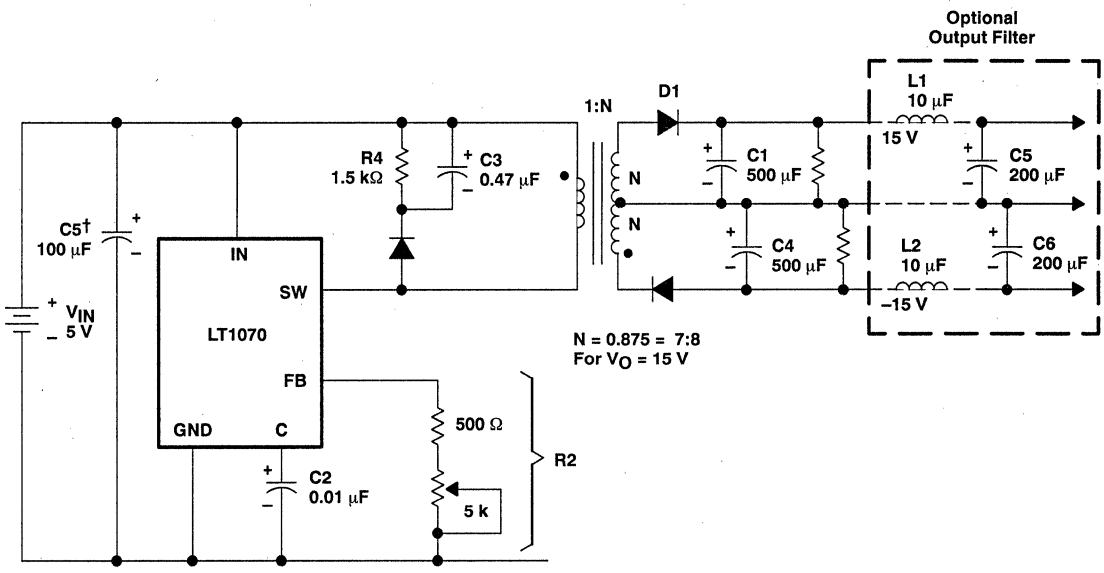
TYPICAL CHARACTERISTICS



† Under very low output current conditions, duty cycle for most circuits will approach 10% or less.

Figure 21

APPLICATION INFORMATION



†Capacitors are required if input lead length exceeds 2 inches.

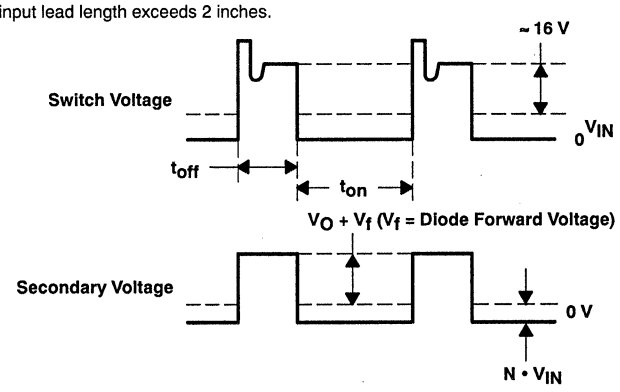
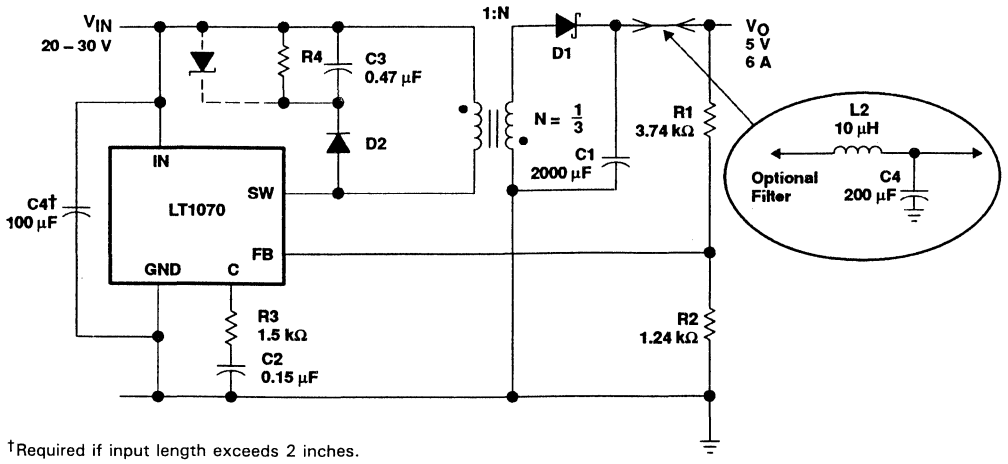


Figure 22. Totally Isolated Converter

APPLICATION INFORMATION



†Required if input length exceeds 2 inches.

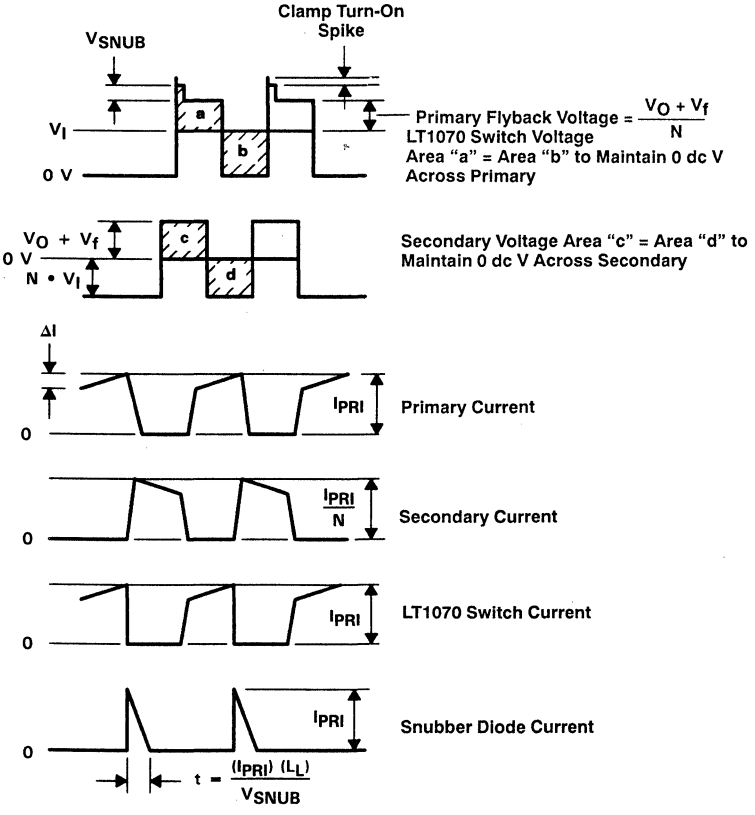
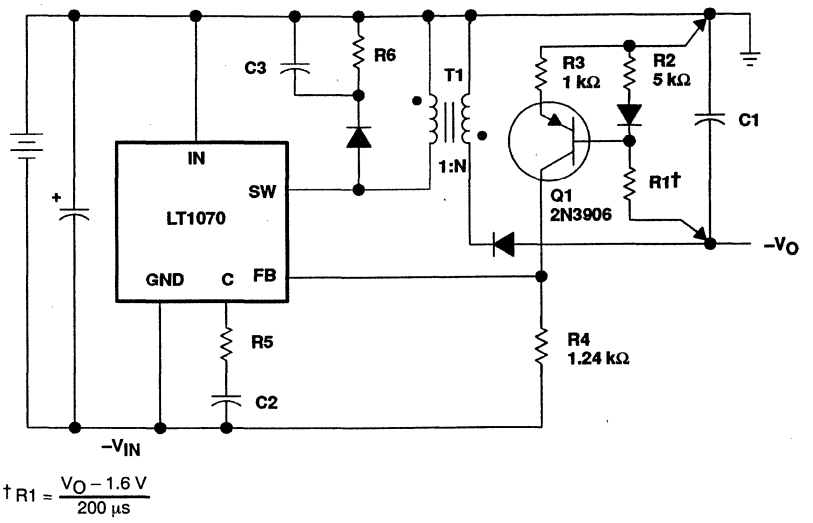


Figure 23. Flyback Converter

APPLICATION INFORMATION



† $R1 = \frac{V_O - 1.6\ V}{200\ \mu s}$

Figure 24. Negative Input – Negative Output Flyback Converter

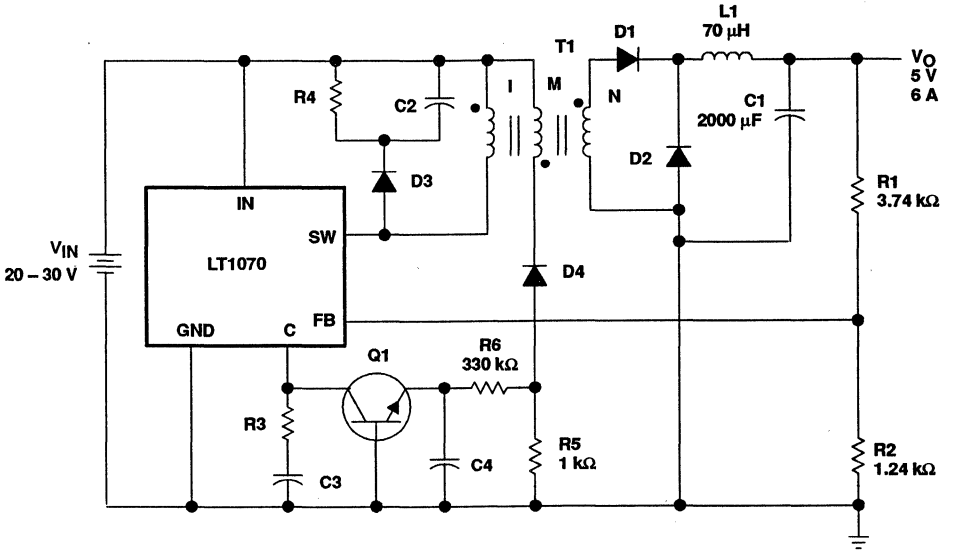


Figure 25. Forward Converter

APPLICATION INFORMATION

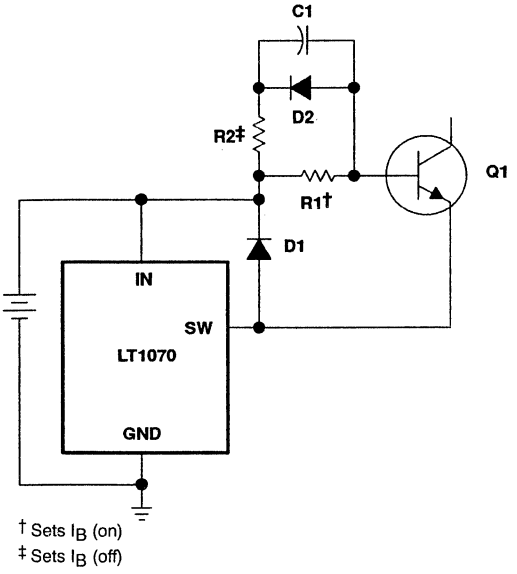


Figure 26. Driving High-Voltage NPN Transistor

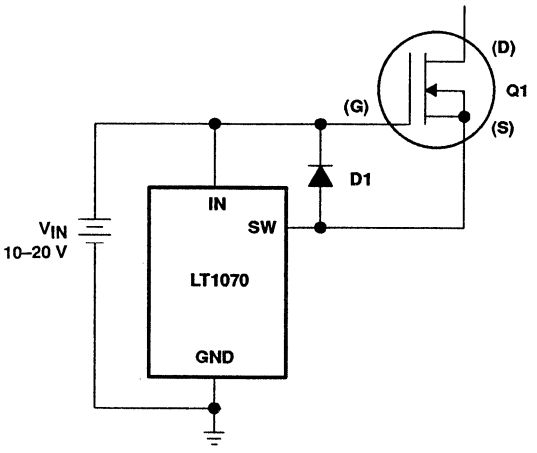


Figure 27. Driving High-Voltage FET

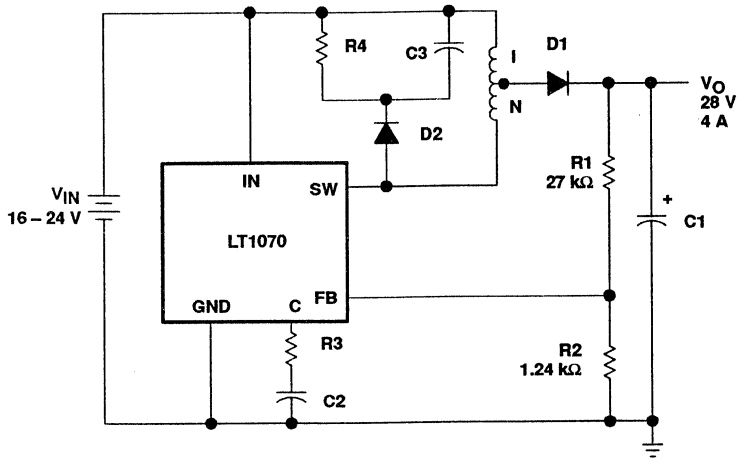


Figure 28. Current-Boosted Boost Converter

APPLICATION INFORMATION

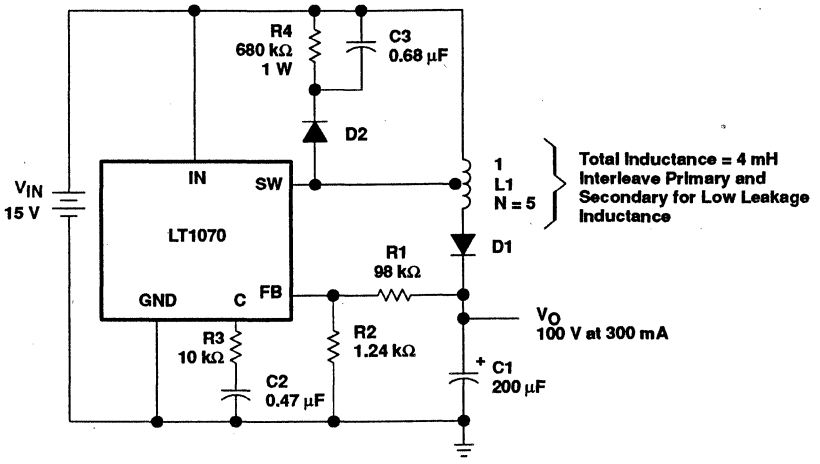
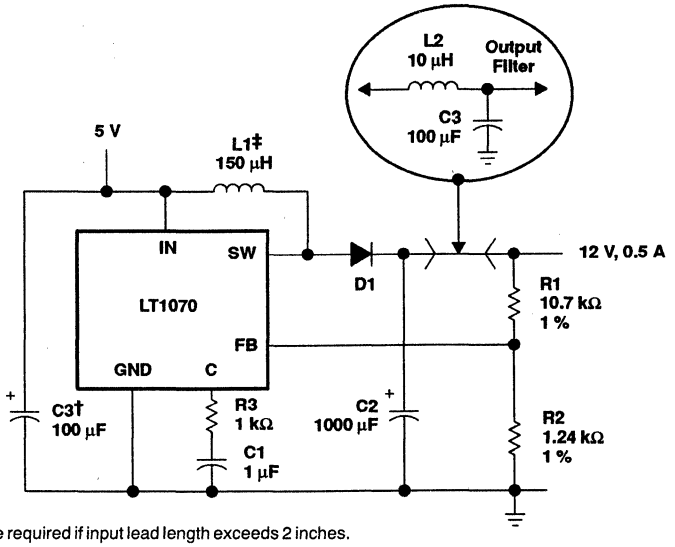


Figure 29. Voltage-Boosted Boost Converter



† Capacitors are required if input lead length exceeds 2 inches.

‡ Pulse Engineering 92113.

Figure 30. Boost Converter (5 V to 12 V)

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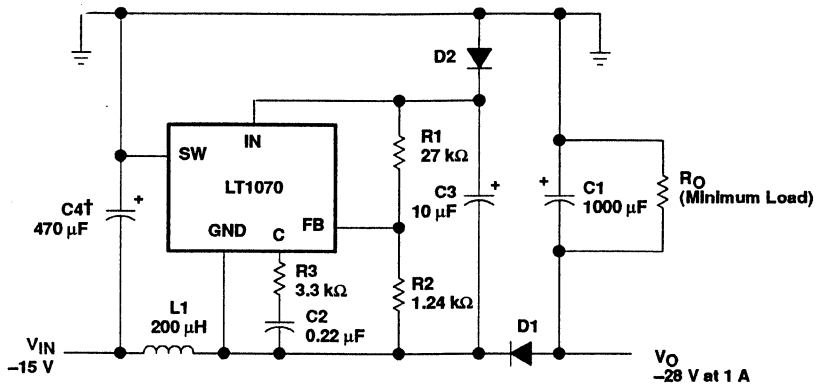
APPLICATION INFORMATION



† Required if input lead length exceeds 2 inches.

Figure 31. Negative Boost Regulator

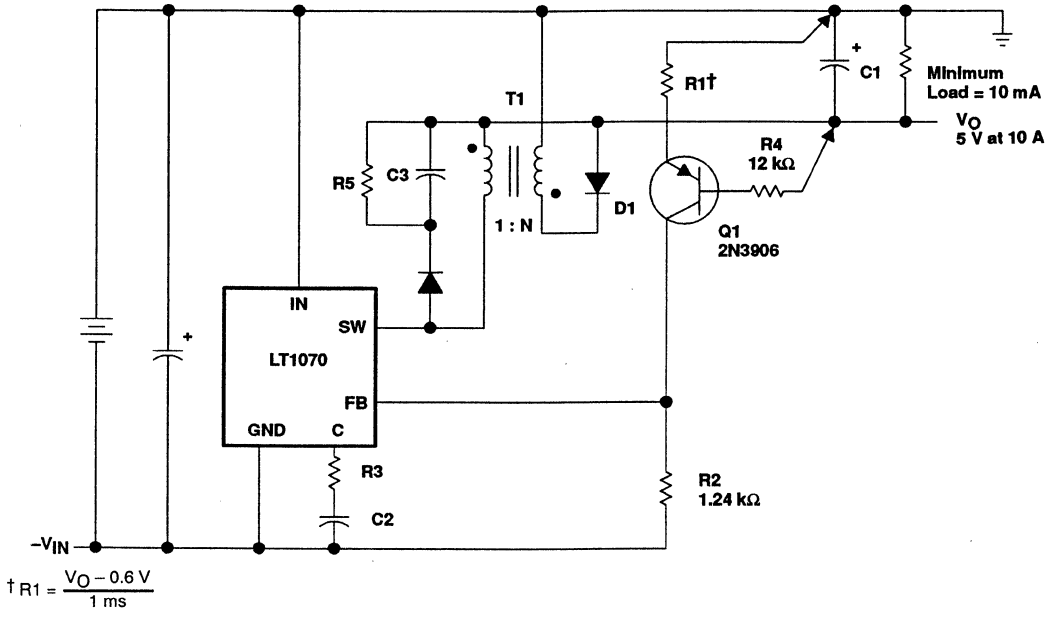
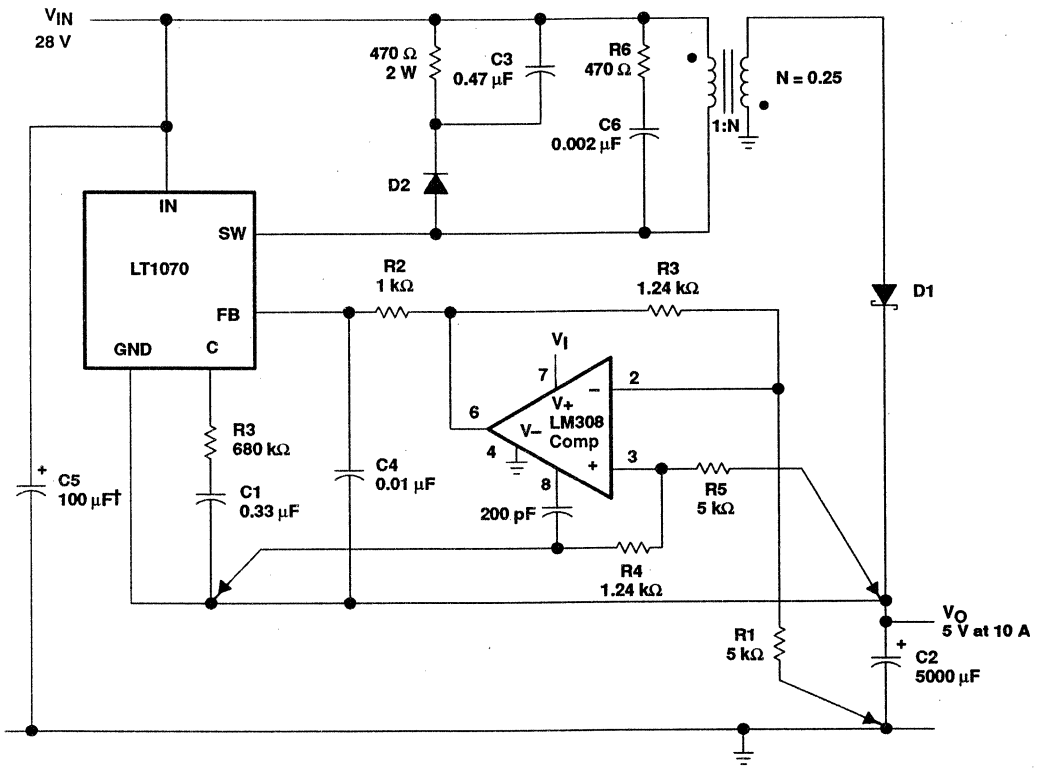


Figure 32. Negative Current-Boosted Buck Converter

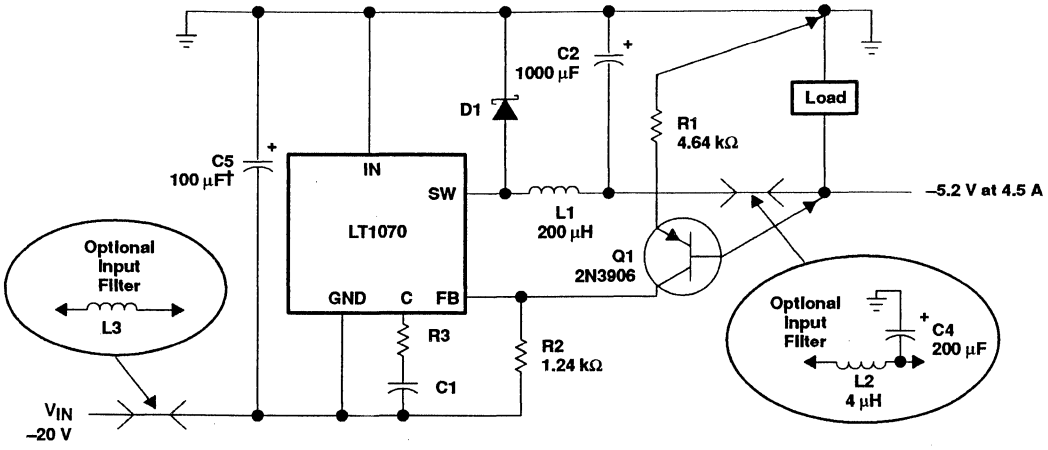
APPLICATION INFORMATION



† Required if input lead length exceeds 2 inches.

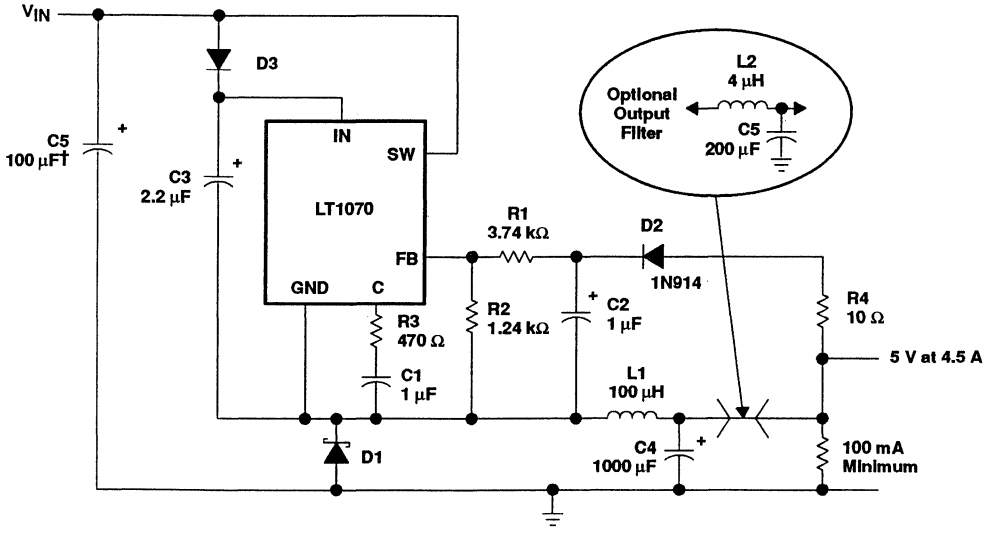
Figure 33. Positive Current-Boosted Buck Converter

APPLICATION INFORMATION



† Required if input lead length exceeds 2 inches.

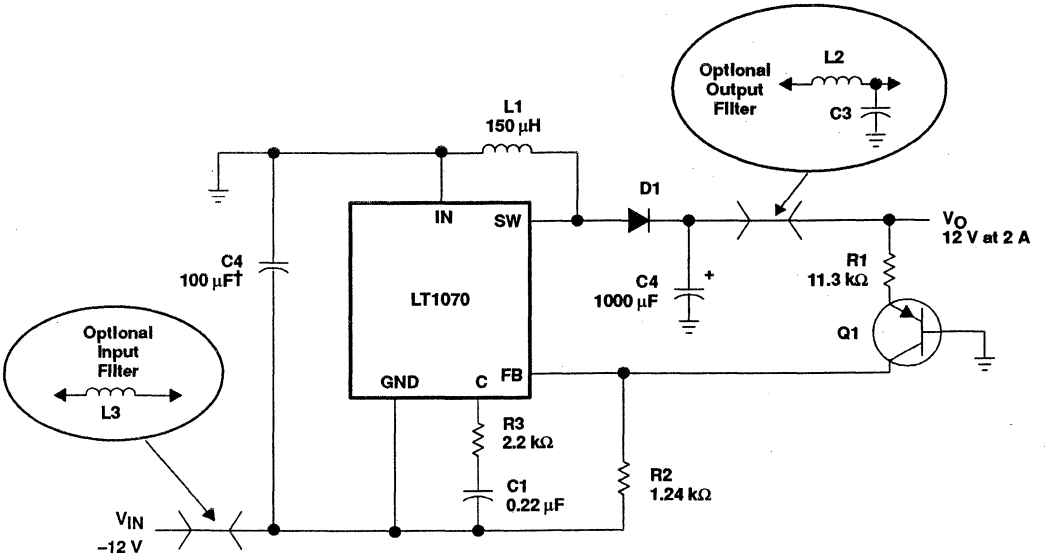
Figure 34. Negative Buck Converter



† Required if input lead length exceeds 2 inches.

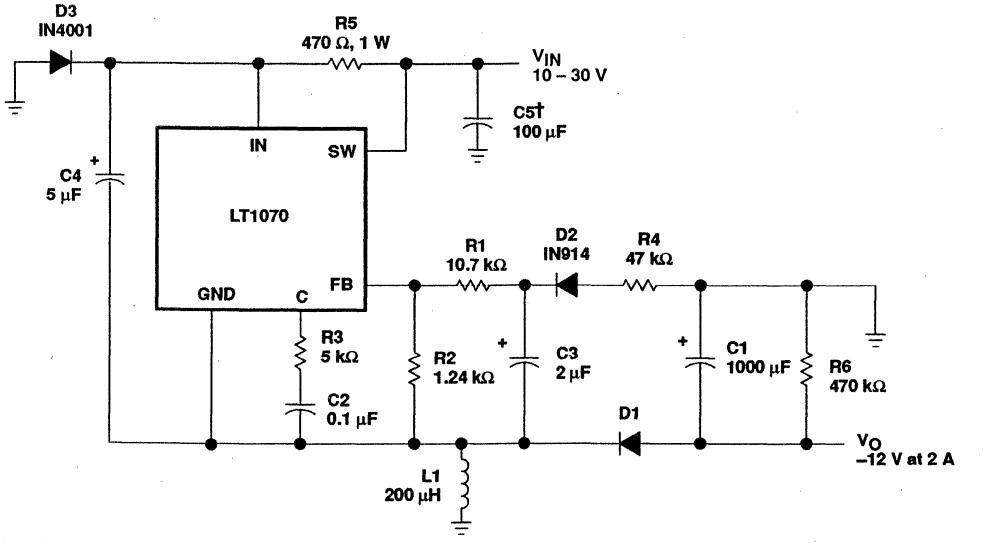
Figure 35. Positive Buck Converter

APPLICATION INFORMATION



† Required if input lead length exceeds 2 inches.

Figure 36. Negative-to-Positive Buck-Boost Converter



† Required if input lead length exceeds 2 inches.

Figure 37. Positive-to-Negative Buck-Book Converter

APPLICATION INFORMATION

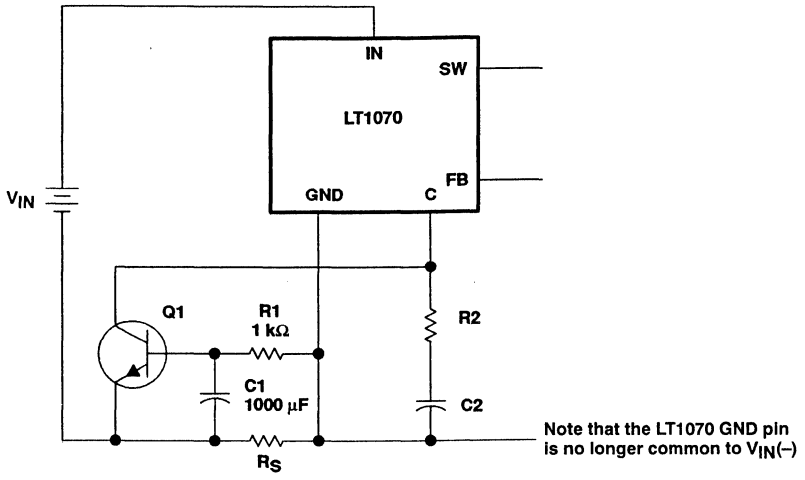


Figure 38. External Current Limit

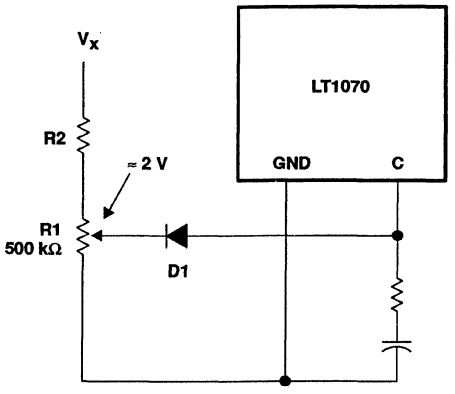
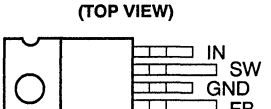


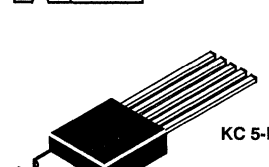
Figure 39. External Current Limit (Adjustable)

D3344, JULY 1989–REVISED AUGUST 1991

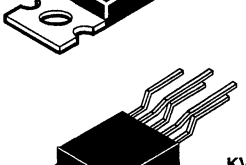
- **Wide Supply-Voltage Range:**
  LT1071HV . . . 3 V to 60 V
  LT1071 . . . 3 V to 40 V
- **Low Quiescent Current . . . 6 mA Typ**
- **Internal 2.5-A Switch**
- **Few External Parts Required**
- **Self-Protected Against Overloads**
- **Operates in Most Switching Configurations**
- **Low Shutdown-Mode Supply Current**
- **Floating Outputs in Flyback-Regulated Mode**
- **Available in Standard KC and KV Packages**
- **Can Be Externally Synchronized**

KC AND KV PACKAGE
(KV Package Used for Illustration)
(TOP VIEW)





KC 5-Lead



KV 5-Lead

AVAILABLE OPTIONS

T_J	MAX INPUT VOLTAGE	KC PACKAGE	KV PACKAGE
0°C to	60 V	LT1071HVCKC	LT1071HVCKV
100°C	40 V	LT1071CKC	LT1071CKV
−40°C to	60 V	LT1071HVIKC	LT1071HVIKV
125°C	40 V	LT1071IKC	LT1071IKV

description

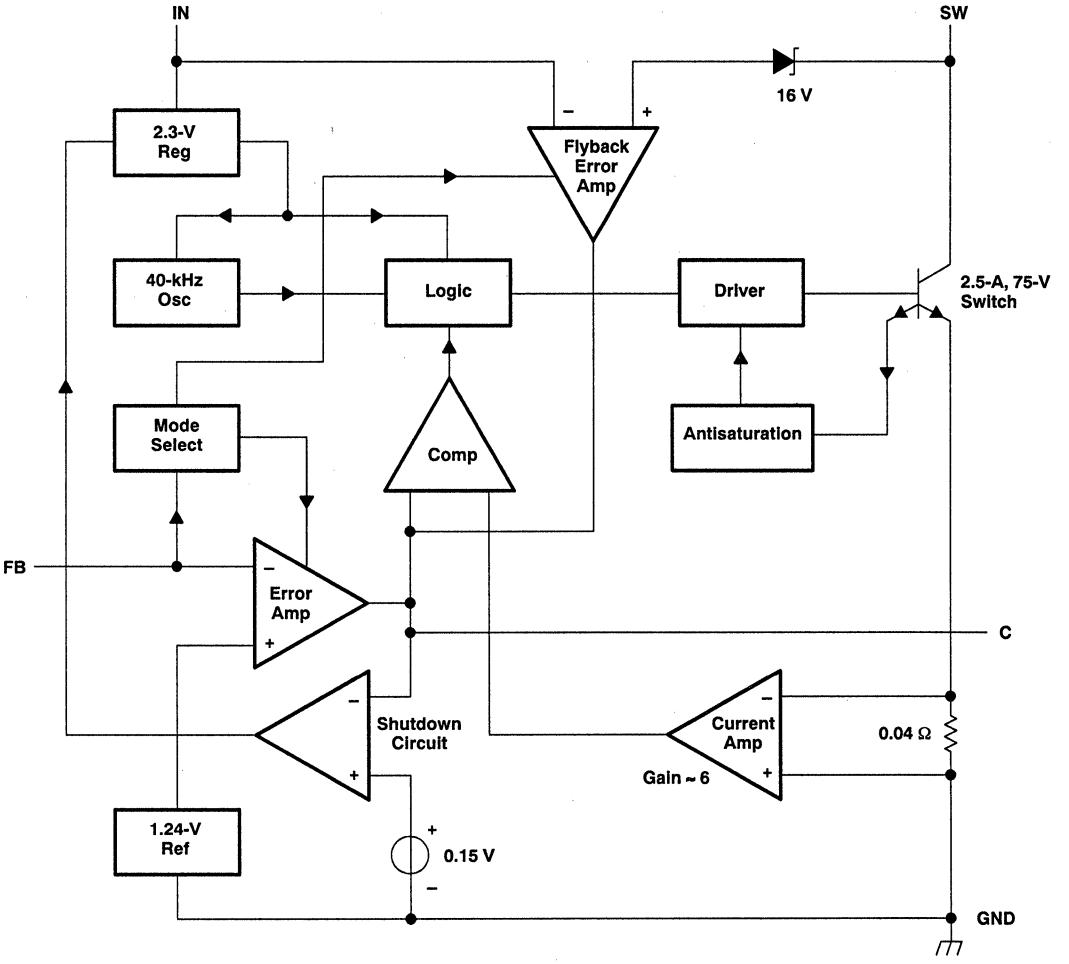
The LT1071 is a monolithic, high-efficiency switching regulator. It can be operated in all standard switching configurations including: step-down (buck), step-up (boost), flyback, forward, inverting, and Cuk†. A high-current, high-efficiency switch is included in the package along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1071 to be built in a standard 5-pin KC or KV package. This makes it extremely easy to use and provides reliable operation similar to that obtained with 3-pin linear regulators.

The LT1071 operates with supply voltages from 3 V to 40 V. The LT1071HV, a high-voltage version of the LT1071, operates with supply voltages from 3 V to 60 V. These devices draw only 6 mA of quiescent current, deliver load power up to 100 W with no external power devices, and by utilizing current-mode switching techniques, provide excellent ac and dc input and output regulation.

The LT1071 is much easier to use than the low-power control chips that are presently available and has many unique features that are not found on these chips. It uses an adaptive saturation-preventing switch drive to allow very-wide-ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional flyback-regulation mode built into the LT1071 without using optocouplers or extra transformer windings.

† A boost-buck-derived regulator circuit patented by Slobodan Ćuk.

functional block diagram



Resistor value shown is nominal.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Supply voltage, V_{IN} (see Note 1): LT1071 ..... 40 V
LT1071HV ..... 60 V
Switch output voltage: LT1071 ..... 65 V
LT1071HV ..... 75 V
Feedback input voltage, V_{FB} (transient, 1 ms) ..... ±15 V
Continuous total dissipation ..... See Dissipation Rating Tables 1 and 2
Operating virtual-junction temperature range: LT1071C, LT1071HVC ..... 0°C to 125°C
LT1071I, LT1071HVI ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

NOTE 1: Minimum switch-on time for the LT1071 in current limit is ≈ 1 μs. This limits the maximum input voltage during short-circuit conditions, in the step-down and inverting modes only, to ≈ 35 V. Normal (unshorted) conditions are not affected. If the LT1071 is being operated in the step-down or inverting mode at high input voltages and short-circuit conditions are expected, a resistor must be placed in series with the inductor.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
KC	2000 mW	16 mW/°C	400 mW
KV	2000 mW	16 mW/°C	400 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 70°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 70°C$	$T_C = 125°C$ POWER RATING
KC	20 W	250 mW/°C	6.25 W
KV	20 W	250 mW/°C	6.25 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_{IN}	LT1071C, LT1071I	3	40	V
	LT1071HVC, LT1071HVI	3	60	
Virtual-junction temperature, T_J	LT1071C, LT1071HVC	0	100	°C
	LT1071I, LT1071HVI	−40	125	

electrical characteristics at specified virtual junction temperature, V_{IN} = 15 V, V_{FB} = V_{ref} with SW output open (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
V_{ref}	Output voltage	Measured at FB input,	V_C = 0.6 V	25°C	1.224	1.244	1.264	V
				Full range	1.214		1.274	
	Input regulation	V_{IN} = 3 V to MAX,	V_C = 0.6 V	Full range			0.03	%/V

error amplifier section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
I_{FB}	Feedback input current	V_{FB} = V_{ref}		25°C		350	750	nA
				Full range			1100	
g_m	Transconductance	ΔI_C = ±25 µA		25°C	3000	4400	6000	µmho
				Full range	2400		7000	
	Source current	V_C = 1.5 V,	V_{FB} = 0.8 V	25°C	150	200	350	µA
				Full range	120		400	
	Sink current	V_C = 1.5 V,	V_{FB} = 1.5 V	25°C	150	200	350	µA
				Full range	120		400	
$V_{O(C)}$	Output voltage	High state,	V_{FB} = 1 V	25°C	1.8		2.3	V
		Low state,	V_{FB} = 1.5 V		0.25	0.38	0.52	
A_V	Voltage amplication	V_C = 0.7 V to 1.4 V		Full range	500	800	2000	V/V
$V_{T(C)}$	Control threshold voltage	Duty cycle = 0		25°C	0.8	0.9	1.08	V
				Full range	0.6		1.25	

flyback amplifier section

PARAMETER		TEST CONDITIONS†			T_J‡	MIN	TYP§	MAX	UNIT
$V_{T(FB)}$	Flyback threshold voltage	I_{FB} = 50 µA			25°C	0.4	0.45	0.54	V
V_Z	Flyback reference	I_{FB} = 50 µA,	I_C = –1 to +1 µA,	V_C = 0.6 V	25°C	15	16.3	17.6	V
					Full range	14		18	
ΔV_Z	Change in flyback reference	I_{FB} = 0.05 to 1 mA,	I_C = –1 to +1 µA,	V_C = 0.6 V	25°C	4.5	6.8	8.5	V
	Flyback reference input regulation	I_{FB} = 50 µA, I_C = –1 to +1 µA,	V_{IN} = 3 V to MAX, V_C = 0.6 V		25°C		0.01	0.03	%/V
g_m	Transconductance	I_{FB} = 50 µA,	$\Delta I_C \leq \pm 10$ µA		25°C	150	300	500	µmho
	Sink or source current	V_C = 1.5 V,	I_{FB} = 50 µA,	Source	Full range	15	32	50	µA
		$V_{(SW)} = V_Z + V_{IN} \pm 1$ V		Sink		25	40	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1071C and LT1071HVC and –40°C to 125°C for LT1071I and LT1071HVI.
§ All typical values are T_A = 25°C.

electrical characteristics at specified virtual junction temperature, V_{IN} = 15 V, V_{FB} = V_{ref} with SW output open (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS†			T_J‡	MIN	TYP§	MAX	UNIT
$V_{(BR)SW}$	Switch breakdown voltage	V_{FB} = 1.5 V, I_{SW} = 5 mA	V_{IN} = 3 V to MAX,	LT1071	Full range	65			V
				LT1071HV		75			
Ron	Switch on-state resistance	V_{FB} = 0.8 V,	I_{SW} = 2 A		Full range		0.3	0.5	Ω
g_m	Control-to-switch transconductance				25°C		4		mho
$I_{SW(lim)}$	Switch current limit	V_{FB} = 0.8 V, See Note 2	Duty cycle ≤ 50%		≥25°C	2.5		5	A
			Duty cycle ≤ 50%		<25°C	2.5		5.5	
			Duty cycle = 80%		Full range	2		5	
$\Delta I_{IN}/\Delta I_{SW}$	Input current increase during switch turn-on	V_{FB} = 0.8 V			25°C		25	35	mA/A
f	Frequency				25°C	35	40	45	kHz
					Full range	33		47	
	Maximum duty cycle	V_{FB} = 1 V			25°C	90%	92%	97%	
t_d	Flyback sense delay time				25°C		1.5		μs

shutdown section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$I_{IN(off)}$	Shutdown mode input current	V_{IN} = 3 V to MAX,	V_C = 0.05 V	25°C		100	250	μA
$V_{C(off)}$	Control threshold voltage	V_{IN} = 3 V to MAX,		25°C	100	150	250	mV
				Full range	50		300	

total device

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$V_{IN(min)}$	Minimum input voltage			Full range		2.6	3	V
I_{IN}	Input current	V_{IN} = 3 V to MAX,	V_C = 0.6 V	25°C		6	9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1071C and LT1071HVC and −40°C to 125°C for LT1071I and LT1071HVI.
§ All typical values are T_A = 25°C.
NOTE 2: For duty cycles between 50% and 80%, minimum switch output current is given by $I_{SW(lim)}$ = 1.67 (2-duty cycle).

theory of operation

The LT1071 is a current-mode switcher. This means that the switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the functional block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when the switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set the current trip level. This technique has several advantages. First, it has immediate response to input-voltage variations, which is unlike ordinary switchers that have poor input transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy-storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input-voltage or output-load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3-V supply for all internal circuitry on the LT1071. This low-dropout design allows input voltage to vary from 3 V to 60 V with virtually no change in device performance. A 40-kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn off of the switch.

A 1.2-V band-gap reference biases the positive input of the error amplifier. The negative input is brought out for output-voltage sensing. This feedback pin has a second function when pulled low with an external resistor. It programs the LT1071 to disconnect the main error-amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1071 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback-topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1071 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation, this pin sits at a voltage between 0.9 V (low output current) and 2 V (high output current). The error amplifiers are current-output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft start. Switch duty cycle goes to zero if the C pin is pulled to ground through a diode. This places the LT1071 in an idle mode. Pulling the C pin below 0.15 V causes total regulator shutdown, with only 50-μA supply current for shutdown-circuitry biasing.

TYPICAL CHARACTERISTICS

table of graphs

				FIGURE
P_{OM}	Maximum output power	vs	Input voltage	1
f	Switching frequency	vs	Junction temperature	2
V_{ref}	Reference voltage	vs	Junction temperature	2
	Reference voltage change	vs	Input voltage	3
I_{FB}	Feedback input current	vs	Junction temperature	4
g_m	Error amplifier transconductance	vs	Junction temperature	5
g_m	Error amplifier transconductance	vs	Frequency	6
	Error amplifier phase shift	vs	Frequency	6
I_C	Control current	vs	Control voltage	7
$V_{T(FB)}$	Normal-flyback-mode threshold voltage	vs	Junction temperature	8
I_{FB}	Feedback input current	vs	Junction temperature	8
V_Z	Flyback reference voltage	vs	Junction temperature	9
t_d	Flyback sense delay time	vs	Junction temperature	10
$I_{O(SW)}$	Switch (output with switch off) current	vs	Switch voltage	11
	Driver base current	vs	Switch output current	12
$V_{sat(SW)}$	Switch saturation voltage	vs	Switch output current	13
$I_{O(SW)}$	Switch output current limit	vs	Duty cycle	14
	Maximum duty cycle	vs	Junction temperature	15
I_{IN}	Shutdown-mode input current	vs	Control threshold voltage	16
I_{IN}	Shutdown-Mode input current	vs	Input voltage	17
$V_{T(C)}$	Shutdown-mode control threshold voltage	vs	Junction temperature	18
$I_{T(C)}$	Shutdown-mode control threshold current	vs	Junction temperature	18
V_{FB}	Feedback input voltage	vs	Feedback input current	19
	Minimum input voltage	vs	Junction temperature	20
I_{IN}	Input current	vs	Junction temperature	21
I_{IN}	Input current	vs	Input voltage	22

table of application circuits

APPLICATION	FIGURE
Totally isolated converter	23
Boost converter (5 V to 12 V)	24

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT POWER
vs
INPUT VOLTAGE

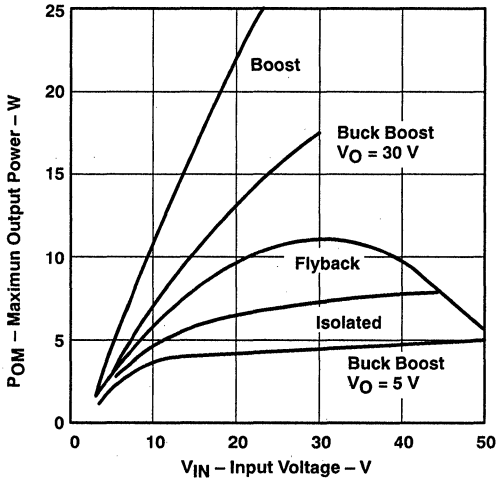


Figure 1

REFERENCE VOLTAGE AND
SWITCHING FREQUENCY
vs
JUNCTION TEMPERATURE

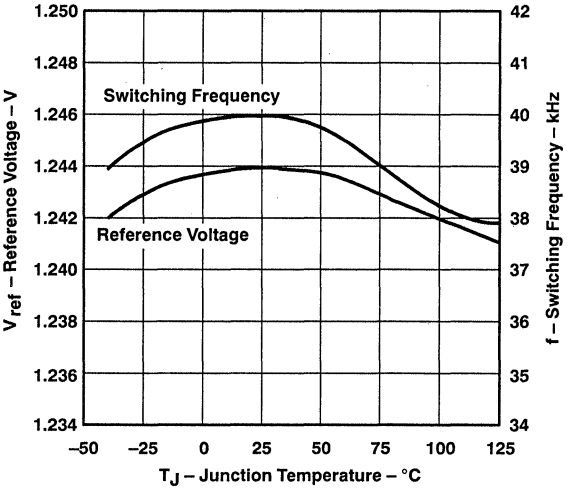


Figure 2

REFERENCE VOLTAGE INPUT REGULATION

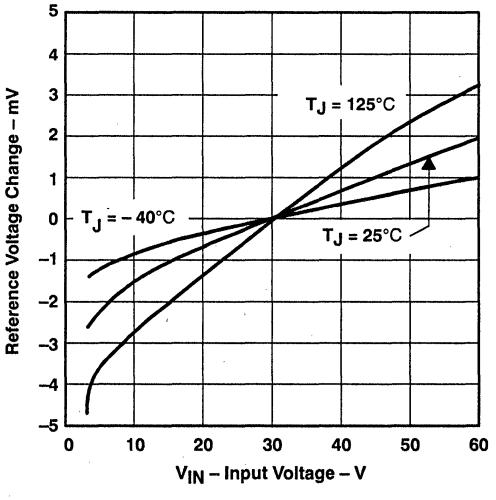


Figure 3

FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

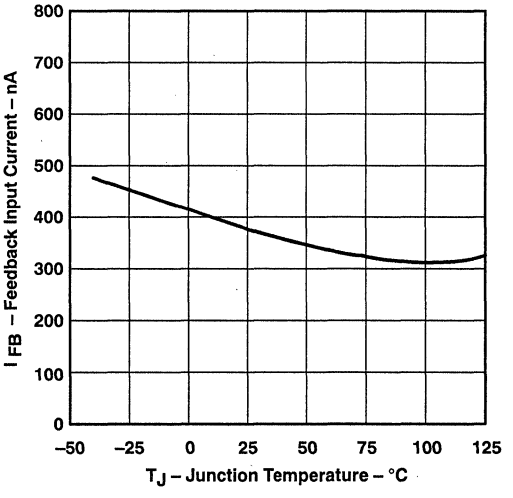


Figure 4

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER TRANSDUCTANCE
vs
JUNCTION TEMPERATURE

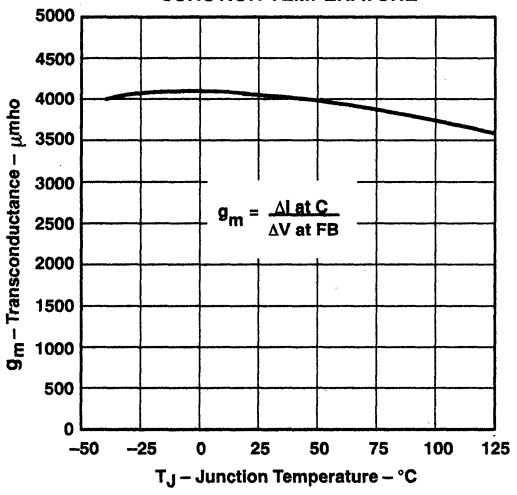


Figure 5

ERROR AMPLIFIER TRANSCONDUCTANCE
AND PHASE SHIFT
vs
FREQUENCY

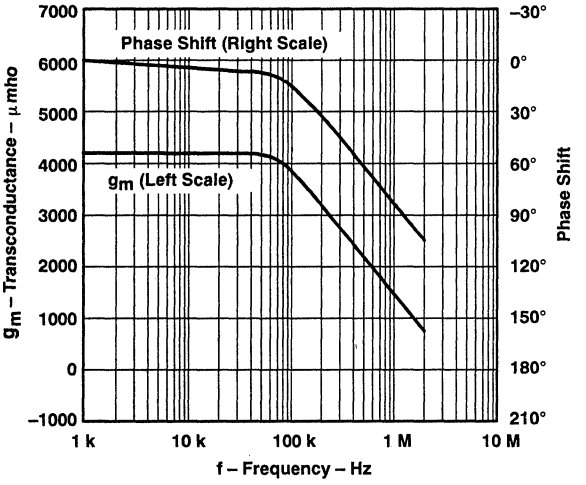


Figure 6

CONTROL CURRENT
vs
CONTROL VOLTAGE

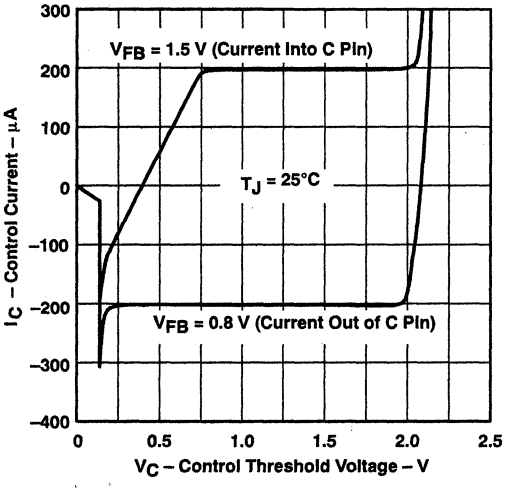


Figure 7

NORMAL-FLYBACK-MODE THRESHOLD VOLTAGE
AND FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

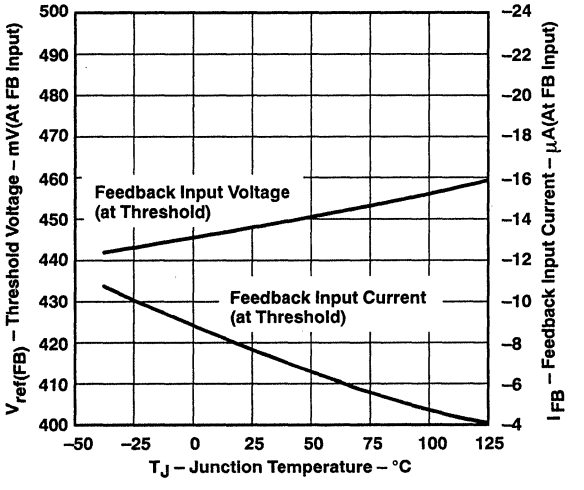


Figure 8

TYPICAL CHARACTERISTICS

FLYBACK MODE REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

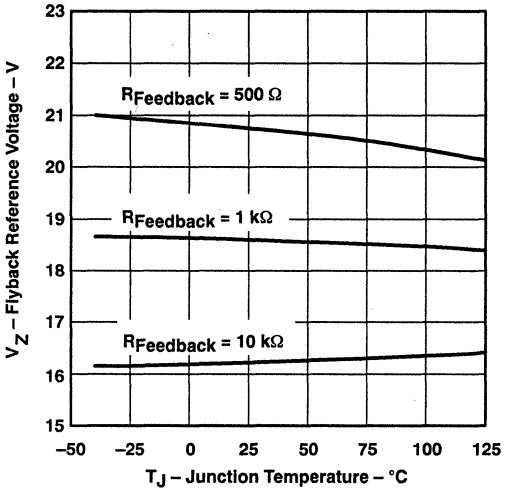


Figure 9

FLYBACK SENSE DELAY TIME
vs
JUNCTION TEMPERATURE

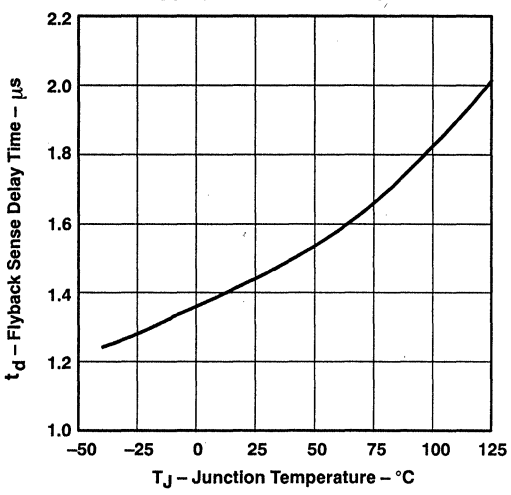


Figure 10

SWITCH OUTPUT CURRENT
vs
SWITCH VOLTAGE AND INPUT VOLTAGE
(WITH SWITCH OFF)

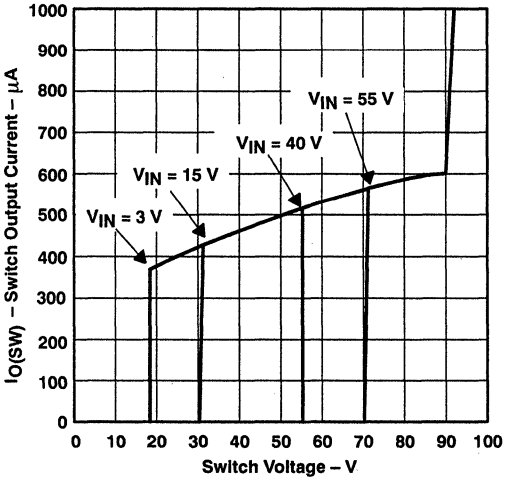


Figure 11

DRIVER BASE CURRENT†
vs
SWITCH OUTPUT CURRENT

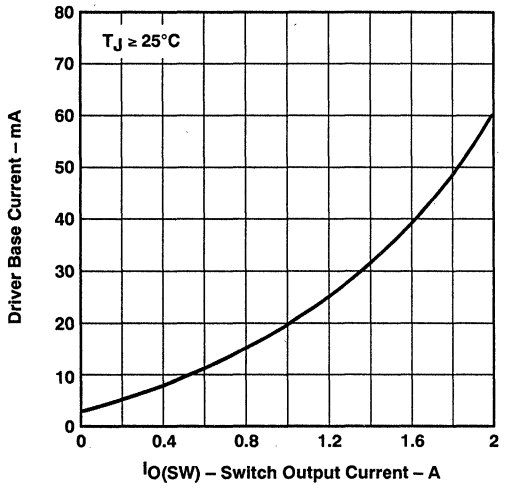


Figure 12

† Average power driver base current is found by multiplying driver base current by duty cycle plus quiescent current.

TYPICAL CHARACTERISTICS

SWITCH SATURATION VOLTAGE
vs
SWITCH CURRENT

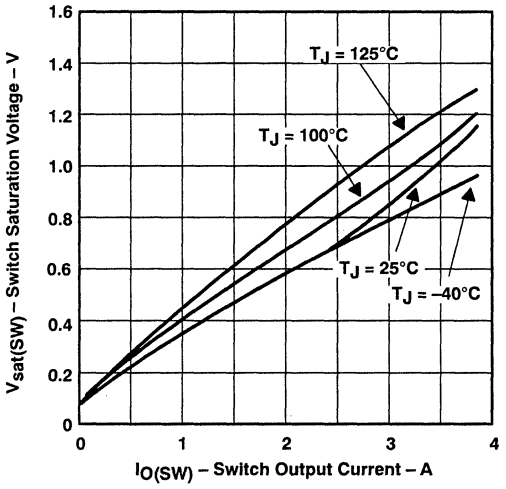


Figure 13

SWITCH OUTPUT CURRENT LIMIT
vs
DUTY CYCLE

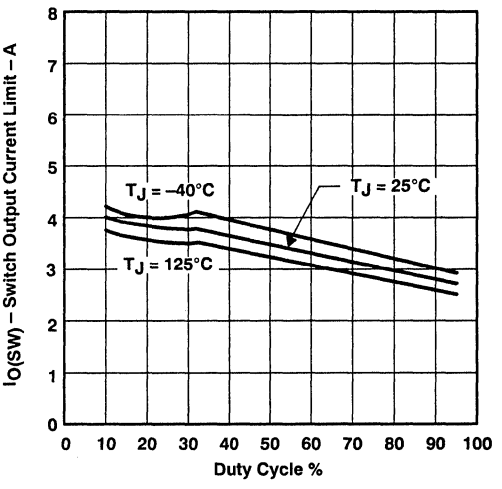


Figure 14

DUTY CYCLE (MAX)
vs
JUNCTION TEMPERATURE

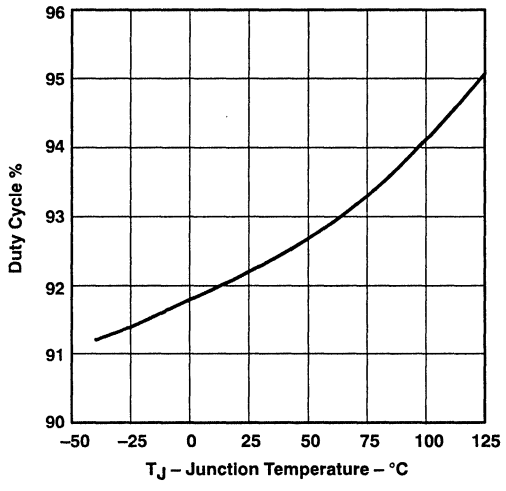


Figure 15

SHUTDOWN MODE
INPUT CURRENT
vs
CONTROL THRESHOLD VOLTAGE

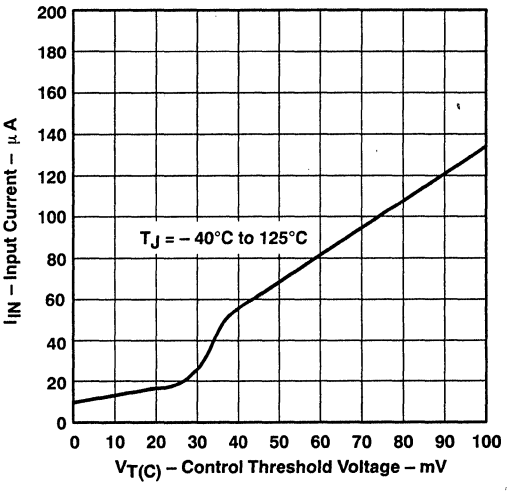


Figure 16

TYPICAL CHARACTERISTICS

SHUTDOWN MODE
INPUT CURRENT
vs
INPUT VOLTAGE

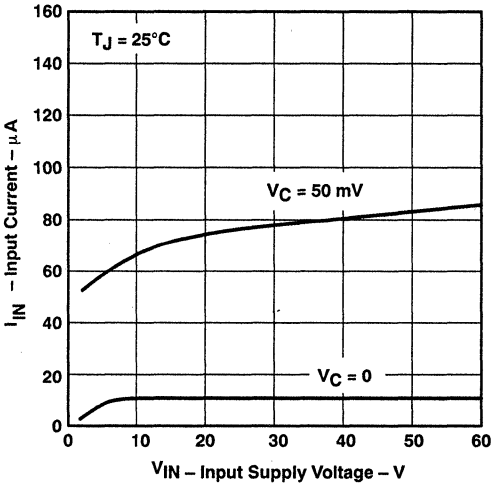


Figure 17

SHUTDOWN MODE
CONTROL THRESHOLD VOLTAGE AND CURRENT
vs
JUNCTION TEMPERATURE

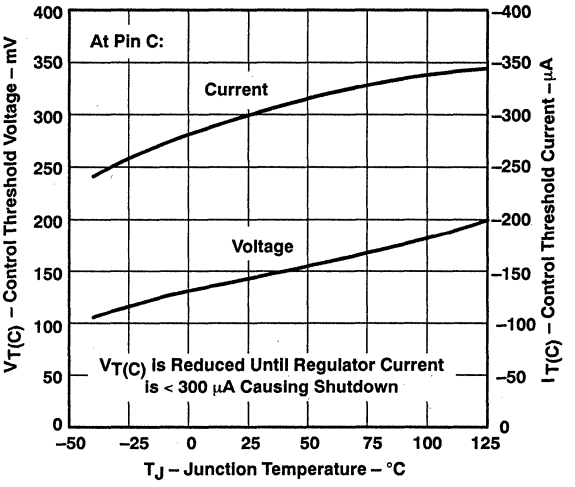


Figure 18

FEEDBACK INPUT VOLTAGE
vs
FEEDBACK INPUT CURRENT

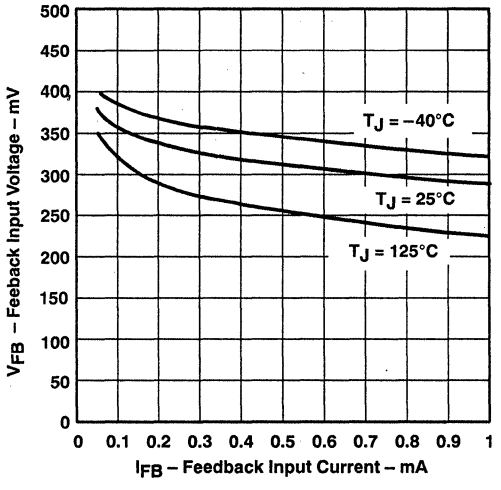


Figure 19

MINIMUM INPUT VOLTAGE
vs
JUNCTION TEMPERATURE

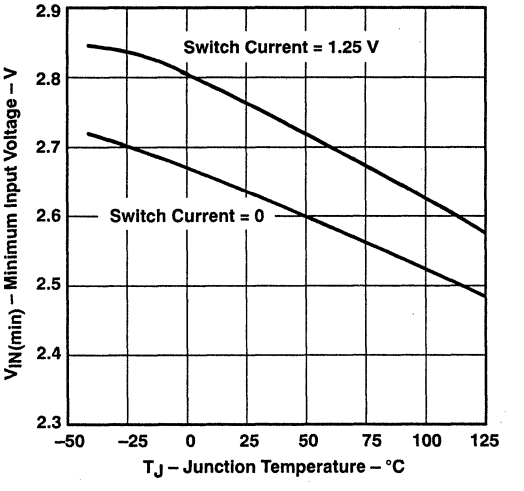


Figure 20

TYPICAL CHARACTERISTICS

**INPUT CURRENT
vs
JUNCTION TEMPERATURE
(SW OUTPUT OPEN)**

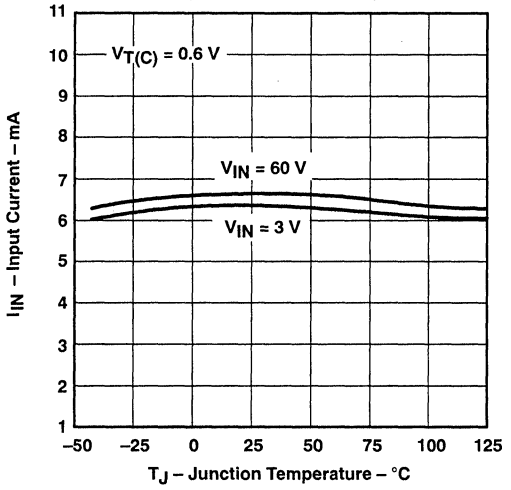
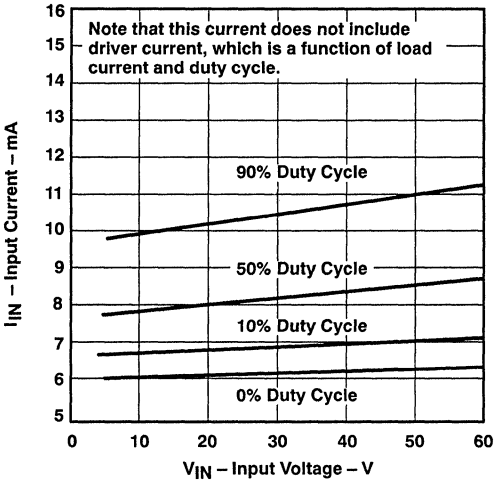


Figure 21

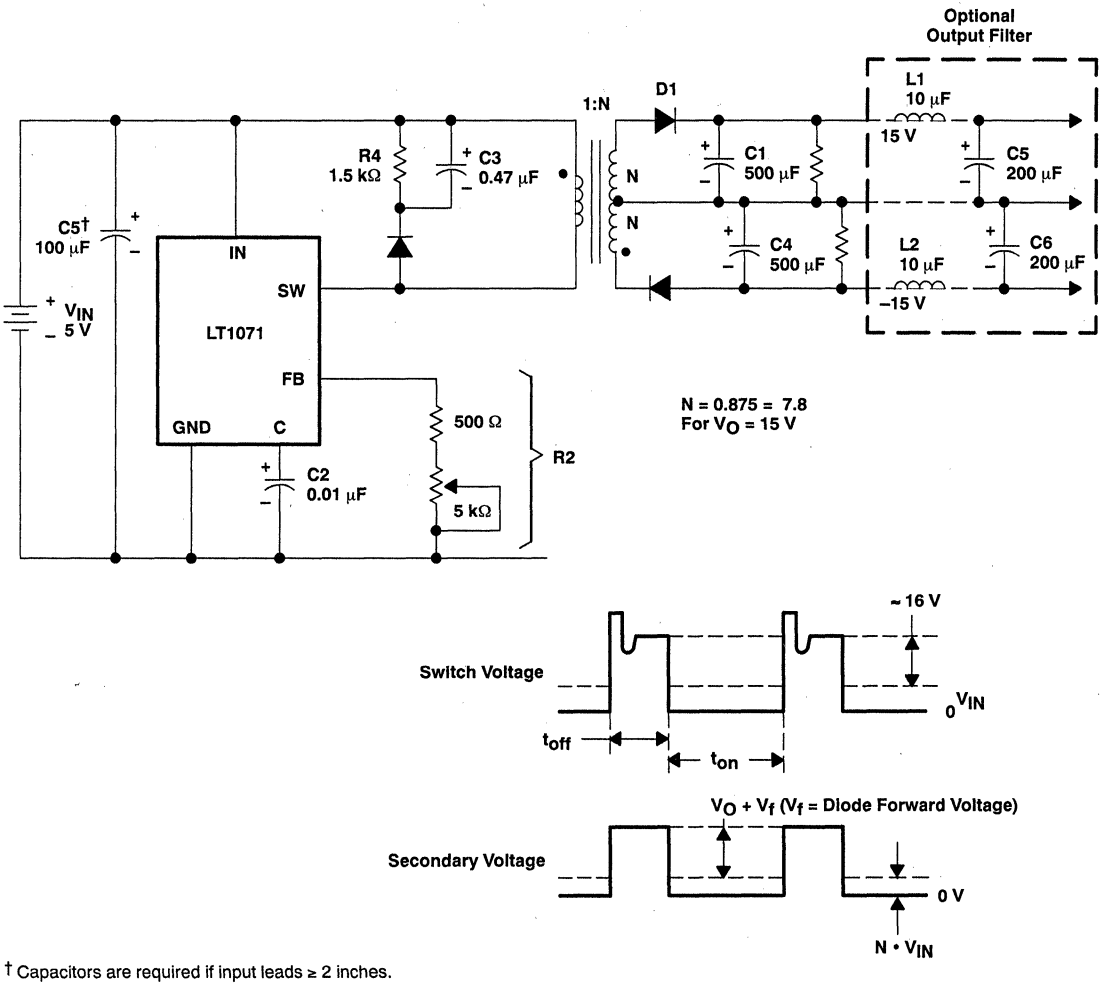
**INPUT CURRENT
vs
INPUT VOLTAGE†**



† Under very low output current conditions, duty cycle for most circuits will approach 10% or less.

Figure 22

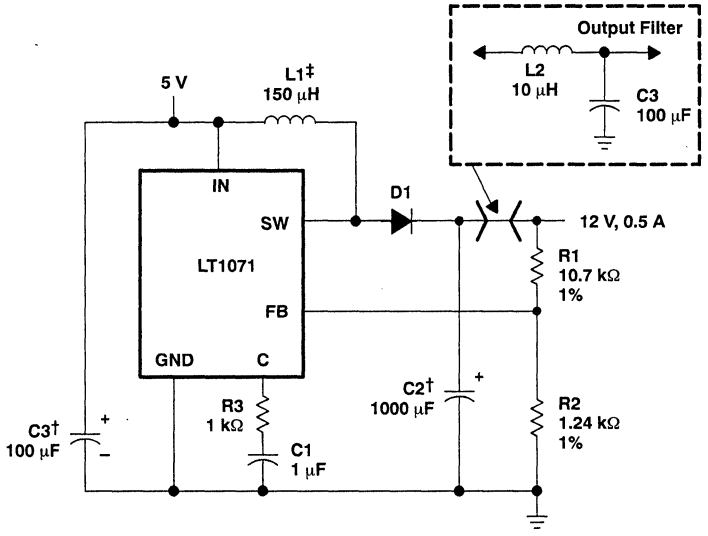
APPLICATION INFORMATION



† Capacitors are required if input leads ≥ 2 inches.

Figure 23. Totally Isolated Converter

APPLICATION INFORMATION



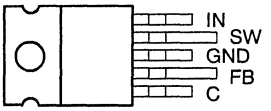
† Capacitors are required if input leads ≥ 2 inches.
‡ Pulse Engineering 92113

Figure 24. Boost Converter (5 V to 12 V)

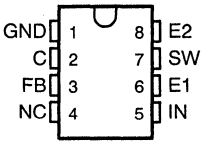
D3369, NOVEMBER 1989–REVISED AUGUST 1991

- **Wide Supply-Voltage Range:**
  LT1072HV . . . 3 V to 60 V
  LT1072 . . . 3 V to 40 V
- **Low Quiescent Current . . . 6 mA Typ**
- **Internal 1.25-A Switch**
- **Few External Parts Required**
- **Self-Protected Against Overloads**
- **Operates in Most Switching Configurations**
- **Low Shutdown-Mode Supply Current**
- **Floating Outputs in Flyback-Regulated Mode**
- **Can Be Externally Synchronized**

KC AND KV PACKAGE
(KV Package Used for Illustration)
(TOP VIEW)



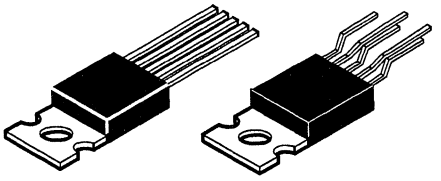
P Package
(TOP VIEW)



NC = No internal connection

AVAILABLE OPTIONS

T_J	MAX INPUT VOLTAGE	KC PACKAGE	KV PACKAGE	P PACKAGE
0°C to	60 V	LT1072HVCKC	LT1072HVCKV	LT1072HVCP
100°C	40 V	LT1072CKC	LT1072CKV	LT1072CP
−40°C to	60 V	LT1072HVIKC	LT1072HVIKV	LT1072HVIP
125°C	40 V	LT1072IKC	LT1072IKV	LT1072IP



KC 5-Lead **KV 5-Lead**

description

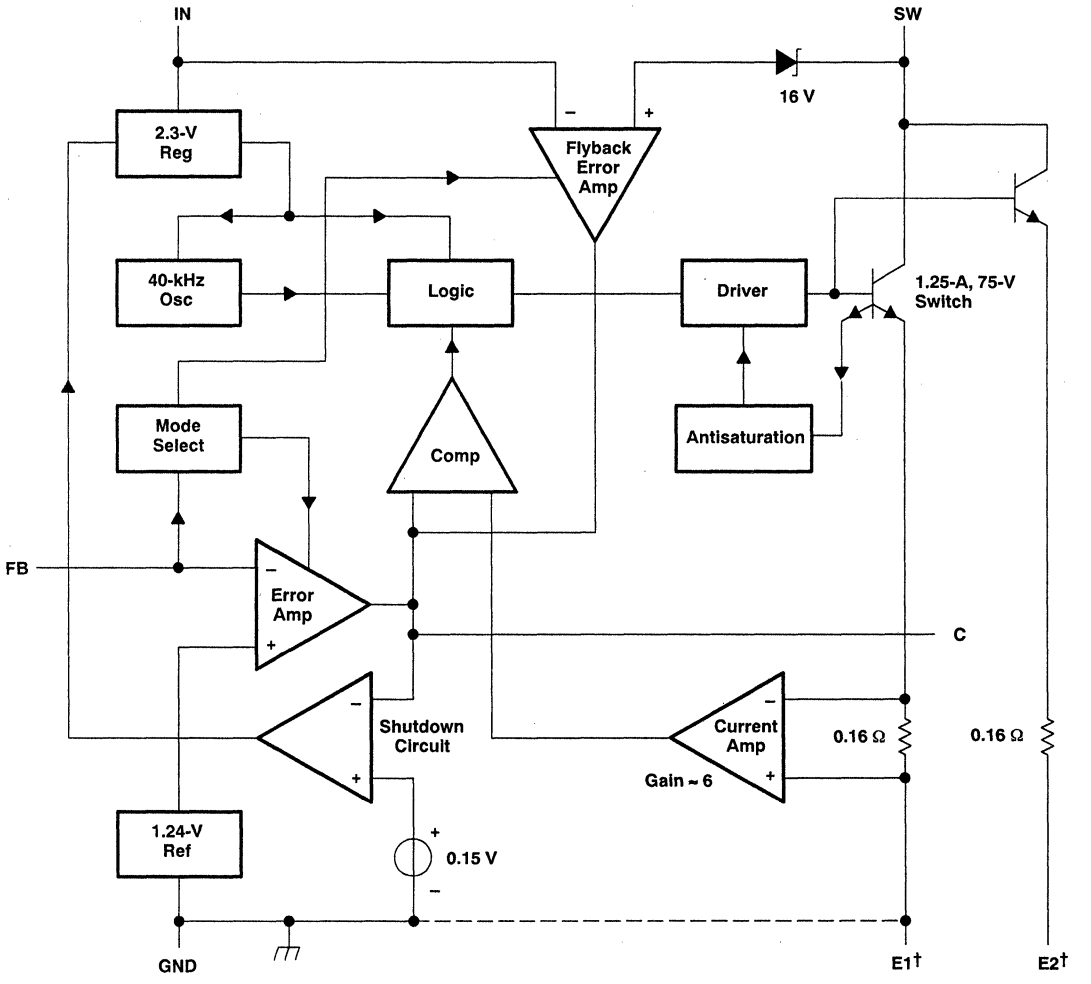
The LT1072 is a monolithic, high-efficiency switching regulator. It can be operated in all standard switching configurations including: step-down (buck), step-up (boost), flyback, forward, inverting, and Cuk†. A high-current, high-efficiency switch is included in the package along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1072 to be built in standard 5-pin KC or a KV packages and the 8-pin P package. This makes it extremely easy to use and provides reliable operation similar to that obtained with 3-pin linear regulators.

The LT1072 operates with supply voltages from 3 V to 40 V. The LT1072HV, a high-voltage version of the LT1072, operates with supply voltages from 3 V to 60 V. These devices draw only 6 mA of quiescent current, deliver load power up to 20 W with no external power devices, and by utilizing current-mode switching techniques, provide excellent ac and dc input and output regulation.

The LT1072 is much easier to use than the low-power control chips that are presently available and has many unique features that are not found on these chips. It uses an adaptive saturation-preventing switch drive to allow very-wide-ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional flyback-regulation mode built into the LT1072 without using optocouplers or extra transformer windings.

† A boost-buck-derived regulator circuit patented by Slobodan Ćuk.

functional block diagram



All resistor values shown are nominal.

† Always connect E1 to ground when using the P package. The emitters (E1 and E2) are tied internally to ground on the KC and KV packages.

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Supply voltage, V_{IN} (see Note 1): LT1072 ..... 40 V
LT1072HV ..... 60 V
Switch output voltage: LT1072 ..... 65 V
LT1072HV ..... 75 V
Feedback input voltage, V_{FB} (transient, 1 ms) ..... ±15 V
Continuous total dissipation ..... See Dissipation Rating Tables 1 and 2
Operating virtual-junction temperature range: LT1072C, LT1072HVC ..... 0°C to 125°C
LT1072I, LT1072HVI ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Minimum switch-on time for the LT1072 in current limit is ≈ 0.7 μs. This limits the maximum input voltage during short-circuit conditions, in the step-down and inverting modes only, to ≈ 40 V. Normal (unshorted) conditions are not affected. If the LT1072 is being operated in the step-down or inverting mode at high input voltages and short-circuit conditions are expected, a resistor must be placed in series with the inductor.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
KC	2000 mW	16 mW/°C	400 mW
KV	2000 mW	16 mW/°C	400 mW
P	1000 mW	8 mW/°C	200 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 70°C$	$T_C = 125°C$ POWER RATING
KC	20 W	250 mW/°C	6.25 W
KV	20 W	250 mW/°C	6.25 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_{IN}	LT1072C, LT1072I	3	40	V
	LT1072HVC, LT1072HVI	3	60	
Virtual-junction temperature, T_J	LT1072C, LT1072HVC	0	100	°C
	LT1072I, LT1072HVI	−40	125	

electrical characteristics at specified virtual junction temperature, V_{IN} = 15 V, V_{FB} = V_{ref} with SW output open (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS†	T_J‡	MIN	TYP§	MAX	UNIT
V_{ref}	Output voltage	Measured at FB input, V_C = 0.6 V	25°C	1.224	1.244	1.264	V
			Full range	1.214		1.274	
	Input regulation	V_{IN} = 3 V to MAX, V_C = 0.6 V	Full range			0.03	%/V

error amplifier section

PARAMETER		TEST CONDITIONS†	T_J‡	MIN	TYP§	MAX	UNIT
I_{FB}	Feedback input current	V_{FB} = V_{ref}	25°C		350	750	nA
			Full range			1100	
g_m	Transconductance	ΔI_C = ±25 µA	25°C	3000	4400	6000	µmho
			Full range	2400		7000	
	Source current	V_C = 1.5 V, V_{FB} = 0.8 V	25°C	150	200	350	µA
			Full range	120		400	
	Sink current	V_C = 1.5 V, V_{FB} = 1.5 V	25°C	150	200	350	µA
			Full range	120		400	
$V_{O(C)}$	Output voltage	High state, V_{FB} = 1 V	25°C	1.8		2.3	V
		Low state, V_{FB} = 1.5 V		0.25	0.38	0.52	
A_V	Voltage amplication	V_C = 0.7 V to 1.4 V	Full range	500	800	2000	V/V
$V_{T(C)}$	Control threshold voltage	Duty cycle = 0	25°C	0.8	0.9	1.08	V
			Full range	0.6		1.25	

flyback amplifier section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$V_{T(FB)}$	Flyback threshold voltage	I_{FB} = 50 µA		25°C	0.4	0.45	0.54	V
V_Z	Flyback reference	I_{FB} = 50 µA, I_C = −1 to +1 µA, V_C = 0.6 V		25°C	15	16.3	17.6	V
				Full range	14		18	
ΔV_Z	Change in flyback reference	I_{FB} = 0.05 to 1 mA, I_C = −1 to +1 µA, V_C = 0.6 V		25°C	4.5	6.8	8.5	V
	Flyback reference input regulation	I_{FB} = 50 µA, I_C = −1 to +1 µA, V_{IN} = 3 V to MAX, V_C = 0.6 V		25°C		0.01	0.03	%/V
g_m	Transconductance	I_{FB} = 50 µA, $\Delta I_C \le \pm 10$ µA		25°C	150	300	500	µmho
	Sink or source current	V_C = 1.5 V, I_{FB} = 50 µA,	Source	Full range	15	32	50	µA
		$V_{(SW)} = V_Z + V_{IN} \pm 1$ V	Sink		25	40	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1072C and LT1072HVC and −40°C to 125°C for LT1072I and LT1072HVI.
§ All typical values are T_A = 25°C.

electrical characteristics at specified virtual junction temperature, V_{IN} = 15 V, V_{FB} = V_{ref} with SW output open (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS†			T_J‡	MIN	TYP§	MAX	UNIT
$V_{(BR)SW}$	Switch breakdown voltage	V_{FB} = 1.5 V, I_{SW} = 5 mA	V_{IN} = 3 V to MAX,	LT1072	Full range	65			V
				LT1072HV		75			
Ron	Switch on-state resistance	V_{FB} = 0.8 V,	I_{SW} = 1.25 mA		Full range		0.6	1	Ω
g_m	Control-to-switch transconductance				25°C		2		mho
$I_{SW(lim)}$	Switch current limit	V_{FB} = 0.8 V, See Note 2	Duty cycle ≤ 50%		≥25°C	1.25		3	A
			Duty cycle ≤ 50%		<25°C	1.25		3.5	
			Duty cycle = 80%		Full range	1		2.5	
$\Delta I_{IN}/\Delta I_{SW}$	Input current increase during switch turn-on	V_{FB} = 0.8 V			25°C		25	35	mA/A
f	Frequency				25°C	35	40	45	kHz
					Full range	33		47	
	Maximum duty cycle	V_{FB} = 1 V			25°C	90%	92%	97%	
t_d	Flyback sense delay time				25°C		1.5		μs

shutdown section

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$I_{IN(off)}$	Shutdown mode input current	V_{IN} = 3 V to MAX,	V_C = 0.05 V	25°C		100	250	μA
$V_{C(off)}$	Control threshold voltage	V_{IN} = 3 V to MAX,		25°C	100	150	250	mV
				Full range	50		300	

total device

PARAMETER		TEST CONDITIONS†		T_J‡	MIN	TYP§	MAX	UNIT
$V_{IN(min)}$	Minimum input voltage			Full range		2.6	3	V
I_{IN}	Input current	V_{IN} = 3 V to MAX,	V_C = 0.6 V	25°C		6	9	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
‡ Full range virtual junction temperature is 0°C to 100°C for LT1072C and LT1072HVC and −40°C to 125°C for LT1072I and LT1072HVI.
§ All typical values are T_A = 25°C.
NOTE 2: For duty cycles between 50% and 80%, minimum switch output current is given by $I_{SW(lim)}$ = 0.833 (2-duty cycle).

theory of operation

The LT1072 is a current-mode switcher. This means that the switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the functional block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when the switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set the current trip level. This technique has several advantages. First, it has immediate response to input-voltage variations, which is unlike ordinary switchers that have poor input transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy-storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input-voltage or output-load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3-V supply for all internal circuitry on the LT1072. This low-dropout design allows input voltage to vary from 3 V to 60 V with virtually no change in device performance. A 40-kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn off of the switch.

A 1.2-V band-gap reference biases the positive input of the error amplifier. The negative input is brought out for output-voltage sensing. This feedback pin has a second function when pulled low with an external resistor. It programs the LT1072 to disconnect the main error-amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1072 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback-topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1072 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation, this pin sits at a voltage between 0.9 V (low output current) and 2 V (high output current). The error amplifiers are current-output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft start. Switch duty cycle goes to zero if the C pin is pulled to ground through a diode. This places the LT1072 in an idle mode. Pulling the C pin below 0.15 V causes total regulator shutdown, with only 50-μA supply current for shutdown-circuitry biasing.

In the P package, the emitters of the power transistors are brought out separately from the ground pin. This eliminates errors due to ground-pin voltage drops and allows the user to reduce the switch-current limit (2:1) by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch on-state resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 100 mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operations, even though dissipation in current-limit mode will *decrease*.

TYPICAL CHARACTERISTICS

table of graphs

				FIGURE
P_{OM}	Maximum output power	vs	Input voltage	1
V_{ref}	Reference voltage	vs	Junction temperature	2
f	Switching frequency	vs	Junction temperature	2
	Reference voltage change	vs	Input voltage	3
I_{FB}	Feedback input current	vs	Junction temperature	4
g_m	Error amplifier transconductance	vs	Junction temperature	5
g_m	Error amplifier transconductance	vs	Frequency	6
	Error amplifier phase shift	vs	Frequency	6
I_C	Control current	vs	Control voltage	7
$V_{T(FB)}$	Normal/flyback mode threshold voltage	vs	Junction temperature	8
I_{FB}	Feedback input current	vs	Junction temperature	8
V_Z	Flyback reference voltage	vs	Junction temperature	9
t_d	Flyback sense delay time	vs	Junction temperature	10
$I_{O(SW)}$	Switch output current (with switch off)	vs	Switch voltage	11
	Driver base current	vs	Switch output current	12
$V_{sat(SW)}$	Switch saturation voltage	vs	Switch output current	13
$I_{O(SW)}$	Switch output current limit	vs	Duty cycle	14
	Maximum duty cycle	vs	Junction temperature	15
I_{IN}	Shutdown-mode input current	vs	Control voltage	16
I_{IN}	Shutdown-mode input current	vs	Input voltage	17
$V_{T(C)}$	Shutdown-mode control threshold voltage	vs	Junction temperature	18
$I_{T(C)}$	Shutdown-mode control threshold current	vs	Junction temperature	18
V_{FB}	Feedback input voltage at normal/flyback mode threshold	vs	Feedback input current	19
	Minimum input voltage	vs	Junction temperature	20
I_{IN}	Input current (SW output open)	vs	Junction temperature	21
I_{IN}	Input current	vs	Input voltage	22

table of application circuits

APPLICATION	FIGURE
Totally isolated converter	23
Boost converter (5 V to 12 V)	24

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT POWER
vs
INPUT VOLTAGE

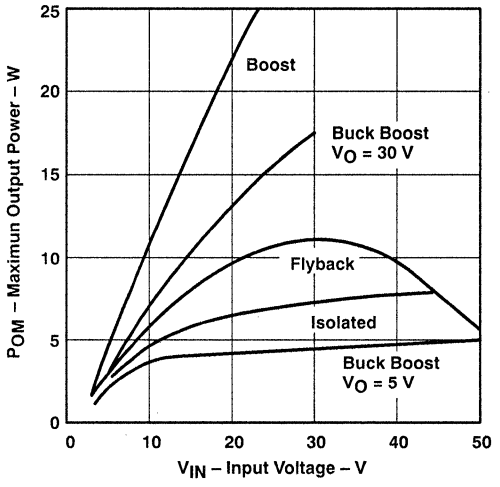


Figure 1

REFERENCE VOLTAGE AND
SWITCHING FREQUENCY
vs
JUNCTION TEMPERATURE

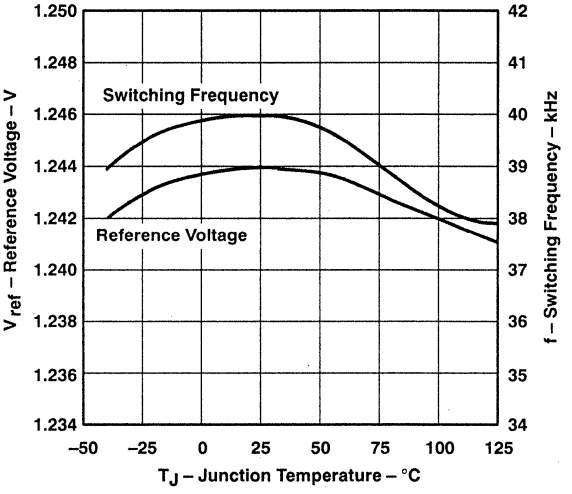


Figure 2

REFERENCE VOLTAGE INPUT REGULATION

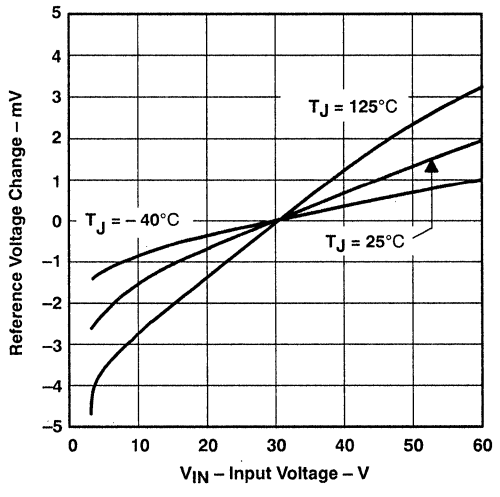


Figure 3

FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

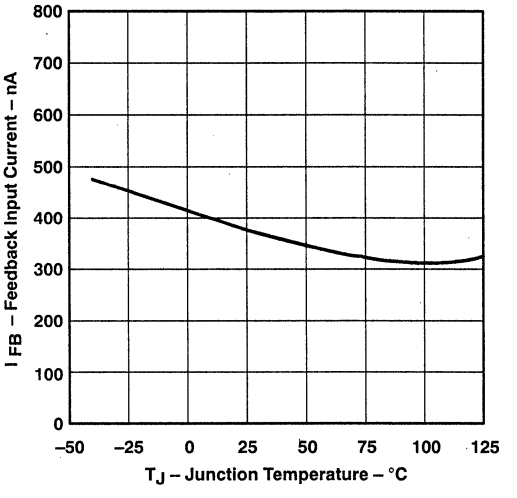


Figure 4

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER TRANSDUCTANCE
vs
JUNCTION TEMPERATURE

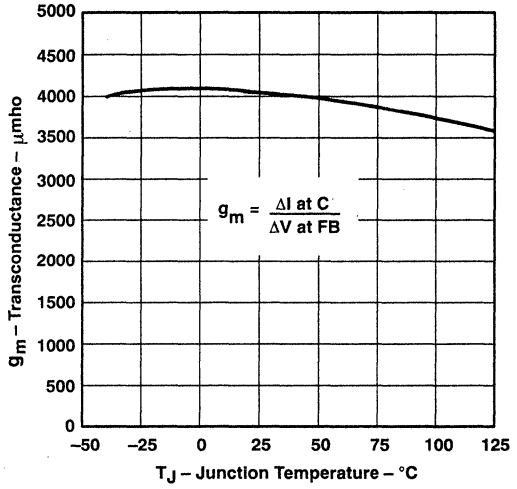


Figure 5

ERROR AMPLIFIER TRANSCONDUCTANCE
AND PHASE SHIFT
vs
FREQUENCY

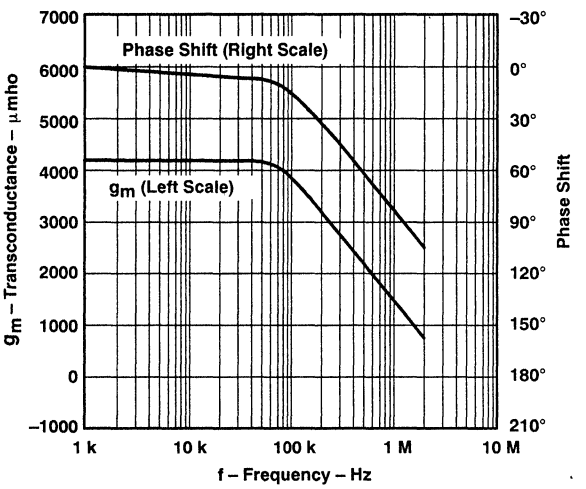


Figure 6

CONTROL CURRENT
vs
CONTROL VOLTAGE

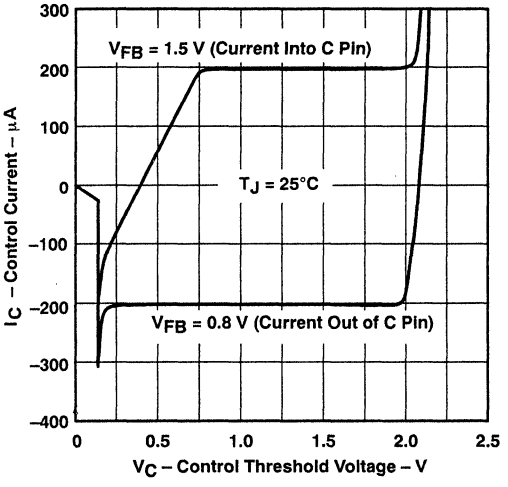


Figure 7

NORMAL-FLYBACK-MODE THRESHOLD VOLTAGE
AND FEEDBACK INPUT CURRENT
vs
JUNCTION TEMPERATURE

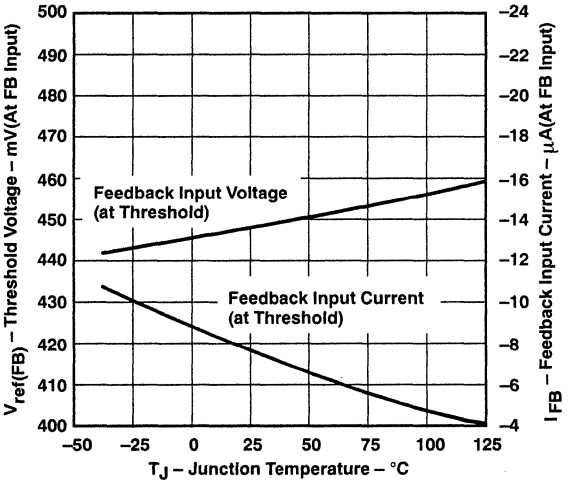


Figure 8

TYPICAL CHARACTERISTICS

FLYBACK MODE REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

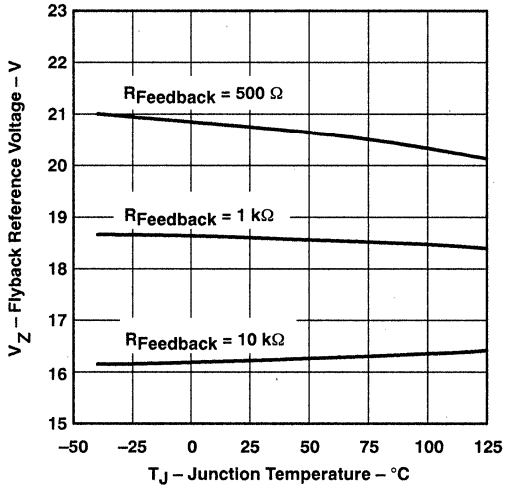


Figure 9

FLYBACK SENSE DELAY TIME
vs
JUNCTION TEMPERATURE

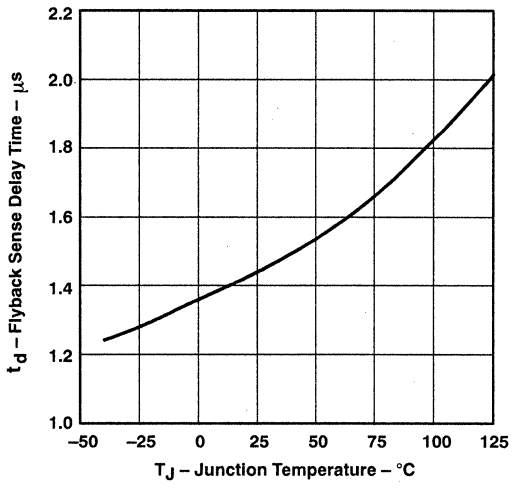


Figure 10

SWITCH OUTPUT CURRENT
vs
SWITCH VOLTAGE AND INPUT VOLTAGE
(WITH SWITCH OFF)

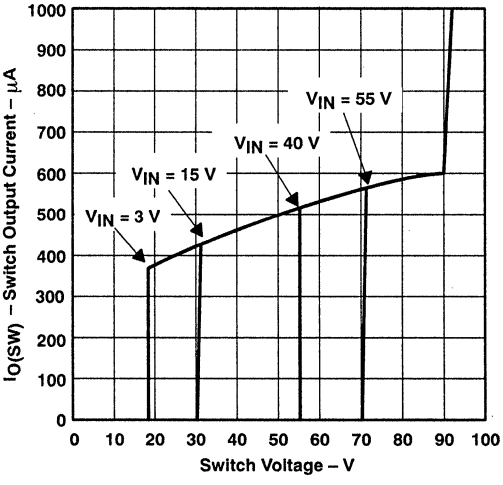


Figure 11

DRIVER BASE CURRENT†
vs
SWITCH OUTPUT CURRENT

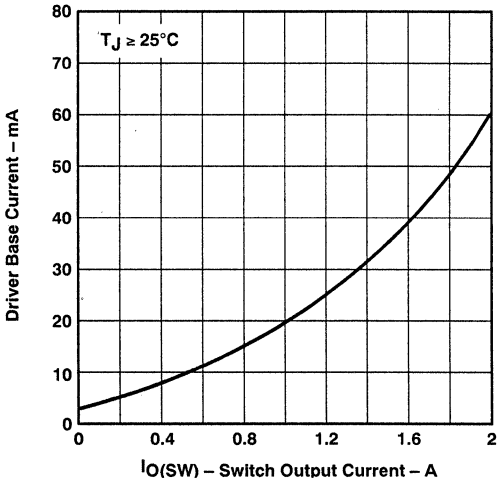


Figure 12

† Average input current is found by multiplying driver base by duty cycle plus quiescent current.

TYPICAL CHARACTERISTICS

SWITCH SATURATION VOLTAGE
vs
SWITCH CURRENT

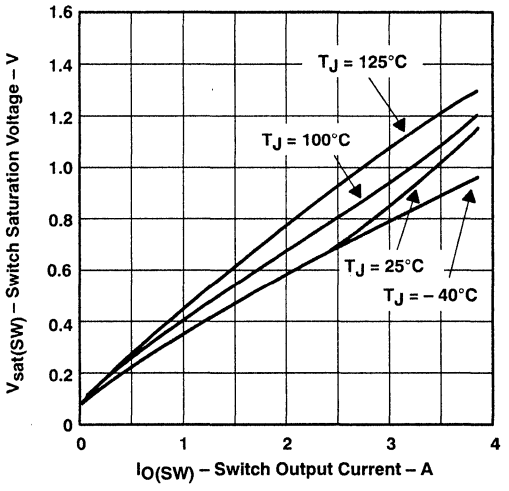


Figure 13

SWITCH OUTPUT CURRENT LIMIT
vs
DUTY CYCLE

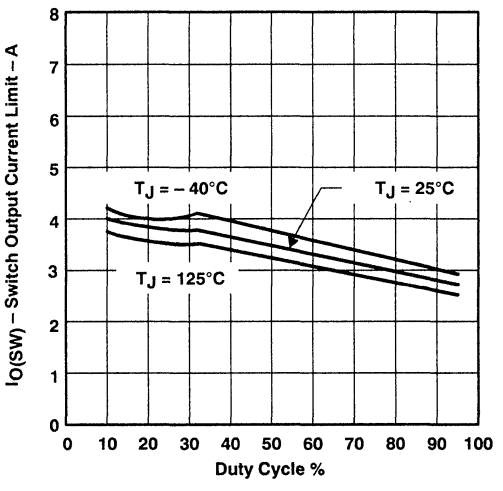


Figure 14

DUTY CYCLE (MAX)
vs
JUNCTION TEMPERATURE

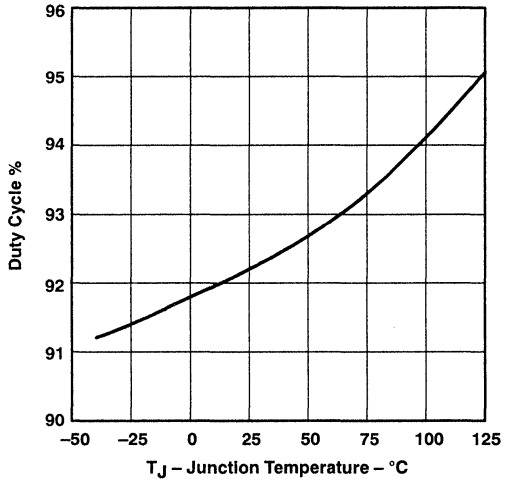


Figure 15

SHUTDOWN MODE
INPUT CURRENT
vs
CONTROL THRESHOLD VOLTAGE

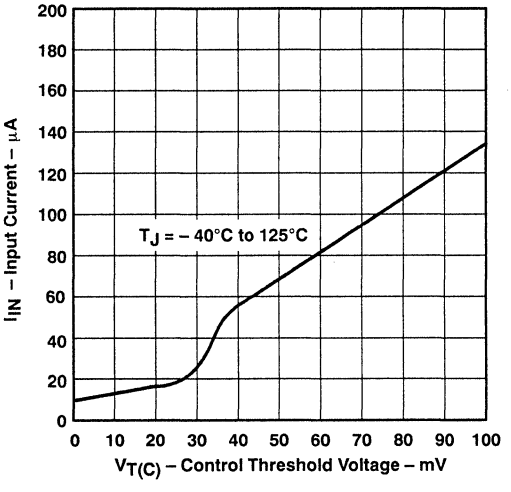


Figure 16

TYPICAL CHARACTERISTICS

SHUTDOWN MODE
INPUT CURRENT
vs
INPUT VOLTAGE

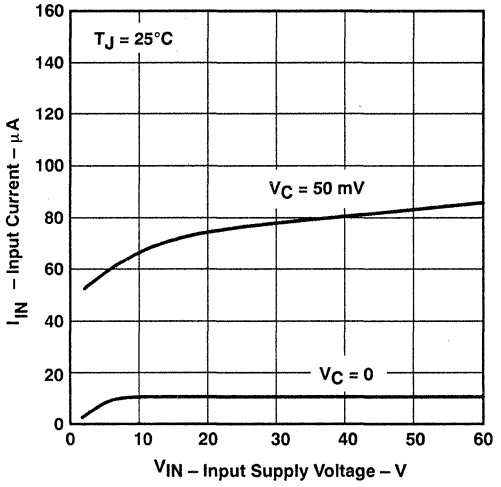


Figure 17

SHUTDOWN MODE
CONTROL THRESHOLD VOLTAGE AND CURRENT
vs
JUNCTION TEMPERATURE

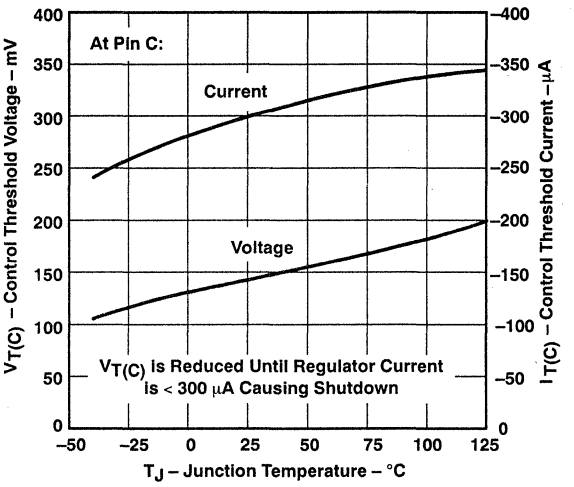


Figure 18

FEEDBACK INPUT VOLTAGE
vs
FEEDBACK INPUT CURRENT

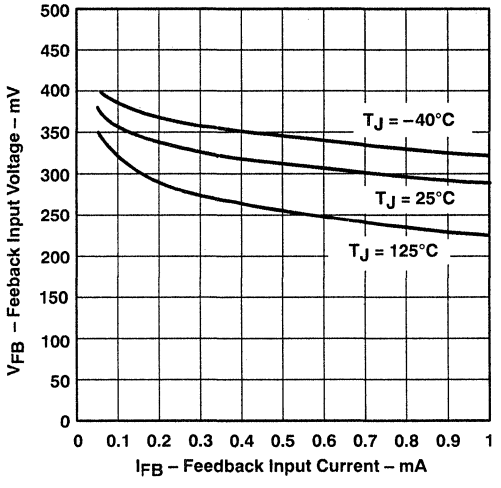


Figure 19

MINIMUM INPUT VOLTAGE
vs
JUNCTION TEMPERATURE

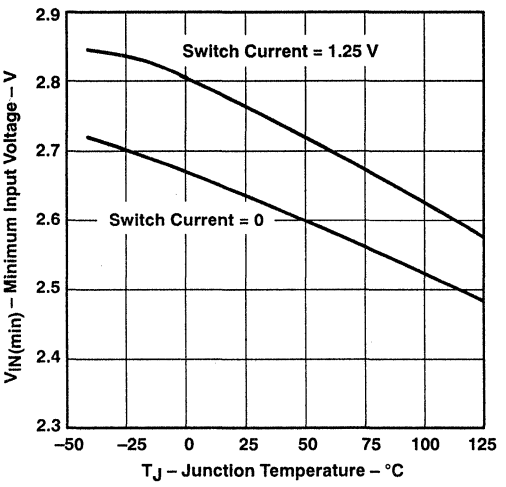


Figure 20

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
JUNCTION TEMPERATURE
(SW OUTPUT OPEN)

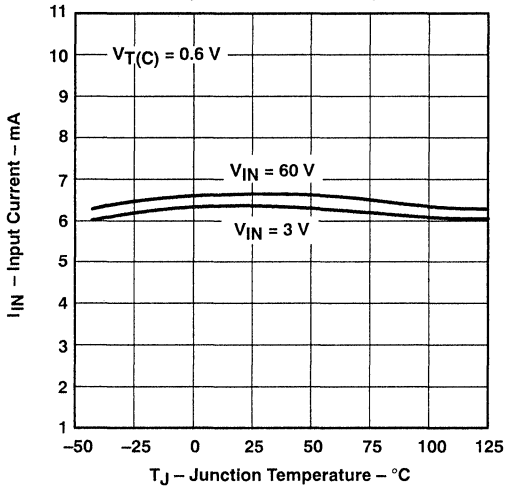
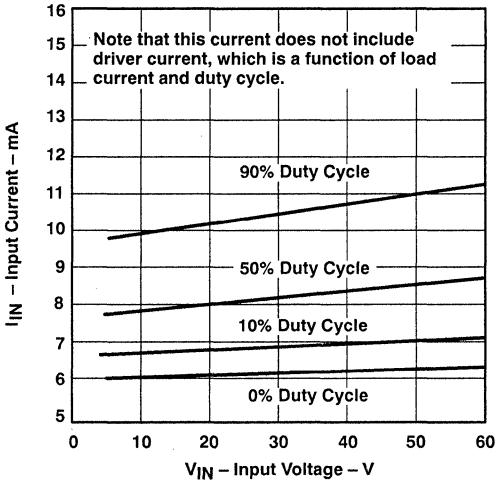


Figure 21

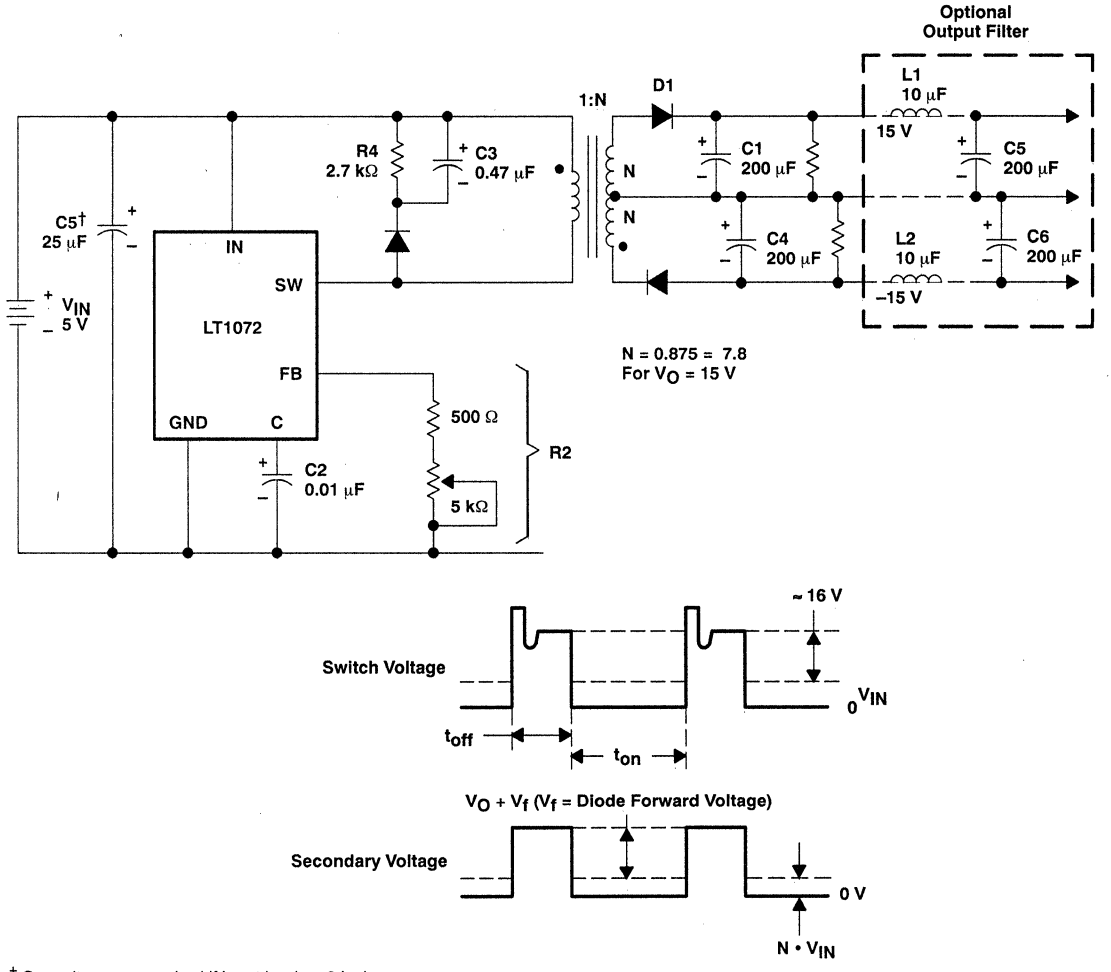
INPUT CURRENT
vs
INPUT VOLTAGE†



† Under very low output current conditions, duty cycle for most circuits will approach 10% or less.

Figure 22

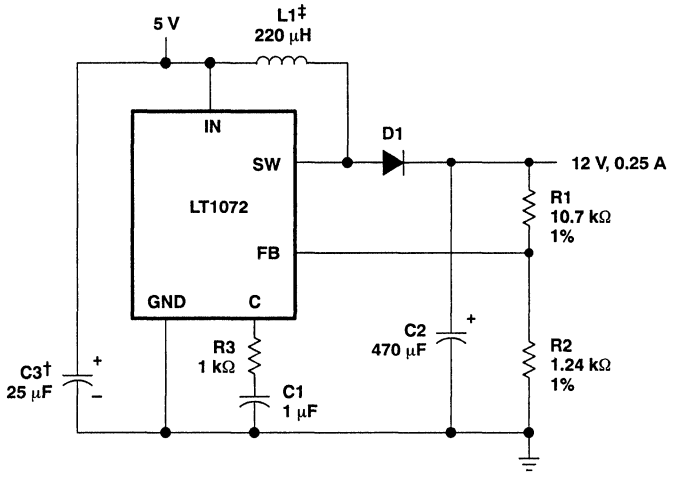
APPLICATION INFORMATION



† Capacitors are required if input leads ≥ 2 inches.

Figure 23. Totally Isolated Converter

APPLICATION INFORMATION



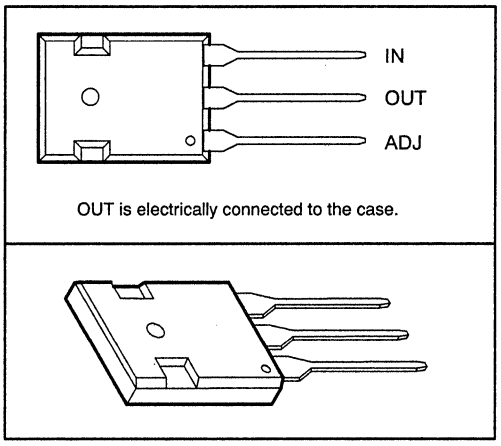
† Capacitor is required if input leads ≥ 2 inches.
‡ Pulse Engineering 52626

Figure 24. Boost Converter (5 V to 12 V)

D3118, JULY 1988 – REVISED JANUARY 1992

- **Adjustable Output . . . 1 V to 35 V**
- **5-A Output Capability**
- **Dropout Voltage**
  1.5 V at Maximum Current
  1 V at Minimum Current
- **Input Regulation . . . 0.015% Typ**
- **Output Regulation . . . 0.01% Typ**
- **100% Thermal Limit Burn-In**

KK PACKAGE
(TOP VIEW)



OUT is electrically connected to the case.

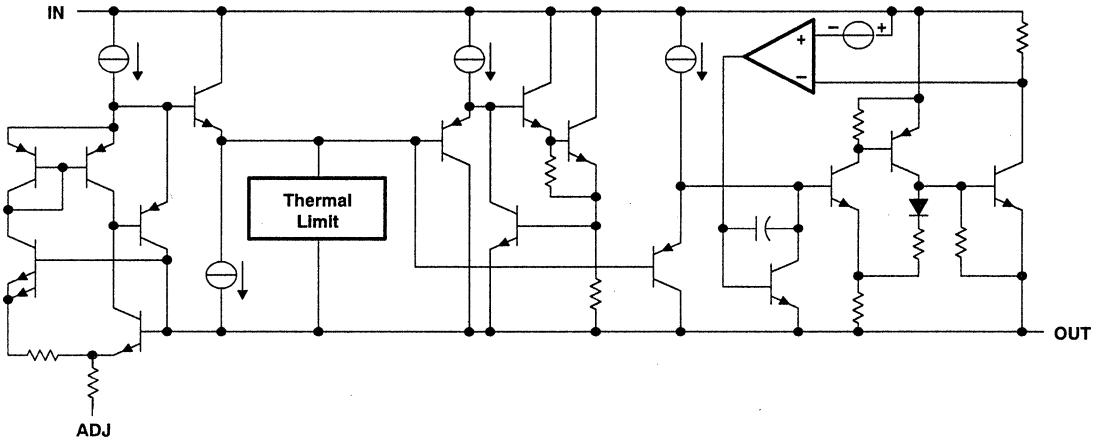
description

The LT1084C is a 3-terminal low-dropout adjustable positive regulator that operates with higher efficiency than currently available devices with output loads up to 5 A. Internal circuitry is designed to operate with a small input-to-output differential voltage of 1.3 V (typical) and all dropout voltages are specified as a function of output current. Dropout voltage reaches a maximum of 1.5 V at maximum output current. On-chip circuitry holds the reference voltage constant to within 1%. Current limiting is used to minimize the stress on both the regulator and power source circuits under overload conditions.

The LT1084C is terminal compatible with older 3-terminal regulators. A 10-μF output capacitor is required, as in most regulator designs. In P-N-P regulators, up to 10% of the output current is lost as bias (quiescent) current, but the LT1084C bias current flows into the load, which improves power efficiency.

Typical applications include high-efficiency linear regulators, post regulators for switching power supplies, constant-current regulators, and battery chargers.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage ..... 30 V
Output current, I_O ..... 8 A
Power dissipation ..... Internally self-limited
Operating virtual-junction temperature range: Control section ..... 0°C to 125°C
Power transistor ..... 0°C to 150°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

recommended operating conditions

		MIN	MAX	UNIT
Output current, I_O			5	A
Operating virtual-junction temperature, T_J	Control section	0	125	°C
	Power transistor	0	150	

electrical characteristics at specified virtual-junction temperature (unless otherwise noted)

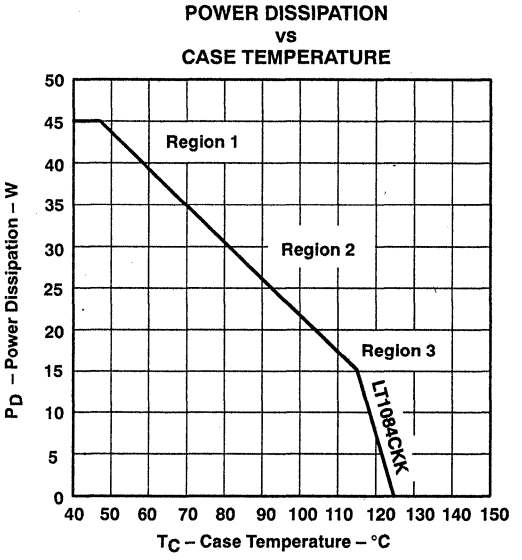
PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Input regulation	$V_I - V_O$ = 1.5 V to 15 V, I_O = 10 mA	25°C		0.015%	0.2%	
		Full range		0.035%	0.2%	
	$V_I - V_O$ = 15 V to 30 V, See Notes 1 and 2	Full range		0.05%	0.5%	
Ripple rejection	$V_I - V_O$ = 3 V, I_O = 5 A (full load), f = 120 Hz, See Notes 3 and 4	Full range	60	75		dB
Output regulation	$V_I - V_O$ = 3 V, I_O = 10 mA to 5 A (full load), See Notes 1, 2, and 3	25°C		0.1%	0.3%	
		Full range		0.2%	0.4%	
Output voltage change with temperature		Full range		0.5%		
Thermal regulation	t_w = 30 ms	T_A = 25°C		0.003	0.015	%/W
Output voltage long-term drift	After 1000 hours at T_J = 125°C	25°C		0.3%	1%	
Output noise voltage (% of V_O)	f = 10 Hz to 10 kHz	25°C		0.003%		
Minimum output operating current	$V_I - V_O$ = 25 V	Full range		5	10	mA
Current limit	$V_I - V_O$ = 5 V	Full range	5.5	6.5		A
	$V_I - V_O$ = 25 V		0.3	0.6		
Dropout voltage	ΔV_{ref} = 1%, I_O = full load	Full range		1.3	1.5	V
ADJ current		25°C		55		μA
		Full range			120	
Change in ADJ current	$V_I - V_O$ = 1.5 V to 25 V, I_O = 10 mA to 5 A (full load), See Note 3	Full range		0.2	5	μA
Reference voltage, $V_O - V_{ADJ}$	$V_I - V_O$ = 1.5 V to 25 V, I_O = 10 mA to 5 A (full load), See Note 3	Full range	1.225	1.250	1.270	V

† Full range is 0°C to 125°C.

NOTES: 1. Input regulation is expressed as the percentage change in output voltage per 1-V change at the input. See thermal regulation specifications for changes in output voltage due to heating effects. Input and output regulation are measured at a constant junction temperature by low-duty-cycle pulse testing. Use pulses ($t_w \leq 10$ μs, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

2. Input and output regulation are specified up to the maximum power dissipation of 45 W. Power dissipation is determined by the product of input-to-output differential voltage and output current. Maximum power dissipation is not available over the full input-to-output voltage range. See Figure 2.
3. I_O (full load) is defined on the current-limit graph (Figure 2) as the minimum value of current limiting as a function of input-to-output differential voltage. Note that 45-W power dissipation is achievable, but only over a limited range of input-to-output differential voltage.
4. Ripple rejection is measured with a 25-μF capacitor between ADJ and ground and a 25-μF tantalum capacitor between OUT and ground.

TYPICAL CHARACTERISTICS



Region 1 is limited by the full load current, see Figure 2 and Notes 2 and 3.

Region 2 is limited by the maximum junction temperature of the power transistor. The slope is based on the thermal resistance $R_{\theta JC}$, which is 2.3°C/W.

Region 3 is limited by the maximum junction temperature of the control section. The slope is based on the thermal resistance $R_{\theta JC}$, which is 0.65°C/W.

Figure 1

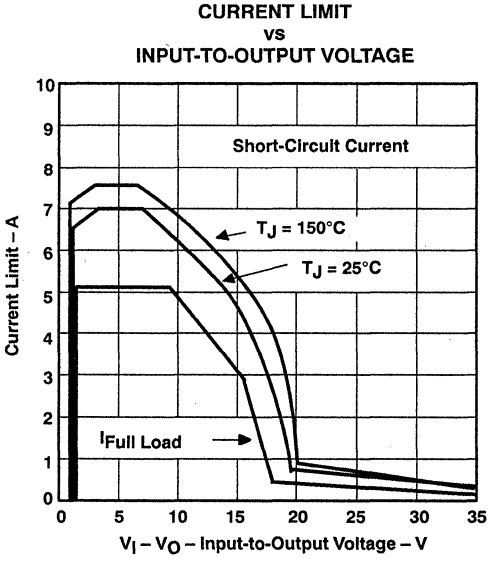


Figure 2

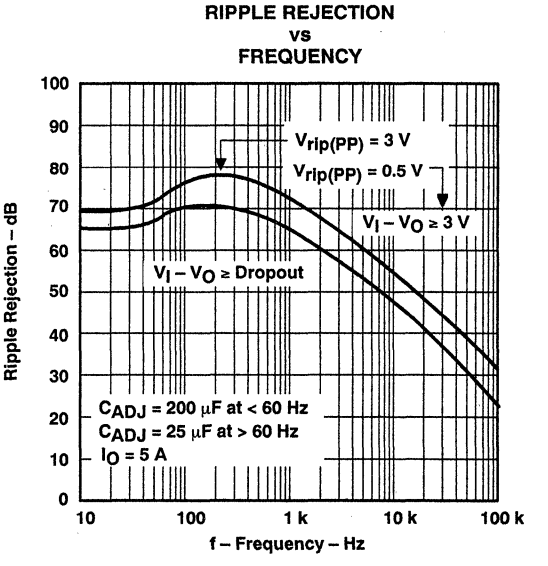


Figure 3

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
OUTPUT CURRENT

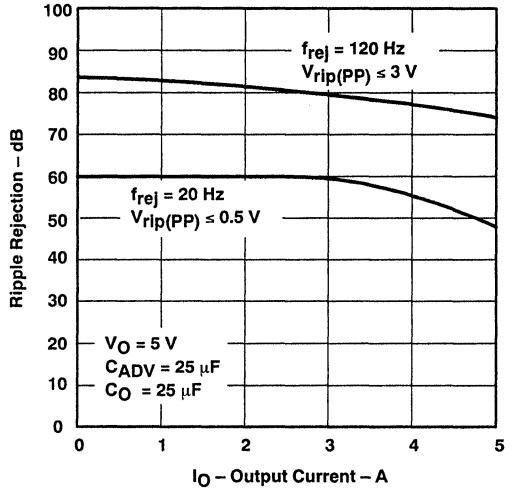


Figure 4

OUTPUT REGULATION
vs
JUNCTION TEMPERATURE

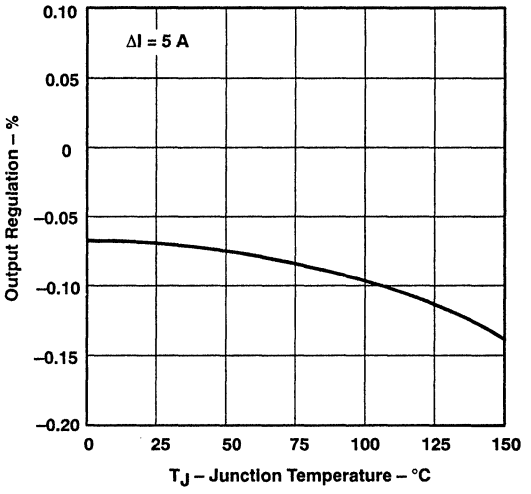


Figure 5

MINIMUM OPERATING CURRENT
vs
INPUT-TO-OUTPUT VOLTAGE

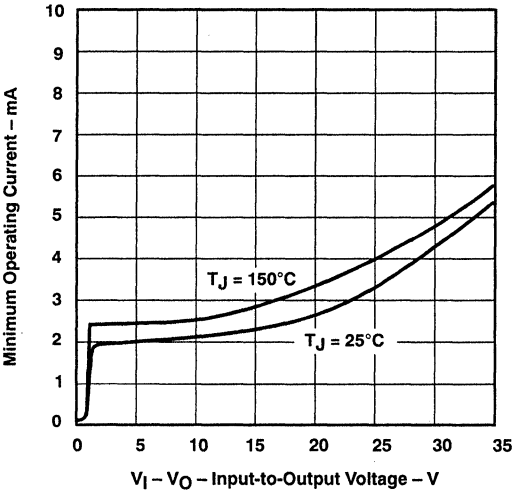


Figure 6

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

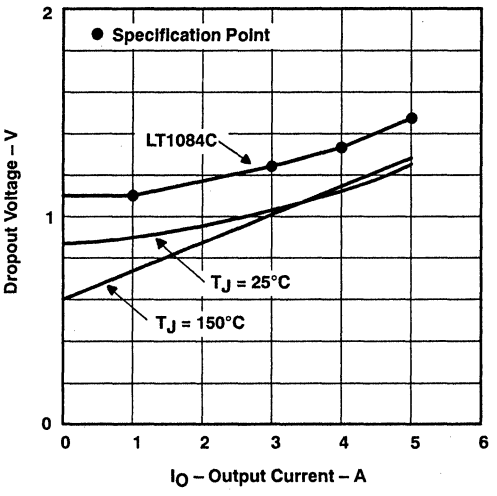


Figure 7

TYPICAL CHARACTERISTICS

ADJ CURRENT
vs
VIRTUAL-JUNCTION TEMPERATURE

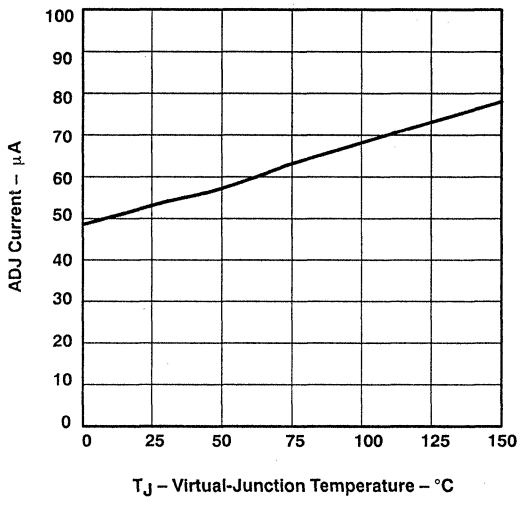


Figure 8

REFERENCE VOLTAGE
vs
VIRTUAL-JUNCTION TEMPERATURE

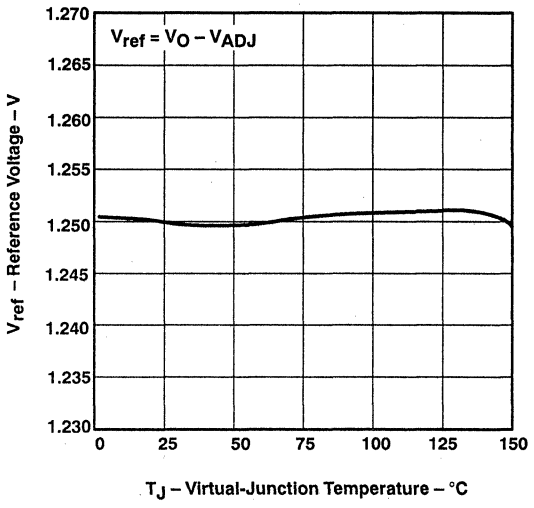


Figure 9

INPUT TRANSIENT RESPONSE

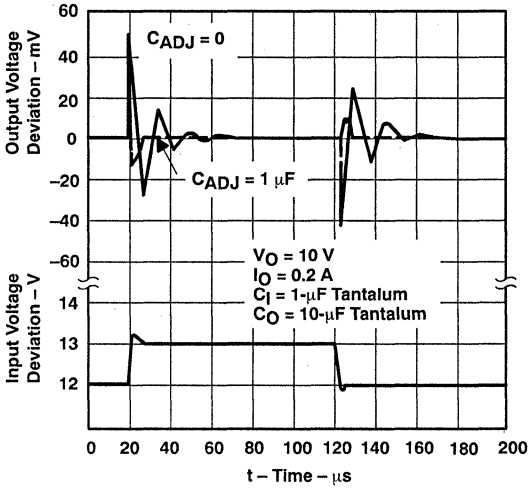


Figure 10

OUTPUT TRANSIENT RESPONSE

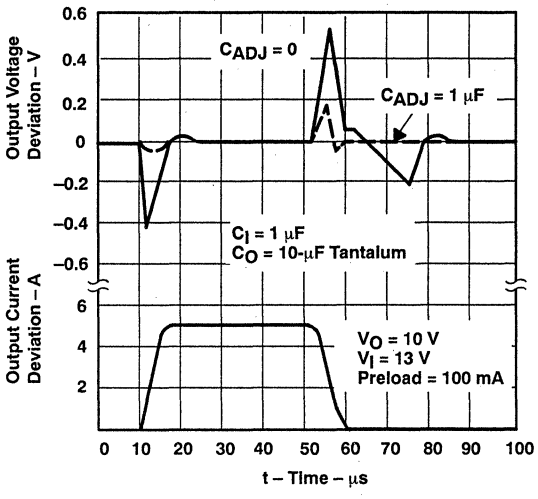


Figure 11

APPLICATION INFORMATION

The LT1084C 3-terminal adjustable regulator is easy to use and has all the protection features that are expected in high-performance voltage regulators. It is short-circuit protected. Safe-area protection and thermal shutdown turn off the regulator when the junction temperature exceeds approximately 165°C.

The regulator is terminal compatible with older 3-terminal adjustable devices and offers lower dropout voltage and voltage reference tolerance. The reference voltage-versus-temperature stability is improved. The only circuit difference between using the LT1084C and older regulators is the need for an output capacitor for more stability.

stability

The circuit design used in the LT1084C requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150-μF aluminum electrolytic or a 22-μF solid tantalum capacitor on the output ensures stability. Typically, capacitors that are much smaller in value can be used with the LT1084C. Many different types of capacitors, with widely varying characteristics, are available that differ in capacitor tolerance (up to plus or minus 100%), equivalent series resistance, and capacitor temperature coefficient. The 150-μF or 22-μF values will ensure stability.

When ADJ bypassed to improve ripple rejection, the requirement for an output capacitor increases. The 22-μF tantalum or 150-μF electrolytic capacitor values cover all cases of bypassing ADJ. Without bypassing ADJ, smaller capacitors can be used with good results. The recommended capacitors needed to ensure stability are listed in the following table:

RECOMMENDED OUTPUT CAPACITOR VALUES

IN	OUT	ADJ
10 μF	10-μF Tantalum or 50-μF Aluminum	None
10 μF	22-μF Tantalum or 150-μF Aluminum	20 μF

Typically, capacitor values of 100 μF are used on the output of many regulators to ensure good transient response with large load-current changes. Output capacitance can be increased without limit to improve the stability and transient response of the LT1084C regulator.

Another stability problem that can occur in monolithic regulators is current-limit oscillations. This problem occurs during current limiting when the safe-area protection exhibits a negative impedance. The safe-area protection decreases the current limit as the input-to-output voltage increases. This acts as a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limiting is not unique to the LT1084C and is present on all power IC regulators. The value of negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may be unstable. This system problem is not necessarily easy to solve; however, it does not cause any problems with the IC regulator and can usually be ignored.

protection diodes

In normal operation, the LT1084C does not need any protection diodes. Older adjustable regulators required protection diodes between ADJ and OUT and from OUT to IN to prevent overstressing the IC. The internal current paths on the LT1084C ADJ are limited by the internal resistors. Therefore, no protection diode is needed to ensure device safety under short-circuit conditions even with capacitors on ADJ. See Figure 12.

APPLICATION INFORMATION

Diodes between IN and OUT are usually not needed. The internal diode between IN and OUT of the LT1084C can handle microsecond surge currents of 50 A to 100 A. Even with large output capacitances, it is difficult to obtain those values of surge currents in normal operations. Damage can occur only when using high values of output capacitance (1000 μF to 5000 μF) with IN instantaneously shorted to ground. A crowbar circuit at IN can generate those kinds of currents, and a diode from output-to-input is then recommended. Normal power supply on-off cycling or even connecting and disconnecting in the system will not generate a large enough current to cause damage. ADJ can be driven, on a transient basis, plus or minus 25 V with respect to OUT without device degradation. As with any IC regulator, exceeding the maximum input-to-output differential voltage causes the internal transistors to break down, and the protection circuitry does not prevent this.

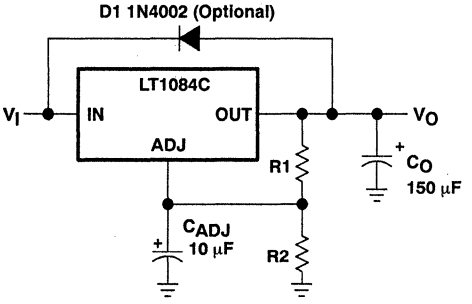


Figure 12

overload recovery

The LT1084C regulator has safe-area protection that decreases the current limit as input-to-output voltage increases, so the power transistor operates inside a safe region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is turned on and IN voltage rises, the OUT follows IN and the input-to-output differential voltage remains small to allow a large current demand on the regulator to be supplied. With high input voltage and low output voltage, a problem occurs that is common to older regulators (such as the 7800 series) as well as the LT1084C. OUT voltage will not recover after removal of an output short. The load line for such a large load may intersect the OUT current curve at two points. If this happens, there are two stable OUT operating points for the regulator. With a double intersection, the power supply may need to be cycled to zero and brought up again to make OUT recover.

ripple rejection

The typical curves for ripple rejection reflect values for a bypassed ADJ. This curve will be true for all values of output voltage. For proper bypassing and ripple rejection near the values shown, the impedance of the ADJ capacitor at the ripple frequency should equal the value of resistor R1 (normally 100 Ω to 120 Ω). The capacitance of the required ADJ capacitor is a function of the input ripple frequency. The ADJ capacitor should be 13 μF with R1 equal to 100 Ω at a frequency of 120 Hz. Only 0.16 μF is needed at 10 kHz. See Figure 16.

APPLICATION INFORMATION

Ripple rejection is a function of OUT voltage for circuits without an ADJ bypass capacitor. The output ripple will increase directly as a ratio of the OUT voltage to the reference voltage (V_O/V_{ref}). For example, the output ripple will be higher by the ratio of 5 V/1.25 V or four times larger with OUT voltage equal to 5 V and with no ADJ capacitor. Ripple rejection would be degraded 12 dB from the value shown on the typical curve.

output voltage

The LT1084C develops a 1.25-V reference voltage between OUT and ADJ (see Figure 13). When resistor R1 is placed between these two terminals, a constant current flows through R1 and through R2 to set the overall OUT voltage. Normally this current is the specified minimum output current of 10 mA. Since I_{ADJ} is very small and constant when compared with the current through R1, I_{ADJ} can usually be ignored and represents a small error.

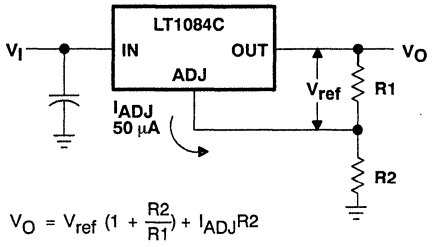


Figure 13

output regulation

The LT1084C is not able to provide true remote-load sensing with only three terminals. Output regulation will be limited by the resistance of the wire connecting the regulator to the load. The data-sheet specification for output regulation is measured at the bottom of the package. Negative-side sensing is a true Kelvin connection that has the bottom of the output divider returned to the negative side of the load. The best output regulation is obtained when the top of the resistor divider R1 is connected directly to the case or OUT, not to the load. This is illustrated in Figure 14. If resistor R1 were connected to the load, the effective resistance between the regulator and the load would be as shown:

$$R_{eff} = R_P \times (R2 + R1)/R1$$

Assuming R_P = 0.004 Ω per foot (16-gauge wire), this calculation gives 4 mV per foot at a load current of 1 A. It is important to keep the positive lead between regulator and load as short as possible and use large wire or circuit-board traces to minimize this problem. Connected as shown in Figure 14, R_P is not multiplied by the divider ratio.

thermal considerations

The LT1084C regulator has internal power and thermal-limiting circuitry designed to protect the device under overload conditions. For continuous normal-load conditions, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from device junction to ambient. This includes junction-to-case, case-to-heat-sink interface, and heat-sink resistance. New

APPLICATION INFORMATION

thermal-resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The maximum ratings table and the explanation with Figure 1 provide maximum junction temperature and thermal resistance for the control section and separately for the power transistor. Previous regulators used a single junction-to-case thermal resistance specification that was an average of the two values. This method could allow excessive junction temperatures under certain conditions of ambient temperature and heat-sink resistance. To avoid this possibility, calculations should be made for both sections of the device to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat-sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally-conductive spacer can be used, but the added contribution to thermal resistance must be considered. The KK package is electrically connected to OUT.

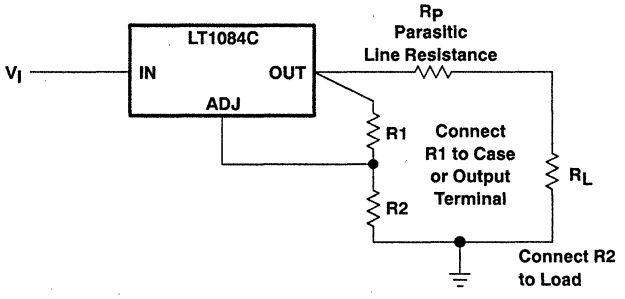


Figure 14

thermal example

Using an LT1084CCKK regulator (KK plastic package and commercial temperature) and assuming:

V_I = 9 V (maximum continuous), V_O = 5 V, I_O = 5 A,
T_A = 75°C, $R_{\theta HSA}$ = 1°C/W, $R_{\theta CHS}$ = 0.2C°/W

Maximum thermal resistances: (see Figure 1)

Control section $R_{\theta JC}$ = 0.65°C/W,
Power transistor $R_{\theta JC}$ = 2.3°C/W

Power dissipation under these conditions is equal to:

$$P_D = (V_I - V_O)\ (I_O) = (9 - 5)\ (5) = 20\ W$$

Junction temperature is calculated using:

$$T_J = T_A + P_D(R_{\theta HSA} + R_{\theta CHS} + R_{\theta JC})$$

Junction temperature for control section:

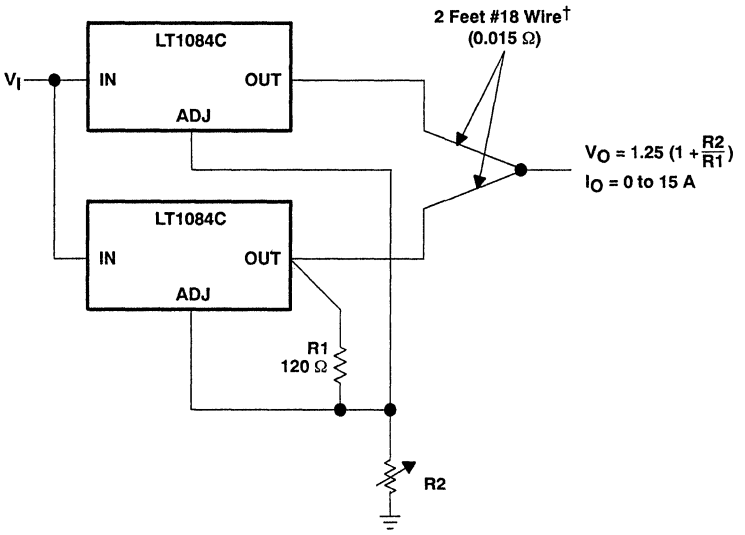
$$T_J = 75 + 20(1 + 0.2 + 0.65) = 112°C$$

Junction temperature for power transistor:

$$T_J = 75 + 20(1 + 0.2 + 2.3) = 145°C$$

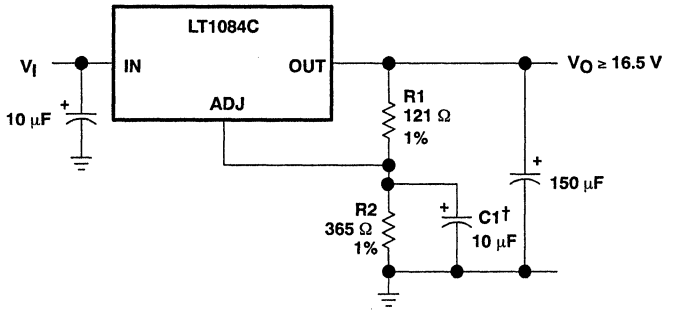
In both cases, the junction temperature is below the maximum rating for the respective sections.

APPLICATION INFORMATION



† The # 18 wire acts as ballast resistance, insuring current sharing between both devices.

Figure 15. Paralleling Regulators



† C1 improves ripple rejection. X_C should be equal to R1 at ripple frequency.

Figure 16. Improving Ripple Rejection

APPLICATION INFORMATION

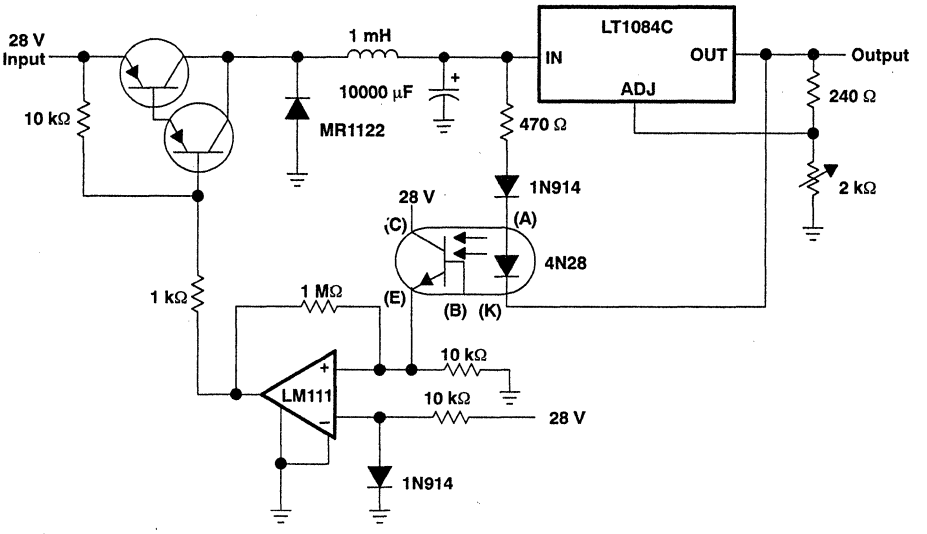


Figure 17. High-Efficiency Regulator

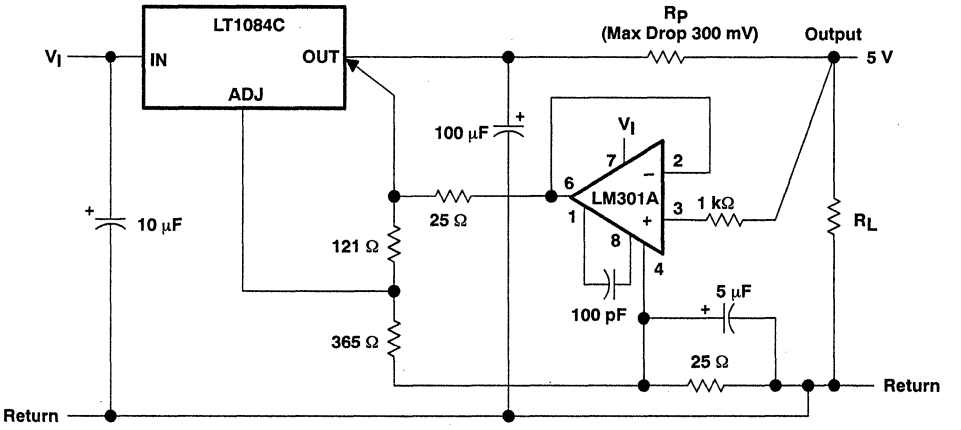
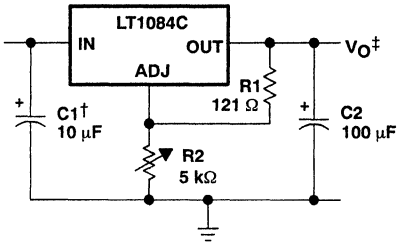


Figure 18. Remote Sensing

APPLICATION INFORMATION



† Needed if device is far from filter capacitors.

‡ $V_O = 1.25(1 + \frac{R2}{R1})V$

Figure 19. 1.2-V to 15-V Adjustable Regulator

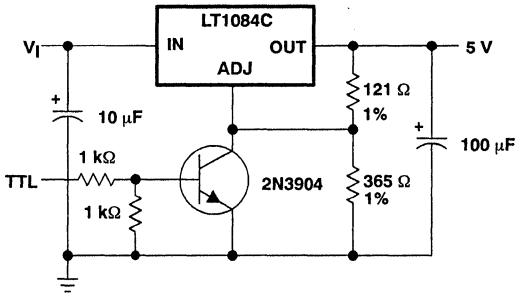


Figure 20. 5-V Regulator With Shutdown

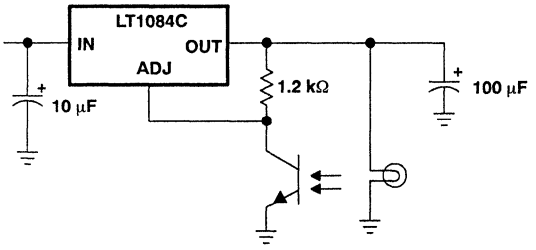


Figure 21. Automatic Light Control

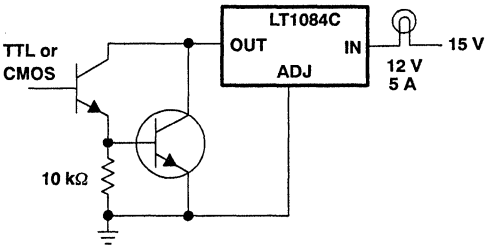
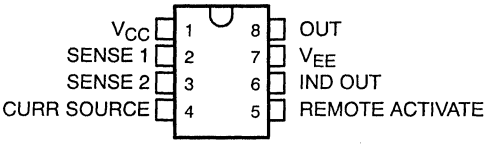


Figure 22. Protected High-Current Lamp Driver

D2439, APRIL 1978—REVISED MARCH 1988

- **Separate Outputs for Crowbar and Logic Circuitry**
- **Programmable Time Delay to Eliminate Noise Triggering**
- **TTL-Level Activation Isolated From Voltage-Sensing Inputs**
- **2.6-V Internal Voltage Reference With Temperature Coefficient Typically 0.06%/°C**

D OR P PACKAGE
(TOP VIEW)

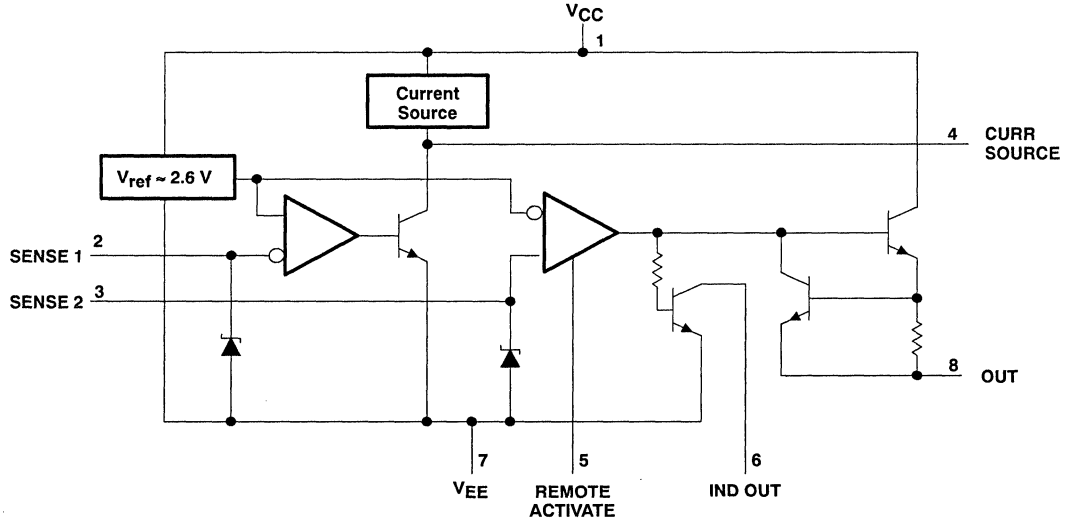


description

The MC3423 overvoltage-sensing circuit is designed to protect sensitive electronic circuitry by monitoring the supply rail and triggering an external crowbar SCR in the event of a voltage transient or loss of regulation. The protective mechanism may be activated by an overvoltage condition at the SENSE 2 input or by application of a TTL-high level to REMOTE ACTIVATE. Separate outputs are available to trigger the crowbar circuit and to provide a logic pulse to indicator or power supply control circuitry. The SENSE 2 input provides a direct control of the output circuitry. The SENSE 1 input controls an internal current source that may be utilized to implement a delayed trigger by connecting its output to an external capacitor and the SENSE 2 input. This protects against false triggering due to noise at the SENSE 1 input.

The MC3423 is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 40 V
Input voltage, SENSE 1 ..... 6.5 V
Input voltage, SENSE 2 ..... 6.5 V
Input voltage, REMOTE ACTIVATE ..... 7 V
Output current, I_O ..... 300 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are measured with respect to the V_{EE} terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	40	V
High-level input voltage, REMOTE ACTIVATE	2		V
Low-level input voltage, REMOTE ACTIVATE		0.5	V

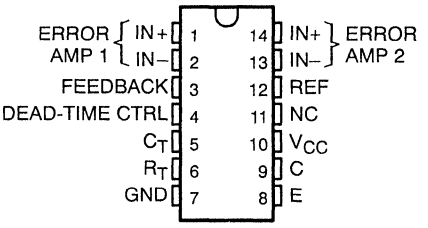
electrical characteristics over operating free-air temperature range, V_{CC} = 5 V to 36 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	REMOTE ACTIVATE input voltage at 2 V, I_O = 100 mA	$V_{CC}-2.2$	$V_{CC}-1.8$		V
Indicator low-level output voltage	REMOTE ACTIVATE input voltage at 2 V, I_O = 1.6 mA		0.1	0.4	V
Threshold voltage of either sense input	T_A = 25°C	2.45	2.6	2.75	V
Temperature coefficient of input threshold voltage			0.06		%/°C
I_O Output current, CURR SOURCE	SENSE 1 input voltage at 3 V, CURR SOURCE input voltage at 1.3 V	0.1	0.22	0.3	mA
High-level input current, REMOTE ACTIVATE	V_{CC} = 5 V, V_I = 2 V		5	40	μA
Low-level input current, REMOTE ACTIVATE	V_{CC} = 5 V, V_I = 0.8 V		−120	−180	μA
Supply current	Outputs open		6	10	mA
Propagation delay time, REMOTE ACTIVATE to output	T_A = 25°C		0.5		μs
Output current rate of rise	T_A = 25°C		400		mA/μs

D2714, MARCH 1983–REVISED FEBRUARY 1988

- **Complete PWM Power Control Circuitry**
- **Uncommitted Output for 200-mA Sink or Source Current**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply**
- **Circuit Architecture Provides Easy Synchronization**
- **Direct Replacement for Motorola MC34060**

D OR N PACKAGE
(TOP VIEW)



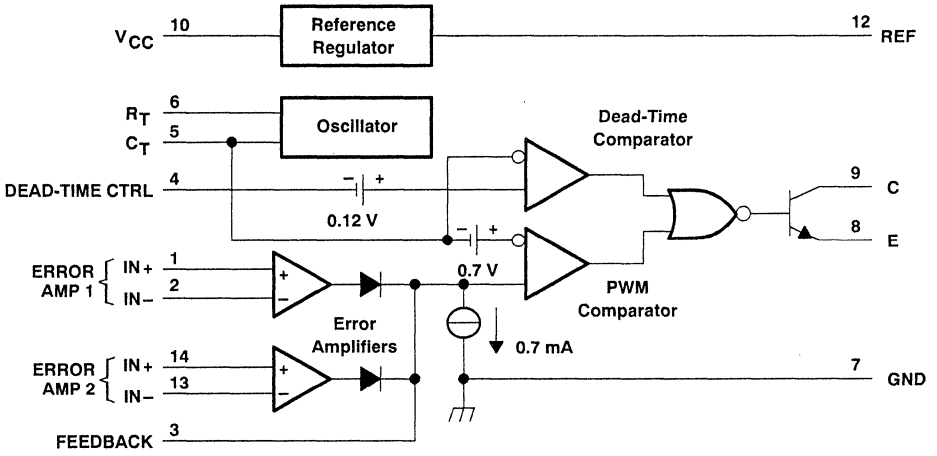
NC – No internal connection

description

The MC34060 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the device contains an on-chip 5-V regulator, two error amplifiers, an adjustable oscillator, and a dead-time control comparator. The uncommitted output transistor provides either common-emitter or emitter-follower output capability. The internal amplifiers exhibit a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common MC34060 circuitry and provide a sawtooth input for associated control circuitry in multiple rail power supplies.

The MC34060 is characterized for operation from 0°C to 70°C.

functional block diagram



All voltage and current values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 42 V
Amplifier input voltage ..... V_{CC} + 0.3 V
Collector output voltage ..... 42 V
Collector output current ..... 250 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values except differential voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	900 mW	7.6 mW/°C	31°C	606 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Amplifier input voltages, V_I	−0.3	V_{CC}−2	V
Collector output voltage, V_O		40	V
Collector output current (each transistor)		200	mA
Reference output current		10	mA
Current into feedback terminal		0.3	mA
Timing capacitor, C_T	0.47	10000	nF
Timing resistor, R_T	1.8	500	kΩ
Oscillator frequency, f_{osc}	1	200	kHz
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 25 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Output voltage (REF)	I_O = 1 mA		4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	25	mV
Output regulation	I_{IO} = 1 to 10 mA,	T_A = 25°C		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2%	2.6%	
Short-circuit output current§	REF = 0,	T_A = 25°C		35		mA

oscillator section

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Frequency	C_T = 0.001 μF,	R_T = 47 kΩ		25		kHz
Standard deviation of frequency¶	C_T = 0.001 μF,	R_T = 47 kΩ		3%		
Frequency change with voltage	V_{CC} = 7 V to 40 V,	T_A = 25°C		0.1%		
Frequency change with temperature	C_T = 0.001 μF, ΔT_A = MIN to MAX	R_T = 47 kΩ,			±2%	

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
Input bias current (DEAD-TIME CTRL)	V_I = 0 to 5.25 V				–2	–10	μA
Maximum duty cycle	V_I (DEAD-TIME CTRL) = 0	C_T = 0.1 μF,	R_T = 12 kΩ	90%	96%	100%	
		C_T = 0.001 μF,	R_T = 47 kΩ		92%	100%	
Input threshold voltage (DEAD-TIME CTRL)	Zero duty cycle				3	3.3	V
	Maximum duty cycle			0			

error-amplifier section

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
Input offset voltage	V_O (FEEDBACK) = 2.5 V				2	10	mV
Input offset current	V_O (FEEDBACK) = 2.5 V				25	250	nA
Input bias current	V_O (FEEDBACK) = 2.5 V				0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V					–0.3 to V_{CC}–2	V
Open-loop voltage amplification	ΔV_O = 3 V,	R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ			800		kHz
Phase margin at unity gain	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ			65°		
Common-mode rejection ratio	V_{CC} = 40 V			65	80		dB
Output sink current (FEEDBACK)	V_{ID} = –15 mV to –5 V,	V(FEEDBACK) = 0.7 V		0.3	0.7		mA
Output source current (FEEDBACK)	V_{ID} = 15 mV to 5 V,	V(FEEDBACK) = 3.5 V		–2			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except "output voltage" characteristics are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N-1}}$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 25 kHz (unless otherwise noted) (continued)

output section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Collector off-state current		V_C = 40 V, V_E = 0 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V,	I_E = −200 mA		1.5	2.5	

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (FEEDBACK)	Zero duty cycle		4	4.5	V
Input sink current (FEEDBACK)	V(FEEDBACK) = 0.7 V	0.3	0.7		mA

total device

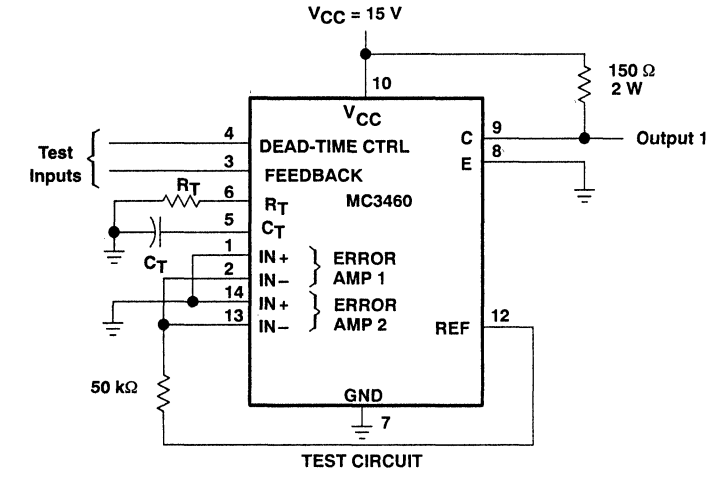
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	R_T at REF,	V_{CC} = 15 V		6	10	mA
	All other inputs and outputs open	V_{CC} = 40 V		9	15	
Average supply current	V(DEAD-TIME CTRL) = 2 V, R_T = 47 kΩ, See Figure 1	C_T = 0.001 μF,		7.5		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time			40	100	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



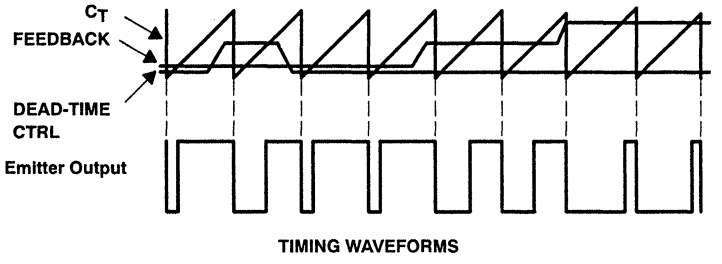


Figure 1. Dead-Time and Feedback Controls

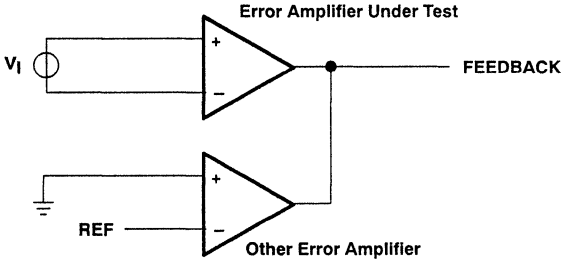


Figure 2. Error-Amplifier Characteristics

PARAMETER MEASUREMENT INFORMATION

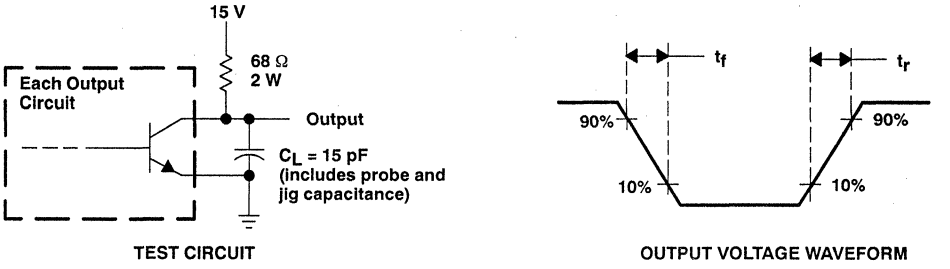


Figure 3. Common-Emitter Configuration

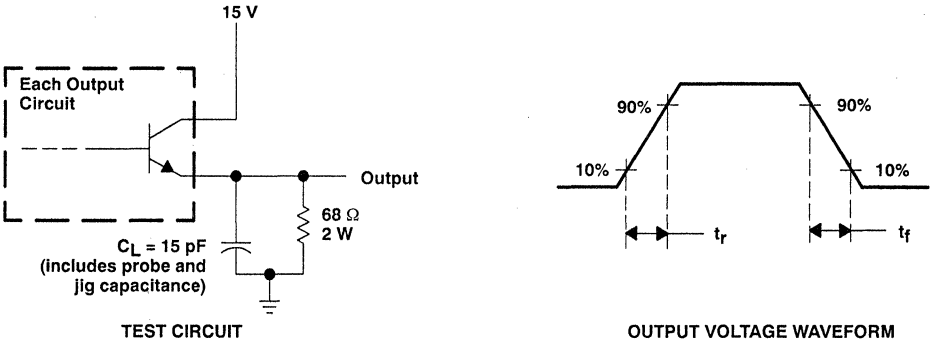
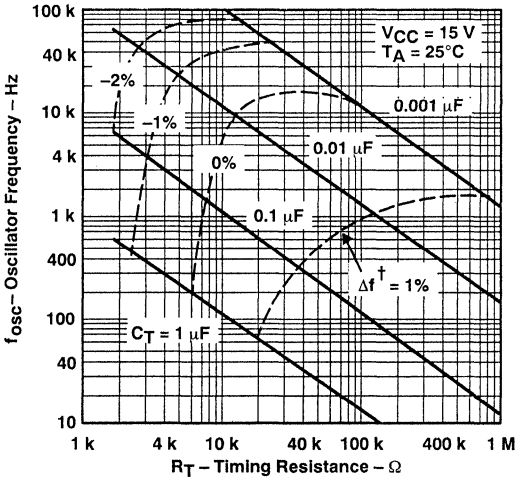


Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND
FREQUENCY VARIATION†
VS
TIMING RESISTANCE



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION
VS
FREQUENCY

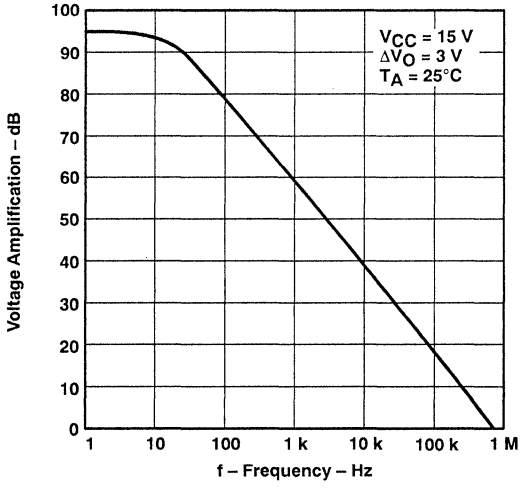
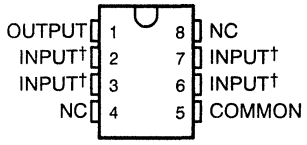


Figure 6

D2565, OCTOBER 1982–REVISED NOVEMBER 1991

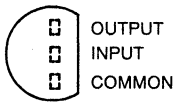
- **3-Terminal Regulators**
- **Output Current Up to 100 mA**
- **No External Components Required**
- **Internal Thermal Overload Protection**
- **Internal Short-Circuit Current Limiting**
- **Direct Replacement for Motorola MC79L00 Series**
- **Available in 5% or 10% Selections**

D PACKAGE
(TOP VIEW)



† Internally connected

LP SILENT PACKAGE
(TOP VIEW)



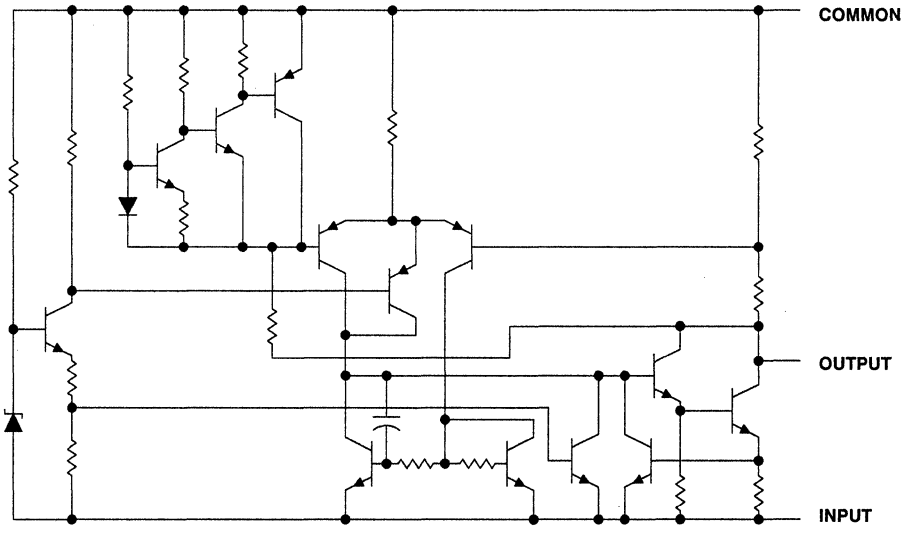
NC–No internal connection

description

This series of fixed negative-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features make them essentially immune to overload. When used as a replacement for a zener diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude and lower bias current.

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
–5 V	MC79L05AC	MC79L05C
–12 V	MC79L12AC	MC79L12C
–15 V	MC79L15AC	MC79L15C

equivalent schematic



absolute maximum ratings over operating temperature ranges (unless otherwise noted)

	MC79L05	MC79LI2 MC79L15	UNIT
Input voltage	−30	−35	V
Continuous total dissipation	See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range	0 to 150	0 to 150	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	825 mW	6.6 mW/°C	25°C	528 mW
LP†	775 mW	6.2 mW/°C	25°C	496 mW

† The LP package dissipation rating is based on thermal resistance measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.0 mW/°C	95°C	725 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	MC79L05	−7	−20	V
	MC79L12	−14.5	−27	
	MC79L15	−17.5	−30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = –10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J‡	MC79L05C			MC79L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage§		25°C	–4.6	–5	–5.4	–4.8	–5	–5.2	V
	V_I = –7 V to –20 V, I_O = 1 mA to 40 mA	Full range	–4.5		–5.5	–4.75		–5.25	
	V_I = –10 V, I_O = 1 mA to 70 mA	Full range	–4.5		–5.5	–4.75		–5.25	
Input regulation	V_I = –7 V to –20 V	25°C			200			150	mV
	V_I = –8 V to –20 V				150			100	
Ripple rejection	V_I = –8 V to –18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			60			60	mV
	I_O = 1 mA to 40 mA				30			30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6			6	mA
		125°C			5.5			5.5	
Bias current change	V_I = –8 V to –20 V	Full range			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

electrical characteristics at specified virtual junction temperature, V_I = –19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J‡	MC79L12C			MC79L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage§		25°C	–11.1	–12	–12.9	–11.5	–12	–12.5	V
	V_I = –14.5 V to –27 V, I_O = 1 mA to 40 mA	Full range	–10.8		–13.2	–11.4		–12.6	
	V_I = –19 V, I_O = 1 mA to 70 mA	Full range	–10.8		–13.2	–11.4		–12.6	
Input regulation	V_I = –14.5 V to –27 V	25°C			250			250	mV
	V_I = –16 V to –27 V				200			200	
Ripple rejection	V_I = –15 V to –25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			100			100	mV
	I_O = 1 mA to 40 mA				50			50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = –16 V to –27 V	Full range			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Full range virtual junction temperature is 0°C to 125°C.

§ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = –23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J‡	MC79L15C			MC79L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage§		25°C	–13.8	–15	–16.2	–14.4	–15	–15.6	V
	V_I = –17.5 V to –30 V, I_O = 1 mA to 40 mA	Full range	–13.5		–16.5	–14.25		–15.75	
	V_I = –23 V, I_O = 1 mA to 70 mA	Full range	–13.5		–16.5	–14.25		–15.75	
Input regulation	V_I = –17.5 V to –30 V	25°C			300			300	mV
	V_I = –17.5 V to –30 V				250			250	
Ripple rejection	V_I = –18.5 V to –28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			150			150	mV
	I_O = 1 mA to 40 mA				75			75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = –20 V to –30 V	Full range			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

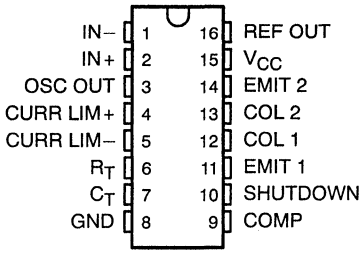
‡ Full range virtual junction temperature is 0°C to 125°C.

§ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

D2294, APRIL 1977–REVISED DECEMBER 1991

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for Single-Ended or Push-Pull Applications**
- **Low Standby Current . . . 8 mA Typ**
- **Interchangeable With Silicon General SG2524 and SG3524**

N PACKAGE
(TOP VIEW)

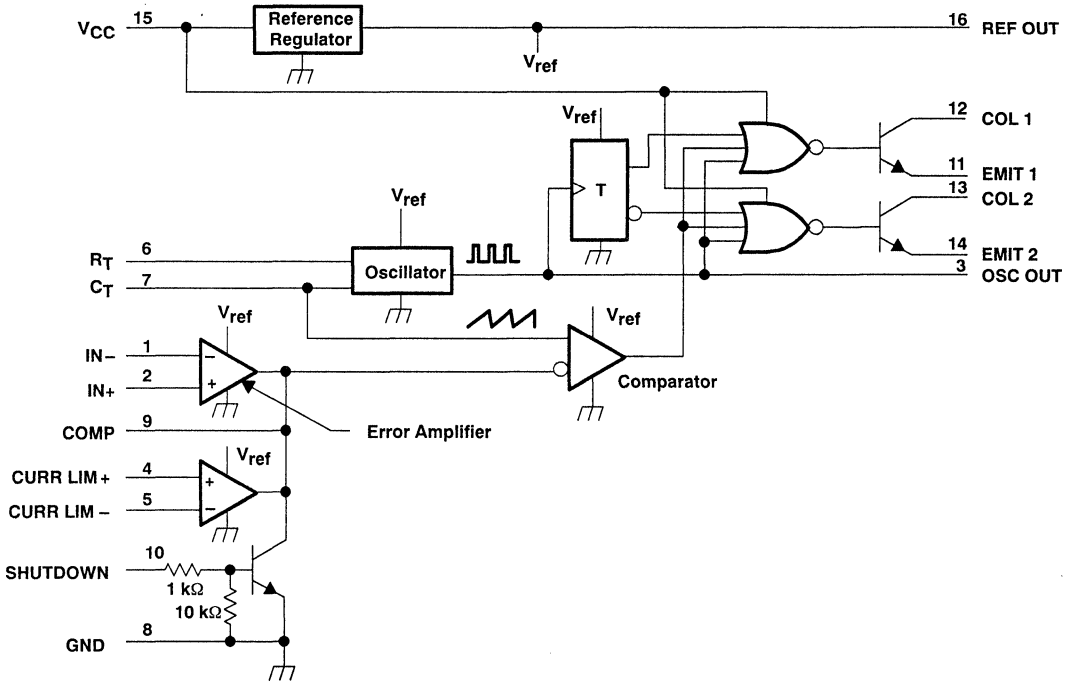


description

The SG2524 and SG3524 incorporate on single monolithic chips all the functions required in the construction of a regulating power supply, inverter, or switching regulator. They can also be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width-modulation techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

The SG2524 is characterized for operation from −25°C to 85°C, and the SG3524 is characterized for operation from 0°C to 70°C.

functional block diagram



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2) ..... 40 V
Collector output current ..... 100 mA
Reference output current ..... 50 mA
Current through C_T terminal ..... −5 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SG2524 ..... −25°C to 85°C
SG3524 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The reference regulator may be bypassed for operation from a fixed 5-V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration, the maximum supply voltage is 6 V.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1000 mW	9.2 mW/ °C	41°C	736 mW	598 mW

recommended operating conditions

	SG2524		SG3524		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	8	40	8	40	V
Reference output current	0	50	0	50	mA
Current through C_T terminal	−0.03	−2	−0.03	−2	mA
Timing resistor, R_T	1.8	100	1.8	100	kΩ
Timing capacitor, C_T	0.001	0.1	0.001	0.1	μF
Operating free-air temperature	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	SG2524			SG3524			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage		4.8	5	5.2	4.6	5	5.4	V
Input regulation	V_{CC} = 8 V to 40 V		10	20		10	30	mV
Ripple rejection	f = 120 Hz		66			66		dB
Output regulation	I_O = 0 mA to 20 mA		20	50		20	50	mV
Output voltage change with temperature	T_A = MIN to MAX		0.3%	1%		0.3%	1%	
Short-circuit output current§	V_{ref} = 0		100			100		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values, except output voltage change with temperature, are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

oscillator section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
f_{osc}	Oscillator frequency	C_T = 0.001 μF, R_T = 2 kΩ		450		kHz
	Standard deviation of frequency§	All values of voltage, temperature, resistance, and capacitance constant		5%		
Δf_{osc}	Frequency change with voltage	V_{CC} = 8 V to 40 V, T_A = 25°C			1%	
Δf_{osc}	Frequency change with temperature	T_A = MIN to MAX			2%	
	Output amplitude at OSC OUT	T_A = 25°C		3.5		V
t_w	Output pulse duration (width) at OSC OUT	C_T = 0.01 μF, T_A = 25°C		0.5		μs

error amplifier section

PARAMETER		TEST CONDITIONS†	SG2524			SG3524			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{IC} = 2.5 V		0.5	5		2	10	mV
I_{IB}	Input bias current	V_{IC} = 2.5 V		2	10		2	10	μA
	Open-loop voltage amplification		72	80		60	80		dB
V_{ICR}	Common-mode input voltage range	T_A = 25°C	1.8 to 3.4			1.8 to 3.4			V
CMMR	Common-mode rejection ratio			70			70		dB
B_1	Unity-gain bandwidth			3			3		MHz
	Output swing	T_A = 25°C	0.5		3.8	0.5		3.8	V

output section

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{(BR)CE}$	Collector-emitter breakdown voltage		40			V
	Collector off-state current	V_{CE} = 40 V		0.01	50	μA
V_{sat}	Collector-emitter saturation voltage	I_C = 50 mA		1	2	V
V_O	Emitter output voltage	V_C = 20 V, I_E = −250 μA	17	18		V
t_r	Turn-off voltage rise time	R_C = 2 kΩ		0.2		μs
t_f	Turn-on voltage fall time	R_C = 2 kΩ		0.1		μs

comparator section

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
	Maximum duty cycle, each output		45%			
V_T	Input threshold voltage at COMP	Zero duty cycle		1		V
		Maximum duty cycle		3.5		
I_{IB}	Input bias current			−1		μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values, except for temperature coefficients, are at T_A = 25°C

§ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$$

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V, f = 20 kHz (unless otherwise noted)

current limiting section

PARAMETER		TEST CONDITIONS	SG2524			SG3524			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage range (either input)		−1 to 1			−1 to 1			V
$V_{(sense)}$	Sense voltage at T_A = 25°C	$V_{(IN+)} - V_{(IN-)} \geq 50$ mV,	190	200	210	180	200	220	mV
	Temperature coefficient of sense voltage	$V_{(COMP)}$ = 2 V		0.2			0.2		mV/°C

total device

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{st}	Standby current	V_{CC} = 40 V, IN+ at 2 V,	IN−, CURR LIM+, C_T, GND, COMP, EMIT 1, EMIT 2 grounded All other inputs and outputs open		8	10	mA

† All typical values, except for temperature coefficients, are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

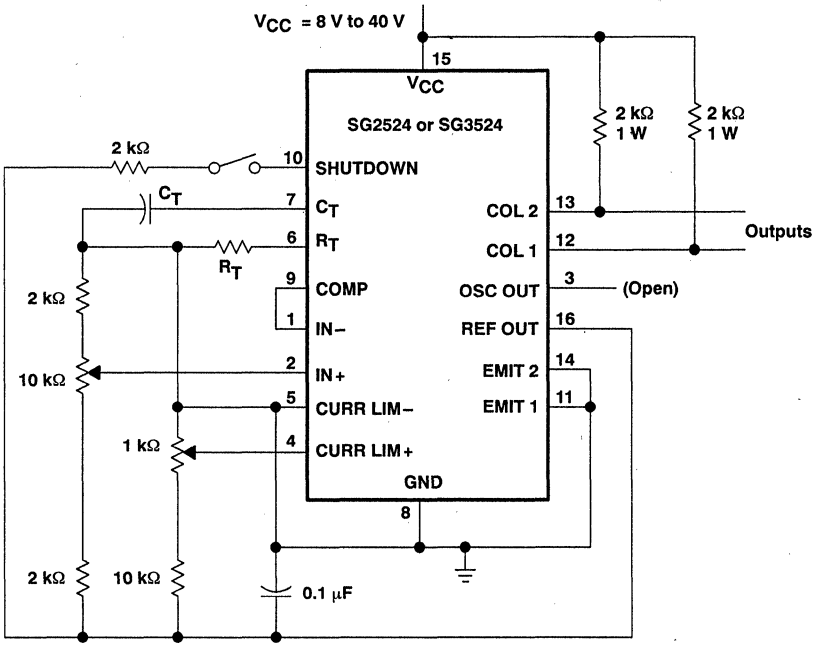


Figure 1. General Test Circuit

PARAMETER MEASUREMENT INFORMATION

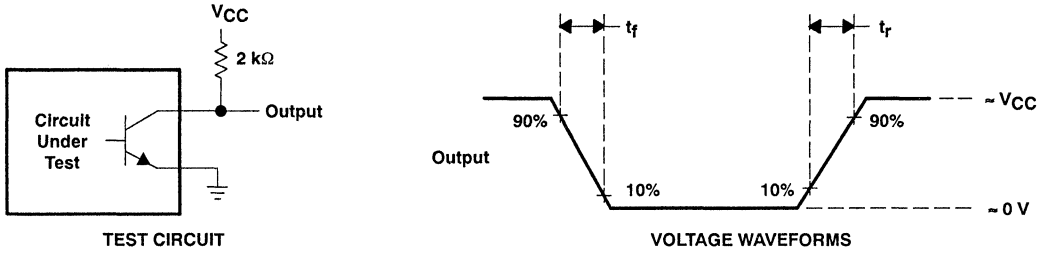


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE AMPLIFICATION
OF ERROR AMPLIFIER
vs
FREQUENCY

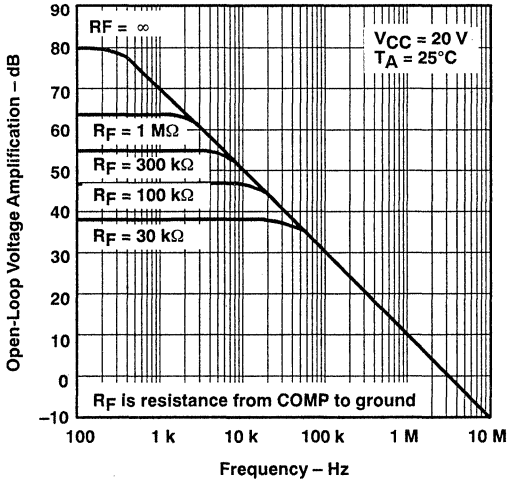


Figure 3

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

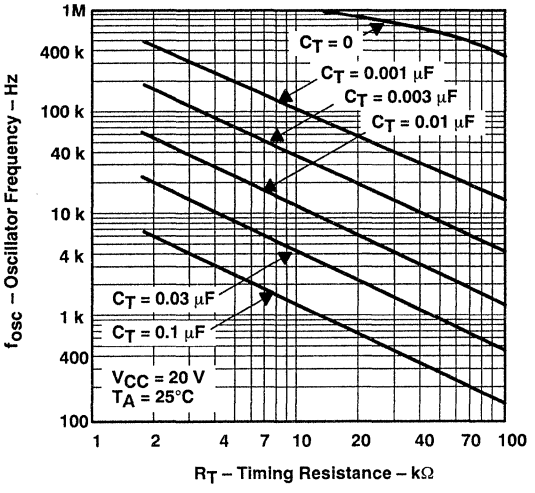


Figure 4

TYPICAL CHARACTERISTICS

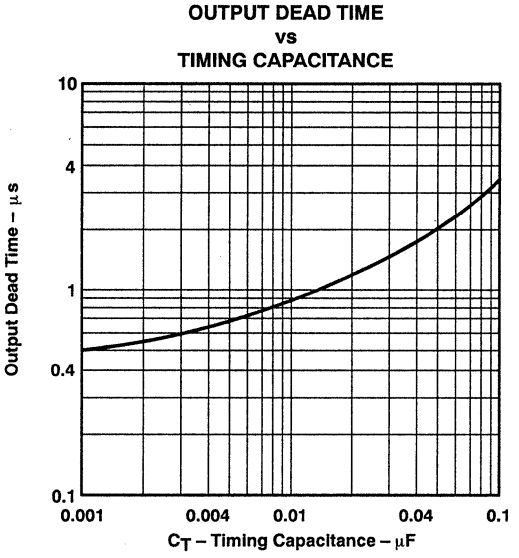


Figure 5

PRINCIPLES OF OPERATION†

The SG2524 is a fixed-frequency pulse-width-modulation voltage-regulator control circuit. The regulator operates at a fixed frequency that is programmed by one timing resistor R_T and one timing capacitor C_T. R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse duration (width) by the error amplifier. The SG2524 contains an on-board 5-V regulator that serves as a reference as well as supplying the SG2524 internal regulator control circuitry. The internal reference voltage is divided externally by a resistor ladder network to provide a reference within the common-mode range of the error amplifier as shown in Figure 6, or an external reference may be used. The output is sensed by a second resistor divider network and the error signal is amplified. This voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q1 or Q2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The duration of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current-limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, to compensate the error amplifier, or to provide additional control to the regulator.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

oscillator

The oscillator controls the frequency of the SG2524 and is programmed by R_T and C_T as shown in Figure 4.

$$f \approx \frac{1.30}{R_T\ C_T}$$

where R_T is in kΩ
C_T is in μF
f is in kHz

Practical values of C_T fall between 0.001 and 0.1 μF. Practical values of R_T fall between 1.8 and 100 kΩ. This results in a frequency range typically from 140 Hz to 500 kHz.

blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse duration is controlled by the value of C_T as shown in Figure 5. If small values of C_T are required, the oscillator output pulse duration may still be maintained by applying a shunt capacitance from OSC OUT to ground.

synchronous operation

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kΩ. In this configuration, R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more SG2524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other SG2524s operate. In this application, the C_T R_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a longer pulse duration and will subsequently reset the slave regulators.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

voltage reference

The 5-V internal reference may be employed by use of an external resistor divider network to establish a reference within the error amplifiers common-mode voltage range (1.8 V to 3.4 V) as shown in Figure 6, or an external reference may be applied directly to the error amplifier. For operation from a fixed 5-V supply, the internal reference may be bypassed by applying the input voltage to both the V_{CC} and V_{REF} terminals. In this configuration, however, the input voltage is limited to a maximum of 6 V.

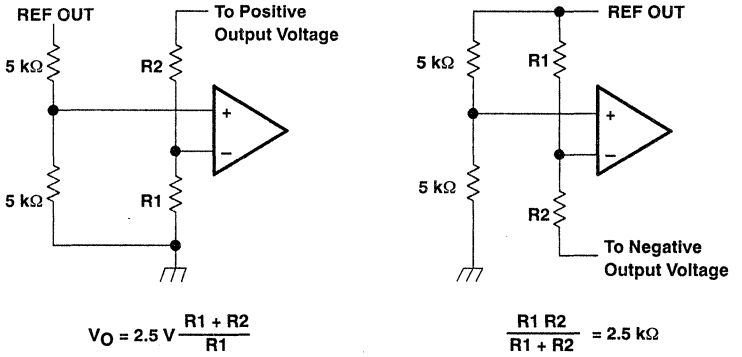


Figure 6. Error Amplifier Bias Circuits

error amplifier

The error amplifier is a differential-input transconductance amplifier. The output is available for dc gain control or ac phase compensation. The compensation node (COMP) is a high-impedance node (R_L = 5 MΩ). The gain of the amplifier is $A_V = (0.002\ \Omega^{-1})R_L$ and can easily be reduced from a nominal 10,000 by an external shunt resistance from COMP to ground. Refer to Figure 3 for data.

compensation

COMP, as discussed above, is made available for compensation. Since most output filters will introduce one or more additional poles at frequencies below 200 Hz, which is the pole of the uncompensated amplifier, introduction of a zero to cancel one of the output filter poles is desirable. This can best be accomplished with a series RC circuit from COMP to ground in the range of 50 kΩ and 0.001 μF. Other frequencies can be canceled by use of the formula $f \approx 1/RC$.

shut-down circuitry

COMP can also be employed to introduce external control of the SG2524. Any circuit that can sink 200 μA can pull the compensation terminal to ground and thus disable the SG2524.

In addition to constant-current limiting, CURR LIM+ and CURR LIM− may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse should transformer saturation occur. CURR LIM− may also be grounded to convert CURR LIM+ into an additional shut-down terminal.

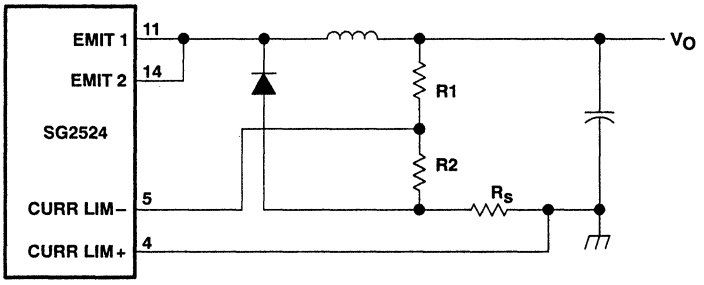
† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

current limiting

A current-limiting sense amplifier is provided in the SG2524. The current-limiting sense amplifier exhibits a threshold of 200 mV and must be applied in the ground line since the voltage range of the inputs is limited to +1 V to −1 V. Caution should be taken to ensure the −1 V limit is not exceeded by either input, otherwise damage to the device may result.

Foldback current limiting can be provided with the network shown in Figure 7. The current-limit schematic is shown in Figure 8.



$$I_{O(max)} = \frac{1}{R_S}\left(V_{(sense)} + \frac{V_O\ R2}{R1 + R2}\right)$$

$$I_{OS} = \frac{V_{(sense)}}{R_S} \text{ where } V_{(sense)} = 20 \text{ mV}$$

Figure 7. Foldback Current Limiting for Shorted Output Conditions

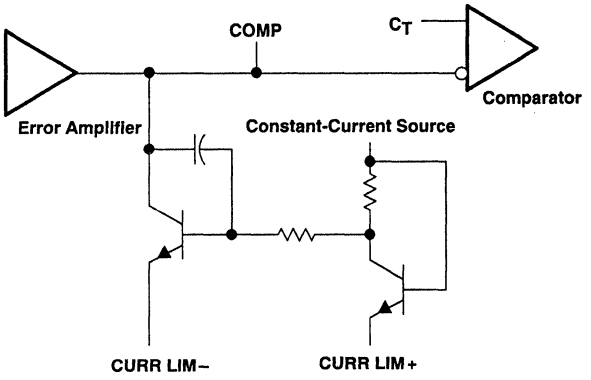


Figure 8. Current-Limit Schematic

output circuitry

The SG2524 contains two identical n-p-n transistors, the collectors and emitters of which are uncommitted. Each transistor has antisaturation circuitry that limits the current through that transistor to a maximum of 100 mA for fast response.

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

general

There are a wide variety of output configurations possible when considering the application of the SG2524 as a voltage regulator control circuit. They can be segregated into three basic categories:

1. Capacitor-diode-coupled voltage multipliers
2. Inductor-capacitor-implemented single-ended circuits
3. Transformer-coupled circuits

Examples of these categories are shown in Figures 9, 10 and 11, respectively. Detailed diagrams of specific applications are shown in Figures 12 through 15.

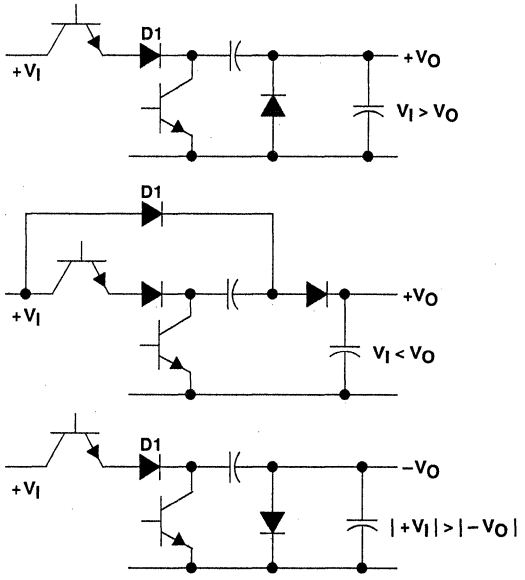


Figure 9. Capacitor-Diode-Coupled Voltage-Multiplier Output Stages

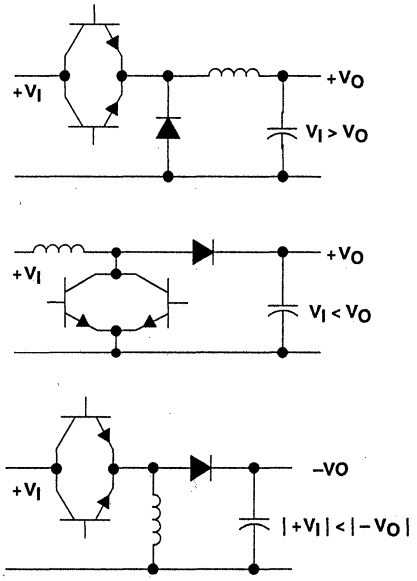


Figure 10. Single-Ended Inductor Circuit

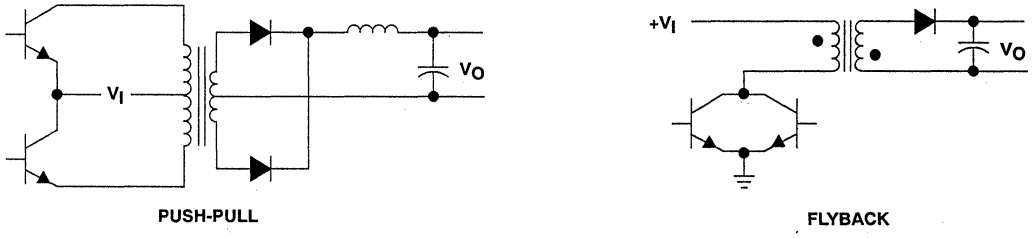


Figure 11. Transformer-Coupled Outputs

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

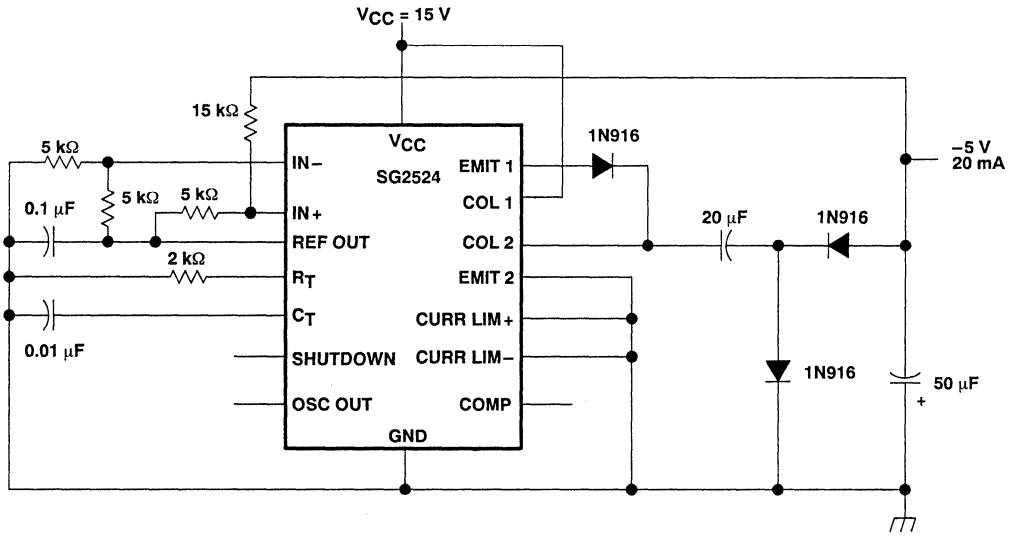


Figure 12. Capacitor-Diode Output Circuit

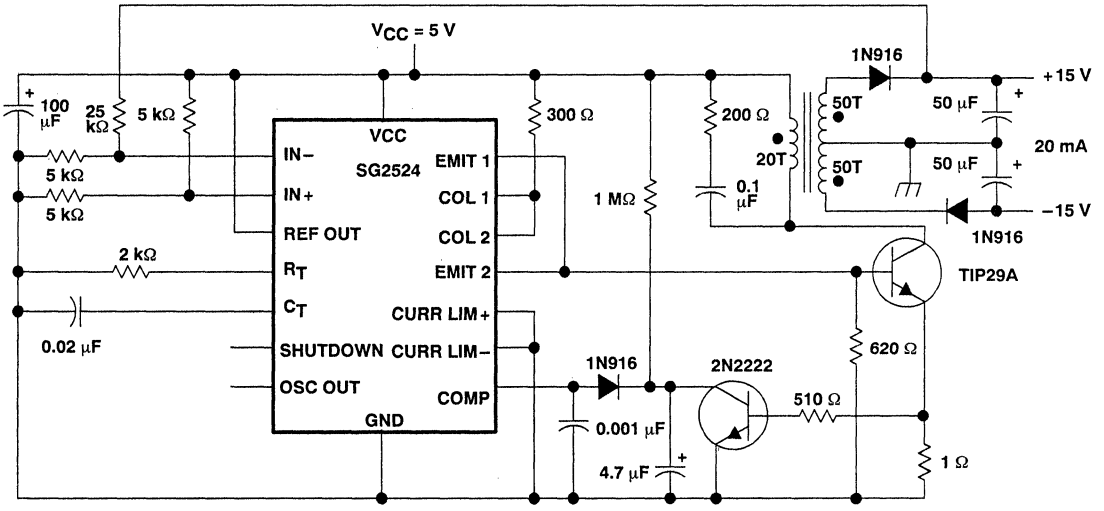


Figure 13. Flyback Converter Circuit

† Throughout these discussions, references to the SG2524 apply also to the SG3524.

APPLICATION INFORMATION†

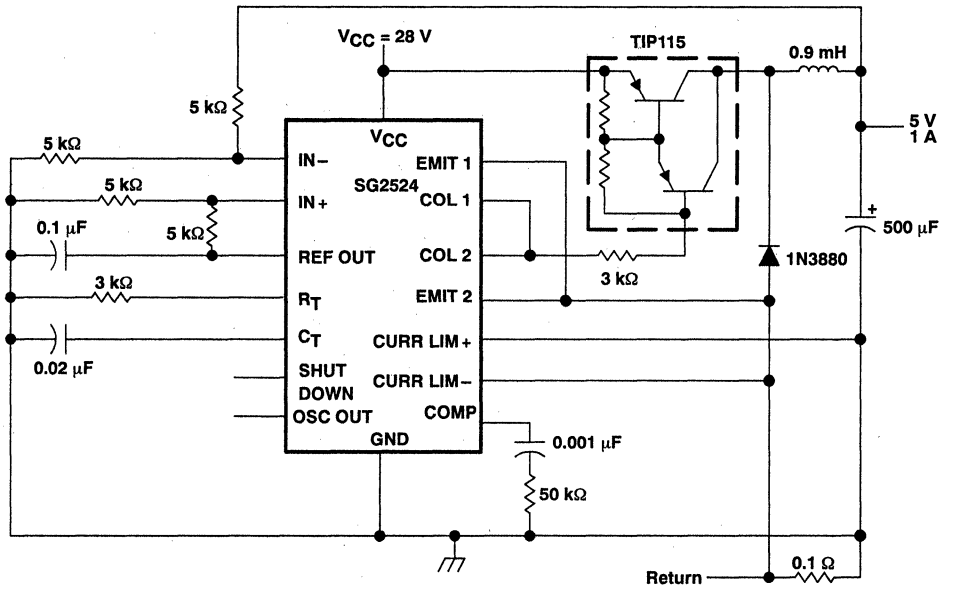


Figure 14. Single-Ended LC Circuit

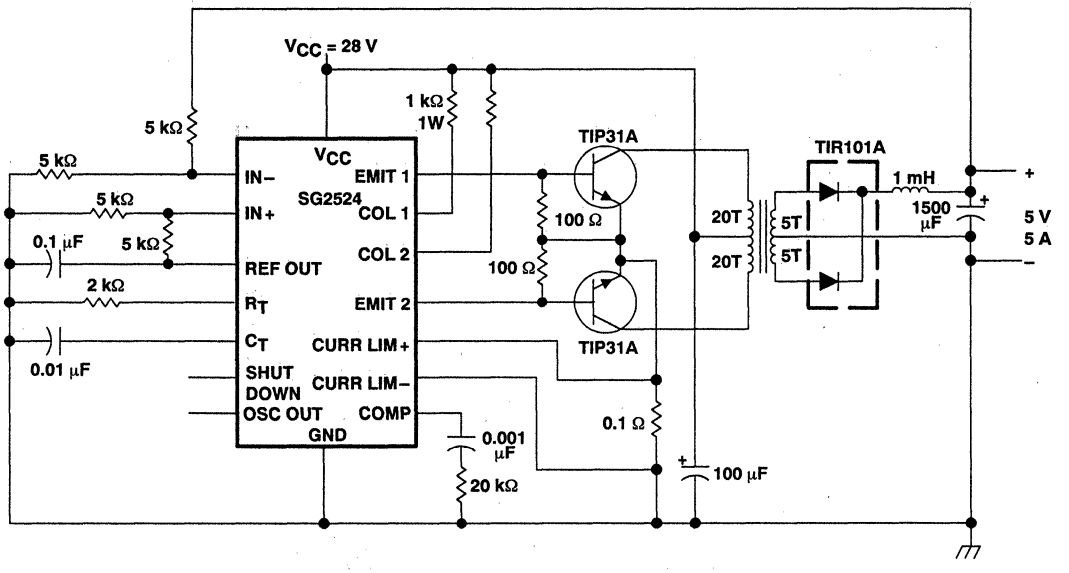


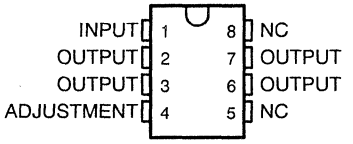
Figure 15. Push-Pull Transformer-Coupled Circuit

†Throughout these discussions, references to the SG2524 apply also to the SG3524.

D2527, APRIL 1979–REVISED AUGUST 1991

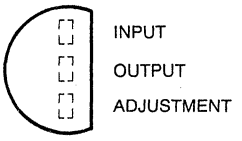
- **Output Voltage Range Adjustable From 1.2 V to 32 V When Used With an External Resistor Divider**
- **Output Current Capability of 100 mA**
- **Input Regulation Typically 0.01% Per Input-Voltage Change**
- **Output Regulation Typically 0.5%**
- **Ripple Rejection Typically 80 dB**

D PACKAGE
(TOP VIEW)



NOTE: OUTPUT terminals are all internally connected.

LP SILECT PACKAGE
(TOP VIEW)



NC–No internal connection

description

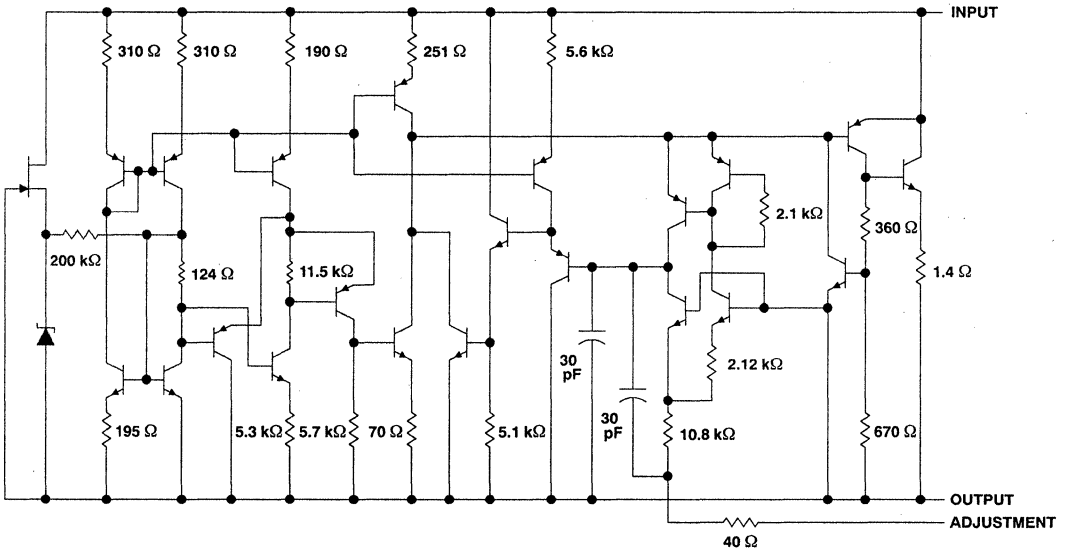
The TL317C is an adjustable 3-terminal positive-voltage regulator capable of supplying 100 mA over an output-voltage range of 1.2 V to 32 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The device is packaged in standard packages that are easily mounted and handled.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload protection circuitry remains fully functional even if ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

In addition to replacing fixed regulators, the TL317C regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.2 V where most loads draw little current.

The TL317C is characterized for operation from 0°C to 125°C.

schematic



All component values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ ..... 35 V
Continuous total dissipation ..... See Dissipation Rating Tables 1 and 2
Operating free-air, case, or virtual-junction temperature range ..... 0°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	145 mW
LP†	775 mW	6.2 mW/°C	155 mW

† The LP package dissipation rating is based on thermal resistance measured in still air with the device mounted in an Augat socket. The bottom of the package is 10 mm (0.375 in.) above the socket.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	29.6 mW/°C	96°C	740 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		35	V
Output current, I_O	2.5	100	mA
Operating virtual-junction temperature, T_J	0	125	°C

electrical characteristics over recommended operating virtual-junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Input regulation (see Note 1)	$V_I - V_O$ = 3 V to 35 V	T_J = 25°C		0.01	0.02	%/V
		I_O = 2.5 mA to 100 mA		0.02	0.05	
Ripple regulation	V_O = 10 V,	f = 120 Hz		65		dB
	V_O = 10 V, 10-μF capacitor between ADJUSTMENT and ground	f = 120 Hz,	66	80		
Output regulation	I_O = 2.5 mA to 100 mA, T_J = 25°C	$V_O \le 5$ V		25		mV
		$V_O \ge 5$ V		0.5%		
	I_O = 2.5 mA to 100 mA	$V_O \le 5$ V		50		mV
		$V_O \ge 5$ V		1%		
Output voltage change with temperature	T_J = 0°C to 125°C			1%		
Output voltage long-term drift (see Note 2)	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35 V			0.3%	1%	
Output noise voltage	f = 10 Hz to 10 kHz,	T_J = 25°C		0.003%		
Minimum output current to maintain regulation	$V_I - V_O$ = 35 V			1.5	2.5	mA
Peak output current	$V_I - V_O \le 35$ V		100	200		mA
ADJUSTMENT current				50	100	μA
Change in ADJUSTMENT current	$V_I - V_O$ = 2.5 V to 35 V,	I_O = 2.5 mA to 100 mA		0.2	5	μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 3 V to 35 V, P ≤ rated dissipation	I_O = 2.5 mA to 100 mA,	1.2	1.25	1.3	V

† Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 40 mA. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible. All characteristics are measured with a 0.1-μF capacitor across the input and a 1-μF capacitor across the output.

NOTES: 1. Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input
2. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

APPLICATION INFORMATION

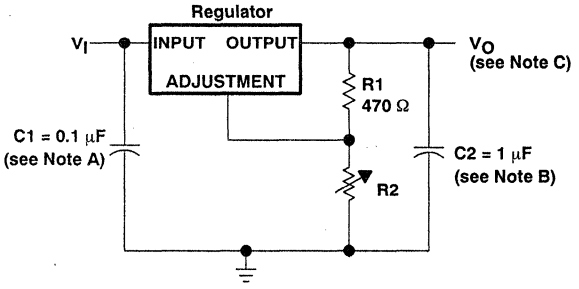


Figure 1. Adjustable Voltage Regulator

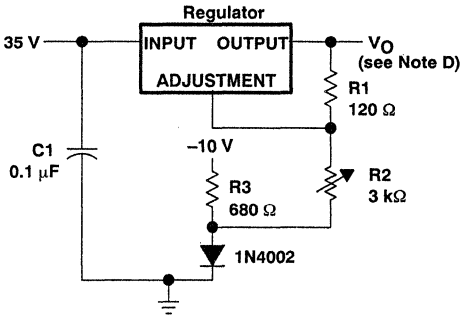
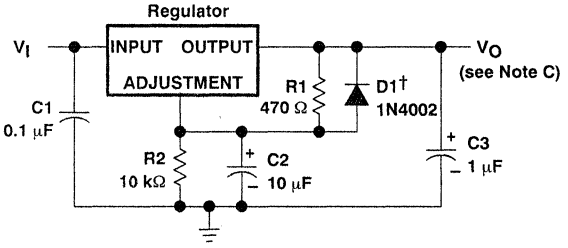


Figure 2. 0-V to 30-V Regulator Circuit



† D1 discharges C2 if output is shorted to ground.

Figure 3. Regulator Circuit
With Improved Ripple Rejection

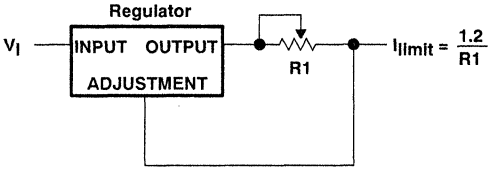


Figure 4. Precision Current-Limiter Circuit

NOTES: A. Use of an input bypass capacitor is recommended if regulator is far from the filter capacitors.

B. Use of an output capacitor improves transient response but is optional.

C. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2}{R1}\right)$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages.

D. Output voltage is calculated from the equation: $V_O = V_{ref}\left(1 + \frac{R2 + R3}{R1}\right) - 10\ V$

where: V_{ref} equals the difference between OUTPUT and ADJUSTMENT voltages.

APPLICATION INFORMATION

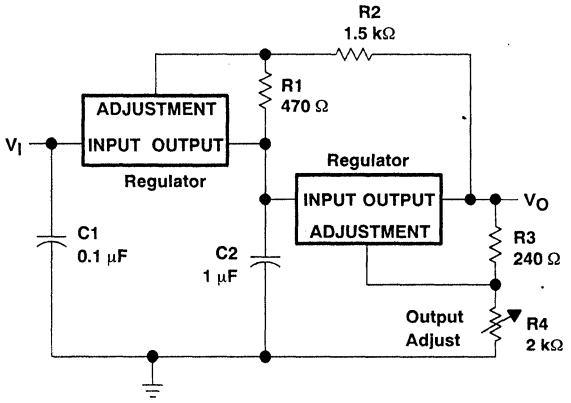


Figure 5. Tracking Preregulator Circuit

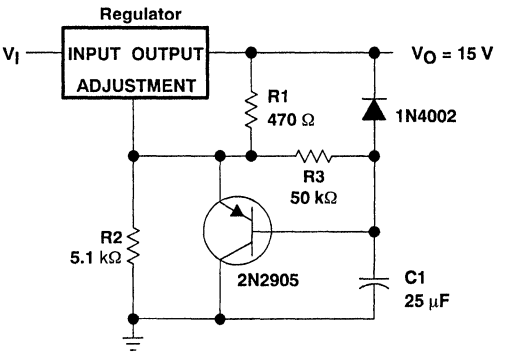


Figure 6. Slow-Turn-On 15-V Regulator Circuit

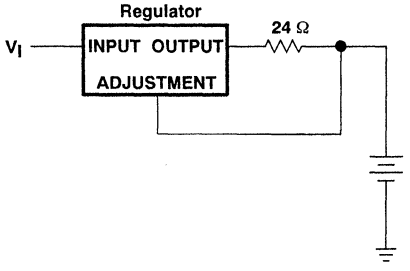
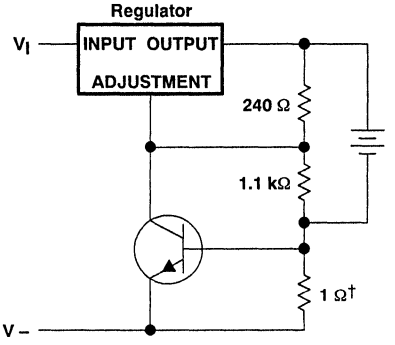


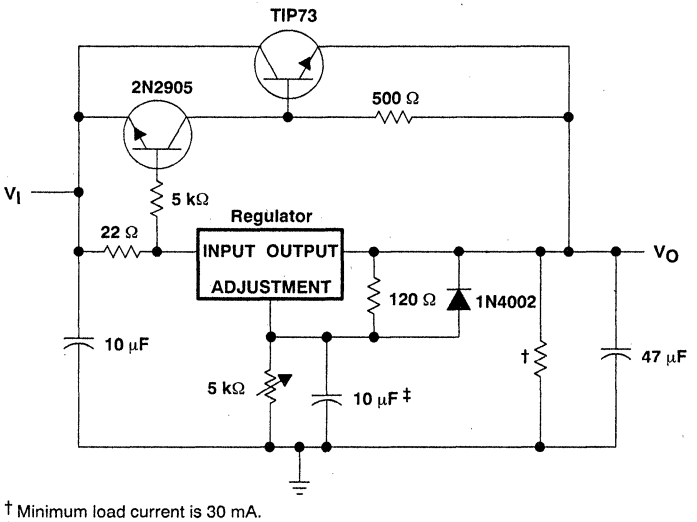
Figure 7. 50-mA Constant-Current Battery Charger Circuit



† This resistor sets peak current (100 mA for 6 Ω).

Figure 8. Current-Limited 6-V Charger

APPLICATION INFORMATION

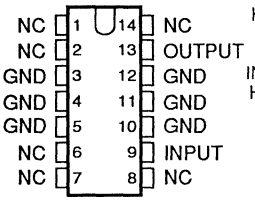


† Minimum load current is 30 mA.
‡ Optional capacitor improves ripple rejection

Figure 9. High-Current Adjustable Regulator

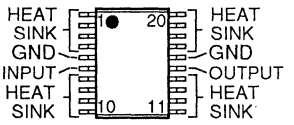
- **Fully Matches Parameters for Alternative 2 SCSI Active Termination**
- **Fixed 2.85-V Output**
- **±1% Maximum Output Tolerance at T_J = 25°C**
- **0.6-V Maximum Dropout Voltage**
- **620-mA Output Current**
- **±2% Absolute Output Variation**
- **Internal Overcurrent Limiting Circuitry**
- **Internal Thermal Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



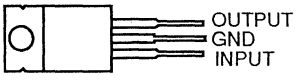
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE
(TOP VIEW)

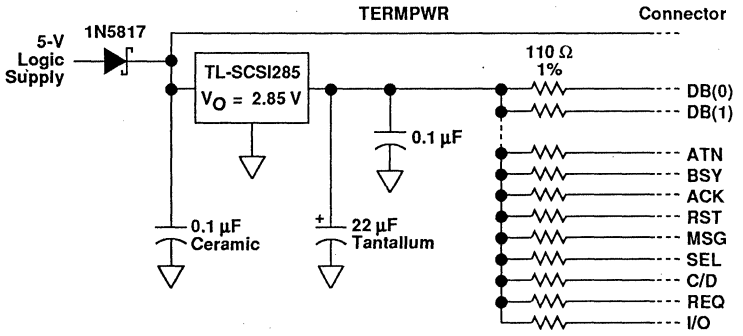


description

The TL-SCSI285 is a low-dropout (0.6-V) fixed voltage regulator specifically designed for Small Computer Systems Interface (SCSI) alternative 2 active signal termination. The TL-SCSI285's 0.6-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the ±1% initial tolerance on its 2.85-V output voltage ensures a tighter line driver current tolerance, thereby increasing system noise margin.

The fixed 2.85-V output voltage of the TL-SCSI285 supports the SCSI alternative 2 termination standard while reducing system power consumption. The 0.6-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL-SCSI285, with internal current limiting,

typical application schematic



AVAILABLE OPTIONS

T_J	PACKAGE		
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†
0°C to 125°C	TL-SCSI285KC	TL-SCSI285N	TL-SCSI285PWLE

†The PW package is only available left-end taped and reeled.

description (continued)

overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

When configured as a SCSI active terminator, the TL-SCSI285 low-dropout regulator eliminates the 220-Ω and 330-Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with 110-Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

The TL-SCSI285 is characterized for operation from 0°C to 125°C virtual junction temperature.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Continuous input voltage . . . . . 7.5 V
Continuous total dissipation (see Note 1) . . . . . See Dissipation Rating Table
Operating virtual junction temperature range . . . . . –55°C to 150°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16 mW/°C	1280 mW	1040 mW	400 mW
	T_C	20000 mW	182 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	775 mW	6.4 mW/°C	520 mW	423 mW	161 mW

Derate above 40°C

DISSIPATION DERATING CURVE vs FREE-AIR TEMPERATURE

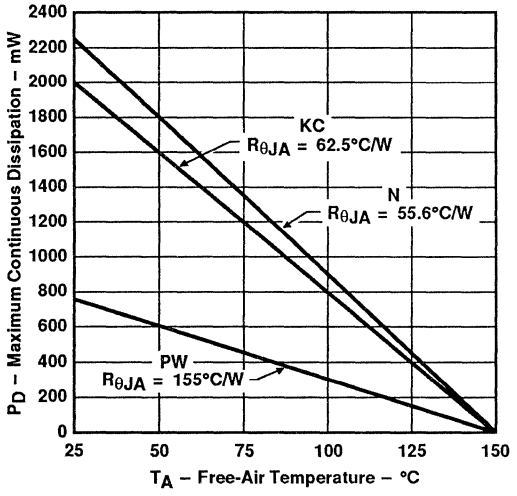


Figure 1

DISSIPATION DERATING CURVE vs CASE TEMPERATURE

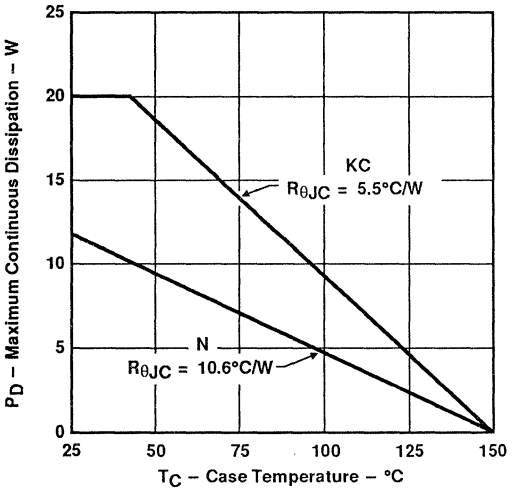


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		3.45	5.5	V
Output current, I_O	KC and N packages	0	620	mA
	PW package	0	500	mA
Operating virtual junction temperature range, T_J		0	125	°C

TL-SCSI285KC, TL-SCSI285N electrical characteristics at, V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 620 mA, V_I = 3.45 V to 5.5 V	$T_A = T_J$ = 25°C	2.82	2.85	2.88	V
		T_J = 0 to 125°C	2.79		2.91	
Input regulation	V_I = 3.45 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}			–62		dB
Output regulation	I_O = 20 mA to 620 mA			5	30	mV
	I_O = 20 mA to 500 mA			5	30	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 500 mA				0.6	V
	I_O = 620 mA				0.8	
Bias current	I_O = 0			2	5	mA
	I_O = 27 mA, equivalent 1 line asserted			3	6	
	I_O = 500 mA, equivalent 18 line asserted (8 bit)			26	49	
	I_O = 620 mA			37	62	

TL-SCSI285PW electrical characteristics at, V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.55 V to 5.5 V	$T_A = T_J$ = 25°C	2.82	2.85	2.88	V
		T_J = 0 to 125°C	2.79		2.91	
Input regulation	V_I = 3.55 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}			–62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 500 mA				0.7	V
Bias current	I_O = 0			2	5	mA
	I_O = 27 mA, equivalent 1 line asserted			3	6	
	I_O = 500 mA, equivalent 18 line asserted (8 bit)			26	49	

Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TL-SCSI285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

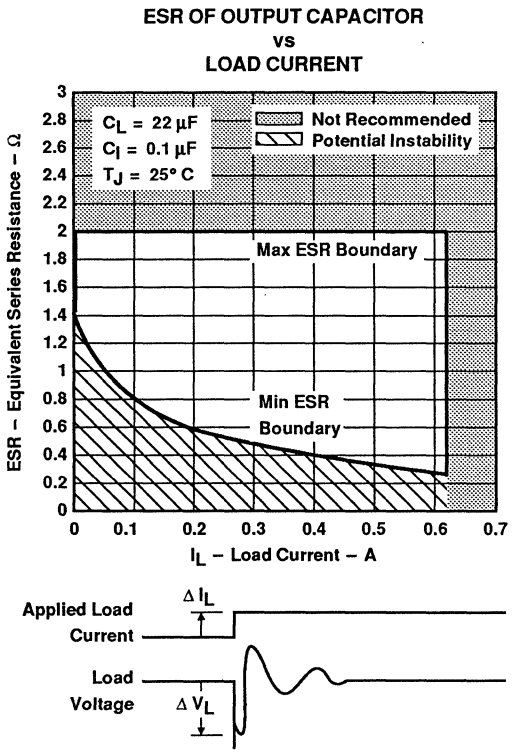


Figure 3

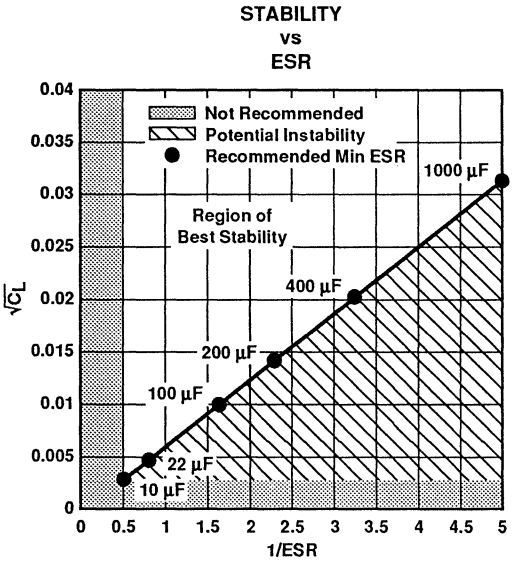
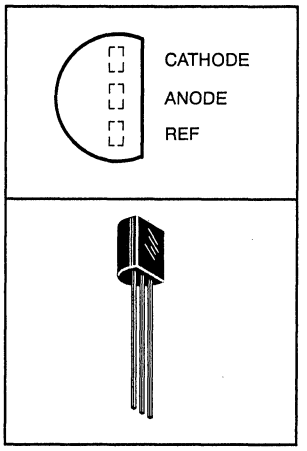


Figure 4

D2165, JUNE 1976–REVISED AUGUST 1991

- **Temperature Compensated**
- **Programmable Output Voltage**
- **Low Output Resistance**
- **Low Output Noise**
- **Sink Capability to 100 mA**

LP PACKAGE
(TOP VIEW)

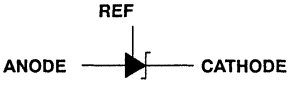


description

The TL430 is a 3-terminal adjustable shunt regulator featuring excellent temperature stability, wide operating current range, and low output noise. The output voltage may be set by two external resistors to any desired value between 3 V and 30 V. The TL430 can replace zener diodes in many applications providing improved performance

The TL430C is characterized for operation from 0°C to 70°C. The TL430I is characterized for operation from −40°C to 85°C.

symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Regulator voltage (see Note 1) ..... 30 V
Continuous regulator current ..... 150 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 775 mW
Operating free-air temperature range: TL430C ..... 0°C to 70°C
TL430I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the anode terminal.
2. For operation above 25°C free-air temperature, derate at 6.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Regulator voltage, V_Z		V_{ref}	30	V
Regulator curent, I_Z		2	100	mA
Operating free-air temperature, T_A	TL430C	0	70	°C
	TL430I	−40	85	

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		TL430C			TL430I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_Z = V_{ref}$,	I_Z = 10 mA	2.5	2.75	3	2.6	2.75	2.9	V
αV_{ref}	Temperature coefficient of reference input voltage	1	$V_Z = V_{ref}$, T_A = full range†	I_Z = 10 mA,		120			120	200	ppm/°C
I_{ref}	Reference input current	2	I_Z = 10 mA, R2 = ∞	R1 = 10 kΩ,		3	10		3	10	μA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{ref}$			0.5	2		0.5	2	mA
I_{ZM}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{ref}$		50			50			mA
		2	V_Z = 5 V to 30 V,	See Note 3	100			100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{ref}$, ΔI_Z = (52 – 2) mA			1.5	3		1.5	3	Ω
V_{nz}	Noise voltage	2	f = 0.1 Hz to 10 Hz	V_Z = 3 V		50			50		μV
				V_Z = 12 V		200			200		
				V_Z = 30 V		650			650		

† Full temperature range is 0°C to 70°C for the TL430C and –40°C to 85°C for the TL430I.

NOTES: 3. The average power dissipation, $V_Z \cdot I_Z$ • duty cycle, must not exceed the maximum continuous rating in any 10-ms interval.

4. The regulator resistance for $V_Z > V_{ref}$, r_z, is given by:

$$r_z' = r_z \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

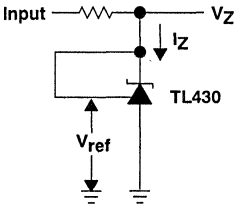
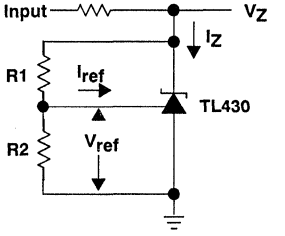


Figure 1. Test Circuit for $V_Z = V_{ref}$



$$V_Z = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \times R1$$

Figure 2. Test Circuit for $V_Z > V_{ref}$

TYPICAL CHARACTERISTICS

SMALL-SIGNAL REGULATOR IMPEDANCE
vs
FREQUENCY

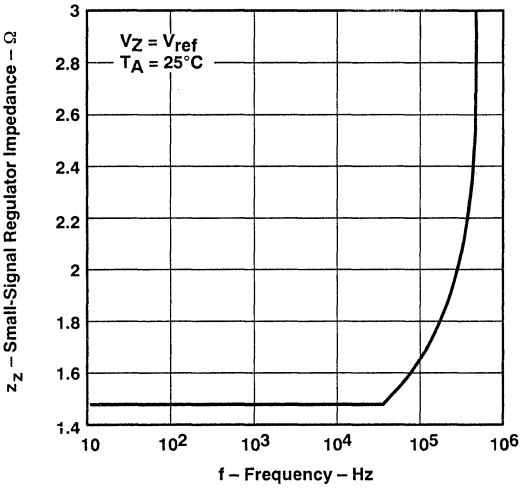


Figure 3

CURRENT
vs
VOLTAGE

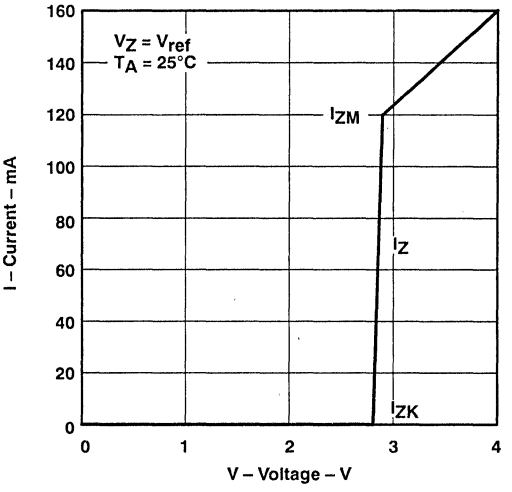
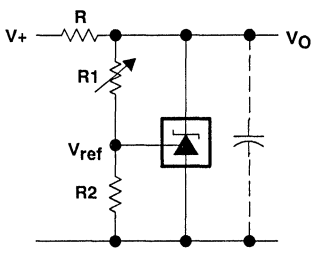


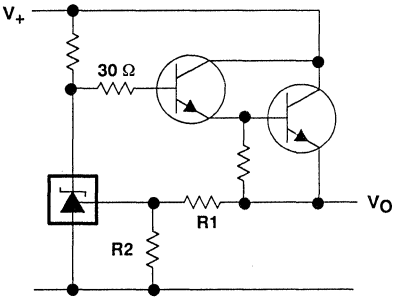
Figure 4

APPLICATION INFORMATION



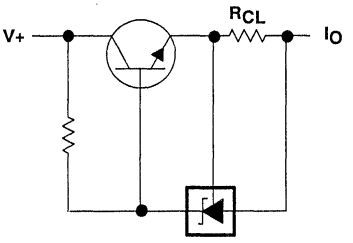
$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 5. Shunt Regulator



$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{ref}$$

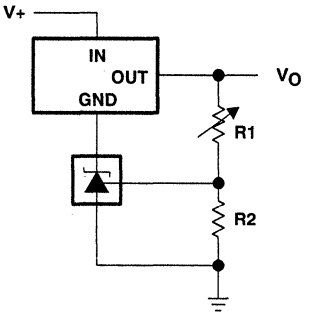
Figure 6. Series Regulator



$$I_O \approx \frac{V_{ref}}{R_{CL}}$$

Figure 7. Current Limiter

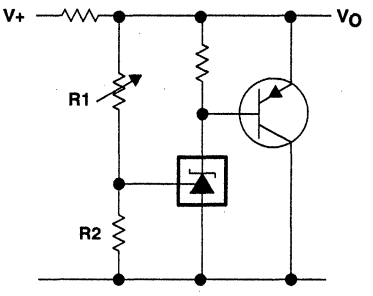
APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right)$$

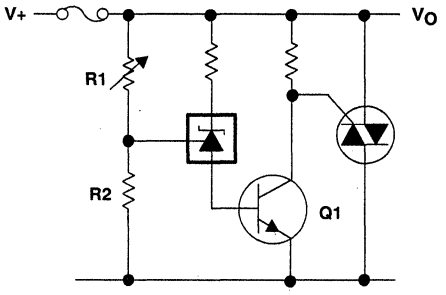
$$\text{Min } V_O = V_{ref} + 5$$

Figure 8. Output Control of a 3-Terminal Fixed Regulator



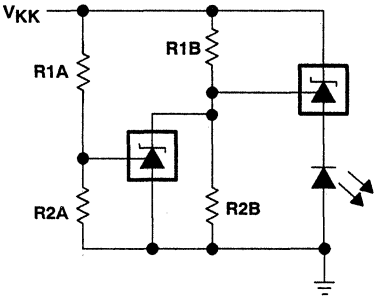
$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 9. Higher-Current Applications



$$V_{limit} \approx \left(1 + \frac{R1}{R2}\right)\left(V_{ref} + V_{BE(Q1)}\right)$$

Figure 10. Crowbar



$$\text{Low limit} \approx V_{ref}\left(1 + \frac{R1B}{R2B}\right) + V_{BE}$$

$$\text{High limit} \approx V_{ref}\left(1 + \frac{R1A}{R2A}\right)$$

Figure 11. V_{CC} Monitor

D2410, JULY 1978–REVISED AUGUST 1991

- **Equivalent Full-Range Temperature Coefficient . . . 30 ppm/°C**
- **0.2 Ω Typical Output Impedance**
- **Sink Current Capability . . . 1 mA to 100 mA**
- **Low Output Noise**
- **Adjustable Output Voltage . . . V_{ref} to 36 V**
- **Available in a Wide Range of High Density Packaging Options:**
  - **Small Outline (D)**
  - **TO-226AA (LP)**
  - **SOT-89 (PK)**

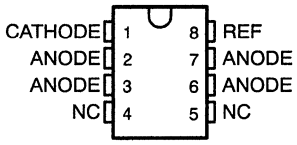
description

The TL431 and TL431A are 3-terminal adjustable shunt regulators with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes in many applications like on-board regulation, adjustable power supplies, and switching power supplies.

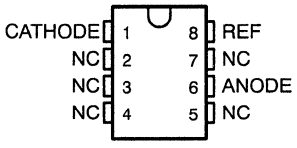
The TL431 is offered in a wide variety of high-density packaging options that includes an SOT-89-type package (suffix PK).

The TL431C and TL431AC are characterized for operation from 0°C to 70°C, and the TL431I and TL431AI are characterized for operation from −40°C to 85°C. The TL431M is characterized for operation over the full military temperature range of −55°C to 125°C.

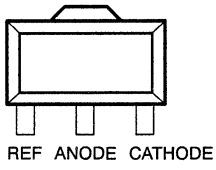
D PACKAGE
(TOP VIEW)



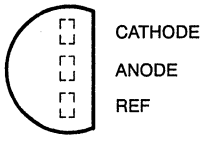
JG AND P PACKAGE
(TOP VIEW)



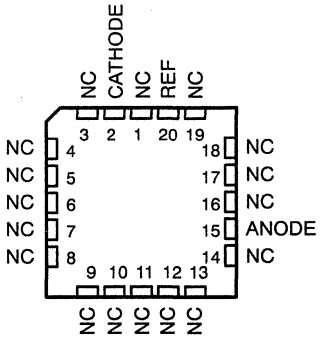
PK PACKAGE
(TOP VIEW)



LP PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

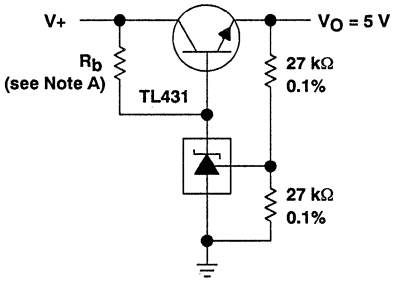
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (D)	CHIP CARRIER (FX)	CERAMIC DIP (JG)	TO-226AA (LP)	PLASTIC DIP (P)	SOT-89 (PK)
0°C to 70°C	TL431CD TL431ACD			TL431CLP TL431ACLP	TL431CP TL431ACP	TL431CPK TL431ACPK
−40°C to 85°C	TL431ID TL431AID			TL431ILP TL431AILP	TL431IP TL431AIP	TL431IPK TL431AIPK
−55°C to 125°C		TL431MFK	TL431MJG			

D and LP packages are available taped and reeled. Add "R" suffix to device type (e.g., TL431CDR). PK package is only available taped and reeled. No "R" suffix required.

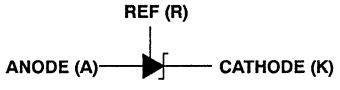
application schematic

Efficient 5-V Precision Regulator

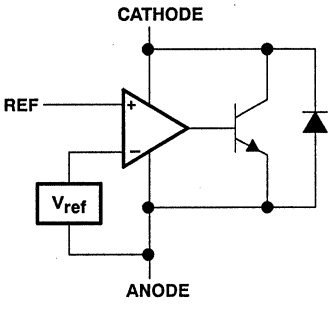


NOTE A: R_b should provide ≥ 1 mA cathode current to the TL431.

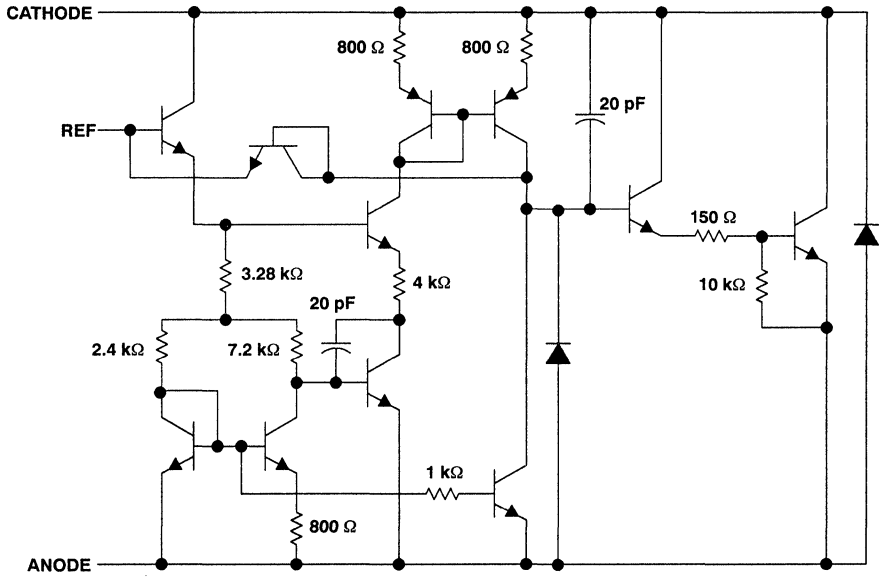
symbol



functional block diagram



equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Cathode voltage (see Note 1) ..... 37 V
Continuous cathode current range ..... −100 mA to 150 mA
Reference input current range ..... −50 μA to 10 mA
Continuous power dissipation ..... See Dissipation Rating Tables 1 and 2
Operating free-air temperature range, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
M-suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG, LP or PK package ..... 300°C

NOTE 1: Voltage values are with respect to the anode terminal unless otherwise noted.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	5.8 mW/°C	725 mW	464 mW	429 mW	
FK	11 mW/°C	1375 mW	880 mW	715 mW	275 mW
JG	8.4 mW/°C	1050 mW	672 mW	546 mW	210 mW
LP	6.2 mW/°C	775 mW	496 mW	403 mW	
P	8.0 mW/°C	1000 mW	640 mW	520 mW	
PK	4.0 mW/°C	500 mW	320 mW	266 mW	

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	DERATING FACTOR ABOVE T_C = 25°C	T_C = 25°C POWER RATING	T_C = 70°C POWER RATING	T_C = 85°C POWER RATING
PK	25 mW/°C	3125 mW	2000 mW	2625 mW

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	36	V
Cathode current, I_K	1	100	mA

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

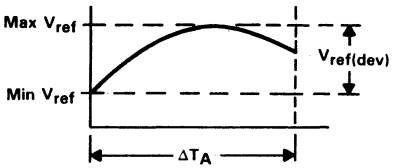
PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431M			TL431I			TL431C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2400	2495	2600	2440	2495	2550	2440	2495	2550	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†			22			5	30		4	17	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−3		−1.4	−2.7		−1.4	−2.7	$\frac{mV}{V}$
				ΔV_{KA} = 36 V − 10 V		−1	−2.3		−1	−2		−1	−2	
I_{ref}	Reference input current	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	8*		2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			1			0.8	2.5		0.4	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	1.5		0.4	1		0.4	1	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	3		0.1	1		0.1	1	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.9*		0.2	0.5		0.2	0.5	Ω

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full temperature range is −55°C to 125°C for the TL431M, −40°C to 85°C for the TL431I and TL431AI, and 0°C to 70°C for the TL431C and TL431AC.

‡ The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, α_{Vref}, is defined as:

$$|\alpha_{Vref}| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

α_{Vref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

Example: Max V_{ref} = 2496 mV at 30°C, Min V_{ref} = 2492 mV at 0°C, V_{ref} = 2495 mV at 25°C, ΔT_A = 70°C for TL431C

$$|\alpha_{Vref}| = \frac{\left(\frac{4\ mV}{2495\ mV}\right) \times 10^6}{70°C} \approx 23\ ppm/°C$$

Because minimum V_{ref} occurs at the lower teperature, the coefficient is positive.

§The dynamic impedance is defined as: $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors, (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

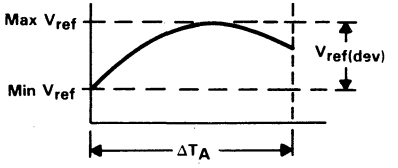
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431AI			TL431AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2470	2495	2520	2470	2495	2520	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†			5	25		4	15	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−2.7		−1.4	−2.7	mV / V
				ΔK_{VA} = 36 V − 10 V		−1	−2		−1	−2	
I_{ref}	Reference input current	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			0.8	2.5		0.8	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	0.7		0.4	0.6	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	0.5		0.1	0.5	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.5		0.2	0.5	Ω

†Full temperature range is 0°C to 70°C for TL431AC and −40°C to 85°C for TL431AI .

‡The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$|\alpha_{Vref}| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

Example: Max V_{ref} = 2496 mV at 30°C, Min V_{ref} = 2492 mV at 0°C, V_{ref} = 2495 mV at 25°C, ΔT_A = 70°C for TL431C

$$|\alpha_{Vref}| = \frac{\left(\frac{4\ mV}{2495\ mV}\right) \times 10^6}{70°C} \approx 23\ ppm/°C$$

Because minimum V_{ref} occurs at the lower teperature, the coefficient is positive.

§The dynamic impedance is defined as: $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors, (see Figure 2), the total dynamic impedance of the circuit is given by:

$$|z'| = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

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PARAMETER MEASUREMENT INFORMATION

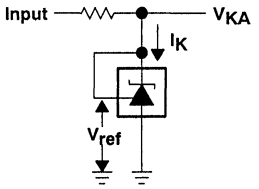

Figure 1. Test Circuit for $V_{KA} = V_{ref}$

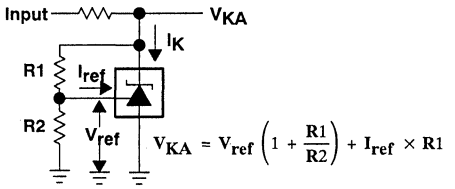

Figure 2. Test Circuit for $V_{KA} > V_{ref}$

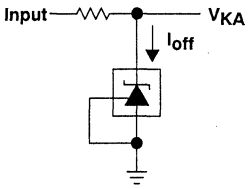

Figure 3. Test Circuit for I_{off}

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{ref}	Reference voltage	vs Temperature	4
I_{ref}	Reference current	vs Temperature	5
I_K	Cathode current	vs Cathode voltage	6 and 7
I_{off}	Off-State cathode current	vs Temperature	8
ΔV_{ref}	Change in reference voltage to change in cathode voltage	vs Temperature	9
V_n	Noise voltage	vs Frequency over a 10-second time-period	10 and 11
A_V	Voltage amplification	vs Frequency	12
$\|\|z_{ka}\|\|$	Reference impedance	vs Frequency	13
	Pulse response		14
	Stability boundary conditions		15

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TYPICAL CHARACTERISTICS†

REFERENCE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE †

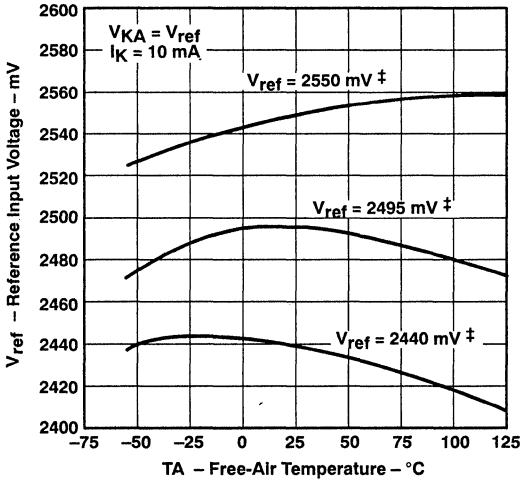


Figure 4

REFERENCE INPUT CURRENT
vs
FREE-AIR TEMPERATURE †

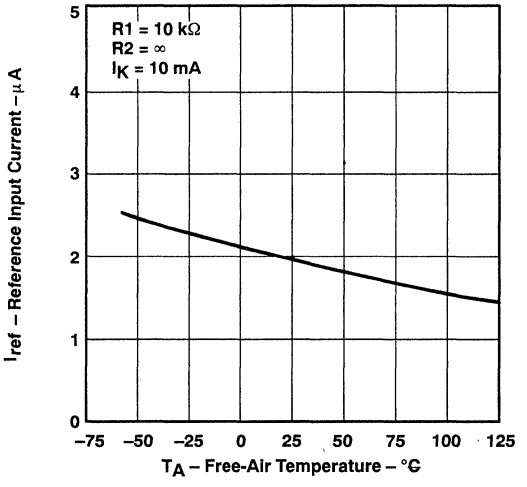


Figure 5

CATHODE CURRENT
vs
CATHODE VOLTAGE

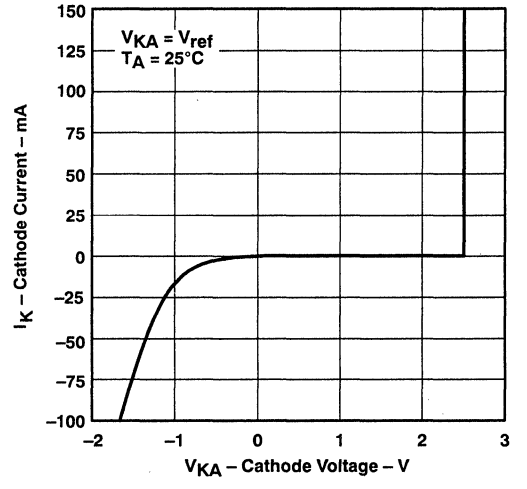


Figure 6

CATHODE CURRENT
vs
CATHODE VOLTAGE

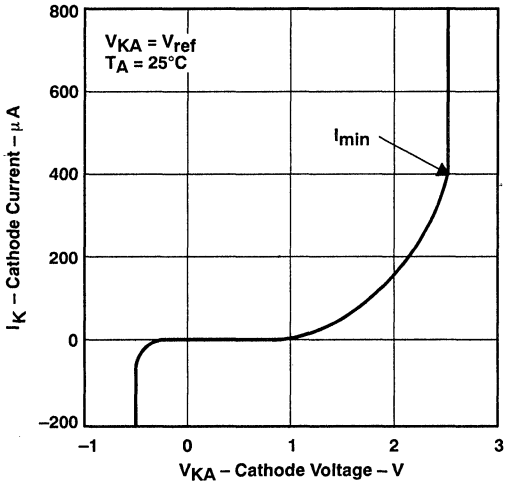


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ Data is for devices having the indicated value of V_{ref} at I_K = 10 mA, T_A = 25°C.

TYPICAL CHARACTERISTICS†

OFF-STATE CATHODE CURRENT
vs
FREE-AIR TEMPERATURE †

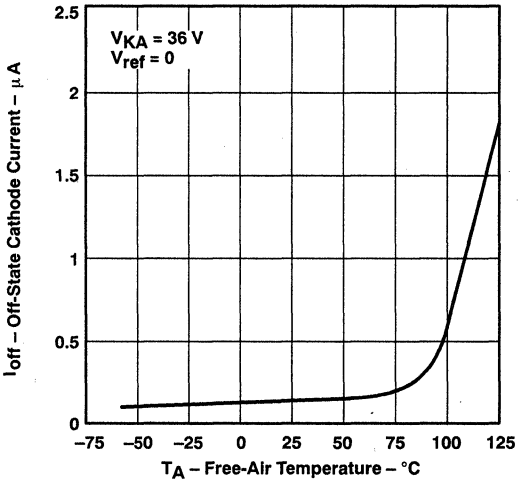


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE TO
DELTA CATHODE VOLTAGE
vs
FREE-AIR TEMPERATURE

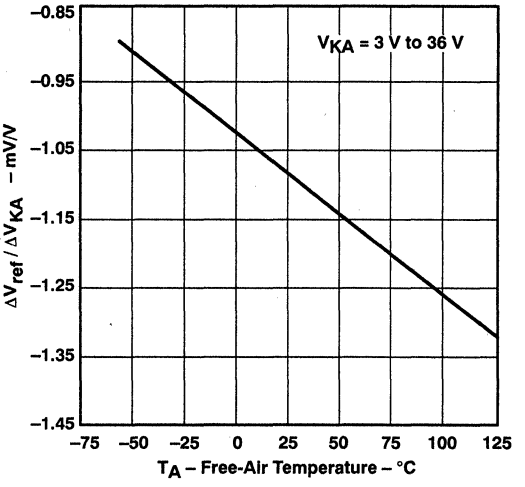


Figure 9

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

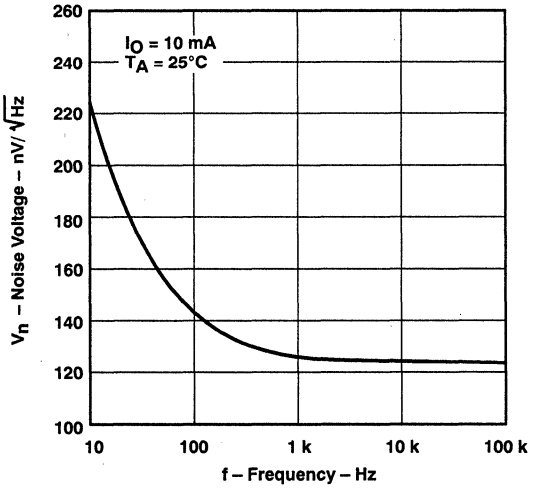
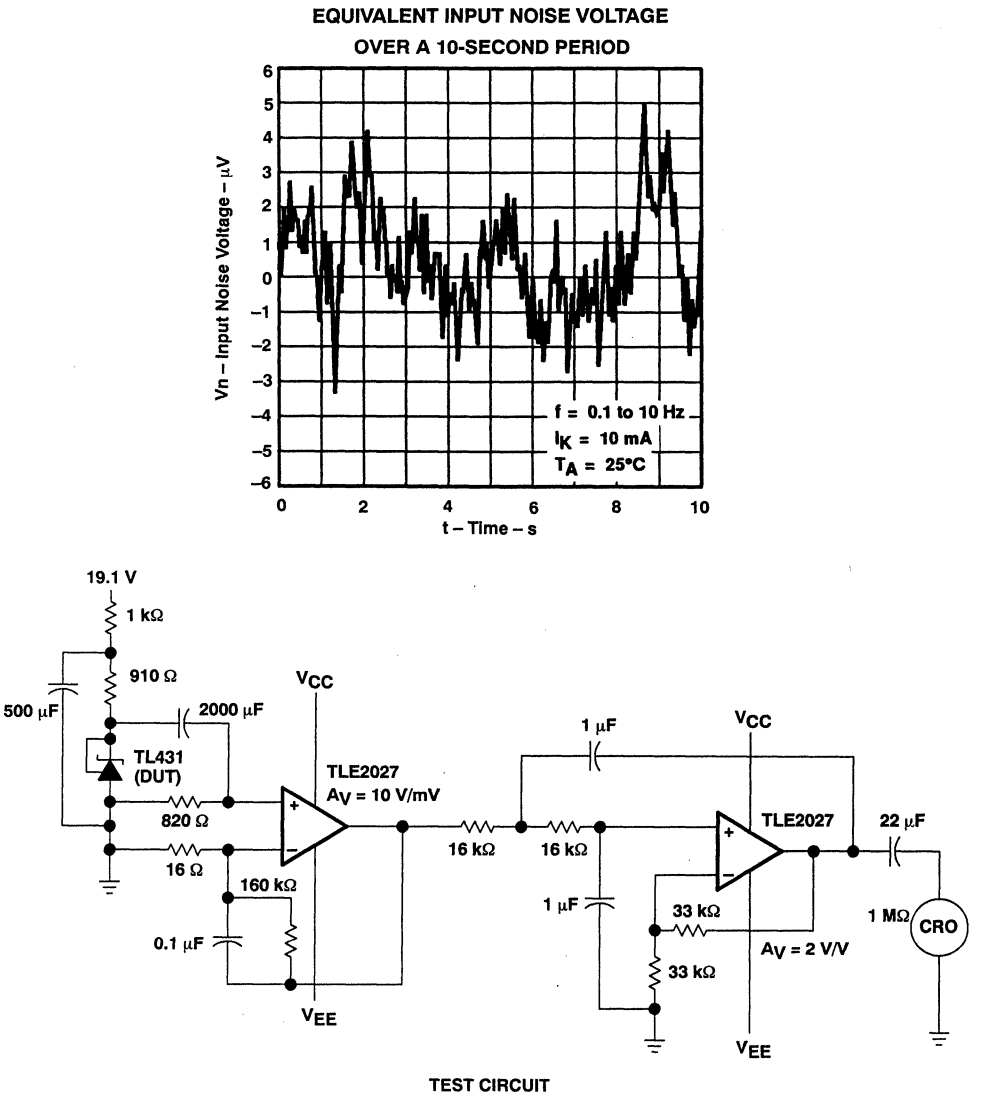


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

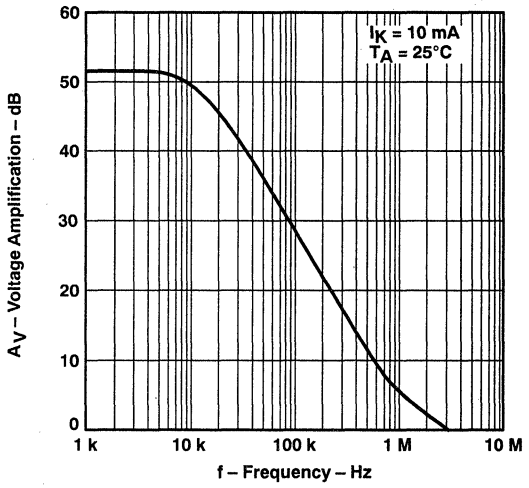


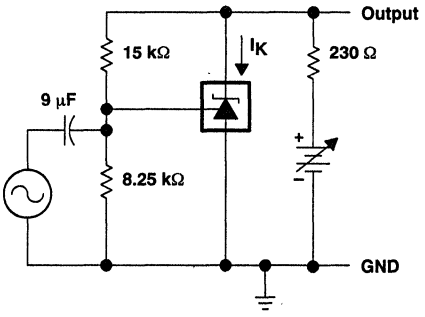
TEST CIRCUIT

Figure 11

TYPICAL CHARACTERISTICS

SMALL-SIGNAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

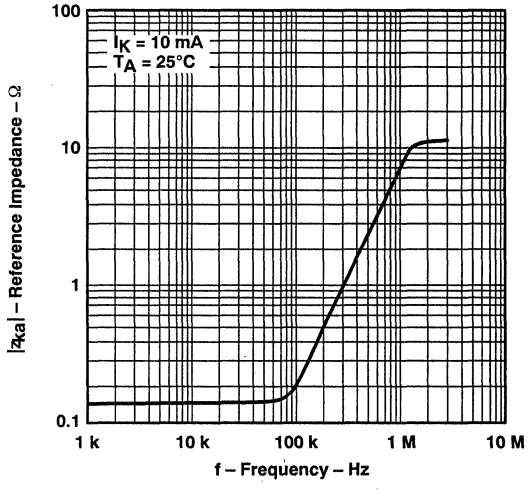


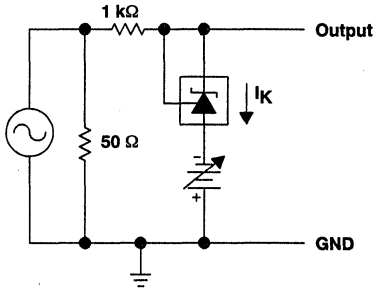


TEST CIRCUIT FOR VOLTAGE AMPLIFICATION

Figure 12

REFERENCE IMPEDANCE
vs
FREQUENCY





TEST CIRCUIT FOR REFERENCE IMPEDANCE

Figure 13

TYPICAL CHARACTERISTICS

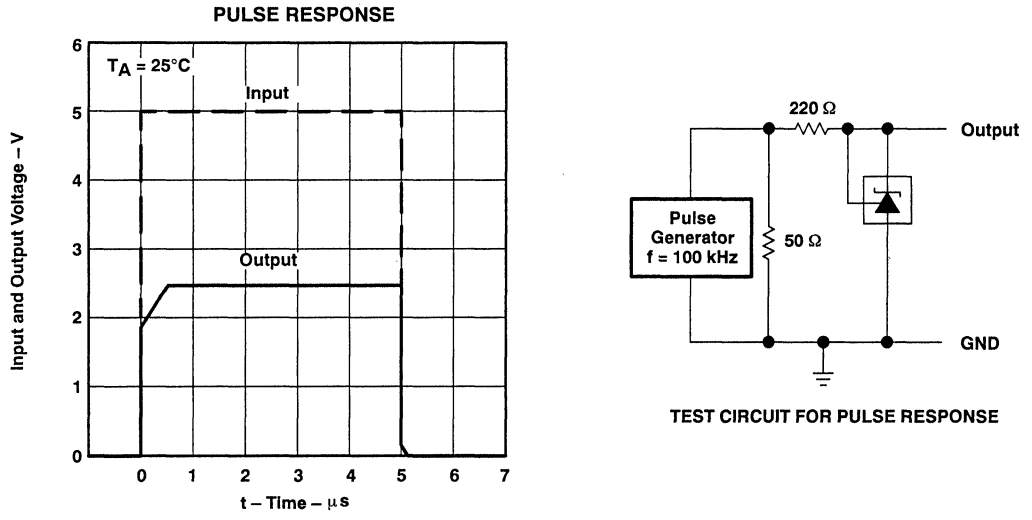


Figure 14

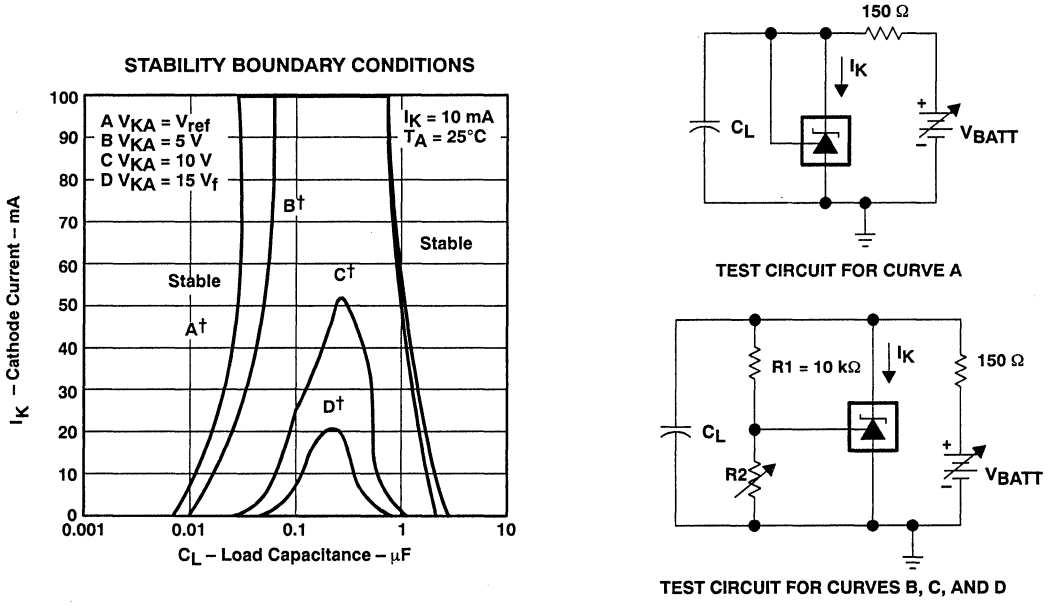
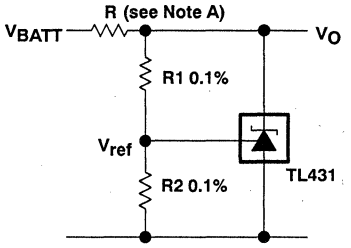


Figure 15

† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{BATT} and C_L were then adjusted to determine the ranges of stability.

APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

NOTE A: R should provide ≥ 1 mA cathode current to the TL431 at minimum V_{BATT}.

Figure 16. Shunt Regulator

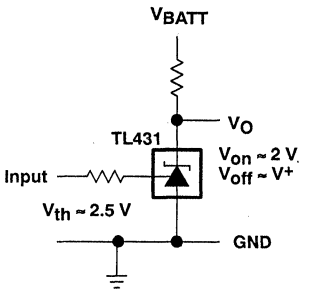
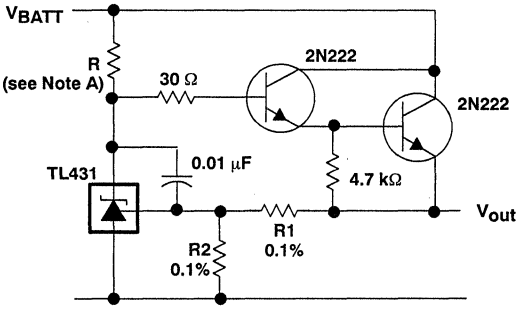


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

NOTE A: R should provide ≥ 1 mA cathode current to the TL431 at minimum V_{BATT}.

Figure 18. Precision High-Current Series Regulator

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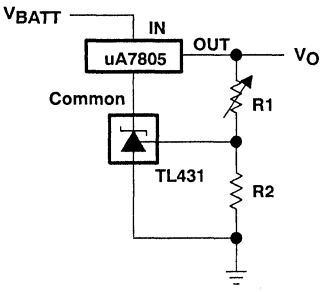
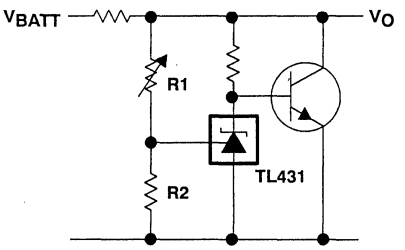
APPLICATION INFORMATION



$$V = \left(1 + \frac{R1}{R2}\right) + V_{ref}$$

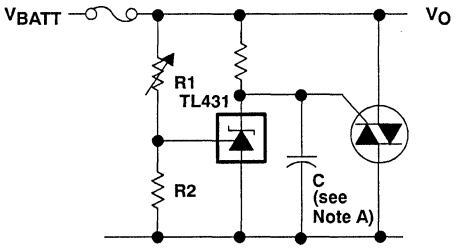
$$\text{Min } V = V_{ref} + 5\ V$$

Figure 19. Output Control of a 3-Terminal Fixed Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 20. High Current Shunt Regulator



NOTE A: Refer to the stability boundary conditions in Figure 15 to determine allowable values for C.

Figure 21. Crowbar Circuit

APPLICATION INFORMATION

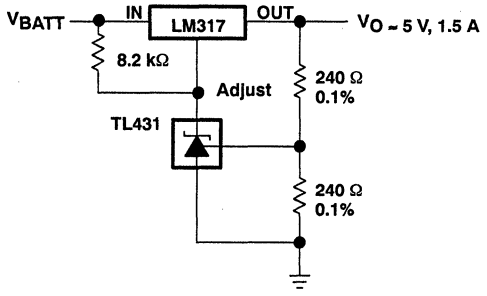
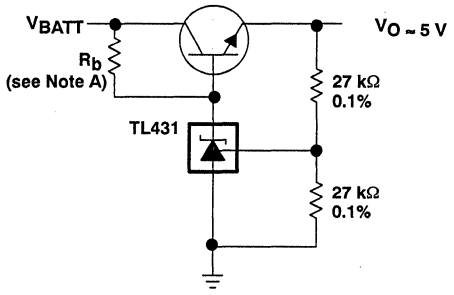


Figure 22. Precision 5-V, 1.5-A Regulator



NOTE A: R_b should provide ≥ 1-mA cathode current to the TL431.

Figure 23. Efficient 5-V Precision Regulator

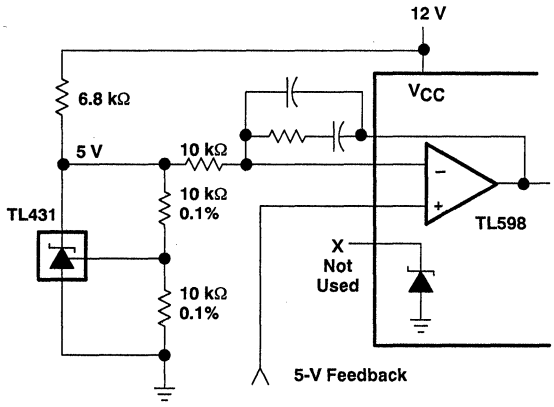
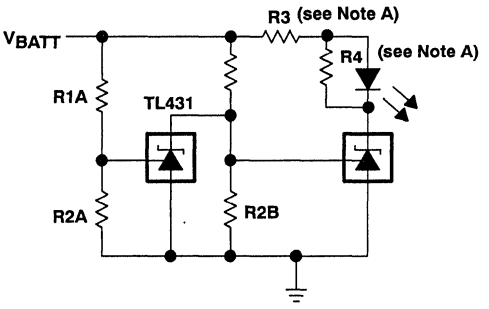


Figure 24. PWM Downconverter With Reference

APPLICATION INFORMATION



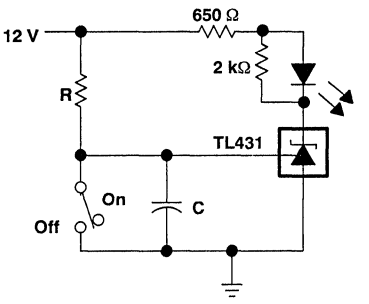
$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{ref}$$

$$\text{High Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{ref}$$

LED On When
Low Limit < V_{BATT} < High Limit

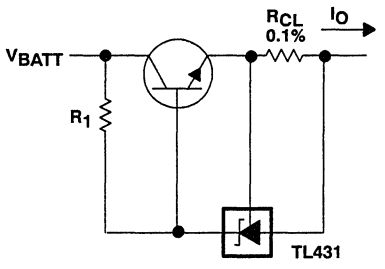
NOTE A: R3 and R4 are selected to provide the desired LED intensity and ≥ 1 mA cathode current to the TL431 at the available V+.

Figure 25. Voltage Monitor



$$\text{Delay} = R \times C \times \ln\left(\frac{12\ V}{12\ V - V_{ref}}\right)$$

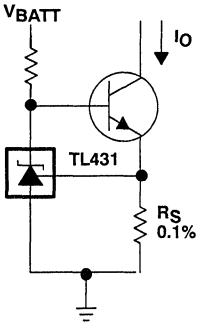
Figure 26. Delay Timer



$$I_{out} = \frac{V_{ref}}{R_{CL}} + I_K$$

$$R_1 = \frac{V+}{\frac{I_O}{h_{FE}} + I_K}$$

Figure 27. Precision Current Limiter



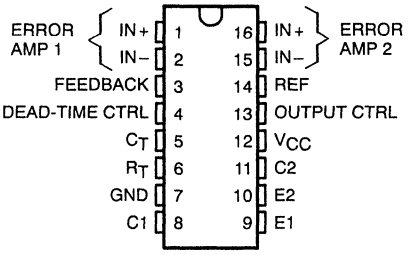
$$I_O = \frac{V_{ref}}{R_S}$$

Figure 28. Precision Constant-Current Sink

D2535, JANUARY 1983–REVISED SEPTEMBER 1991

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

TL494C, TL494I . . . D OR N PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE	
	SURFACE MOUNT (D)	PLASTIC DIP (N)
0°C to 70°C	TL494CD	TL494CN
−40°C to 85°C	TL494ID	TL494IN

The D package is available taped and reeled. Add "R" suffix to device type (e.g., TL494CDR).

FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
$V_I \le 0$	Single-ended or parallel output
$V_I \le$ REF	Normal push-pull operation

description

The TL494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, this device offers the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

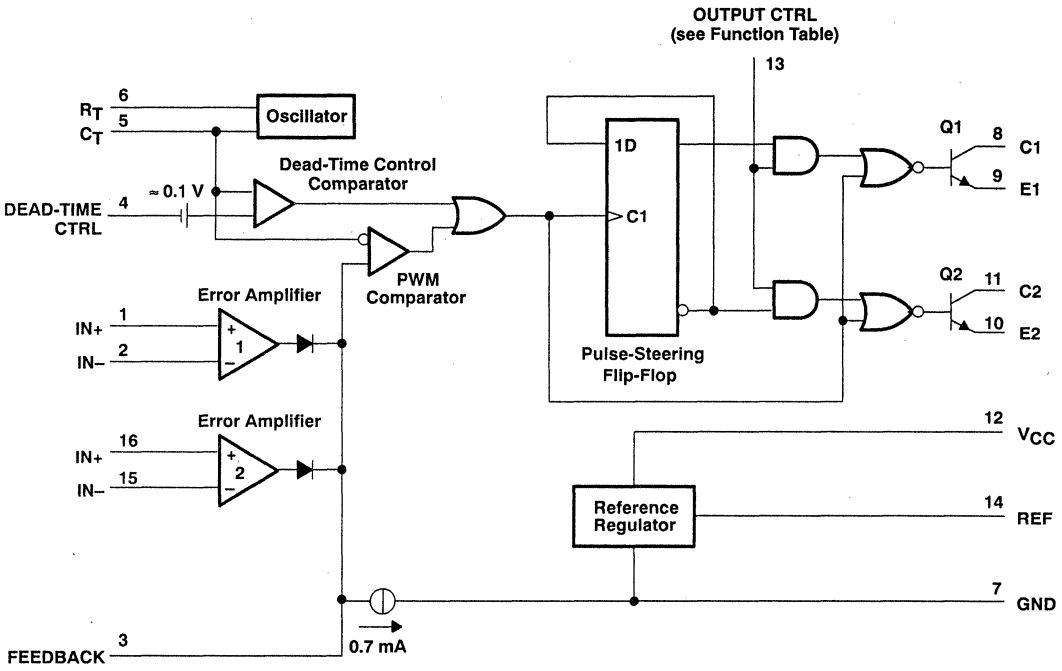
The TL494 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control comparator, a pulse-steering control flip-flop, a 5-V, 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T to the reference output and providing a sawtooth input to C_T, or it may be used to drive the common circuits in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. The TL494 provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of this device prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494C is characterized for operation from 0°C to 70°C. The TL494I is characterized for operation from −40°C to 85°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL494C	TL494I	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	V
Amplifier input voltage	V_{CC} + 0.3	V_{CC} + 0.3	V
Collector output voltage	41	41	V
Collector output current	250	250	mA
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range	0 to 70	−40 to 85	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260	260	°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	900 mW	7.6 mW/°C	25°C	608 mW	494 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

	TL494C		TL494I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltage, V_I	−0.3	V_{CC}−2	−0.3	V_{CC}−2	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Oscillator frequency	1	300	1	300	kHz
Timing capacitor, C_T	0.47	10000	0.47	10000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Operating free-air temperature, T_A	0	70	−40	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			UNIT
		MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 mA to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX		0.2%	1%	
Short-circuit output current§	REF = 0		35		mA

oscillator section C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	TL494C, TL494I			UNIT
		MIN	TYP‡	MAX	
Frequency	C_T = 0.01 μF, R_T = 12 kΩ		10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, and T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%		
Frequency change with temperature#	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = MIN to MAX			1%	

error amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	V_O (pin 3) = 2.5 V		2	10	mV
Input offset current	V_O (pin 3) = 2.5 V		25	250	nA
Input bias current	V_O (pin 3) = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	−0.3 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	V_{ID} = −15 mV to −5 V, V (pin 3) = 0.7 V	0.3	0.7		nA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V, V (pin 3) = 3.5 V	−2			nA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N-1}}$
# Temperature coefficient of timing capacitor and timing resistor not taken into account.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS		TL494C, TL494I			UNIT
				MIN	TYP†	MAX	
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V,	I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}				3.5	mA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	V_I (pin 4) = 0, C_T = 0.1 μF, R_T = 12 kΩ		45%		
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	V (pin 3) = 0.7 V	0.3	0.7		mA

total device

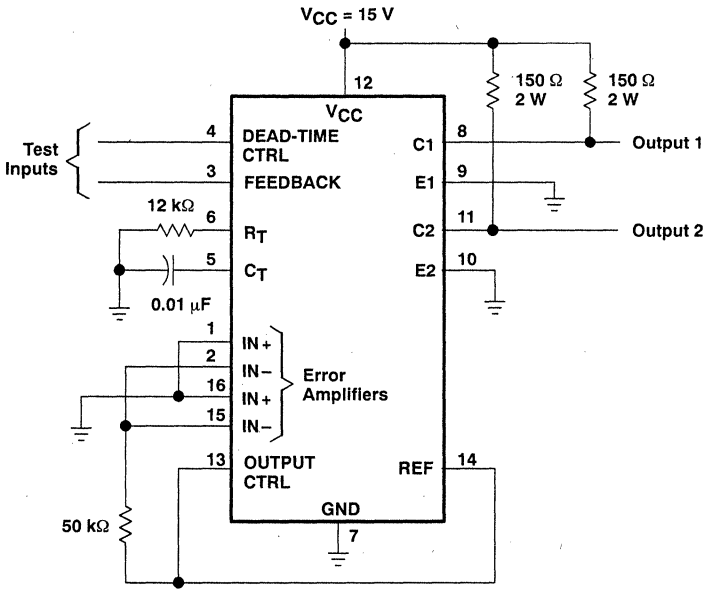
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at REF,	V_{CC} = 15 V		6	10	mA
	All other inputs and outputs open	V_{CC} = 40 V		9	15	
Average supply current	V_I (pin 4) = 2 V,	See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

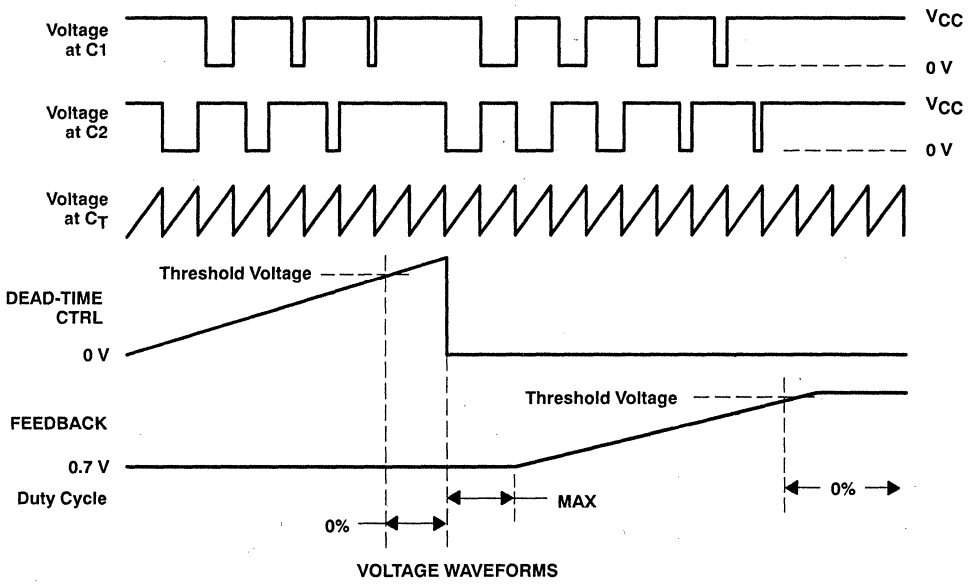
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time			40	100	ns

† All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

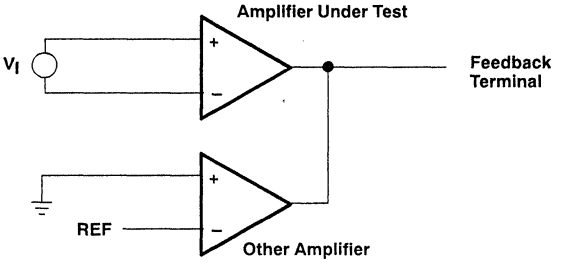


Figure 2. Amplifier Characteristics

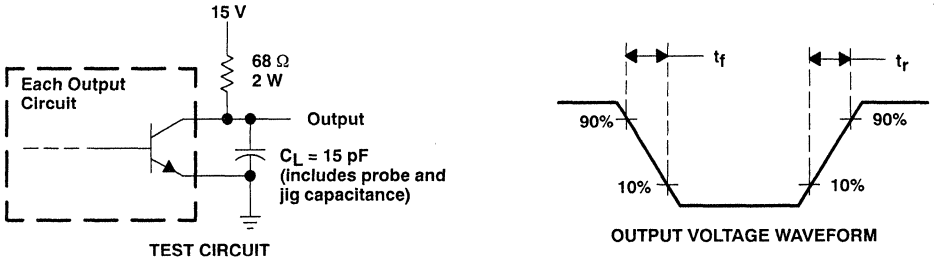


Figure 3. Common-Emitter Configuration

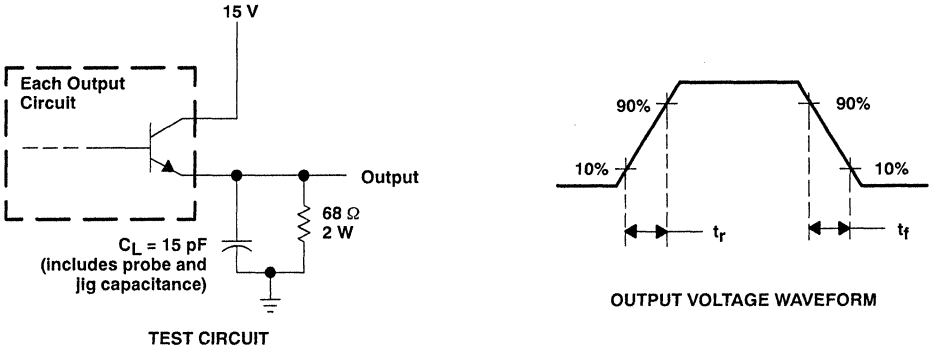


Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

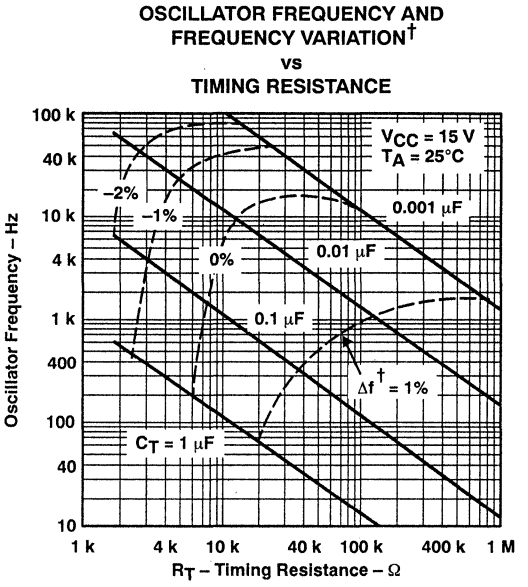


Figure 5

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

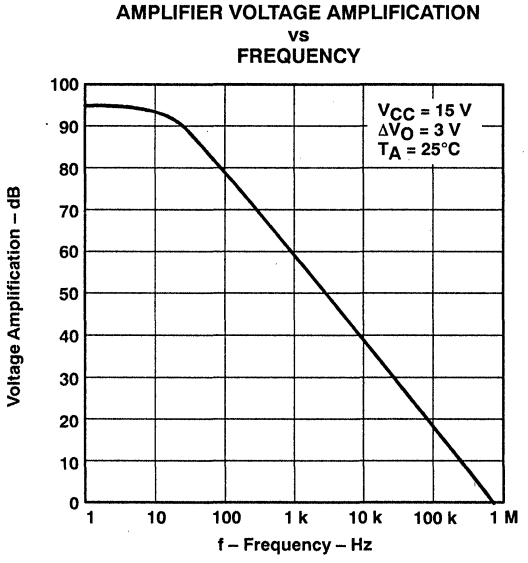
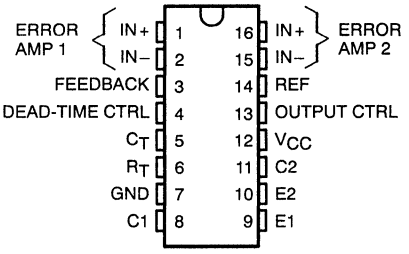


Figure 6

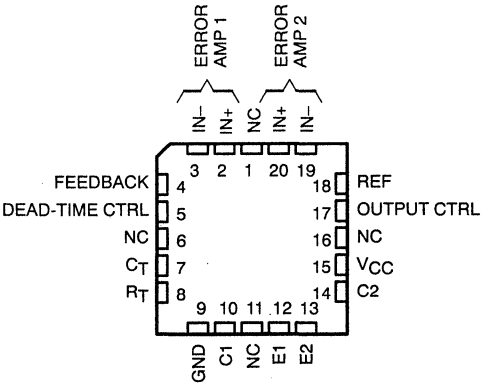
D3883, SEPTEMBER 1991

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance**
- **Circuit Architecture Allows Easy Synchronization**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL494M incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

The TL494M contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control comparator, a pulse-steering control flip-flop, a 5-V 5%-precision regulator, and output-control circuits.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T to the reference output and providing a sawtooth input to C_T, or it may be used to drive the common circuits in synchronous multiple-rail power supplies.

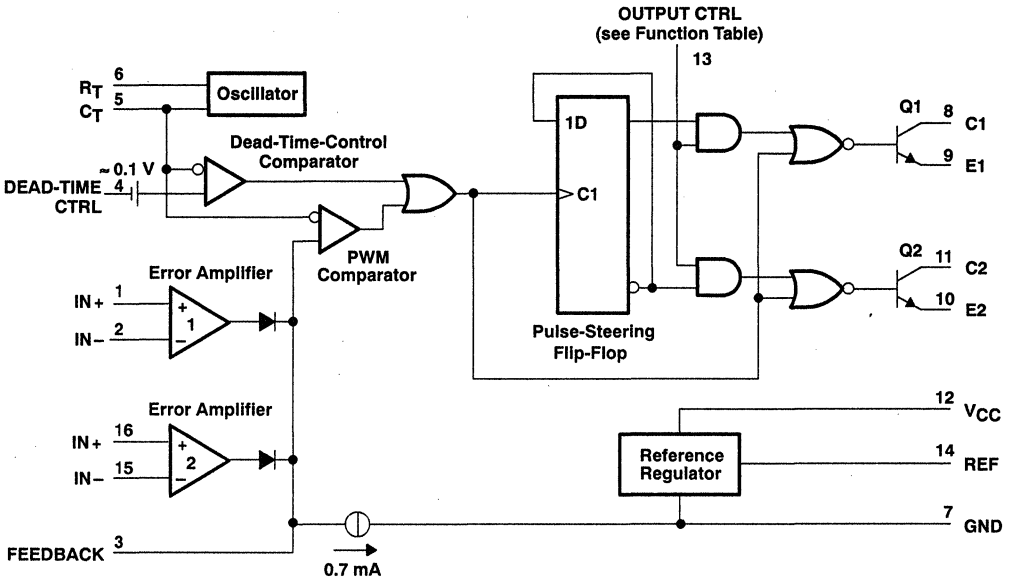
FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = 0	Single-ended or parallel output
V_I = REF	Normal push-pull operation

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation, which may be selected through the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation.

The TL494M is characterized for operation from −55°C to 125°C.

functional block diagram



Pin numbers shown are for J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage ..... V_{CC} + 0.3 V
Collector output voltage ..... 41 V
Collector output current ..... 250 mA
Continuous total dissipation (see Note 2) ..... 1375 mW
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 275 mW at the rate of 11 mW/°C.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Amplifier input voltage, V_I	−0.3	V_{CC}−2	V
Collector output voltage, V_O		40	V
Collector output current (each transistor)		200	mA
Current into feedback terminal		0.3	mA
Timing capacitor, C_T	0.47	10000	nF
Timing resistor, R_T	1.8	500	kΩ
Oscillator frequency, f_{osc}	1	300	kHz
Operating free-air temperature, T_A	−55	125	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (REF)	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V		2	25	mV
Output regulation	I_O = 1 to 10 mA		1	15	mV
Output voltage change with temperature	ΔT_A = MIN to MAX‡		0.2%	3%*	
Short-circuit output current§	REF = 0		35		mA

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	C_T = 0.01 μF, R_T = 12 kΩ		10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, and T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%		
Frequency change with temperature#	C_T = 0.01 μF, R_T = 12 kΩ, ΔT_A = MIN to MAX‡			1%*	

error amplifier section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pin 3) = 2.5 V		2	10	mV
Input offset current	V_O (pin 3) = 2.5 V		25	250	nA
Input bias current	V_O (pin 3) = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0.3 to V_{CC}–2			V
Open-loop voltage amplification	ΔV_O = 3 V, R_L = 2 kΩ, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V, R_L = 2 kΩ		800		kHz
Common-mode rejection ratio	ΔV_O = 40 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	V_{ID} = –15 mV to –5 V, V (pin 3) = 0.7 V	0.3	0.7		mA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V, V (pin 3) = 3.5 V	–2			mA

* This parameter is not production tested.
† All typical values except for parameter changes with temperature are at T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Duration of the short circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$
# Temperature coefficient of timing capacitor and timing resistor not taken into account.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

output section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Collector off-state current		V_{CE} = 40 V,	V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V,	V_E = 0			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0,	I_C = 200 mA		1.1	1.3	V
	Emitter-follower	V_C = 15 V,	I_E = −200 mA		1.5	2.5	
Output control input current		V_I = REF				3.5	mA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V			−2	−10	μA
Maximum duty cycle, each output	V_I (pin 4) = 0,	C_T = 0.1 μF, R_T = 12 kΩ		45%	50%*	
Input threshold voltage (pin 4)	Zero duty cycle			3	3.3	V
	Maximum duty cycle		0*			

pwm comparator section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	V (pin 3) = 0.7 V	0.3	0.7		mA

total device (see Figure 1)

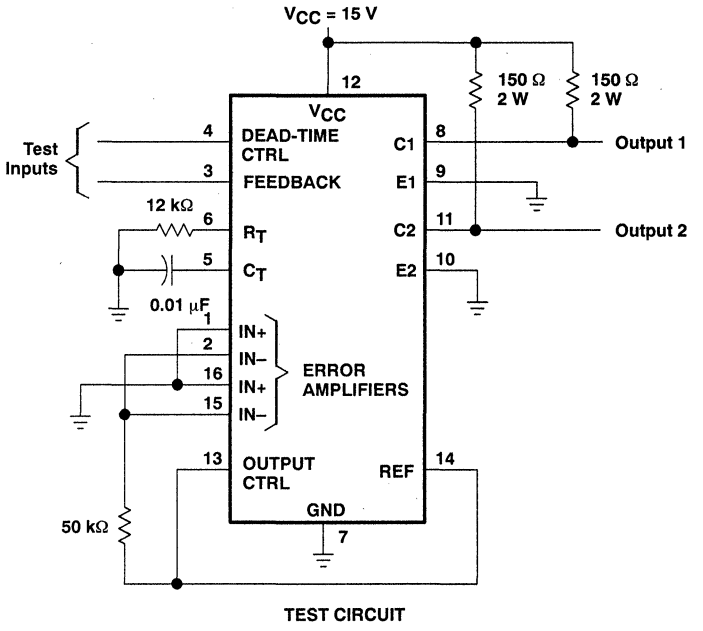
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at REF,	V_{CC} = 15 V		6	21	mA
	All other inputs and outputs open	V_{CC} = 40 V		9	26	
Average supply current	V_I (pin 4) = 2 V,	See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

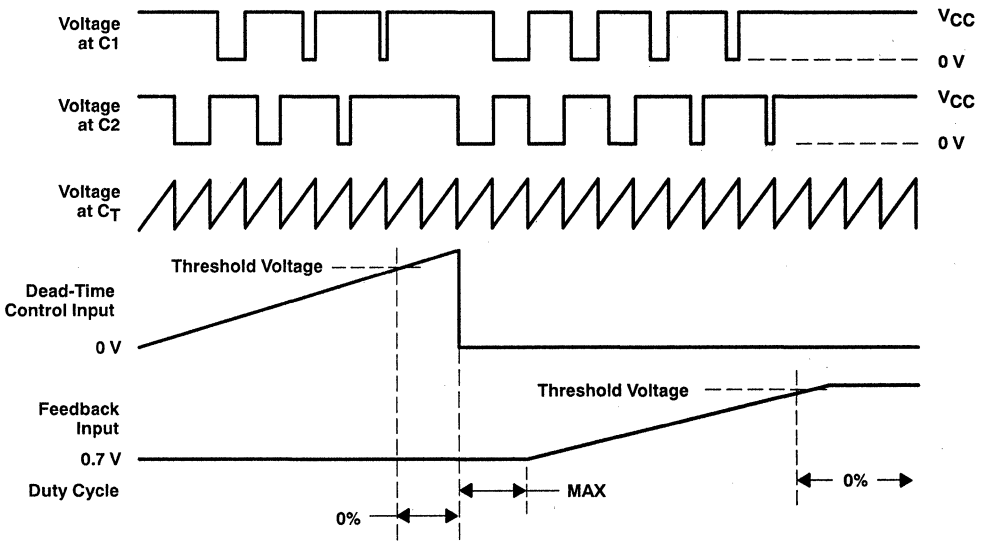
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200*	ns
Output voltage fall time			25	100*	
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200*	ns
Output voltage fall time			40	100*	

* This parameter is not production tested.
† All typical values except for temperature coefficient are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

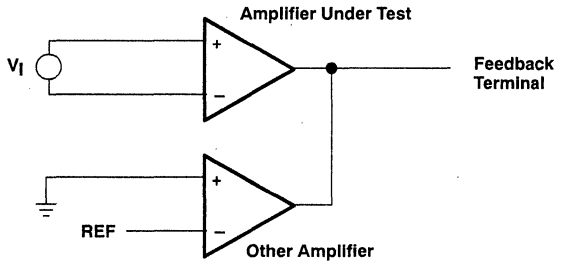


Figure 2. Amplifier Characteristics

Figure 3. Common-Emitter Configuration

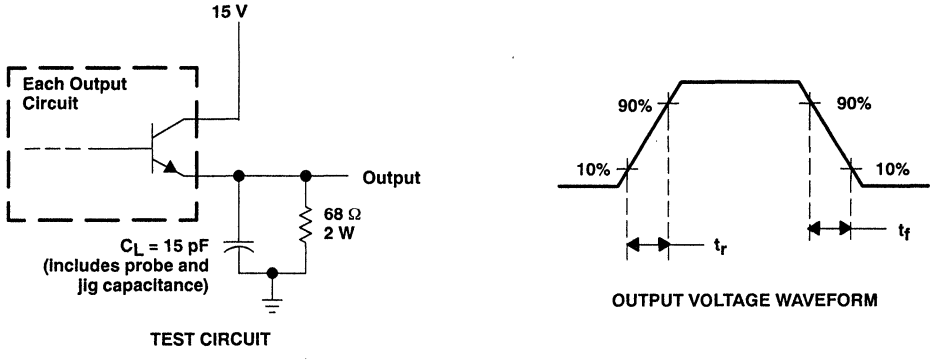


Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE

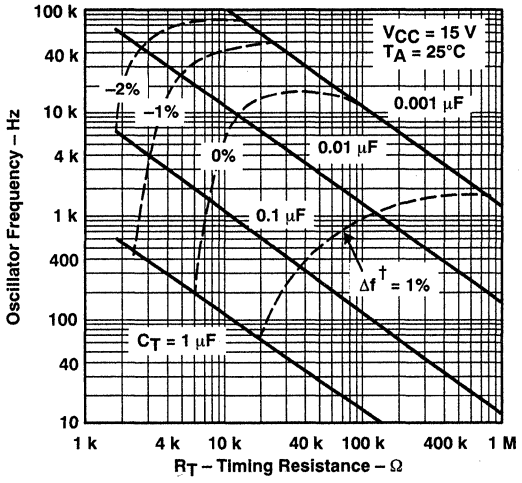


Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

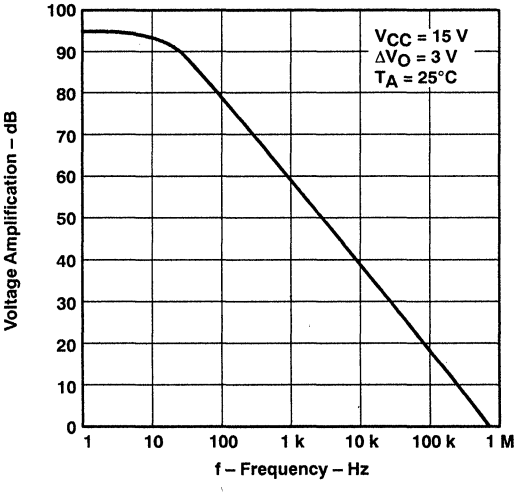


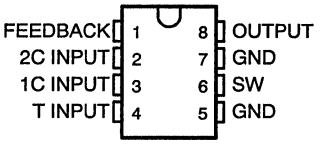
Figure 6

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D2486, AUGUST 1978–REVISED NOVEMBER 1991

- **Internal Step-Up Switching Regulator**
- **Fixed 9-V Output**
- **Charges Battery Source During Transformer-Coupled-Input Operation**
- **Minimum External Components Required (1 Inductor, 1 Capacitor, 1 Diode)**
- **1- or 2-Cell-Input Operation**

D OR P PACKAGE
(TOP VIEW)



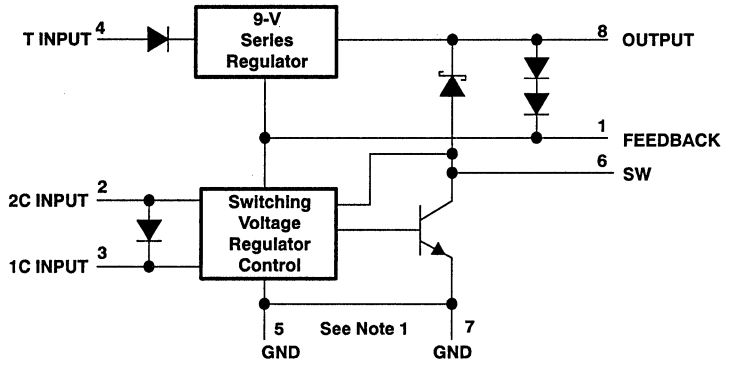
Pins 5 and 7 are connected together internally.

description

The TL496C power-supply control circuit is designed to provide a 9-V regulated supply from a variety of input sources. Operable from a 1- or 2-cell battery input, the TL496C performs as a switching regulator with the addition of a single inductor and filter capacitor. When ac coupled with a step-down transformer, the TL496C operates as a series regulator to maintain the regulated output voltage and, with the addition of a single catch diode, time shares to recharge the input batteries.

The design of the TL496C allows minimal supply current drain during standby operation (125 μA typical). With most battery sources, this allows a constant bias to be maintained on the power supply. This makes power instantly available to the system, thus eliminating power-up sequencing problems.

functional block diagram



NOTE 1: Pins 5 and 7, though connected together internally, must both be terminated to ground to ensure proper circuit operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage: 2C INPUT	3.5 V
1C INPUT	2.5 V
T INPUT	20 V
Output voltage, SW	12 V
Diode reverse voltage, OUTPUT	12 V
Switch current, SW	1.2 A
Diode current, OUTPUT	1.2 A
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, one-cell operation (2C and 1C INPUTS to ground)	1.1	1.5	V
Input voltage, two-cell operation (2C INPUT to ground)	2.3	3	V
Input voltage, one-cell or two-cell operation (T INPUT to ground)	V_O +2	20	V

electrical characteristics at T_A = 25°C

series regulator section (T INPUT)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage	V_I = 5 V, I_O = −50 mA			1.5	2	V
Regulated output voltage	V_I = 20 V	I_O = −50 μA	9.5	10.1	11.2	V
		I_O = −80 mA	9	10	11	
	V_I = 20 V, FEEDBACK shorted to OUTPUT	I_O = −50 μA	8.5	9	9.7	
		I_O = −80 mA	6.7	8.6	9.5	
Standby current, T INPUT	V_I = 20 V, OUTPUT at 12 V				400	μA
Reverse current through T INPUT	V_I = −1.5 V, 1 mA into OUTPUT				−25	μA

output switch

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CE(sat)}$ Collector-emitter saturation voltage	800 mA into SW, 2C INPUT at 2.25 V		0.35	0.6	V

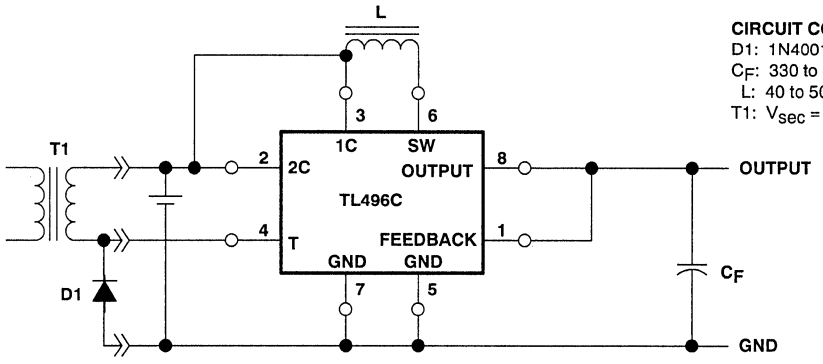
diode (SW to OUTPUT)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F Forward voltage	I_F = 1.5 A		1.6	2.5	V
I_R Reverse current through SW	SW at 0 V, 1 mA into OUTPUT			−20	μA

control section

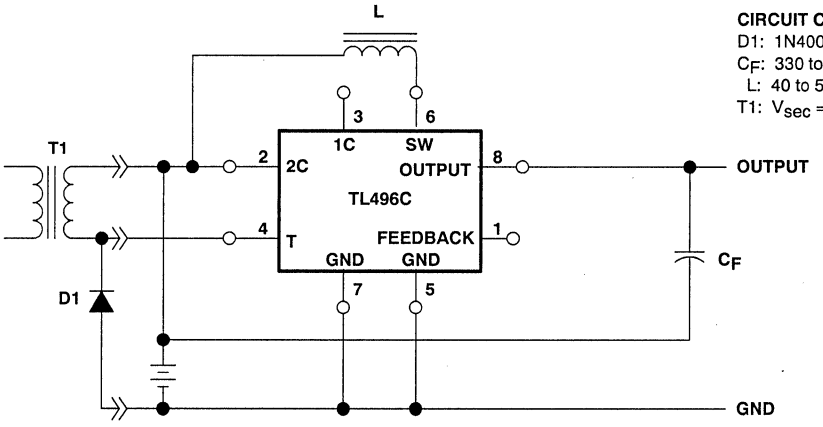
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
On-state current (2C INPUT)	FEEDBACK and OUTPUT at 0 V, 2C INPUT at 3 V		60	100	mA
Standby current (FEEDBACK)	FEEDBACK at 8.65 V, 2C INPUT and SW at 3 V			40	μA
Standby current (2C INPUT and SW)	FEEDBACK at 8.65 V, 2C INPUT and SW at 3 V			400	μA
Start-up current (current into SW to initiate cycle)	FEEDBACK, 2C INPUT, SW, and OUTPUT at 2.25 V	16			mA

APPLICATION INFORMATION



CIRCUIT COMPONENT INFORMATION
D1: 1N4001
C_F: 330 to 470 μF, 10 V, electrolytic
L: 40 to 50 μH, Q ≈ 3, R < 0, 15 Ω
T1: V_{sec} = 6.8 V RMS typ, R_{sec} = 11 Ω typ

Figure 1. One-Cell Operation



CIRCUIT COMPONENT INFORMATION
D1: 1N4001
C_F: 330 to 470 μF, 10 V, electrolytic
L: 40 to 50 μH, Q ≈ 3, R < 0, 15 Ω
T1: V_{sec} = 6.8 V RMS typ, R_{sec} = 11 Ω typ

Figure 2. Two-Cell Operation

electrical characteristics for one- and two-cell input operations

PARAMETER		ONE-CELL OPERATION (see Figure 1)	TWO-CELL OPERATION (see Figure 2)
Input current	No load	125 μA	125 μA
	R_L = 120 Ω	525 mA	405 mA
Output voltage	Without T1	7.2 V	8.6 V
	With T1	8.6 V	10 V
Output current capability		40 mA	80 mA
Efficiency		66%	66%
Battery life (AA NiCad) no load		60 days	166 days

functional description

The TL496C is designed to operate from either a single-cell or two-cell source. To operate the device from a single cell (1.1 V to 1.5 V), the source must be connected to both inputs 1C and 2C as shown in Figure 1. For a two-cell operation (2.3 V to 3 V), the input is applied to the 2C input only and the 1C input is left open (see Figure 2).

battery operation

The TL496C operates as a switching regulator from a battery input. The cycle is initiated when a low-voltage condition is sensed by the internal feedback (the thresholds at pin 1 and pin 8 are approximately 7.2 and 8.6 V, respectively). An internal latch is set and the output transistor is turned on. This causes the current in the external inductor (L) to increase linearly until it reaches a peak value of approximately 1 A. When the peak current is sensed, the internal latch is reset and the output transistor is turned off. The energy developed in the inductor is then delivered to the output storage capacitor through the blocking diode. The latch remains in the off state until the feedback signal indicates the output voltage is again deficient.

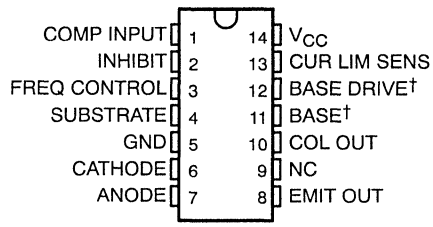
transformer-coupled operation

The TL496C operates on alternate half cycles of the ac input during transformer-coupled operation to first sustain the output voltage and second, recharge the batteries. The TL496C performs like a series regulator to supply charge to the output filter/storage capacitor during the first half cycle. The output voltage of the series regulator is slightly higher voltage than that created by the switching circuit; this maintains the feedback voltage above the switching regulator control circuit threshold, effectively inhibiting the switching control circuitry. During the second half cycle, an external diode (1N4001) is used to clamp the negative-going end of the transformer secondary to ground, thus allowing the positive-going end (end connected to V+ side of battery) to pump a charge into the standby batteries.

D2225, JUNE 1976 – REVISED AUGUST 1991

- **High Efficiency . . . 60% or Greater**
- **Output Current . . . 500 mA**
- **Input Current Limit Protection**
- **TTL-Compatible Inhibit**
- **Adjustable Output Voltage**
- **Input Regulation . . . 0.2% Typ**
- **Output Regulation . . . 0.4% Typ**
- **Soft Start-Up Capability**

TL497AC, TL497AI . . . D OR N PACKAGE
(TOP VIEW)



NC - No internal connection

† The BASE pin (#11) and BASE DRIVE pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

description

The TL497AC and TL497AI incorporate on a single monolithic chip all the active functions required in the construction of switching voltage regulators. They can also be used as the control element to drive external components for high-power-output applications. The TL497AC and TL497AI were designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

The TL497AC and TL497AI are fixed-on-time variable-frequency switching voltage regulator control circuits. The on time is programmed by a single external capacitor connected between the FREQ CONTROL pin and GND. This capacitor, C_T, is charged by an internal constant-current generator to a predetermined threshold. The charging current and the threshold vary proportionally with V_{CC}. Thus, the on time remains constant over the specified range of input voltage (4.5 V to 12 V). Typical on times for various values of C_T are as follows:

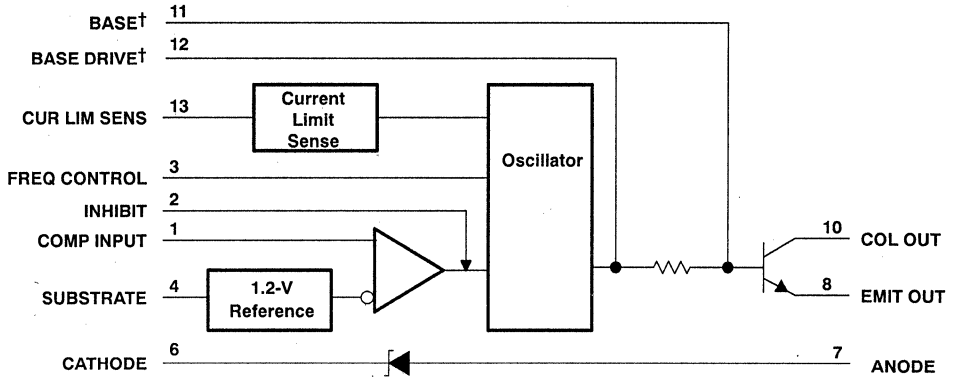
TIMING CAPACITOR, C_T (pF)	200	250	350	400	500	750	1000	1500	2000
ON TIME (μs)	19	22	26	32	44	56	80	120	180

The output voltage is controlled by an external resistor ladder network (R1 and R2 in Figures 1, 2, and 3) that provides a feedback voltage to the comparator input. This feedback voltage is compared to the reference voltage of 1.2 V (relative to the SUBSTRATE pin) by the high-gain comparator. When the output voltage decays below the value required to maintain 1.2 V at the comparator input, the comparator enables the oscillator circuit, which charges and discharges C_T as described above. The internal pass transistor is driven on during the charging of C_T. The internal transistor may be used directly for switching currents up to 500 mA. Its collector and emitter are uncommitted, and it is current driven to allow operation from the positive supply voltage or ground. An internal Schottky diode matched to the current characteristics of the internal transistor is also available for blocking or commutating purposes. The TL497AC and TL497AI also have on-chip current-limit circuitry that senses the peak currents in the switching regulator and protects the inductor against saturation and the pass transistor against overstress. The current limit is adjustable and is programmed by a single sense resistor, R_{CL}, connected between V_{CC} and CUR LIM SENS. The current-limit circuitry is activated when 0.7 V is developed across R_{CL}. External gating is provided by the INHIBIT input. When the INHIBIT input is high, the output is turned off.

Simplicity of design is a primary feature of the TL497AC and TL497AI. With only six external components (three resistors, two capacitors, and one inductor), the TL497AC and TL497AI will operate in numerous voltage conversion applications (step-up, step-down, invert) with as much as 85% of the source power delivered to the load. The TL497AC and TL497AI replace the TL497 in all applications.

The TL497AC is characterized for operation from 0°C to 70°C, and the TL497AI is characterized for operation from −40°C to 85°C.

functional block diagram



† The BASE pin (#11) and BASE DRIVE pin (#12) are used for device testing only. They are not normally used in circuit applications of the device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 15 V
Output voltage, V_O ..... 35 V
Comparator input voltage ..... 5 V
Inhibit input voltage ..... 5 V
Diode reverse voltage ..... 35 V
Power switch current ..... 750 mA
Diode forward current ..... 750 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL497AC ..... 0°C to 70°C
TL497AI ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 260°C

NOTE 1: All voltage values except diode voltages are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

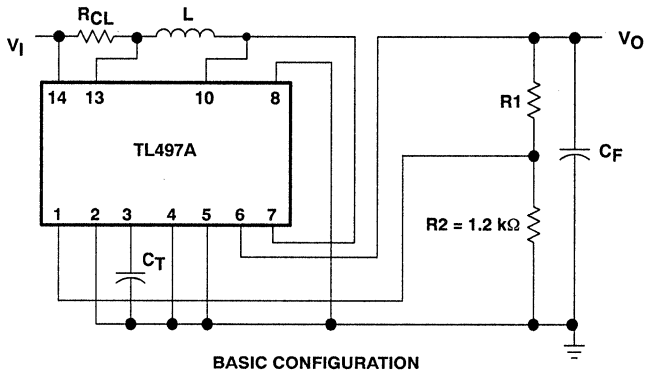
			MIN	MAX	UNIT
Supply voltage, V_{CC}			4.5	12	V
High-level input voltage, V_{IH}, INHIBIT			2.5		V
Low-level input voltage, V_{IL}, INHIBIT				0.8	V
Output voltage	Step-up configuration (see Figure 1)		$V_I + 2$	30	V
	Step-down configuration (see Figure 2)		V_{ref}	$V_I - 1$	
	Inverting regulator (see Figure 3)		$-V_{ref}$	−25	
Power switch current				500	mA
Diode forward current				500	mA
Operating free-air temperature, T_A		TL497AC	0	70	°C
		TL497AI	−40	85	

electrical characteristics at specified free-air temperature, V_{CC} = 6 V (unless otherwise noted)

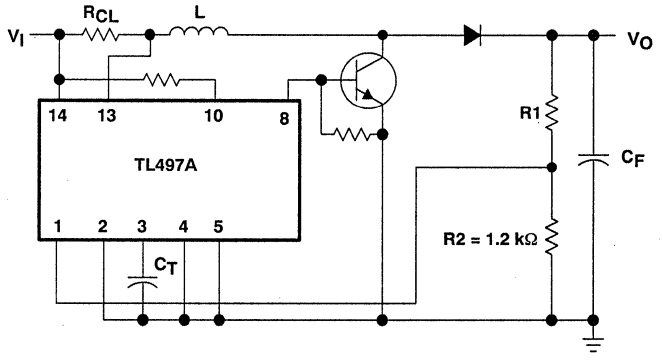
PARAMETER	TEST CONDITIONS		T_A†	TL497AC			TL497AI			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level inhibit input current	$V_{I(I)}$ = 5 V		Full range		0.8	1.5		0.8	1.5	mA
Low-level inhibit input current	$V_{I(I)}$ = 0 V		Full range		5	10		5	20	μA
Comparator reference voltage	V_I = 4.5 V to 6 V		Full range	1.08	1.2	1.32	1.14	1.2	1.26	V
Comparator input bias current	V_I = 6 V		Full range		40	100		40	100	μA
Switch on-state voltage	V_I = 4.5 V	I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
		I_O = 500 mA	Full range			0.85			1	
Switch off-state current	V_I = 4.5 V, V_O = 30 V		25°C		10	50		10	50	μA
			Full range			200			500	
Current-limit sense voltage	V_I = 6 V		25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA		Full range		0.75	0.85		0.75	0.95	V
	I_O = 100 mA		Full range		0.9	1		0.9	1.1	
	I_O = 500 mA		Full range		1.33	1.55		1.33	1.75	
Diode reverse voltage	I_O = 500 μA		Full range				30			V
	I_O = 200 μA		Full range	30						
On-state supply current			25°C		11	14		11	14	mA
			Full range			15			16	
Off-state supply current			25°C		6	9		6	9	mA
			Full range			10			11	

† Full range for the TL497AC is 0°C to 70°C and full range for the TL497AI is −40°C to 85°C.
‡ All typical values are at T_A = 25°C.

APPLICATION INFORMATION



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\ I_O max \left[\frac{V_O}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}} t_{on}\ (\mu s)$

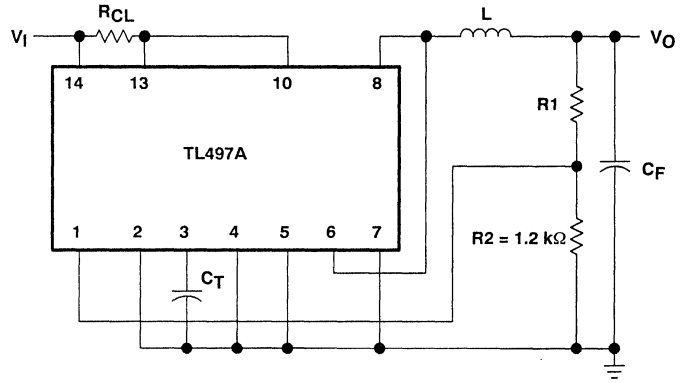
Choose L (50 to 500 μH), calculate t_{on} (25 to 150 μs)

- $C_T (pF) \approx 12\ t_{on}\ (\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$
- $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{V_O} I_{PK} + I_O\right]}{V_{ripple}\ (PK)}$

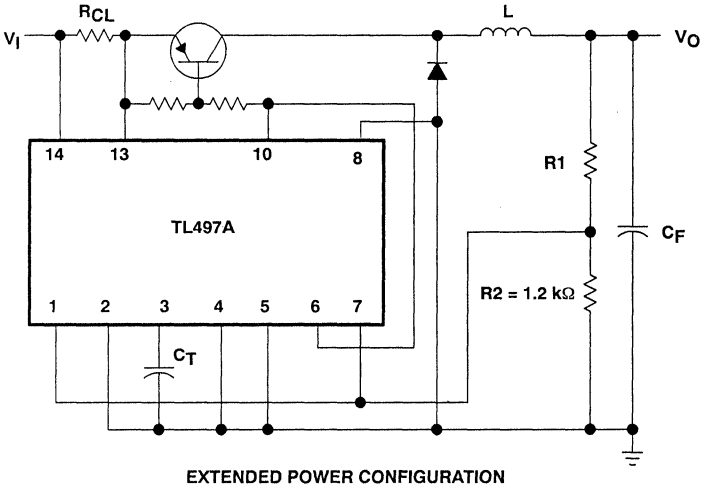
Figure 1. Positive Regulator, Step-Up Configurations

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

DESIGN EQUATIONS

- $I_{PK} = 2\ I_O max$
- $L\ (\mu H) = \dfrac{V_I - V_O}{I_{PK}} t_{on}(\mu s)$

Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

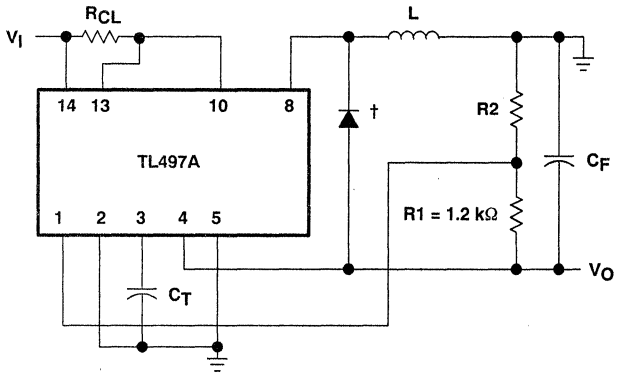
- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$

$$R_{CL} = \frac{0.5\ V}{I_{PK}}$$

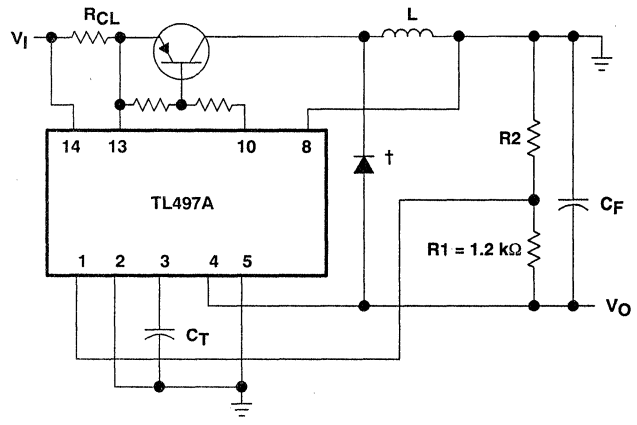
- $$C_F\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\dfrac{V_I}{V_O} I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$$

Figure 2. Positive Regulator, Step-Down Configurations

APPLICATION INFORMATION



BASIC CONFIGURATION
(I_{PK} < 500 mA)



EXTENDED POWER CONFIGURATION
(USING EXTERNAL TRANSISTOR)

† Use external catch-diode, e.g., 1N4001, when building an inverting supply with the TL497A.

Figure 3. Inverting Applications

DESIGN EQUATIONS

- $I_{PK} = 2\ I_{O\,max}\left[1 + \frac{|V_O|}{V_I}\right]$
- $L\ (\mu H) = \frac{V_I}{I_{PK}} t_{on}(\mu s)$

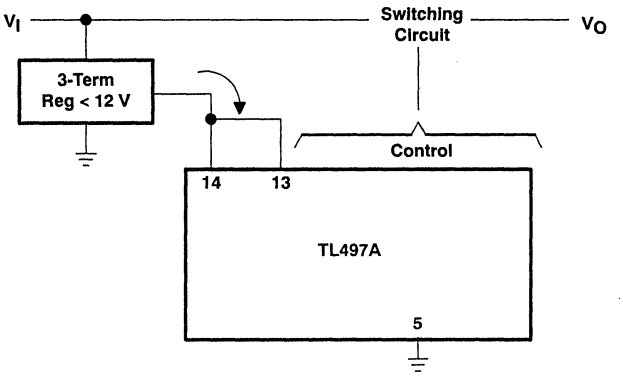
Choose L (50 to 500 μH), calculate t_{on} (10 to 150 μs)

- $C_T(pF) \approx 12\ t_{on}(\mu s)$
- $R1 = (V_O - 1.2)\ k\Omega$

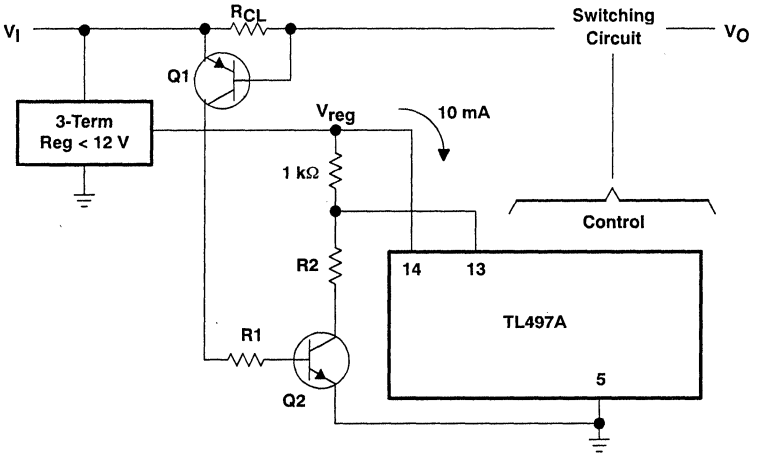
  $R_{CL} = \frac{0.5\ V}{I_{PK}}$
- $C_F\ (\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{V_O} I_{PK} + I_O\right]}{V_{ripple\ (PK)}}$

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION



EXTENDED INPUT CONFIGURATION WITHOUT CURRENT LIMIT



CURRENT LIMIT FOR EXTENDED INPUT CONFIGURATION

DESIGN EQUATIONS

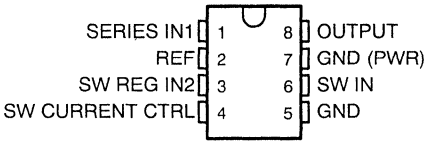
- $R_{CL} = \frac{V_{BE(Q1)}}{I_{limit\ (PK)}}$
- $R1 + \frac{V_I}{I_{B(Q2)}}$
- $R2 = (V_{reg} - 1)\ 10\ k\Omega$

Figure 4. Extended Input Voltage Range (V_I > 12 V)

D2762, JANUARY 1984–REVISED NOVEMBER 1991

- **Internal Series-Pass and Step-Up Switching Regulator**
- **Output Adjustable From 2.9 V to 30 V**
- **1-V to 10-V Input for Switching Regulator**
- **4.5-V to 32-V Input for Series Regulator**
- **Externally-Controlled Switching Current**
- **No External Rectifier Required**

D OR P PACKAGE
(TOP VIEW)



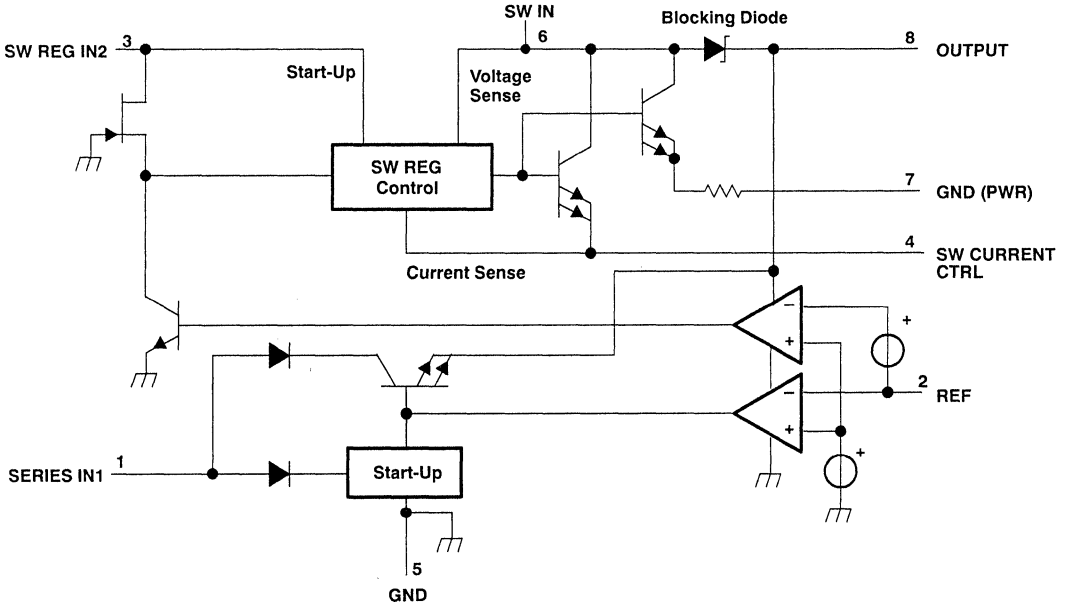
description

The TL499AC is a monolithic integrated circuit designed to provide a wide range of adjustable regulated supply voltages. The regulated output voltage is adjustable from 2.9 V to 30 V by adjusting two external resistors. When the TL499AC is ac-coupled to line power through a step-down transformer, it operates as a series dc voltage regulator to maintain the regulated output voltage. With the addition of a battery from 1.1 V to 10 V, an inductor, a filter capacitor, and two resistors, the TL499AC operates as a step-up switching regulator during an ac-line failure.

The adjustable regulated output voltage makes the TL499AC useful for a wide range of applications. Providing backup power during an ac-line failure makes the TL499AC extremely useful as backup power in microprocessor memory applications.

The TL499AC is designed for operation from –20°C to 85°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage, V_O (see Note 1) ..... 35 V
Input voltage, series regulator, V_I1 ..... 35 V
Input voltage, switching regulator, V_I2 ..... 10 V
Blocking diode reverse voltage ..... 35 V
Blocking diode forward current ..... 1 A
Power switch current (at SW IN) ..... 1 A
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... –20°C to 85°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	825 mW	6.6 mW/°C	429 mW
P	1000 mW	8 mW/°C	520 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Output voltage, V_O	2.9		30	V
Input voltage, SERIES IN1, V_I1	4.5		32	V
Input voltage, SW REG IN2, V_I2	1.1		10	V
Output-to-input differential voltage, switching regulator, $V_O - V_I2$ (see Note 2)	1.2		28.9	V
Continuous output current, I_O			100	mA
Power switch current (at SW IN)			500	mA
Current-limiting resistor, R_{CL}	150		1000	Ω
Filter capacitor	100		470	μF
Pass capacitor		0.1		μF
Inductor, L ($r_i \leq 0.1$ Ω)	50		150	μH
Operating free-air temperature, T_A	–20		85	°C

NOTE 2: When operating temperature range is $T_A \leq 70°C$, minimum $V_O - V_I2$ is ≥ 1.2 V. When operating temperature range is $T_A \leq 85°C$, minimum $V_O - V_I2$ is ≥ 1.9 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage deviation (see Note 3)				2%	3%	
Dropout voltage	Switching regulator	T_A = −20°C to 70°C			1.2	V
		T_A = −20°C to 85°C			1.9	V
	Series regulator	V_I1 = 15 V, I_O = 50 mA			1.8	V
Reference voltage (internal)		V_I2 = 5 V, V_O = 3 V, I_O = 1 mA	1.2	1.26	1.32	V
Reference voltage change with temperature		T_A = −20°C to 85°C		0.5%	1%	
Output regulation (of reference voltage)		I_O = 1 mA to 50 mA		1%	3%	
Output current (see Figure 1)	Switching regulator	V_I2 = 1.1 V, V_O = 12 V, R_{CL} = 150 Ω, T_A = 25°C	10			mA
		V_I2 = 1.5 V, V_O = 15 V, R_{CL} = 150 Ω, T_A = 25°C	15			
		V_I2 = 6 V, V_O = 30 V, R_{CL} = 150 Ω, T_A = 25°C	65			
	Series regulator				100	
Standby current	Switching regulator	V_I2 = 3 V, V_O = 9 V, T_A = 25°C		15	80	μA
	Series regulator	V_I1 = 15 V, V_O = 9 V, R_E2 = 4.7 kΩ		0.8	1.2	mA

NOTE 3: Voltage deviation is the output voltage change in percent that occurs in a change from series regulation to switching regulation.

$$\text{voltage deviation} = \frac{V_O \text{ (series reg)} - \text{(switching reg)}}{V_O \text{ (series reg)}} \times 100\%$$

APPLICATION INFORMATION

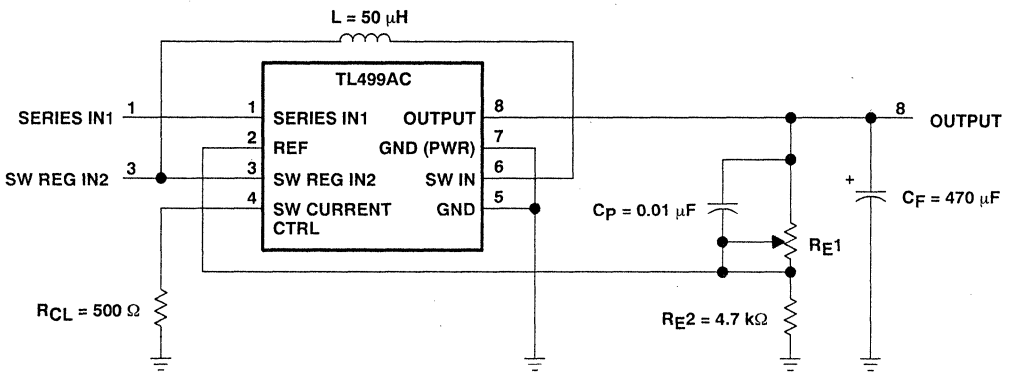


Figure 1. TL499AC Basic Configuration

Table 1. Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 150 Ω

V_O, OUTPUT VOLTAGE (V)	V_I2, SWITCHING REGULATOR INPUT VOLTAGE (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	I_O, OUTPUT CURRENT (mA)										
30										65	90
25									50	80	100
20						20	25	30	80	100	100
15				15	20	30	45	55	100	100	100
12	10	15	20	25	30	40	55	70	100	100	100
10	15	20	25	30	35	45	65	80	100	100	
9	20	25	25	35	40	50	70	90	100	100	
6	30	35	40	45	55	75	95	100			
5	35	40	45	55	70	85	100	100	Circuit of Figure 1 except:		
4.5	35	45	50	60	75	95	100	100†	R_{CL} = 150 Ω		
3	55	65†	75†	95†	100†				C_F = 330 μF		
2.9	60†	70†	75†	100†	100†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

APPLICATION INFORMATION

Table 2. Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 200 Ω

V_O, OUTPUT VOLTAGE (V)	V_I2, SWITCHING REGULATOR INPUT VOLTAGE (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	I_O, OUTPUT CURRENT (mA)										
30										50	100
25									50	70	100
20						15	25	30	70	90	100
15				10	15	25	35	45	90	100	100
12	10	10	15	20	25	35	45	60	100	100	100
10	15	20	20	25	30	40	55	70	100	100	
9	20	20	25	30	35	45	60	80	100		
6	25	30	35	45	50	65	90	100			
5	30	35	40	55	60	75	100	100	Circuit of Figure 1 except:		
4.5	35	40	45	55	65	85	100	100†	R_{CL} = 200 Ω		
3	50	55†	65†	80†	90†				C_F = 330 μF		
2.9	50†	60†	65†	85†	100†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 3. Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 300 Ω

V_O, OUTPUT VOLTAGE (V)	V_I2, SWITCHING REGULATOR INPUT VOLTAGE (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	I_O, OUTPUT CURRENT (mA)										
30										40	70
25									40	55	100
20						10	15	20	55	70	100
15				10	10	20	30	35	75	95	100
12	10	10	10	15	20	25	35	45	95	100	100
10	15	15	15	20	25	30	45	55	100	100	
9	15	15	20	25	30	35	50	60	100	100	
6	25	25	30	35	45	55	70	90			
5	30	30	35	45	50	65	85	100	Circuit of Figure 1 except:		
4.5	30	35	40	45	55	70	95	100†	R_{CL} = 300 Ω		
3	45	50†	55†	70†	90†				C_F = 330 μF		
2.9	45†	50†	60†	75†	95†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

APPLICATION INFORMATION

Table 4. Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 510 Ω

V_O, OUTPUT VOLTAGE (V)	V_I2, SWITCHING REGULATOR INPUT VOLTAGE (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	I_O, OUTPUT CURRENT (mA)										
30										30	50
25									25	40	75
20									40	55	90
15							15	20	55	70	100
12					10	15	25	35	65	80	100
10				10	20	25	30	40	70	85	
9	10	10	10	15	20	25	35	45	75	100	
6	15	20	20	25	30	35	50	60			
5	20	20	25	30	35	45	55	70	Circuit of Figure 1 except:		
4.5	20	25	30	35	40	50	65	90†	R_{CL} = 510 Ω		
3	35	35†	40†	50†	75†				C_F = 330 μF		
2.9	35†	35†	40†	55†	80†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

Table 5. Output Current vs Input and Output Voltages for Step-Up Switching Regulator With R_{CL} = 1 kΩ

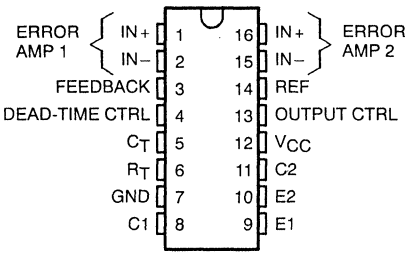
V_O, OUTPUT VOLTAGE (V)	V_I2, SWITCHING REGULATOR INPUT VOLTAGE (V)										
	1.1	1.2	1.3	1.5	1.7	2	2.5	3	5	6	9
	I_O, OUTPUT CURRENT (mA)										
30											35
25										35	50
20										35	60
15								10	30	45	65
12								20	40	45	85
10							15	25	40	55	
9				10	10	15	25	30	45	60	
6	10	10	10	15	20	20	30	35			
5	10	10	15	20	20	25	35	40	Circuit of Figure 1 except:		
4.5	15	15	15	20	25	30	40	45†	R_{CL} = 1 kΩ		
3	20	25†	25†	30†	35†				C_F = 330 μF		
2.9	20†	25†	25†	30†	45†				C_P = 0.1 μF		

† The difference between the output and input voltage for these combinations is greater than the minimum output-to-input differential voltage specification at 70°C (1.2 V), but less than the minimum at 85°C (1.9 V).

D2712, APRIL 1988–REVISED NOVEMBER1991

- **Complete PWM Power Control Circuitry**
- **Uncommitted Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Single-Ended or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply Trimmed to 1%**
- **Circuit Architecture Allows Easy Synchronization**
- **Undervoltage Lockout for Low V_{CC} Conditions**

D OR N PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGE	
	SURFACE MOUNT (D)	PLASTIC DIP (N)
0°C to 70°C	TL594CD	TL594CN
−40°C to 85°C	TL594ID	TL594IN

The D package is available taped and reeled. Add "R" suffix to device type (e.g., TL594CDR).

FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
$V_I \le 0$	Single-ended or parallel output
$V_I \le$ REF	Normal push-pull operation

description

The TL594 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, these devices offer the systems engineer the flexibility to tailor the power supply control circuitry to a specific application.

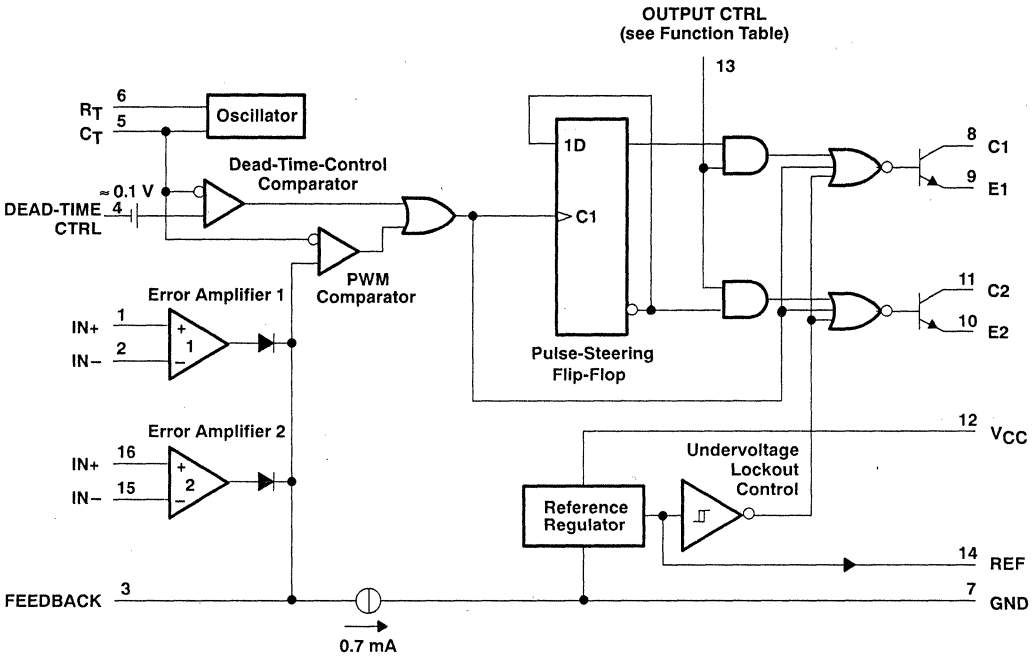
The TL594 contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control comparator, a pulse-steering control flip-flop, a 5-V regulator with a precision of 1%, an undervoltage lockout control circuit, and output control circuitry.

The error amplifiers exhibit a common-mode voltage range from −0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that provides approximately 5% dead time when externally altered. The on-chip oscillator may be bypassed by terminating R_T to the reference output and providing a sawtooth input to C_T, or it may be used to drive the common circuitry in synchronous multiple-rail power supplies.

The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Each device provides for push-pull or single-ended output operation with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output being pulsed twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

The TL594C is characterized for operation from 0°C to 70°C. The TL594I is characterized for operation from −40°C to 85°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL594C	TL594I	UNIT
Supply voltage, V_{CC} (see Note 1)	41	41	V
Amplifier input voltage	$V_{CC}+0.3$	$V_{CC}+0.3$	V
Collector output voltage	41	41	V
Collector output current	250	250	mA
Continuous total dissipation	See Dissipation Rating Table		
Operating free-air temperature range	0 to 70	−40 to 85	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: All voltage values, except differential voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	494 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	598 mW

recommended operating conditions

	TL594C		TL594I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltage, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10000	0.47	10000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency, f_{osc}	1	300	1	300	kHz
Operating free-air temperature, T_A	0	70	−40	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Output voltage (REF)	I_O = 1 mA,	T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7 V to 40 V,	T_A = 25°C		2	25	mV
Output regulation	I_O = 1 to 10 mA,	T_A = 25°C		14	35	mV
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2%	1%*	
Short-circuit output current§	V_{ref} = 0		10	35	50	mA

oscillator section, C_T = 0.01 μF, R_T = 12 kΩ (see Figure 2)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			10		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, and T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%		
Frequency change with temperature#	ΔT_A = MIN to MAX			5%	

amplifier section (see Figure 1)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
Input offset voltage, error amplifier	FEEDBACK at 2.5 V				2	10	mV
Input offset current	FEEDBACK at 2.5 V				25	250	nA
Input bias current	FEEDBACK at 2.5 V				0.2	1	μA
Common-mode input voltage range, error amplifier	V_{CC} = 7 V to 40 V			0.3 to V_{CC}–2			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3 V,	R_L = 2 kΩ,	V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth	V_O = 0.5 V to 3.5 V,	R_L = 2 kΩ			800		kHz
Common-mode rejection ratio, error amplifier	V_{CC} = 40 V,	T_A = 25°C		65	80		dB
Output sink current (pin 3)	V_{ID} = –15 mV to –5 V,	FEEDBACK at 0.5 V		0.3	0.7		mA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V,	FEEDBACK at 3.5 V		–2			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{X})^2}{N-1}}$
# Temperature coefficient of timing capacitor and timing resistor not taken into account.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted)

dead-time control section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input bias current	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	DEAD-TIME CTRL at 0 V	45%			
Input threshold voltage	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

output section

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Collector off-state current		V_C = 40 V, V_E = 0 V, V_{CC} = 40 V		2	100	μA
		V_C = 15 V, V_E = 0 V, V_{CC} = 1 to 3 V, DEAD-TIME CTRL and OUTPUT CTRL at 0 V		4	200	
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Collector-emitter saturation voltage	Common emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V, I_E = −200 mA		1.5	2.5	
Output control input current		V_I = REF			3.5	mA

pwm comparator section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input threshold voltage, FEEDBACK	Zero duty cycle		4	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V	0.3	0.7		mA

undervoltage lockout section (see Figure 2)

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Threshold voltage	T_A = 25°C		6	V
	ΔT_A = MIN to MAX	3.5	6.9	
Hysteresis§		100		mV

total device (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Standby supply current	R_T at REF, All other inputs and outputs open	V_{CC} = 15 V		9	15	mA
		V_{CC} = 40 V		11	18	
Average supply current	DEAD-TIME CTRL at 2 V,	See Figure 2		12.4		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			30	100	
Output voltage rise time	Emitter-follower configuration, See Figure 4		200	400	
Output voltage fall time			45	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

PARAMETER MEASUREMENT INFORMATION

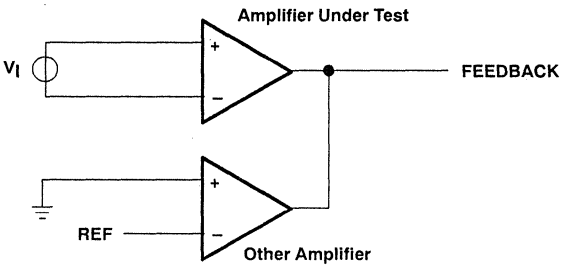

Figure 1. Amplifier Characteristics Test Circuit

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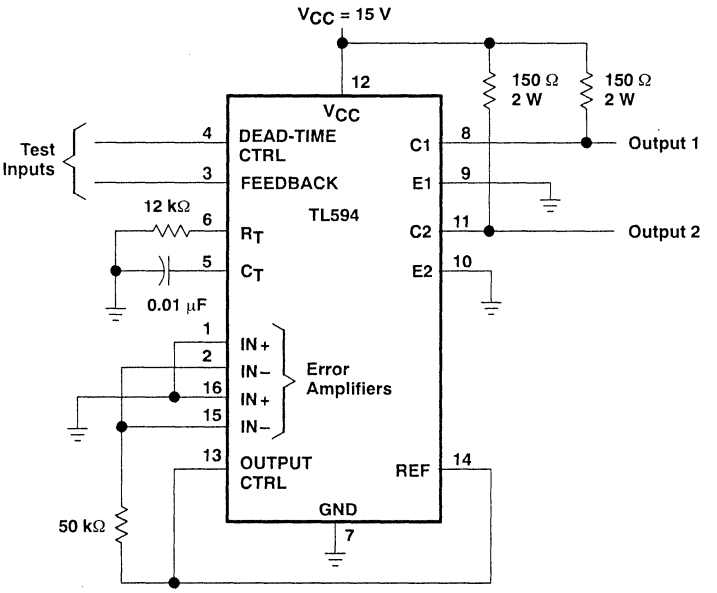
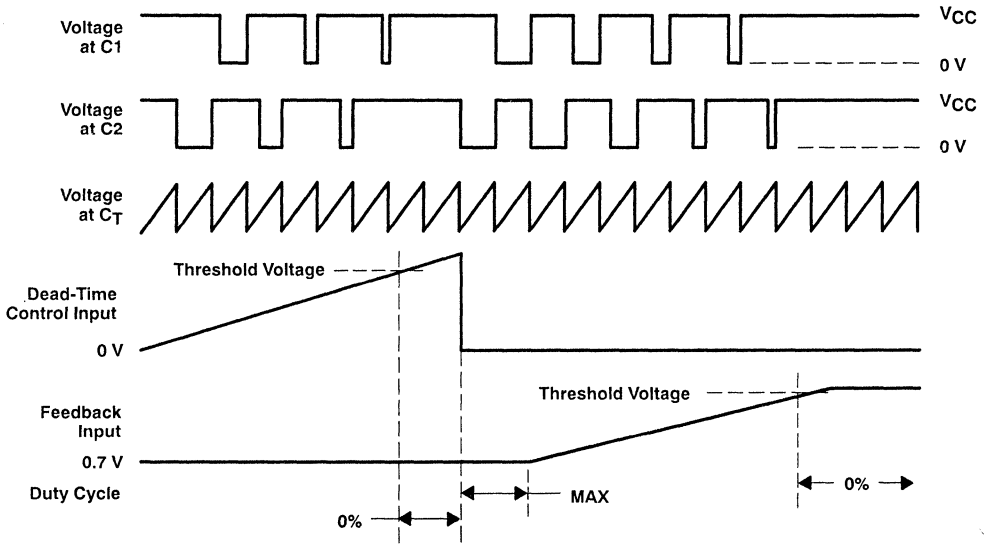
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Operational Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

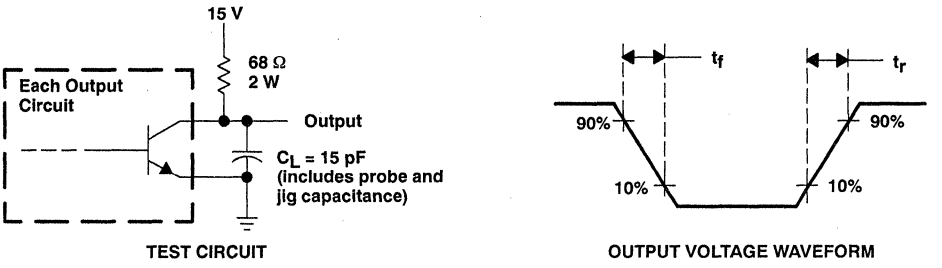


Figure 3. Common-Emitter Configuration

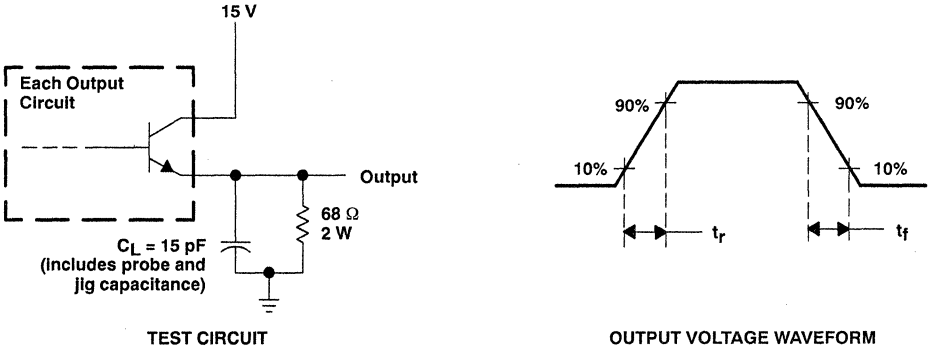


Figure 4. Emitter-Follower Configuration

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND
FREQUENCY VARIATION†
vs
TIMING RESISTANCE

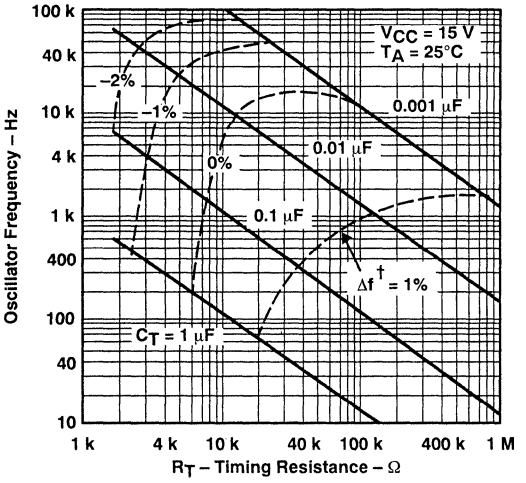


Figure 5

AMPLIFIER VOLTAGE AMPLIFICATION
vs
FREQUENCY

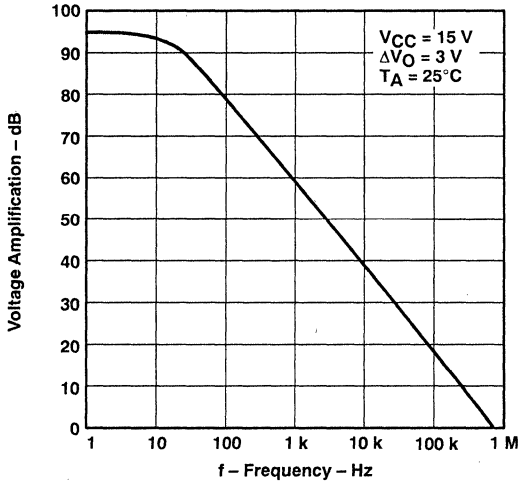


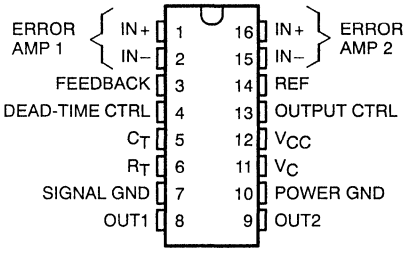
Figure 6

† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

D3026, FEBRUARY 1988–REVISED SEPTEMBER 1991

- **Complete PWM Power Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead-Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Undervoltage Lockout for Low V_{CC} Conditions**
- **Separate Power and Signal Grounds**
- **TL598Q Has Extended Temperature Range . . . –40°C to 125°C**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = REF	Normal push-pull operation

description

The TL598 incorporates all the functions required in the construction of pulse-width-modulated controlled systems on a single monolithic chip. Designed primarily for power supply control, the TL598 provides the systems engineer with the flexibility to tailor the power supply control circuits to a specific application.

The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control comparator, a pulse-steering flip-flop, a 5-V precision reference, an undervoltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise and fall time performance for power FET control. The outputs share a common source supply and common power ground pins, which allow system designers to eliminate errors caused by high, current-induced voltage drops and common-mode noise.

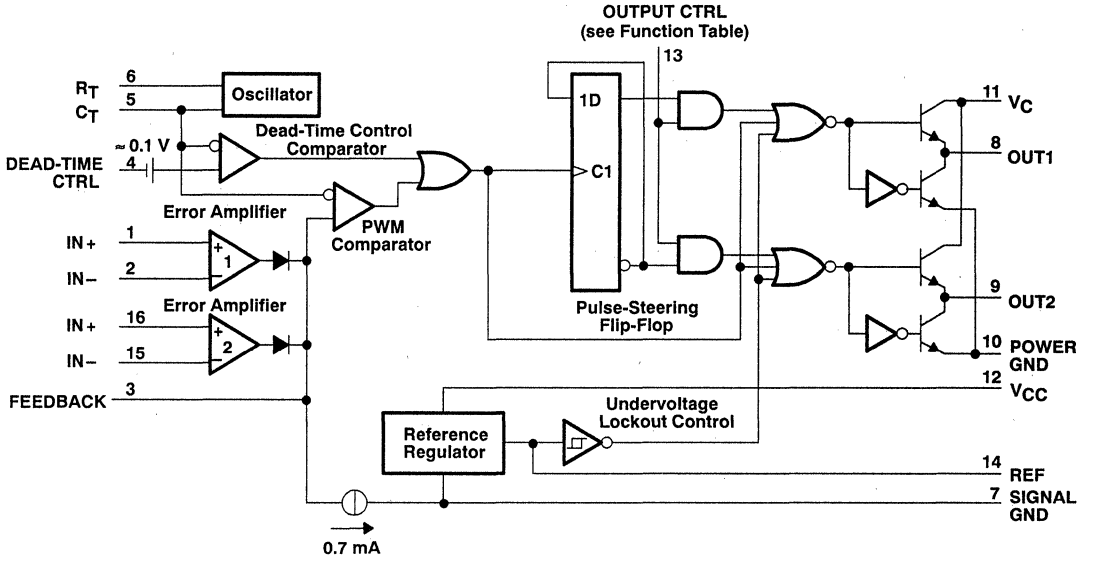
The error amplifier has a common-mode voltage range from 0 V to V_{CC} –2 V. The dead-time control comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. Synchronous multiple supply operation may be achieved by connecting pin 6 to the reference output and providing a sawtooth input to pin 5.

The TL598 device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation. The output frequency for push-pull applications is one-half the oscillator frequency ($f_o = \frac{1}{2 R_T C_T}$). For single-ended applications:

$$f_o = \frac{1}{R_T C_T}$$

The TL598C is characterized for operation from 0°C to 70°C. The TL598Q is characterized for operation from –40°C to 125°C.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage, V_I ..... V_{CC} + 0.3 V
Collector voltage ..... 41 V
Output current (each output), sink or source, I_O ..... 250 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J: TL598C ..... 0°C to 150°C
TL598Q ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values, except differential voltages, are with respect to the signal ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	6.8 mW	190 mW
N	1150 mW	9.2 mW/°C	736 mW	230 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		7	40	V
Amplifier input voltage, V_I		0	$V_{CC}-2$	V
Collector voltage			40	V
Output current (each output), sink or source, I_O			200	mA
Current into feedback terminal, I_{IL}			0.3	mA
Timing capacitor, C_T		0.00047	10	μF
Timing resistor, R_T		1.8	500	kΩ
Oscillator frequency, f_{osc}		1	300	kHz
Operating free-air temperature, T_A	TL598C	0	70	°C
	TL598Q	−40	125	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted) (see Note 2)

reference section

PARAMETER	TEST CONDITIONS†		TL598C			TL598Q			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	25		2	22	mV
Output regulation	I_O = 1 to 10 mA	T_A = 25°C		1	15		1	15	mV
		T_A = MIN to MAX			50			80	
Output voltage change with temperature	ΔT_A = MIN to MAX			0.2%	1%		0.2%	1%	
Short-circuit output current§	REF = 0		−10	−48		−10	−48		mA

oscillator section, C_T = 0.001 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			100		kHz
Standard deviation of frequency¶	All values of V_{CC}, C_T, R_T, T_A constant		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1%	1%	
Frequency change with temperature#	ΔT_A = MIN to MAX		7%	12%	
	ΔT_A = MIN to MAX, C_T = 0.01 μF		5%	8%	

error amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	Feedback pin at 2.5 V		2	10	mV
Input offset current	Feedback pin at 2.5 V		25	250	nA
Input bias current	Feedback pin at 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	0 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O (pin 3) = 3 V, V_O (pin 3) = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 6.5 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	Feedback pin at 0.5 V	0.3	0.7		mA
Output source current (pin 3)	Feedback pin at 3.5 V	−2			mA
Phase margin at unity gain	Feedback pin at 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply voltage rejection ratio	Feedback pin at 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - X)^2}{N-1}}$
# Effects of temperature on external R_T and C_T are not taken into account.
NOTE 2: Pulse-testing techniques that will maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V (unless otherwise noted) (see Note 2)

undervoltage lockout section

PARAMETER	TEST CONDITIONS†	TL598C		TL598Q		UNIT
		MIN	MAX	MIN	MAX	
Threshold voltage	T_A = 25°C	4	6	4	6	V
	ΔT_A = MIN to MAX	3.5	6.9	3	6.9	
Hysteresis‡	T_A = 25°C	100		100		mV
	T_A = MIN to MAX	50		30		

output section

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Collector off-state current	V_{CE} = 40 V, V_{CC} = 40 V, Dead-time pin is connected to 0 V			2	100	μA
High-level output voltage	V_{CC} = 15 V,	I_O = −200 mA	12			V
	V_C = 15 V	I_O = −20 mA	13			
Low-level output voltage	V_{CC} = 15 V,	I_O = 200 mA			2	V
	V_C = 15 V	I_O = 20 mA			0.4	
Output control input current	V_I = REF				3.5	mA
	V_I = 0.4 V				100	μA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	TL598C			TL598Q			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10		−2	−25	μA
Maximum duty cycle, each output	Dead-time control at 0 V	45%			45%			
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3		3	3.2	V
	Maximum duty cycle	0			0			

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
Input threshold voltage (pin 3)	Dead-time control = 0 V		3.75	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.5 V	0.3	0.7		mA

total device (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Standby supply current	Pin 6 at REF,	V_{CC} = 15 V		15	21	mA
	All other inputs and outputs open	V_{CC} = 40 V		20	26	
Average supply current	Dead-time control at 2 V			15		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage rise time	C_L = 1500 pF, V_C = 15 V, V_{CC} = 15 V, See Figure 2		60	150	ns
Output voltage fall time			35	75	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 2: Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

PARAMETER MEASUREMENT INFORMATION

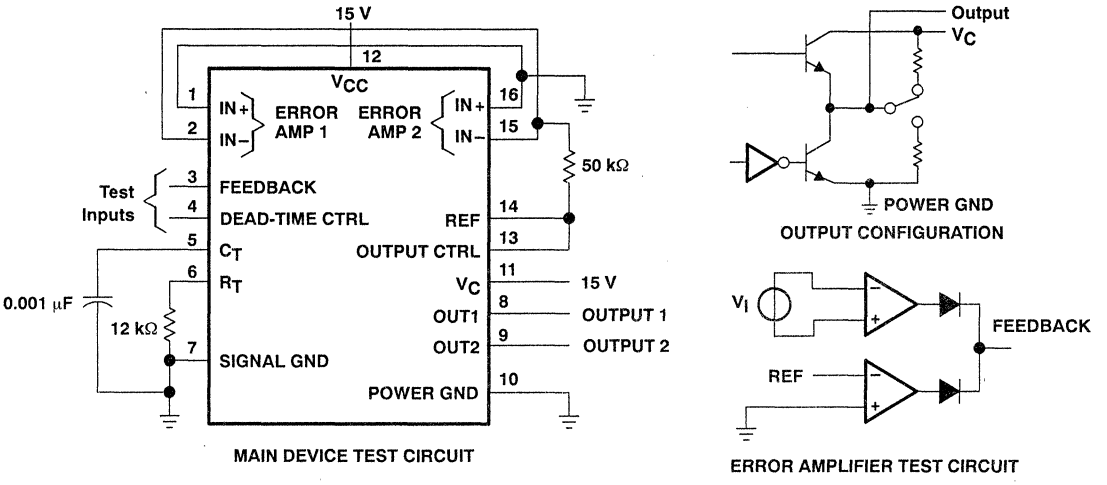


Figure 1. Test Circuits

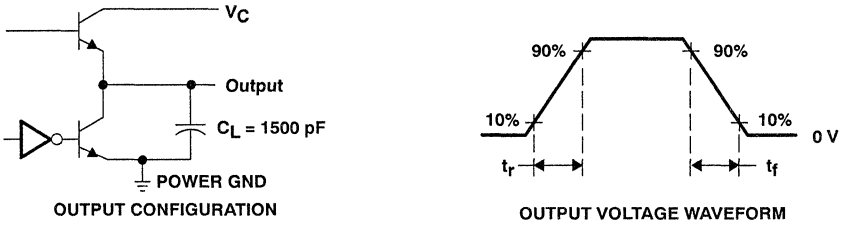
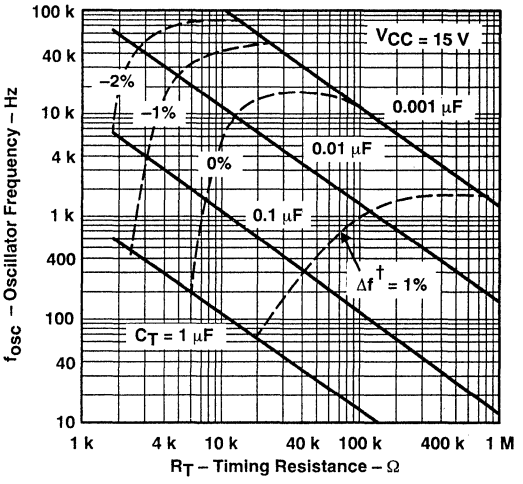


Figure 2. Switching Output Configuration and Voltage Waveform

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† vs TIMING RESISTANCE



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 3

AMPLIFIER VOLTAGE AMPLIFICATION vs FREQUENCY

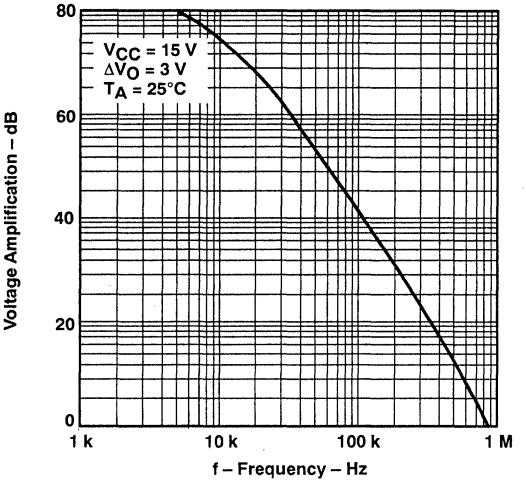
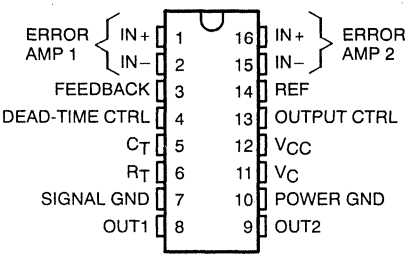


Figure 4

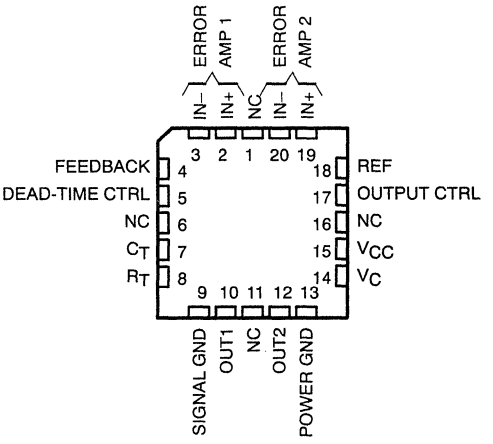
D3726, APRIL 1991–REVISED SEPTEMBER 1991

- **Complete PWM Power Control Function**
- **Totem-Pole Outputs for 200-mA Sink or Source Current**
- **Output Control Selects Parallel or Push-Pull Operation**
- **Internal Circuitry Prohibits Double Pulse at Either Output**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 5-V Reference Supply, Trimmed to 1% Tolerance**
- **On-Board Output Current-Limiting Protection**
- **Undervoltage Lockout for Low V_{CC} Conditions**
- **Separate Power and Signal Grounds**

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL598M incorporates all the functions required in the construction of pulse-width-modulated controlled systems on a single monolithic chip. Designed primarily for power supply control, the TL598M provides the systems engineer with the flexibility to tailor the power supply control circuits to a specific application.

The TL598M contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control comparator, a pulse-steering flip-flop, a 5-V precision reference, an undervoltage lockout control, and output control circuits. Two totem-pole outputs provide exceptional rise and fall time performance for power FET control. The outputs share common source supply and power ground pins, which allow system designers to eliminate errors caused by high current-induced voltage drops and common-mode noise.

FUNCTION TABLE

INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
V_I = REF	Normal push-pull operation

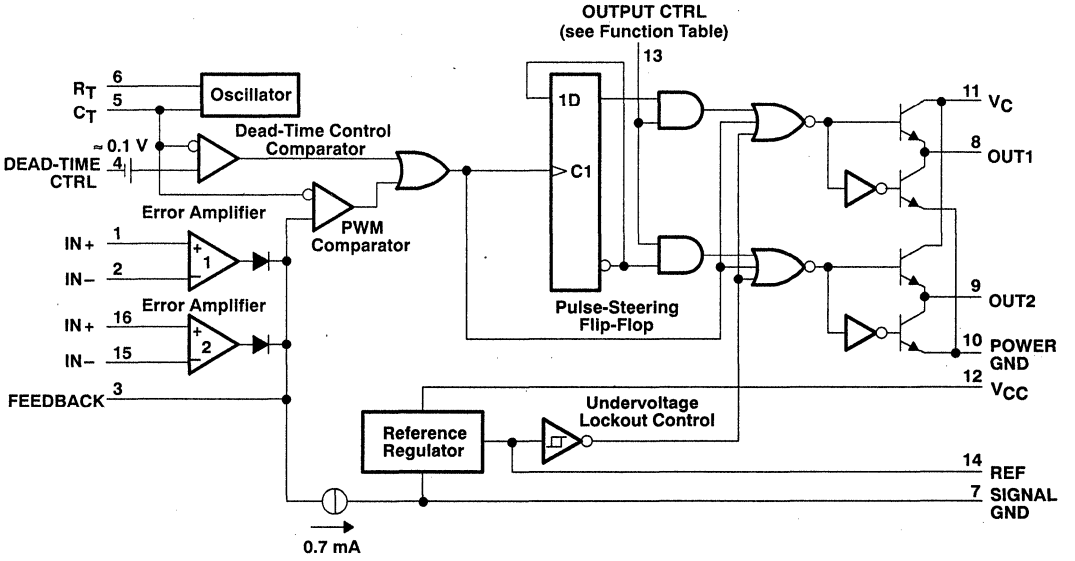
The error amplifier has a common-mode voltage range from 0.3 V to V_{CC} −2 V. The dead-time control comparator has a fixed offset that prevents overlap of the outputs during push-pull operation. Synchronous multiple supply operation may be achieved by connecting pin 6 to the reference output and providing a sawtooth input to pin 5.

description (continued)

The TL598M device provides an output control function to select either push-pull or parallel operation. Circuit architecture prevents either output from being pulsed twice during push-pull operation. The output frequency for push-pull applications is one-half the oscillator frequency ($f_o = \frac{1}{2 R_T C_T}$). For single-ended applications: $f_o = \frac{1}{R_T C_T}$

The TL598M is characterized for operation from −55°C to 125°C.

logic diagram (positive logic)



Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 41 V
Amplifier input voltage, V_I ..... V_{CC} + 0.3 V
Collector voltage ..... 41 V
Output current (each output), sink or source, I_O ..... 250 mA
Continuous total dissipation (see Note 2) ..... 1375 mW
Operating virtual junction temperature range, T_J ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Case temperature for 60 seconds: FK package ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the signal ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 275 mW at the rate of 11 mW/°C.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Amplifier input voltage, V_I	0.3	V_{CC}−2	V
Collector voltage		40	V
Output current (each output), sink or source, I_O		200	mA
Current into FEEDBACK terminal, I_{IL}		0.3	mA
Timing capacitor, C_T	0.00047	10	μF
Timing resistor, R_T	1.8	500	kΩ
Oscillator frequency, f_{osc}	1	300	kHz
Operating free-air temperature, T_A	−55	125	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted) (see Note 3)

reference section

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Output voltage (REF)	I_O = 1 mA	T_A = 25°C	4.95	5	5.05	V
		T_A = MIN to MAX	4.9		5.1	
Input regulation	V_{CC} = 7 V to 40 V	T_A = 25°C		2	22	mV
Output regulation	I_O = 1 to 10 mA	T_A = 25°C		1	15	mV
		T_A = MIN to MAX			80	
Output voltage change with temperature	ΔT_A = MIN to MAX			0.5%		
Short-circuit output current§	REF = 0 V		−10	−48		mA

oscillator section, C_T = 0.001 μF, R_T = 12 kΩ (see Figure 1)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
Frequency			100		kHz
Standard deviation of frequency¶	T_A constant at any value within recommended operating conditons		10%		
Frequency change with voltage	V_{CC} = 7 V to 40 V, f_{osc} = 28.06 kHz, T_A = 25°C		0.1%	1%	
Frequency change with temperature#	ΔT_A = MIN to MAX		7%	15%*	

error amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Input offset voltage	FEEDBACK at 2.5 V		2	10	mV
Input offset current	FEEDBACK at 2.5 V		25	250	nA
Input bias current	FEEDBACK at 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V, T_A = 25°C	0.3 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O FEEDBACK = 3 V, V_O FEEDBACK = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, ΔV_{IC} = 37.7 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	FEEDBACK at 0.5 V	0.3	0.7		mA
Output source current (pin 3)	FEEDBACK at 3.5 V	−2			mA
Phase margin at unity gain	FEEDBACK at 0.5 V to 3.5 V, R_L = 2 kΩ		65°		
Supply voltage rejection ratio	FEEDBACK at 2.5 V, ΔV_{CC} = 33 V, R_L = 2 kΩ		100		dB

* This parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values except for parameter changes with temperature are at T_A = 25°C.
§ Duration of the short-circuit should not exceed one second.
¶ Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \overline{X})^2}{N-1}}$
# Effects of temperature on external R_T and C_T are not taken into account.
NOTE 3: Pulse-testing techniques that will maintain the junction temperature as close to the ambient temperature as possible must be used.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, (unless otherwise noted) (see Note 3)

undervoltage lockout section

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Threshold voltage	T_A = 25°C	4	6	V
	ΔT_A = MIN to MAX	3	6.9	
Hysteresis‡	T_A = 25°C	100		mV
	T_A = MIN to MAX	30		

output section

PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Collector off-state current	V_C = 40 V, V_{CC} = 40 V, DEAD-TIME CTRL at 0 V			2	100	μA
High-level output voltage	V_{CC} = 15 V,	I_O = −200 mA	12			V
	V_C = 15 V	I_O = −20 mA	13			
Low-level output voltage	V_{CC} = 15 V,	I_O = 200 mA			2	V
	V_C = 15 V	I_O = 20 mA			0.4	
Output control input current	V_I = REF				3.5	mA
	V_I = 0.4 V				100	μA

dead-time control section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
Input bias current	V_I = 0 to 5.25 V		−2	−25	μA
Maximum duty cycle, each output	DEAD-TIME CTRL at 0 V, T_A = 25°C	45%*			
Input threshold voltage	Zero duty cycle		3	3.2	V
	Maximum duty cycle	0*			

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
Input threshold voltage, FEEDBACK	DEAD-TIME CTRL = 0 V		3.75	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5 V	0.3	0.7		mA

total device (see Figure 1)

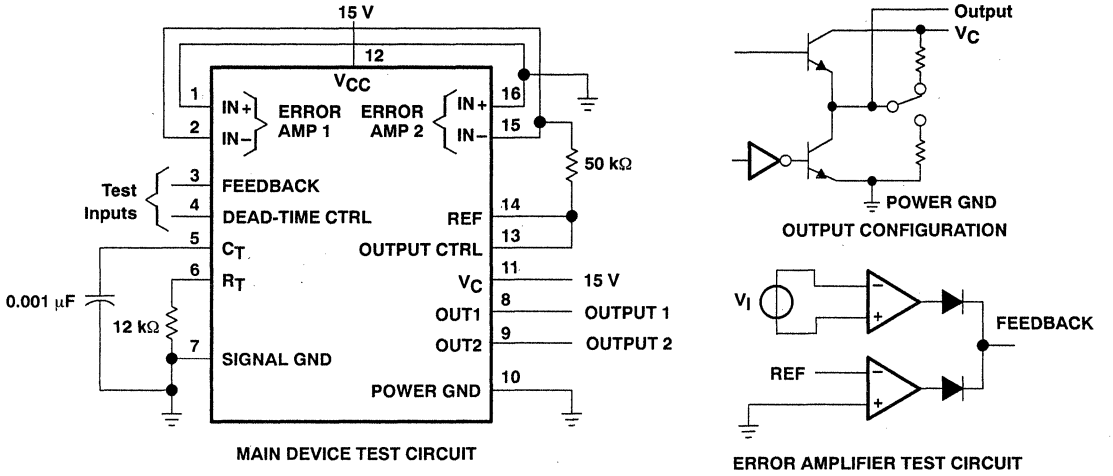
PARAMETER	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
Standby supply current	R_T at REF,	V_{CC} = 15 V		15	21	mA
	All other inputs and outputs open	V_{CC} = 40 V		20	26	
Average supply current	DEAD-TIME CTRL at 2 V			15		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
Output voltage rise time	V_{CC} = 15 V, V_C = 15 V, C_L = 1500 pF, See Figure 2		60	150*	ns
Output voltage fall time			35	75*	

* This parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.
§ All typical values except for parameter changes with temperature are at T_A = 25°C.
NOTE 3. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

PARAMETER MEASUREMENT INFORMATION



Pin numbers shown are for J package.

Figure 1. Test Circuits

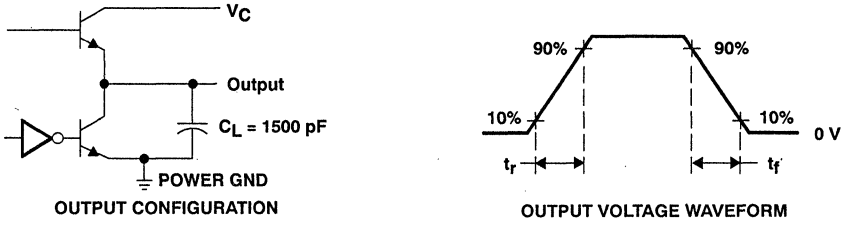
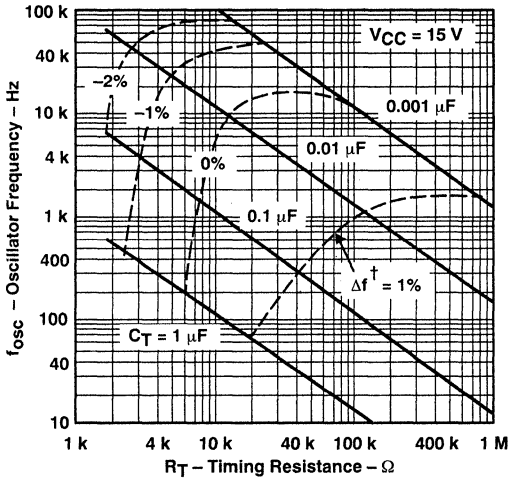


Figure 2. Switching Output Configuration and Voltage Waveform

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY AND FREQUENCY VARIATION† VS TIMING RESISTANCE



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 3

AMPLIFIER VOLTAGE AMPLIFICATION VS FREQUENCY

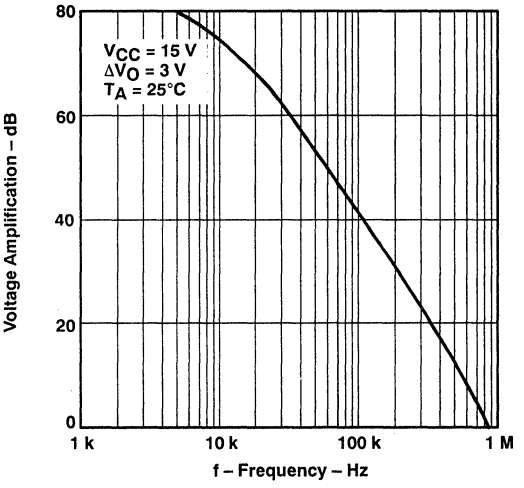


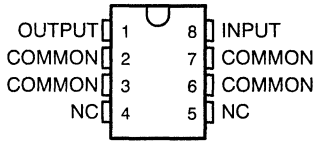
Figure 4

D3017, SEPTEMBER 1987–REVISED FEBRUARY 1991

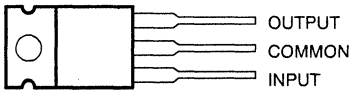
- Very Low Dropout Voltage, Less Than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751L Series, TL751L05M, and TL751L12M
- 60-V Load-Dump Protection
- Reverse Transient Protection to −50 V
- Internal Thermal Overload Protection
- Overvoltage Protection
- Internal Overcurrent Limiting Circuitry
- Less Than 500-μA Disable (TL751L Series, TL75L05M, and TL75L12M)

terminal assignments

TL750L . . . D
SMALL-OUTLINE PACKAGE
(TOP VIEW)



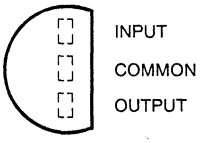
TL750L . . . KC
HEAT-SINK-MOUNTED PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

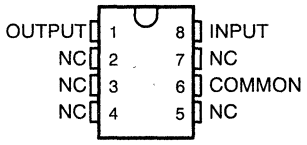
TO-220AB

TL750L . . . LP
SILECT™ PACKAGE
(TOP VIEW)

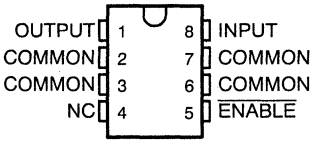


TO-226AA

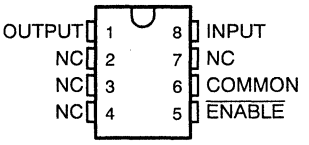
TL750L . . . P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



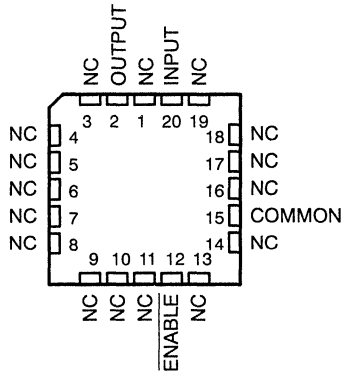
TL751L . . . D
SMALL-OUTLINE PACKAGE
(TOP VIEW)



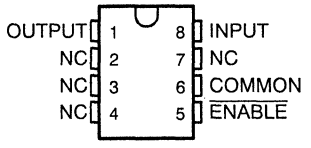
TL751L . . . P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL751L05M, TL751L12M . . . FK PACKAGE
(TOP VIEW)



TL751L05M, TL751L12M . . . JG PACKAGE
(TOP VIEW)



NC–No internal connection

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description

The TL750L and TL751L series and the TL751L05M and TL751L12M are low-dropout positive voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry along with internal reverse-battery protection circuitry to protect both itself and the regulated system. Both series and the TL751L05M and TL751L12M are fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

The TL750L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. They are available in TO-226AA (formerly TO-92) (LP) packages, TO-220AB (KC) packages, 8-pin small-outline plastic packages (D), and 8-pin plastic dual-in-line packages (P).

The TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. This series is offered in the 8-pin small-outline plastic package and the 8-pin plastic dual-in-line package.

The TL751L05M and TL751L12M fixed-output voltage regulators also offer 5-V and 12-V options with an enable input. The enable input, when taken high, places the regulator output in a high-impedance state. This gives the designer complete control over power up, power down, or emergency shut down. This TL751L_M is offered in the FK and JG package.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)

		TL750L	TL751L TL751L_M	UNIT
Continuous input voltage		26	26	V
Transient input voltage, T_A = 25°C (see Note 1)		60	60	V
Continuous reverse input voltage		−15	−15	V
Transient reverse input voltage: t ≤ 100 ms		−50	−50	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	D package	825	825	mW
	FK package		1375	
	JG package		1050	
	KC package	2000		
	LP package	775		
	P package	1000	1000	
Operating virtual junction temperature range		−40 to 150	−40 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) for 10 seconds		260	260	°C

NOTES: 1. The transient input voltage rating applies for the waveform described in Figure 1.
2. For operation above 25°C free-air temperature, linearly derate the D package at the rate of 6.6 mW/°C, the FK package at 11 mW/°C, the JG package at 8.4 mW/°C, the KC package at 15.2 mW/°C, the LP package at 6.2 mW/°C, and the P package at 8 mW/°C.

recommended operating conditions over recommended operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNITS
Input voltage, V_I		TL75_L05 and TL751L05M	6	26	V
		TL75_L08	9	26	
		TL75_L10	11	26	
		TL75_L12 and TL751L12M	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}		TL751L and TL751L_M	2	15	V
Low-level $\overline{\text{ENABLE}}$ input voltage	V_{IL}†, T_A = 25°C	TL751L and TL751L_M	−0.3	0.8	V
	V_{IL}†, T_A = Full range	TL751L and TL751L_M	−0.15	0.8	V
Output current range, I_O		TL75_L and TL751L_M	0	150	mA
Operating virtual junction temperature, T_J		TL75_L_C	0	125	°C
		TL75_L_Q	−40	125	
		TL751L_M	−55	125	

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL750L05, TL751L05, and TL751L05M electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	4.80	5	5.2	V
		T_J = $T_J$min to 125°C	4.75		5.25	
Input regulation	V_I = 9 V to 16 V			5	10	mV
	V_I = 6 V to 26 V			6	30	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		60*	65		dB
Output regulation	I_O = 5 mA to 150 mA			20	50	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 6 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	

TL750L08 and TL751L08 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
		T_J = $T_J$min to 125°C	7.6		8.4	
Input regulation	V_I = 10 V to 17 V			10	20	mV
	V_I = 9 V to 26 V			25	50	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		60*	65		dB
Output regulation	I_O = 5 mA to 150 mA			40	80	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 9 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

‡ Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω across the output.

TL750L10 and TL751L10 electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = $T_J$min to 125°C	9.5		10.5	
Input regulation	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60*	65		dB
Output regulation	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	

TL750L12, TL751L12, and TL751L12M electrical characteristics at 25°C virtual junction temperature, V_I = 14 V, I_O = 10 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = $T_J$min to 125°C	11.4		12.6	
Input regulation	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50*	55		dB
Output regulation	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		μV
Bias current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA,	T_J = $T_J$min to 125°C		1	2	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Pulse-testing techniques are used to maintain the junction temperature as closes to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 1 Ω across the output.

TYPICAL CHARACTERISTICS

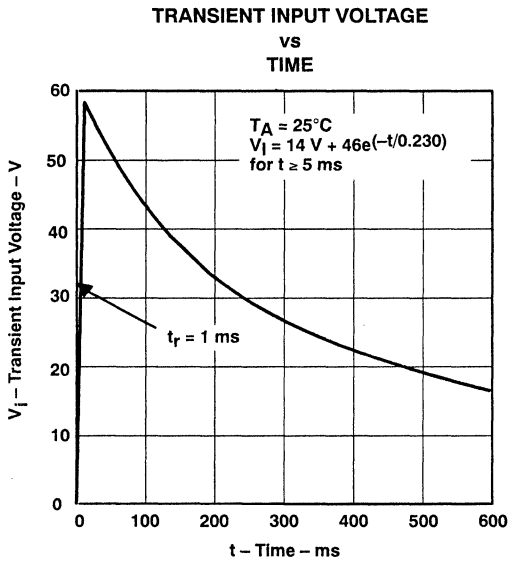
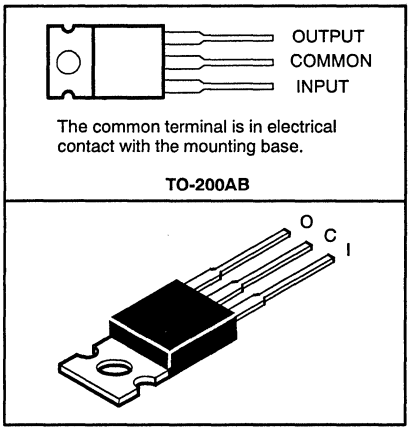


Figure 1

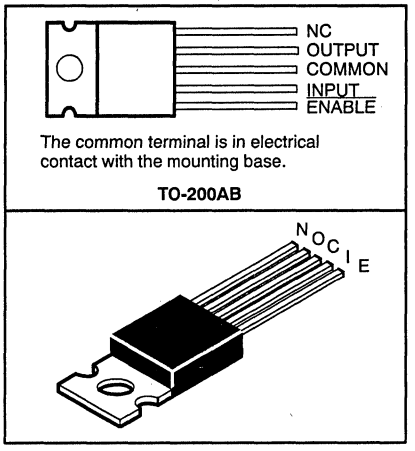
D3017, JANUARY 1988–REVISED SEPTEMBER 1990

- **Very Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **60-V Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Overcurrent Limiting Circuitry**

3-LEAD KC PACKAGE
(TOP VIEW)



5-LEAD KC PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M incorporate on-board overvoltage and current-limit protection circuitry to protect both themselves and the regulated system. Both series are fully protected against 60-V load-dump and reverse battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options available in 3-lead KC (TO-220AB) plastic packages.

The TL751M series of fixed-output voltage regulators also offer 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input gives the designer complete control over power-up, allowing sequential power up or emergency shutdown. When taken high, the enable input places the regulator output in a high-impedance state. It is completely TTL- and CMOS-compatible. The TL751M series is offered in 5-lead KC plastic packages.

The TL750M_C and TL751M_C are characterized for operation from 0°C to 125°C virtual junction temperature, and the TL750M_Q and TL751M_Q series are characterized for operation from −40°C to 125°C virtual junction temperature.

absolute maximum ratings over virtual junction temperature range (unless otherwise noted)

Continuous input voltage ..... 26 V
Transient input voltage (see Figure 1) ..... 60 V
Continuous reverse input voltage ..... −15 V
Transient reverse input voltage: t = 100 ms ..... −50 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 2 W
Continuous total dissipation at (or below) 40°C case temperature (see Note 1) ..... 20 W
Operating free-air, case, or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: For operation above T_A = 25°C and T_C = 40°C, refer to Figures 2 and 3. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions over recommended virtual junction temperature range (unless otherwise noted)

	DEVICE	MIN	MAX	UNIT
Input voltage range, V_I	TL75_M05	6	26	V
	TL75_M08	9	26	
	TL75_M10	11	26	
	TL75_M12	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}	TL751M_	2	15	V
Low-level $\overline{\text{ENABLE}}$ input voltage, V_{IL}	TL751M_	0	0.8	
Output current range, I_O	TL75_M		750	mA
Operating virtual junction temperature range, T_J	TL75_M_C	0	125	°C
	TL75_M_Q	−40	125	

TL750M05 and TL751M05 electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M05, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 750 mA	T_J = 25°C	4.95	5	5.05	V
		T_J = MIN to MAX†	4.9		5.1	
Input regulation	V_I = 9 V to 16 V, I_O = 250 mA			10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA			12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		50	55		dB
Output regulation	I_O = 5 mA to 750 mA			20	50	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL750M08 and TL751M08 electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M08, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 750 mA	T_J = 25°C	7.92	8	8.08	V
		T_J = MIN to MAX†	7.84		8.16	
Input regulation	V_I = 10 V to 17 V, I_O = 250 mA			12	40	mV
	V_I = 9 V to 26 V, I_O = 250 mA			15	68	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		50	55		dB
Output regulation	I_O = 5 mA to 750 mA			24	80	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	μA

TL750M10 and TL751M10 electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M10, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 750 mA	T_J = 25°C	9.9	10	10.1	V
		T_J = MIN to MAX†	9.8		10.2	
Input regulation	V_I = 12 V to 18 V, I_O = 250 mA			15	43	mV
	V_I = 11 V to 26 V, I_O = 250 mA			20	75	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation	I_O = 5 mA to 750 mA			30	100	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL750M12 and TL751M12 electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS (see Note 2)		MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 750 mA	T_J = 25°C	11.88	12	12.12	V
		T_J = MIN to MAX†	11.76		12.24	
Input regulation	V_I = 14 V to 19 V, I_O = 250 mA			15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA			20	78	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation	I_O = 5 mA to 750 mA			30	120	mV
Dropout voltage	I_O = 500 mA				0.5	V
	I_O = 750 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			1000		μV
Bias current	I_O = 750 mA			60	75	mA
	I_O = 10 mA				5	
Bias current	$\overline{\text{ENABLE}}$ V_{IH} ≥ 2 V				200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 4.

TL751Mxx electrical characteristics, V_I = 14 V, I_O = 300 mA, T_J = 25°C

	MIN	TYP	MAX	UNIT
Response time, $\overline{\text{ENABLE}}$ to output		50		μs

TYPICAL CHARACTERISTICS

TRANSIENT INPUT VOLTAGE vs TIME

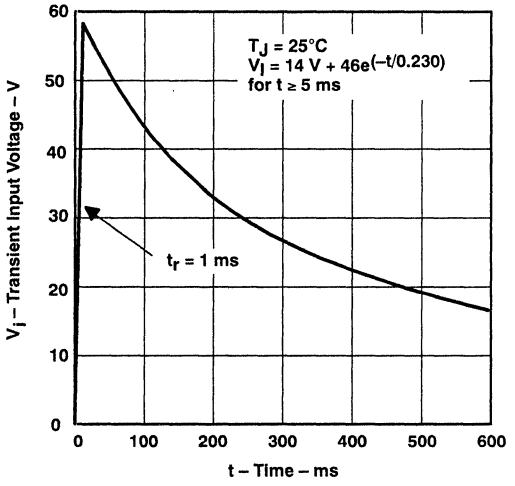


Figure 1

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

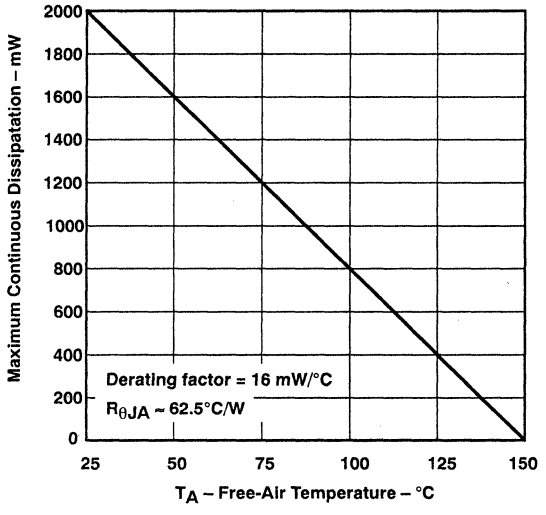


Figure 2

CASE TEMPERATURE DISSIPATION DERATING CURVE

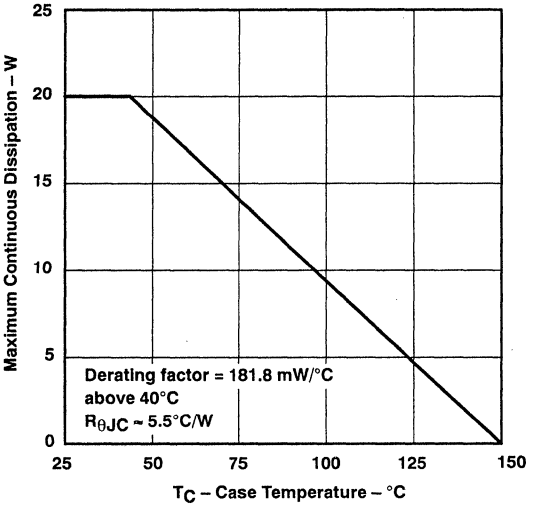


Figure 3

PARAMETER MEASUREMENT INFORMATION

The TL751MXX is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 4 and 5 can be used to establish the capacitance value and ESR range for best regulator performance.

Figure 4 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output. This figure shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit. For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 5 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 μF and a maximum ESR limit of 2 Ω. This figure is used to establish the amount that the minimum ESR limit shown in Figure 4 can be adjusted for different capacitor values. For example, if the minimum load needed is 200 mA, Figure 4 suggests an ESR range of 0.8 Ω to 2 Ω for 10 μF. Figure 5 shows that changing the capacitor from 10 μF to 400 μF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω, achieving an expanded ESR range by using a larger capacitor at the output.

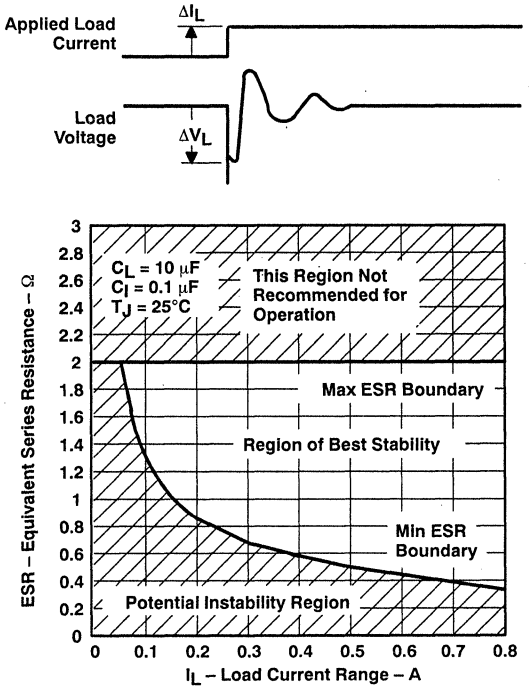


Figure 4. Output Capacitor ESR vs Load Current

PARAMETER MEASUREMENT INFORMATION

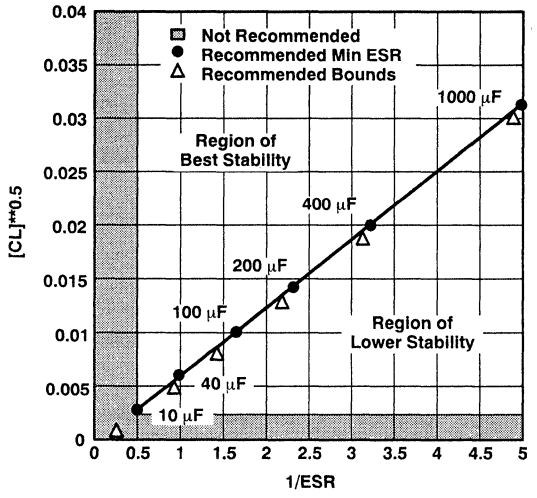


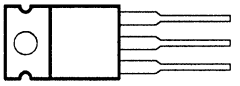
Figure 5. TL751M10 Stability vs ESR

D2643, APRIL 1981–REVISED AUGUST 1991

- **±1% Output Tolerance at 25°C**
- **±2% Output Tolerance Over Full Operating Range**
- **Thermal Shutdown**
- **Internal Short-Circuit Current Limiting**
- **Pinout Identical to uA7800 Series**
- **Improved Version of uA7800 Series**

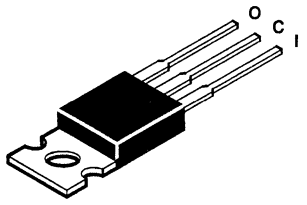
NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	TL780-05C
12 V	TL780-12C
15 V	TL780-15C

KC PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

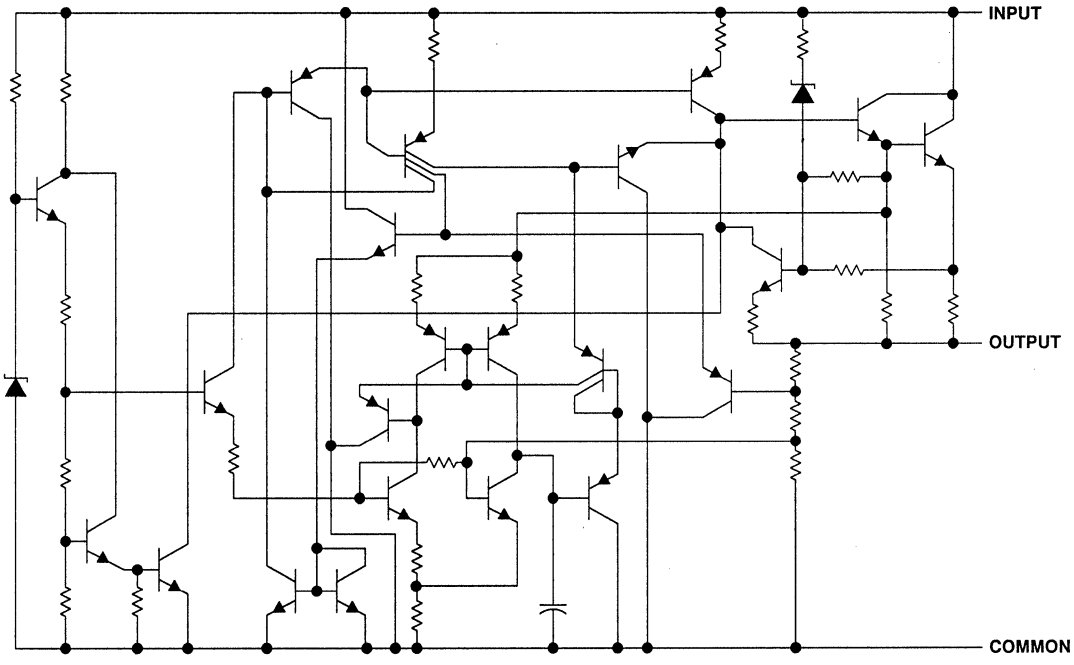
TO-200AB



description

Each fixed-voltage precision regulator in this series is capable of supplying 1.5 A of load current. A unique temperature-compensation technique coupled with an internally trimmed band-gap reference has resulted in improved accuracy when compared to other 3-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current limiting and thermal shutdown features make the devices essentially immune to overload.

schematic



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage	35 V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	15 W
Operating free-air, case, or virtual junction temperature range	0°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

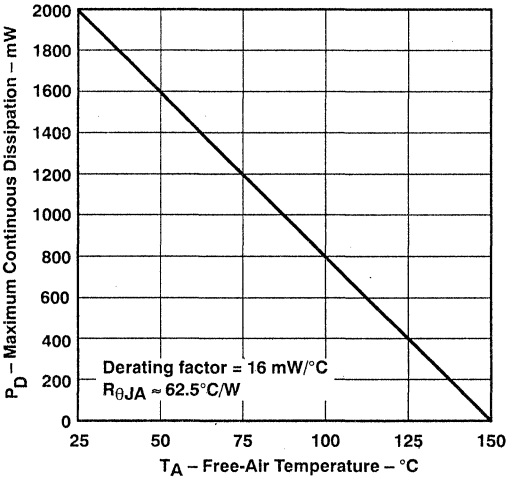


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

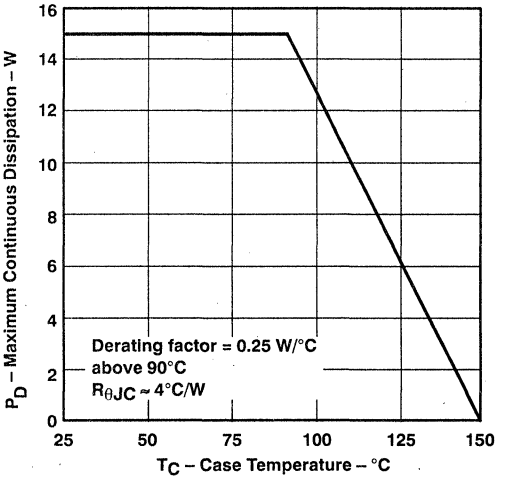


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	TL780-05C	7	25	V
	TL780-12C	14.5	30	
	TL780-15C	17.5	30	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

TL780-05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,	25°C	4.95	5	5.05	V
	V_I = 7 V to 20 V	0°C to 125°C	4.9		5.1	
Input regulation	V_I = 7 V to 25 V	25°C		0.5	5	mV
	V_I = 8 V to 12 V			0.5	5	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	70	85		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		4	25	mV
	I_O = 250 mA to 750 mA			1.5	15	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C		0.7	1.3	mA
	I_O = 5 mA to 1 A			0.003	0.5	
Short-circuit output current	V_I = 35 V	25°C		750		mA
Peak output current		25°C		2.2		A

TL780-12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W,	25°C	11.88	12	12.12	V
	V_I = 14.5 V to 27 V	0°C to 125°C	11.76		12.24	
Input regulation	V_I = 14.5 V to 30 V	25°C		1.2	12	mV
	V_I = 16 V to 22 V			1.2	12	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	65	80		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		6.5	60	mV
	I_O = 250 mA to 750 mA			2.5	36	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		180		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current	V_I = 35 V	25°C		350		mA
Peak output current		25°C		2.2		A

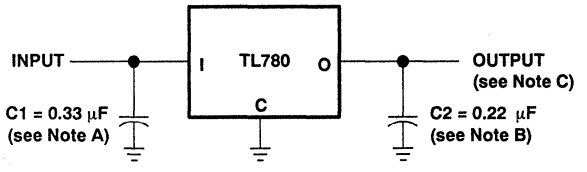
† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

TL780-15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 17.5 V to 30 V	25°C	14.85	15	15.15	V
		0°C to 125°C	14.7		15.3	
Input regulation	V_I = 17.5 V to 30 V	25°C		1.5	15	mV
	V_I = 20 V to 26 V			1.5	15	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	60	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		7	75	mV
	I_O = 250 mA to 750 mA			2.5	45	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		225		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		5.5	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.02	0.5	
Short-circuit output current	V_I = 35 V	25°C		230		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.22-μF capacitor across the output.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C1 is required if the regulator is far from the power supply filter.
B. C2 is not required for stability; however, transient response is improved.
C. Permanent damage can occur if output is pulled below ground.

Figure 3. Test Circuit

APPLICATION INFORMATION

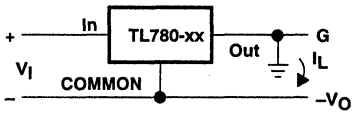
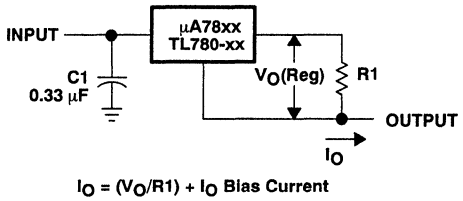


Figure 4. Positive Regulator in Negative Configuration (V_I Must Float)



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 5. Current Regulator

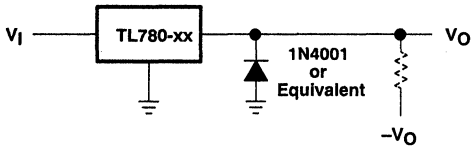


Figure 6. Output Polarity Reversal Protection Circuit

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., op amps, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

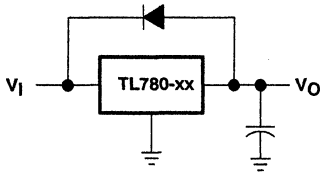


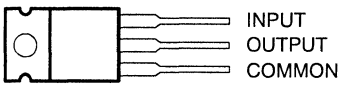
Figure 7. Reverse-Bias Protection Circuit

reverse-bias protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 7.

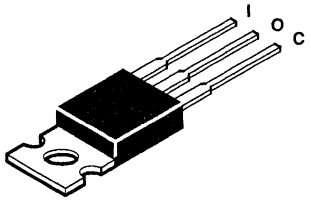
- **Overvoltage Protection**
- **Thermal Shutdown Protection**
- **Internal Short-Circuit Current Limiting**
- **Peak Output Current Constant Over Temperature Range**
- **TL782Q Has Extended Temperature Range of −40°C to 125°C**

KC PACKAGE
(TOP VIEW)



The common terminal is in electrical contact with the mounting base.

TO-220AB



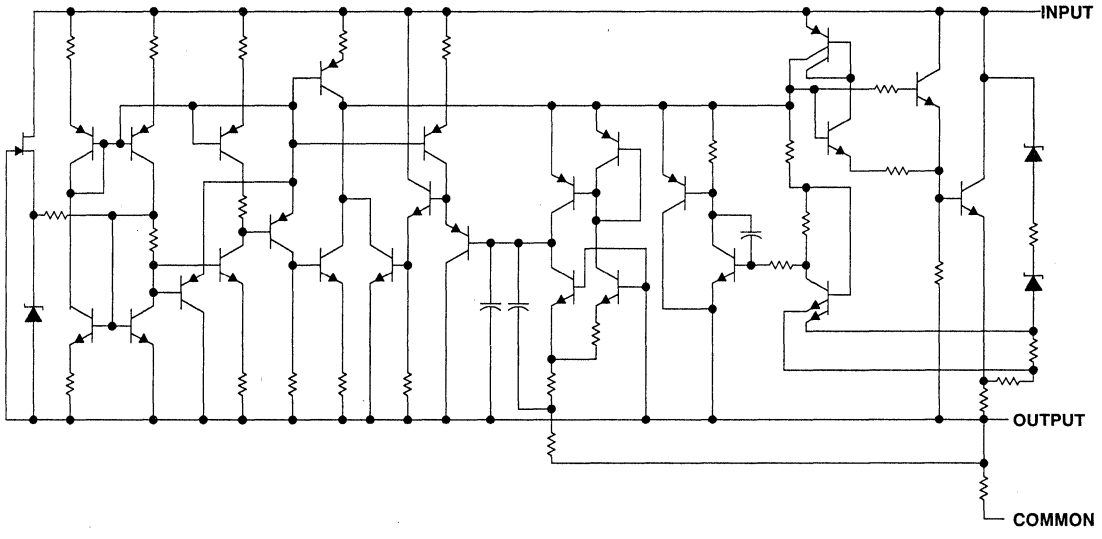
description

The TL782C and the TL782Q are fixed 2-V positive voltage regulators designed to address industry needs. With superior input and output regulation, they can regulate input voltages of 4.5 V to 30 V and are capable of supplying up to 1.5 A of load current.

In addition to high performance, the TL782C and TL782Q feature on-board overvoltage and thermal overload protection circuitry, and the output is current-limit protected.

The TL782C is characterized for operation from 0°C to 125°C virtual temperature range. The TL782Q is characterized for operation from −40°C to 125°C virtual temperature range.

schematic



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage ..... 40 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 2 W
Continuous total dissipation at (or below) 70°C case temperature (see Note 1) ..... 20 W
Operating free-air, case, or virtual junction temperature range: TL782C ..... 0°C to 125°C
TL782Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: For operation above 25°C free-air or 70°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

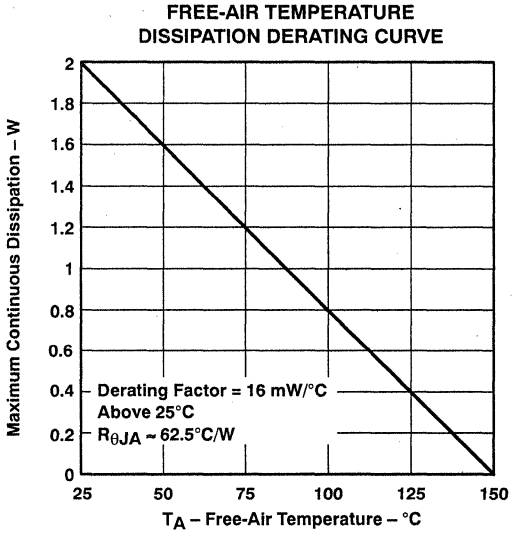


Figure 1

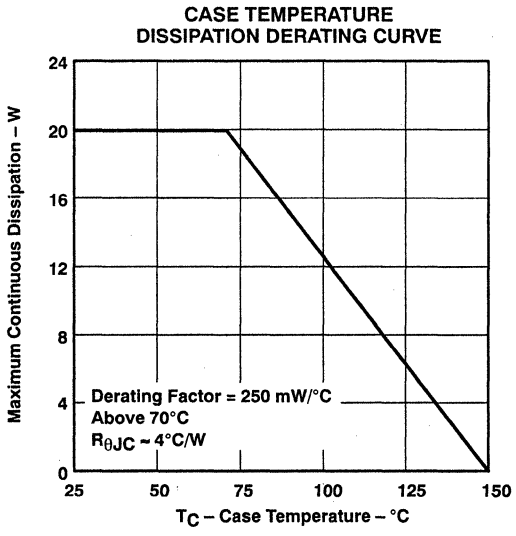


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		4.5	30	V
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J	TL782C	0	125	°C
	TL782Q	−40	125	

electrical characteristics at specified virtual junction temperature, V_I = 5 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J‡	MIN	TYP	MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, $P_D \leq$ 15 W,	25°C	1.94	2	2.06	V
	V_I = 4.5 V to 30 V	Full range	1.9		2.1	
Input regulation	V_I = 5 V to 20 V	25°C			25	mV
	V_I = 8 V to 12 V				15	
	V_I = 5 V to 20 V	Full range			35	
	V_I = 8 V to 12 V				25	
Ripple rejection	$V_{I(AV)}$ = 10 V, V_{PP} = 10 V, f = 120 Hz	25°C	60			dB
Output regulation	I_O = 5 mA to 1.5 A	25°C			25	mV
	I_O = 250 mA to 750 mA				15	
	I_O = 5 mA to 1.5 A	Full range			70	
	I_O = 250 mA to 750 mA				35	
Temperature coefficient of output voltage	I_O = 5 mA	Full range		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Bias current		25°C		8	9	mA
		Full range			10	
Bias current change	V_I = 5 V to 20 V	Full range			1.4	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current	V_I = 2.5 V	25°C		750		mA
Peak output current		25°C		2.2		A

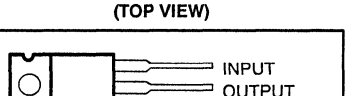
† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the free-air temperature as possible. All characteristics are measured with a 0.33-μF capacitor across the input and a 1-μF capacitor across the output.

‡ For the TL782C, full range is 0°C to 125°C, and for the TL782Q, full range is −40°C to 125°C.

D2659, SEPTEMBER 1981–REVISED DECEMBER 1991

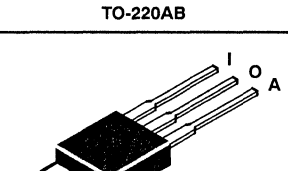
- **Output Adjustable From 1.25 V to 125 V, When Used With an External Resistor Divider**
- **700-mA Output Current**
- **Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection**
- **0.001%/V Typical Input Regulation**
- **0.15% Typical Output Regulation**
- **76-dB Typical Ripple Rejection**
- **Standard TO-220AB Package**

KC PACKAGE
(TOP VIEW)



The output terminal is in electrical contact with the mounting base.

TO-220AB



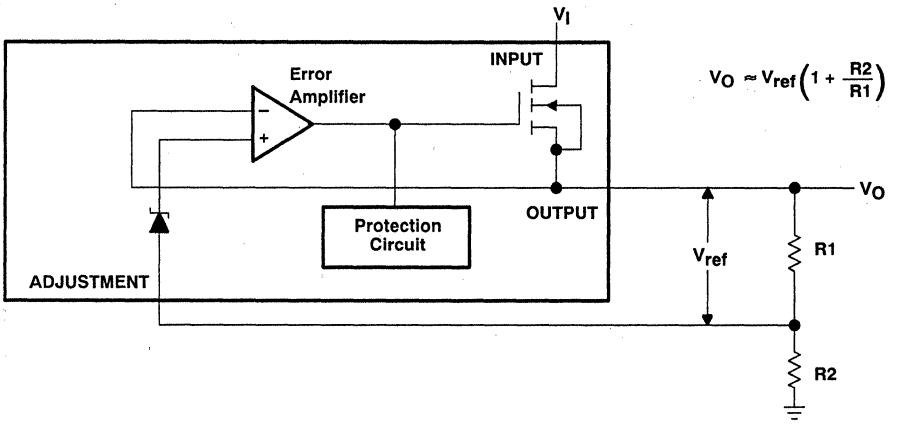
description

The TL783C is an adjustable 3-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783C combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs, the TL783C maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if the adjustment terminal is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, will improve transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$ ..... 125 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 2 W
Continuous total dissipation at (or below) 70°C case temperature (see Note 1) ..... 20 W
Operating free-air, case, or virtual junction temperature range ..... 0°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: For operation above 25°C free-air or 70°C case temperature, refer to Figures 1 and 2, respectively. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

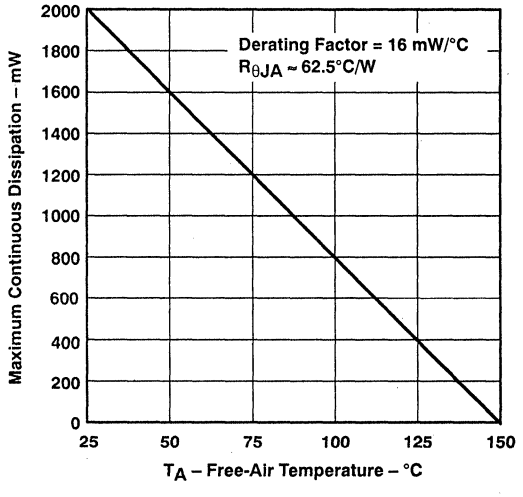


Figure 1

CASE TEMPERATURE DISSIPATION DERATING CURVE

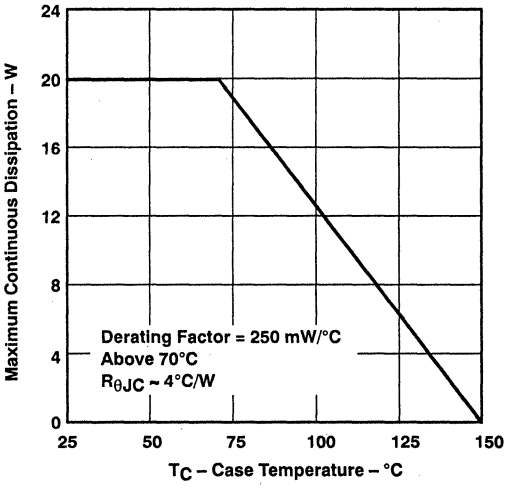


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics at $V_I - V_O = 25$ V, $I_O = 0.5$ A, $T_J = 0°C$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Input regulation‡	$V_I - V_O$ = 20 V to 125 V, P ≤ rated dissipation	T_J = 25°C		0.001	0.01	%/V
		T_J = 0°C to 125°C		0.004	0.02	
Ripple rejection	$\Delta V_{I(PP)}$ = 10 V, V_O = 10 V,	f = 120 Hz	66	76		dB
Output regulation	I_O = 15 mA to 700 mA, T_J = 25°C	V_O ≤ 5 V		7.5	25	mV
		V_O ≥ 5 V		0.15%	0.5%	
	I_O = 15 mA to 700 mA, P ≤ rated dissipation	V_O ≤ 5 V		20	70	mV
		V_O ≥ 5 V		0.3%	1.5%	
Output voltage change with temperature				0.4%		
Output voltage long-term drift	1000 hours at T_J = 125°C, $V_I - V_O$ = 125 V,	See Note 2		0.2%		
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C			0.003%		
Minimum output current to maintain regulation	$V_I - V_O$ = 125 V				15	mA
Peak output current	$V_I - V_O$ = 25 V, t = 1 ms			1100		mA
	$V_I - V_O$ = 15 V, t = 30 ms			715		
	$V_I - V_O$ = 25 V, t = 30 ms		700	900		
	$V_I - V_O$ = 125 V, t = 30 ms		100	250		
Adjustment-terminal current				83	110	μA
Change in adjustment-terminal current	$V_I - V_O$ = 15 V to 125 V, I_O = 15 mA to 700 mA, P ≤ rated dissipation			0.5	5	μA
Reference voltage (OUTPUT to ADJUSTMENT)	$V_I - V_O$ = 10 V to 125 V, I_O = 15 mA to 700 mA, P ≤ rated dissipation, See Note 3		1.2	1.27	1.3	V

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

NOTES: 2. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

3. Due to the dropout voltage and output current limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

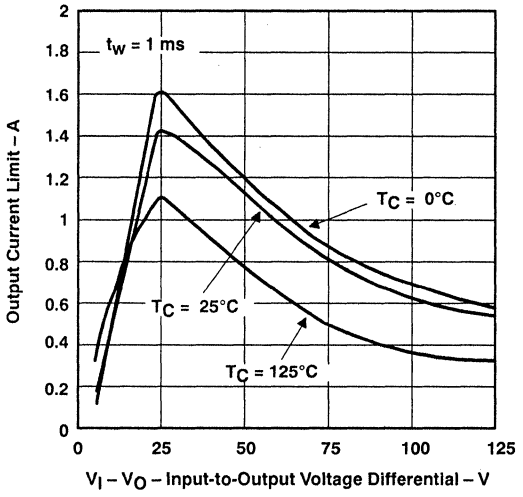


Figure 3

OUTPUT CURRENT LIMIT
vs
INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL

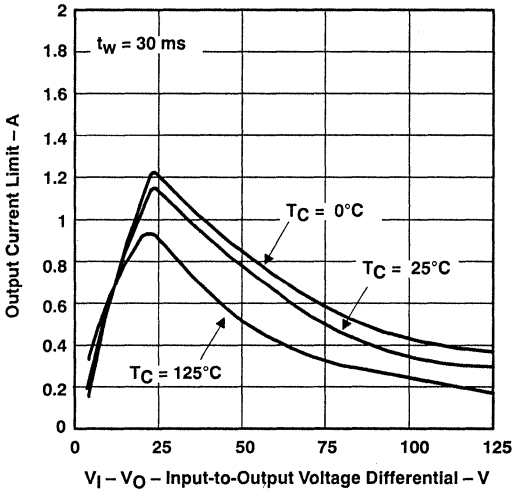


Figure 4

OUTPUT CURRENT LIMIT
vs
TIME

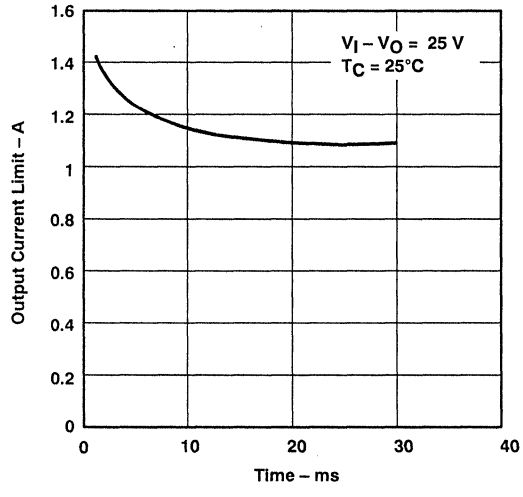


Figure 5

RIPPLE REJECTION
vs
OUTPUT VOLTAGE

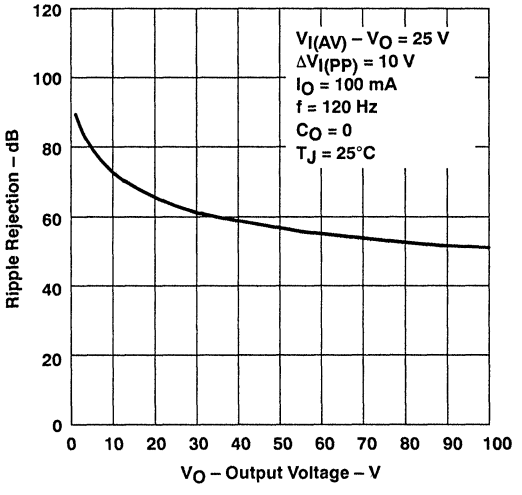


Figure 6

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
OUTPUT CURRENT

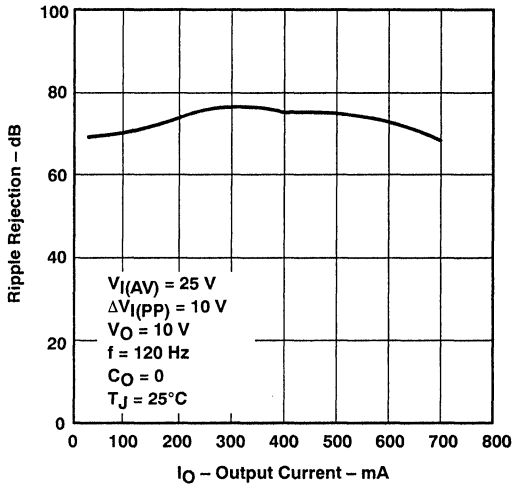


Figure 7

RIPPLE REJECTION
vs
FREQUENCY

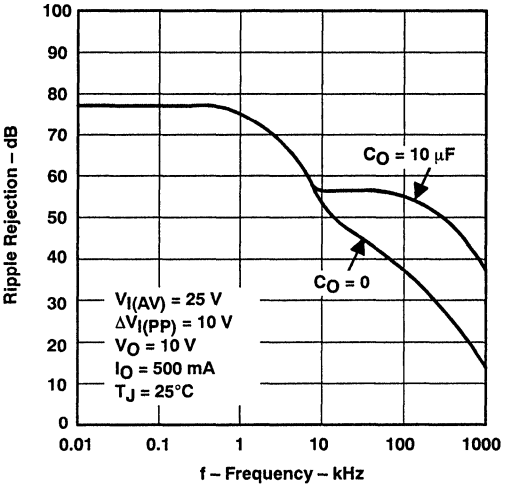


Figure 8

OUTPUT IMPEDANCE
vs
FREQUENCY

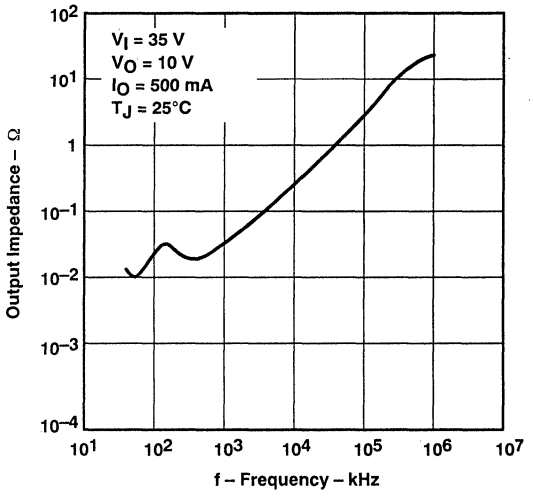


Figure 9

REFERENCE VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

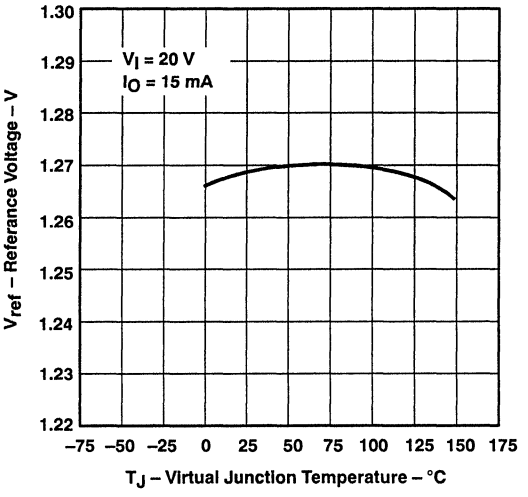


Figure 10

TYPICAL CHARACTERISTICS

ADJUSTMENT-TERMINAL CURRENT
vs
VIRTUAL JUNCTION TEMPERATURE

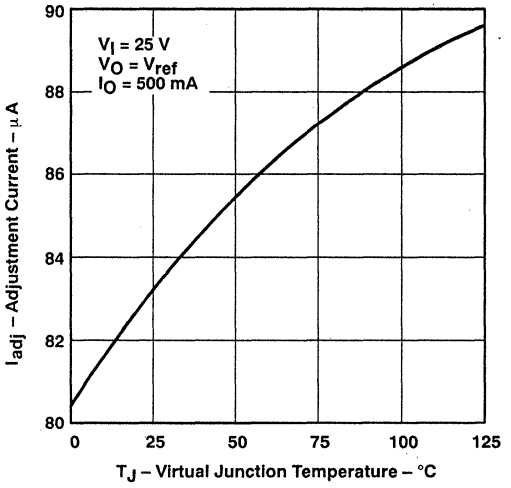


Figure 11

DROPOUT VOLTAGE
vs
VIRTUAL JUNCTION TEMPERATURE

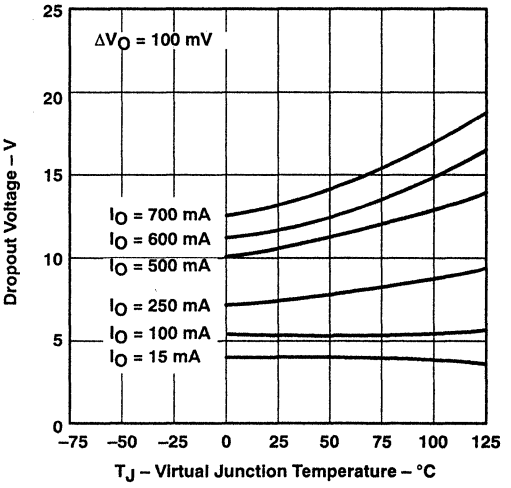


Figure 12

LOAD REGULATION
vs
VIRTUAL JUNCTION TEMPERATURE

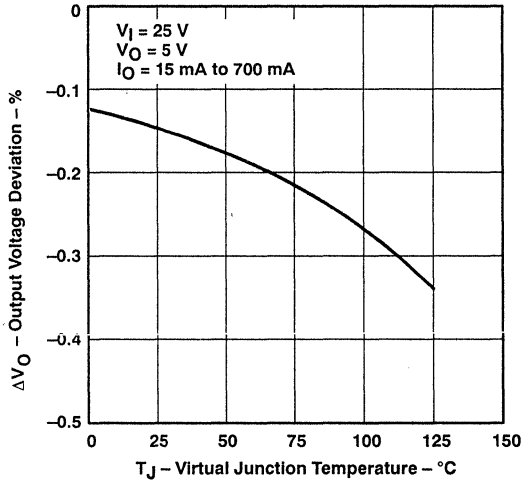


Figure 13

MINIMUM OUTPUT CURRENT
TO MAINTAIN REGULATION
vs
INPUT VOLTAGE

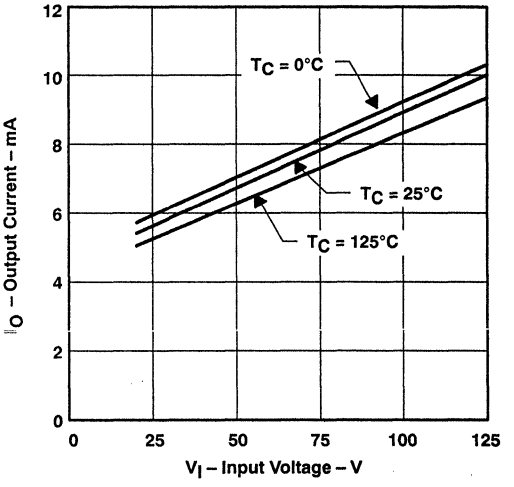


Figure 14

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

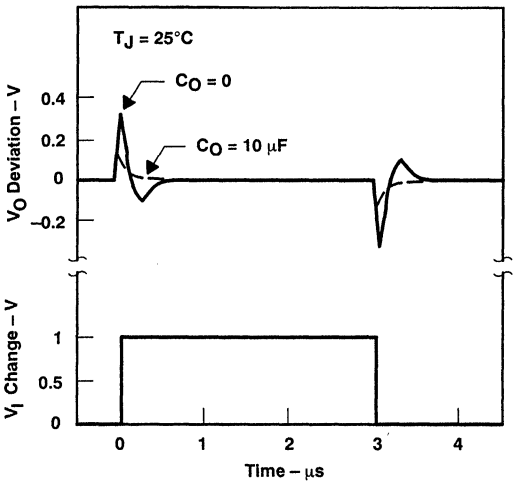


Figure 15

LOAD TRANSIENT RESPONSE

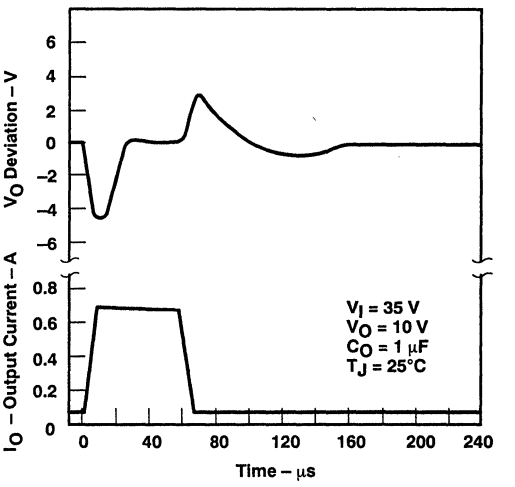


Figure 16

DESIGN CONSIDERATIONS

The internal reference (see functional block diagram) is used to generate 1.25 V nominal (V_{ref}) between the output and adjustment terminals. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R2/R1) + I_{adj} (R2)$$

or

$$V_O \sim V_{ref} (1 + R2/R1).$$

The TL783C was designed to minimize I_{adj} and maintain consistency over line and load variations, thereby minimizing the I_{adj} (R2) error term.

To maintain I_{adj} at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω will provide a minimum load current of 15 mA. Larger values may be used if the input-to-output differential voltage is less than 125 V (see minimum operating current curve) or if the load will sink some portion of the minimum current.

bypass capacitors

The TL783C regulator is stable without bypass capacitors; however, any regulator will become unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1-μF tantalum or electrolytic capacitor is usually sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783C because they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large load transient conditions. Addition of an output bypass capacitor will greatly enhance load transient response as well as prevent dropout. For most applications, it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_O\ (\mu F) = 15/V_O$$

Larger values will provide proportionally better transient response characteristics.

protection circuitry

The TL783C regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits are meant to protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783C will protect the device up to maximum-rated V_I as long as certain precautions are taken. If V_I is instantaneously switched on, transients exceeding maximum input ratings may occur, which can destroy the regulator. These are usually caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, if rise times in excess of 10 V/ns are applied to the input, a parasitic n-p-n transistor in parallel with the DMOS output can be turned on causing the device to fail. If the device is operated over 50 V and the input is switched on rather than ramped on, a low-Q capacitor, such as tantalum or electrolytic should be used rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015 or greater will usually provide adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, if an instantaneous short circuit is applied to the outputs, both ringing and excessive fall times can result. A tantalum or electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I. A protective diode (see Figure 17) is required only for capacitance values greater than:

$$C_O\ (\mu F) = 3 \times 10^4/(V_O)^2.$$

Care should always be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

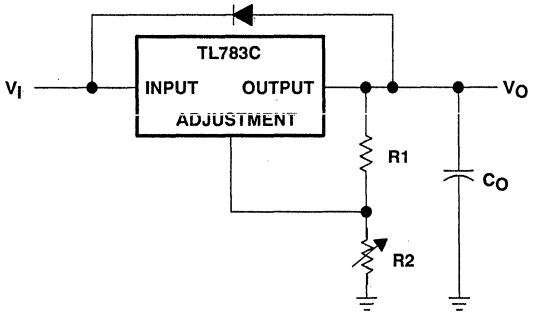


Figure 17. Regulator With Protective Diode

load regulation

The current set resistor (R1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R1 and R2 to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

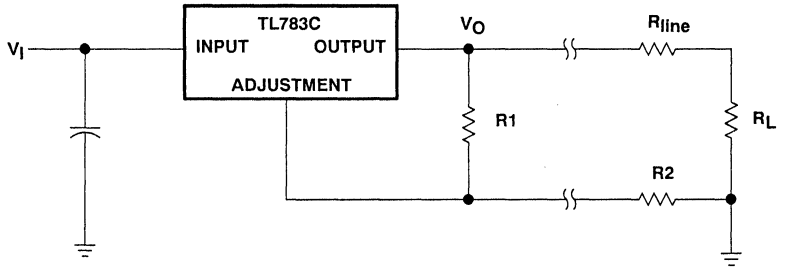
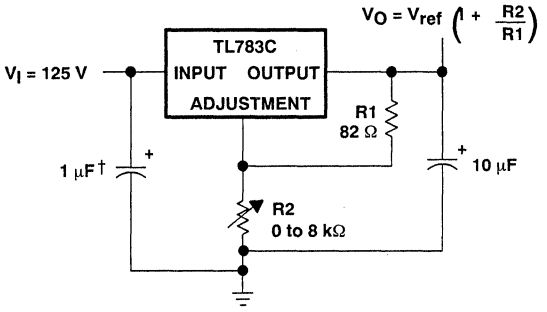


Figure 18. Regulator With Current-Set Resistor

APPLICATION INFORMATION



† Needed if device is more than 4 inches from filter capacitor

Figure 19. 1.25-V to 115-V Adjustable Regulator

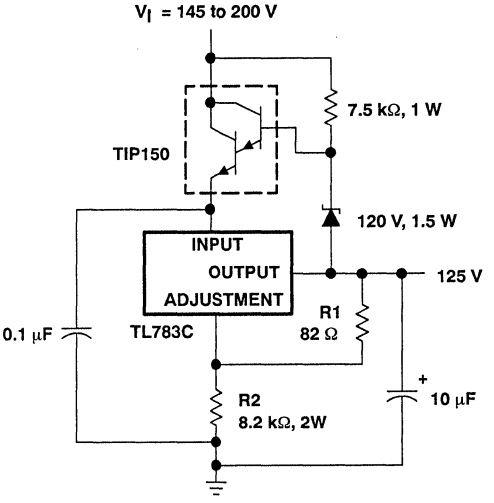


Figure 20. 125-V Short-Circuit-Protected Off-Line Regulator

APPLICATION INFORMATION

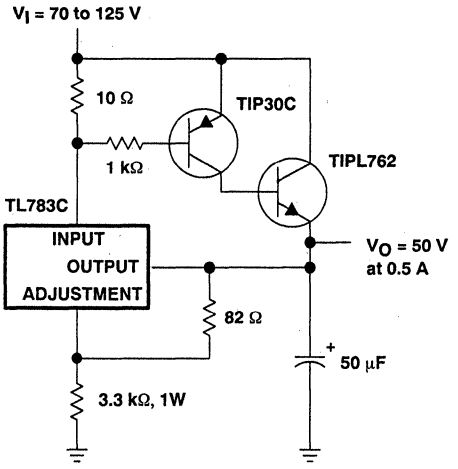


Figure 21. 50-V Regulator With Current Boost

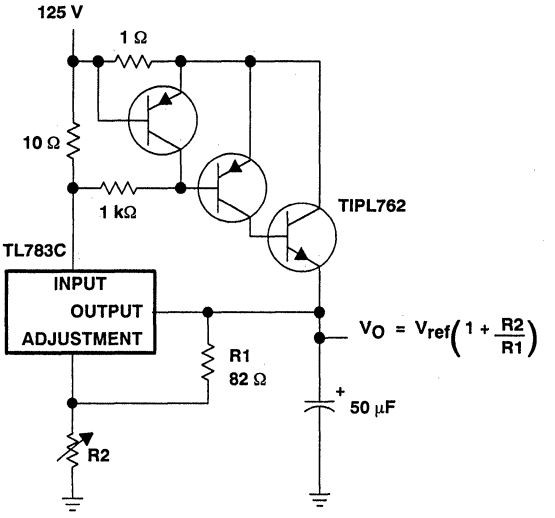


Figure 22. Adjustable Regulator With Current Boost and Current Limit

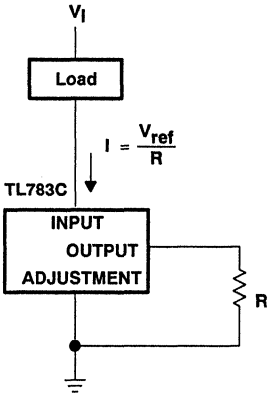


Figure 23. Current-Sinking Regulator

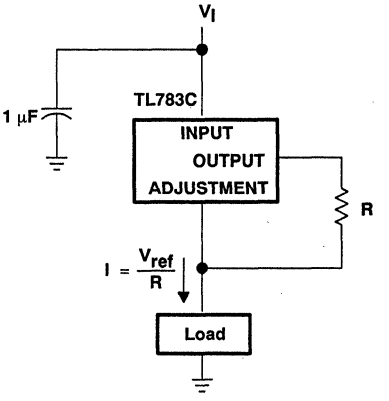


Figure 24. Current-Sourcing Regulator

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APPLICATION INFORMATION

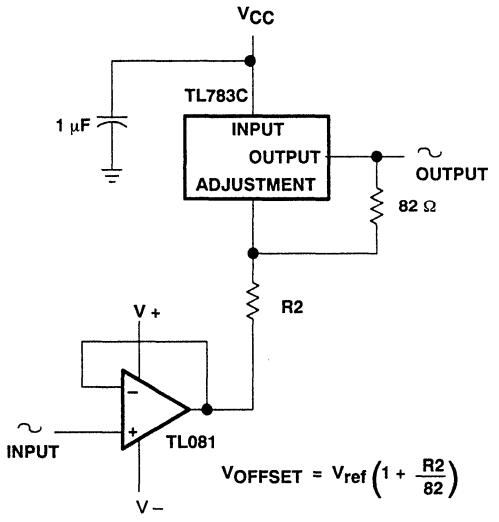


Figure 25. High-Voltage Unity-Gain Offset Amplifier

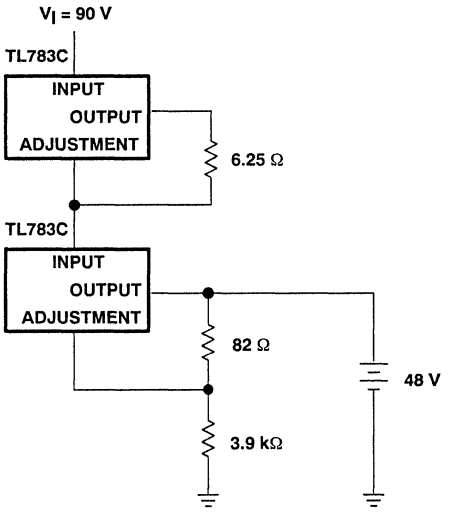
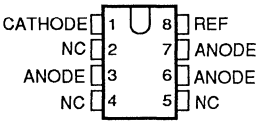


Figure 26. 48-V, 200-mA Float Charger

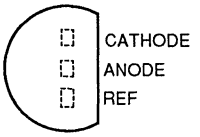
D3858, DECEMBER 1991

- 0.4% Initial Voltage Tolerance
- 0.1-Ω Typical Output Impedance
- Fast Turn-On . . . 500 ns
- Sink Current Capability . . . 1 mA to 100 mA
- Low Ref Pin Current
- Adjustable Output Voltage . . . V_{ref} to 36 V
- Available in a Wide Range of High Density Packaging Options:
  - Small Outline (D)
  - TO-226AA (LP)
  - SOT-89 (PK)

D PACKAGE
(TOP VIEW)

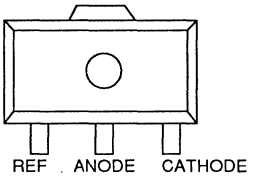


LP PACKAGE
(TOP VIEW)



NC – No internal connection

PK PACKAGE
(TOP VIEW)



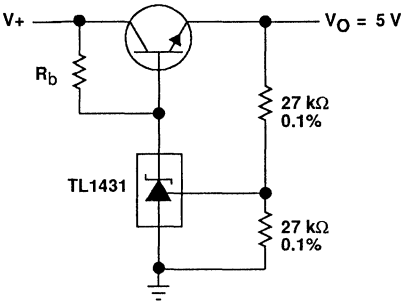
description

The TL1431 is a 3-terminal precision programable reference with specified thermal stability over applicable automotive and commercial temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 V) and 36 V with two external resistors (see Figure 16). These devices have a typical output impedance of 0.1 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes and other types of references in many applications like on-board regulation, adjustable power supplies, and switching power supplies.

The TL1431 is offered in a wide variety of high-density packaging options that includes an SOT-89-type package (suffix PK). It is also offered in both the automotive temperature range and the commercial temperature range. The TL1431Q is characterized for operation over the automotive temperature range of –40°C to 125°C. The TL1431C is characterized for operation over the commercial temperature range of 0°C to 70°C.

application schematic

Efficient 5-V Precision Regulator



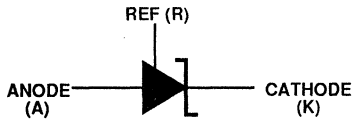
Note: R_b should provide ≥ 1 mA cathode current to the TL1431.

AVAILABLE OPTIONS

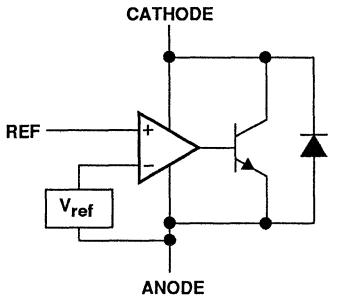
T_A	PACKAGE			CHIP FORM (Y)
	SMALL OUTLINE (D)	TO-226AA (LP)	SOT-89 (PK)	
0°C to 70°C	TL1431CD	TL1431CLP	TL1431CPK	TL1431Y
– 40°C to 125°C	TL1431QD	TL1431QLP	—	

D and LP packages are available taped and reeled. Add "R" suffix to device type (e.g., TL1431CDR). PK package is only available taped and reeled. No "R" suffix required. Chips are tested at 25°C.

symbol



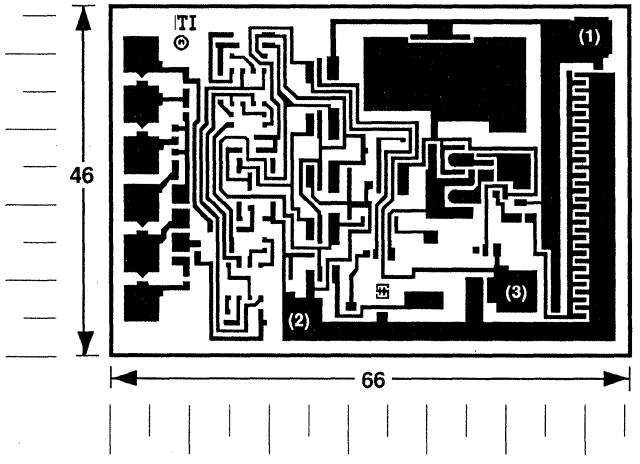
functional block diagram

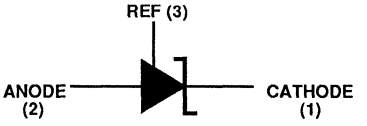


TL1431Y chip information

These chips, properly assembled, display characteristics similar to the TL1431 (see electrical table for TL1431Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Chip Thickness:
15 Typical

Bonding Pads:
4 X 4 Minimum

Tolerances ± 10%

All Dimensions Are In Mils

T_J max = 150°C

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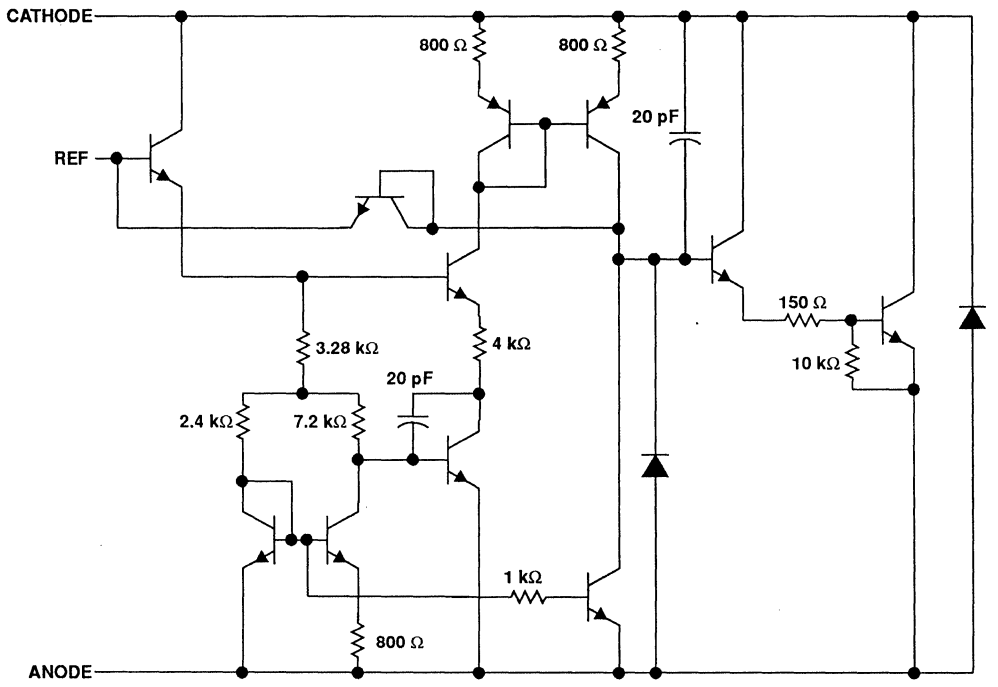
equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Cathode voltage (see Note 1) . . . . . 37 V
Continuous cathode current range . . . . . –100 mA to 150 mA
Reference input current range . . . . . –50 μA to 10 mA
Continuous power dissipation . . . . . See Dissipation Rating Tables 1 and 2
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
Q-suffix . . . . . –40°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the anode terminal unless otherwise noted.

TABLE 1. DISSIPATION RATING TABLE FREE-AIR TEMPERATURE

PACKAGE	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
D	5.8 mW/°C	725 mW	464 mW	261 mW	145 mW
LP	6.2 mW/°C	775 mW	496 mW	279 mW	155 mW
PK	4.0 mW/°C	500 mW	320 mW	180 mW	100 mW

TABLE 2. DISSIPATION RATING TABLE CASE TEMPERATURE

PACKAGE	DERATING FACTOR ABOVE T_C = 25°C	$T_C \leq 25°C$ POWER RATING	T_C = 70°C POWER RATING	T_C = 105°C POWER RATING	T_C = 125°C POWER RATING
PK	25 mW/°C	3125 mW	2000 mW	1125 mW	625 mW

recommended operating conditions

	C-SUFFIX		Q-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Cathode to anode voltage, V_{KA}	V_{ref}	36	V_{ref}	36	V
Cathode current, I_K	1	100	1	100	mA
Operating free-air temperature, T_A	0	70	– 40	125	°C

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electrical characteristics at specified free-air temperature, I_K = 10 mA (unless otherwise noted)

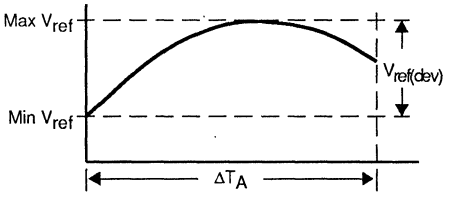
PARAMETER		TEST CONDITIONS	T_A	TEST CIRCUIT	TL1431C			TL1431Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	V_{KA} = V_{ref}	25°C	1	2490	2500	2510	2490	2500	2510	mV
			Full range		2480		2520	2470		2530	
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range	V_{KA} = V_{ref}	Full range	1		4	15		17	30	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	Full range	2		−1.1	−2		−1.1	−2	mV/V
I_{ref}	Reference input current	R1 = 10 kΩ, R2 = ∞	25°C	2		1.5	1.9		1.5	1.9	μA
			Full range				2.3			2.3	
$I_{ref(dev)}$	Deviation of reference input current over full temperature range	R1 = 10 kΩ, R2 = ∞	Full range	2		0.2	1.2		0.5	1.2	μA
I_{min}	Minimum cathode current for regulation	V_{KA} = V_{ref} to 36 V	25°C	1		0.45	1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, V_{ref} = 0	25°C	3		0.18	0.5		0.18	0.5	μA
			Full range				2			2	
$\lvert z_{ka} \rvert$	Output impedance§	V_{KA} = V_{ref}, f ≤ 1 kHz, I_K = 1 mA to 100 mA	25°C	1		0.1	0.2		0.1	0.2	Ω

† Full range is 0°C to 70°C for C-suffix devices and – 40°C to 125°C for Q-suffix devices.

The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage α_{Vref} is defined as:

$$|\alpha_{Vref}| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating temperature range of the device.



αV_{ref} can be positive or negative depending on whether miminum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature.

§ The output impedance is defined as: $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{ka}| \left(1 + \frac{R1}{R2}\right)$

electrical characteristics at 25°C free-air temperature, I_K = 10 mA

PARAMETER		TEST CONDITIONS	TEST CIRCUIT	TL1431Y			UNIT
				MIN	TYP	MAX	
V_{ref}	Reference input voltage	V_{KA} = V_{ref}	1	2490	2500	2510	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	ΔV_{KA} = 3 V to 36 V	2		−1.1	−2	mV/V
I_{ref}	Reference input current	R1 = 10 kΩ, R2 = ∞	2		1.44	1.9	μA
I_{min}	Minimum cathode current for regulation	V_{KA} = V_{ref} to 36 V	1		0.45	1	mA
I_{off}	Off-state cathode current	V_{KA} = 36 V, V_{ref} = 0	3		.18	0.5	μA
$\|z_{ka}\|$	Output impedance§	V_{KA} = V_{ref}, f ≤ 1 kHz, I_K = 1 mA to 100 mA	1		0.1	0.2	Ω

§The output impedance is defined as: $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$|z'| = \frac{\Delta V}{\Delta I}$, which is approximately equal to $|z_{ka}| \left(1 + \frac{R1}{R2}\right)$

PARAMETER MEASUREMENT INFORMATION

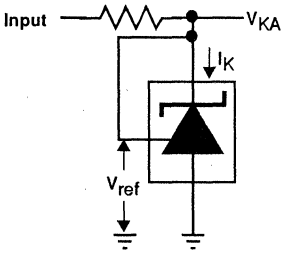


Figure 1. Test Circuit for V_{KA} = V_{ref}

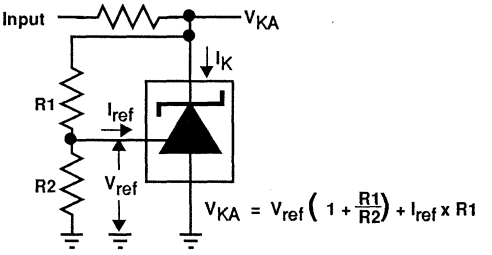


Figure 2. Test Circuit for V_{KA} > V_{ref}

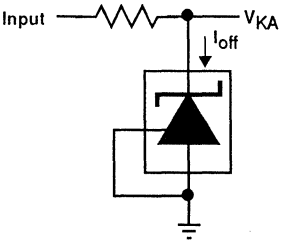


Figure 3. Test Circuit for I_{off}

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TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{ref}	Reference voltage	vs Temperature	4
I_{ref}	Reference current	vs Temperature	5
I_K	Cathode current	vs Cathode voltage	6 and 7
I_{off}	Off-state cathode current	vs Temperature	8
ΔV_{ref}	Ratio of delta reference voltage to delta cathode voltage	vs Temperature	9
V_n	Noise voltage	vs Frequency over a 10-second time-period	10 11
A_V	Voltage amplification	vs Frequency	12
$\lvert z_{ka} \rvert$	Reference impedance	vs Frequency	13
	Pulse response		14
	Stability boundary conditions		15

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TYPICAL CHARACTERISTICS†

REFERENCE VOLTAGE
vs
FREE-AIR TEMPERATURE

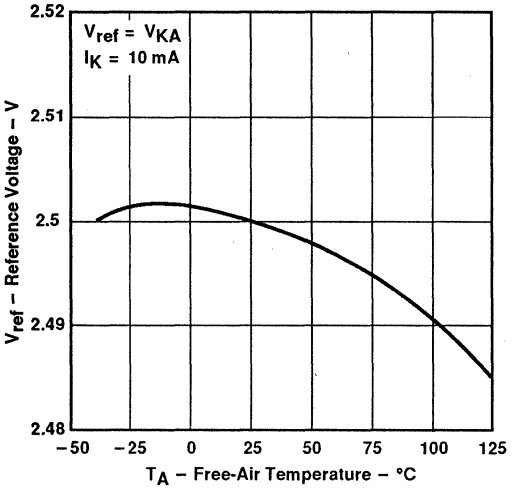


Figure 4

REFERENCE CURRENT
vs
FREE-AIR TEMPERATURE

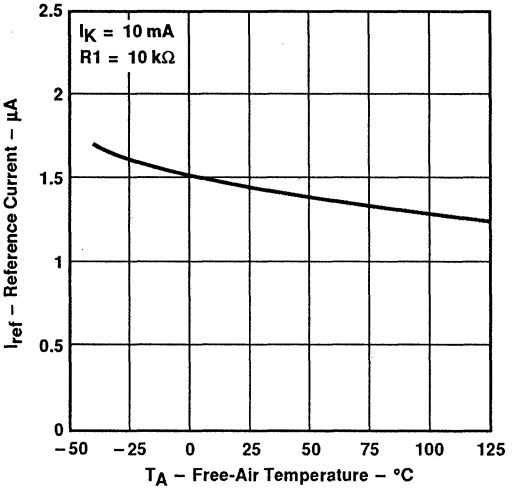


Figure 5

CATHODE CURRENT
vs
CATHODE VOLTAGE

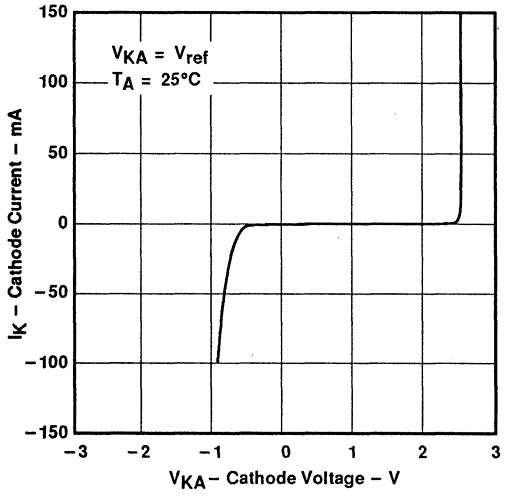


Figure 6

CATHODE CURRENT
vs
CATHODE VOLTAGE

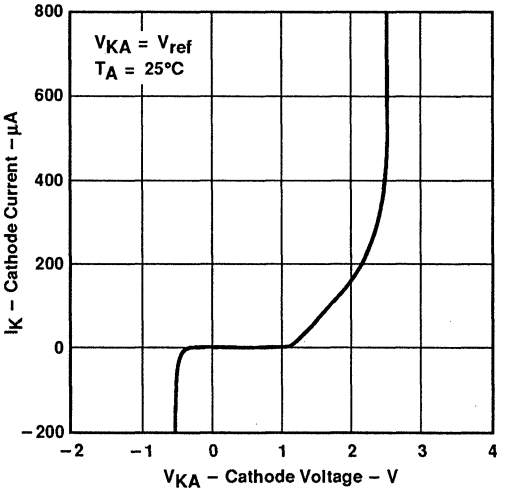


Figure 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OFF-STATE CATHODE CURRENT
vs
FREE-AIR TEMPERATURE

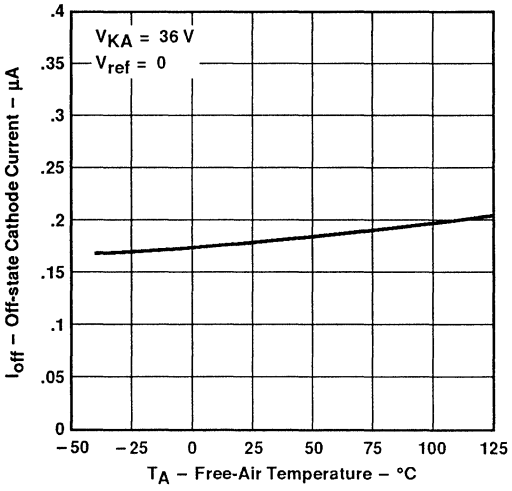


Figure 8

RATIO OF DELTA REFERENCE VOLTAGE TO
DELTA CATHODE VOLTAGE
vs
FREE-AIR TEMPERATURE

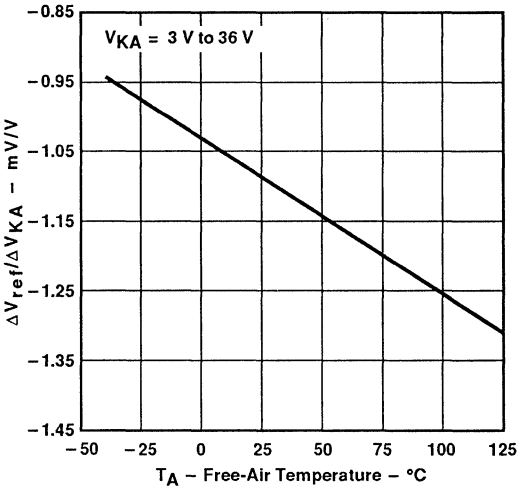


Figure 9

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

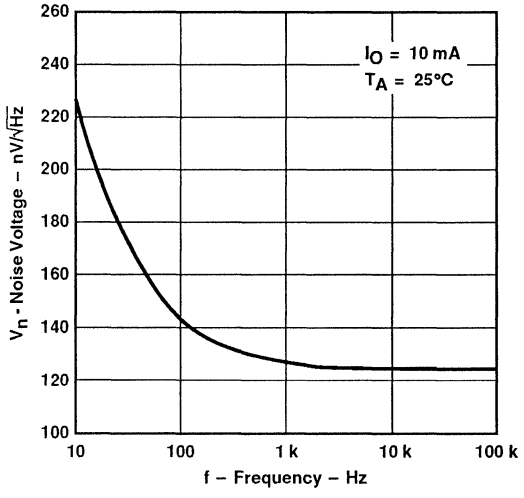
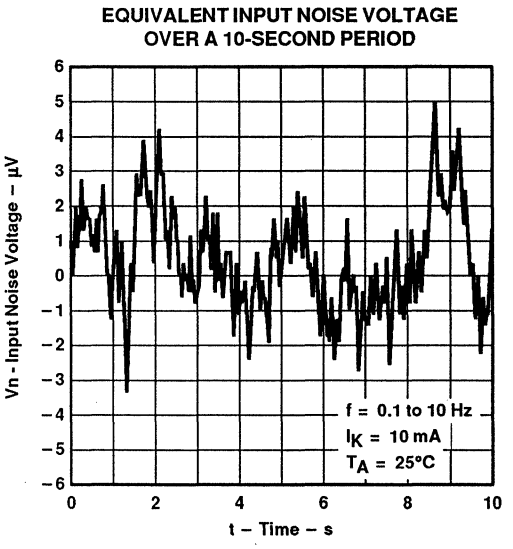
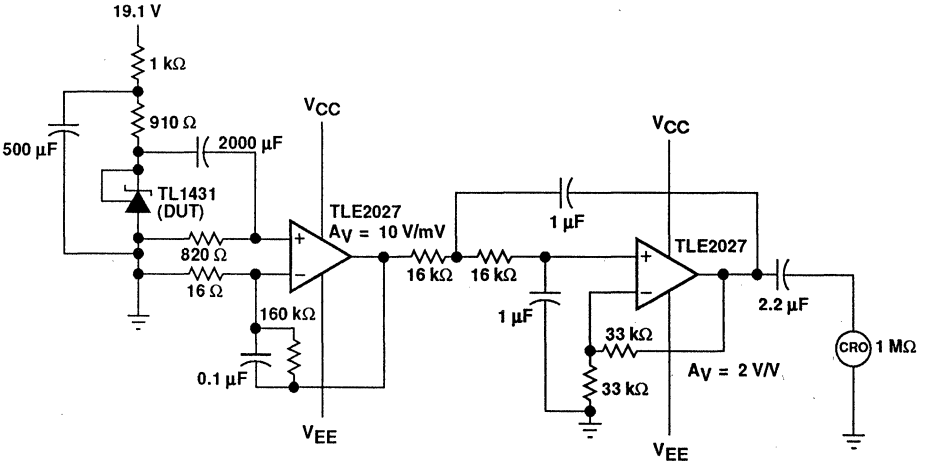


Figure 10

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



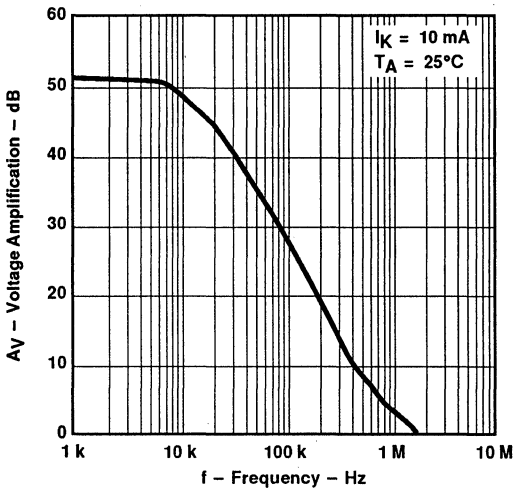


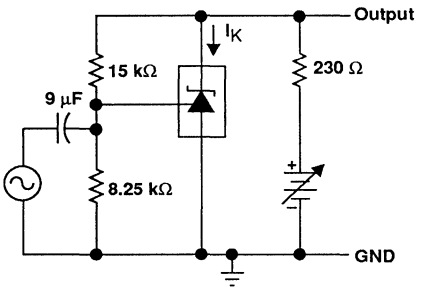
Test Circuit for 0.1-Hz to 10-Hz Equivalent Input Noise Voltage

Figure 11

TYPICAL CHARACTERISTICS

SMALL-SIGNAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

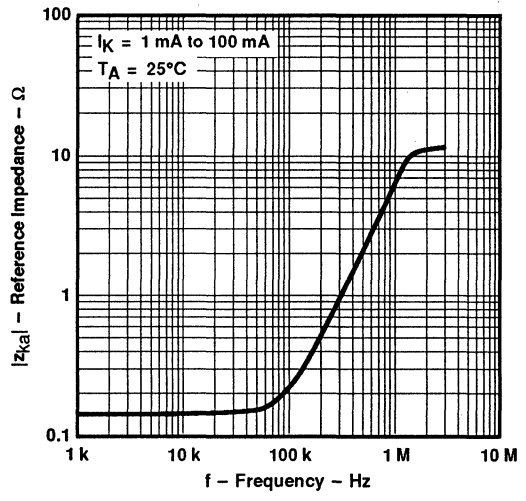


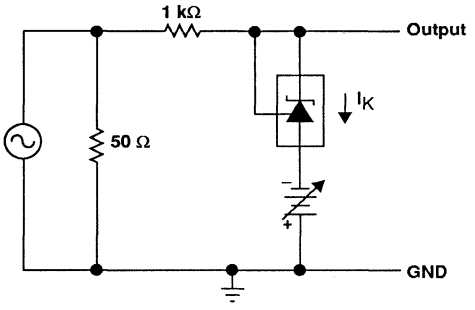


Test Circuit for Voltage Amplification

Figure 12

REFERENCE IMPEDANCE
vs
FREQUENCY

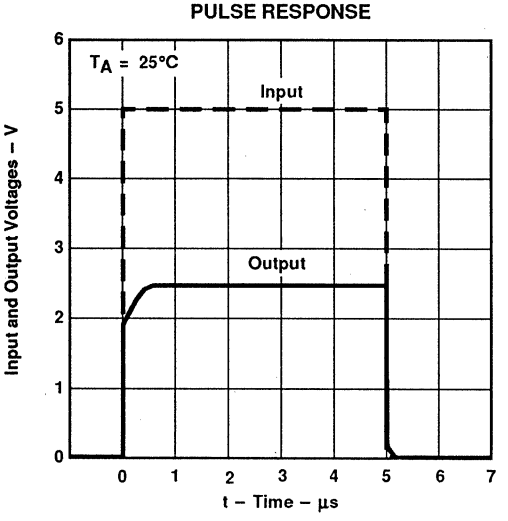


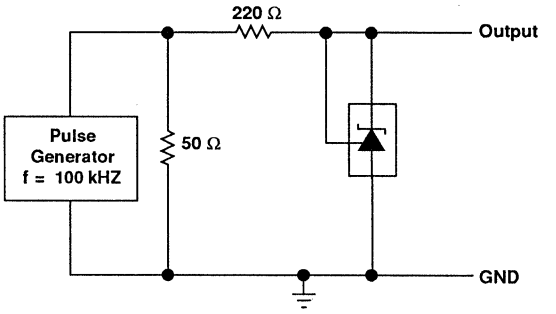


Test Circuit for Reference Impedance

Figure 13

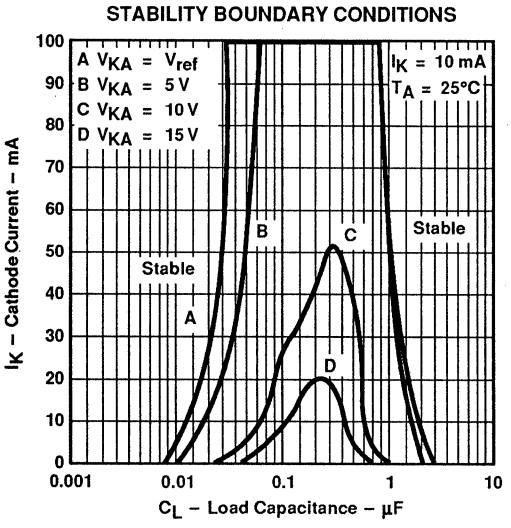
TYPICAL CHARACTERISTICS

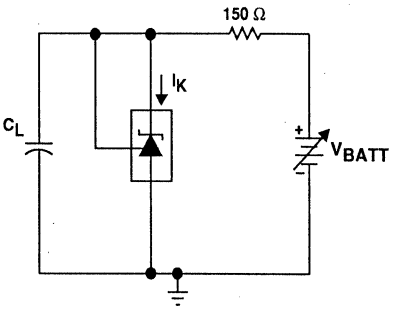




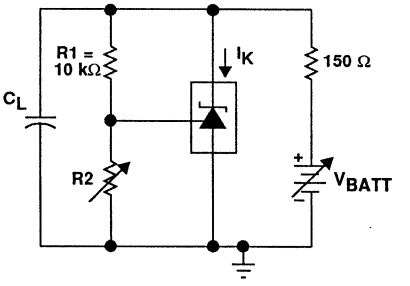
Test Circuit for Pulse Response

Figure 14





Test Circuit for Curve A



Test Circuit for Curves B, C, and D

†The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{BATT} and C_L were then adjusted to determine the ranges of stability.

Figure 15

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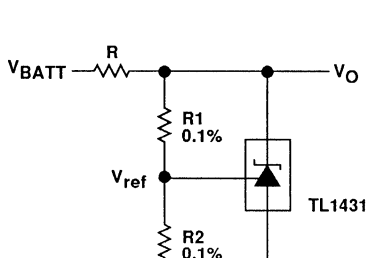
APPLICATION INFORMATION



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

NOTE: R should provide ≥ 1-mA cathode current to the TL1431 at minimum V_{BATT}.

Figure 16. Shunt Regulator

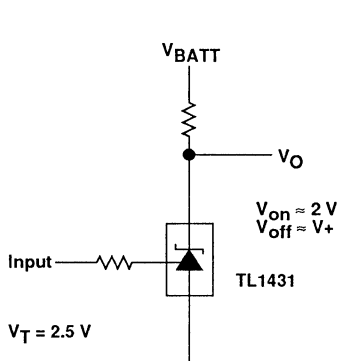
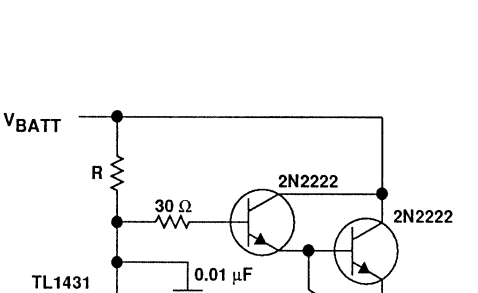


Figure 17. Single-Supply Comparator With Temperature-Compensated Threshold



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

NOTE: R should provide ≥ 1-mA cathode current to the TL1431 at minimum V_{BATT}.

Figure 18. Precision High-Current Series Regulator

APPLICATION INFORMATION

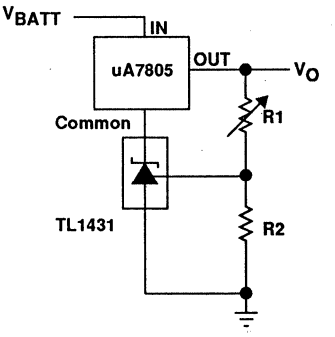


Figure 19. Output Control of a 3-Terminal Fixed Regulator

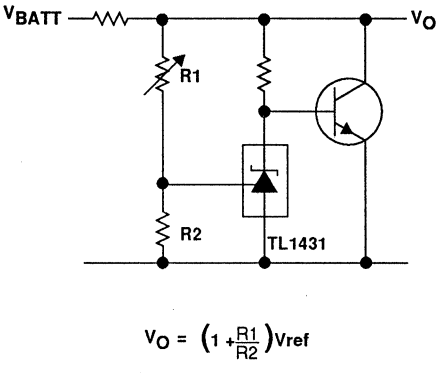
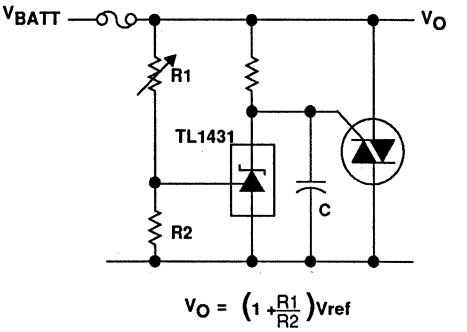


Figure 20. Higher-Current Shunt Regulator



Note: Refer to the stability boundary conditions on Figure 15 to determine allowable values for the capacitor.

Figure 21. Crowbar

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APPLICATION INFORMATION

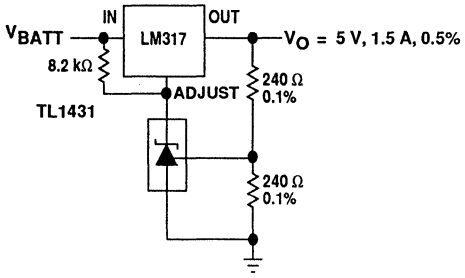
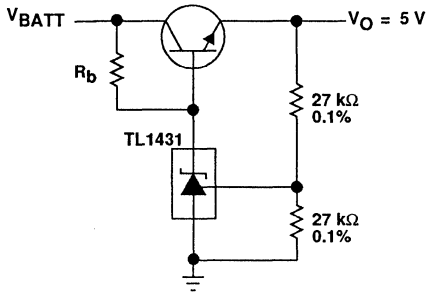


Figure 22. Precision 5-V, 1.5-A, 0.5% Regulator



Note: R_b should provide ≥ 1-mA cathode current to the TL1431.

Figure 23. Efficient 5-V, Precision Regulator

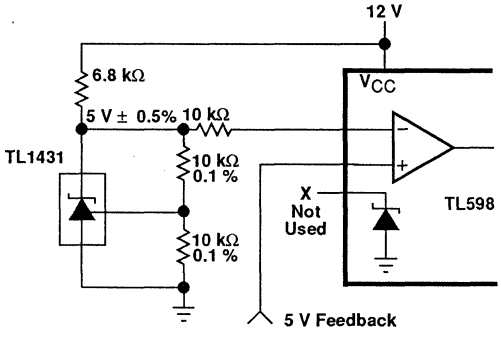
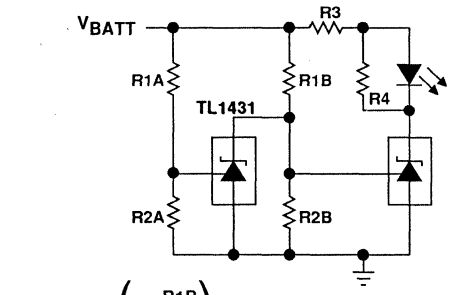


Figure 24. PWM Down Converter With 0.5% Reference

APPLICATION INFORMATION



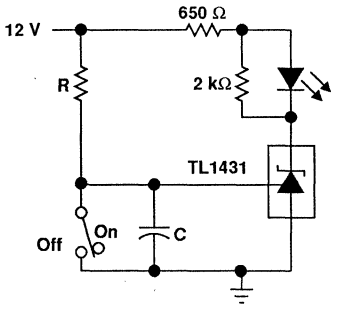
$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right) V_{ref}$$

$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right) V_{ref}$$

LED On When
Low Limit < V_{BATT} < High Limit

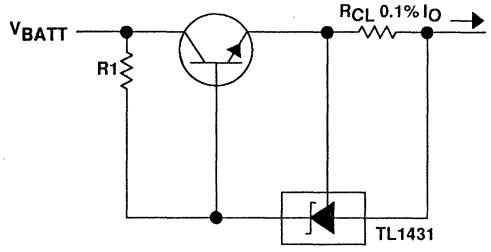
Note: R3 & R4 are selected to provide the desired LED intensity and ≥ 1 mA cathode current to the TL1431 at the available V+.

Figure 25. Voltage Monitor



$$\text{Delay} = R \times C \times I_I \frac{12\ V}{(12\ V) - Vref}$$

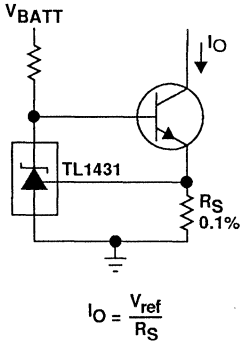
Figure 26. Delay Timer



$$I_O = \frac{V_{ref}}{R_{CL}} + I_K$$

$$R1 = \frac{V+}{\left(\frac{I_O}{h_{FE}}\right) + I_K}$$

Figure 27. Precision Current Limiter



$$I_O = \frac{V_{ref}}{R_S}$$

Figure 28. Precision Constant-Current Sink

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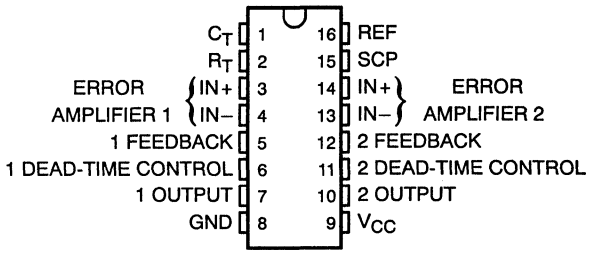
D2730, FEBRUARY 1983–REVISED AUGUST 1991

- **Complete PWM Power Control Circuitry**
- **Completely Synchronized Operation**
- **Internal Undervoltage Lockout Protection**
- **Wide Supply Voltage Range**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 500 kHz Max**
- **Variable Dead Time Provides Control Over Total Range**
- **Internal Regulator Provides a Stable 2.5-V Reference Supply**

DB†, N, NS, OR PW† PACKAGE
(TOP VIEW)



† The DB and PW packages are only available left-end taped and reeled (add LE suffix, i.e., TL1451ACPWLE)

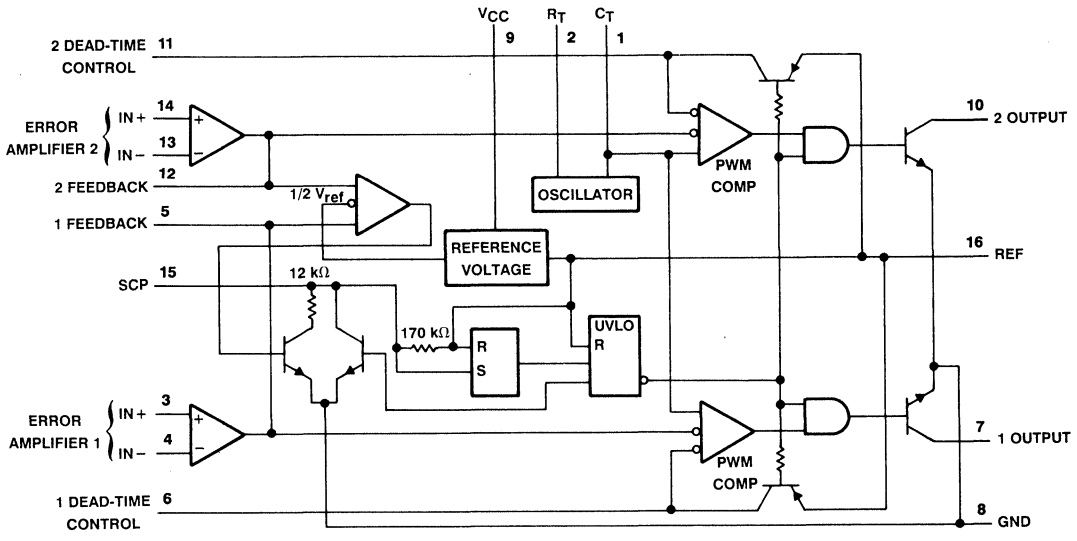
description

The TL1451AC incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation control circuits. Designed primarily for power supply control, the TL1451AC contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control comparator has no offset unless externally altered and may be used to provide 0% to 100% dead time. The on-chip oscillator may be operated by terminating R_T and C_T. During low V_{CC} conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from –20°C to 85°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} ..... 51 V
Amplifier input voltage ..... 20 V
Collector output voltage ..... 51 V
Collector output current ..... 21 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... −20°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	775 mW	6.2 mW/°C	496 mW	403 mW
N	1000 mW	8.0 mW/°C	640 mW	520 mW
NS	500 mW	4.0 mW/°C	320 mW	260 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	3.6	50	V
Amplifier input voltage, V_I	1.05	1.45	V
Collector output voltage, V_O		50	V
Collector output current		20	mA
Current into feedback terminal		45	μA
Feedback resistor, R_F	100		kΩ
Timing capacitor, C_T	150	15000	pF
Timing resistor, R_T	5.1	100	kΩ
Oscillator frequency	1	500	kHz
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (pin 16)	I_O = 1 mA	2.4	2.5	2.6	V
Output voltage change with temperature	T_A = −20°C to 25°C		−0.1%	±1%	
	T_A = 25°C to 85°C		−0.2%	±1%	
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output regulation	I_O = 0.1 mA to 1 mA		1	7.5	mV
Short-circuit output current	V_O = 0	3	10	30	mA

undervoltage lockout section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Upper threshold voltage (pin 9)	I_{Oref} = 0.1 mA, T_A = 25°C		2.72		V
Lower threshold voltage (pin 9)			2.6		V
Hysteresis (pin 9)		80	120		mV
Reset threshold voltage (pin 9)		1.5	1.9		V

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

protection control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 15)	T_A = 25°C	0.65	0.7	0.75	V
Standby voltage (pin 15)	No pullup	140	185	230	mV
Latched input voltage (pin 15)	No pullup		60	120	mV
Input (source) current	V_I = 0.7 V, T_A = 25°C	–10	–15	–20	μA
Comparator threshold voltage (pins 5 and 12)			1.18		V

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	C_T = 330 pF, R_T = 10 kΩ		200		kHz
Standard deviation of frequency	C_T = 330 pF, R_T = 10 kΩ		10%		
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1%		
Frequency change with temperature	T_A = –20°C to 25°C		–0.4%	±2%	
	T_A = 25°C to 85°C		–0.2%	±2%	

dead-time control section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pins 6 and 11)				1	μA
Latch mode (source) current (pins 6 and 11)	T_A = 25°C	–80	–145		μA
Latched input voltage (pins 6 and 11)	I_O = 40 μA	2.3			V
Input threshold voltage at f = 10 kHz (pins 6 and 11)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

error-amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pins 5 and 12) = 1.25 V			±6	mV
Input offset current	V_O (pins 5 and 12) = 1.25 V			±100	nA
Input bias current	V_O (pins 5 and 12) = 1.25 V		160	500	nA
Common-mode input voltage range	V_{CC} = 3.6 V to 40 V	1.05 to 1.45			V
Open-loop voltage amplification	R_F = 200 kΩ	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		V_{ref}–0.1			V
Negative output voltage swing				1	V
Output (sink) current (pins 5 and 12)	V_{ID} = –0.1 V, V_O = 1.25 V	0.5	1.6		mA
Output (source) current (pins 5 and 12)	V_{ID} = 0.1 V, V_O = 1.25 V	–45	–70		μA

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 200 kHz (unless otherwise noted) (continued)

output section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current	V_O = 50 V			10	μA
Output saturation voltage	I_O = 10 mA		1.2	2	V
Short-circuit output current	V_O = 6 V		90		mA

pwm comparator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage at	Zero duty cycle		2.05	2.25	V
f = 10 kHz (pins 5 and 12)	Maximum duty cycle	1.2	1.45		

total device

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	R_T = 10 kΩ		1.7	2.4	mA

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

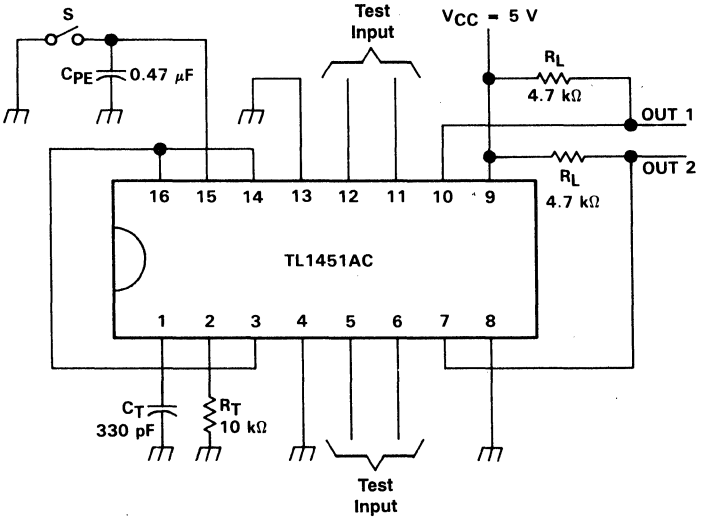


Figure 1. Test Circuit

PARAMETER MEASUREMENT INFORMATION

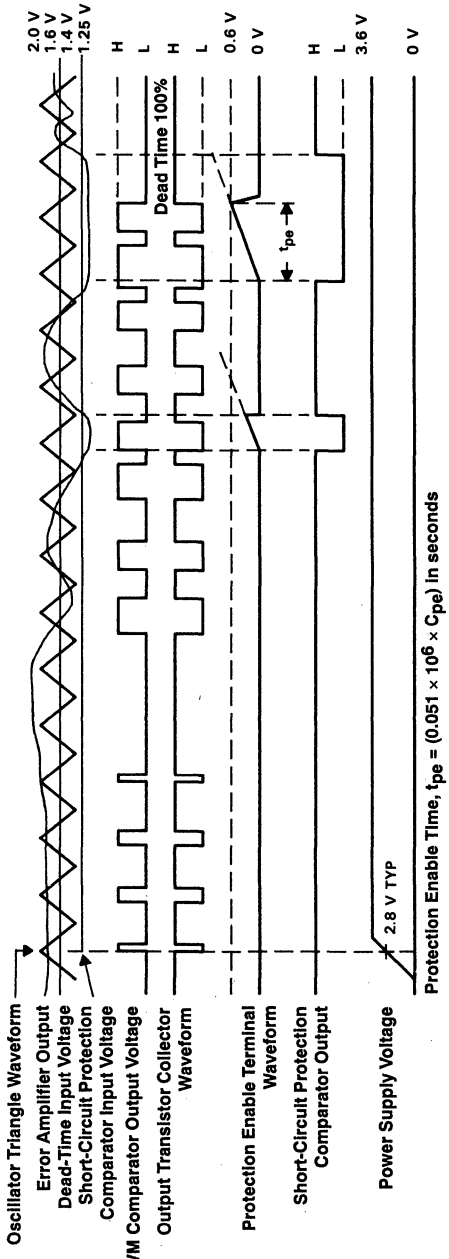


Figure 2. TL1451AC Timing Diagram

TYPICAL CHARACTERISTICS

TRIANGLE OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

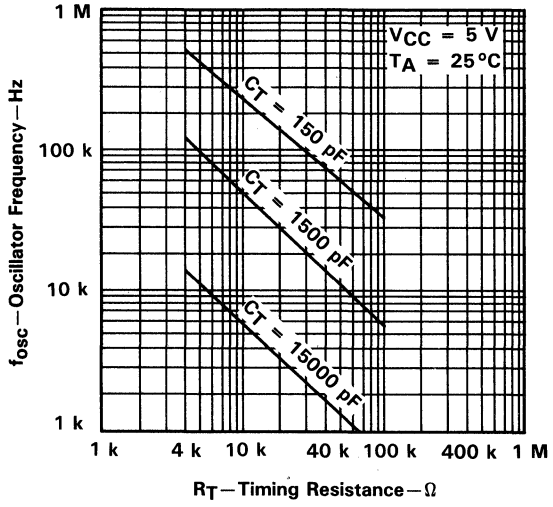


Figure 3

OSCILLATOR FREQUENCY VARIATION
vs
FREE-AIR TEMPERATURE

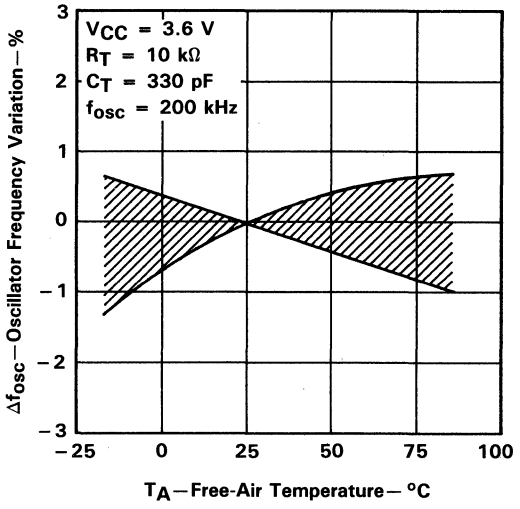


Figure 4

TRIANGLE WAVEFORM SWING VOLTAGE
vs
TIMING CAPACITANCE

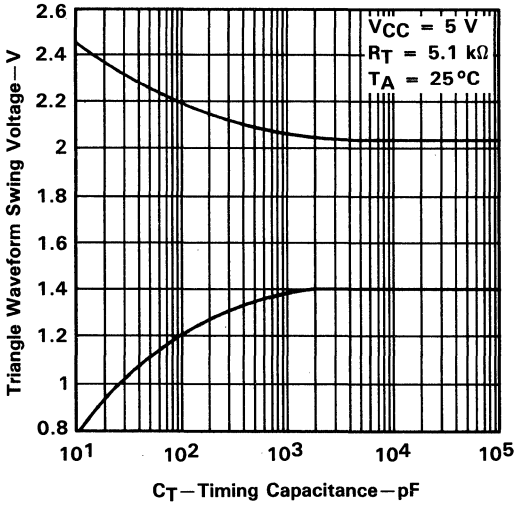


Figure 5

TRIANGLE WAVEFORM PERIOD
vs
TIMING CAPACITANCE

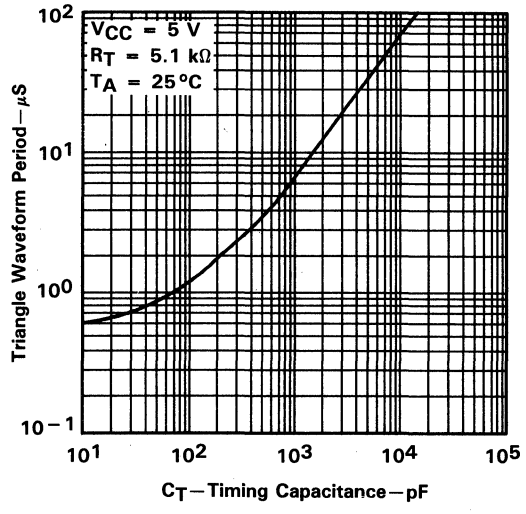


Figure 6

TYPICAL CHARACTERISTICS

REFERENCE OUTPUT VOLTAGE VARIATION
vs
FREE-AIR TEMPERATURE

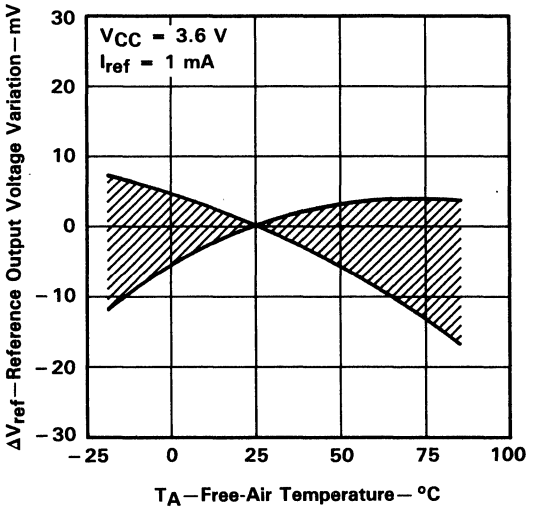


Figure 7

REFERENCE OUTPUT VOLTAGE VARIATION
vs
FREE-AIR TEMPERATURE

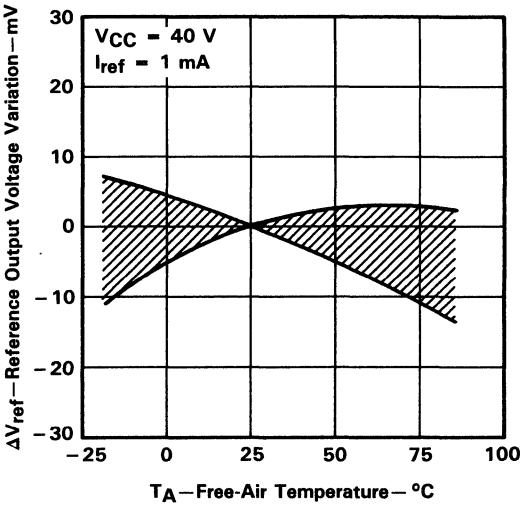


Figure 8

REFERENCE OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

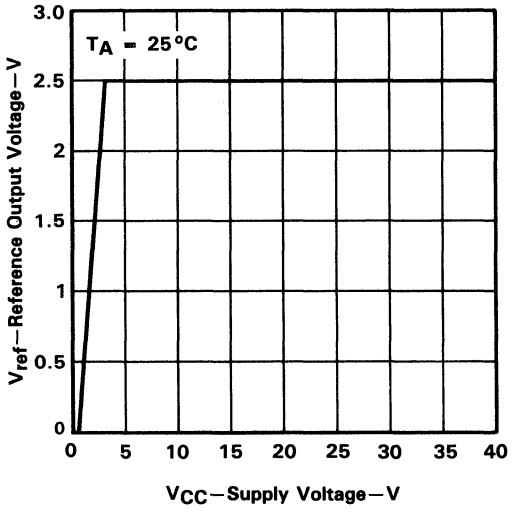


Figure 9

DROP-OUT VOLTAGE VARIATION
vs
FREE-AIR TEMPERATURE

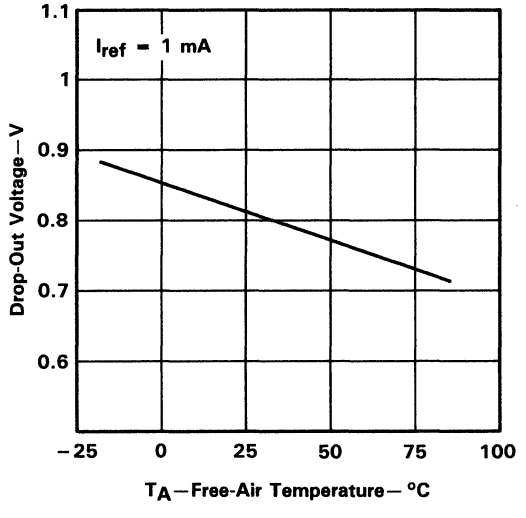


Figure 10

TYPICAL CHARACTERISTICS

UNDERVOLTAGE LOCKOUT
HYSTERESIS CHARACTERISTICS
vs
SUPPLY VOLTAGE

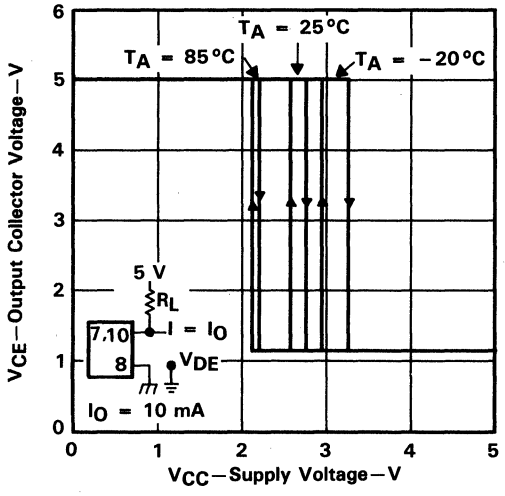


Figure 11

UNDERVOLTAGE LOCKOUT CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

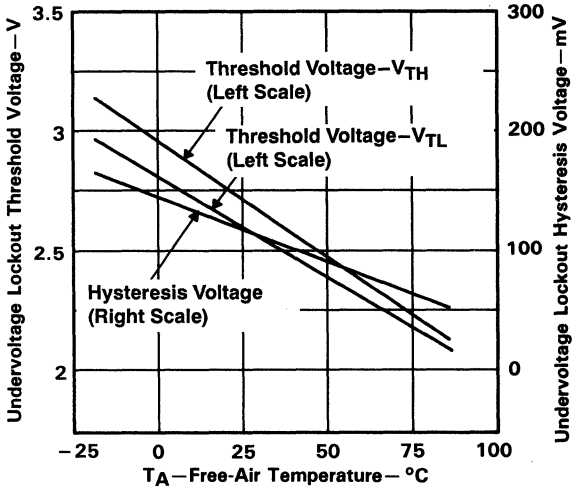


Figure 12

SHORT-CIRCUIT PROTECTION CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

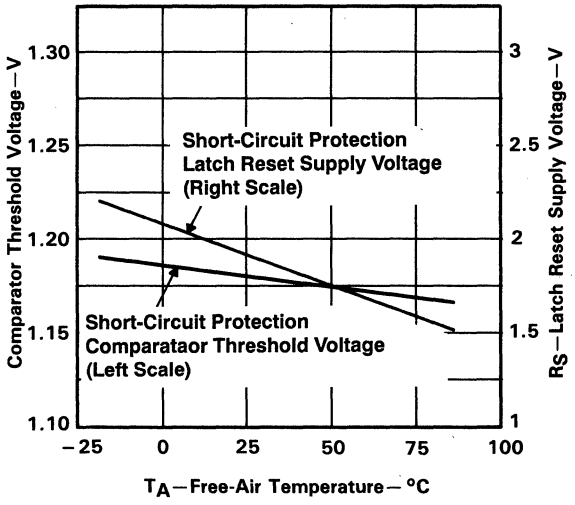
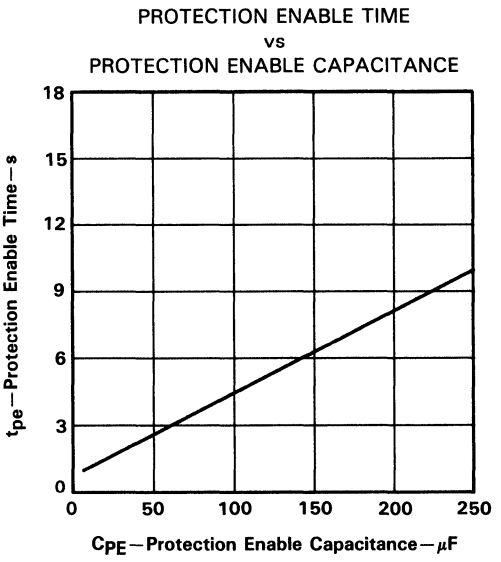


Figure 13

TYPICAL CHARACTERISTICS



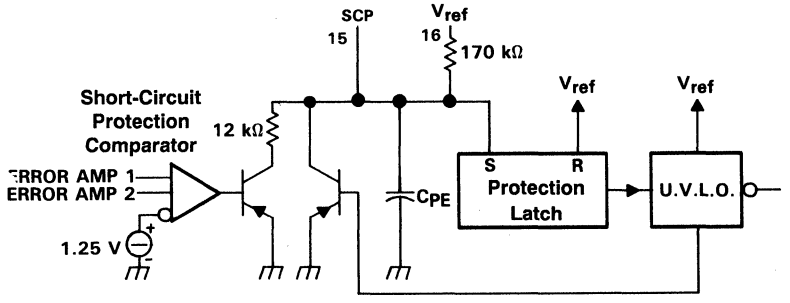


Figure 14

TYPICAL CHARACTERISTICS

ERROR AMP MAXIMUM OUTPUT VOLTAGE SWING
vs
FREQUENCY

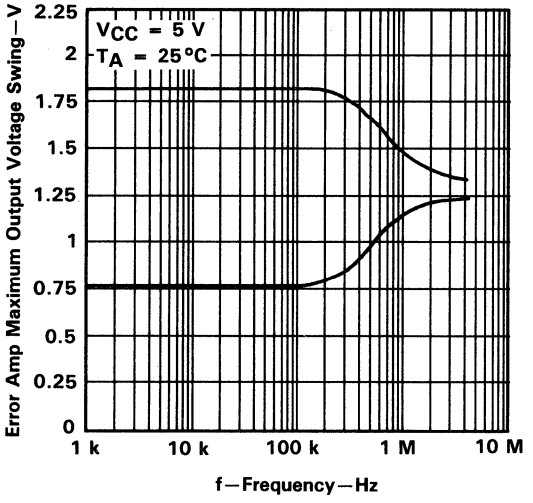


Figure 15

OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREQUENCY

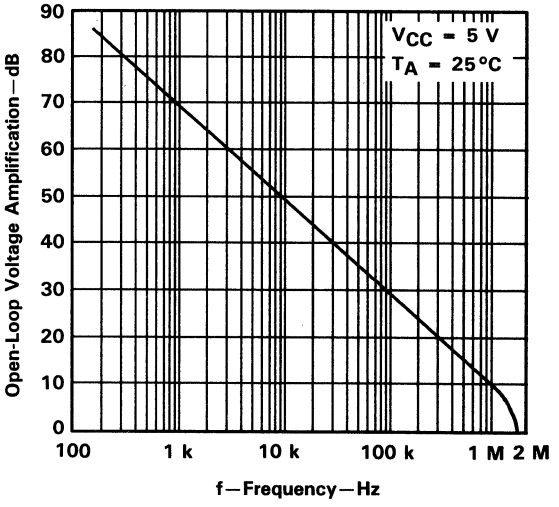


Figure 16

GAIN OF AN AMPLIFIER
IN UNITY-GAIN CONFIGURATION
vs
FREQUENCY

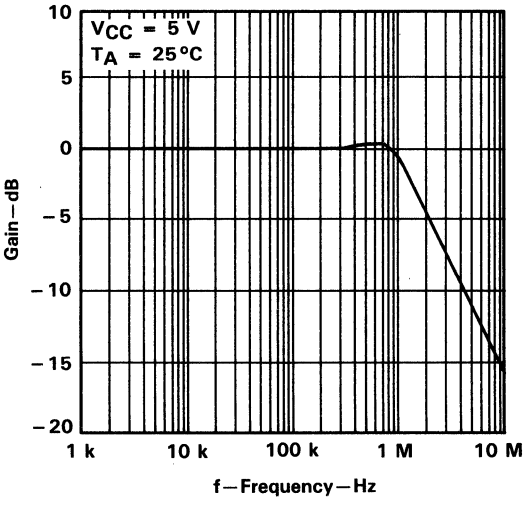
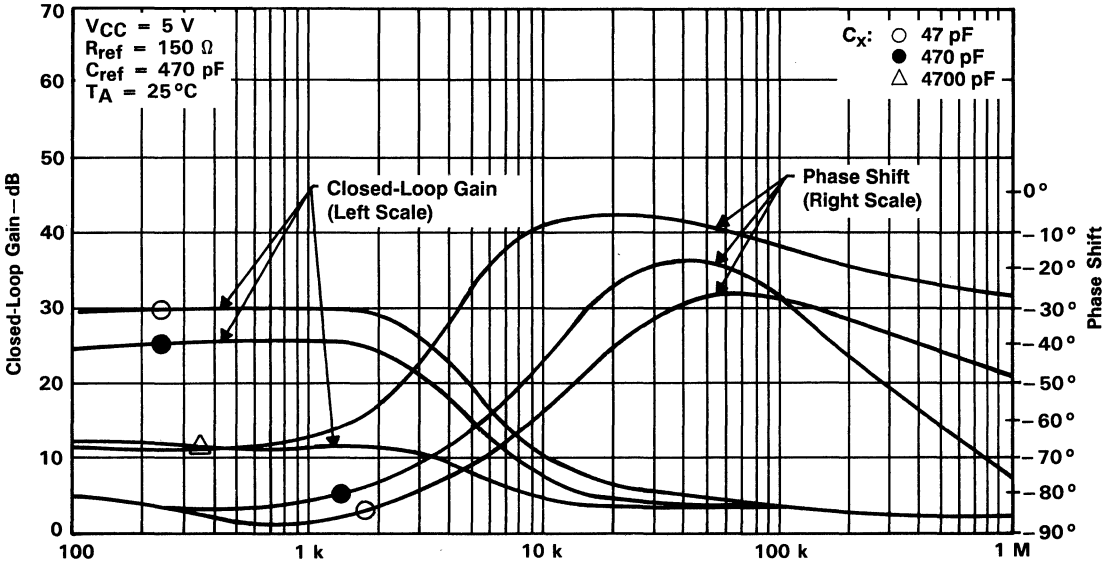
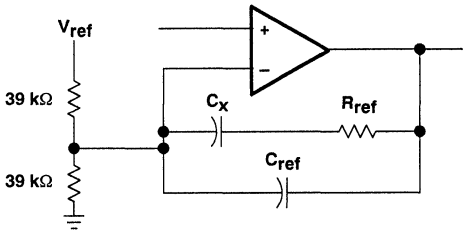


Figure 17

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



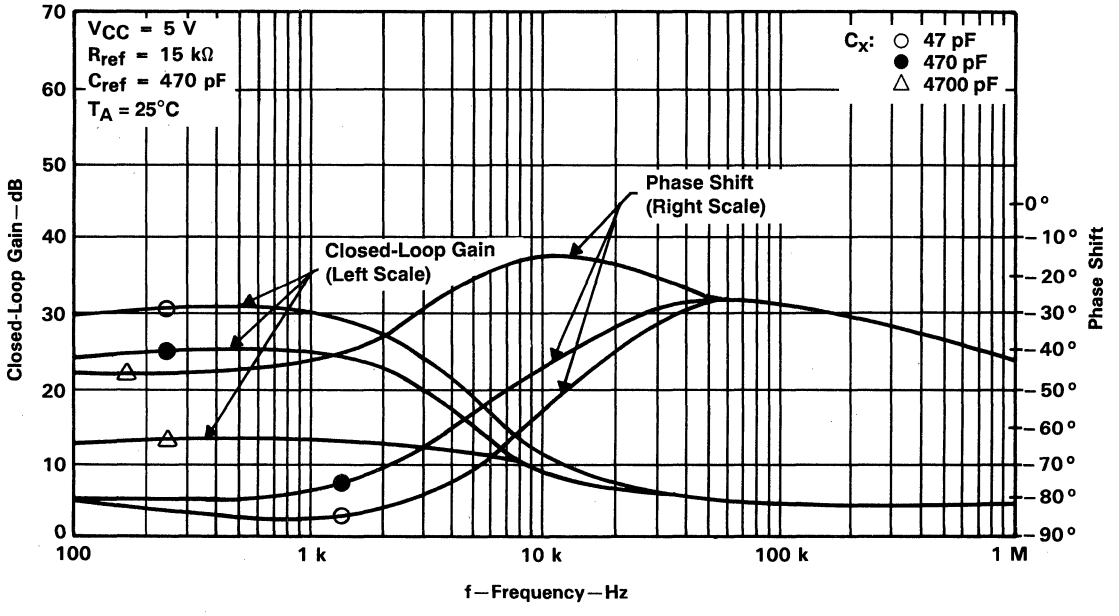


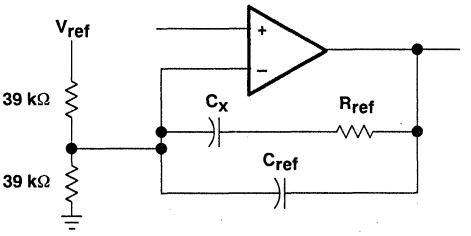
TEST CIRCUIT

Figure 18

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



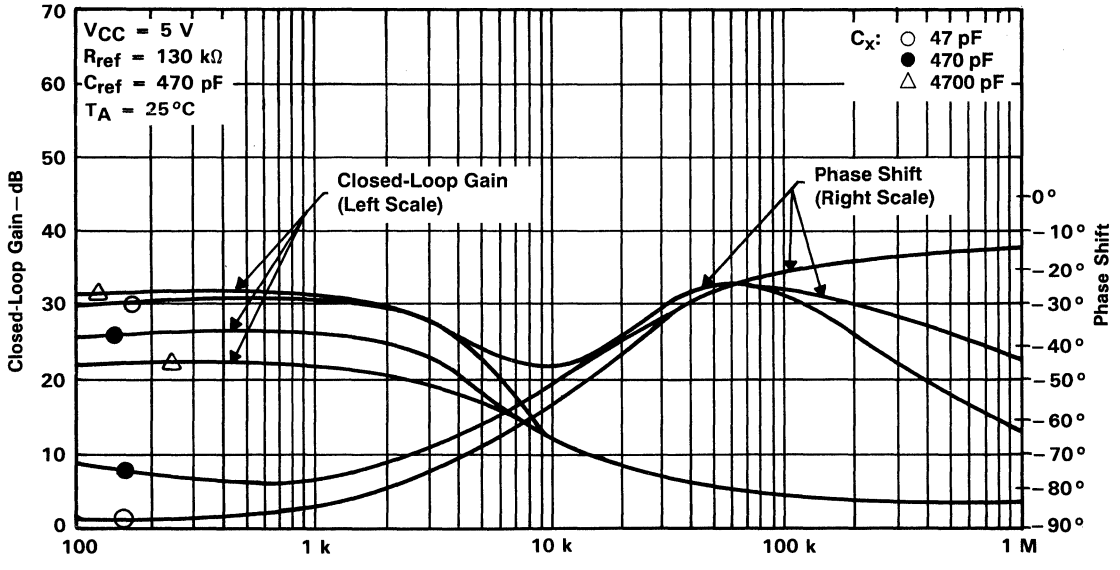


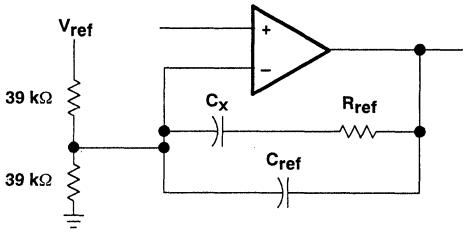
TEST CIRCUIT

Figure 19

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY



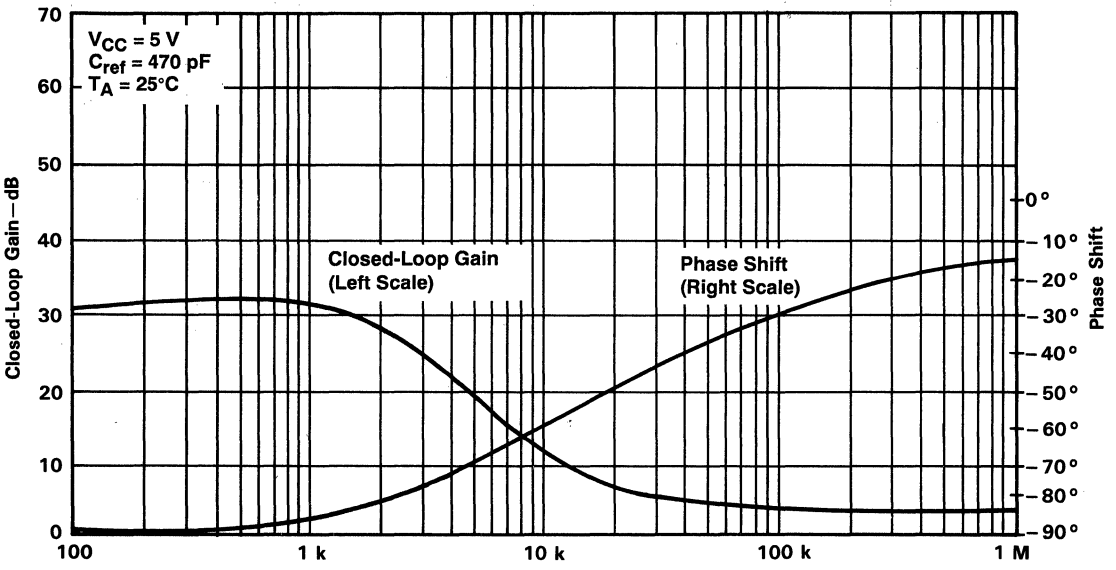


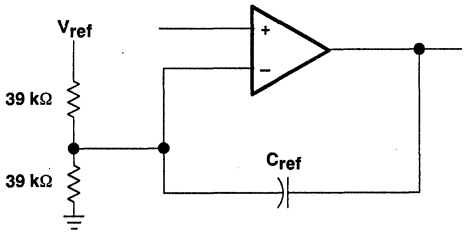
TEST CIRCUIT

Figure 20

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE SHIFT
vs
FREQUENCY





TEST CIRCUIT

Figure 21

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT
vs
COLLECTOR OUTPUT SATURATION VOLTAGE

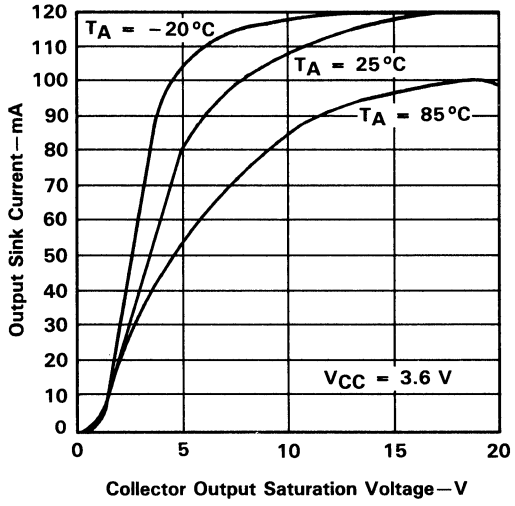
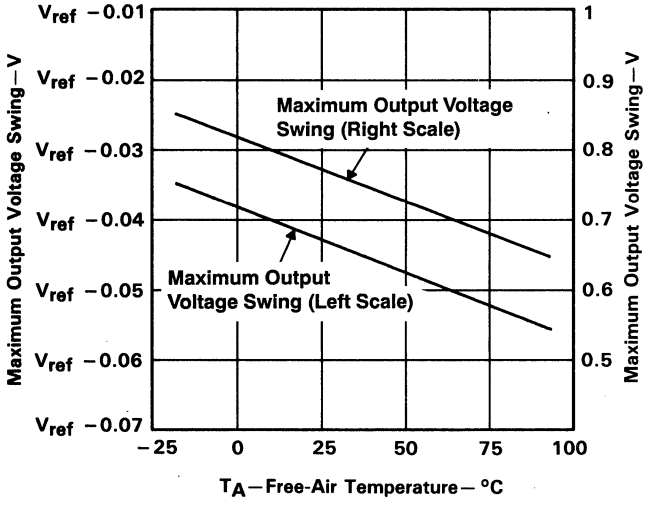
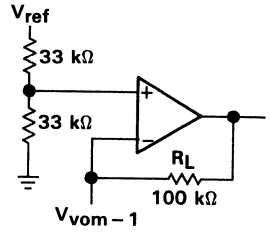


Figure 22

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE





V_{CC} = 3.6 V
R_L = 100 kΩ
V_{vom} +1 = 1.25 V
V_{vom} −1 = 1.15 V (Right Scale)
V_{vom} −1 = 1.35 V (Left Scale)

TEST CIRCUIT

Figure 23

TYPICAL CHARACTERISTICS

OUTPUT TRANSISTOR "ON" DUTY CYCLE
vs
DEAD-TIME INPUT VOLTAGE

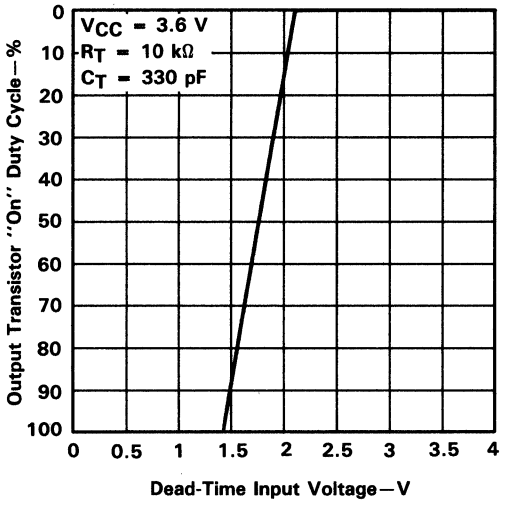


Figure 24

STANDBY CURRENT
vs
SUPPLY VOLTAGE

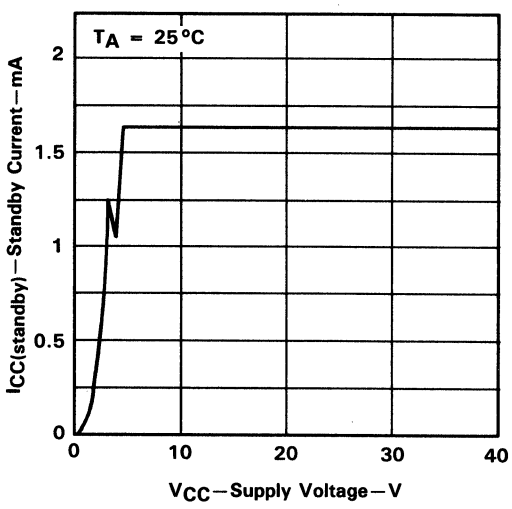


Figure 25

STANDBY CURRENT
vs
FREE-AIR TEMPERATURE

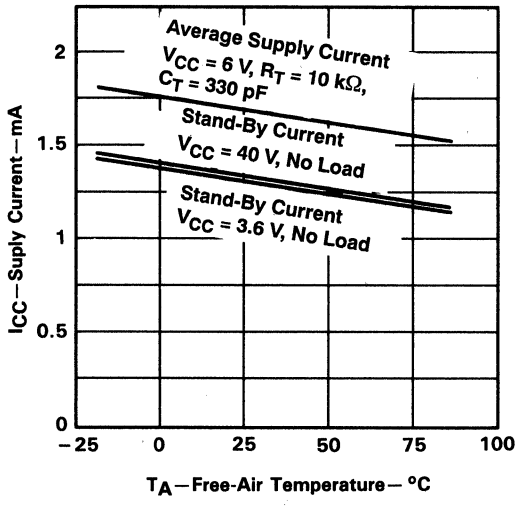


Figure 26

MAXIMUM CONTINUOUS POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

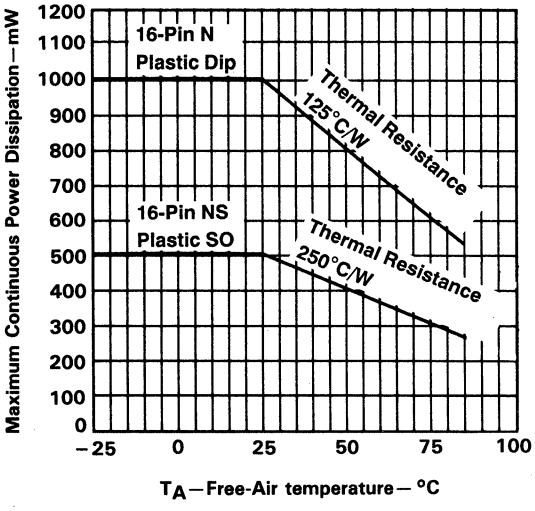
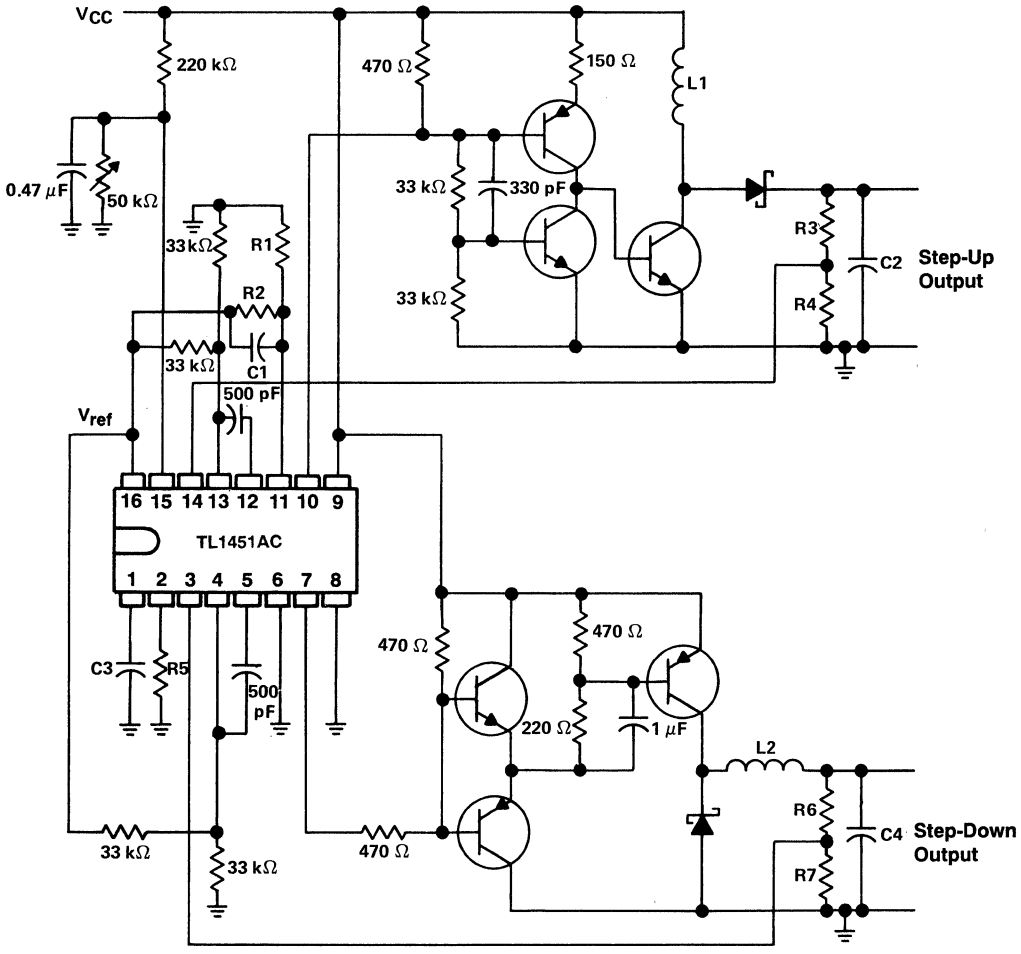


Figure 27

APPLICATION INFORMATION



Values for R1 through R7, C1 through C4, and L1 and L2 depend upon individual application.

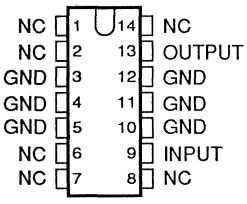
Figure 28. High-Speed Dual Switching Regulator

TL2217-285
FIXED VOLTAGE REGULATOR FOR SCSI ACTIVE TERMINATION

D3942, NOVEMBER 1991

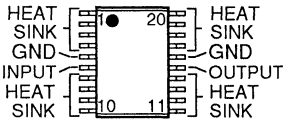
- **Fully Matches Parameters for Alternative 2 SCSI Active Termination**
- **Fixed 2.850-V Output**
- **±1.5% Maximum Output Tolerance at T_J = 25°C**
- **1-V Maximum Dropout Voltage**
- **500-mA Output Current**
- **±3% Absolute Output Variation**
- **Internal Overcurrent Limiting**
- **Internal Thermal Overload Protection**
- **Internal Overvoltage Protection**

N PACKAGE
(TOP VIEW)



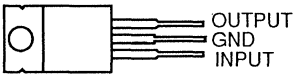
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded or electrically isolated.

KC PACKAGE
(TOP VIEW)

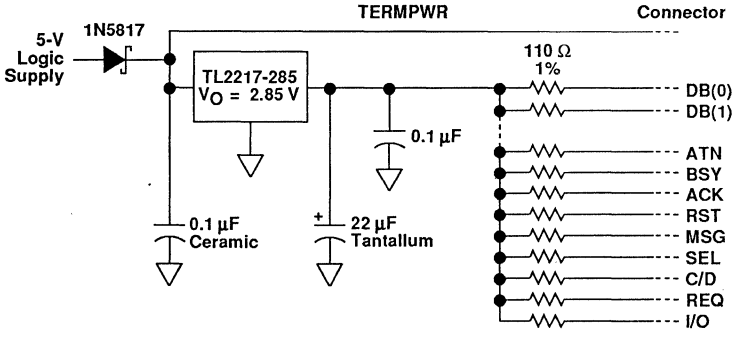


description

The TL2217-285 is a low-dropout (1-V) fixed voltage regulator specifically designed for Small Computer Systems Interface (SCSI) alternative 2 active signal termination. The TL2217-285's 1-V maximum dropout ensures compatibility with existing SCSI systems, while providing a wide TERMPWR voltage range. At the same time, the ±1.5% initial tolerance on its 2.85-V output voltage ensures a tighter line driver current tolerance, thereby increasing system noise margin.

The fixed 2.85-V output voltage of the TL2217-285 supports the SCSI alternative 2 termination standard while reducing system power consumption. The 1-V maximum dropout voltage brings increased TERMPWR isolation, making the device ideal for battery-powered systems. The TL2217-285, with internal current limiting,

typical application schematic



AVAILABLE OPTIONS

T_J	PACKAGE		
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†
0°C to 125°C	TL2217-285KC	TL2217-285N	TL2217-285PWLE

†The PW package is only available left-end taped and reeled.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

overvoltage protection, ESD protection, and thermal protection, offers designers enhanced system protection and reliability.

When configured as a SCSI active terminator, the TL2217-285 low-dropout regulator eliminates the 220-Ω and 330-Ω resistors required for each transmission line with a passive termination scheme, reducing significantly the continuous system power drain. When placed in series with 110-Ω resistors, the device matches the impedance level of the transmission cable and eliminates reflections.

The TL2217-285 is characterized for operation from 0°C to 125°C virtual junction temperature.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Continuous input voltage . . . . . 7.5 V
Continuous total dissipation (see Note 1) . . . . . See Dissipation Rating Table
Operating virtual junction temperature range . . . . . –55°C to 150°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16 mW/°C	1280 mW	1040 mW	400 mW
	T_C	20000 mW	182 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18.0 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	775 mW	6.4 mW/°C	520 mW	423 mW	161 mW

Derate above 40°C

DISSIPATION DERATING CURVE vs FREE-AIR TEMPERATURE

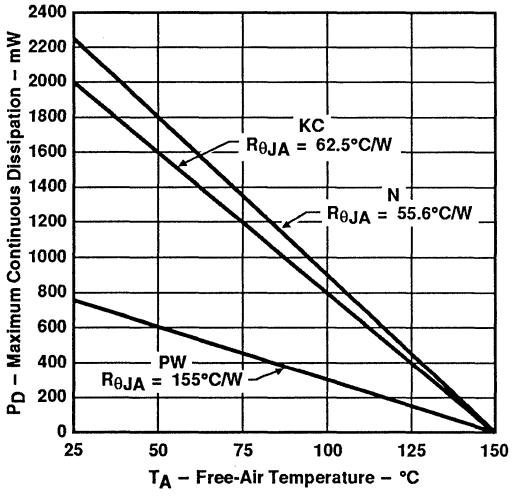


Figure 1

DISSIPATION DERATING CURVE vs CASE TEMPERATURE

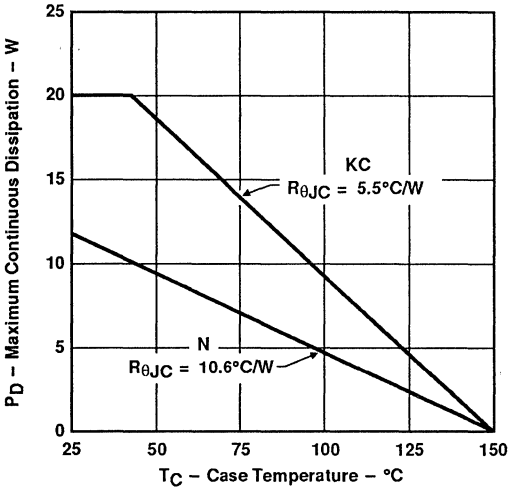


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.85	5.5	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.85 V to 5.5 V	$T_A = T_J$ = 25°	2.81	2.85	2.89	V
		T_J = 0°C to 125°C	2.765		2.935	
Input regulation	V_I = 3.85 V to 5.5 V, I_O = 500 mA			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}			–62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Dropout voltage	I_O = 500 mA				1	V
Bias current	I_O = 0			2	5	mA
	I_O = 27 mA, equivalent 1 line asserted			3	6	
	I_O = 500 mA, equivalent 18 line asserted (8 bit)			26	49	

Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 22-µF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TL2217-285 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

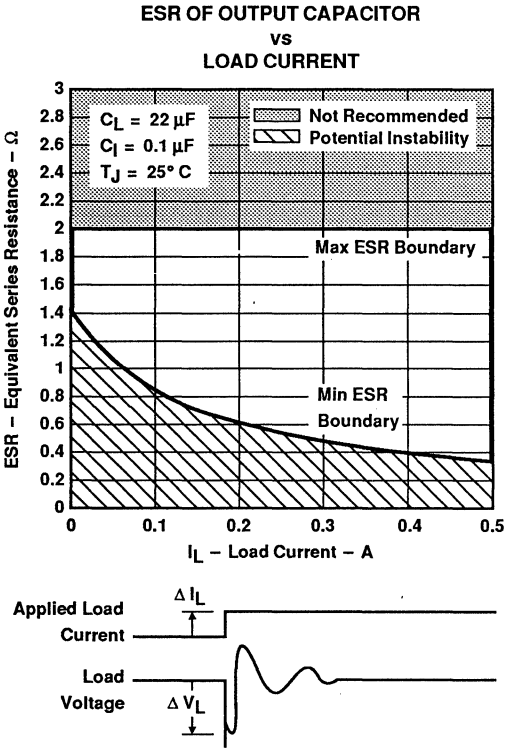


Figure 3

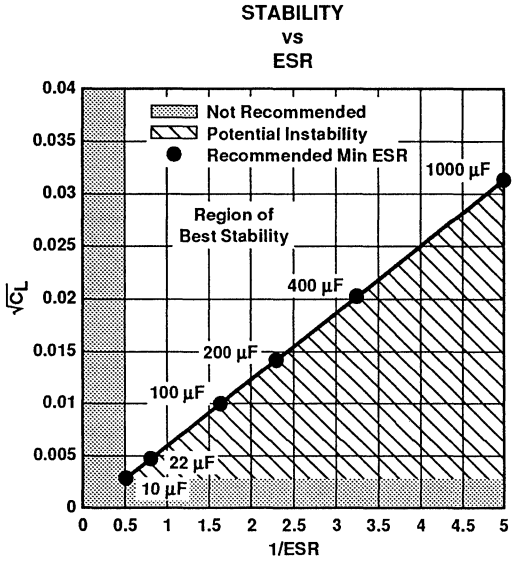
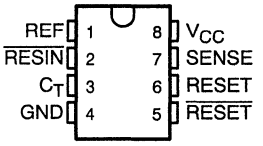


Figure 4

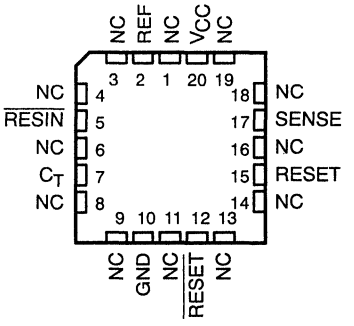
D2722, APRIL 1983–REVISED NOVEMBER 1991

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Wide Supply Voltage Range**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL77_ _ A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). If an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

During power down (assuming that SENSE is below V_{T-}), the outputs remain active until the V_{CC} falls below a maximum of 2 V. After this, the outputs are undefined.

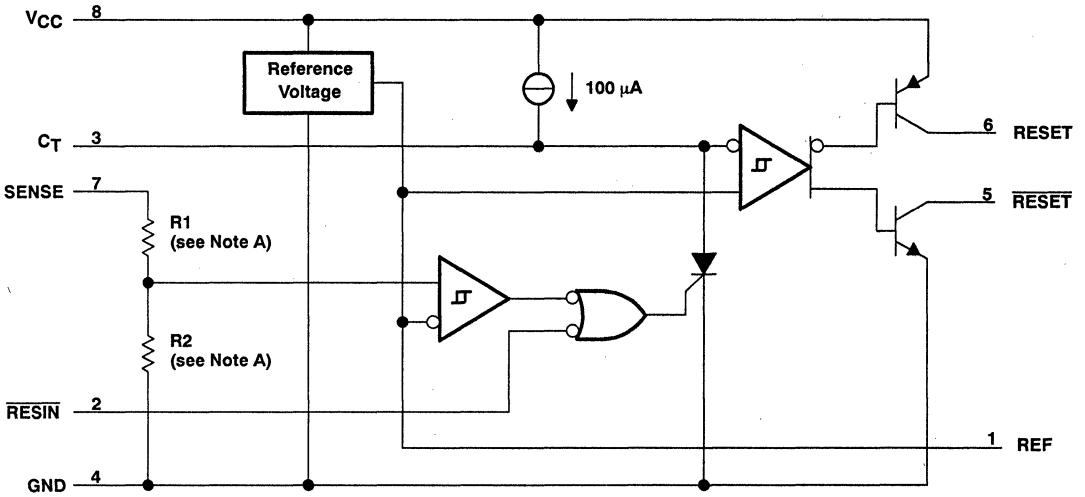
An external capacitor (typically 0.1 μF for the TL77_ _ AC and TL77 _ _Al and typically 0.02 μF for the TL77 _ _ AM) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77_ _ AC series are characterized for operation from 0°C to 70°C. The TL77_ _ Al series are characterized for operation from –25°C to 85°C. The TL7702AM and TL7705AM are characterized for operation over the full military range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TL7702ACD thru TL7715ACD			TL7702ACP thru TL7715ACP
–25°C to 85°C	TL7702AID thru TL7715AID			TL7702AIP thru TL7715AIP
–55°C to 125°C		TL7702AMFK TL7705AMFK	TL7702AMJG TL7705AMJG	

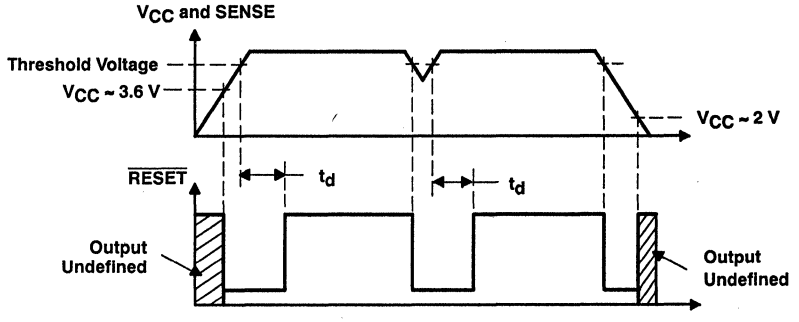
functional block diagram



NOTE A: TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ

Pin numbers shown are for the D, JG, or P package.

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, $\overline{RESIN}$ ..... −0.3 V to 20 V
Input voltage range, SENSE: TL7702A (see Note 2) ..... −0.3 V to 6 V
TL7705A ..... −0.3 V to 10 V
TL7709A ..... −0.3 V to 15 V
TL7712A, TL7715A ..... −0.3 V to 20 V
High-level output current, $\overline{RESET}$ ..... −30 mA
Low-level output current, $\overline{RESET}$ ..... 30 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL77_ _AC ..... 0°C to 70°C
TL77_ _AI ..... −25°C to 85°C
TL7702AM, TL7705AM ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 second: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	888 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		TL77_ _AC and TL77_ _AI		TL77_ _AM		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		3.6	18	3.6	10	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2		2		V
Low-level input voltage at $\overline{RESIN}$, V_{IL}			0.6		0.6	V
Input voltage, SENSE, V_I	TL7702A	0	See Note 2	0	See Note 2	V
	TL7705A	0	10	0	10	
	TL7709A	0	15			
	TL7712A	0	20			
	TL7715A	0	20			
High-level output current, RESET, I_{OH}			−16		−16	mA
Low-level output current, $\overline{RESET}$, I_{OL}			16		16	mA
Operating free-air temperature range, T_A	TL77_ _AC	0	70			°C
	TL77_ _AI	−25	85			
	TL7702AM, TL7705AM			−55	125	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC}−1 V or 6 V, whichever is less.

electrical characteristics over recommended opoerating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage		T_A = 25°C	2.48	2.53	2.58	V
V_{T-}	Negative-going threshold voltage, SENSE	TL7702A	T_A = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V_{hys}	Hysteresis, SENSE ($V_{T+} - V_{T-}$)	TL7702A	T_A = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current, $\overline{\text{RESIN}}$		V_I = 2.4 V to V_{CC}			20	μA
			V_I = 0.4 V			–100	
I_I	Input current, SENSE	TL7702A	V_{ref} < V_I < V_{CC} – 1.5 V		0.5	2	μA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 18 V			50	μA
I_{OL}	Low-level output current, RESET		V_O = 0			–50	μA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.1-μF capacitors connected at REF, C_T, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
$t_{wS(min)}$	Minimum pulse duration at SENSE input to switch outputs	V_{IH} = V_{T-} +200 mV, V_{IL} = V_{T-} –200 mV			2	μs
t_{pd}	Propagation delay time from $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	V_{CC} = 5 V		1.5		μs
t_r	RESET	V_{CC} = 5 V, See Note 3			0.2	μs
	$\overline{\text{RESET}}$				3.5	
t_f	RESET				3.5	μs
	$\overline{\text{RESET}}$				0.2	

‡ All switching characteristics are measured with 0.1-μF capacitors connected at REF and V_{CC} to GND.
NOTE 3: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA	V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference voltage			2.38	2.53	2.63	V
V_{T-}	Negative-going threshold voltage, SENSE	TL7702AM	V_{CC} = 3.6 V to 10 V	2.38	2.53	2.63	V
		TL7705AM		4.25	4.55	4.7	
V_{hys}	Hysteresis SENSE ($V_{T+} - V_{T-}$)	TL7702AM	V_{CC} = 3.6 V to 10 V		10		mV
		TL7705AM			15		
I_I	Input current, $\overline{\text{RESIN}}$		V_I = 2.4 V to V_{CC}			20	μA
			V_I = 0.4 V			–100	
I_I	Input current, SENSE	TL7702AM	$V_{ref} < V_I < V_{CC} - 1.5$ V		0.5	2	μA
I_{OH}	High-level output current, $\overline{\text{RESET}}$		V_O = 10 V			50	μA
I_{OL}	Low-level output current, RESET		V_O = 0			–50	μA
I_{CC}	Supply current		All inputs and outputs open		1.8	3	mA

† All electrical characteristics are measured with 0.02-μF capacitors connected at REF, C_T, and V_{CC} to GND.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
$t_{wS(min)}$	Minimum pulse duration at SENSE input to switch outputs	$V_{IH} = V_{T-} + 200$ mV, $V_{IL} = V_{T-} - 200$ mV			2*	μs
t_{pd}	Propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	V_{CC} = 5 V		1.5		μs
t_r	RESET	V_{CC} = 5 V, See Note 3			0.2*	μs
	$\overline{\text{RESET}}$				3.5*	
t_f	RESET				3.5*	μs
	$\overline{\text{RESET}}$				0.2*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† All switching characteristics are measured with 0.02-μF capacitors connected at REF and V_{CC} to GND.
NOTE 3: The rise and fall times are measured with a 4.7-kΩ load resistor at $\overline{\text{RESET}}$ and RESET.

PARAMETER MEASUREMENT INFORMATION

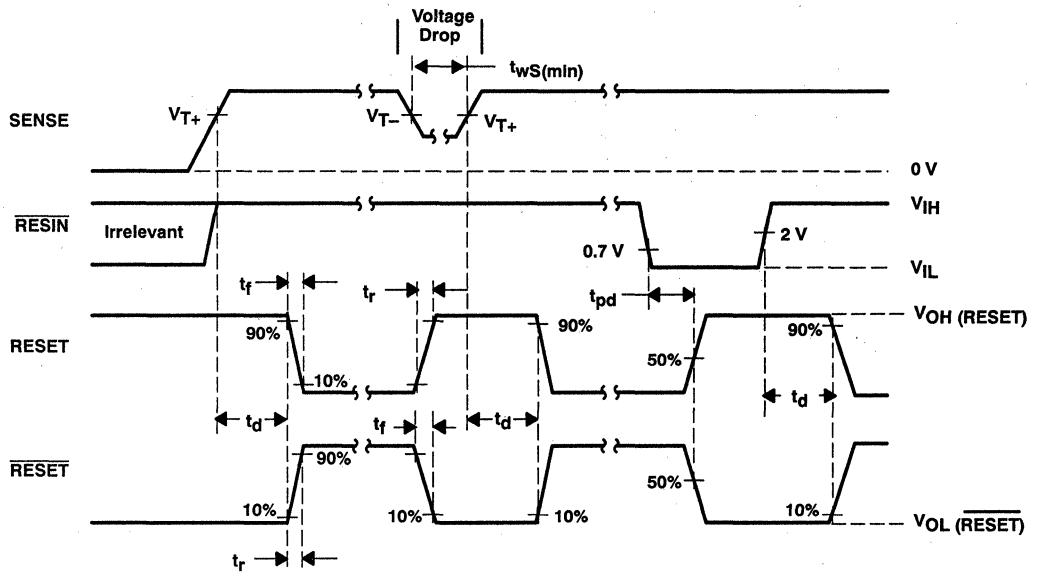
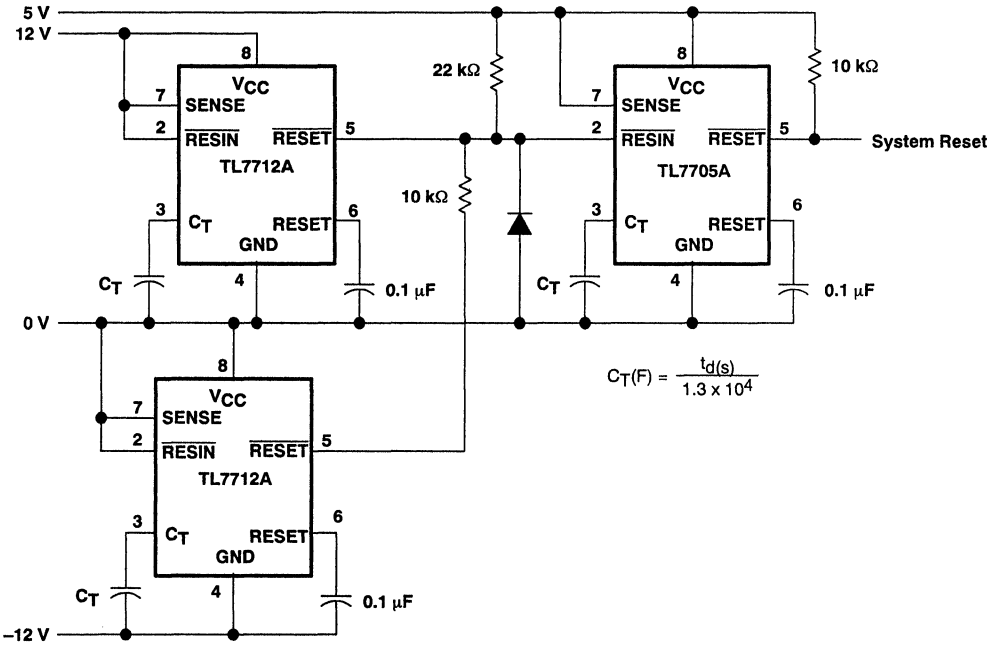


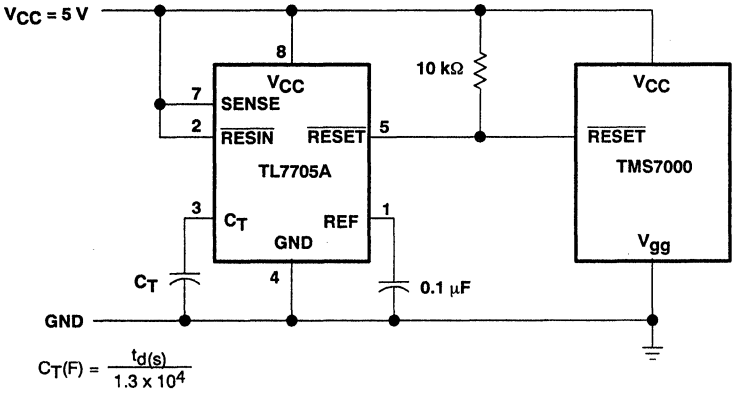
Figure 1. Voltage Waveforms

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, and P packages.

Figure 2. Multiple Power Supply System Reset Generation



Pin numbers shown are for the D, JG, and P packages.

Figure 3. Reset Controller for TMS7000 System

APPLICATION INFORMATION

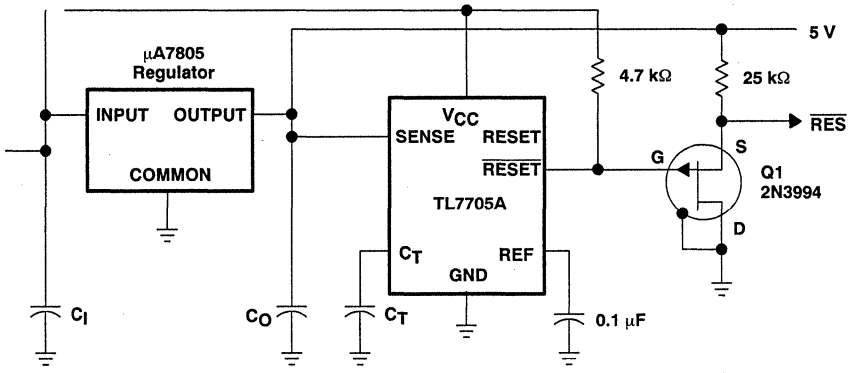


Figure 4. Eliminating Undefined States Using a P-Channel JFET

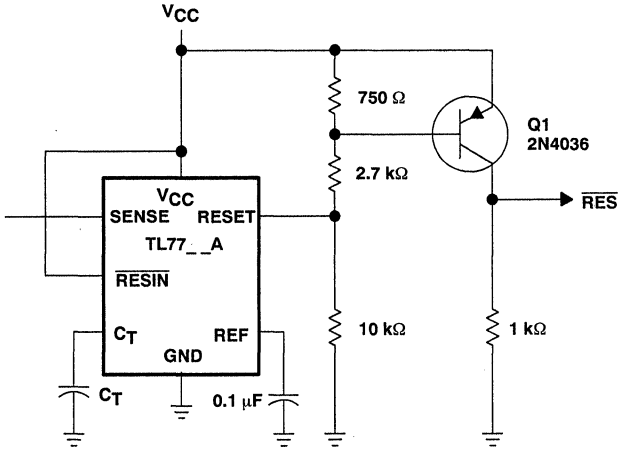
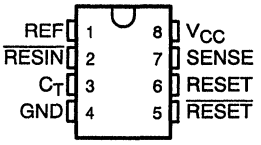


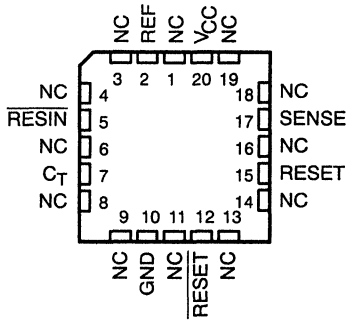
Figure 5. Eliminating Undefined States Using a P-N-P Transistor

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Defined Output From $V_{CC} \geq 1$ V**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **True and Complement Reset Outputs**
- **Externally Adjustable Pulse Duration**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

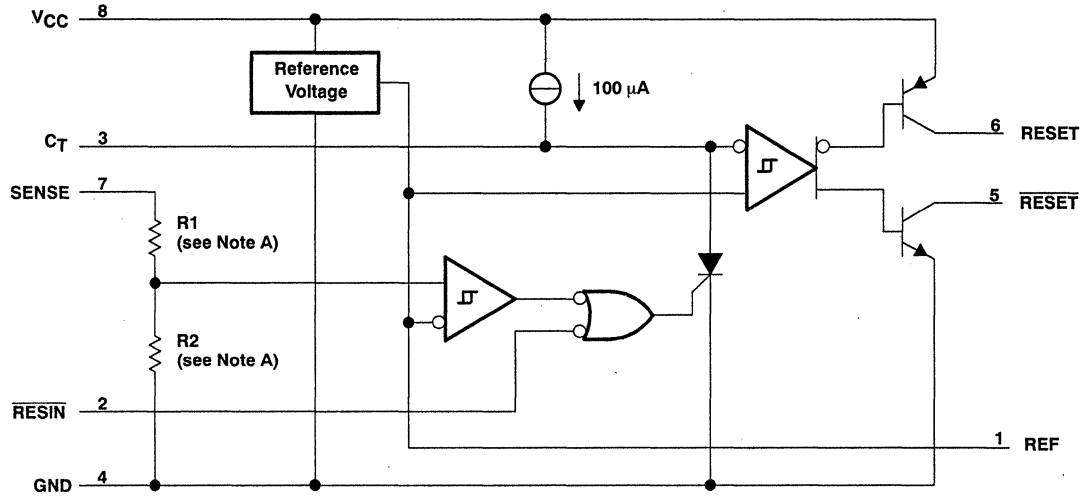
description

The TL7702B and TL7705B are monolithic integrated circuit voltage supervisors designed for use as reset controllers in microcomputer and microprocessor systems. The supply voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 1 V. As V_{CC} approaches 3 V (assuming that SENSE is above V_{T+}), the delay timer function activates a time delay after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). If an undervoltage condition occurs during normal operation, outputs $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

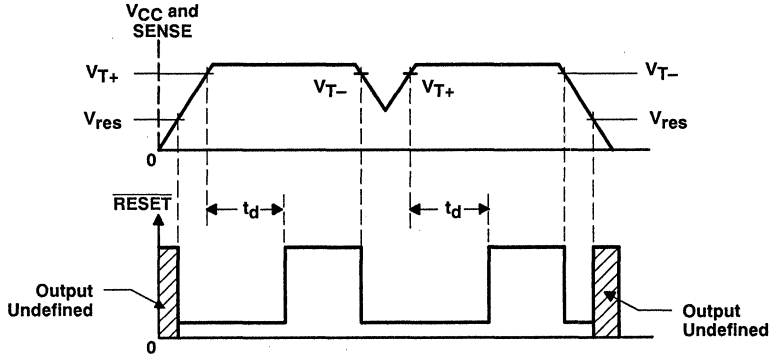
The TL7702BC and TL7705BC are characterized from 0°C to 70°C. The TL7702BI and TL7705BI are characterized for operation from –40°C to 85°C. The TL7702BQ and TL7705BQ are characterized for operation from –40°C to 125°C. The TL7702BM and TL7705BM are characterized for operation from –55°C to 125°C.

functional block diagram



NOTE A: TL7702B: R1 = 0 Ω, R2 = open
TL7705B: R1 = 16 kΩ, R2 = 8 kΩ

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range at $\overline{RESIN}$ ..... −0.3 V to 20 V
Input voltage range at SENSE: TL7702B ..... −0.3 V to 20 V
TL7705B ..... −0.3 V to 20 V
High-level output current at $\overline{RESET}$ ..... −30 mA
Low-level output current at $\overline{RESET}$ ..... 30 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL77_BC ..... 0°C to 70°C
TL77_BI ..... −40°C to 85°C
TL77_BQ ..... −40°C to 125°C
TL77_BM ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	18	V
High-level input voltage at $\overline{RESIN}$, V_{IH}		2	18	V
Low-level input voltage at $\overline{RESIN}$, V_{IL}		0	0.8	V
Input voltage at SENSE, V_I		0	18	V
High-level output current at RESET, I_{OH}			−16	mA
Low-level output current at $\overline{RESET}$, I_{OL}			16	mA
Operating free-air temperature range, T_A	TL77_BC	0	70	°C
	TL77_BI	−40	85	
	TL77_BQ	−40	125	
	TL77_BM	−55	125	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{RESET}$		I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage		I_{ref} = 500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{T-}	Negative-going threshold voltage, SENSE	TL7702B	T_A = 25°C		2.505	2.53	2.555	V
		TL7705B			4.5	4.55	4.6	
		TL7702B			2.48	2.53	2.58	
		TL7705B			4.45	4.55	4.65	
V_{hys}	Hysteresis SENSE ($V_{T+} - V_{T-}$)	TL7702B	V_{CC} = 3.6 V to 18 V,			10		mV
		TL7705B	T_A = 25°C			30		
I_I	Input current, $\overline{RESIN}$		V_I = 0.4 V to V_{CC}				–10	µA
I_I	Input current, SENSE	TL7702B	V_I = V_{ref} to 18 V			–0.1	–2	µA
I_{OH}	High-level output current, $\overline{RESET}$		V_O = 18 V,	See Figure 1			50	µA
I_{OL}	Low-level output current, RESET		V_O = 0 V,	See Figure 1			–50	µA
V_{res}‡	Power-up reset voltage		$I_{OL(\overline{RESET})}$ = 2 mA,	T_A = 25°C			1	V
I_{CC}	Supply current		V_{SENSE} = 15 V,	$\overline{RESIN}$ ≥ 2 V		1.8	3	mA

† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, C_T, and V_{CC} to GND.
‡ This is the lowest voltage at which $\overline{RESET}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{RESIN}$	RESET	See Figures 1, 2, and 3		270	500	ns
t_{PHL}	Propagation delay time from low-to-high-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500	ns
$t_{w(min)}$	Pulse duration, minimum effective	$\overline{RESIN}$		See Figure 2(a)		150		ns
		SENSE		See Figure 2(b)		100		
t_r	Rise time		$\overline{RESET}$	See Figures 1, 2, and 3			75	ns
t_f	Fall time					150	200	
t_r	Rise time		RESET			75	150	ns
t_f	Fall time						50	

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, RESET		I_{OH} = –16 mA		V_{CC}–1.5			V
V_{OL}	Low-level output voltage, $\overline{RESET}$		I_{OL} = 16 mA				0.4	V
V_{ref}	Reference voltage		I_{ref} = 500 µA,	T_A = 25°C	2.48	2.53	2.58	V
V_{T-}	Negative-going threshold voltage at SENSE input	TL7702B	T_A = 25°C		2.505	2.53	2.555	V
		TL7705B			4.5	4.55	4.6	V
		TL7702B			2.48	2.53	2.58	V
		TL7705B			4.45	4.55	4.65	V
V_{hys}	Hysteresis, SENSE ($V_{T+} - V_{T-}$)	TL7702B	V_{CC} = 3.6 V to 18 V,			10		mV
		TL7705B	T_A = 25°C			30		mV
I_I	Input current, $\overline{RESIN}$		V_I = 0.4 V to V_{CC}				–10	µA
I_I	Input current, SENSE	TL7702B	V_I = V_{ref} to V_{CC} – 1.5 V			–0.1	–2	µA
I_{OH}	High-level output current, $\overline{RESET}$		V_O = 18 V				50	µA
I_{OL}	Low-level output current, RESET		V_O = 0				–50	µA
I_{CC}	Supply current		V_{SENSE} = 15 V,	RESIN ≥ 2 V		1.8	3	mA
V_{res}‡	Power-up reset voltage		$I_{OL}\overline{RESET}$ = 2 mA,	T_A = 25°C	1			V

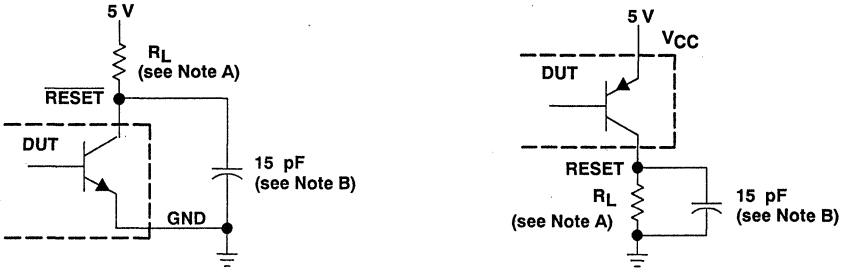
† All electrical characteristics are measured with 0.1-µF capacitors connected at REF, C_T, and V_{CC} to GND.
‡ This is the lowest value at which $\overline{RESET}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time from low-to-high-level output	$\overline{RESIN}$	RESET	See Figures 1, 2, and 3		270	500*	ns
t_{PHL}	Propagation delay time from high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$	See Figures 1, 2, and 3		270	500*	ns
$t_{w(min)}$	Pulse duration, minimum effective	$\overline{RESIN}$		See Figure 2(a)		150		ns
		SENSE		See Figure 2(b)		100		ns
t_r	Rise time		$\overline{RESET}$	See Figures 1, 2, and 3			75*	ns
t_f	Fall time					150	200*	ns
t_r	Rise time		RESET			75	150*	ns
t_f	Fall time						50*	ns

*For products compliant to MIL-STD-883, Class B, these parameters are not production tested.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. For I_{OL} and I_{OH}, R_L = 10 kΩ. For all switching characteristics, R_L = 511 Ω.
B. Includes jig and probe capacitance.

Figure 1. RESET and $\overline{\text{RESET}}$ Output Configurations

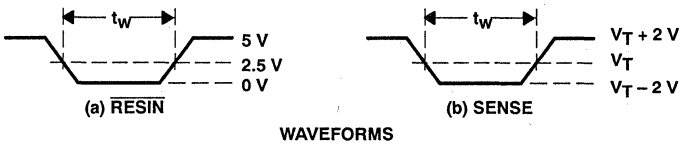


Figure 2. Input Pulse Definition

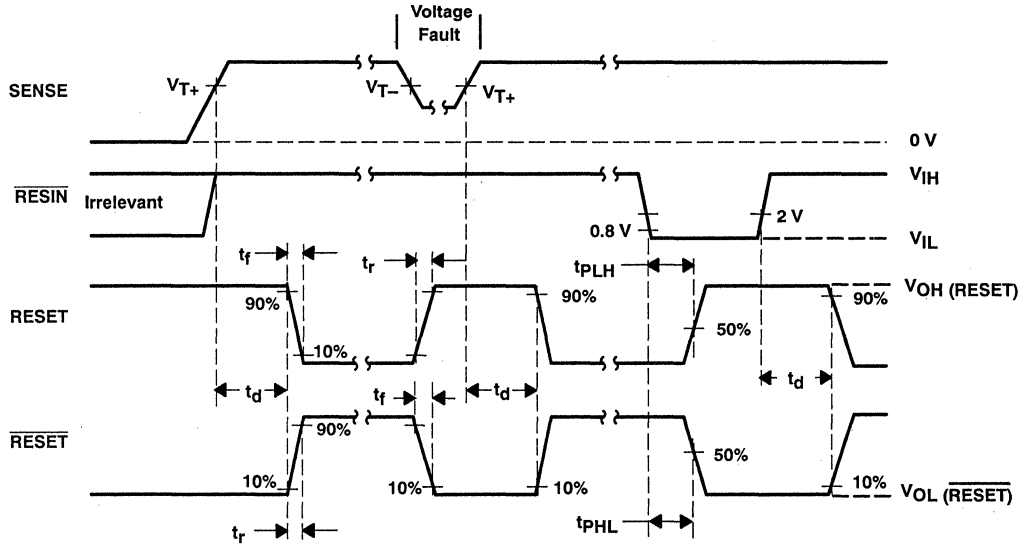
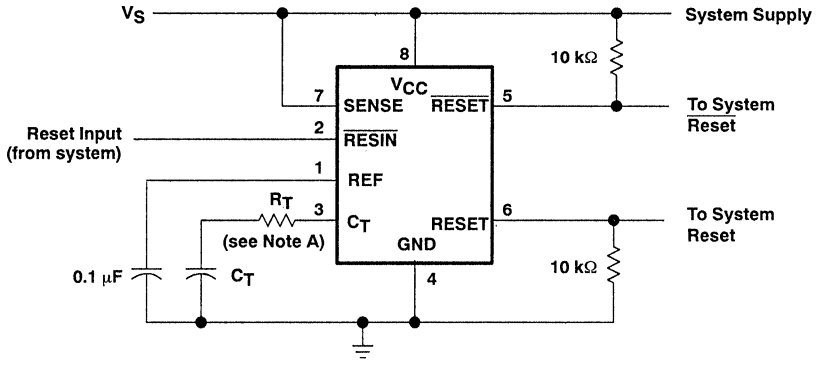


Figure 3. Voltage Waveforms

APPLICATION INFORMATION



NOTE A: When V_{CC} and SENSE are connected to the same point, it is recommended that series resistance (R_T) be added between the time delay programming capacitor (C_T) and the voltage supervisor device pin (C_T).

The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{T-}}{1 \times 10^{-3}}$$, where V_I = (the lesser of 7.1 V or V_S)

When this series resistor is used, the t_d calculation is as follows:

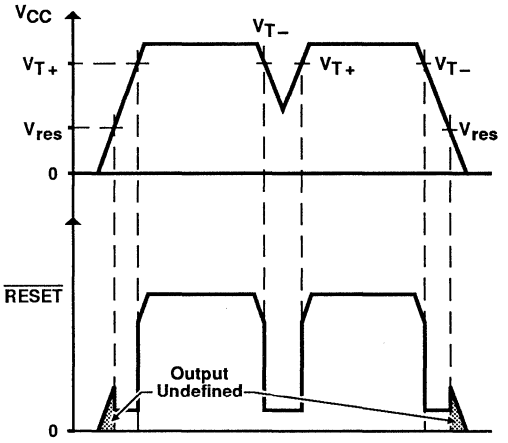
$$t_d = \frac{1.3 - [(1 \times 10^{-4}) \times R_T]}{1 \times 10^{-4}} \times C_T$$

Figure 4. System Reset Controller With Undervoltage Sensing

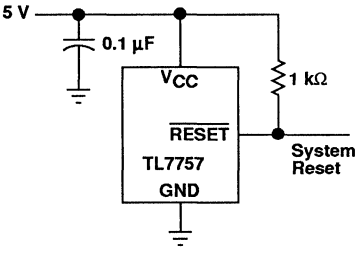
available features

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Low Standby Current . . . 20 µA
- Reset Output Defined When V_{CC} Exceeds 1 V
- Complementary Reset Output
- Precision Threshold Voltage 4.55 V ± 120 mV
- High Output Sink Capability . . . 20 mA
- Comparator Hysteresis Prevents Erratic Resets

TYPICAL TIMING DIAGRAM



TYPICAL APPLICATION DIAGRAM



description

The TL7757 is a monolithic supply voltage supervisor designed for use in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power-up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the $\overline{\text{RESET}}$ output becomes active (low) to prevent undefined operation. If at any time the supply voltage drops below threshold voltage level (V_{T-}), the $\overline{\text{RESET}}$ output goes to the active (low) level until the supply undervoltage fault condition is eliminated.

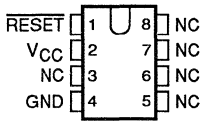
The C-suffix device is characterized for operation from 0°C to 70°C. The I-suffix device is characterized for operation from – 40°C to 85°C. The M-suffix device is characterized for operation from – 55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE			CHIP FORM (Y)
	SMALL-OUTLINE (D)	TO-226AA (LP)	SOT-89 (PK)	
0°C to 70°C	TL7757CD	TL7757CLP	TL7757CPK	TL7757Y
– 40°C to 85°C	TL7757ID	TL7757ILP	TL7757IPK	
– 55°C to 125°C	TL7757MD	TL7757MLP	———	

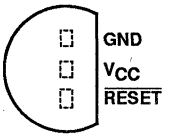
D and LP packages are available taped and reeled. Add "R" suffix to device type (e.g., TL7757CDR). Chips are tested at 25°C.

D PACKAGE
(TOP VIEW)

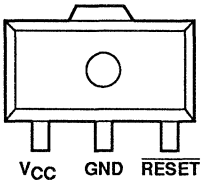


NC - No internal connection

LP PACKAGE
(TOP VIEW)



PK PACKAGE
(TOP VIEW)

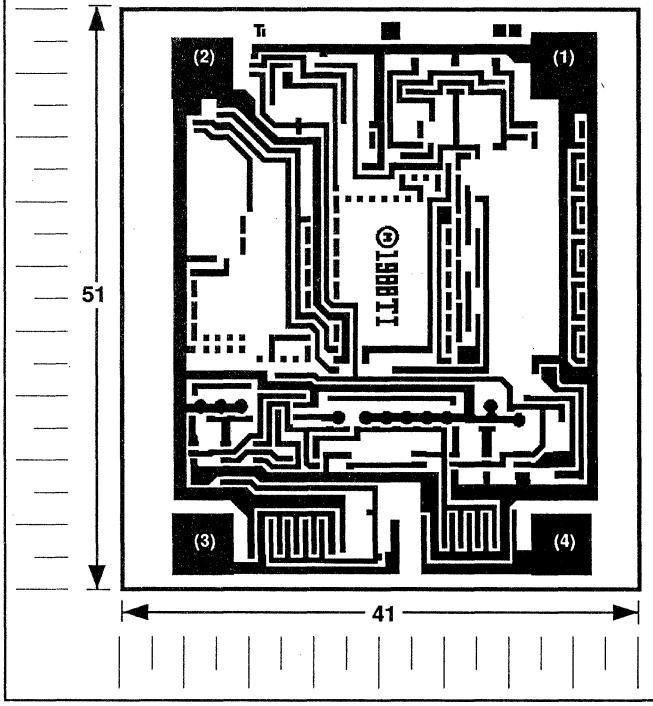


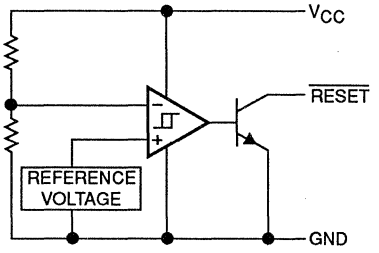
GND is in electrical contact with the tab.

TL7757Y chip information

These chips, properly assembled, display characteristics similar to the TL7757. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





BOND PAD ASSIGNMENTS

1 GND†
2 V_{CC}
3 NOT USED
4 $\overline{RESET}$

CHIP THICKNESS:
11 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALLIZATION

† Backside of chip has an internal electrical connection to pad 1.

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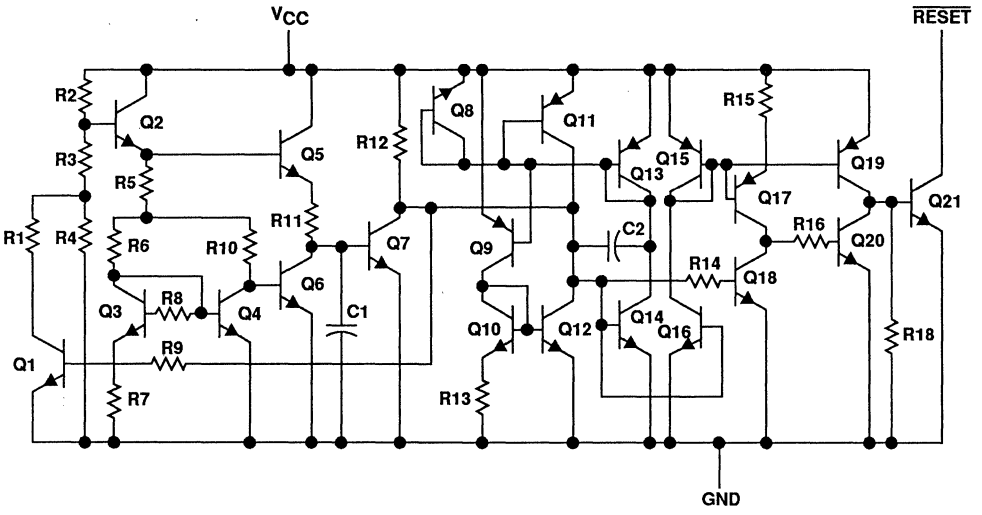
equivalent schematic



ACTUAL DEVICE COMPONENT COUNT	
Transistors	27
Resistors	20
Capacitors	2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.3 V to 20 V
Offstate output voltage range (see Note 1) . . . . . – 0.3 V to 20 V
Output current . . . . . 30 mA
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . – 40°C to 85°C
M-suffix . . . . . – 55°C to 125°C
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE	$T_A = 70°C$	$T_A = 85°C$	$T_A = 125°C$
D	725 mW	5.8 mW/°C	$T_A = 25°C$	464 mW	377 mW	145 mW
LP	775 mW	6.2 mW/°C	$T_A = 25°C$	496 mW	403 mW	155 mW
PK	500 mW	4.0 mW/°C	$T_A = 25°C$	320 mW	260 mW	100 mW
PK	3125 mW	25 mW/°C	$T_C = 25°C$	2000 mW	1625 mW	625 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	1	7	1	7	1	7	V
High-level output voltage, V_{OH}		15		15		15	V
Low-level output current, I_{OL}		20		20		20	mA
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

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electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{T-}	Threshold voltage (negative-going V_{CC})		25°C	4.43	4.55	4.67	V
			Full range	4.4		4.7	
V_{hys}‡	Hysteresis at V_{CC} input		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.1	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 4.7 to 7 V, V_{OL} = 15 V, See Figure 1	25°C			1	μA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 K, V_{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	μA
			Full range			2000	
		V_{CC} = 4.7 V to 7 V	25°C			40	
			Full range			45	

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		3.4	5	μs
			Full range			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	μs
			Full range			5	
t_r	Rise time	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		0.4	1	μs
			Full range			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	μs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C	5			μs
			Full range	5			

† Full range is 0°C to 70°C.
‡ This is the difference between positive-going input threshold voltage, V_{T+}, and negative-going input threshold voltage, V_{T-}.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{T-}	Threshold voltage (negative-going V_{CC})		25°C	4.43	4.55	4.67	V
			Full range	4.4		4.7	
V_{hys}‡	Hysteresis at V_{CC} input		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.1	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 4.7 to 7 V, V_{OL} = 15 V, See Figure 1	25°C			1	μA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 K, V_{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	μA
			Full range			2100	
		V_{CC} = 4.7 V to 7 V	25°C			40	
			Full range			45	

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		3.4	5	μs
			Full range			5	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5	μs
			Full range			5	
t_r	Rise time	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		0.4	1	μs
			Full range			1	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1	μs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C	5			μs
			Full range	5			

† Full range is –40°C to 85°C.
‡ This is the difference between positive-going input threshold voltage, VT+, and negative-going input threshold voltage, VT–.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{T-}	Threshold voltage (negative-going V_{CC})		25°C	4.43	4.55	4.67	V
			Full range	4.35		4.7	
V_{hys}‡	Hysteresis at V_{CC} input		25°C	40	50	60	mV
			Full range	30		70	
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V	25°C		0.1	0.8	V
			Full range			0.8	
I_{OH}	High-level output current	V_{CC} = 4.7 to 7 V, V_{OL} = 15 V, See Figure 1	25°C			1	μA
			Full range			1	
V_{res}§	Power-up reset voltage	R_L = 2.2 K, V_{CC} slew rate ≤ 5 V/μs	25°C		0.8	1	V
			Full range			1.2	
I_{CC}	Supply current	V_{CC} = 4.3 V	25°C		1400	2000	μA
			Full range			2500	
		V_{CC} = 4.7 V to 7 V	25°C			40	
			Full range			45	

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		3.4	5*	μs
			Full range			6*	
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3	25°C		2	5*	μs
			Full range			5*	
t_r	Rise time	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs	25°C		0.4	1*	μs
			Full range			1*	
t_f	Fall time	See Figures 2 and 3	25°C		0.05	1*	μs
			Full range			1	
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		25°C	5*			μs
			Full range	6*			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is –55°C to 125°C.
‡ This is the difference between positive-going input threshold voltage, V_{T+}, and negative-going input threshold voltage, V_{T-}.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T-}	Threshold voltage (negative-going V_{CC})		4.43	4.55	4.67	V
V_{hys}†	Hysteresis at V_{CC} input		40	50	60	mV
V_{OL}	Low-level output voltage	I_{OL} = 20 mA, V_{CC} = 4.3 V		0.1	0.8	V
I_{OH}	High-level output current	V_{CC} = 4.7 to 7 V, V_{OL} = 15 V, See Figure 1			1	μA
V_{res}‡	Power-up reset voltage	R_L = 2.2 K, V_{CC} slew rate ≤ 5 V/μs		0.8	1	V
I_{CC}	Supply current	V_{CC} = 4.3 V		1400	2000	μA
		V_{CC} = 4.7 V to 7 V			40	

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs		3.4	5	μs
t_{PHL}	Propagation delay time, high-to-low-level output	See Figures 2 and 3		2	5	μs
t_r	Rise time	See Figures 2 and 3, V_{CC} slew rate ≤ 5 V/μs		0.4	1	μs
t_f	Fall time	See Figures 2 and 3		0.05	1	μs
$t_{w(min)}$	Minimum pulse duration at V_{CC} for output response		5			μs

† This is the difference between positive-going input threshold voltage, V_{T+}, and negative-going input threshold voltage, V_{T-}.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

PARAMETER MEASUREMENT INFORMATION

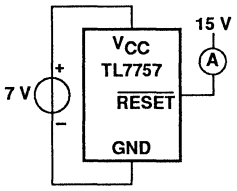
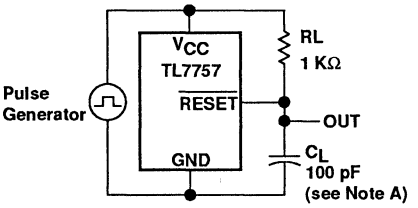
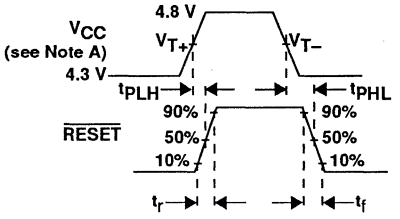


Figure 1. Test Circuit for Output Leakage Current



NOTE A: Includes jig and probe capacitance.

Figure 2. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics



NOTE A: V_{CC} slew rate ≤ 5 μs

Figure 3. Switching Diagram

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{CC}	Supply voltage	vs Output voltage	1
I_{CC}	Supply current	vs Supply voltage	2
		vs Temperature	3
V_{OL}	Low-level output voltage	vs Output current	4
		vs Temperature	5
I_{OL}	Output current	vs Supply voltage	6
V_{T-}	Threshold voltage (negative-going V_{CC})	vs Temperature	7
V_{res}	Power-up reset voltage	vs Temperature	8
			9
t_{PLH}	Propagation delay time low to high		10
t_{PHL}	Propagation delay time high to low		

TYPICAL CHARACTERISTICS†

SUPPLY VOLTAGE
vs
$\overline{\text{RESET}}$ OUTPUT VOLTAGE

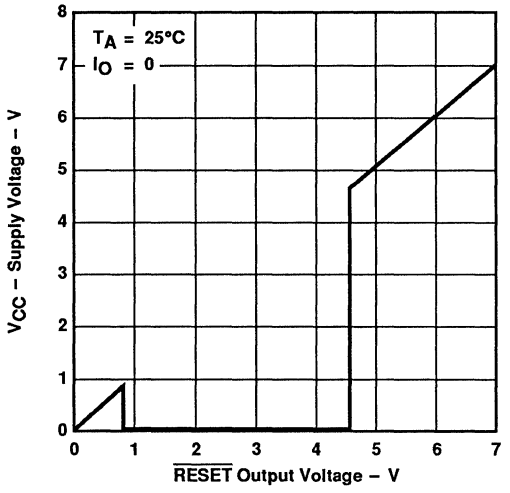


Figure 1

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

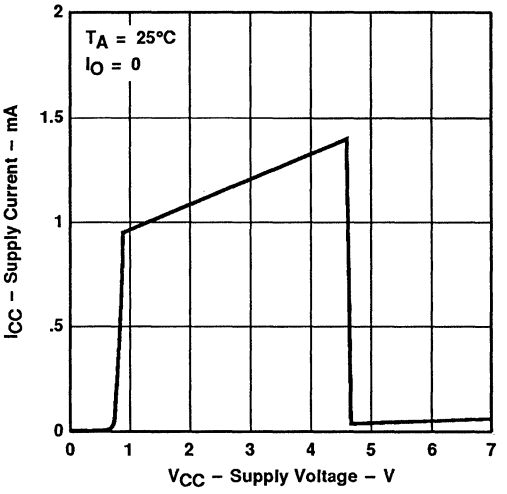


Figure 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

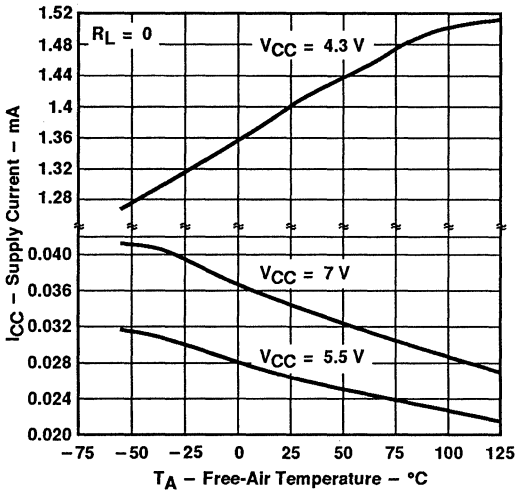


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

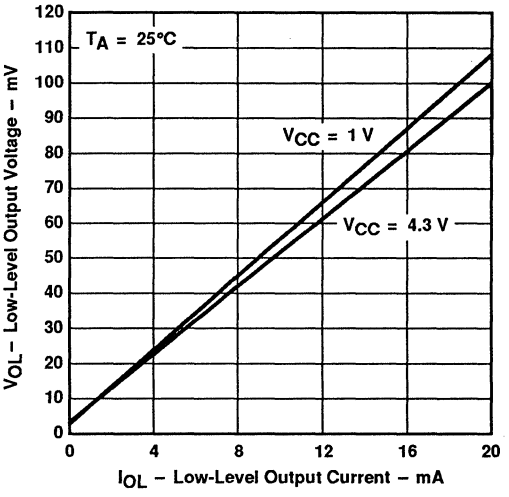


Figure 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

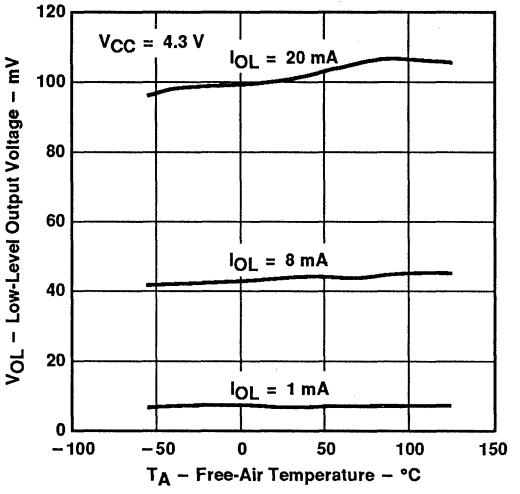


Figure 5

OUTPUT CURRENT
vs
SUPPLY VOLTAGE

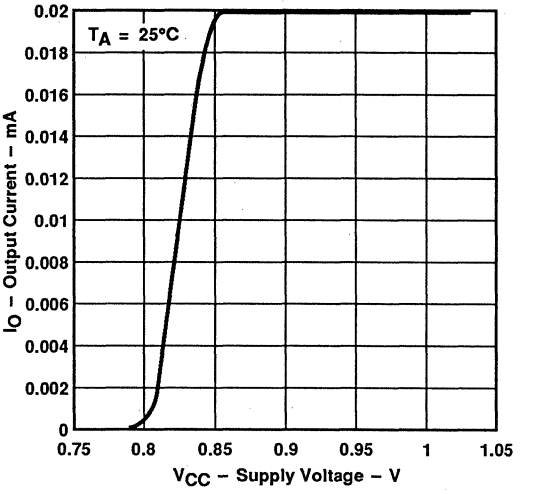


Figure 6

THRESHOLD VOLTAGE (NEGATIVE GOING V_{CC})
vs
FREE-AIR TEMPERATURE

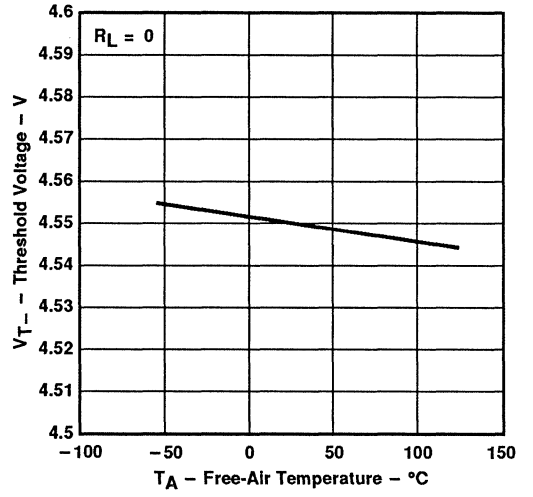


Figure 7

POWER-UP RESET VOLTAGE
vs
FREE-AIR TEMPERATURE

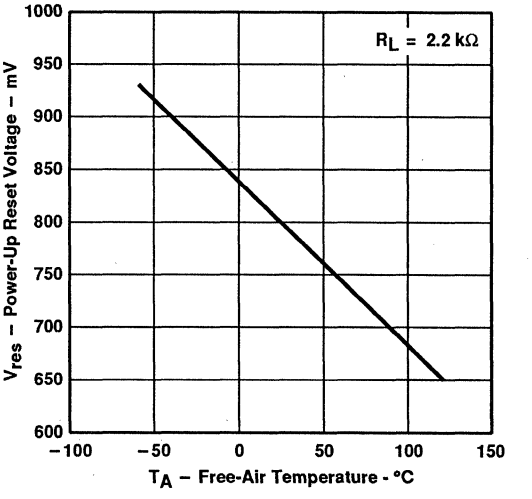


Figure 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

POWER-UP RESET VOLTAGE

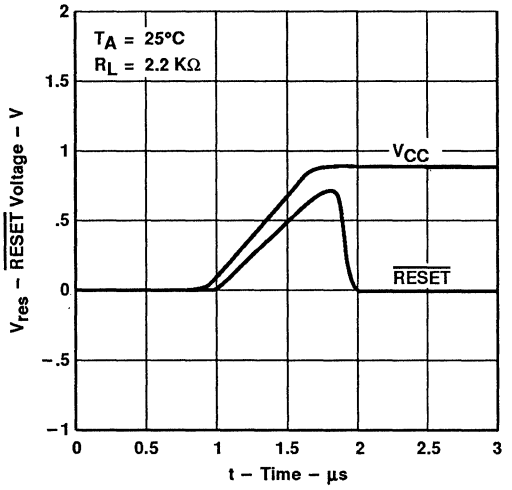


Figure 9

PROPAGATION DELAY

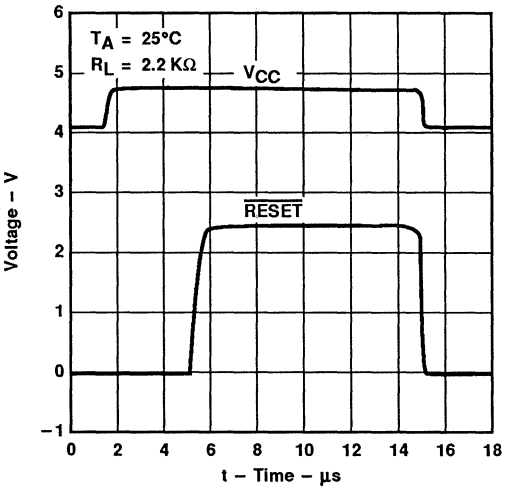
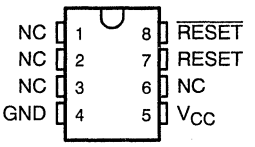


Figure 10

D3905, JANUARY 1991–REVISED SEPTEMBER 1991

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Threshold Voltage**
  4.55 V ±120 mV
- **Low Standby Current . . . 20 μA**
- **Reset Outputs Defined When V_{CC} Exceeds 1 V**
- **True and Complementary Reset Outputs**
- **Wide Operating Temperature Range**
  0°C to 70°C
- **Wide Supply Voltage Range . . . 1 V to 7 V**

D OR P PACKAGE
(TOP VIEW)



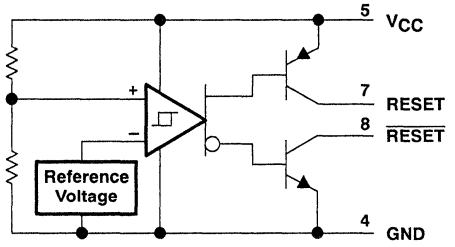
NC – No internal connection

description

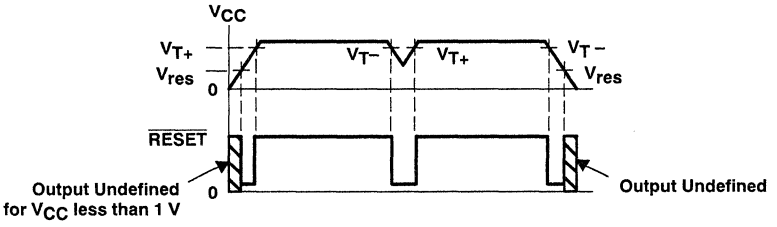
The TL7759C is a monolithic supply voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power-up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. If at any time the supply voltage drops below the threshold voltage level (V_{T-}), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value.

The TL7759C is characterized for operation from 0°C to 70°C.

functional block diagram



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Off-state output voltage range: $\overline{\text{RESET}}$ voltage ..... −0.3 V to 20 V
RESET voltage ..... −0.3 V to 20 V
Low-level output current, I_{OL} ($\overline{\text{RESET}}$) ..... 30 mA
High-level output current, I_{OH} (RESET) ..... −10 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
Output voltage, V_O (see Note 2)	Transistor off $\overline{\text{RESET}}$ voltage		15	V
	Transistor off RESET voltage	0		
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		24	mA
High-level output current, I_{OH}	RESET		−8	
Operating free-air temperature, T_A		0	70	°C

NOTE 2: RESET output must not be pulled down below GND potential.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4	0.8	V
V_{OH}	High-level output voltage	RESET		I_{OH} = −8 mA	V_{CC}−1			
V_{T-}	Threshold voltage (negative-going V_{CC})		T_A = 25°C		4.43	4.55	4.67	V
			T_A = 0°C to 70°C		4.4		4.7	
V_{res}‡	Power-up reset voltage		R_L = 2.2 kΩ	T_A = 25°C		0.8	1	V
				T_A = 0°C to 70°C			1.2	
V_{hys}§	Hysteresis at V_{CC} input		T_A = 25°C		40	50	60	mV
			T_A = 0°C to 70°C		30		70	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_{CC} = 7 V, See Figure 1	V_{OH} = 15 V			1	μA
I_{OL}	Low-level output current	RESET		V_{OL} = 0 V			−1	
I_{CC}	Supply current		No load	V_{CC} = 4.3 V		1400	2000	μA
				V_{CC} = 5.5 V			40	

† Typical values are at T_A = 25°C.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≥ 5 V/μs.
§ This is the difference between positive-going input threshold voltage, V_{T+}, and negative-going input threshold voltage, V_{T-}.

switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC}	RESET	See Figures 2 and 3†			5	μs
t_{PHL}	Propagation delay time, high-to-low-level output	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4			5	
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 2 and 4†			1	
t_f	Fall time		$\overline{\text{RESET}}$	See Figures 2 and 4			1	
$t_{w(min)}$	Minimum pulse duration	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4	5			

† V_{CC} slew rate > 5 V/μs.

PARAMETER MEASUREMENT INFORMATION

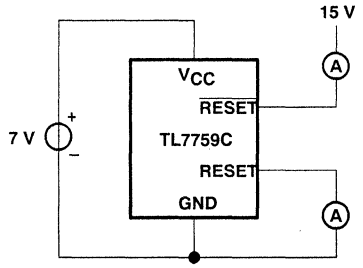
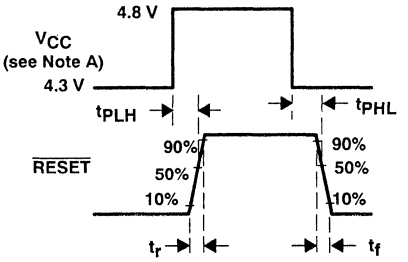
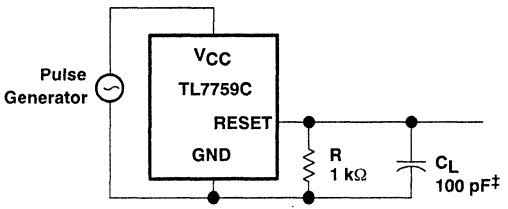


Figure 1. Test Circuit for Output Leakage Current



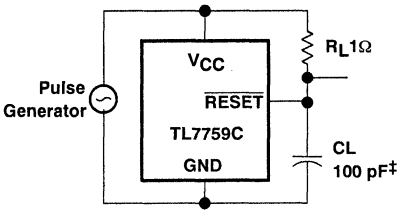
NOTE A: V_{CC} slew rate > 5 V/μs.

Figure 2. Switching Diagram



‡Includes jig and probe capacitance

Figure 3. Test Circuit for RESET Output Switching Characteristics



‡Includes jig and probe capacitance

Figure 4. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics

APPLICATION INFORMATION

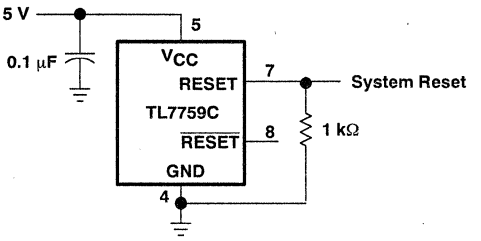
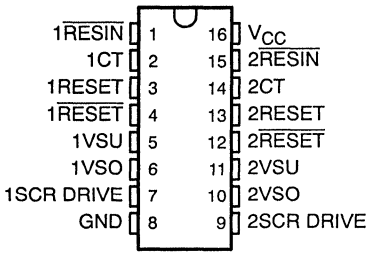


Figure 5. Power Supply System Reset Generation

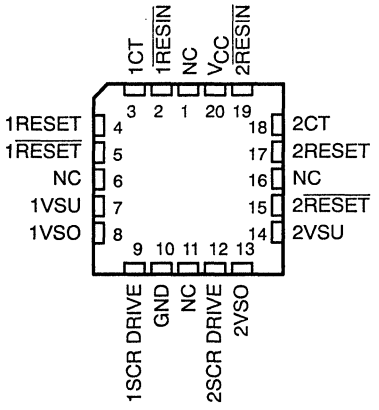
D3035, OCTOBER 1987–REVISED NOVEMBER 1991

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **Wide Supply Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TL7770 is a monolithic integrated circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU pins, respectively. When V_{CC} attains the minimum voltage of 1 V during power-up, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the delay timer function activates latching RESET and $\overline{\text{RESET}}$ active (high and low, respectively) for a time delay, t_d, after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low activates the time delay function, RESET and $\overline{\text{RESET}}$, during normal system voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value V_{T+} for a time delay, t_d, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

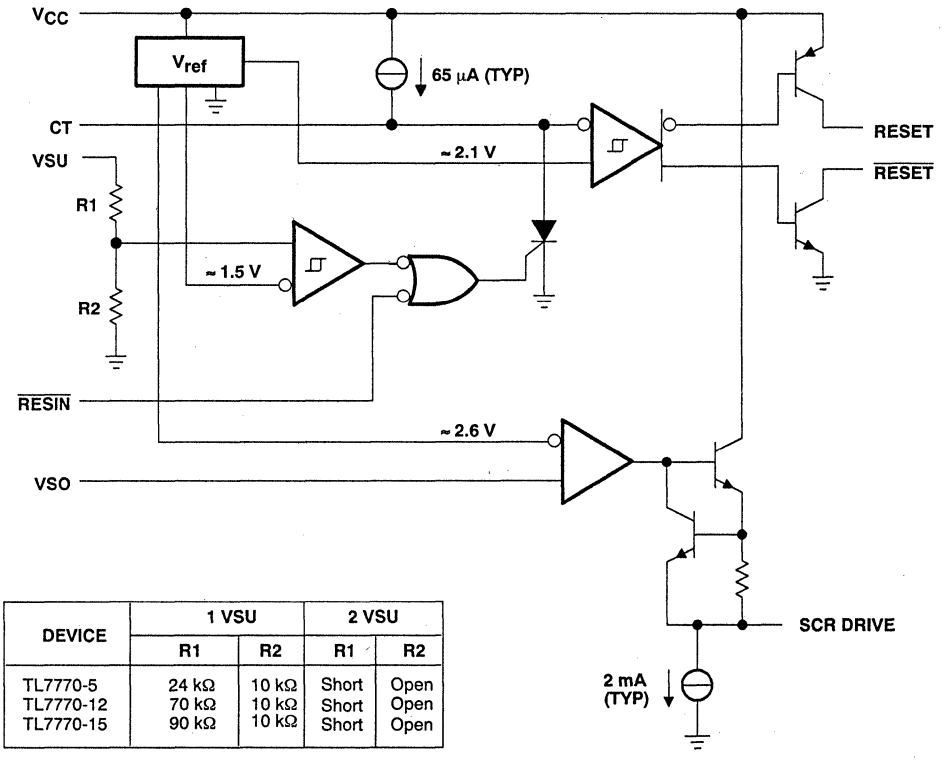
The overvoltage-detection circuit is programmable for a wide range of user designs. During an overvoltage condition, an internal SCR is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive pin, which can be used to drive an external high-current SCR gate or an overvoltage warning circuit.

The TL7770C is characterized for operation from 0°C to 70°C. The TL7770M series is characterized for operation from −55°C to 125°C. The TL7770Q series is characterized for operation from −40°C to 125°C.

AVAILABLE OPTIONS

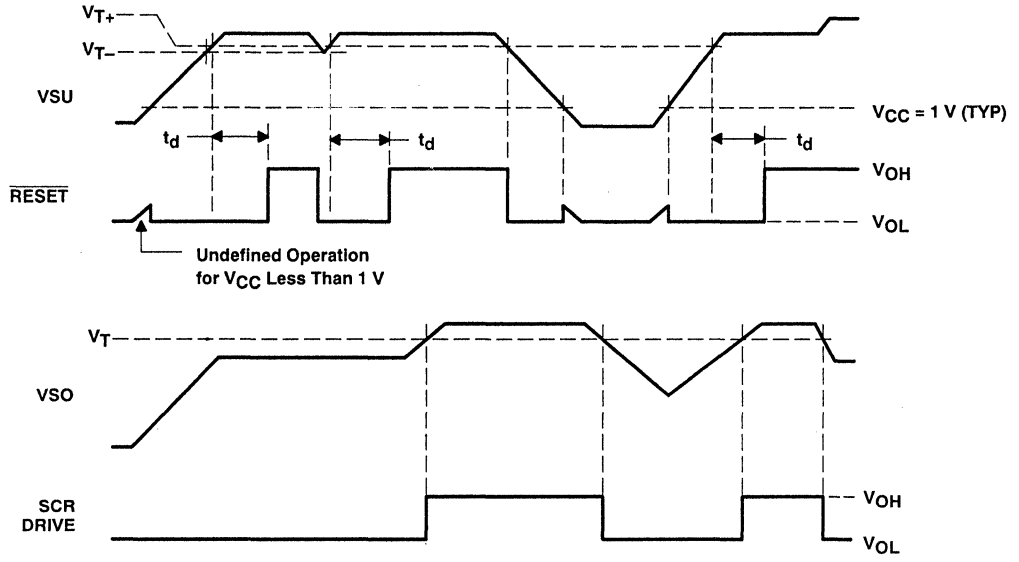
T_A	PACKAGE			
	SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TL7770-5CDW TL7770-12CDW TL7770-15CDW			TL7770-5CN TL7770-12CN TL7770-15CN
–40°C to 125°C	TL7770-5QDW TL7770-12QDW TL7770-15QDW			TL7770-5QN TL7770-12QN TL7770-15QN
–55°C to 125°C		TL7770-5MFK TL7770-12MFK TL7770-15MFK	TL7770-5MJ TL7770-12MJ TL7770-15MJ	

logic diagram (each channel)



DEVICE	1 VSU		2 VSU	
	R1	R2	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open
TL7770-15	90 kΩ	10 kΩ	Short	Open

typical timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO ..... –0.3 V to 18 V
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL} ..... 20 mA
High-level output current (1RESET and 2RESET), I_{OH} ..... –20 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL7770_C ..... 0°C to 70°C
TL7770_M ..... –55°C to 125°C
TL7770–Q ..... –40°C to 125°C
Operating virtual junction temperature range ..... –40°C to 150°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 2)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage (1CT and 2CT), V_O			5	V
High-level input voltage range, V_{IH}, $1\overline{RESIN}$, $2\overline{RESIN}$		2	18	V
Low-level input voltge range, V_{IL}, $1\overline{RESIN}$, $2\overline{RESIN}$		0	0.8	V
Output sink current (1CT and 2CT), I_O			50	μA
High-level output current (1RESET and 2RESET), I_{OH}			−16	mA
Low-level output current ($1\overline{RESET}$ and $2\overline{RESET}$, I_{OL}			16	mA
Continuous output current (1SCR DRIVE and 2SCR DRIVE), I_O			25	mA
Operating free-air temperature, T_A	TL7770C Series	0	70	°C
	TL7770M Series	−55	125	
	TL7770Q Series	−40	125	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	RESET	I_{OH} = −15 mA	V_{CC}−1.5			V
		SCR DRIVE	I_{OH} = −20 mA	V_{CC}−1.5			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{T-}	Undervoltage threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
		TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
		TL7770-5 (5-V sense, 1VSU)		4.46		4.64	
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-15 (15-V sense, 1VSU)		13.36		13.91	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{T+} - V_{T-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-15 (15-V sense, 1VSU)			45		
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
			T_A = MIN to MAX	2.48		2.68	
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			−10	μA
		VSO	V_I = 2.4 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	μA
I_{OL}	Low-level output current	RESET	V_O = 0			−50	μA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

total device

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{res}§	Power-up reset voltage	V_{CC}	V_{OL} = 0.4 V, I_{OL} = 1 mA		0.8	1	V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	RESET	I_{OH} = −15 mA	V_{CC}−1.5			V
		SCR DRIVE	I_{OH} = −20 mA	V_{CC}−1.5			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
V_{T-}	Undervoltage threshold at VSU (negative-going)	TL7770-5M (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.632	V
		TL7770-12M (12-V sense, 1VSU)		10.8	10.9	11.07	
		TL7770-15M (15-V sense, 1VSU)		13.5	13.64	13.866	
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)		1.485	1.5	1.527	
		TL7770-5M (5-V sense, 1VSU)	T_A = −55°C TO 125°C	4.4		4.646	
		TL7770-12M (12-V sense, 1VSU)		10.62		11.12	
		TL7770-15M (15-V sense, 1VSU)		13.36		13.916	
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)		1.47		1.542	
V_{hys}	Hysteresis at VSU ($V_{T+} - V_{T-}$)	TL7770-5M (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7770-12M (12-V sense, 1VSU)			36		
		TL7770-15M (15-V sense, 1VSU)			45		
		TL7770-5M, TL7770-12M, TL7770-15M (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5M, TL7770-12M, TL7770-15M (VSO)	T_A = 25°C	2.53	2.58	2.63	V
			T_A = MIN to MAX	2.48		2.68	
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			−10	μA
		VSO	V_I = 2.4 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = V_{CC}			50	μA
I_{OL}	Low-level output current	RESET	V_O = 1			−50	μA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

total device

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
I_{CC} Supply current	1VSU 18 V, 2 VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
		T_A = MIN to MAX			6.5	

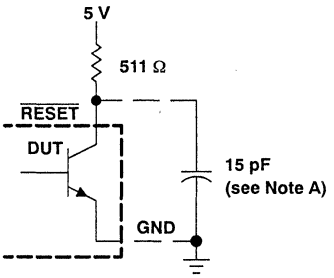
† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, CT open, T_A = 25°C

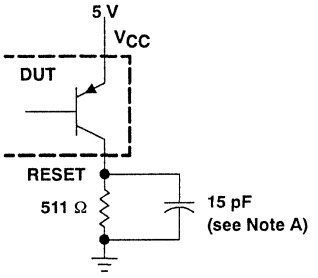
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{RESIN}$	RESET	See Figure 1		270	500*	ns
t_{PLH}	Propagation delay time, high-to-low-level output	$\overline{RESIN}$	$\overline{RESET}$			270	500*	ns
t_r	Rise time		RESET				75*	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{RESET}$			75		ns
t_f	Fall time						50*	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{RESIN}$		See Figure 2(a)		150		ns
		VSU		See Figure 2(b)		100		

*On products compliant to MIL-STD-883, Class B, parameters are not production tested.

PARAMETER MEASUREMENT INFORMATION



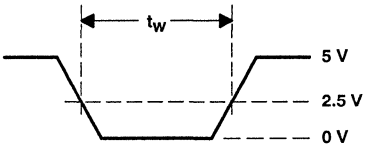
$\overline{RESET}$ OUTPUT CONFIGURATION



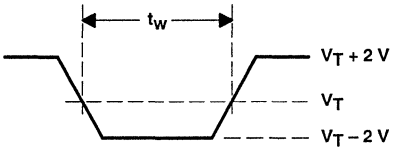
RESET OUTPUT CONFIGURATION

NOTE A: Include jig and probe capacitance.

Figure 1. RESET and $\overline{RESET}$ Output Configurations



(a) $\overline{RESIN}$

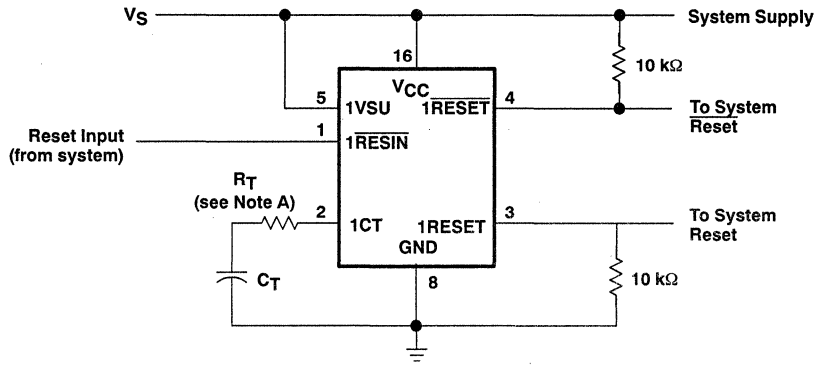


(b) VSU

WAVEFORMS

Figure 2. Input Pulse Definition

APPLICATION INFORMATION



Pin numbers shown are for the DW, J, and N packages.

NOTE A: When V_{CC} and 1VSU are connected to the same point, it is recommended that series resistance (R_T) be added between the time delay programming capacitor (C_T) and the voltage supervisor device pin (1CT).

The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{T-}}{1 \times 10^{-3}}, \text{ where } V_I = \text{(the lesser of 7.1 V or } V_S\text{)}$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - [(1 \times 10^{-4}) \times R_T]}{6.5 \times 10^{-4}} \times C_T$$

Figure 3. System Reset Controller With Undervoltage Sensing

D3824, MARCH 1991, REVISED JUNE 1991

- **2.5-V Virtual Ground for 5-V/GND Analog Systems**
- **Self-Contained in Small Outline, Dual-In-Line or 3-Terminal TO-226AA Packages**
- **High Output-Current Capability**
  Sink or Source . . . 20 mA Typ
- **Micropower Operation . . . 170 µA Typ**
- **Excellent Regulation Characteristics**
  Output Regulation = ±45 µV Typ,
  I_O = 0 to ±10mA
  Input Regulation = 1.5 µV/V Typ
- **Low-Impedance Output . . . 0.0075 Ω Typ**
- **Macromodel Included**

description

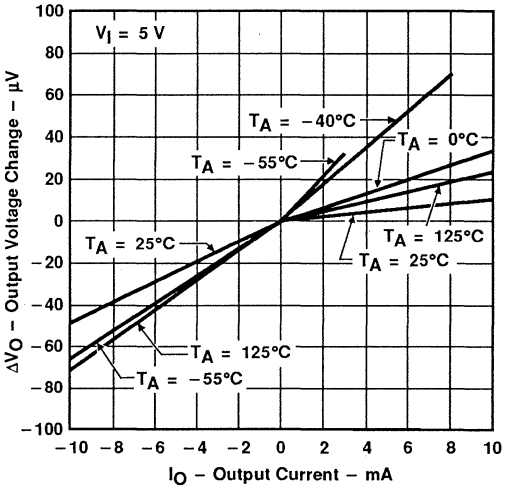
In signal-conditioning applications using a single power source, a reference voltage is required for termination of all signal grounds. To accomplish this, engineers have typically used solutions consisting of resistors, capacitors, operational amplifiers, and voltage references. Texas Instruments has eliminated all of those components with one easy-to-use 3-terminal device. That device is the TLE2425 precision virtual ground.

Use of the TLE2425 over other typical circuit solutions gives the designer increased dynamic signal range, improved signal-to-noise ratio, lower distortion, improved signal accuracy, and easier interfacing to ADCs and DACs. These benefits are the result of combining a precision micropower voltage reference and a high-performance precision operational amplifier in a single silicon chip. It is the precision and performance of these two circuit functions together that yield such dramatic system-level performance.

The TLE2425 improves input regulation as well as output regulation, and in addition reduces output impedance and power dissipation in a majority of virtual-ground-generation circuits. Both input regulation and load regulation exceed 12 bits of accuracy on a single 5-V system. Signal-conditioning front-ends of data acquisition systems that push 12 bits and beyond can use the TLE2425 to eliminate a major source of system error.

The TLE2425C is characterized for operation from 0°C to 70°C. The TLE2425I is characterized for operation from –40°C to 85°C. The TLE2425M is characterized for operation over the full military temperature range of –55°C to 125°C.

OUTPUT REGULATION

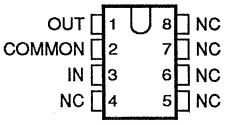


AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC TO-226AA (LP)	CHIP FORM (Y)
0°C to 70°C	TLE2425CD	———	TLE2425CLP	TLE2425Y
–40°C to 85°C	TLE2425ID	———	TLE2425ILP	
–55°C to 125°C	TLE2425MD	TLE2425MJG	TLE2425MLP	

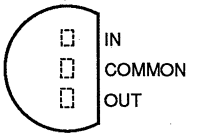
D and LP packages are available taped and reeled in the commercial temperature range only. Add "R" suffix to device type (e.g., TLE2425CDR).

D OR JG PACKAGE
(TOP VIEW)



NC – No internal connection

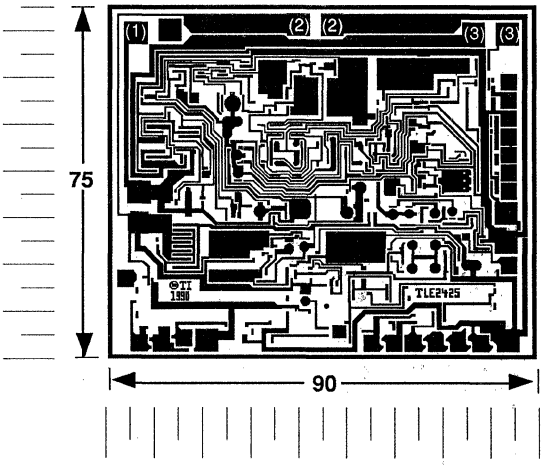
LP PACKAGE
(TOP VIEW)

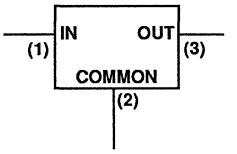


TLE2425Y chip information

These chips, properly assembled, display characteristics similar to the TLE2425, (see electrical table on TLE2425Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

Note: Both number-2 bonding pads and both number-3 bonding pads must be bonded out to the corresponding pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage . . . . . 40 V
Output current, I_O . . . . . ±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
M-suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package . . . . . 300°C

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	155 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	μA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	μV
			Full range			25	
	V_I = 4 V to 40 V		25°C		1.5	20	μV/V
			Full range			25	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to –10 mA		25°C	–160	–45	160	μV
			Full range	–250		250	
	I_O = 0 to –20 mA		25°C	–450	–150	450	
Output regulation‡ (sink current)	I_O = 0 to 10 mA		25°C	–160	15	160	μV
			Full range	–250		250	
	I_O = 0 to 20 mA		25°C	–235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			–30	–50		
Output noise voltage, rms	f =10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		μs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is 0°C to 70°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	μA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	μV
			Full range			75	
	V_I = 4 V to 40 V		25°C		1.5	20	μV/V
			Full range			75	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to −10 mA		25°C	−160	−45	160	μV
			Full range	−250		250	
	I_O = 0 to −20 mA		25°C	−450	−150	450	
Output regulation‡ (sink current)	I_O = 0 to 8 mA		25°C	−160	15	160	μV
			Full range	−250		250	
	I_O = 0 to 20 mA		25°C	−235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			−30	−50		
Output noise voltage, rms	f = 10 Hz to 10 kHz		25°C		100		μV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		μs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		μs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		μs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is −40°C to 85°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.48	2.5	2.52	V
			Full range	2.47		2.53	
Temperature coefficient of output voltage			25°C		20		ppm/°C
Bias current	I_O = 0		25°C		170	250	µA
			Full range			250	
Input regulation	V_I = 4.5 V to 5.5 V		25°C		1.5	20	µV
			Full range			100	
	V_I = 4.5 V to 40 V		25°C		1.5	20	µV/V
			Full range			100	
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V		25°C		80		dB
Output regulation‡ (source current)	I_O = 0 to –10 mA		25°C	–160	–45	160	µV
			Full range	–250		250	
	I_O = 0 to –20 mA		25°C	–450	–150	450	
Output regulation‡ (sink current)	I_O = 0 to 3 mA		25°C	–160	15	160	µV
			Full range	–250		250	
	I_O = 0 to 20 mA		25°C	–235	65	235	
Long-term drift of output voltage	Δt = 1000 h, Noncumulative		25°C		15		ppm
Output impedance			25°C		7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		25°C	30	55		mA
	Source current, V_O = 0			–30	–50		
Output noise voltage, rms	f =10 Hz to 10 kHz		25°C		100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		110		µs
		C_L = 100 pF			115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0			180		
		C_L = 100 pF			180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%		25°C		12		µs
	V_I = 4.5 to 5.5 V, V_O to 0.01%				30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%		25°C		125		µs
	V_I = 0 to 5 V, V_O to 0.01%				210		

†Full range is –55°C to 125°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at V_I = 5 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage			2.48	2.5	2.52	V
Temperature coefficient of output voltage				20		ppm/°C
Bias current	I_O = 0			170	250	µA
Input regulation	V_I = 4.5 V to 5.5 V			1.5	20	µV
	V_I = 4 V to 40 V			1.5	20	µV/V
Ripple rejection	f = 120 Hz, $\Delta V_{I(PP)}$ = 1 V			80		dB
Output regulation (source current)‡	I_O = 0 to –10 mA		–160	–45	160	µV
	I_O = 0 to –20 mA		–450	–150	450	
Output regulation (sink current)‡	I_O = 0 to 10 mA		–160	15	160	µV
	I_O = 0 to 20 mA		–235	65	235	
Output impedance				7.5	22.5	mΩ
Short-circuit output current	Sink current, V_O = 5 V		30	55		mA
	Source current, V_O = 0		–30	–50		
Output noise voltage, rms	f =10 Hz to 10 kHz			100		µV
Output voltage response to output current step	V_O to 0.1%, I_O = ± 10 mA	C_L = 0		110		µs
		C_L = 100 pF		115		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0		180		
		C_L = 100 pF		180		
Output voltage response to input voltage step	V_I = 4.5 to 5.5 V, V_O to 0.1%			12		µs
	V_I = 4.5 to 5.5 V, V_O to 0.01%			30		
Output voltage turn-on response	V_I = 0 to 5 V, V_O to 0.1%			125		µs
	V_I = 0 to 5 V, V_O to 0.01%			210		

‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

TYPICAL CHARACTERISTICS

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Output voltage	Distribution	1
	vs Temperature	2
Output voltage hysteresis	vs Temperature	3
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Input regulation		6
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Output regulation		8
Output impedance	vs Frequency	9
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Spot noise voltage	vs Frequency	11
Wideband noise voltage	vs Frequency	12
Output voltage change with current step	vs Time	13
Output voltage change with voltage step	vs Time	14
Output voltage power-up response	vs Time	15
Stability range	vs Load capacitance	16

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF
OUTPUT VOLTAGE

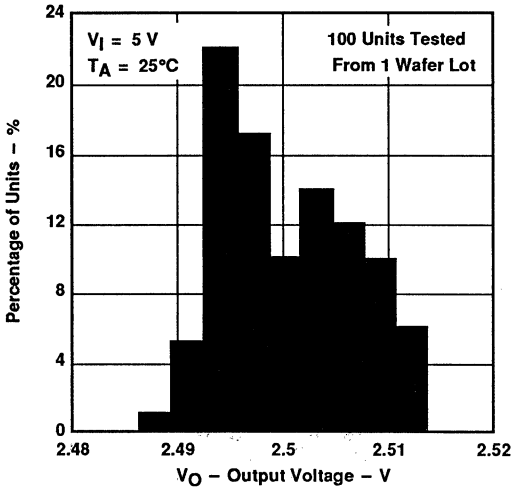


Figure 1

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

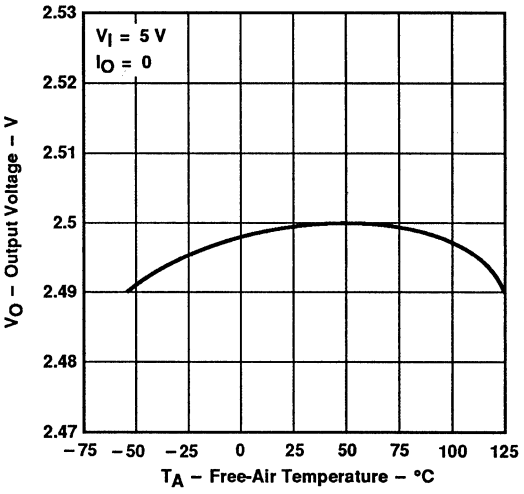


Figure 2

OUTPUT VOLTAGE HYSTERESIS
vs
FREE-AIR TEMPERATURE

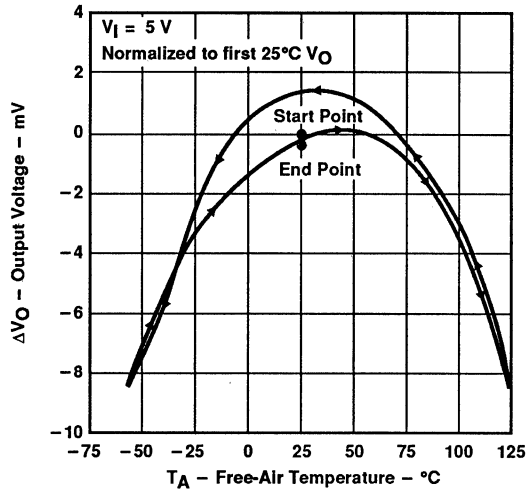


Figure 3

BIAS CURRENT
vs
INPUT VOLTAGE

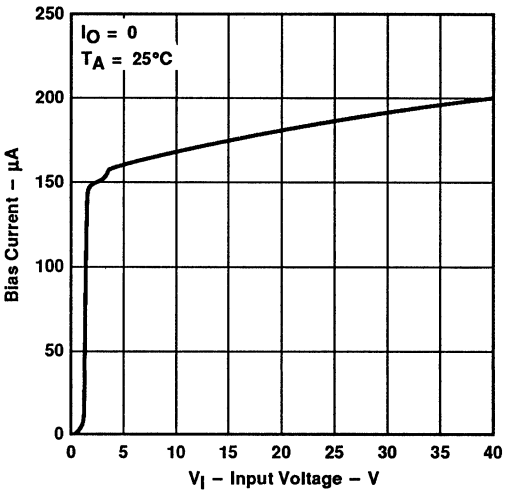


Figure 4

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

BIAS CURRENT vs FREE-AIR TEMPERATURE

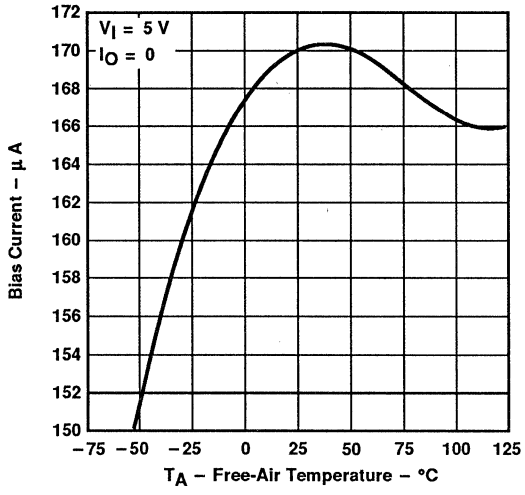


Figure 5

INPUT REGULATION

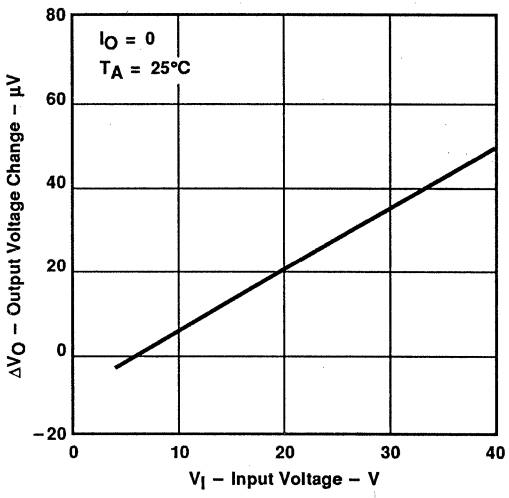


Figure 6

RIPPLE REJECTION vs FREQUENCY

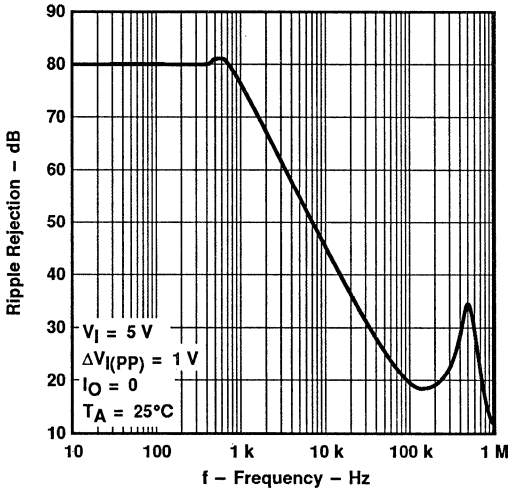


Figure 7

OUTPUT REGULATION

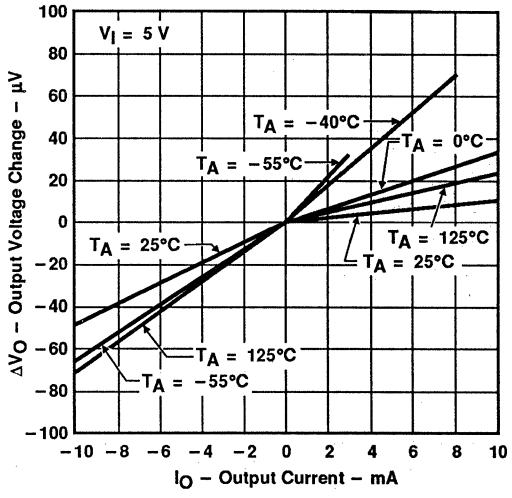


Figure 8

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE
vs
FREQUENCY

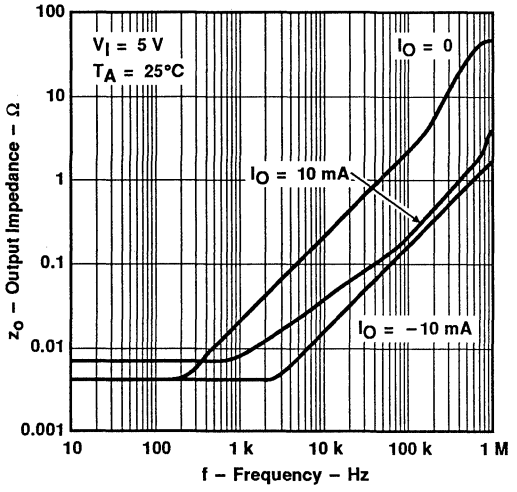


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

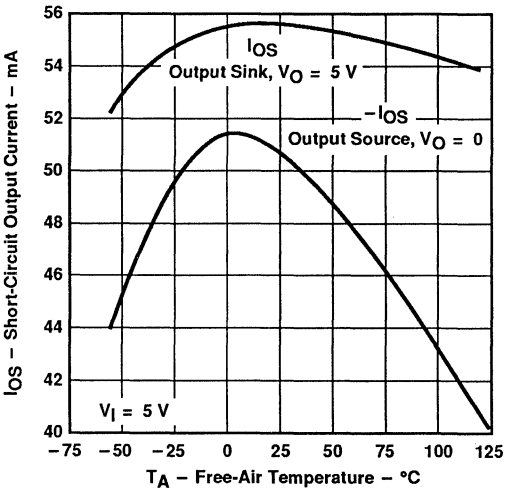


Figure 10

SPOT NOISE VOLTAGE
vs
FREQUENCY

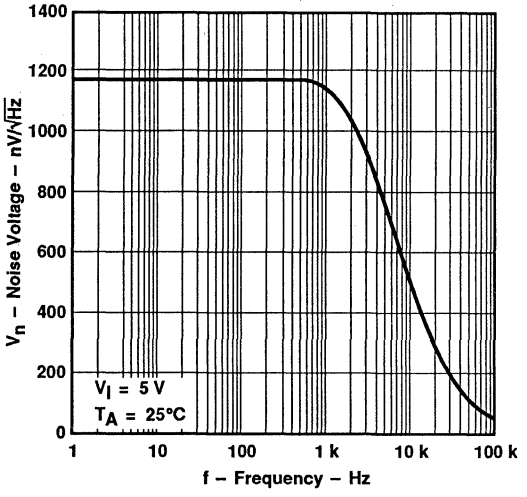


Figure 11

WIDEBAND NOISE VOLTAGE
vs
FREQUENCY

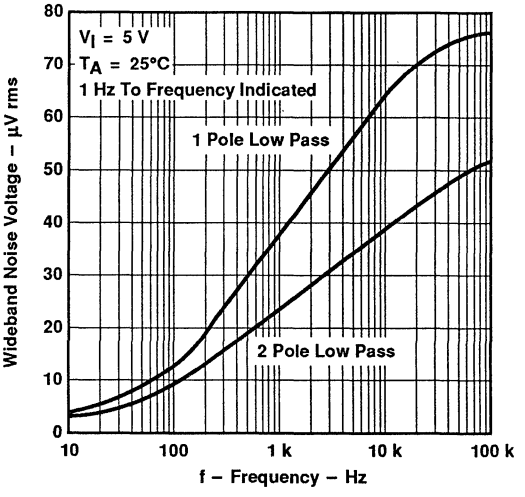


Figure 12

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RESPONSE
TO OUTPUT CURRENT STEP
vs
TIME

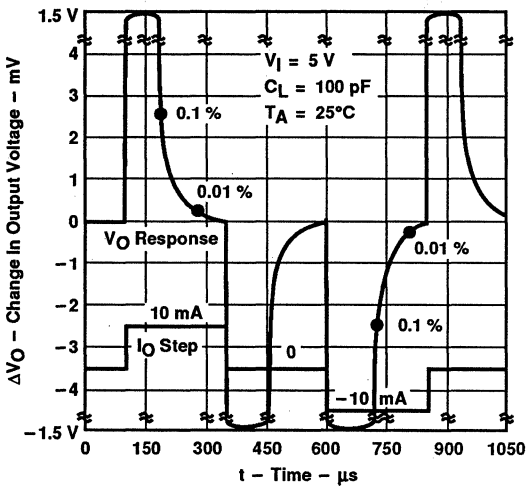


Figure 13

OUTPUT VOLTAGE RESPONSE
TO INPUT VOLTAGE STEP
vs
TIME

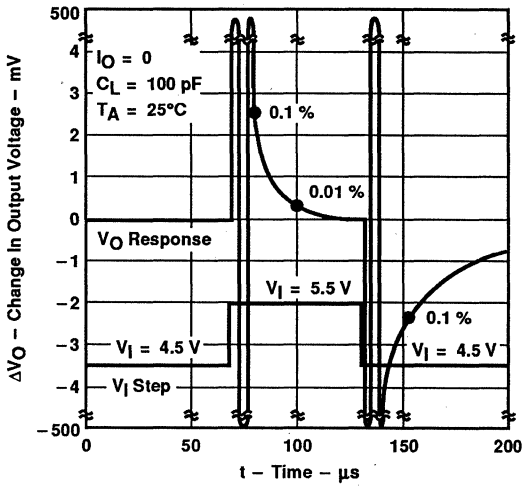


Figure 14

OUTPUT VOLTAGE POWER-UP RESPONSE
vs
TIME

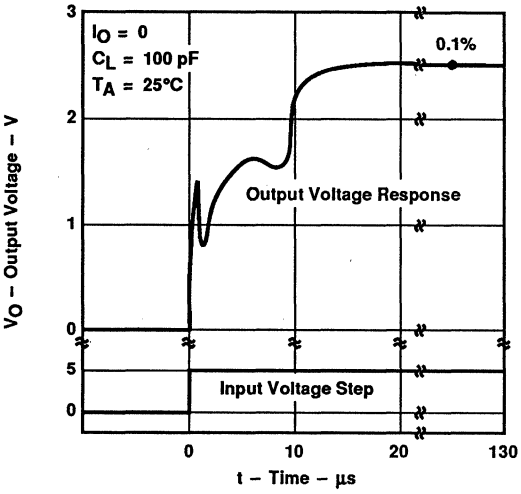


Figure 15

STABILITY RANGE
vs
LOAD CAPACITANCE

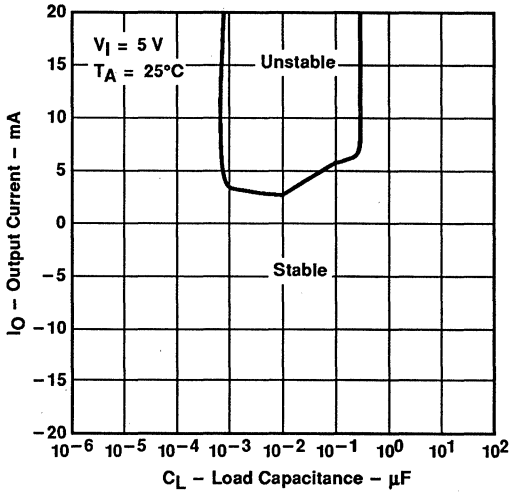


Figure 16

macromodel information

```
* TLE2425 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
* REV (N/A)       SUPPLY VOLTAGE: 5 V
* CONNECTIONS:    INPUT
*                 | COMMON
*                 | | OUTPUT
*                 | | |
.SUBCKT TLE2425   3 4 5
*
*--------------------------------------------------------------------------------
* OPAMP SECTION
  C1       11    12    21.66E-12
  C2        6     7    30.00E-12
  C3       87     0    10.64E-9
  CPSR     85    86    15.9E-9
  DCM+     81    82    DX
  DCM-     83    81    DX
  DC        5    53    DX
  DE       54     5    DX
  DLP      90    91    DX
  DLN      92    90    DX
  DP        4     3    DX
  ECMR     84    99    (2,99) 1
  EGND     99     0    POLY(2) (3,0) (4,0) 0 .5 .5
  EPSR     85     0    POLY(1) (3,4) -16.22E-6  3.24E-6
  ENSE     89     2    POLY(1) (88,0) 120E-6  1
  FB        7    99    POLY(6) VB VC VE VLP VLN VPSR 0 74.8E6 -10E6 10E6 10E6
+ -10E6 74E6
  GA        6     0    11 12 320.4E-6
  GCM       0     6    10 99 1.013E-9
  GPSR     85    86    (85,86) 100E-6
  GRC1      4    11    (4,11) 3.204E-4
  GRC2      4    12    (4,12) 3.204E-4
  GRE1     13    10    (13,10) 1.038E-3
  GRE2     14    10    (14,10) 1.038E-3
  HLIM     90     0    VLIM 1K
  HCMR     80     1    POLY(2) VCM+ VCM- 0 1E2 1E2
  IRP       3     4    146E-6
  IEE       3    10    DC 24.05E-6
  IIO       2     0    .2E-9
  I1       88     0    1E-21
  Q1       11    89    13 QX
  Q2       12    80    14 QX
  R2        6     9    100.0E3
  RCM      84    81    1K
  REE      10    99    8.316E6
  RN1      87     0    2.55E8
  RN2      87    88    11.67E3
```

macromodel information (continued)

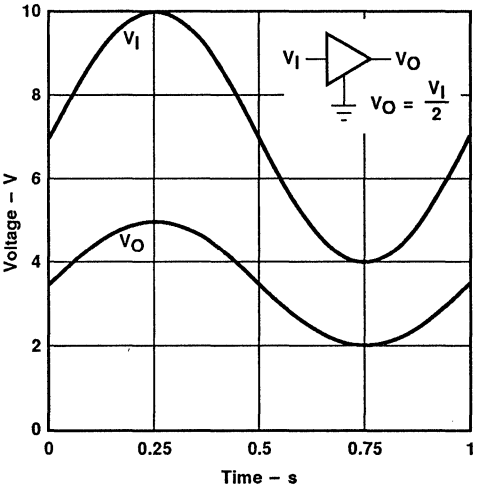
```
  RO1      8     5    63
  RO2      7    99    62
  VCM+    82    99    1.0
  VCM-    83    99    -2.3
  VB       9     0    DC 0
  VC       3    53    DC 1.400
  VE      54     4    DC 1.400
  VLIM     7     8    DC 0
  VLP     91     0    DC 30
  VLN      0    92    DC 30
  VPSR     0    86    DC 0
  RFB      5     2    1K
  RIN     30     1    1K
  RCOM    34     4    .1
*REGULATOR SECTION
  RG1     30     0    20MEG
  RG2     30    31    .2
  RG3     31    35    400K
  RG4     35    34    411K
  RG5     31    36    25MEG
  HREG    31    32    POLY(2) VPSET VNSET 0 1E2 1E2
  VREG    32    33    DC 0V
  EREG    33    34    POLY(1) (36,34) 1.23 1
  VADJ    36    34    1.27V
  HPSET   37     0    VREG 1.030E3
  VPSET   38     0    DC 20V
  HNSET   39     0    VREG 6.11E5
  VNSET   40     0    DC -20V
  DSUB     4    34    DX
  DPOS    37    38    DX
  DNNEG   40    39    DX
.MODEL DX D(IS=800.0E-18)
.MODEL QX PNP(IS=800.0E-18 BF=480)
.ENDS
```

- 1/2 V_I Virtual Ground for Analog Systems
- Self-Contained 3-terminal TO-226AA Package
- Micropower Operation . . . 170 µA Typ, V_I = 5
- Wide V_I Range . . . 4 V to 40 V
- High Output-Current Capability
  Sink . . . 20 mA Typ
  Source . . . 20 mA Typ
- Excellent Output Regulation . . . ±45 µV Typ
  I_O = −10 mA to 10 mA
- Low-Impedance Output . . . 0.0075 Ω Typ
- Noise Reduction Pin (D, JG, and P Packages Only)

description

In signal-conditioning applications utilizing a single power source, a reference voltage equal to one-half the supply voltage is required for termination of all analog signal "grounds". Texas Instruments introduces a precision virtual ground whose output voltage is always equal to one-half the input voltage, the TLE2426 "rail splitter".

INPUT/OUTPUT TRANSFER CHARACTERISTICS



The unique combination of a high-performance, micropower operational amplifier and a precision-trimmed divider on a single silicon chip results in a precise V_O/V_I ratio of 0.5 while sinking and sourcing current. The TLE2426 provides a low impedance output with 20 mA of sink and source capability while quiescently drawing less than 280 µA of supply current over the full input range of 4 to 40 V. A designer need not pay the price in terms of board space for a conventional signal ground solution consisting of resistors, capacitors, operational amplifiers, and voltage references. The performance and precision of the TLE2426 is availiable in an easy-to-use, space saving, 3-terminal LP package. For increased performance, the optional 8-pin packages provide a noise-reduction pin. With the addition of an external capacitor (C_{NR}), peak-to-peak noise is reduced while line ripple rejection is improved.

AVAILABLE OPTIONS

T_A	PACKAGE				CHIP FORM (Y)
	SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC (LP)	PLASTIC DIP (P)	
0°C to 70°C	TLE2426CD	———	TLE2426CLP	TLE2426CP	TLE2426Y
−40°C to 85°C	TLE2426ID	———	TLE2426ILP	TLE2426IP	
−55°C to 125°C	TLE2426MD	TLE2426MJG	TLE2426MLP	TLE2426MP	

D and LP packages are available taped and reeled in the commercial temperature range only.
Add "R" suffix to device type (e.g., TLC2426CDR). Chips are tested at 25°C.

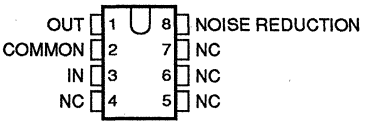
description (continued)

Initial output tolerence for a single 5-V or 12-V system is better than 1% with 3.6% over the full 40-V input range. Load rejection exceeds 12 bits of accuracy. Whether the application is for a data acquisition front-end, analog signal termination, or simply a precision voltage reference, the TLE2426 eliminates a major source of system error. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized from – 40°C to 85°C. The M-suffix devices are characterized over the full military temperature range of –55°C to 125°C.

TLE2426Y chip information

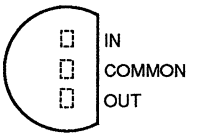
These chips, properly assembled, display characteristics similar to the TLE2426. (see electrical table on TLE2426Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

D, P, OR JG PACKAGE
(TOP VIEW)

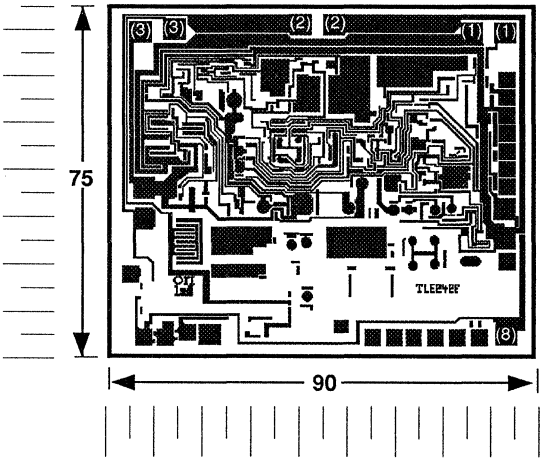


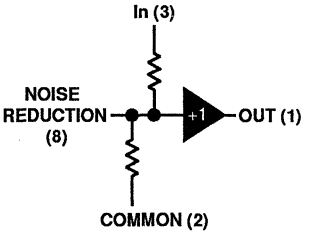
NC – No internal connection.

LP PACKAGE
(TOP VIEW)



BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

Note: Both bonding pads number 1, both number 2, and both number 3, must be bonded out to the corresponding functions pin.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous input voltage . . . . . 40 V
Continuous filter trap voltage . . . . . 40 V
Output current, I_O . . . . . ±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
M-suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package . . . . . 300°C

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	270 mW
LP	775 mW	6.2 mW/°C	496 mW	403 mW	155 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C-SUFFIX		I-SUFFIX		M-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975	1.995	2.015	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 5 V		Full range	2.475		2.525	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	250	μA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		– 45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
			Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 5 V		25°C	20	26		mA
	Sourcing current, V_O = 0			–20	– 47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		μs
	V_I = 0 to 5 V, V_O to 0.01%				160		

†Full range is 0°C to 70°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

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electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975	1.995	2.015	V
	V_I = 12 V			6	6.05	6.1	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 12 V		Full range	5.995		6.105	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	250	μA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		– 45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
			Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 12 V		25°C	20	31		mA
	Sourcing current, V_O = 0			–20	– 70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		12		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

†Full range is 0°C to 70°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975	1.995	2.015	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 5 V		Full range	2.47		2.53	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	250	µA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		–45	±160	µV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	µV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 5 V		25°C	20	26		mA
	Sourcing current, V_O = 0			–20	–47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		µV
		C_{NR} = 1 µF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		µs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		µs
	V_I = 0 to 5 V, V_O to 0.01%				160		

†Full range is – 40°C to 85°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

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electrical characteristics at specified free-air temperature, V_I = 12V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975	1.995	2.015	V
	V_I = 12 V			6	6.05	6.1	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 12 V		Full range	5.985		6.115	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	250	μA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		– 45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 12 V		25°C	20	31		mA
	Sourcing current, V_O = 0			–20	– 70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		12		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

†Full range is – 40°C to 85°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975	1.995	2.015	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 5 V		Full range	2.465		2.535	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	250	μA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		– 45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
	I_O = 0 to 3 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 5 V		25°C	20	26		mA
	Sourcing current, V_O = 0			–20	– 47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		μs
	V_I = 0 to 5 V, V_O to 0.01%				120		

†Full range is –55°C to 125°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

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electrical characteristics at specified free-air temperature, V_I = 12V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		25°C	1.975		2.015	V
	V_I = 12 V			6	6.05	6.1	
	V_I = 40 V			20.5	20.7	20.9	
	V_I = 12 V		Full range	5.975		6.125	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	250	μA
		V_I = 4 to 40 V	Full range			350	
Output regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		– 45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current, V_O = 12 V		25°C	20	31		mA
	Sourcing current, V_O = 0			–20	– 70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		12		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

†Full range is –55°C to 125°C.
‡Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

electrical characteristics at specified free-air temperature, V_I = 5V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		1.975	1.995	2.015	V
	V_I = 5 V		2.48	2.5	2.52	
	V_I = 40 V		20.5	20.7	20.9	
Supply current	No load			170	250	µA
Output regulation (sourcing current)†	I_O = 0 to –10 mA			– 45	±160	µV
	I_O = 0 to –20 mA			–150	±450	
Output regulation (sinking current)†	I_O = 0 to 10 mA			15	±160	µV
	I_O = 0 to 20 mA			65	±235	
Output impedance				7.5	22.5	mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current, V_O = 5 V		20	26		mA
	Sourcing current, V_O = 0		–20	– 47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF		20		µs
	V_I = 0 to 5 V, V_O to 0.01%			160		

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	V_I = 4 V		1.975	1.995	2.015	V
	V_I = 12 V		6	6.05	6.1	
	V_I = 40 V		20.5	20.7	20.9	
Supply current	No load			195	250	µA
Output regulation (sourcing current)‡	I_O = 0 to –10 mA			– 45	±160	µV
	I_O = 0 to –20 mA			–150	±450	
Output regulation (sinking current)‡	I_O = 0 to 3 mA			15	±160	µV
	I_O = 0 to 20 mA			65	±235	
Output impedance				7.5	22.5	mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current, V_O = 12 V		20	31		mA
	Sourcing current, V_O = 0		–20	– 70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current step response	V_O to 0.1%, I_O = ± 10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ± 10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF		12		µs
	V_I = 0 to 12 V, V_O to 0.01%			120		

†Sample tested. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

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TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†

DISTRIBUTION
OF
OUTPUT VOLTAGE

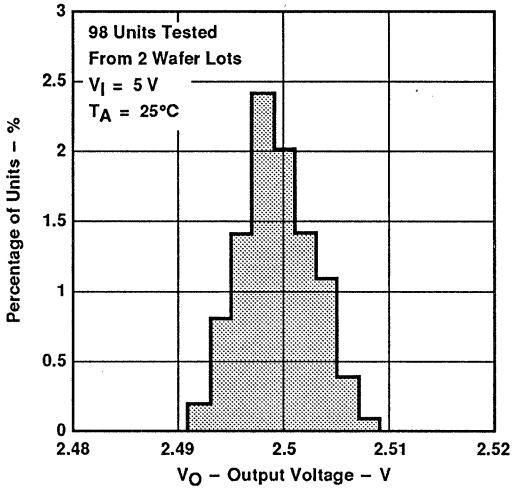


Figure 1

DISTRIBUTION
OF
OUTPUT VOLTAGE

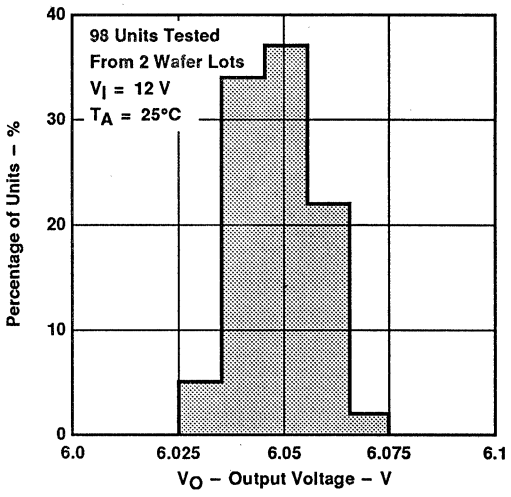


Figure 2

OUTPUT VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

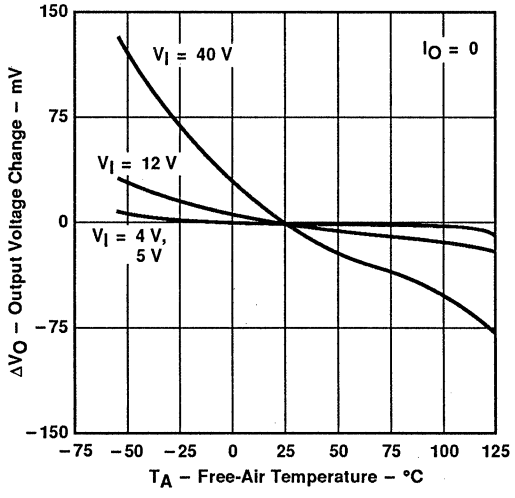


Figure 3

OUTPUT VOLTAGE ERROR
vs
INPUT VOLTAGE

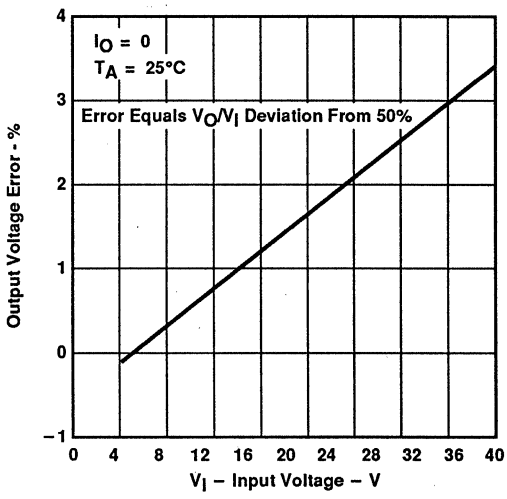


Figure 4

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

BIAS CURRENT
vs
INPUT VOLTAGE

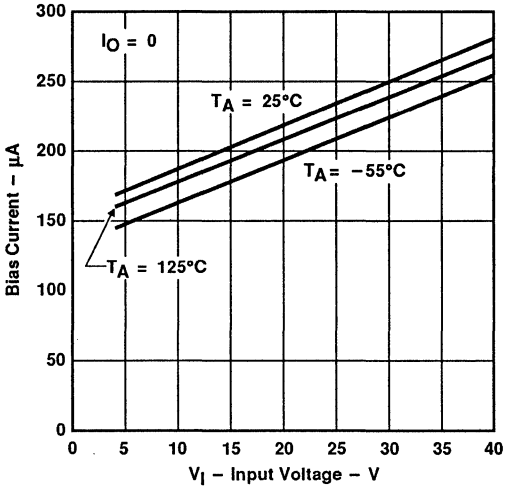


Figure 5

BIAS CURRENT
vs
FREE-AIR TEMPERATURE

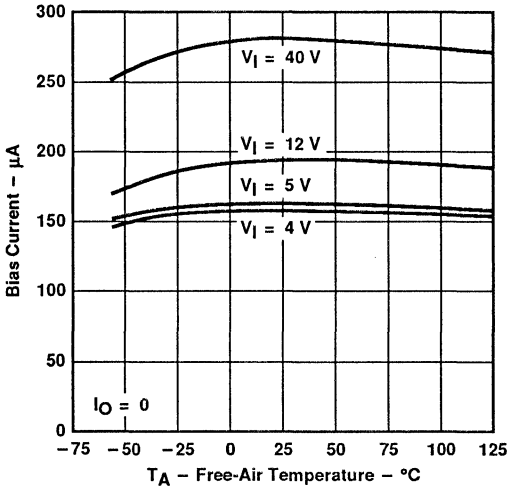


Figure 6

OUTPUT REGULATION
vs
OUTPUT CURRENT

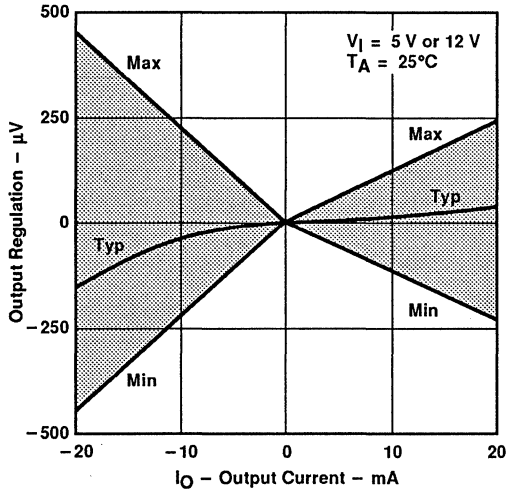


Figure 7

OUTPUT IMPEDANCE
vs
FREQUENCY

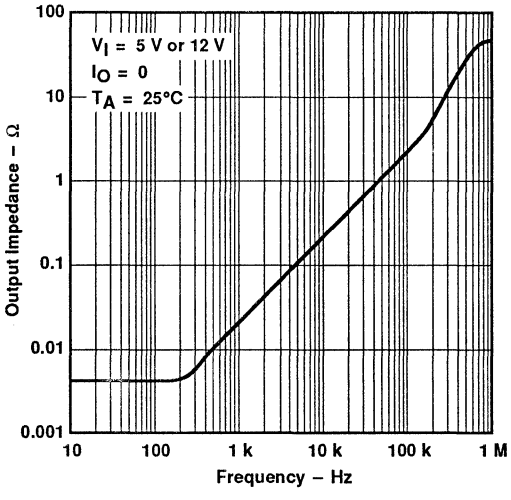


Figure 8

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

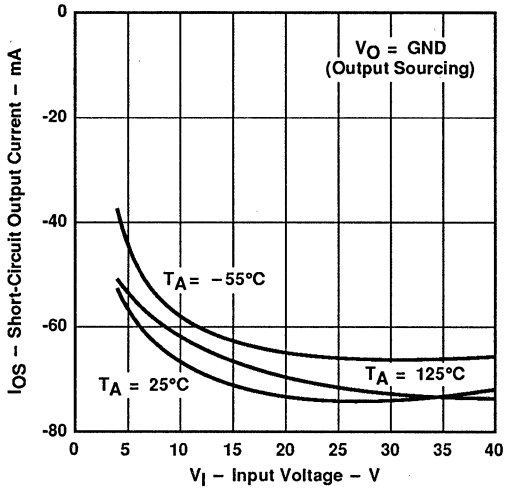


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

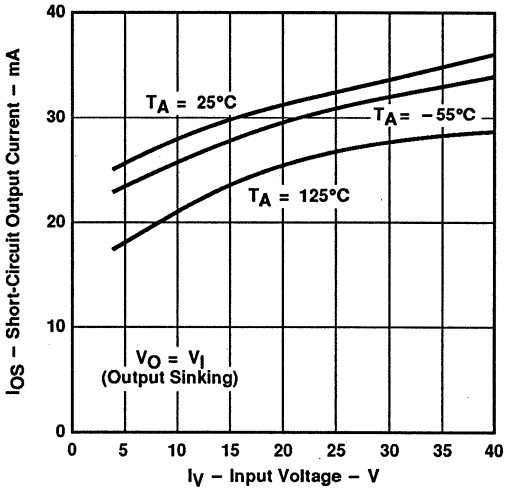


Figure 10

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

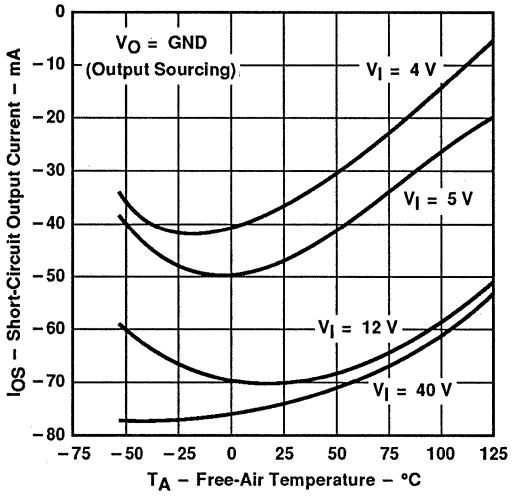


Figure 11

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

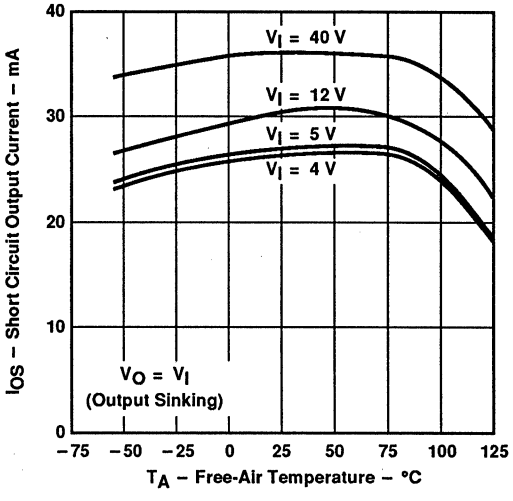


Figure 12

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

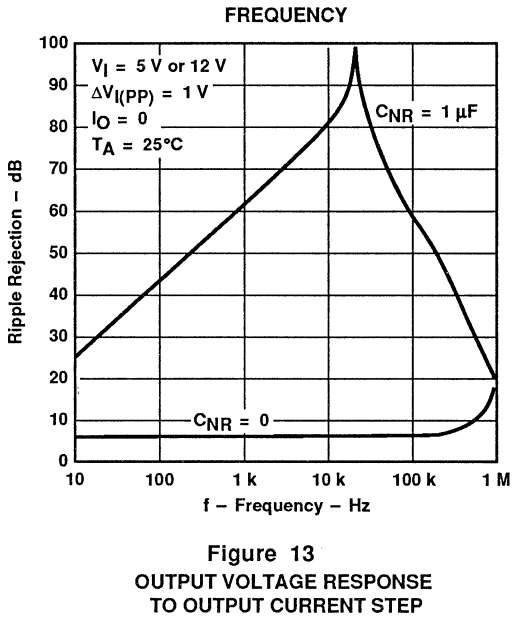


Figure 13

SPOT NOISE
vs
FREQUENCY

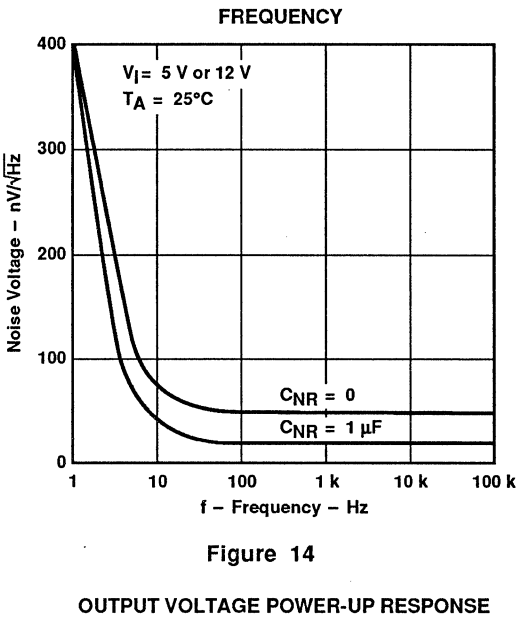


Figure 14

OUTPUT VOLTAGE RESPONSE
TO OUTPUT CURRENT STEP
vs
TIME

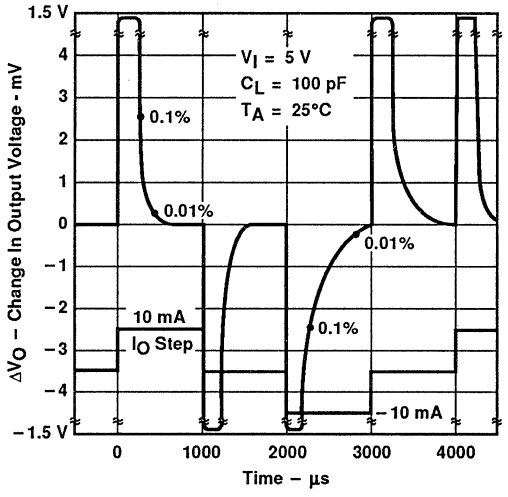


Figure 15

OUTPUT VOLTAGE POWER-UP RESPONSE
vs
TIME

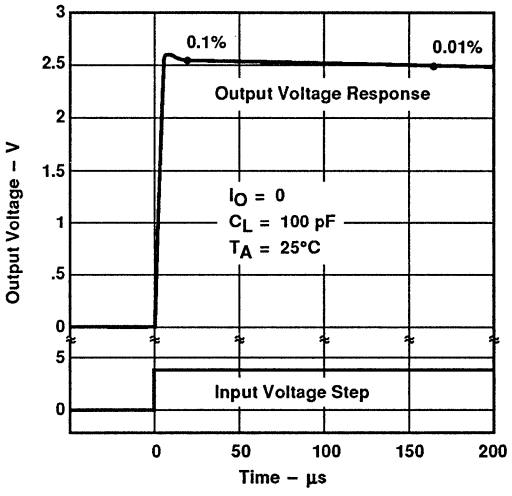


Figure 16

TYPICAL CHARACTERISTICS†

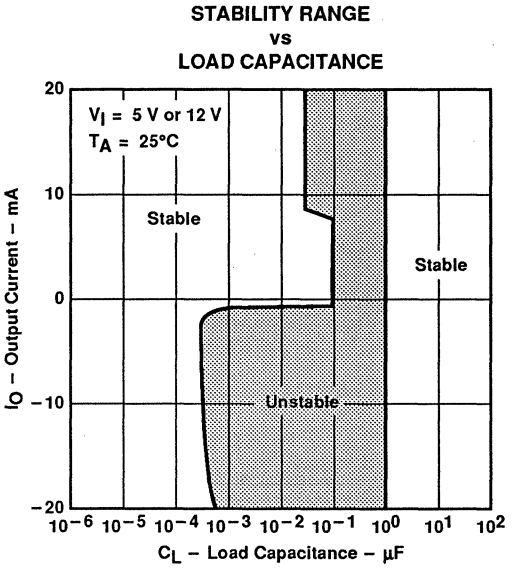


Figure 17

macromodel information

```
* TLE2426 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 08/21/90 AT 13:51
* REV (N/A)       SUPPLY VOLTAGE: 5 V
* CONNECTIONS:      FILTER
                    | INPUT
*                   | | COMMON
*                   | | | OUTPUT
*                   | | | |
.SUBCKT TLE2426     1 3 4 5
```

```
C1      11   12   21.66E-12
C2       6    7   30.00E-12
C3      87    0   10.64E-9
CPSR    85   86   15.9E-9
DCM+    81   82   DX
DCM-    83   81   DX
DC       5   53   DX
DE      54    5   DX
DLP     90   91   DX
DLN     92   90   DX
DP       4    3   DX
ECMR    84   99   (2,99) 1
EGND    99    0   POLY(2) (3,0) (4,0) 0 .5 .5
EPSR    85    0   POLY(1) (3,4) -16.22E-6  3.24E-6
ENSE    89    2   POLY(1) (88,0) 120E-6  1
FB       7   99   POLY(6) VB VC VE VLP VLN VPSR 0 74.8E6 -10E6 10E6 10E6 -10E6 74E6
GA       6    0   11 12 320.4E-6
GCM      0    6   10 99 1.013E-9
GPSR    85   86   (85,86) 100E-6
GRC1     4   11   (4,11) 3.204E-4
GRC2     4   12   (4,12) 3.204E-4
GRE1    13   10   (13,10) 1.038E-3
GRE2    14   10   (14,10) 1.038E-3
HLIM    90    0   VLIM 1K
HCMR    80    1   POLY(2) VCM+ VCM- 0 1E2 1E2
IRP      3    4   146E-6
IEE      3   10   DC 24.05E-6
IIO      2    0   .2E-9
I1      88    0   1E-21
Q1      11   89   13 QX
Q2      12   80   14 QX
R2       6    9   100.0E3
RCM     84   81   1K
REE     10   99   8.316E6
RN1     87    0   2.55E8
RN2     87   88   11.67E3
RO1      8    5   63
R02      7   99   62
VCM+    82   99   1.0
VCM-    83   99   -2.3
VB       9    0   DC 0
```

macromodel information (continued)

```
    VC        3    53    DC 1.400
    VE       54     4    DC 1.400
    VLIM      7     8    DC 0
    VLP      91     0    DC 30
    VLN       0    92    DC 30
    VPSR      0    86    DC 0
    RFB       5     2    1K
    RIN1      3     1    220K
    RIN2      1     4    220K
.MODEL DX D(IS=800.OE-18)
.MODEL QX PNP(IS=800.0E-18 BF=480)
.ENDS
```

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

- **150-mA Load Current Without External Power Transistor**
- **Typically 0.02% Input Regulation and 0.03% Load Regulation (uA723M)**
- **Adjustable Current Limiting Capability**
- **Input Voltages to 40 V**
- **Output Adjustable From 2 V to 37 V**
- **Direct Replacement for Fairchild μA723C and μA723M**

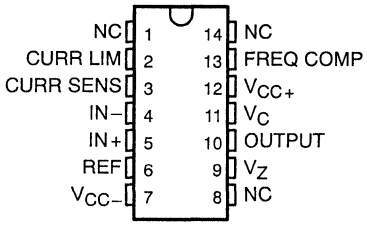
description

The uA723C and uA723M are precision monolithic integrated circuit voltage regulators featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference voltage amplifier, an error amplifier, a 150-mA output transistor, and an adjustable output current limiter.

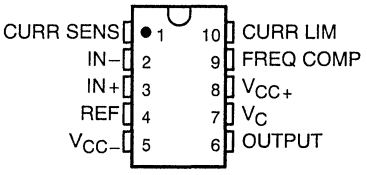
The uA723C and uA723M are designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements may be connected as shown in Figures 4 and 5.

The uA723C is characterized for operation from 0°C to 70°C. The uA723M is characterized for operation over the full military temperature range of −55°C to 125°C.

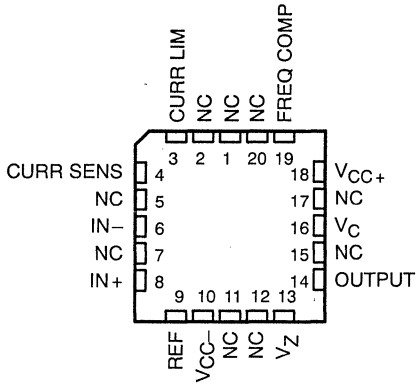
uA723C . . . D OR N PACKAGE
uA723M . . . J PACKAGE
(TOP VIEW)



uA723M . . . U PACKAGE
(TOP VIEW)

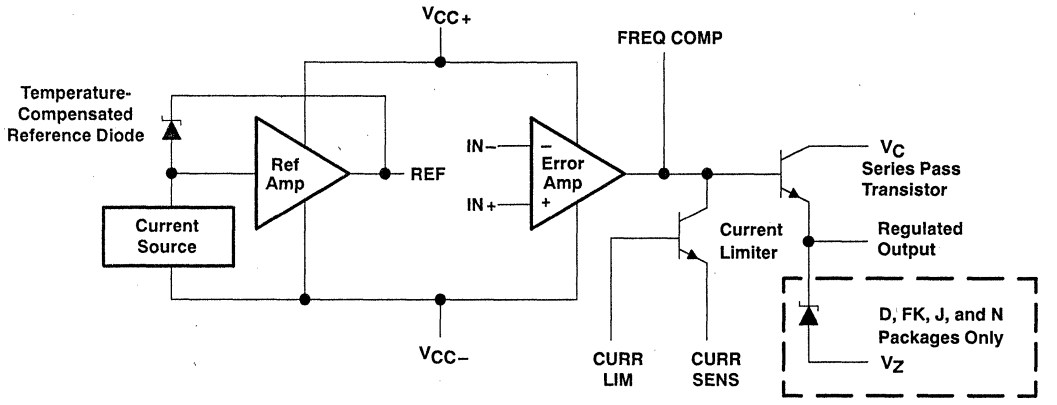


uA723M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Peak voltage from V_{CC+} to V_{CC-} ($t_w \leq 50$ ms) ..... 50 V
Continuous voltage from V_{CC+} to V_{CC-} ..... 40 V
Input-to-output voltage differential ..... 40 V
Differential input voltage to error amplifier ..... ±5 V
Voltage between noninverting input and V_{CC-} ..... 8 V
Current from V_Z ..... 25 mA
Current from REF ..... 15 mA
Continuous total dissipation (see Note 1) ..... See Dissipation Rating Table
Operating free-air temperature range: uA723C ..... 0°C to 70°C
uA723M ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or U package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

NOTE 1: Power dissipation = $[I_{(standby)} + I_{(ref)}] V_{CC} + [V_C - V_O] I_O$.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	25°C	608 mW	
FK and J	1000 mW	11.0 mW/°C	59°C	880 mW	275 mW
N	1000 mW	9.2 mW/°C	41°C	736 mW	
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA

electrical characteristics at specified free-air temperature (see Notes 2 and 3)

PARAMETER	TEST CONDITIONS		T_A†	uA723C			uA723M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V		25°C		0.01%	0.1%		0.01%	0.1%	
	V_I = 12 V to V_I = 40 V		25°C		0.1%	0.5%		0.02%	0.2%	
	V_I = 12 V to V_I = 15 V		Full range			0.3%			0.3%	
Ripple rejection	f = 50 H_z to 10 kHz,	C_{ref} = 0	25°C		74			74		dB
	f = 50 Hz to 10 kHz,	C_{ref} = 5 μF	25°C		86			86		
Output regulation	I_O = 1 mA to 50 mA		25°C		−0.03%	−0.2%		−0.03%	−0.15%	
			Full range			−0.6%			−0.6%	
Reference voltage, V_{ref}			25°C	6.8	7.15	7.5	6.95	7.15	7.35	V
Standby current	V_I = 30 V,	I_O = 0	25°C		2.3	4		2.3	3.5	mA
Temperature coefficient of output voltage			Full range		0.003	0.015		0.002	0.015*	%/°C
Short-circuit output current	R_{SC} = 10 Ω,	V_O = 0	25°C		65			65		mA
Output noise voltage	BW = 100 Hz to 10 kHz,	C_{ref} = 0	25°C		20			20		μV
	BW = 100 Hz to 10 kHz,	C_{ref} = 5 μF	25°C		2.5			2.5		

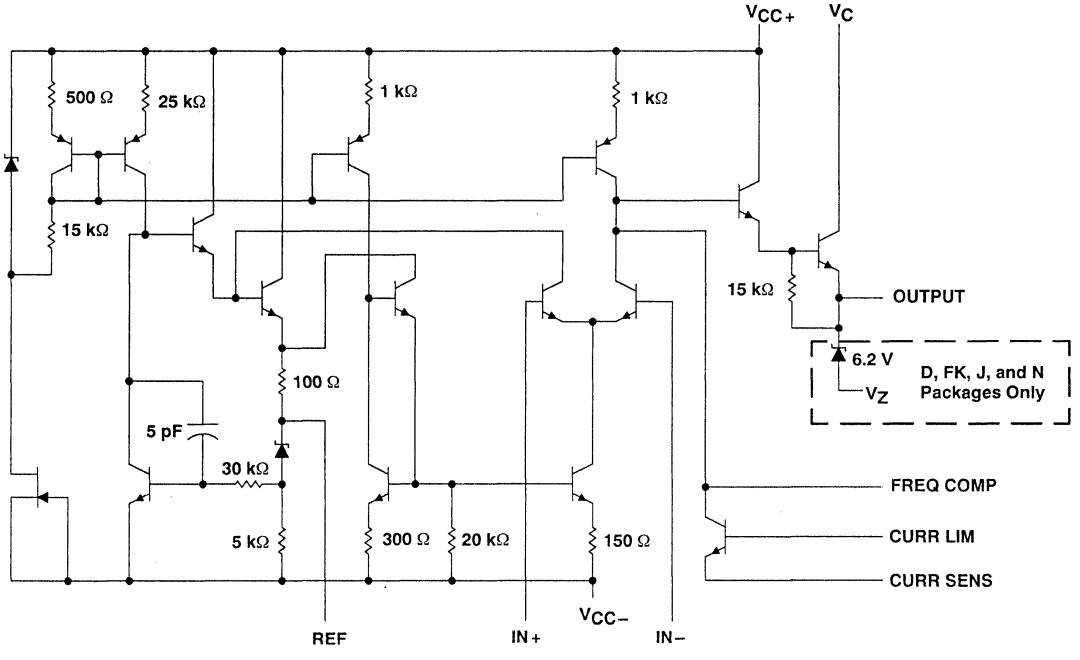
*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full range for uA723C is 0°C to 70°C and for uA723M is −55°C to 125°C.

NOTES: 2. For all values in this table, the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier ≤ 10 kΩ. Unless otherwise specified, $V_I = V_{CC+} = V_C$ = 12 V, V_{CC-} = 0, V_O = 5 V, I_O = 1 mA, R_{SC} = 0, and C_{ref} = 0.

3. Pulse-testing techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

schematic



Resistor and capacitor values shown are nominal.

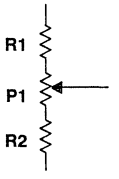
APPLICATION INFORMATION

Table 1. Resistor Values (kΩ) for Standard Output Voltages

OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 4)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (SEE NOTE 5)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	P2 (kΩ)
3.0	1,5,6,9,11, 12 (4)	4.12	3.01	1.8	0.5	1.2
3.6	1,5,6,9,11, 12 (4)	3.57	3.65	1.5	0.5	1.5
5.0	1,5,6,9,11, 12 (4)	2.15	4.99	0.75	0.5	2.2
6.0	1,5,6,9,11, 12 (4)	1.15	6.04	0.5	0.5	2.7
9.0	2,4,(5,6, 9,12)	1.87	7.15	0.75	1.0	2.7
12	2,4,(5,6, 9,12)	4.87	7.15	2.0	1.0	3.0
15	2,4,(5,6, 9,12)	7.87	7.15	3.3	1.0	3.0
28	2,4,(5,6, 9,12)	21.0	7.15	5.6	1.0	2.0
45	7	3.57	48.7	2.2	10	39
75	7	3.57	78.7	2.2	10	68
100	7	3.57	105	2.2	10	91
250	7	3.57	255	2.2	10	240
−6 (Note 6)	3, 10	3.57	2.43	1.2	0.5	0.75
−9	3, 10	3.48	5.36	1.2	0.5	2.0
−12	3, 10	3.57	8.45	1.2	0.5	3.3
−15	3, 10	3.57	11.5	1.2	0.5	4.3
−28	3, 10	3.57	24.3	1.2	0.5	10
−45	8	3.57	41.2	2.2	10	33
−100	8	3.57	95.3	2.2	10	91
−250	8	3.57	249	2.2	10	240

NOTES: 4. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use the figure numbers without parentheses. If the divider is across V_O, use the figure numbers in parentheses.

5. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown below.



Adjustable Output Circuit

6. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

APPLICATION INFORMATION

Table 2. Formulas for Intermediate Output Voltages

Outputs from 2 V to 7 V See Figures 1,5,6,9, 11, 12 (4) and Note 4 $V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	Outputs from 4 V to 250 V See Figure 7 and Note 4 $V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1}$; $R3 = R4$	Current Limiting $I_{(limit)} \approx \frac{0.65\ V}{R_{SC}}$
Outputs from 7 V to 37 V See Figures 2,4,(5,6,9, 11, 12) and Note 4 $V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	Outputs from −6 V to −250 V See Figures 3, 8, 10 and Notes 4 and 6 $V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1}$; $R3 = R4$	Foldback Current Limiting See Figure 6 $I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\ 0.65\ V}{R_{SC} R4}$; $I_{OS} \approx \frac{0.65\ V}{R_{SC}} \times \frac{R3 + R4}{R4}$

NOTES: 4. The R1/R2 divider may be across either V_O or $V_{(ref)}$. If the divider is across $V_{(ref)}$, use figure numbers without parentheses. If the divider is across V_O, use the figure numbers in parentheses.

6. For Figures 3, 8, and 10, the device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.

APPLICATION INFORMATION

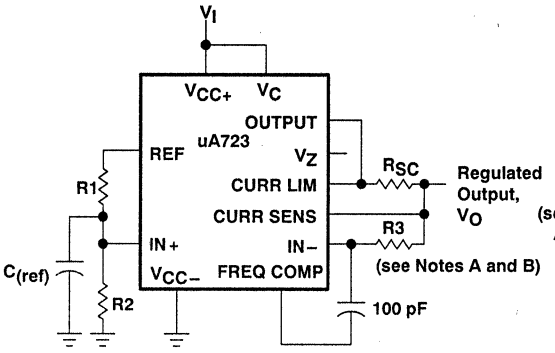


Figure 1. Basic Low-Voltage Regulator (V_O = 2 V to 7 V)

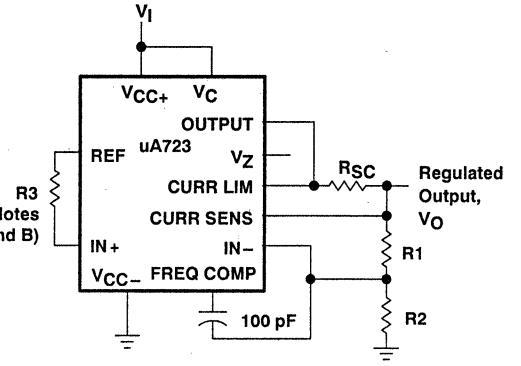


Figure 2. Basic High-Voltage Regulator (V_O = 7 V to 37 V)

NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum α_{VO}.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

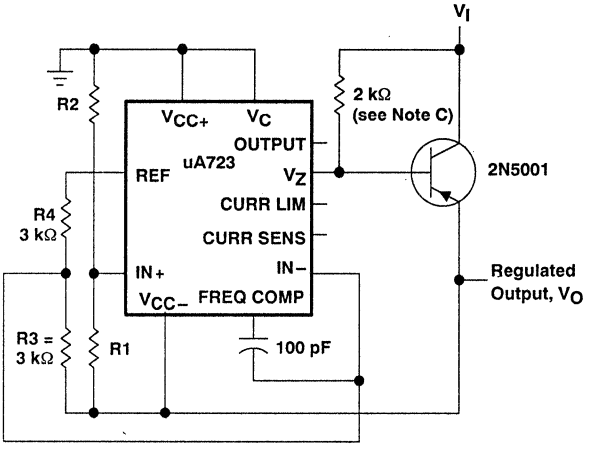


Figure 3. Negative-Voltage Regulator

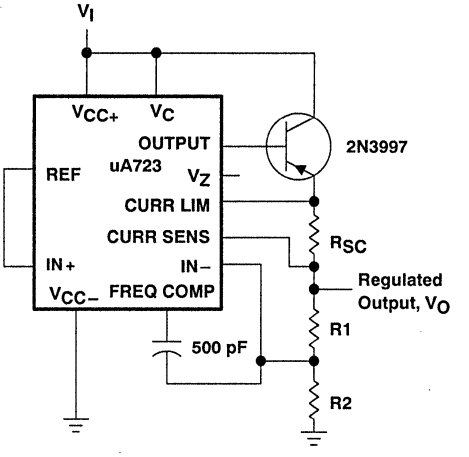


Figure 4. Positive-Voltage Regulator (External N-P-N Pass Terminator)

NOTE C: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

APPLICATION INFORMATION

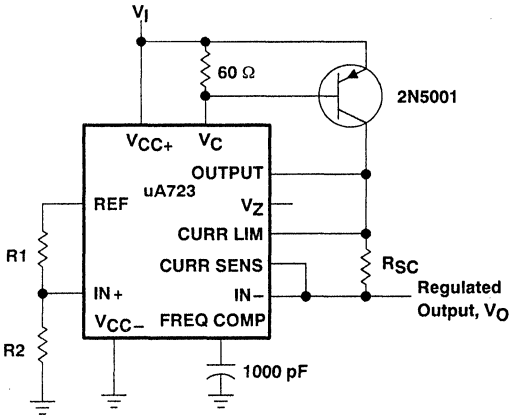


Figure 5. Positive-Voltage Regulator
(External P-N-P Pass Transistor)

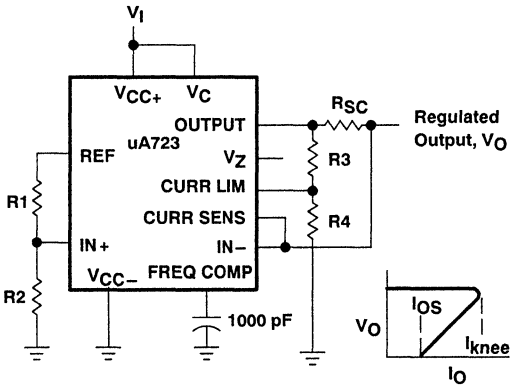


Figure 6. Foldback Current Limiting

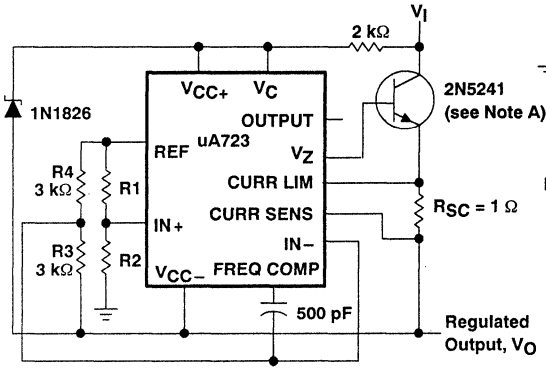


Figure 7. Positive Floating Regulator

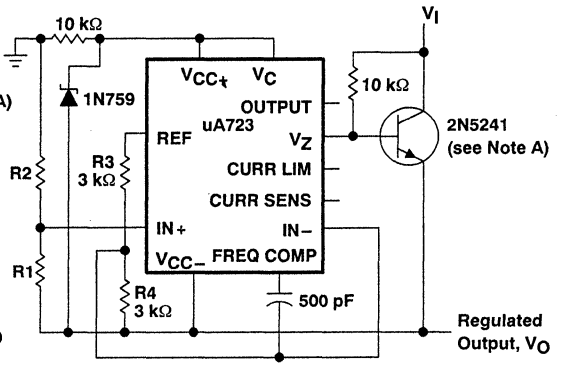


Figure 8. Negative Floating Regulator

NOTE A: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

APPLICATION INFORMATION

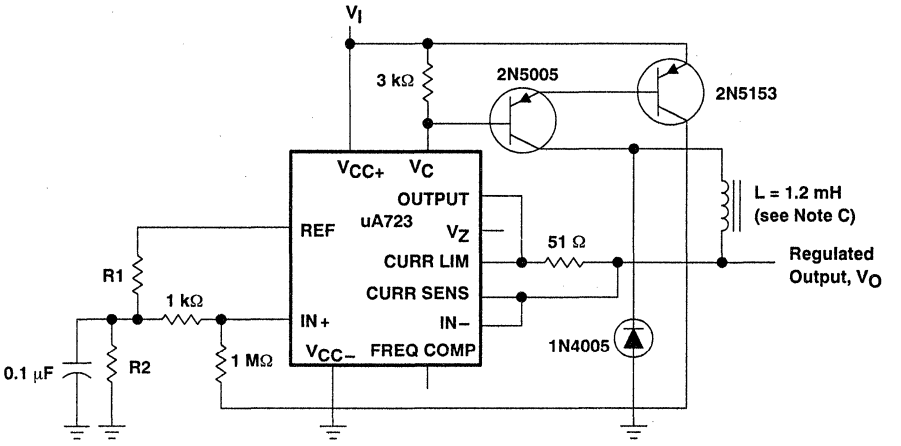


Figure 9. Positive Switching Regulator

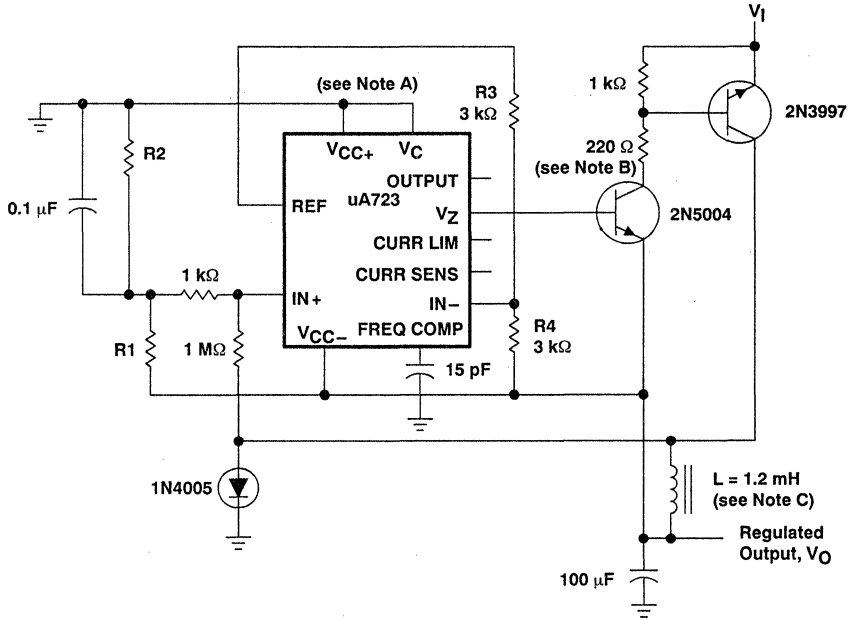
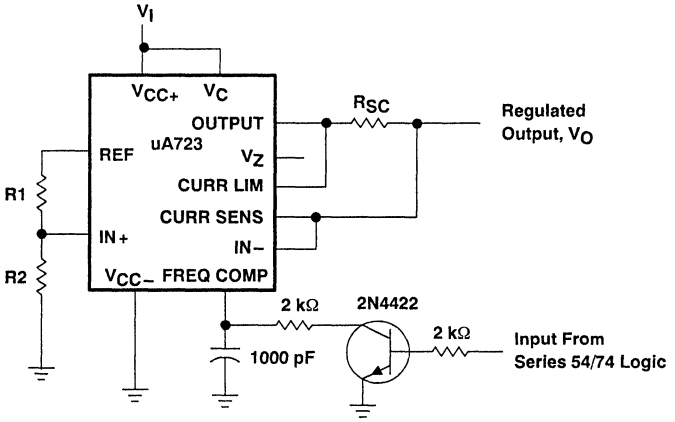


Figure 10. Negative Switching Regulator

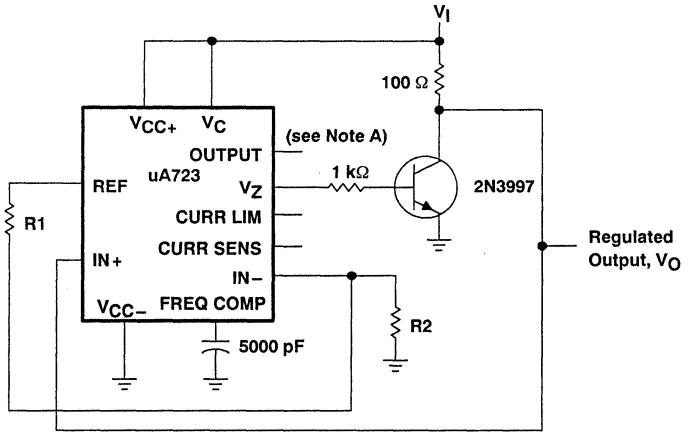
NOTES: A. The device requires a minimum of 9 V between V_{CC+} and V_{CC-} when V_O is equal to or more positive than −9 V.
B. When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.
C. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core or equivalent, with a 0.009-inch air gap.

APPLICATION INFORMATION



NOTE A: A current-limit transistor may be used for shutdown if current limiting is not required.

Figure 11. Remote Shutdown Regulator With Current Limiting



NOTE A: When 10-lead uA723U devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with OUTPUT.

Figure 12. Shunt Regulator

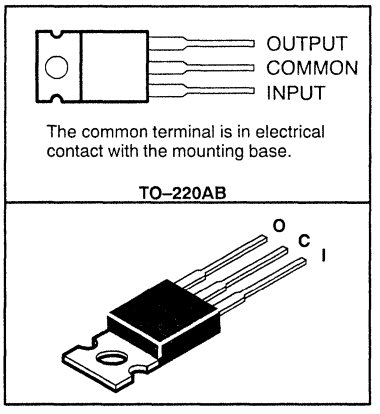
- **3-Terminal Regulators**
- **Output Current Up to 1.5 A**
- **Internal Thermal Overload Protection**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA7800 Series**

NOMINAL OUTPUT VOLTAGE	REGULATOR
5 V	uA7805C
5 V	uA7805Q
6 V	uA7806C
8 V	uA7808C
8.5 V	uA7885C
10 V	uA7810C
12 V	uA7812C
12 V	uA7812Q
15 V	uA7815C
18 V	uA7818C
24 V	uA7824C

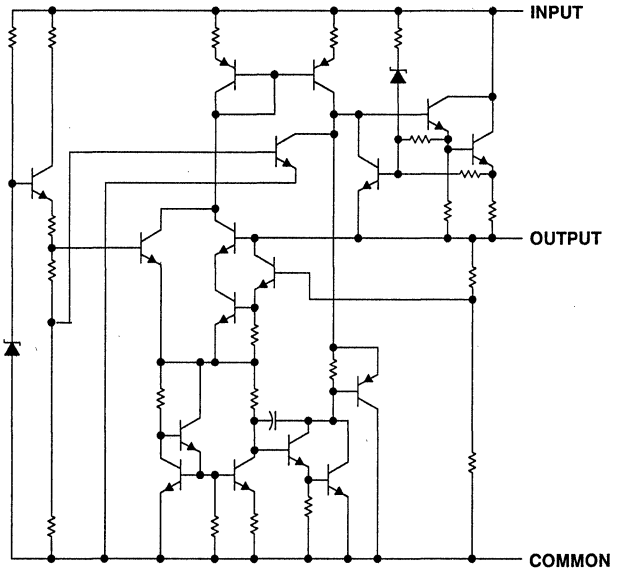
description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be fused with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators. The uA7800C series is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The uA7805Q and uA7812Q are characterized for operation over the virtual junction temperature range of −40°C to 125°C.

KC PACKAGE
(TOP VIEW)



schematic



absolute maximum ratings over operating temperature ranges (unless otherwise noted)

Input voltage:	uA7824C	40 V
	All others	35 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1)		2 W
Continuous total dissipation at (or below) 90°C case temperature (see Note 1)		15 W
Operating free-air, case, or virtual junction temperature range		−40 to 150°C
Storage temperature range		−65 to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

NOTE 1: For operation above 25°C free-air or 90°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATATION DERATING CURVE

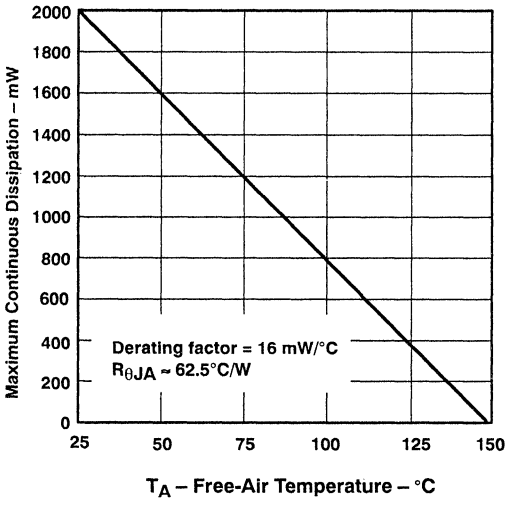


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

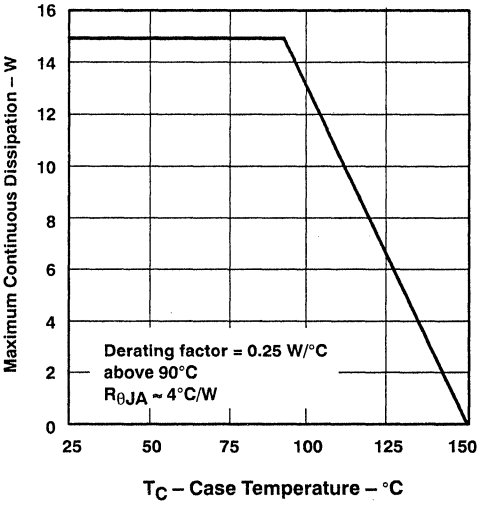


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7805C	7	25	V
	uA7806C	8	25	
	uA7808C	10.5	25	
	uA7885C	10.5	25	
	uA7810C	12.5	28	
	uA7812C	14.5	30	
	uA7815C	17.5	30	
	uA7818C	21	33	
	uA7824C	27	38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J	uA7800C Series	0	125	°C
	uA7805Q, uA7812Q	−40	125	

uA7805C and uA7805Q electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	4.8	5	5.2	V
	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, $P \leq 15$ W	Full range§	4.75		5.25	
Input regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	Full range§	62	78		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	Full range§		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	Full range§		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	Full range§			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

uA7806C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	5.75	6	6.25	V
	I_O = 5 mA to 1 A, V_I = 8 V to 21 V, $P \leq 15$ W	0°C to 125°C	5.7		6.3	
Input regulation	V_I = 8 V to 25 V	25°C		5	120	mV
	V_I = 9 V to 13 V			1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	0°C to 125°C	59	75		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		14	120	mV
	I_O = 250 mA to 750 mA			4	60	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		45		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 8 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		550		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for the uA7805C and −40°C to 125°C for the uA7805Q.

uA7808C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	7.7	8	8.3	V
	I_O = 5 mA to 1 A, V_I = 10.5 V to 23 V, $P \leq 15$ W	0°C to 125°C	7.6		8.4	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	160	mV
	V_I = 11 V to 17 V			2	80	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	55	72		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	160	mV
	I_O = 250 mA to 750 A			4	80	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		52		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

uA7885C electrical characteristics at specified virtual junction temperature, V_I = 15 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	8.15	8.5	8.85	V
	I_O = 5 mA to 1 A, V_I = 11 V to 23.5 V, $P \leq 15$ W	0°C to 125°C	8.1		8.9	
Input regulation	V_I = 10.5 V to 25 V	25°C		6	170	mV
	V_I = 11 V to 17 V			2	85	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	170	mV
	I_O = 250 mA to 750 mA			4	85	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		55		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7810C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	9.6	10	10.4	V
	I_O = 5 mA to 1 A, V_I = 12.5 V to 25 V, P ≤ 15 W	0°C to 125°C	9.5	10	10.5	
Input regulation	V_I = 12.5 V to 28 V	25°C		7	200	mV
	V_I = 14 V to 20 V			2	100	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	200	mV
	I_O = 250 mA to 750 mA			4	100	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 12.5 V to 28 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

uA7812C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	11.5	12	12.5	V
	I_O = 5 mA to 1 A, V_I = 14.5 V to 27 V, P ≤ 15 W	Full range§	11.4		12.6	
Input regulation	V_I = 14.5 V to 30 V	25°C		10	240	mV
	V_I = 16 V to 22 V			3	120	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	Full range§	55	71		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	240	mV
	I_O = 250 mA to 750 mA			4	120	
Output resistance	f = 1 kHz	Full range§		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	Full range§		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 14.5 V to 30 V	Full range§			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for the uA7812C and −40°C to 125°C for the uA7812Q.

uA7815C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	14.4	15	15.6	V
	I_O = 5 mA to 1 A, V_I = 17.5 V to 30 V, $P \leq 15$ W	0°C to 125°C	14.25		15.75	
Input regulation	V_I = 17.5 V to 30 V	25°C		11	300	mV
	V_I = 20 V to 26 V			3	150	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	300	mV
	I_O = 250 mA to 750 mA			4	150	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.4	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

uA7818C electrical characteristics at specified virtual junction temperature, V_I = 27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	17.3	18	18.7	V
	I_O = 5 mA to 1 A, V_I = 21 V to 33 V, $P \leq 15$ W	0°C to 125°C	17.1		18.9	
Input regulation	V_I = 21 V to 33 V	25°C		15	360	mV
	V_I = 24 V to 30 V			5	180	
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz	0°C to 125°C	53	69		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	360	mV
	I_O = 250 mA to 750 mA			4	180	
Output resistance	f = 1 kHz	0°C to 125°C		0.022		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		110		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.5	8	mA
Bias current change	V_I = 21 V to 33 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		200		mA
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7824C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	MIN	TYP	MAX	UNIT
Output voltage‡		25°C	23	24	25	V
	I_O = 5 mA to 1 A, V_I = 27 V to 38 V, P ≤ 15 W	0°C to 125°C	22.8		25.2	
Input regulation	V_I = 27 V to 38 V	25°C		18	480	mV
	V_I = 30 V to 36 V			6	240	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	0°C to 125°C	50	66		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		12	480	mV
	I_O = 250 mA to 750 mA			4	240	
Output resistance	f = 1 kHz	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		170		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.6	8	mA
Bias current change	V_I = 27 V to 38 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

APPLICATION INFORMATION

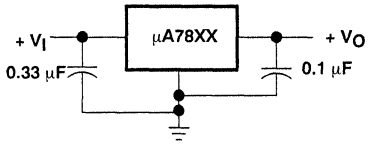


Figure 3. Fixed Output Regulator

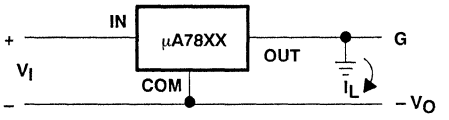


Figure 4. Positive Regulator in Negative Configuration (V_I Must Float)

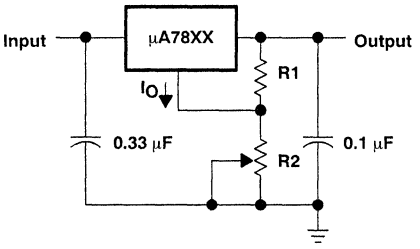


Figure 5. Adjustable Output Regulator

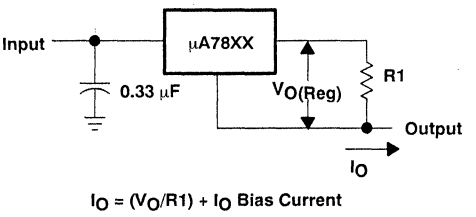


Figure 6. Current Regulator

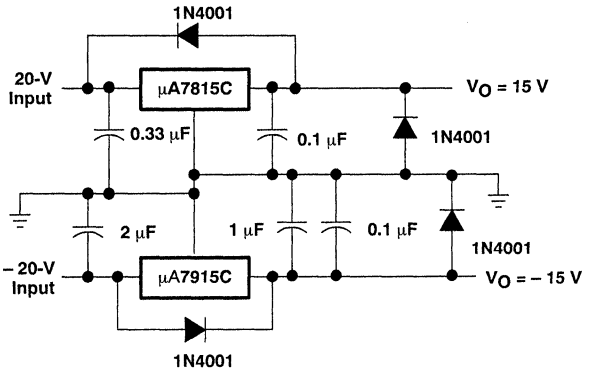


Figure 7. Regulated Dual Supply

APPLICATION INFORMATION

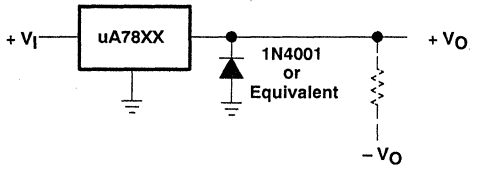


Figure 8. Output Polarity-Reversal Protection Circuit

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., op amps, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 8. This protects the regulator from output polarity reversals during startup and short-circuit operation.

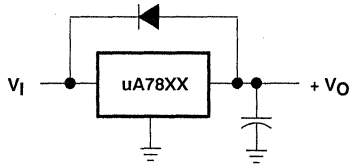


Figure 9. Reverse-Bias Protection Circuit

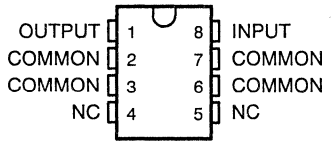
reverse-bias protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 9.

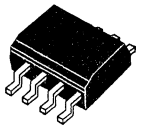
- **3-Terminal Regulators**
- **Output Current Up to 100 mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short-Circuit Limiting**
- **Direct Replacements for Fairchild μA78L00 Series**

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
2.6 V	uA78L02AC	uA78L02C
5 V	uA78L05AC	uA78L05C
5 V	uA78L05AQ	uA78L05Q
6.2 V	uA78L06AC	uA78L06C
8 V	uA78L08AC	uA78L08C
9 V	uA78L09AC	uA78L09C
10 V	uA78L10AC	uA78L10C
12 V	uA78L12AC	uA78L12C
12 V	uA78L12AQ	uA78L12Q
15 V	uA78L15AC	uA78L15C

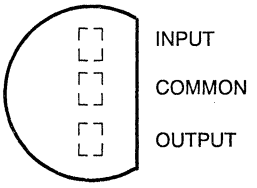
D
"SMALL OUTLINE" PACKAGE
(TOP VIEW)



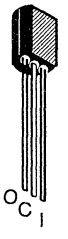
NC–No internal connection



LP
SILECT PACKAGE
(TOP VIEW)



TO-226AA

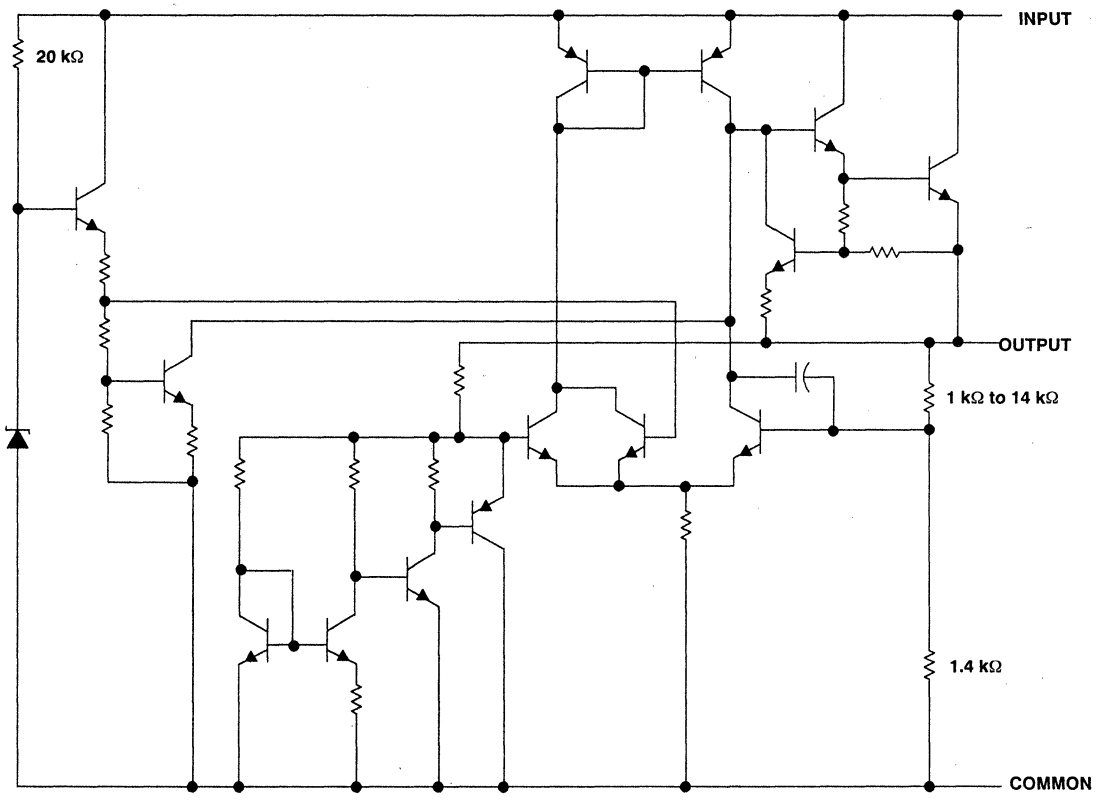


D and LP packages are available taped and reeled. Add "R" suffix to device type (e.g., uA78L05ACDR).

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained together with lower-bias current.

schematic



Resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating temperature ranges (unless otherwise noted)

	uA78L02C, uA78L02AC THRU uA78L10C, uA78L10AC, uA78L05Q, uA78L05AQ	uA78L12C, uA78L12AC, uA78L12Q, uA78L12AQ AND uA78L15C, uA78L15AC	UNIT
Input voltage	30	35	V
Continuous total dissipation (see Note 1)	See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range	−40 to 150	−40 to 150	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW
LP†	775 mW	6.2 mW/°C	25°C	496 mW

† The LP package dissipation rating is based on thermal resistance $R_{\theta JA}$ measured in still air with the device mounted in an Augat socket. The bottom of the package is 10 mm (0.375 in) above the socket.

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_C	$T_C = 125°C$ POWER RATING
D	1600 mW	19.6 mW/°C	65°C	490 mW
LP	1600 mW	28.6 mW/°C	94°C	715 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78L02C, uA78L02AC	4.75	20	V
	uA78L05C, uA78L05AC, uA78L05Q, uA78L05AQ	7	20	
	uA78L06C, uA78L06AC	8.5	20	
	uA78L08C, uA78L08AC	10.5	23	
	uA78L09C, uA78L09AC	11.5	24	
	uA78L10C, uA78L10AC	12.5	25	
	uA78L12C, uA78L12AC, uA78L12Q, uA78L12AQ	14.5	27	
	uA78L15C, uA78L15AC	17.5	30	
Output current, I_O			100	mA
Operating virtual junction temperature, T_J	uA78LxxC, uA78LxxAC,	0	125	°C
	uA78LxxQ, uA78LxxAQ	−40	125	

electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L02C			uA78L02AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	2.4	2.6	2.8	2.5	2.6	2.7	V
	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	Full range§	2.35		2.85	2.45		2.75	
	I_O = 1 mA to 70 mA		2.35		2.85	2.45		2.75	
Input regulation	V_I = 4.75 V to 20 V	25°C		20	125		20	100	mV
	V_I = 5 V to 20 V			16	100		16	75	
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz	25°C	42	51		43	51		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		12	50		12	50	mV
	I_O = 1 mA to 40 mA			6	25		6	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30			30		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.6	6		3.6	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	Full range§			2.5			2.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L05C, uA78L05Q			uA78L05AC, uA78L05AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	4.6	5	5.4	4.8	5	5.2	V
	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	Full range§	4.5		5.5	4.75		5.25	
	I_O = 1 mA to 70 mA		4.5		5.5	4.75		5.25	
Input regulation	V_I = 7 V to 20 V	25°C		32	200		32	150	mV
	V_I = 8 V to 20 V			26	150		26	100	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		15	60		15	60	mV
	I_O = 1 mA to 40 mA			8	30		8	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		42			42		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for uA78L02, uA78L02AC, uA78L05C, and uA78L05AC and −40°C to 125°C for uA78L05Q and uA78L05AQ.

electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L06C			uA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	5.7	6.2	6.7	5.95	6.2	6.45	V
	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	Full range§	5.6		6.8	5.9		6.5	
	I_O = 1 mA to 70 mA		5.6		6.8	5.9		6.5	
Input regulation	V_I = 8.5 V to 20 V	25°C		35	200		35	175	mV
	V_I = 9 V to 20 V			29	150		29	125	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	39	48		40	48		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		16	80		16	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		46			46		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L06C			uA78L06AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	7.36	8	8.64	7.7	8	8.3	V
	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	Full range§	7.2		8.8	7.6		8.4	
	I_O = 1 mA to 70 mA		7.2		8.8	7.6		8.4	
Input regulation	V_I = 10.5 V to 23 V	25°C		42	200		42	175	mV
	V_I = 11 V to 23 V			36	150		36	125	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	36	46		37	46		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		18	80		18	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		54			54		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for uA78L06C and uA78L06AC.

electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L09C			uA78L09AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	8.3	9	9.7	8.6	9	9.4	V
	V_I = 12 V to 24 V, I_O = 1 mA to 40 mA	Full range§	8.1		9.9	8.55		9.45	
	I_O = 1 mA to 70 mA		8.1		9.9	8.55		9.45	
Input regulation	V_I = 12 V to 24 V	25°C		45	225		45	175	mV
	V_I = 13 V to 24 V			40	175		40	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	45		38	45		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		19	90		19	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		58			58		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.1	6		4.1	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 13 V to 24 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L10C			uA78L10AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	9.2	10	10.8	9.6	10	10.4	V
	V_I = 13 V to 25 V, I_O = 1 mA to 40 mA	Full range§	9		11	9.5		10.5	
	I_O = 1 mA to 70 mA		9		11	9.5		10.5	
Input regulation	V_I = 13 V to 25 V	25°C		51	225		51	175	mV
	V_I = 14 V to 25 V			42	175		42	125	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	44		37	44		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		20	90		20	90	mV
	I_O = 1 mA to 40 mA			11	40		11	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		62			62		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.2	6		4.2	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 14 V to 25 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for uA78L09C, uA78L09AC, uA78L10C, and uA78L10AC.

electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L12C, uA78L12Q			uA78L12AC, uA78L12AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	11.1	12	12.9	11.5	12	12.5	V
	V_I = 14 V to 27 V, I_O = 1 mA to 40 mA	Full range§	10.8		13.2	11.4		12.6	
	I_O = 1 mA to 70 mA		10.8		13.2	11.4		12.6	
Input regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			49	200		49	200	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		22	100		22	100	mV
	I_O = 1 mA to 40 mA			13	50		13	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70			70		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.3	6.5		4.3	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA78L15C			uA78L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	13.8	15	16.2	14.4	15	15.6	V
	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	Full range§	13.5		16.5	14.25		15.75	
	I_O = 1 mA to 70 mA		13.5		16.5	14.25		15.75	
Input regulation	V_I = 17.5 V to 30 V	25°C		65	300		65	300	mV
	V_I = 20 V to 30 V			58	250		58	250	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		25	150		25	150	mV
	I_O = 1 mA to 40 mA			15	75		15	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		82			82		μV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.6	6.5		4.6	6.5	mA
		125°C			6			6	
Bias current change	V_I = 10 V to 30 V	Full range§			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

§ Full range virtual junction temperature is 0°C to 125°C for uA78L12C, uA78L12AC, uA78L15C, and uA78L15AC.

APPLICATION INFORMATION

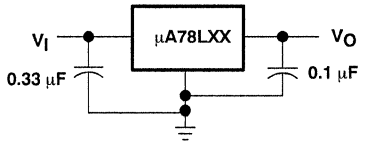


Figure 1. Fixed Output Regulator

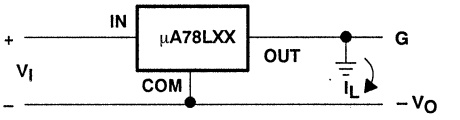


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)

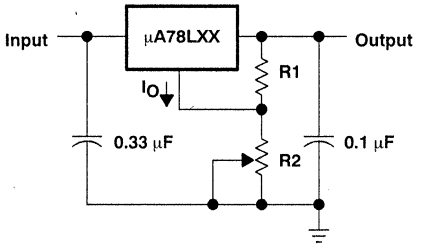
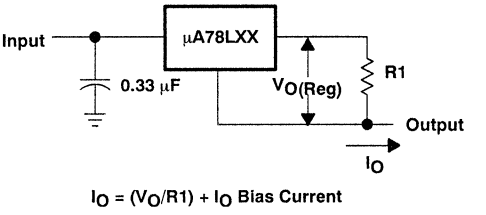


Figure 3. Adjustable Output Regulator



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 4. Current Regulator

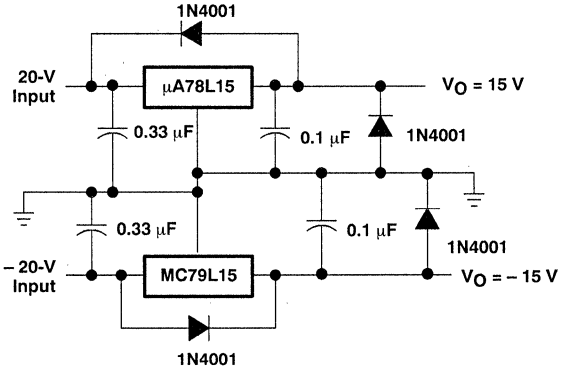


Figure 5. Regulated Dual Supply

APPLICATION INFORMATION

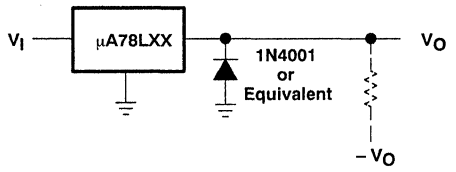


Figure 6. Output Polarity Reversal Protection Circuit

operation with a load common to a voltage of opposite polarity

In many cases, a regulator powers a load that is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g., op amps, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 6. This protects the regulator from output polarity reversals during startup and short-circuit operation.

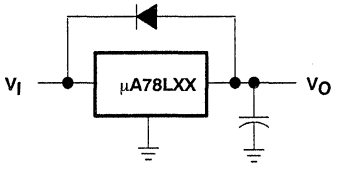


Figure 7. Reverse-Bias Protection Circuit

reverse-bias protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 7.

D2214, JUNE 1976–REVISED SEPTEMBER 1991

- **3-Terminal Regulators**
- **Output Current Up to 500 mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA78M00 Series**

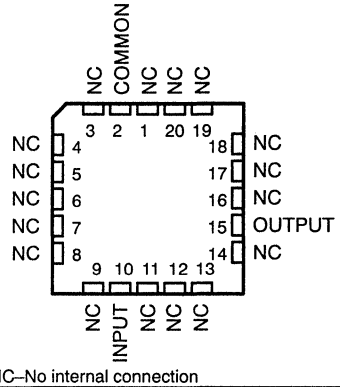
NOMINAL OUTPUT VOLTAGE	0°C TO 125°C OPERATING TEMPERATURE RANGE	–55°C TO 150°C OPERATING TEMPERATURE RANGE
5 V	uA78M05C	uA78M05M
6 V	uA78M06C	
8 V	uA78M08C	
9 V	uA78M09C	
10 V	uA78M10C	
12 V	uA78M12C	uA78M12M
15 V	uA78M15C	
20 V	uA78M20C	
24 V	uA78M24C	
Packages	KC	FK, JG

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

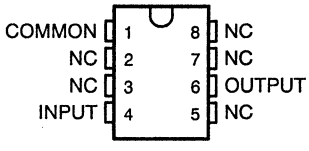
terminal assignments

uA78M_M . . . FK PACKAGE
(TOP VIEW)



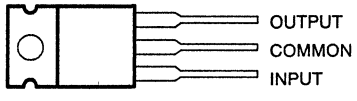
NC–No internal connection

uA78M_M . . . JG PACKAGE
(TOP VIEW)



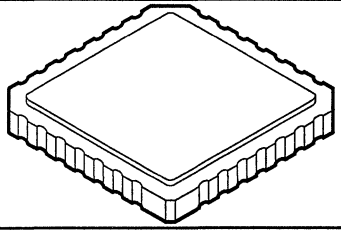
NC–No internal connection

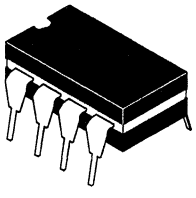
uA78M_C . . . KC PACKAGE
(TOP VIEW)

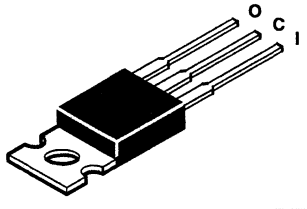


The common terminal is in electrical contact with the mounting base.

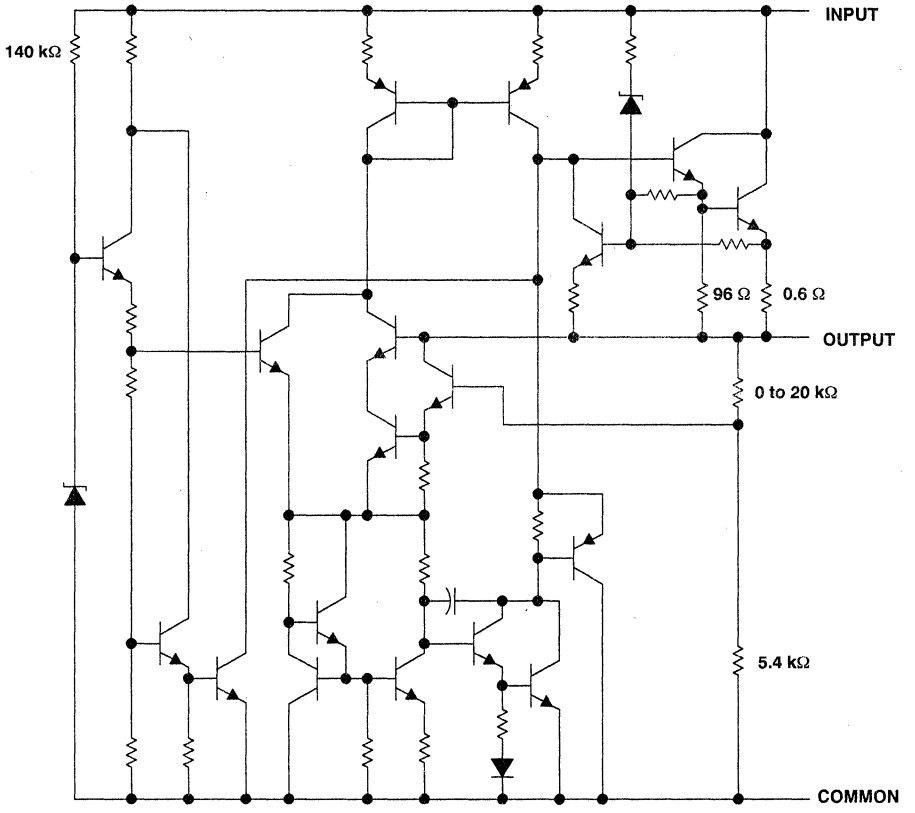
TO–220AB







schematic



Resistor values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

			uA78M05C THRU uA78M24C	uA78M05M uA78M12M	UNIT
Input voltage	uA78M20, uA78M24		−40		V
	All others		35	35	
Continuous total dissipation (see Note 1)			See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range			0 to 150	−55 to 150	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Case temperature for 60 seconds		FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		JG package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		KC package	260		°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW
JG	1050 mW	8.4 mW/°C	672 mW
KC	2000 mW	16 mW/°C	1280 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE

PACKAGE	$T_C \le 50°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 50°C$	$T_C = 125°C$ POWER RATING
KC	20 W	200 mW/°C	5 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78M05C, uA78M05M	7	25	V
	uA78M06C	8	25	
	uA78M08C	10.5	25	
	uA78M09C	11.5	26	
	uA78M10C	12.5	28	
	uA78M12C, uA78M12M	14.5	30	
	uA78M15C	17.5	30	
	uA78M20C	23	35	
	uA78M24C	27	38	
Output current, I_O	All devices		500	mA
Operating virtual junction temperature, T_J	uA78M05C thru uA78M24C	0	125	°C
	uA78M05M and uA78M12M	−55	150	

uA78M05C, uA78M05M electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	uA78M05C			uA78M05M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡	I_O = 5 mA to 350 mA		25°C	4.8	5	5.2	4.8	5	5.2	V
		V_I = 8 V to 20 V	−55°C to 150°C				4.7		5.3	
		V_I = 7 V to 20 V	0°C to 125°C	4.75		5.25				
Input regulation	I_O = 200 mA	V_I = 7 V to 25 V	25°C		3	100		3	50	mV
		V_I = 8 V to 20 V						1	25	
		V_I = 8 V to 25 V			1	50				
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				62*			dB
			0°C to 125°C	62						
		I_O = 300 mA	25°C	62	80		62*	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	100		20	50	mV
	I_O = 5 mA to 200 mA				10	50		10	25	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 25°C						−2*	mV/°C
			25°C to 150°C						−1.5*	
			0°C to 125°C		−1					
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40	200		40	200*	μV
Dropout voltage			25°C		2	2.5		2	2.5	V
Bias current			25°C		4.5	6		4.5	7	mA
Bias current change	I_O = 200 mA,	V_I = 8 V to 25 V	−55°C to 150°C						0.8	mA
			0°C to 125°C			0.8				
	I_O = 5 mA to 350 mA		−55°C to 150°C						0.5	
			0°C to 125°C			0.5				
Short-circuit output current	V_I = 35 V		25°C		300			300	600	mA
Peak output current			25°C		0.7		0.5*	0.7	1.4*	A

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

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uA78M06C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	5.75	6	6.25	V
	I_O = 5 mA to 350 mA	V_I = 8 V to 21 V	0°C to 125°C	5.7		6.3	
Input regulation	I_O = 200 mA	V_I = 8 V to 25 V	25°C		5	100	mV
		V_I = 9 V to 25 V			1.5	50	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	59			dB
		I_O = 300 mA	25°C	59	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	120	mV
	I_O = 5 mA to 200 mA				10	60	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		45		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.5	6	mA
Bias current change	I_O = 200 mA,	V_I = 9 V to 25 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		270		mA
Peak output current			25°C		0.7		A

uA78M08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	7.7	8	8.3	V
	I_O = 5 mA to 350 mA	V_I = 10.5 V to 23 V	0°C to 125°C	7.6		8.4	
Input regulation	I_O = 200 mA	V_I = 10.5 V to 25 V	25°C		6	100	mV
		V_I = 11 V to 25 V			2	50	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	56			dB
		I_O = 300 mA	25°C	56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	160	mV
	I_O = 5 mA to 200 mA				10	80	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		52		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.6	6	mA
Bias current change	I_O = 200 mA,	V_I = 10.5 V to 25 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		250		mA
Peak output current			25°C		0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M09C electrical characteristics at specified virtual junction temperature, V_I = 16 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	8.6	9	9.4	V
	I_O = 5 mA to 350 mA	V_I = 11.5 V to 24 V	0°C to 125°C	8.5		9.5	
Input regulation	I_O = 200 mA	V_I = 11.5 V to 26 V	25°C		6	100	mV
		V_I = 12 V to 26 V			2	50	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	56			dB
		I_O = 300 mA	25°C	56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	180	mV
	I_O = 5 mA to 200 mA				10	90	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		58		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.6	6	mA
Bias current change	I_O = 200 mA,	V_I = 11.5 V to 26 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		250		mA
Peak output current			25°C		0.7		A

uA78M10C electrical characteristics at specified virtual junction temperature, V_I = 17 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	9.6	10	10.4	V
	I_O = 5 mA to 350 mA	V_I = 12.5 V to 25 V	0°C to 125°C	9.5		10.5	
Input regulation	I_O = 200 mA	V_I = 12.5 V to 28 V	25°C		7	100	mV
		V_I = 14 V to 28 V			2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	59			dB
		I_O = 300 mA	25°C	55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	200	mV
	I_O = 5 mA to 200 mA				10	100	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		64		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.7	6	mA
Bias current change	I_O = 200 mA	V_I = 13.5 V to 28 V	0°C to 125°C			0.8	mA
		V_I = 12.5 V to 28 V					
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		245		mA
Peak output current			25°C		0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M12C, uA78M12M electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	uA78M12C			uA78M12M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	11.5	12	12.5	11.5	12	12.5	V
	I_O = 5 mA to 350 mA	V_I = 15.5 V to 27 V	−55°C to 150°C				11.4		12.6	
		V_I = 14.5 V to 27 V	0°C to 125°C	11.4		12.6				
Input regulation	I_O = 200 mA	V_I = 14.5 V to 30 V	25°C		8	100		8	60	mV
		V_I = 16 V to 25 V						2	30	
		V_I = 16 V to 30 V			2	50				
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				55*			dB
			0°C to 125°C	55						
		I_O = 300 mA	25°C	55	80		55*	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	240		25	120	mV
	I_O = 5 mA to 200 mA				10	120		10	60	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 25°C						−4.8*	mV/°C
			25°C to 150°C						−3.6*	
			0°C to 125°C		−1					
Output noise voltage	f = 10 Hz to 100 kHz		25°C		75			75	480*	μV
Dropout voltage			25°C		2			2	2.5	V
Bias current			25°C		4.8	6		4.8	7	mA
Bias current change	I_O = 200 mA	V_I = 15 V to 30 V	−55°C to 150°C						0.8	mA
		V_I = 14.5 V to 30 V	0°C to 125°C			0.8				
	I_O = 5 mA to 350 mA		−55°C to 150°C						0.5	
			0°C to 125°C			0.5				
Short-circuit output current	V_I = 35 V		25°C		240			240	600	mA
Peak output current			25°C		0.7		0.5*	0.7	1.4*	A

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	14.4	15	15.6	V
	I_O = 5 mA to 350 mA	V_I = 17.5 V to 30 V	0°C to 125°C	14.25		15.75	
Input regulation	I_O = 200 mA	V_I = 17.5 V to 30 V	25°C		10	100	mV
		V_I = 20 V to 30 V			3	50	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	54			dB
		I_O = 300 mA	25°C	54	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	300	mV
	I_O = 5 mA to 200 mA				10	150	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		90		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.8	6	mA
Bias current change	I_O = 200 mA,	V_I = 17.5 V to 30 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

uA78M20C electrical characteristics at specified virtual junction temperature, V_I = 29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	19.2	20	20.8	V
	I_O = 5 mA to 350 mA	V_I = 23 V to 35 V	0°C to 125°C	19		21	
Input regulation	I_O = 200 mA	V_I = 23 V to 35 V	25°C		10	100	mV
		V_I = 24 V to 35 V			5	50	
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	53			dB
		I_O = 300 mA	25°C	53	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	400	mV
	I_O = 5 mA to 200 mA				10	200	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		110		μV
Dropout voltage			25°C		2		V
Bias current			25°C		4.9	6	mA
Bias current change	I_O = 200 mA,	V_I = 23 V to 35 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA78M24C electrical characteristics at specified virtual junction temperature, V_I = 33 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	23	24	25	V
	I_O = 5 mA to 350 mA	V_I = 27 V to 38 V	0°C to 125°C	22.8		25.2	
Input regulation	I_O = 200 mA	V_I = 27 V to 38 V	25°C		10	100	mV
		V_I = 28 V to 38 V			5	50	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	50	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	480	mV
	I_O = 5 mA to 200 mA				10	240	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1.2		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		170		μV
Dropout voltage			25°C		2		V
Bias current			25°C		5	6	mA
Bias current change	I_O = 200 mA,	V_I = 27 V to 38 V	0°C to 125°C			0.8	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.5	
Short-circuit output current	V_I = 35 V		25°C		240		mA
Peak output current			25°C		0.7		A

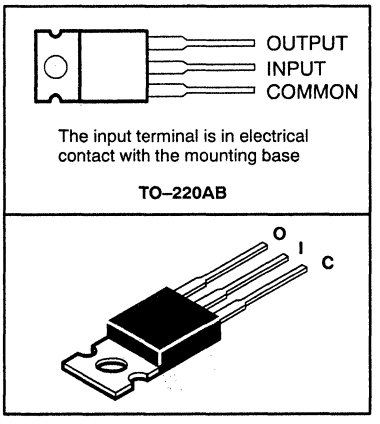
† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

- **3-Terminal Regulators**
- **Output Current Up to 1.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **High-Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Essentially Equivalent to National LM320 Series**

NOMINAL OUTPUT VOLTAGE	REGULATOR
−5 V	uA7905C
−5.2 V	uA7952C
−6 V	uA7906C
−8 V	uA7908C
−12 V	uA7912C
−15 V	uA7915C
−18 V	uA7918C
−24 V	uA7924C

KC PACKAGE
(TOP VIEW)



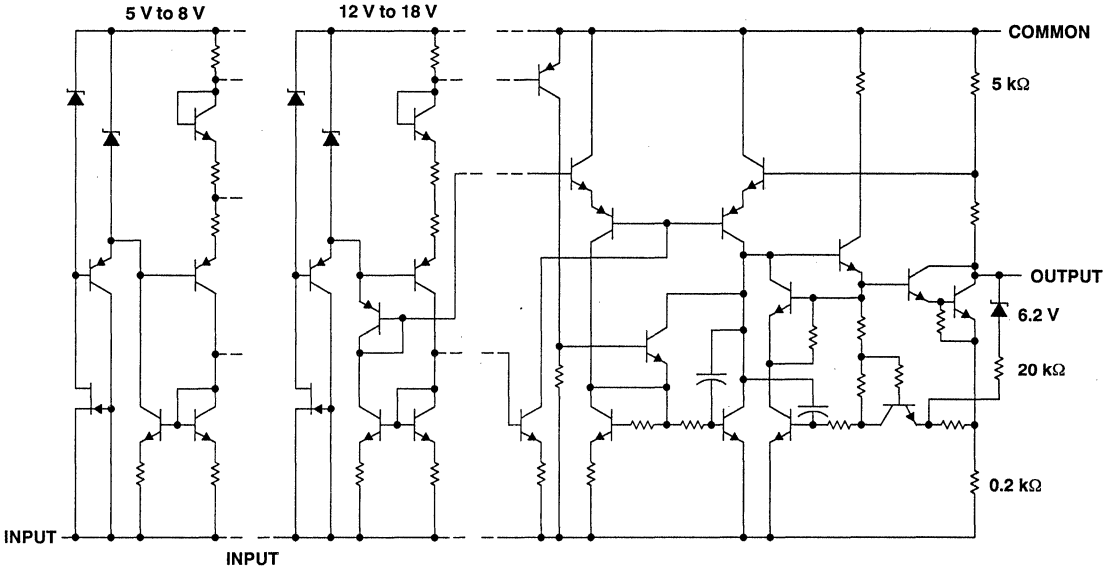
The input terminal is in electrical contact with the mounting base

TO–220AB

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA7800 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic



All component values are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Input voltage, V_I: uA7924C	−40 V
All others	−35 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1)	2 W
Continuous total dissipation at (or below) 90°C case temperature (see Note 1)	15 W
Operating free-air, case, or virtual junction temperature range	0 to 150°C
Storage temperature range	−65 to 150°C
Lead temperature 3.2 mm (1/8 inch) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or 90°C case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATATION DERATING CURVE

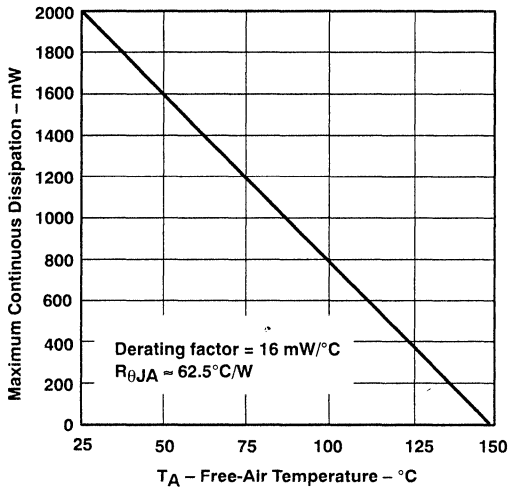


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

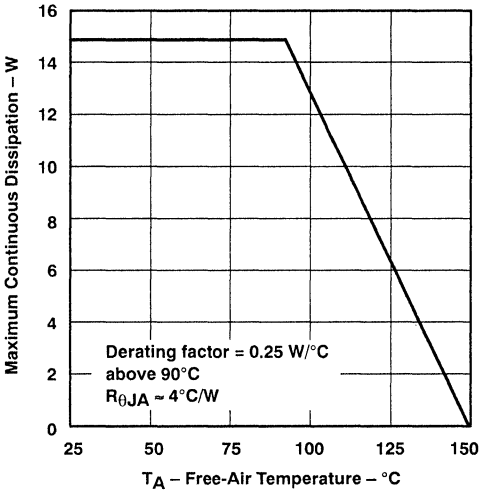


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7905C	−7	−25	V
	uA7952C	−7.2	−25	
	uA7906C	−8	−25	
	uA7908C	−10.5	−25	
	uA7912C	−14.5	−30	
	uA7915C	−17.5	−30	
	uA7918C	−21	−33	
	uA7924C	−27	−28	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7905C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−4.8	−5	−5.2	V
	I_O = 5 mA to 1 A, V_I = −7 V to −20 V, P ≤ 15 W	0°C to 125°C	−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V	25°C		12.5	50	mV
	V_I = −8 V to −12 V			4	15	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7 V to −25 V	0°C to 125°C		0.15	0.5	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7952C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−5	−5.2	−5.4	V
	I_O = 5 mA to 1 A, V_I = −7.2 V to −20 V, P ≤ 15 W	0°C to 125°C	−4.95		−5.45	
Input regulation	V_I = −7.2 V to −25 V	25°C		12.5	100	mV
	V_I = −8.2 V to −12 V			4	50	
Ripple rejection	V_I = −8.2 V to −18 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −7.2 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7906C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−5.75	−6	−6.25	V
	I_O = 5 mA to 1 A, V_I = −8 V to −21 V, P ≤ 15 W	0°C to 125°C	−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V	25°C		12.5	120	mV
	V_I = −9 V to −13 V			4	60	
Ripple rejection	V_I = −9 V to −19 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	120	mV
	I_O = 250 mA to 750 mA			5	60	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		150		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −8 V to −25 V	0°C to 125°C		0.15	1.3	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

electrical characteristics at specified virtual junction temperature, $V_I = -14$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7908C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−7.7	−8	−8.3	V
	I_O = 5 mA to 1 A, V_I = −10.5 V to −23 V, P ≤ 15 W	0°C to 125°C	−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V	25°C		12.5	160	mV
	V_I = −11 V to −17 V			4	80	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	160	mV
	I_O = 250 mA to 750 mA			5	80	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		200		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = −10.5 V to −25 V	0°C to 125°C		0.15	1	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7912C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−11.5	−12	−12.5	V
	I_O = 5 mA to 1 A, V_I = −14.5 V to −27 V, P ≤ 15 W	0°C to 125°C	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V	25°C		5	80	mV
	V_I = −16 V to −22 V			3	30	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		300		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −14.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7915C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−14.4	−15	−15.6	V
	I_O = 5 mA to 1 A, V_I = −17.5 V to −30 V, P ≤ 15 W	0°C to 125°C	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C		5	100	mV
	V_I = −20 V to −26 V			3	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		20	300	mV
	I_O = 250 mA to 750 mA			8	150	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		375		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −17.5 V to −30 V	0°C to 125°C		0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7918C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−17.3	−18	−18.7	V
	I_O = 5 mA to 1 A, V_I = −21 V to −33 V, P ≤ 15 W	0°C to 125°C	−17.1		−18.9	
Input regulation	V_I = −21 V to −33 V	25°C		5	360	mV
	V_I = −24 V to −30 V			3	180	
Ripple rejection	V_I = −22 V to −32 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		30	360	mV
	I_O = 250 mA to 750 mA			10	180	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		450		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −21 V to −33 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

electrical characteristics at specified virtual junction temperature, V_I = −33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	uA7924C			UNIT
			MIN	TYP	MAX	
Output voltage‡		25°C	−23	−24	−25	V
	I_O = 5 mA to 1 A, V_I = −27 V to −38 V, P ≤ 15 W	0°C to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V	25°C		5	480	mV
	V_I = −30 V to −36 V			3	240	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A	25°C		85	480	mV
	I_O = 250 mA to 750 mA			25	240	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		600		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = −27 V to −38 V	0°C to 125°C		0.04	1	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

D2216, JUNE 1976 – REVISED SEPTEMBER 1991

- **3-Terminal Regulators**
- **Output Current Up to 500 mA**
- **No External Components**
- **High Power Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**
- **Direct Replacements for Fairchild μA79M00 Series**

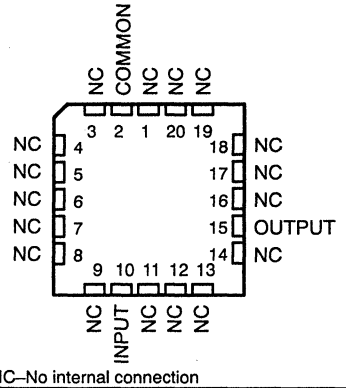
NOMINAL OUTPUT VOLTAGE	0°C TO 125°C OPERATING TEMPERATURE RANGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE
−5 V	uA79M05C	uA79M05M
−6 V	uA79M06C	
−8 V	uA79M08C	
−12 V	uA79M12C	uA79M12M
−15 V	uA79M15C	
−20 V	uA79M20C	
−24 V	uA79M24C	
Package	KC	FK, JG

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement the uA78M00 series in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 500 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

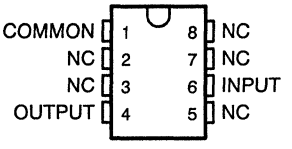
terminal assignments

uA79M_M . . . FK PACKAGE
(TOP VIEW)



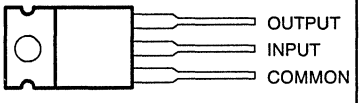
NC–No internal connection

uA79M_M . . . JG PACKAGE
(TOP VIEW)



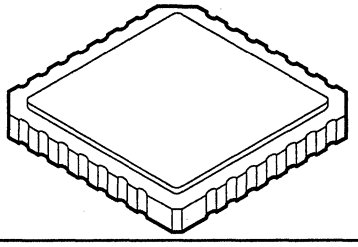
NC–No internal connection

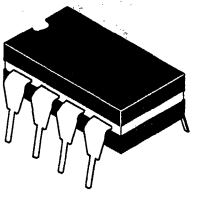
uA79M_C . . . KC PACKAGE
(TOP VIEW)

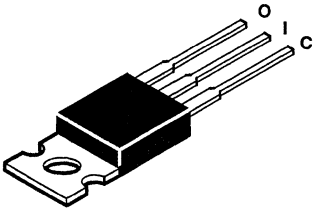


The input terminal is in electrical contact with the mounting base.

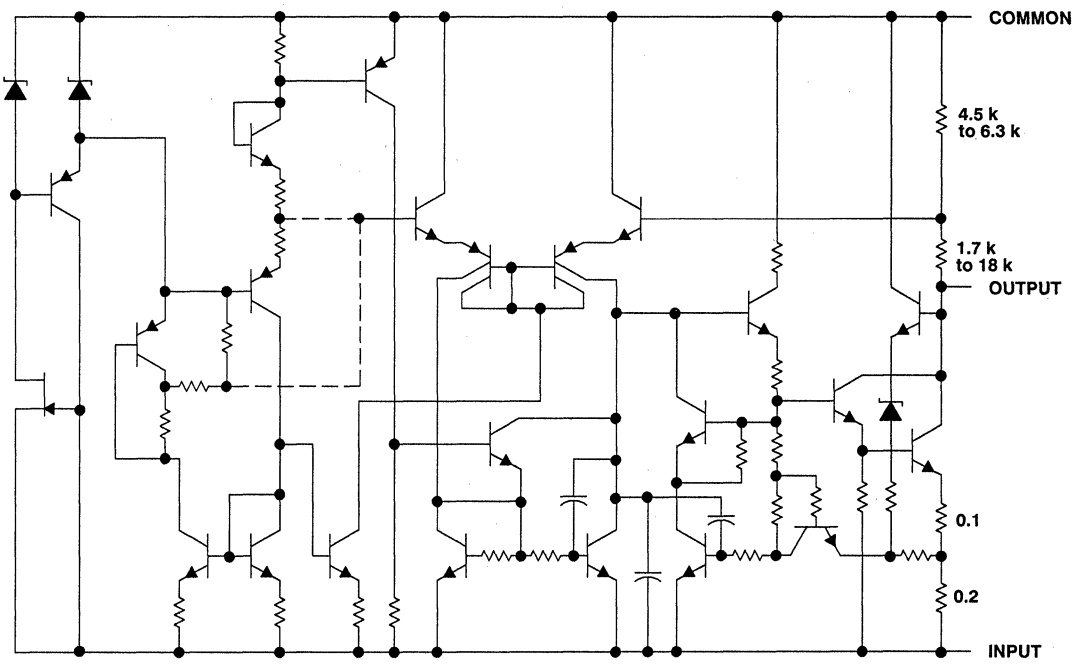
TO-220AB







schematic



Resistor values shown are nominal and in Ω.

absolute maximum ratings over operating temperature range (unless otherwise noted)

			uA79M05C THRU uA79M12C	uA79M05M AND uA79M12M	UNIT
Input voltage	uA79M20, uA79M24		−40		V
	All others		−35	− 35	
Continuous total dissipation (see Note 1)			See Dissipation Rating Tables 1 and 2		
Operating free-air, case, or virtual junction temperature range			0 to 150	−55 to 150	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Case temperature for 60 seconds		FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		JG package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		KC package	260		°C

NOTE 1: To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE 1–FREE-AIR TEMPERATURE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
KC	2000 mW	16 mW/°C	1280 mW	400 mW

DISSIPATION RATING TABLE 2–CASE TEMPERATURE

PACKAGE	$T_C \le 120°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 120°C$	$T_C = 125°C$ POWER RATING
KC	7.5 W	250 mW/°C	6.25 W

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA79M05C, uA79M05M	−7	−25	V
	uA79M06C	−8	−25	
	uA79M08C	−10.5	−25	
	uA79M12C, uA79M12M	−14.5	30	
	uA79M15C	−17.5	−30	
	uA79M20C	−23	−35	
	uA79M24C	−27	−38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J	uA79M05C thru uA79M24C	0	125	°C
	uA79M05M, uA79M12M	−55	150	

electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	uA79M05C			uA79M05M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−4.8	−5	−5.2	−4.8	−5	−5.2	V
	I_O = 5 mA to 350 mA,		−55°C to 150°C				−4.75		−5.25	
	V_I = −7 V to −25 V		0°C to 125°C	−4.75		−5.25				
Input regulation	V_I = −7 V to −25 V		25°C		7	50		7	50	mV
	V_I = −8 V to −18 V				3	30		3	30	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				50*			dB
			0°C to 125°C	50						
		I_O = 300 mA	25°C	54	60		54*	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	100		75	100	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C						−1.5*	mV/°C
			0°C to 125°C		−0.4					
Output noise voltage	f = 10 Hz to 100 kHz		25°C		125			125	400*	μV
Dropout voltage			25°C		1.1			1.1	2.3	V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −8 V to −25 V		−55°C to 150°C						0.4	mA
			0°C to 125°C			0.4				
	I_O = 5 mA to 350 mA		−55°C to 150°C						0.4	
			0°C to 125°C			0.4				
Short-circuit output current	V_I = −30 V		25°C		140				600	mA
Peak output current			25°C		0.65		0.5	0.65	1.4*	A

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	−5.75	−6	−6.25	V
	I_O = 5 mA to 350 mA,	V_I = −8 V to −25 V	0°C to 125°C	−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V		25°C		7	60	mV
	V_I = −9 V to −19 V				3	40	
Ripple rejection	V_I = −9 V to −19 V,	I_O = 100 mA	0°C to 125°C	50			dB
	f = 120 Hz	I_O = 300 mA	25°C	54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		80	120	mV
	I_O = 5 mA to 350 mA				55		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		150		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1	2	mA
Bias current change	V_I = −9 V to −25 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	−7.7	−8	−8.3	V
	I_O = 5 mA to 350 mA,	V_I = −10.5 V to −25 V	0°C to 125°C	−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V		25°C		8	80	mV
	V_I = −11 V to −21 V				4	50	
Ripple rejection	V_I = −11.5 V to −21.5 V,	I_O = 100 mA	0°C to 125°C	50			dB
	f = 120 Hz	I_O = 300 mA	25°C	54	59		
Output regulation	I_O = 5 mA to 500 mA		25°C		90	160	mV
	I_O = 5 mA to 350 mA				60		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		200		μV
Dropout voltage	I_O = 5 mA		25°C		1.1		V
Bias current			25°C		1	2	mA
Bias current change	V_I = −10.5 V to −25 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	uA79M12C			uA79M12M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡			25°C	−11.5	−12	−12.5	−11.5	−12	−12.5	V
	I_O = 5 mA to 350 mA, V_I = −14.5 V to −30 V		−55°C to 150°C				−11.4		−12.6	
			0°C to 125°C	−11.4		−12.6				
Input regulation	V_I = −14.5 V to −30 V		25°C		9	80		9	80	mV
	V_I = −15 V to −25 V				5	50		5	50	
Ripple rejection	V_I = −15V to −25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C				50*			dB
			0°C to 125°C	50						
		I_O = 300 mA	25°C	54	60		54*	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C						−3.6*	mV/°C
			0°C to 125°C		−0.8					
Output noise voltage	f = 10 Hz to 100 kHz		25°C		300			300	960*	μV
Dropout voltage			25°C		1.1			1.1	2.3	V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −14.5 V to −30 V		−55°C to 150°C						0.4	mA
			0°C to 125°C			0.4				
	I_O = 5 mA to 350 mA		−55°C to 150°C						0.4	
			0°C to 125°C			0.4				
Short-circuit output current	V_I = −30 V		25°C		140				600	mA
Peak output current			25°C		0.65		0.5*	0.65	1.4*	A

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡			25°C	−14.4	−15	−15.6	V
	I_O = 5 mA to 350 mA,	V_I = −17.5 V to −30 V	0°C to 125°C	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V		25°C		9	80	mV
	V_I = −18 V to −28 V				7	50	
Ripple rejection	V_I = −18.5 V to −28.5 V,	I_O = 100 mA	0°C to 125°C	50			dB
	f = 120 Hz	I_O = 300 mA	25°C	54	59		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240	mV
	I_O = 5 mA to 350 mA				45		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		375		μV
Dropout voltage	I_O = 5 mA		25°C		1.1		V
Bias current			25°C		1.5	3	mA
Bias current change	V_I = −17.5 V to −30 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA		0°C to 125°C			0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡	I_O = 5 mA to 350 mA, V_I = −23 V to −35 V		25°C	−19.2	−20	−20.8	V
			0°C to 125°C	−19		−21	
Input regulation	V_I = −23 V to −35 V		25°C		12	80	mV
	V_I = −24 V to −34 V				10	70	
Ripple rejection	V_I = −24 V to −34 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		500		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −23 V to −35 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA79M24C electrical characteristics at specified virtual junction temperature, V_I = −33 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_J†	MIN	TYP	MAX	UNIT
Output voltage‡	I_O = 5 mA to 350 mA, V_I = −27 V to −38 V		25°C	−23	−24	−25	V
			0°C to 125°C	−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V		25°C		12	80	mV
	V_I = −28 V to −38 V				12	70	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	I_O = 100 mA	0°C to 125°C	50			dB
		I_O = 300 mA	25°C	54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300	mV
	I_O = 5 mA to 350 mA				50		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz		25°C		600		μV
Dropout voltage			25°C		1.1		V
Bias current			25°C		1.5	3.5	mA
Bias current change	V_I = −27 V to −38 V		0°C to 125°C			0.4	mA
	I_O = 5 mA to 350 mA					0.4	
Short-circuit output current	V_I = −30 V		25°C		140		mA
Peak output current			25°C		0.65		A

† Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

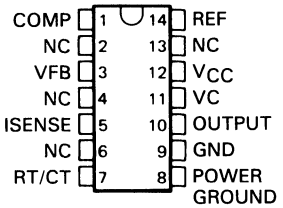
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

CURRENT-MODE PWM CONTROLLERS

D3175, JANUARY 1989—REVISED AUGUST 1991

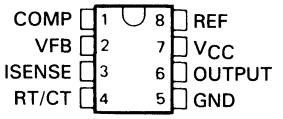
- Optimized for Off-Line and DC-to-DC Converters
- Low Start-Up Current (<1 mA)
- Automatic Feed-Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load-Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double Pulse Suppression
- High-Current Totem-Pole Output
- Internally Trimmed Bandgap Reference
- 500-kHz Operation
- Error Amplifier With Low Output Resistance
- Designed to Be Interchangable With Unitrode UC2842 and UC3842 Series

D PACKAGE
(TOP VIEW)



NC—No internal connection

P PACKAGE
(TOP VIEW)

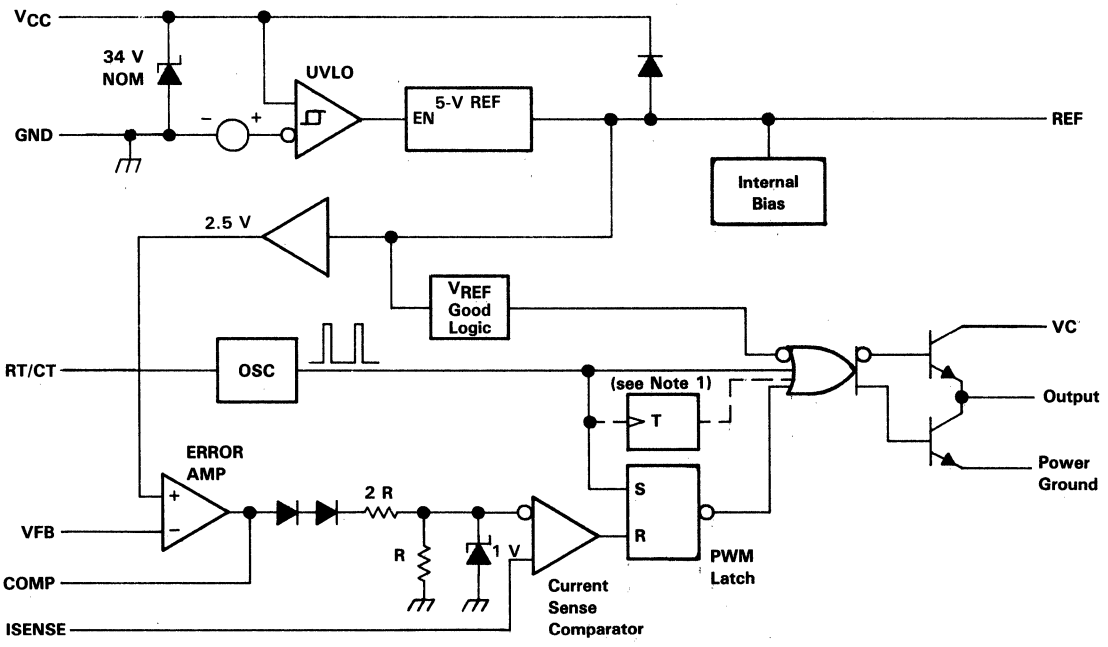


description

The UC2842 and UC3842 series of control integrated circuits provide the features that are necessary to implement off-line or dc-to-dc fixed-frequency current-mode control schemes with a minimum number of external components. Internally implemented circuits include: undervoltage lockout (UVLO) featuring a start-up current of less than 1 mA, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator (which also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

The primary difference between the UC2842-series devices and the UC3842-series devices is the ambient operating temperature range. The UC2842-series devices operate between −25°C and 85°C; the UC3842-series devices operate between 0°C and 70°C. Major differences between members of these series are the undervoltage lockout (UVLO) thresholds and maximum duty cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the UC__842 and UC__844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the UC__843 and UC__845 devices are 8.4 V on and 7.6 V off. The UC__842 and UC__843 devices can operate to duty cycles approaching 100%. A duty cycle range of 0 to 50% is obtained by the UC__844 and UC__845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.

functional block diagram



NOTE 1. The toggle flip-flop is present only in UC2844, UC2845, UC3844, and UC3845.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 2) (I_{CC} < 30 mA) . . . . . Self Limiting
Analog input voltage (VFB and ISENSE terminals) . . . . . −0.3 V to 6.3 V
Voltage on output pin . . . . . 35 V
Voltage on VC pin (14-pin package) . . . . . 35 V
Supply current, I_{CC} . . . . . 30 mA
Output current . . . . . ±1 A
Error amplifier output sink current . . . . . 10 mA
Continuous power dissipation . . . . . see Dissipation Rating Table
Output energy (capacitive load) . . . . . 5 μJ
Operating free-air temperature range, T_A: UC284_ . . . . . −25°C to 85°C
UC384_ . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 2: All voltages are with respect to the device GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

	UC284_			UC384_			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} and V_C†			30			30	V
Voltage on RT/CT input	0		5.5	0		5.5	V
Voltage on VFB and ISENSE inputs	0		5.5	0		5.5	V
Voltage on OUTPUT	0		30	0		30	V
Voltage on POWER GROUND†	−0.1		1	−0.1		1	V
Supply current, externally limited, I_{CC}			25			25	mA
Average output current, I_O			200			200	mA
Reference output current			−20			−20	mA
Timing capacitance, C_T	1			1			nF
Oscillator frequency		100	500		100	500	kHz
Operating free-air temperature, T_A	−25		85	0		70	°C

†These recommended voltages for V_C and POWER GROUND apply only to the D package.

electrical characteristics, V_{CC} = 15 V (see Note 3), R_T = 10 kΩ, C_T = 3.3 nF, T_A = full range (unless otherwise specified)

reference section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Output voltage	I_O = 1 mA, T_J = 25°C	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC} = 12 V to 25 V		6	20		6	20	mV
Load regulation	I_O = 1 mA to 20 mA		6	25		6	25	mV
Temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/°C
Output voltage with worst-case variation	V_{CC} = 12 V to 25 V, I_O = 1 mA to 20 mA	4.9		5.1	4.82		5.18	V
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C		50			50		μV
Output voltage long-term drift	After 1000 h at T_A = 125°C		5	25		5	25	mV
Short-circuit output current		−30	−100	−180	−30	−100	−180	mA

oscillator section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Oscillator frequency (see Note 4)	T_J = 25°C	47	52	57	47	52	57	kHz
Frequency change with supply voltage	V_{CC} = 12 V to 25 V		0.2%	1%		0.2%	1%	
Frequency change with temperature	T_A = T_{MIN} to T_{MAX}		5%			5%		
Peak-to-peak amplitude at RT/CT			1.7			1.7		V

error amplifier section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Feedback input voltage	COMP at 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input bias current			−0.3	−1		−0.3	−2	μA
Open-loop voltage amplification	V_O = 2 V to 4 V	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply voltage rejection ratio	V_{CC} = 12 V to 25 V	60	70		60	70		dB
Output sink current	VFB at 2.7 V, COMP at 1.1 V	2	6		2	6		mA
Output source current	VFB at 2.3 V, COMP at 5 V	−0.5	−0.8		−0.5	−0.8		mA
High-level output voltage	VFB at 2.3 V, R_L = 15 kΩ to GND	5	6		5	6		V
Low-level output voltage	VFB at 2.7 V, R_L = 15 kΩ to pin 8		0.7	1.1		0.7	1.1	V

†All typical values are at T_J = 25°C.

NOTES: 3. Adjust V_{CC} above the start threshold before setting it to 15 V.

4. Output frequency equals oscillator frequency for the UC_842 and UC_843. Output frequency is one-half oscillator frequency for the UC_844 and UC_845.

electrical characteristics, V_{CC} = 15 V (see Note 3), R_T = 10 kΩ, C_T = 3.3 nF, T_A = full range (unless otherwise specified) (continued)

current sense section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Voltage amplification	See Notes 5 and 6	2.85	3	3.13	2.85	3	3.15	V/V
Current sense comparator threshold	COMP at 5 V, See Note 5	0.9	1	1.1	0.9	1	1.1	V
Supply voltage rejection ratio	V_{CC} = 12 V to 25 V, See Note 5		70			70		dB
Input bias current			−2	−10		−2	−10	μA
Delay time to output			150	300		150	300	ns

output section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
High-level output voltage	I_{OH} = −20 mA	13	13.5		13	13.5		V
	I_{OH} = −200 mA	12	13.5		12	13.5		
Low-level output voltage	I_{OL} = 20 mA		0.1	0.4		0.1	0.4	V
	I_{OL} = 200 mA		1.5	2.2		1.5	2.2	
Rise time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns
Fall time	C_L = 1 nF, T_J = 25°C		50	150		50	150	ns

undervoltage lockout section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start threshold voltage	UC_842, UC_844	15	16	17	14.5	16	17.5	V
	UC_843, UC_845	7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after start-up	UC_842, UC_844	9	10	11	8.5	10	11.5	V
	UC_843, UC_845	7	7.6	8.2	7	7.6	8.2	

pulse-width-modulator section

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Maximum duty cycle	UC_842, UC_843	95%	97%	100%	95%	97%	100%	
	UC_844, UC_845	46%	48%	50%	46%	48%	50%	
Minimum duty cycle				0			0	

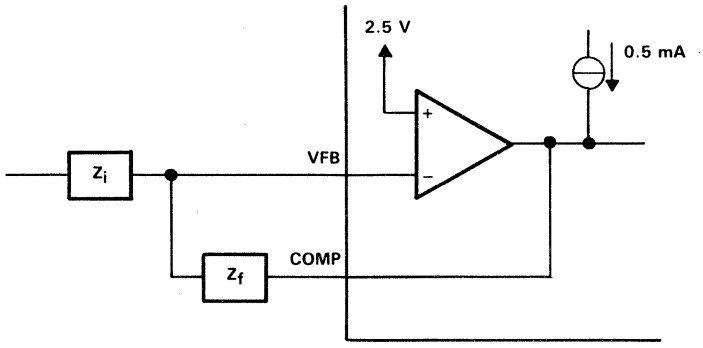
supply voltage

PARAMETER	TEST CONDITIONS	UC284_			UC384_			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
Start-up current			0.5	1		0.5	1	mA
Operating supply current	VFB and ISENSE at 0 V		11	17		11	17	mA
Limiting voltage	I_{CC} = 25 mA		34			34		V

†All typical values are at T_J = 25°C.

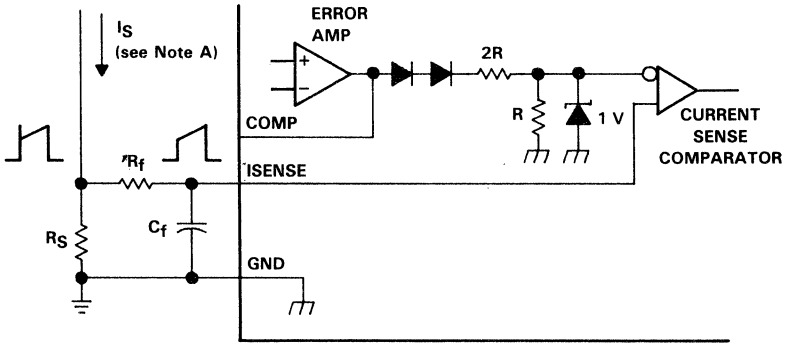
NOTES: 3. Adjust V_{CC} above the start threshold before setting it to 15 V.
5. These parameters are measured at the trip point of the latch with VFB at 0 V.
6. Voltage amplification is measured between the input at ISENSE and the output at COMP with the input changing from 0 V to 0.8 V.

APPLICATION INFORMATION



Note: Error amplifier can source or sink up to 0.5 mA

Figure 1. Error Amplifier Configuration



Note A: Peak current (I_S) is determined by the formula:

$$I_{Smax} \approx \frac{1\ V}{R_S}$$

A small RC filter formed by resistor R_f and capacitor C_f may be required to suppress switch transients.

Figure 2. Current Sense Circuit

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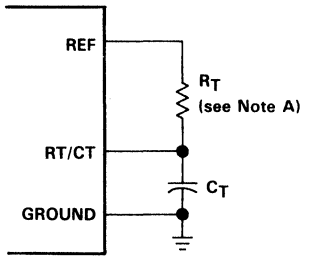
APPLICATION INFORMATION



Note A: For $R_T > 5\ k\Omega$ $\quad f \approx \frac{1.72}{R_T C_T}$

Figure 3. Oscillator Section

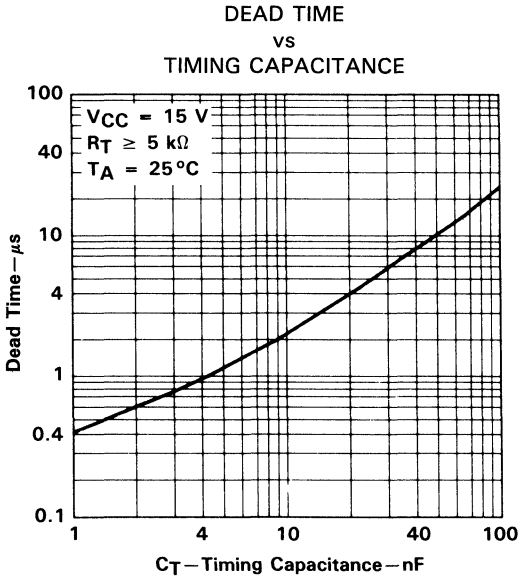


Figure 4

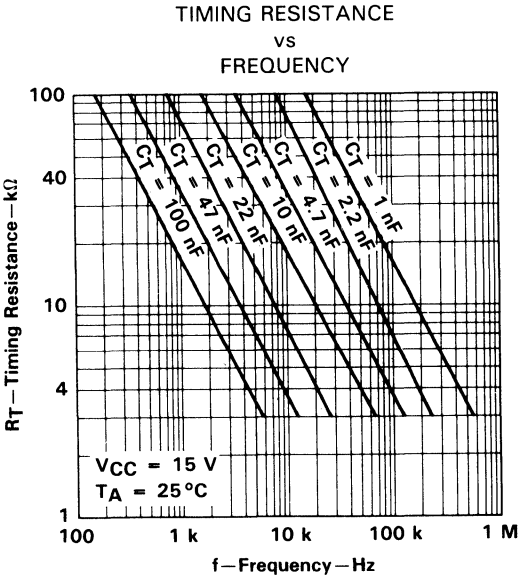


Figure 5

APPLICATION INFORMATION

open-loop laboratory test fixture

In the open-loop laboratory test fixture shown in Figure 6, high-peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single point ground. The transistor and 5-kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

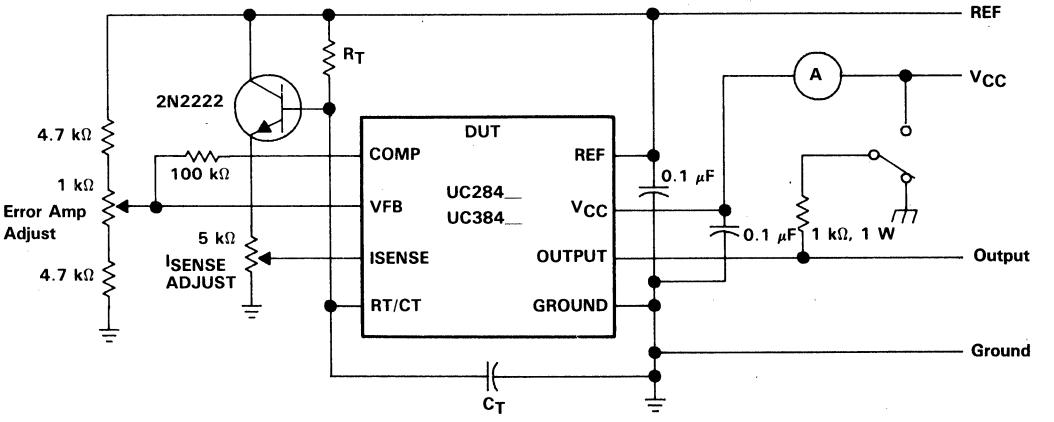


Figure 6. Open-Loop Laboratory Test Fixture

shutdown technique

Shutdown of the PWM controller (see Figure 7) can be accomplished by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR that will be reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

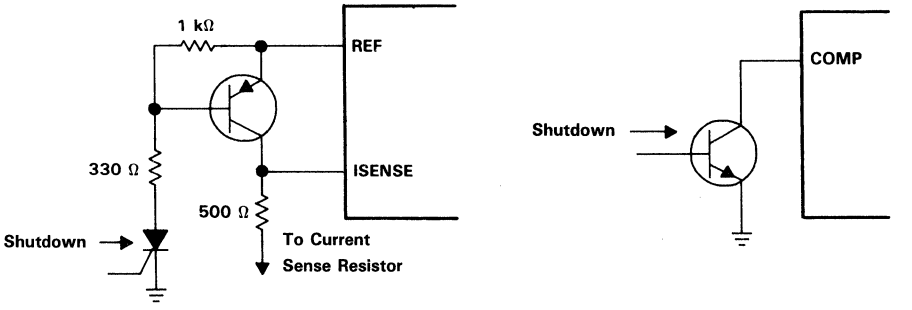


Figure 7. Shutdown Techniques

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APPLICATION INFORMATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 8). Note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

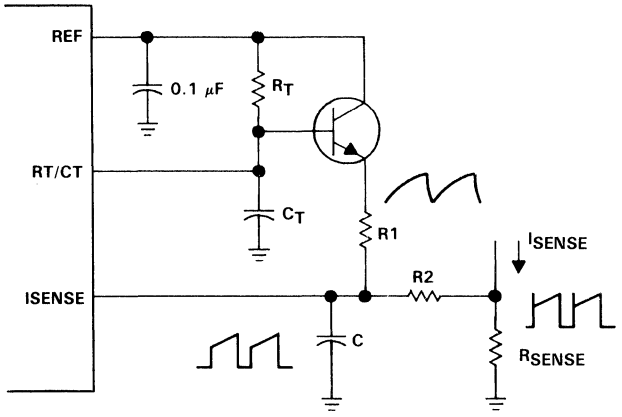


Figure 8. Slope Compensation

General Information 1
VRegs/Supervisors and Bldg Blocks 2
Comparators 3
Special Functions 4
Thermal Design Considerations 5
Mechanical Data 6

3 Comparators

D1312, SEPTEMBER 1973–REVISED FEBRUARY 1992

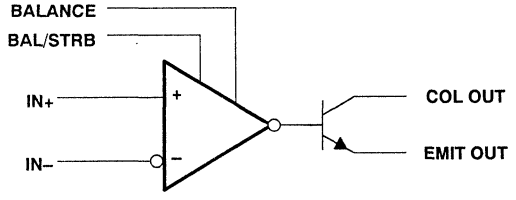
- **Fast Response Times**
- **Strobe Capability**
- **Maximum Input Bias Current . . . 300 nA**
- **Maximum Input Offset Current . . . 70 nA**
- **Can Operate From Single 5-V Supply**
- **Designed to Be Interchangeable With National Semiconductor LM111, LM211, and LM311**

description

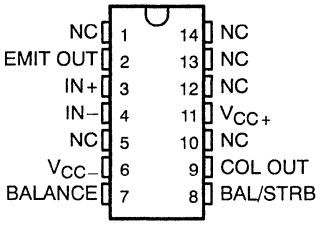
The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltages, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of −55°C to 125°C. The LM211 is characterized for operation from −40°C to 85°C, and the LM311 is characterized for operation from 0°C to 70°C.

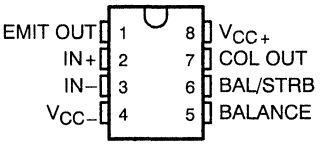
functional block diagram



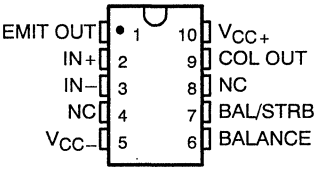
LM111 . . . J PACKAGE
(TOP VIEW)



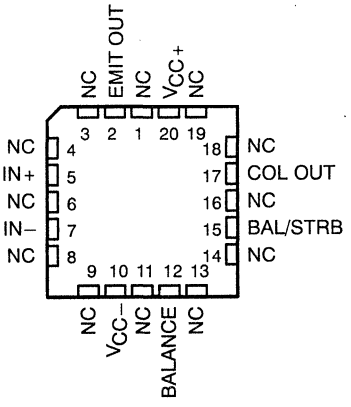
LM111 . . . JG PACKAGE
LM211, LM311 . . . D, DB, P, OR PW PACKAGE
(TOP VIEW)



LM111 . . . U PACKAGE
(TOP VIEW)



LM111 . . . FK PACKAGE
(TOP VIEW)



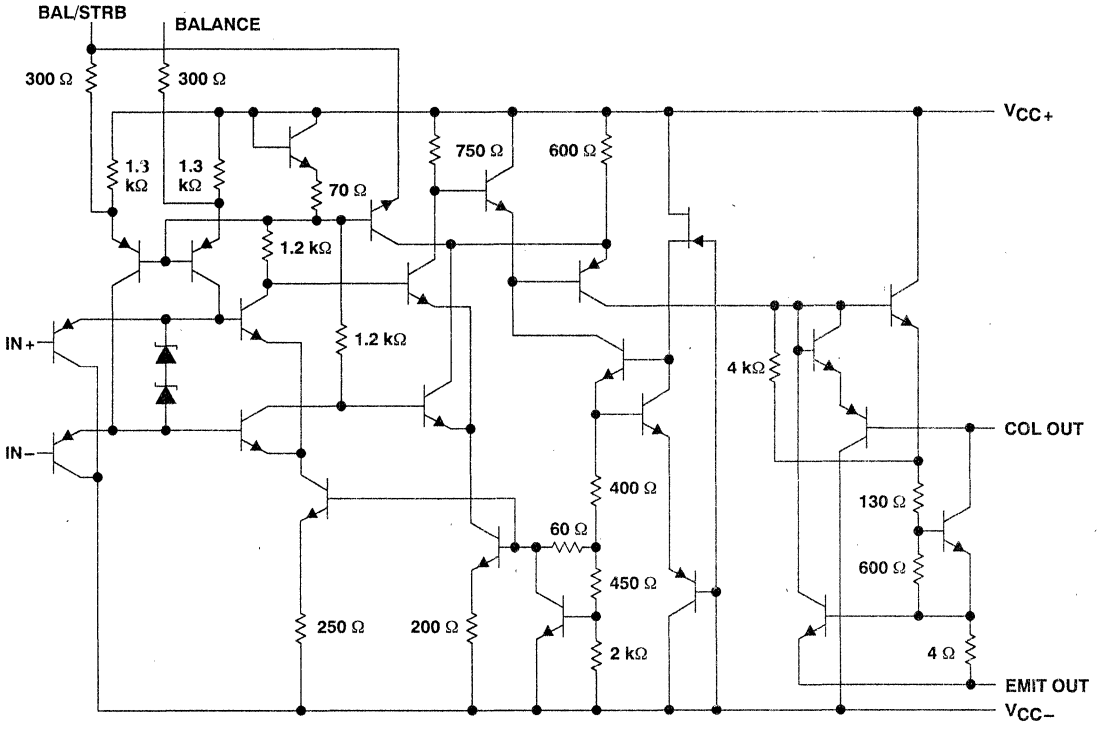
NC–No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE								
		SMALL OUTLINE (D)†	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLATPACK (U)	CHIP FORM (Y)‡
0°C to 70°C	7.5 mV	LM311D	LM311DBLE				LM311P	LM311PWLE		LM311Y
−40°C to 85°C	3 mV	LM211D					LM211P			
−55°C to 125°C	3 mV			LM111FK	LM111J	LM111JG			LM111U	

† The D package is available taped and reeled. Add the suffix R (e.g., LM311DR). The DB and PW packages are only available left-end taped and reeled.
‡ Chips are tested at 25°C.

schematic



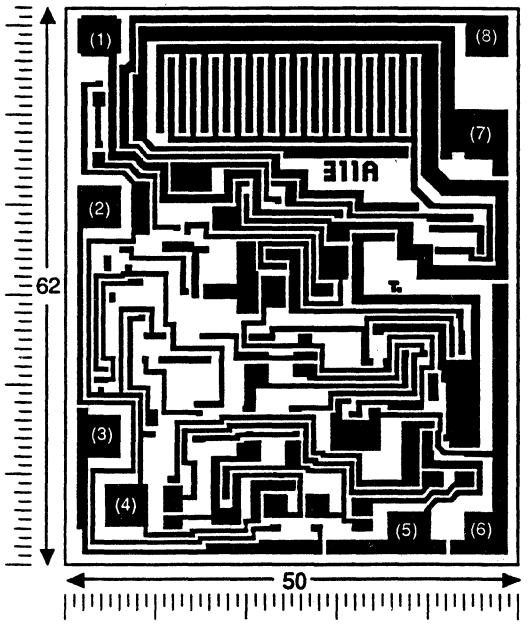
IN+	Noninverting input	Component Count:
IN−	Inverting input	Resistors – 20
V_{CC+}	Positive supply voltage	Diodes – 2
V_{CC-}	Negative supply voltage	Epifet – 1
		Transistors – 22

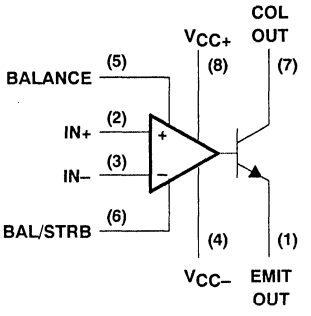
All resistor values shown are nominal.

chip information

These chips, properly assembled, display characteristics similar to the LM311 (see electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}, (see Note 1) ..... 18 V
Supply voltage, V_{CC-}, (see Note 1) ..... −18 V
Supply voltage, $V_{CC+} - V_{CC-}$ ..... 36 V
Differential input voltage (see Note 2) ..... ±30 V
Input voltage (either input, see Notes 1 and 3) ..... ±15 V
Voltage from emitter output to V_{CC-} ..... 30 V
Voltage from collector output to V_{CC-}: LM111 ..... 50 V
LM211 ..... 50 V
LM311 ..... 40 V
Duration of output short circuit (see Note 4) ..... 10 s
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: LM111 ..... −55°C to 125°C
LM211 ..... −40°C to 85°C
LM311 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or U package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, DB, P, or PW package ..... 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
DB or PW	500 mW	4.2 mW/°C	31°C	336 mW	–	–
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC+} - V_{CC-}$		3.5	30	V
Input voltage ($\lvert V_{CC\pm}\rvert \le 15$ V)		$V_{CC-} + 0.5$	$V_{CC+} - 1.5$	V
Operating free-air temperature range, T_A	LM111	−55	125	°C
	LM211	−40	85	
	LM311	0	70	

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LM111, LM211			LM311			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	See Note 5		25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See Note 5		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	V_O = 1 V to 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current (see Note 6)	$V_{(strobe)}$ = 0.3 V,	$V_{ID} \le -10$ mV	25°C		−3			−3		mA
V_{ICR}	Common-mode input voltage range			Full range	13 to −14.5	13.8 to −14.7		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V,	R_L = 1 kΩ	25°C	40	200		40	200		V/mV
I_{OH}	High-level (collector) output current	I_{strobe} = −3 mA, V_{ID} = 5 mV,	V_{OH} = 35 V	25°C		0.2	10				nA
				Full range			0.5				μA
		V_{ID} = 5 mV,	V_{OH} = 35 V	25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA	V_{ID} = −5 mV	25°C		0.75	1.5				V
			V_{ID} = −10 mV	25°C					0.75	1.5	
		V_{CC+} = 4.5 V, V_{CC-} = 0, I_{OL} = 8 mA	V_{ID} = −6 mV	Full range		0.23	0.4				
			V_{ID} = −10 mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output high	V_{ID} = 10 mV,	No load	25°C		−4.1	−5		−4.1	−5	mA

† Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and the emitter output grounded. Full range for LM111 is −55°C to 125°C, for LM211 is −40°C to 85°C, and for LM311 is 0°C to 70°C.

‡ All typical values are at T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to V_{CC+}. These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 mA to −5 mA, see Figures 13 and 27.

switching characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	See Note 5		2	7.5	mV
I_{IO}	Input offset current	See Note 5		6	50	nA
I_{IB}	Input bias current	V_O = 1 V to 14 V		100	250	nA
$I_{IL(S)}$	Low-level strobe current (see Note 6)	V_{strobe} = 0.3 V, $V_{ID} \le -10$ mV		−3		mA
V_{ICR}	Common-mode input voltage range		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V, R_L = 1 kΩ	40	200		V/mV
I_{OH}	High-level (collector) output current	I_{strobe} = −3 mA, V_{ID} = 5 mV, V_{OH} = 35 V		0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA, V_{ID} = −10 mV		0.75	1.5	V
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV, No load		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output low	V_{ID} = 10 mV, No load		−4.1	−5	mA

† Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and the emitter output grounded.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to V_{CC+}. These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 mA to −5 mA, see Figures 13 and 27.

switching characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

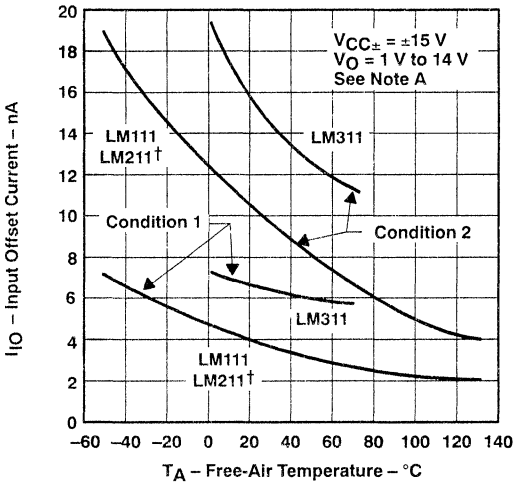


Figure 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

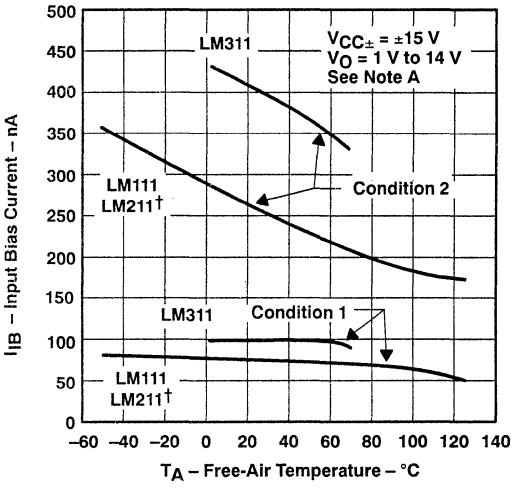
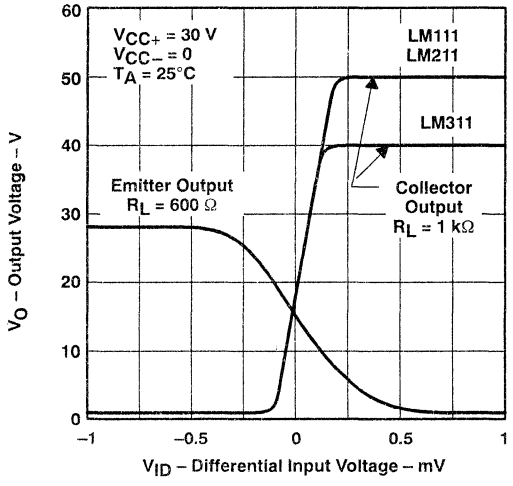
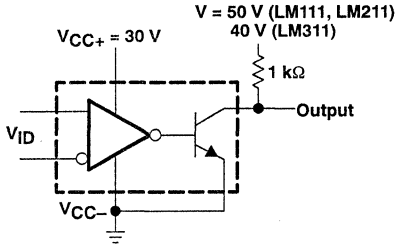


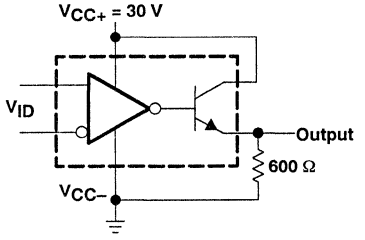
Figure 2

VOLTAGE TRANSFER CHARACTERISTICS





COLLECTOR OUTPUT TRANSFER CHARACTERISTIC
TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC
TEST CIRCUIT FOR FIGURE 3

Figure 3

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE A: Condition 1 is with BALANCE and BAL/STRB open. Condition 2 is with BALANCE and BAL/STRB connected to V_{CC+}.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

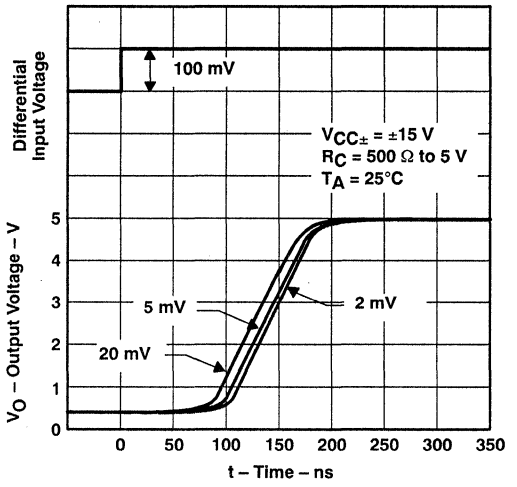


Figure 4

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

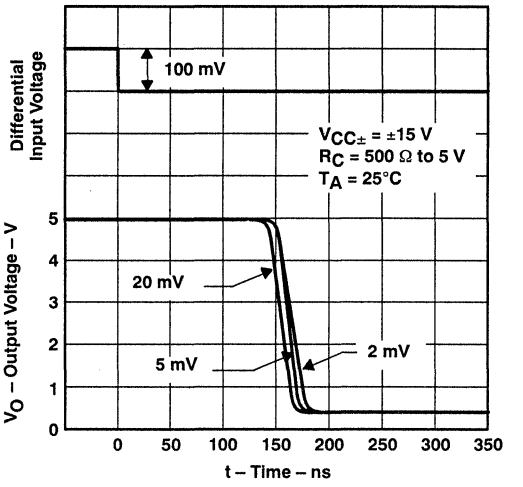
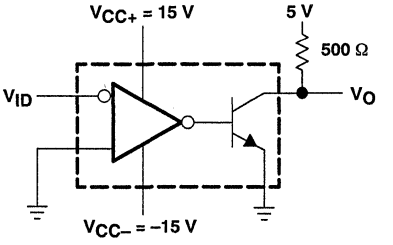


Figure 5



TEST CIRCUIT FOR FIGURES 4 AND 5

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

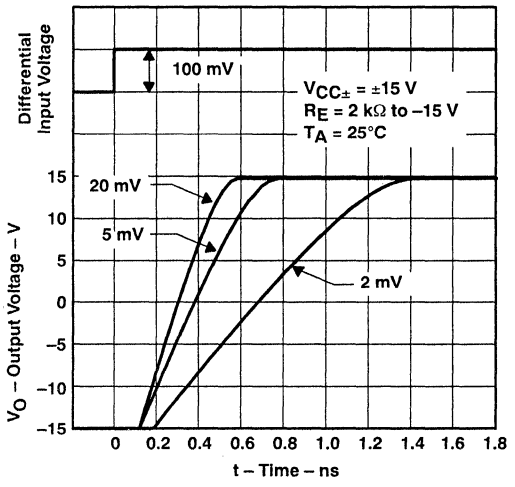


Figure 6

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

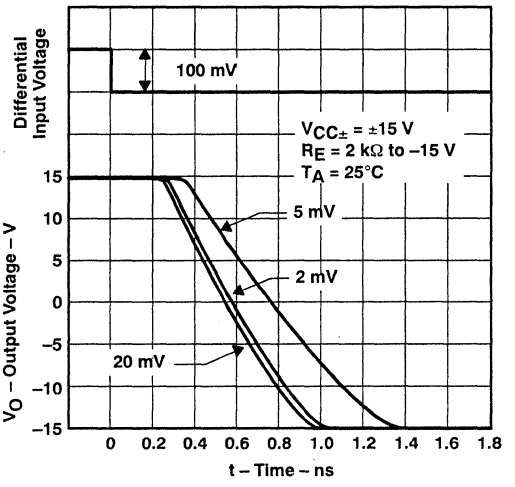
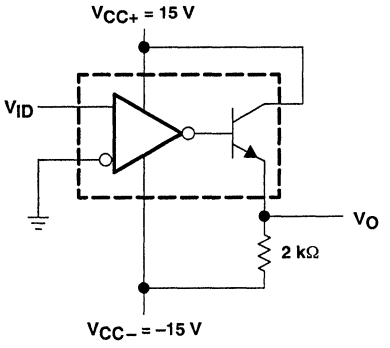


Figure 7



TEST CIRCUIT FOR FIGURES 6 AND 7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT AND DISSIPATION
vs
OUTPUT VOLTAGE

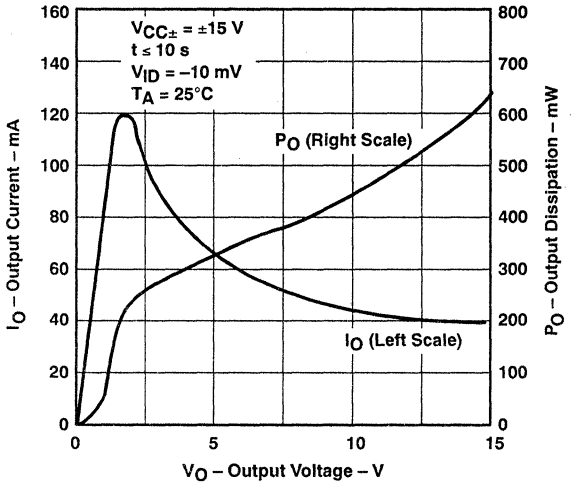


Figure 8

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

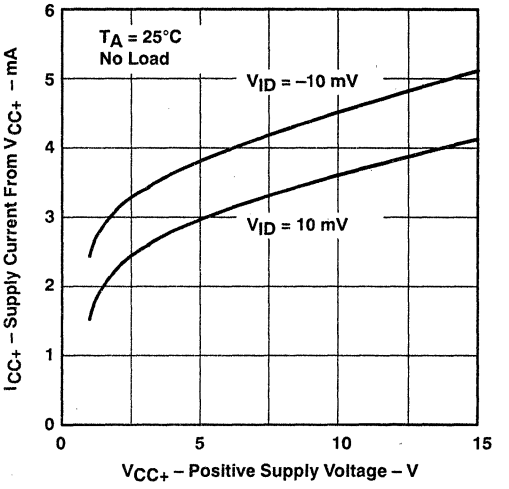


Figure 9

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

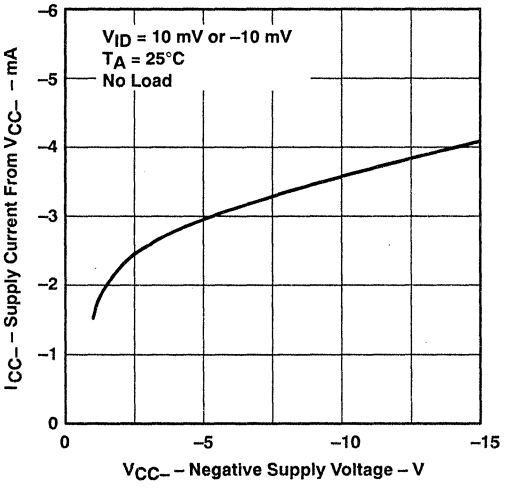


Figure 10

APPLICATION INFORMATION

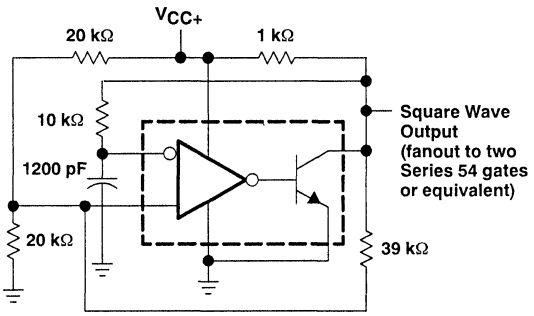


Figure 11. 100-kHz Free-Running Multivibrator

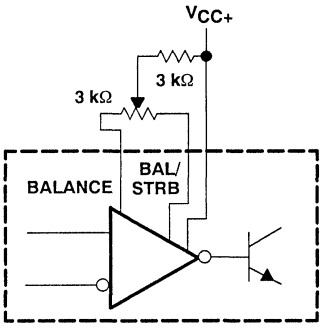


Figure 12. Offset Balancing

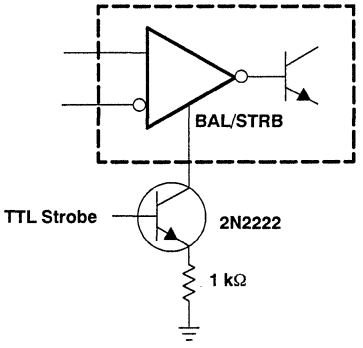


Figure 13. Strobing

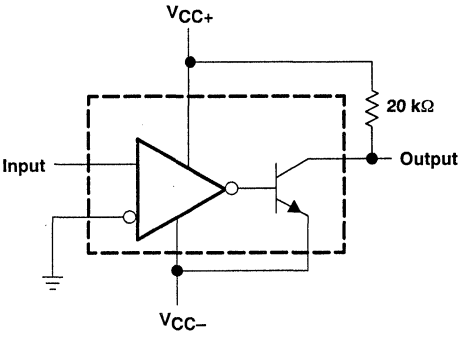
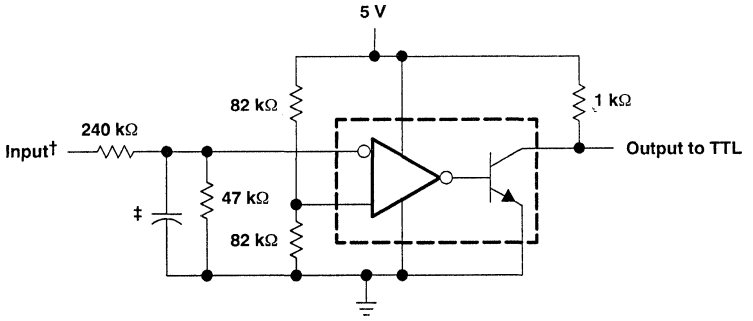


Figure 14. Zero-Crossing Detector



† Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.
‡ May be added to control speed and reduce susceptibility to noise spikes.

Figure 15. TTL Interface With High-Level Logic

APPLICATION INFORMATION

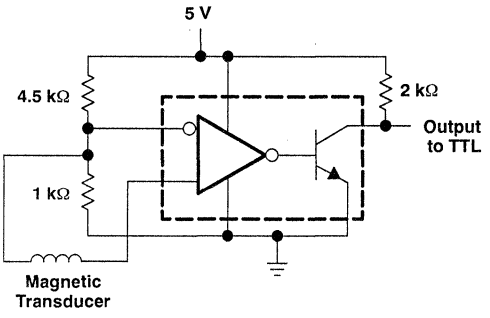


Figure 16. Detector for Magnetic Transducer

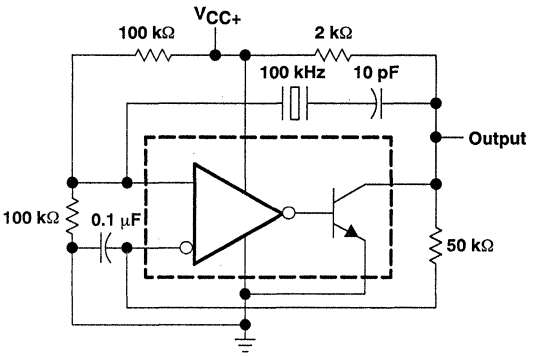


Figure 17. 100-kHz Crystal Oscillator

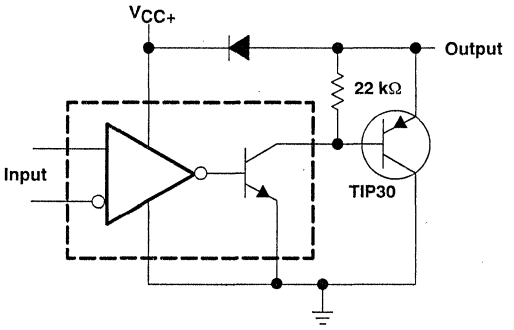
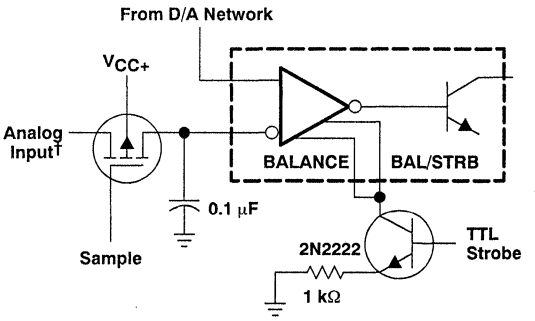


Figure 18. Comparator and Solenoid Driver



†Typical input current is 50 pA with inputs strobed off.

Figure 19. Strobing Both Input and Output Stages Simultaneously

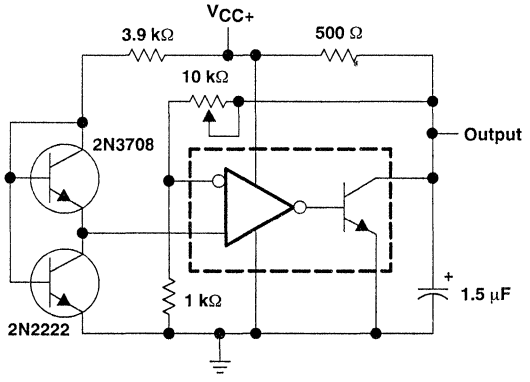


Figure 20. Low-Voltage Adjustable Reference Supply

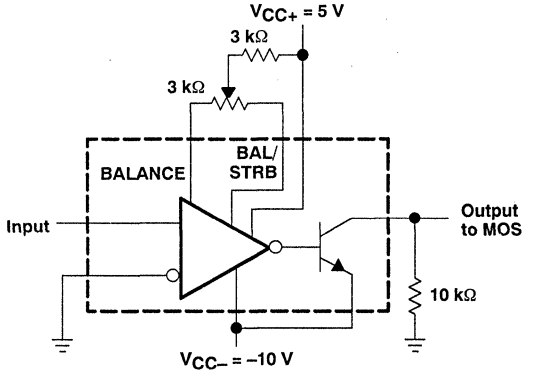
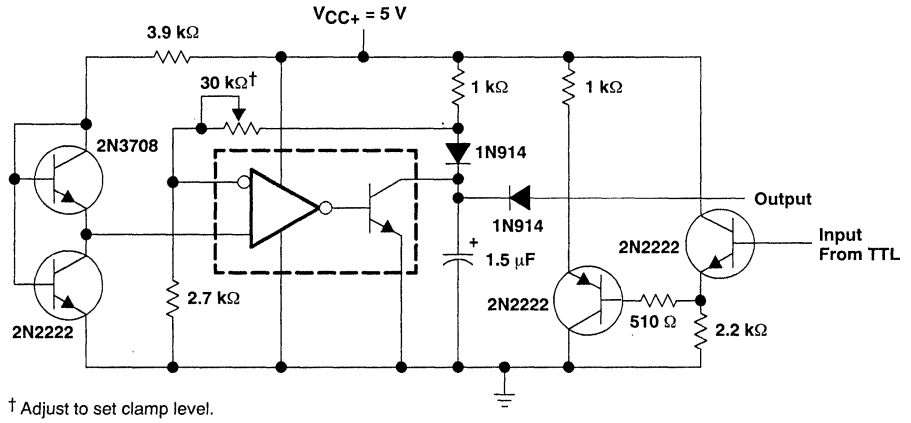


Figure 21. Zero-Crossing Detector Driving MOS Logic

APPLICATION INFORMATION



† Adjust to set clamp level.

Figure 22. Precision Squarer

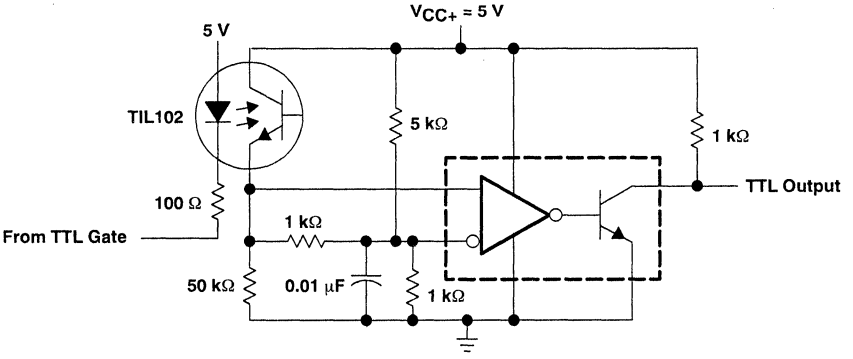


Figure 23. Digital Transmission Isolator

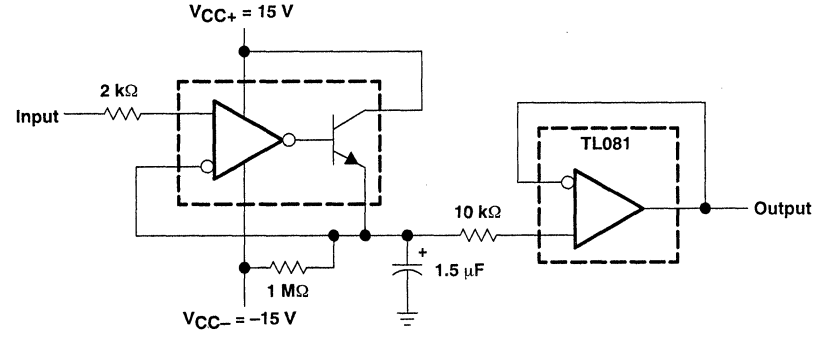


Figure 24. Positive-Peak Detector

APPLICATION INFORMATION

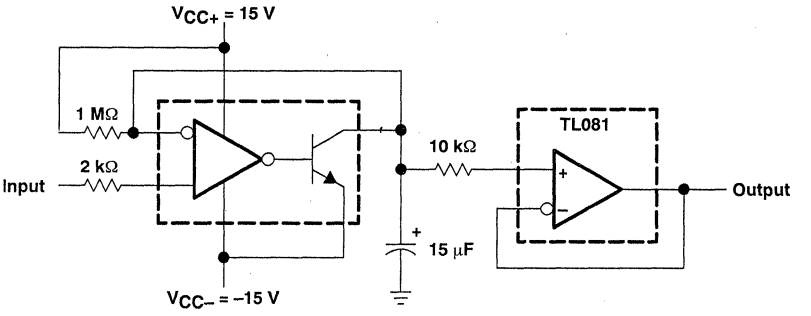
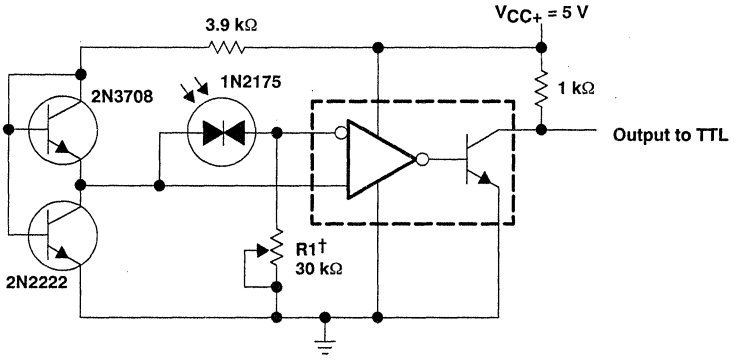
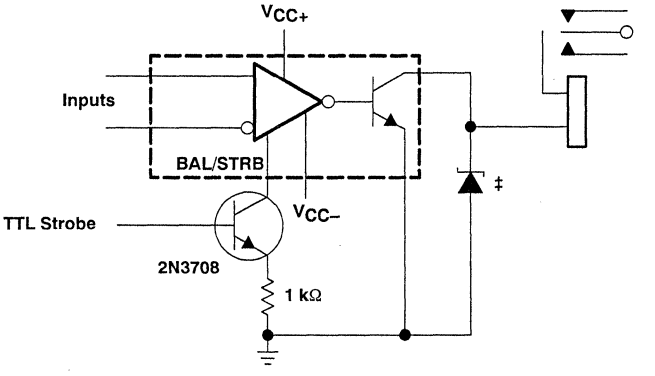


Figure 25. Negative-Peak Detector



† R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it decreasing dark current by an order of magnitude.

Figure 26. Precision Photodiode Comparator



‡ Transient voltage and inductive kickback protection

Figure 27. Relay Driver With Strobe

TEXAS INSTRUMENTS
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APPLICATION INFORMATION

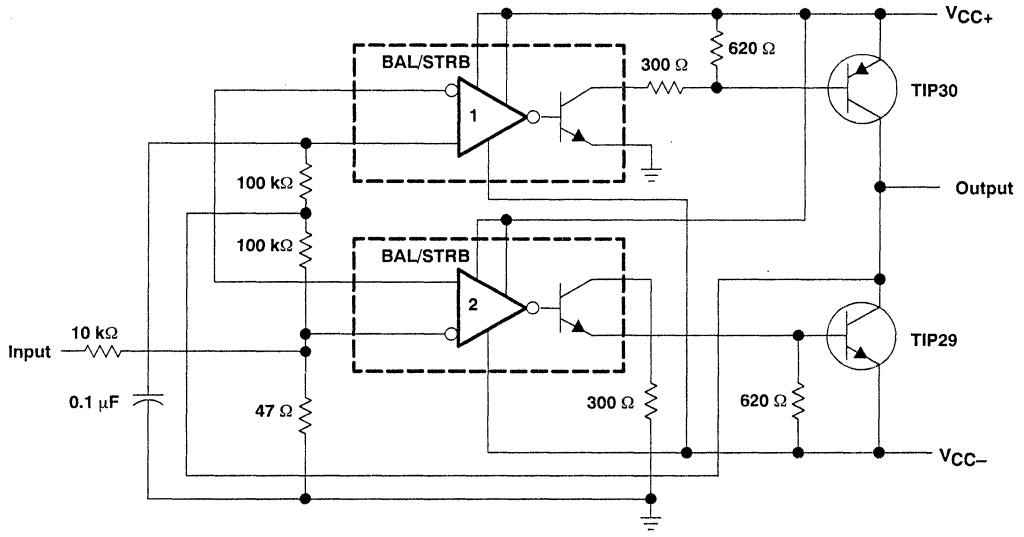


Figure 28. Switching Power Amplifier

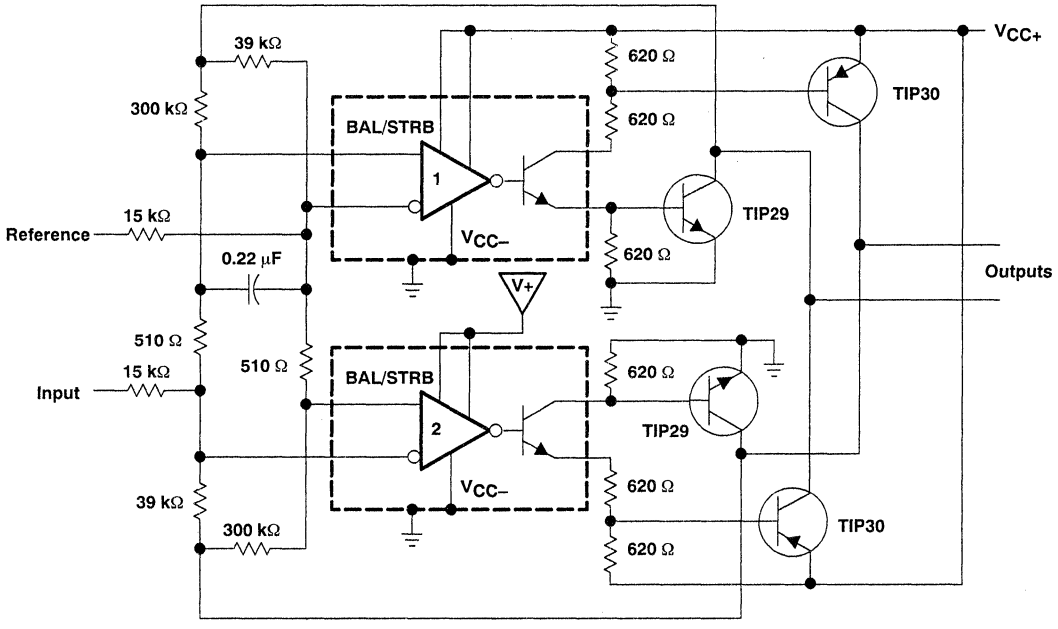
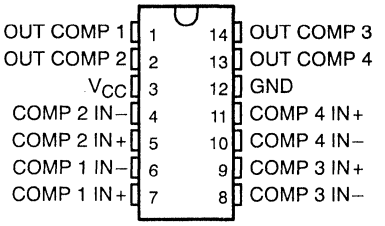


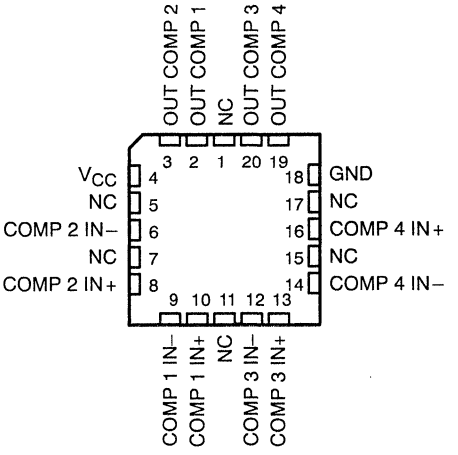
Figure 29. Switching Power Amplifiers

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage 2 V to 36 V**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ (LM139)**
- **Low Input Offset Voltage . . . 2 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

D, DB, J, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



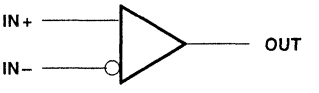
NC–No internal connection

description

These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wire-AND relationships.

The LM139 and LM139A are characterized for operation from −55°C to 125°C. The LM239 and LM239A are characterized for operation from −25°C to 125°C. The LM339 and LM339A are characterized for operation from 0°C to 70°C. The LM2901 and LM2901Q are characterized for operation from −40°C to 85°C.

symbol (each comparator)



AVAILABLE OPTIONS

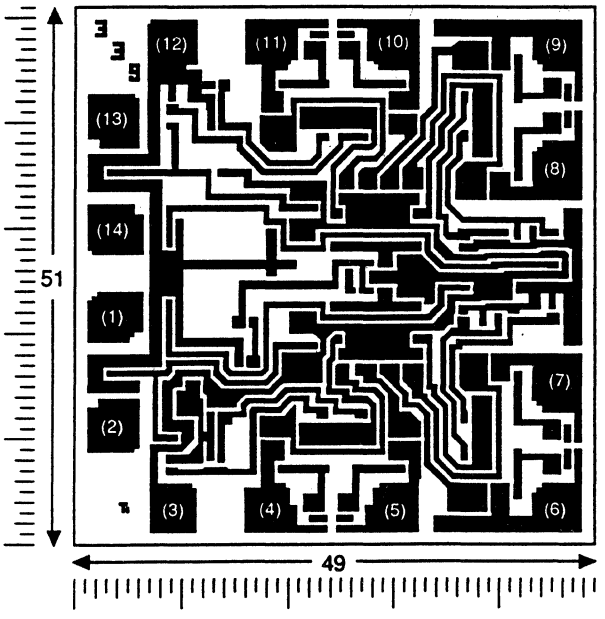
T_A	V_{IO} max at 25°C	PACKAGE						CHIP FORM (Y)§
		SMALL OUTLINE (D)†	SSOP (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)‡	
0°C to 70°C	5 mV 2 mV	LM339D LM339AD	LM339DBLE			LM339N LM339AN	LM339PWLE	LM339Y
−25°C to 85°C	5 mV 2 mV	LM239D LM239AD				LM239N LM239AN		
−40°C to 125°C	7 mV	LM2901D LM2901QD	LM2901DBLE			LM2901N LM2901QN	LM2901PWLE	
−55°C to 125°C	5 mV 2 mV	LM139D LM139AD		LM139FK LM139AFK	LM139J LM139AJ	LM139N LM139AN		

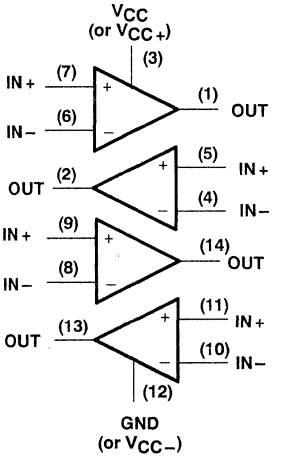
† The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM339DR).
‡ The DB and PW packages are only available left-end taped and reeled.
§ Chips are tested at 25°C. See electrical characteristics.

chip information

These chips, properly assembled, display characteristics similar to the LM339 (see electrical table on the LM339Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

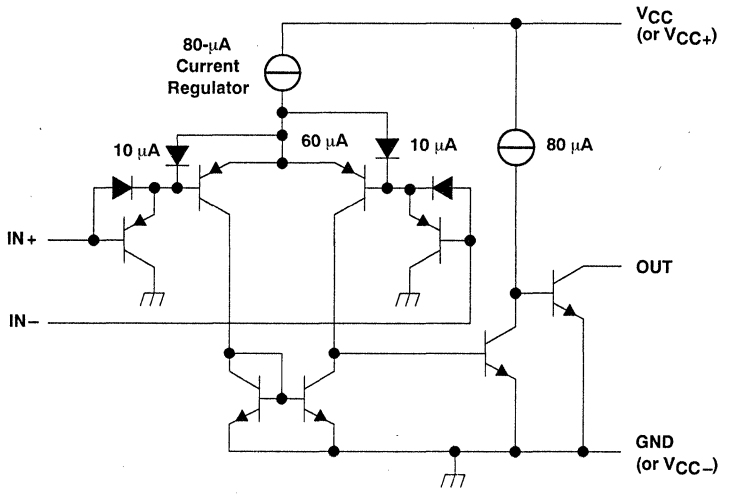
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

schematic (each comparator)



All current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 36 V
Differential input voltage (see Note 2) . . . . . ±36 V
Input voltage range (either input) . . . . . −0.3 V to 36 V
Output voltage . . . . . 36 V
Output current . . . . . 20 mA
Duration of output short circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: LM139, LM139A . . . . . −55°C to 125°C
LM239, LM239A . . . . . −25°C to 85°C
LM339, LM339A . . . . . 0°C to 70°C
LM2901, LM2901Q . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, N, or PW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	31°C	608 mW	494 mW	–
DB	775 mW	6.2 mW/°C	25°C	496 mW	403 mW	155 mW
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	–
PW	700 mW	5.6 mW/°C	25°C	448 mW	364 mW	140 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM139			LM139A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		25°C		2	5		1	2	mV
				−55°C to 125°C			9			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		3	25	nA
				−55°C to 125°C			100			100	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−100		−25	−100	nA
				−55°C to 125°C			−300			−300	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				−55°C to 125°C	0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±7.5 V, V_O = −5 V to 5 V		25°C		200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	−55°C to 125°C			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				−55°C to 125°C			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8	2		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.
‡ All typical values measured at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3		μs
	C_L = 15 pF§, See Note 4	TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM239, LM339			LM239A, LM339A			LM2901, LM2901Q			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		25°C		2	5		1	2		2	7	mV
				Full range			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50		5	50		5	50	nA
				Full range			150			150			200	
I_{IB}	Input bias current			25°C		−25	−250		−25	−250		−25	−250	nA
		V_O = 1.4 V		Full range			−400			−400			−500	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = ≥ 15 kΩ to V_{CC}		25°C	50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1	50		0.1	50		0.1	50	nA
			V_{OH} = 30 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	500	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8	2		0.8	2		0.8	2	mA
		V_{CC} = 30 V, No load	V_O = 15 V,									1	2.5	

† Full range (MIN to MAX) for LM239 and LM239A is −25°C to 85°C, for LM339 and LM339A is 0°C to 70°C, and for LM2901 is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ All typical values measured at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3		μs
	C_L = 15 pF§, See Note 4	TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V	$V_{IC} = V_{ICR}$min,		2	5	mV
I_{IO}	Input offset current	V_O = 1.4 V			5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V			−25	−250	nA
V_{ICR}	Common-mode input voltage range			0 to V_{CC}−1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq 15\ k\Omega$ to V_{CC}	V_O = 1.4 V to 11.4 V,	25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1	50	nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load		0.8	2	mA
		V_O = 30 V, No load	V_O = 15 V,		1	2.5	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

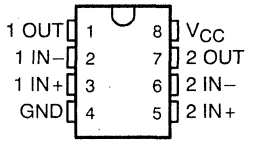
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3		ns
	C_L = 15 pF‡, See Note 4	TTL1-level input step		0.3		

‡ C_L includes probe and jig capacitance.

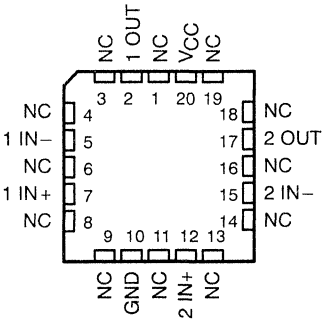
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM193)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

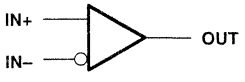
description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM2903Q is manufactured to demanding automotive requirements.

The LM193 is characterized for operation from −55°C to 125°C. The LM293 and LM293A are characterized for operation from −25°C to 85°C. The LM393 and LM393A are characterized for operation from 0°C to 70°C. The LM2903 and LM2903Q are characterized for operation from −40°C to 125°C.

symbol (each comparator)



AVAILABLE OPTIONS

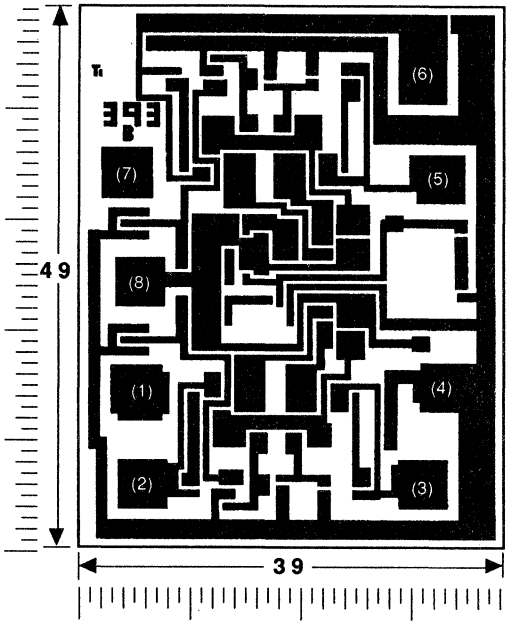
T_A	V_{IO} max at 25°C	PACKAGE						CHIP FORM (Y)§
		SMALL OUTLINE (D)†	SSOP (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)‡	
0°C to 70°C	5 mV	LM393D	LM393DB			LM393P	LM393PW	LM393Y
	2 mV	LM393AD				LM393AP		
−25°C to 85°C	5 mV	LM293D				LM293P		
	2 mV	LM293AD				LM293AP		
−40°C to 125°C	7 mV	LM2903D	LM2903DB			LM2903P	LM2903PW	
	7 mV	LM2903QD				LM2903QP		
−55°C to 125°C	5 mV	LM193D		LM193FK	LM193JG	LM193P		

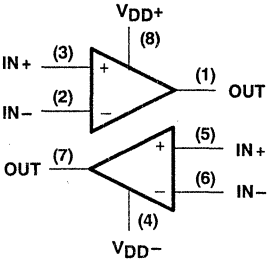
† The D package is available taped and reeled. Add the suffix R (e.g., LM393DR).
‡ The DB and PW packages are only available left-end taped and reeled. Add suffix LE (e.g., LM393DBLE).
§ Chips are tested at 25°C. See LM393Y for electrical characteristics.

LM393Y chip information

These chips, properly assembled, display characteristics similar to the LM393 (see electrical table on LM393Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.6 × 3.6 MINIMUM

$T_J$max = 150°C

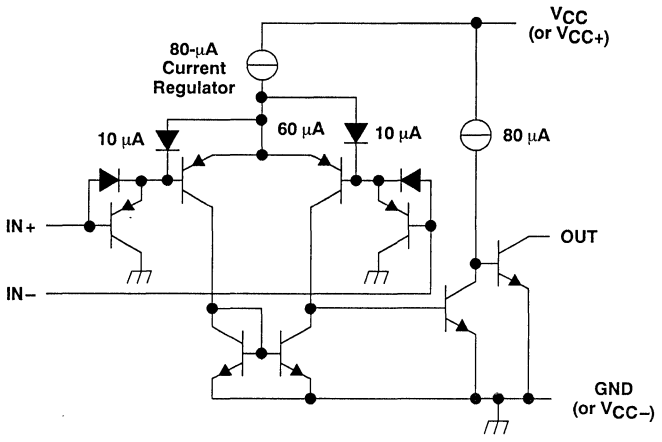
TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALLIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

schematic (each comparator)



Component Count:
Epi-SET 1
Diodes 2
Resistors 2
Transistors 30

Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 36 V
Differential input voltage (see Note 2) ..... ±36 V
Input voltage range (either input) ..... −0.3 V to 36 V
Output voltage ..... 36 V
Output current ..... 20 mA
Duration of output short-circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: LM193 ..... −55°C to 125°C
LM293, LM293A ..... −25°C to 85°C
LM393, LM393A ..... 0°C to 70°C
LM2903, LM2903Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	25°C	336 mW	273 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
JG	900 mW	8.4 mW/°C	43°C	672 mW	546 mW	210 mW
P	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	25°C	336 mW	273 mW	N/A

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM193			LM293, LM393			LM293A, LM393A			LM2903, LM2903Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{IC}$ min, V_O = 1.4 V		25°C		2	5		2	5		1	2		2	7	mV
				Full range			9			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50		5	50		5	50	nA
				Full range			100			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−100		−25	−250		−25	−250		−25	−250	nA
				Full range			−300			−400			−400			−500	
V_{ICR}	Common-mode input voltage range‡			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}		25°C	50	200		50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1			0.1	50		0.1	50		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	Full range			1			1			1			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V	25°C		150	400		150	400		150	400		150	400	mV
				Full range			700			700			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = 1 V	25°C	6			6			6			6			mA
I_{CC}	Supply current	$R_L = \infty$	V_{CC} = 5 V	25°C		0.8	1		0.8	1		0.8	1		0.8	1	mA
			V_{CC} = 30 V	Full range			2.5			2.5			2.5			2.5	

† Full range (MIN or MAX) for LM193 is −55°C to 125°C, for LM293 and LM293A is 25°C to 85°C, for the LM393 and LM393A is 0°C to 70°C, and for LM2903 and LM2903Q is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} −1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3		µs
	C_L = 15 pF§, See Note 4	TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

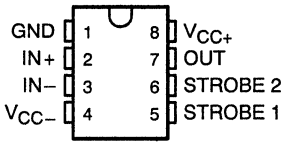
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V	$V_{IC} = V_{ICR}$min,		2	5	mV
I_{IO}	Input offset current				5	50	nA
I_{IB}	Input bias current				−25	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V		0 to V_{CC}−1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq 15\ k\Omega$ to V_{CC}	V_O = 1.4 V to 11.4 V,	25	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V		0.1	50	nA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V		150	400	mV
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = −1 V	6			mA
I_{CC}	Supply current	$R_L = \infty$,	V_{CC} = 5 V		0.8	1	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

D1108, OCTOBER 1979–REVISED OCTOBER 1991

- **Fast Response Times**
- **Improved Gain and Accuracy**
- **Fanout to 10 Series 54/74 TTL Loads**
- **Strobe Capability**
- **Short-Circuit and Surge Protection**
- **Designed to Be Interchangeable With National Semiconductor LM306**

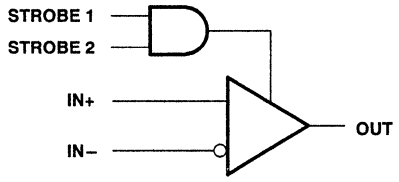
D OR P PACKAGE
(TOP VIEW)



description

The LM306 is a high-speed voltage comparator with differential inputs, a low-impedance high-sink-current (100 mA) output, and two strobe inputs. This device detects low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

functional block diagram



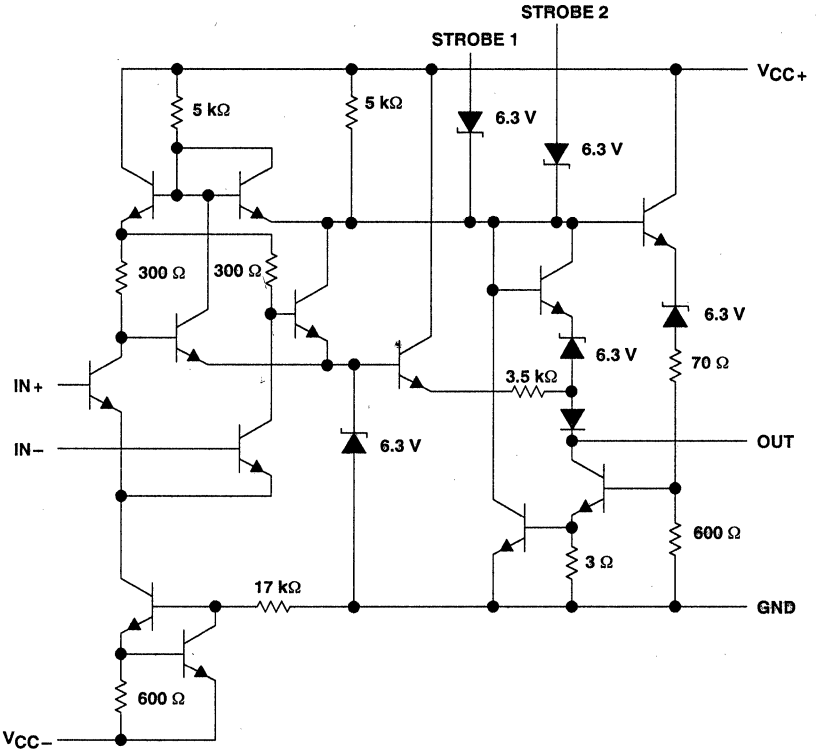
A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between –3 V and –12 V with little difference in performance.

The LM306 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	5 MV	LM306D	LM306P

schematic



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... −15 V
Differential input voltage (see Note 2) ..... ±5 V
Input voltage (either input, see Notes 1 and 3) ..... ±7 V
Strobe voltage range (see Note 1) ..... 0 V to V_{CC+}
Output voltage (see Note 1) ..... 24 V
Voltage from output to V_{CC-} ..... 30 V
Duration of output short-circuit to ground (see Note 4) ..... 10 s
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	600 mW	5.8 mW/°C	46°C	464 mW
P	600 mW	8.0 mW/°C	75°C	600 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −3 V to −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S ≤ 200 Ω,	See Note 5	25°C		1.6§	5	mV
				Full range			6.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω,	See Note 5	Full range		5	20	μV/°C
I_{IO}	Input offset current		See Note 5	25°C		1.8	5	μA
				MIN		1	7.5	
				MAX		0.5	5	
α_{IIO}	Average temperature coefficient of input offset current		See Note 5	MIN to 25°C		24	100	nA/°C
				25°C to MAX		15	50	
I_{IB}	Input bias current	V_O = 0.5 V to 5 V		MIN to 25°C			40	μA
				25°C to MAX		16	25	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = 0.4 V		Full range		−1.7	−3.2	mA
$V_{IH(S)}$	High-level strobe voltage			Full range	2.2			V
$V_{IL(S)}$	Low-level strobe voltage			Full range			0.9	V
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V to −12 V		Full range	±5			V
V_{ID}	Differential input voltage range			Full range	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0.5 V to 5 V		25°C		40		V/mV
V_{OH}	High-level output voltage	I_{OH} = −400 μA	V_{ID} = 8 mV	Full range	2.5		5.5	V
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	V_{ID} = −7 mV	25°C		0.8	2	V
		I_{OL} = 50 mA	V_{ID} = −7 mV	Full range			1	
		I_{OL} = 16 mA	V_{ID} = −8 mV	Full range			0.4	
I_{OH}	High-level output current	V_{OH} = 8 V to 24 V	V_D = 7 mV	MIN to 25°C		0.02	2	μA
			V_{ID} = 8 mV	25°C to MAX			100	
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV,	No load	Full range		6.6	10	mA
I_{CC-}	Supply current from V_{CC-}	No load		Full range		−1.9	−3.6	mA

† Unless otherwise noted, all characteristics are measured with both strobes open.
‡ Full range is 0°C to 70°C.
§ This typical value is at V_{CC+} = 12 V, V_{CC-} = −6 V.
NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_L = 390 Ω to 5 V,	C_L = 15 pF,	See Note 6		28	40	ns

† Unless otherwise noted, all characteristics are measured with both strobes open.
NOTE 6: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

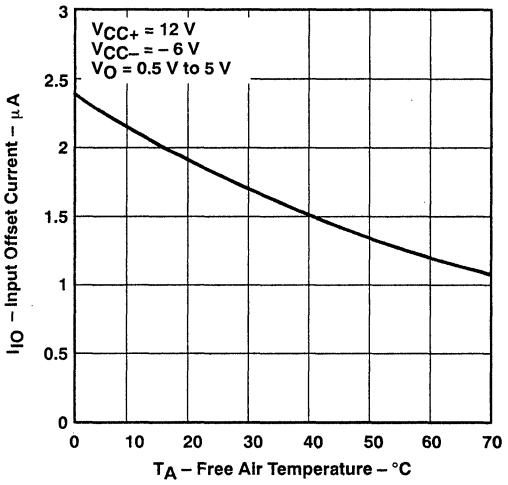


Figure 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

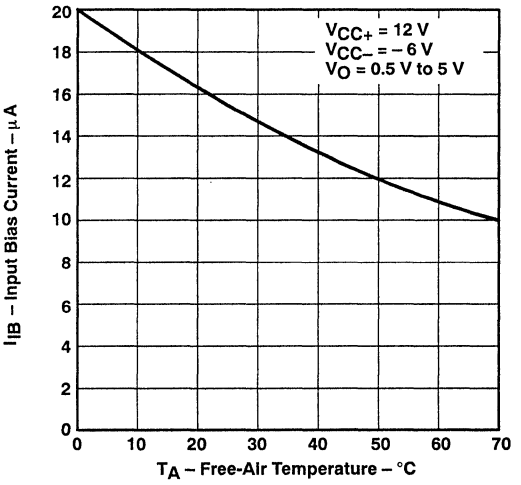


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

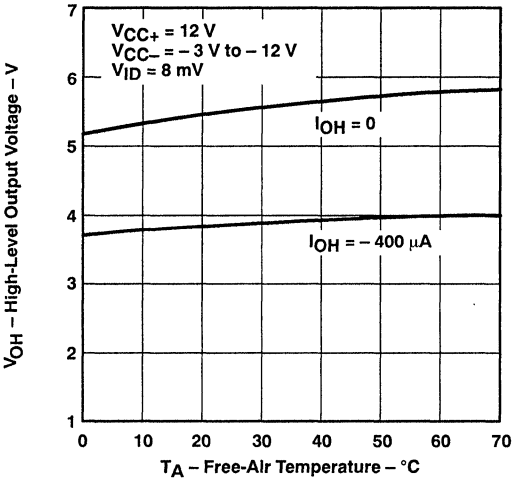


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

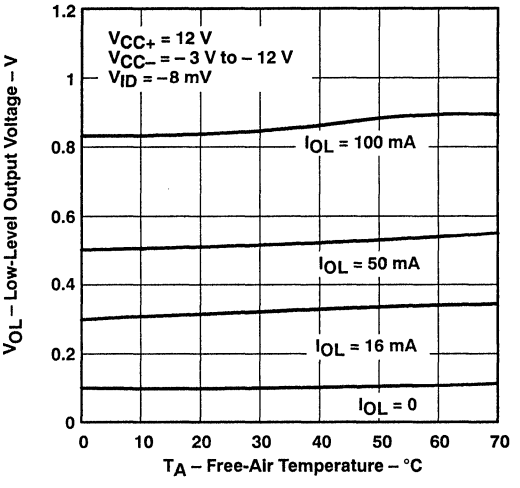


Figure 4

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

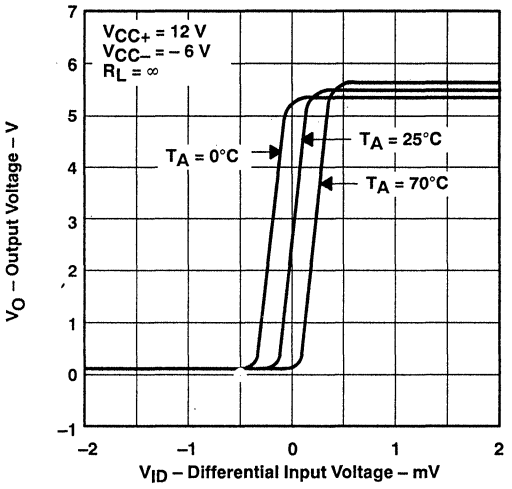


Figure 5

OUTPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

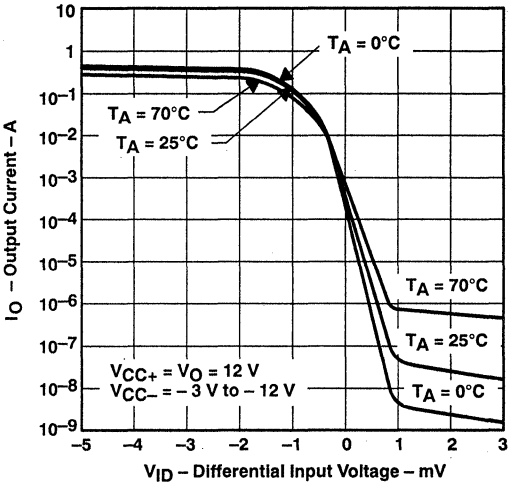


Figure 6

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

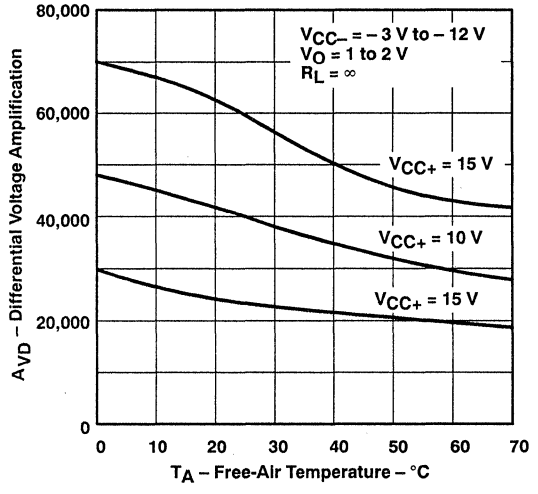


Figure 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

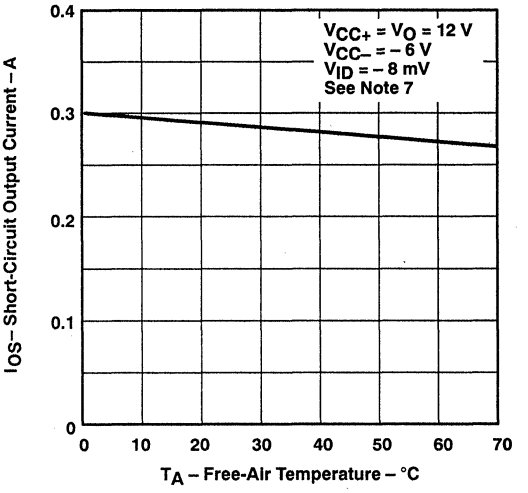


Figure 8

NOTE 7: This parameter was measured using a single 5-ms pulse.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

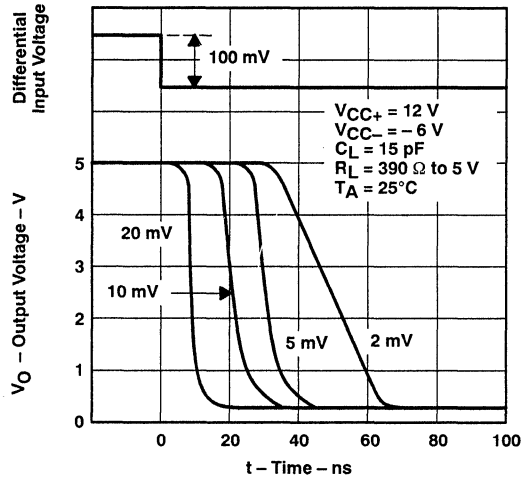


Figure 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

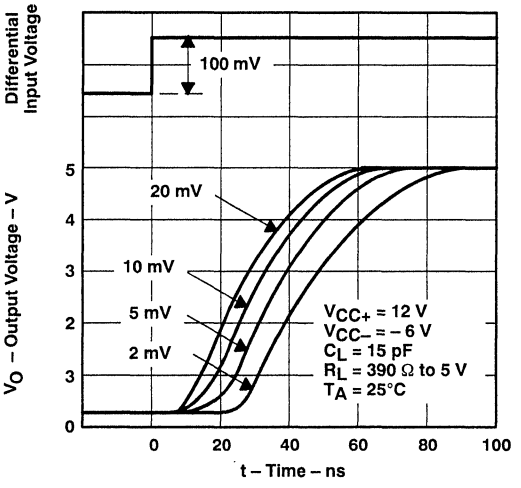


Figure 10

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

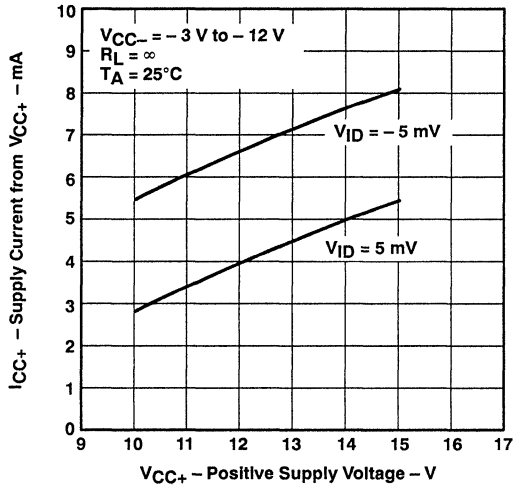


Figure 11

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

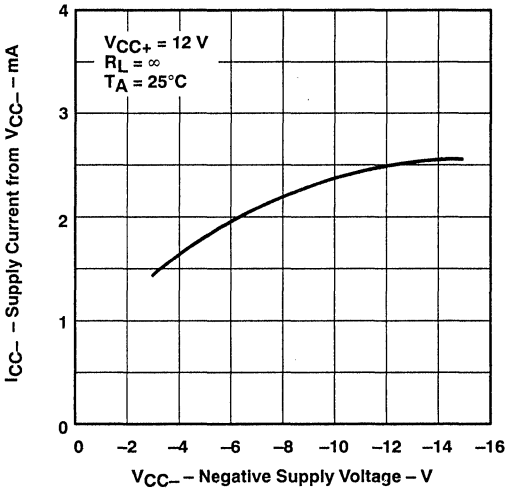


Figure 12

TYPICAL CHARACTERISTICS

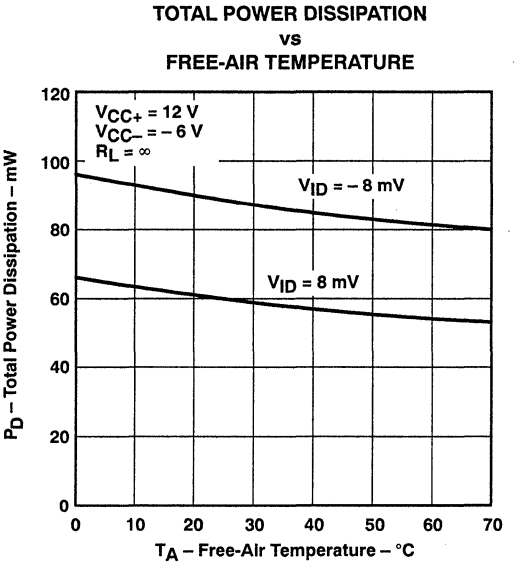


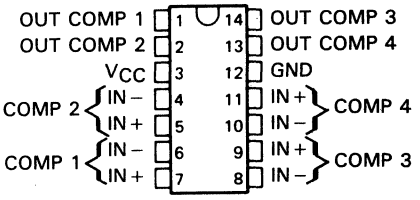
Figure 13

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

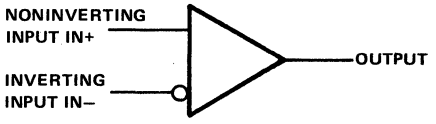
D2402, OCTOBER 1977—REVISED APRIL 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 28 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . .3 nA Typ
- Low Input Offset Voltage . . . 3 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±28 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each comparator)



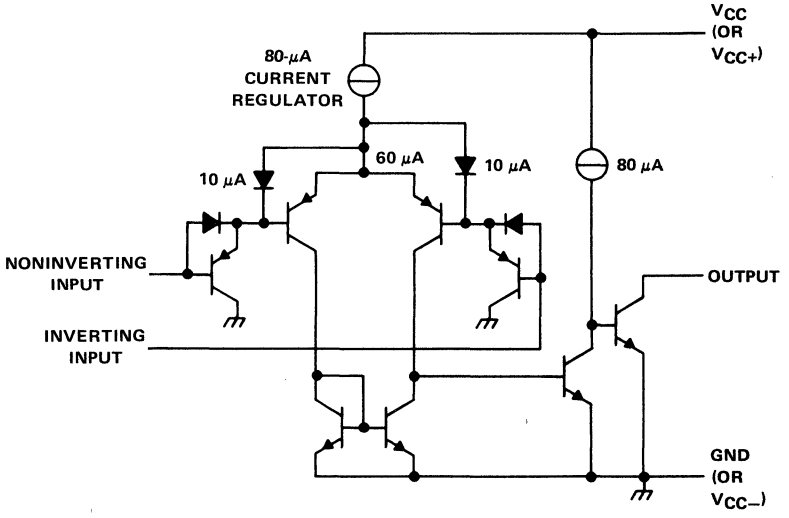
description

This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 28 V and pin 3 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LM3302	D, J, N	−40°C to 85°C	20 mV

The D packages are available taped and reeled. Add the suffix R to the device type, when ordering. (i.e., LM3302DR)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 28 V
Differential input voltage (see Note 2) . . . . . ±28 V
Input voltage range (either input) . . . . . −0.3 V to 28 V
Output voltage . . . . . 28 V
Output current . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 28 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V	25°C		3	20	mV
			−40°C to 85°C			40	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	100	nA
			−40°C to 85°C			300	
I_{IB}	Input bias current		25°C		−25	−500	nA
			−40°C to 85°C			−1000	
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{CC}−1.5			V
			−40°C to 85°C	0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = 15 kΩ to V_{CC}	25°C	2	30		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 5 V	25°C		0.1		nA
			−40°C to 85°C			1	µA
V_{OL}	Low-level output voltage	V_{ID} = 1 V, I_{OL} = 4 mA	25°C		150	500	mV
			40°C to 85°C			700	
I_{OL}	Low-level output current	V_{ID} = 1 V, V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load	25°C		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ to 5 V,	100-mV input step with 5-mV overdrive		1.3		µs
	C_L = 15 pF‡, See Note 4	TTL-level input step		0.3		

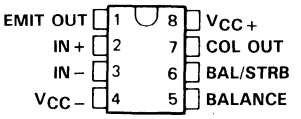
‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

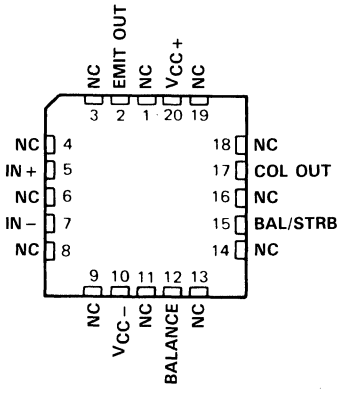
D3019, JUNE 1987—REVISED MAY 1988

- Low Power Drain — 900 μW Typical with 5-V Supply
- Operates from ±15 V or from a Single Supply as Low as 3 V
- Output Drive Capability of 25 mA
- Emitter Output Can Swing Below Negative Supply
- Response Time — 1.2 μs Typ
- Low Input Currents:
  Offset Current . . . 2 nA Typ
  Bias Current . . . 15 nA Typ
- Wide Common-Mode Input Range:
  −14.5 V to 13.5 V with ±15-V Supply
- Same Pinout as LM111, LM211, LM311
- Designed to be Interchangeable with National Semiconductor LP311

LP111 . . . JG DUAL-IN-LINE PACKAGE
LP211, LP311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LP111 . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)

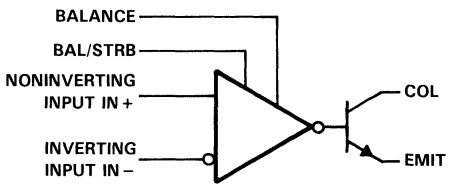


NC—No internal connection

description

The LP111, LP211, and LP311 are a low-power versions of the industry-standard LM111, LM211, and LM311. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption but only a 6:1 slowdown in response time. Thus, they are well-suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ±18 V down to a single 3-V supply with less than 300 μA current drain, but are still capable

functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	7.5 mV	LP311D	—	LP311JG	LP311P
−25°C to 85°C	7.5 mV	LP211D	—	LP211JG	LP211P
−55°C to 125°C	7.5 mV	—	LP111FK	LP111JG	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., LP311DR)

description (continued)

of driving a 25-mA load. The LP111, LP211, and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins.

The LP111 is characterized for operation over the full military temperature range of −55°C to 125°C. The LP211 is characterized for operation from −25°C to 85°C, and the LP311 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −18 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage (either input, see Notes 1 and 3) . . . . . ±15 V
Voltage from emitter output to V_{CC-} . . . . . 30 V
Voltage from collector output to V_{CC-} . . . . . 40 V
Voltage from collector output to emitter output . . . . . 40 V
Duration of output short-circuit (see Note 4) . . . . . 40 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: LP111 . . . . . −55°C to 125°C
LP211 . . . . . −25°C to 85°C
LP311 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	25°C	880 mW	715 mW	275 mW
JG (LP111)	1050 mW	8.4 mW/°C	25°C	672 mW	546 mW	210 mW
JG (LP_11)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	—
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNITS
Input voltage ($\|V_{CC\pm}\| \leq 15$ V)	V_{CC-} +0.5		V_{CC+} −1.5	V
Supply voltage, $V_{CC+} - V_{CC-}$	3.5		30	V

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{ID}	Input offset voltage	RS < 100 kΩ, See Note 5	25°C			2	7.5	mV
			Full Range				10	
I_{IO}	Input offset current	See Note 5	25°C			2	25	nA
			Full Range				35	
I_{IB}	Input bias current		25°C			15	100	nA
			Full Range				150	
V_{OL}	Low-level output voltage	V_{ID} > 10 mV, I_{OL} = 25 mA, See Note 6	25°C			0.4	1.5	V
		V_{CC} = 4.5 V, V_{CC-} = 0, V_{ID} < −10 mV, I_{OL} = 1.6 mA, See Note 6	Full Range	LP111		0.1	0.7	
				LP211 LP311		0.1	0.4	
	Low-level strobe current	$V_{(strobe)}$ = 0.3 V, V_{ID} < −10 mV, See Note 7	25°C			100	300	μA
$I_{O(off)}$	Output off-state current	V_{ID} > 10 mV, V_{CE} = 35 V	25°C			0.2	100	nA
A_{VD}	Large signal differential voltage amplification	R_L = 5 kΩ	25°C		40	100		V/mV
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −50 mV, R_L = ∞	Full Range			150	300	μA
I_{CC-}	Supply current from V_{CC-}	V_{ID} = 50 mV, R_L = ∞	Full Range			−80	−180	μA

†All typical values are at $V_{CC\pm}$ = ±15 V, T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. Voltages are with respect to EMIT OUT and V_{CC-} tied together.

7. The strobe should not be shorted to ground; it should be current driven at 100 μA to 300 μA.

switching characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

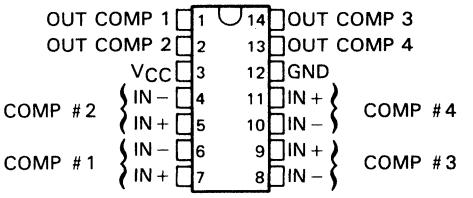
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	See Note 8		1.2		μs

NOTE 8: The response time is specified for a 100-mV input step with 5-mV overdrive.

D3044, OCTOBER 1987—REVISED MAY 1988

- Ultralow Power Supply Current Drain . . . Typically 60 μA
- Low Input Biasing Current . . . 3 nA
- Low Input Offset Current . . . ±0.5 nA
- Low Input Offset Voltage . . . ±2 mV
- Common-Mode Input Voltage Includes Ground
- Output Voltage Compatible with MOS and CMOS Logic
- High Output Sink-Current Capability (30 mA at V_O = 2 V)
- Power Supply Input Reverse-Voltage Protected
- Single-Power-Supply Operation
- Pin-for-Pin Compatible with LM239, LM339, LM2901

D, J, OR N PACKAGE
(TOP VIEW)



description

The LP239, LP339, and LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60-μA drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultralow power supply drain current is independent of the power supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time delay generators, voltage controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, and LP2901 were specifically designed to interface with the CMOS logic family. The ultralow power supply current makes these products desirable in battery-powered applications.

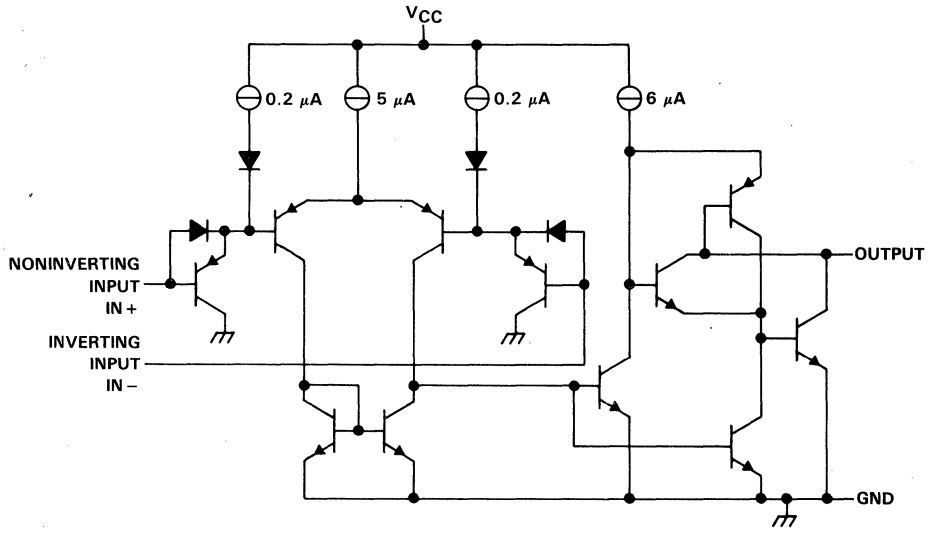
The LP239 is characterized for operation from −25°C to 85°C. The LP339 is characterized for operation from 0°C to 70°C. The LP2901 is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (N)	CERAMIC DIP (J)
0°C to 70°C	±5 mV	LP339D	LP339N	LP339J
−25°C to 85°C	±5 mV	LP239D	LP239N	LP239J
−40°C to 85°C	±5 mV	LP2901D	LP2901N	LP2901J

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., LP339DR).

schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 36 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±36 V
Input voltage range (either input) . . . . . −0.3 V to 36 V
Input current, $V_I \leq -0.3$ V (see Note 3) . . . . . −50 mA
Duration of output short-circuit to ground (see Note 4) . . . . . unlimited
Continuous total dissipation (see Note 5) . . . . . See Dissipation Rating Table
Operating free-air temperature range: LP239 . . . . . −25°C to 85°C
LP339 . . . . . 0°C to 70°C
LP2901 . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive and normal output states are re-established when the input voltage returns to a value more positive than −0.3 V at T_A = 25°C.
4. Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
5. If the output transistors are allowed to saturate, the low bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		LP2901			LP239			LP339			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		5		30	5		30	5		30	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0		3	0		3	0		3	V
	V_{CC} = 30 V	0		28	0		28	0		28	V
Input voltage, V_I	V_{CC} = 5 V	0		3	0		3	0		3	V
	V_{CC} = 30 V	0		28	0		28	0		28	V
Operating free-air temperature, T_A		−40		85	−25		85	0		70	°C

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, RS = 0,	V_O = 2 V, See Note 6	25°C		±2	±5	mV
				Full range			±9	
I_{IO}	Input offset current			25°C		±0.5	±5	nA
				Full range		±1	±15	
I_{IB}	Input bias current	See Note 7		25°C		−2.5	−25	nA
				Full range		−4	−40	
V_{ICR}	Common-mode input voltage range	Single supply		25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V,	R_L = 15 kΩ			500		V/mV
	Output sink current	V_{I-} = 1 V, V_{I+} = 0	V_O = 2 V (see Note 8)	25°C	20	30		mA
				Full range	15			
			V_O = 0.4 V	25°C	0.2	0.7		
	Output leakage current	V_{I+} = 1 V, V_{I-} = 0	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	Full range			1	μA
V_{ID}	Differential input voltage	V_I ≤ 0 (or V_{CC-} on split supplies)					36	V
I_{CC}	Supply current	R_L = ∞ all comparators				60	100	μA

NOTES: 6. V_{IO} is measured over the full common-mode input voltage range.
7. Because of the p-n-p input stage, the direction of the current is out of the device. This current is essentially constant (i.e., independent of the output state). Therefore, no loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.
8. The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V, and smaller currents at output voltages less than 1.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Large-signal response time	TTL logic swing, V_{ref} = 1.4 V		1.3		μs
Response time			8		μs

TYPICAL APPLICATION DATA

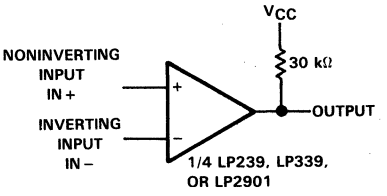


FIGURE 1. BASIC COMPARATOR

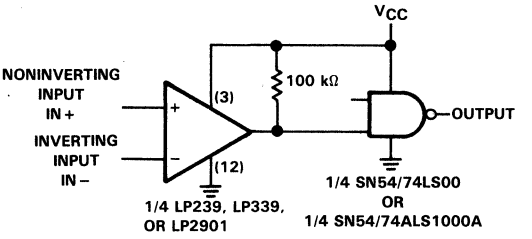


FIGURE 2. CMOS DRIVER

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V. It is usually necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than −0.3 V. The output section has two distinct modes of operation: a Darlington mode and a grounded-emitter mode. This unique drive circuit permits the device to sink 30 mA at V_O = 2 V in the Darlington mode and 700 μA at V_O = 0.4 V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I1 and by the 60-Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc., in this mode while maintaining an ultralow power supply current of 60 μA typically.

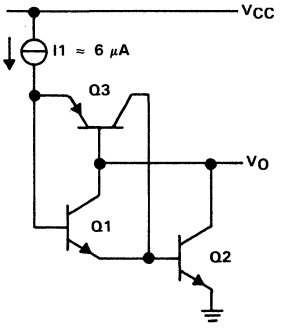


FIGURE 3. OUTPUT SECTION SCHEMATIC DIAGRAM

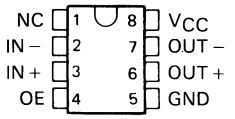
Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the h_{FE} of Q2 (700 μA at V_O = 0.4 V). The output of the devices exhibit a bimodal characteristic with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Therefore several outputs can be tied together to provide a dot logic function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range, and there is no restriction on this voltage based on the magnitude of the voltage that is applied to the V_{CC} terminal of the package.

D2741, JUNE 1983—REVISED JULY 1989

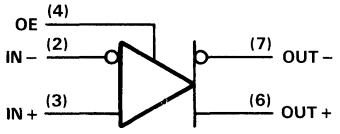
- **Operates from a 5-V Supply**
- **0 to 5 V Common-Mode Input Voltage Range**
- **Self-Biased Inputs**
- **Complementary 3-State Outputs**
- **Enable Capability**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 25 ns Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (positive logic)

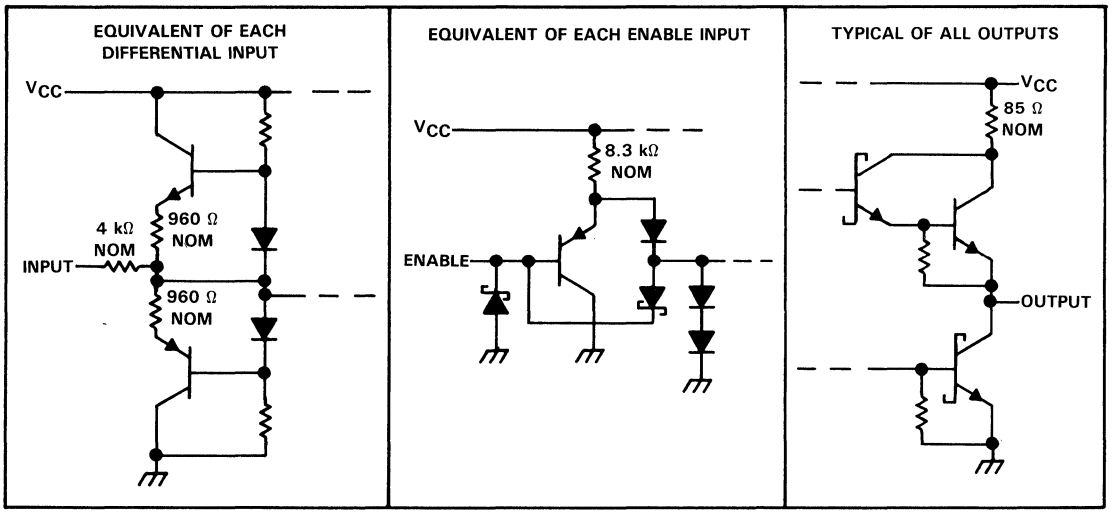


description

The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable, OE, is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

The TL712 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}	0		5	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	V_{ICR} = 0 to 5 V	−100†		100	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV, I_{OH} = −1 mA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 16 mA		0.4	0.5	V
I_{OZ}	Off-state output current	V_O = 2.4 V			−20	μA
I_I	Enable current	V_I = 5.5 V			100	μA
I_{IH}	High-level enable current	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level enable current	V_{IL} = 0.4 V			−360	μA
r_i	Differential input resistance		4			kΩ
r_o	Output resistance				100	Ω
I_{OS}	Short-circuit output current		−15		−85	mA
I_{CC}	Supply current	V_{ID} = 0, No load		17	20	mA

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TTL load (see Figure 1),		25		ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Note 3		25		ns

NOTE 3: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.

PARAMETER MEASUREMENT INFORMATION

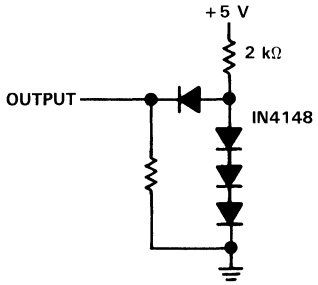


FIGURE 1. TTL OUTPUT LOAD CIRCUIT

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

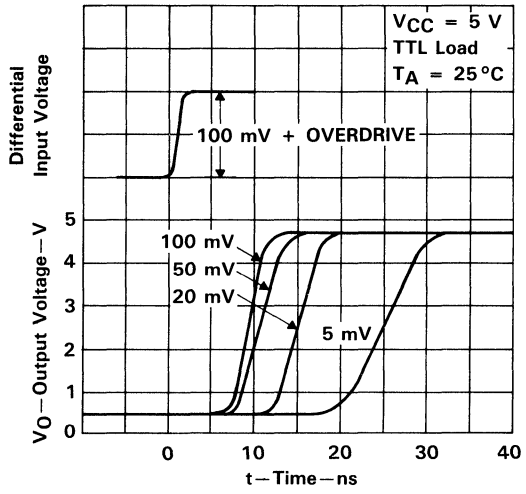


FIGURE 2

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

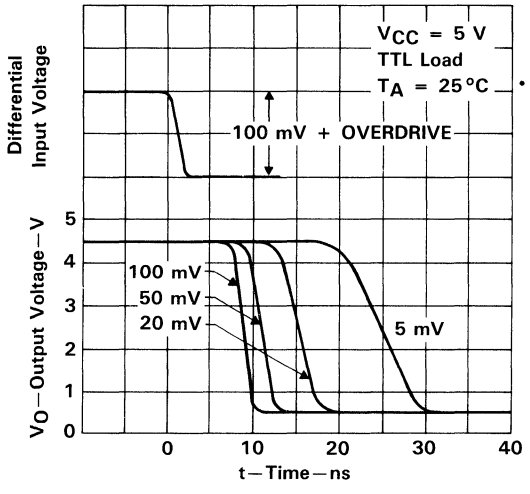


FIGURE 3

TYPICAL CHARACTERISTICS

COMMON-MODE
PULSE RESPONSE

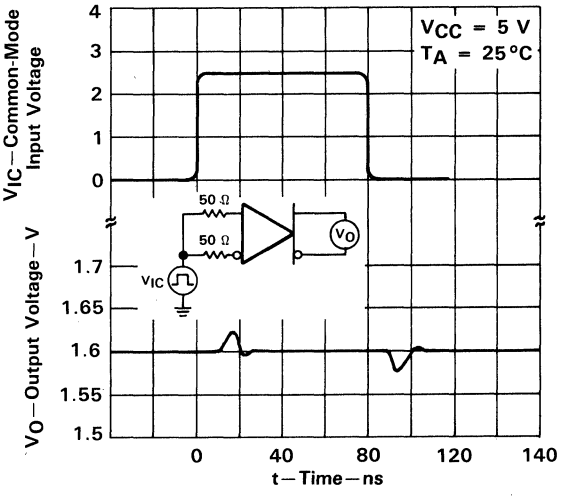
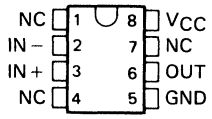


FIGURE 4

D3131, DECEMBER 1988—REVISED JUNE 1989

- **Operates from a 5-V Supply**
- **Self-Biasing Inputs**
- **Hysteresis . . . 10 mV Typical**
- **Response Time . . . 6 ns Typical**
- **Maximum Operating Frequency . . . 50 MHz Typical**

D OR P PACKAGE
(TOP VIEW)



NC—No internal connection

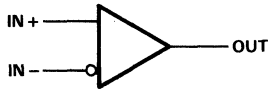
description

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

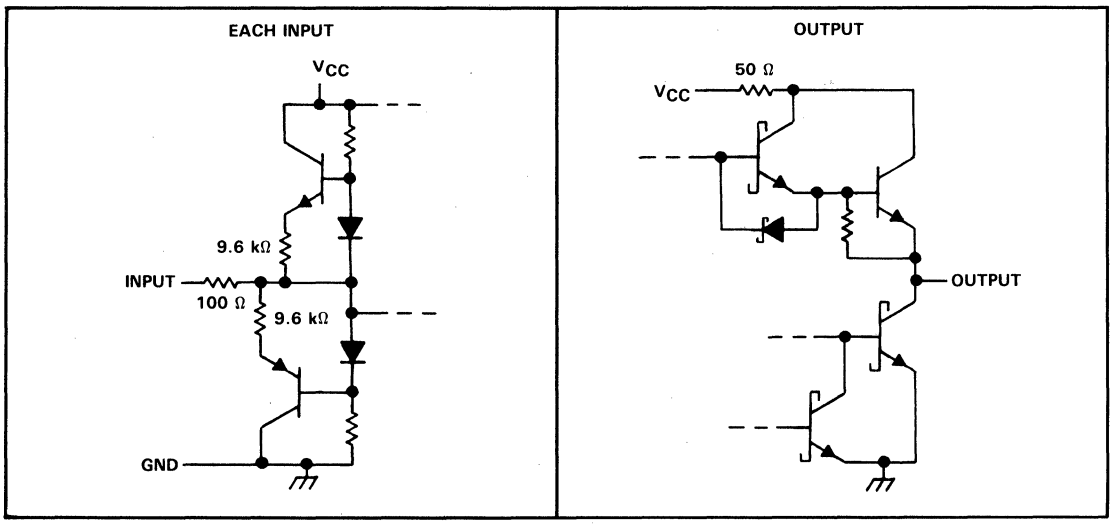
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

The TL714C is characterized for operation from 0°C to 70°C.

symbol



schematic of inputs and output



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Input voltage range . . . . . V_{CC} to GND
Low-level output current, I_{OL} . . . . . 40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except for differential voltage, are with respect to the network ground.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW
P	500 mW	N/A	N/A	500 mW

recommended operating conditions

PARAMETER	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.25	V
Common-mode input voltage, V_{IC}	1.4 to V_{CC} − 1.4		V
High-level output current, I_{OH}		−1	mA
Low-level output current, I_{OL}		16	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over free-air operating temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_T	Threshold voltage	V_{IC} = 1.4 V to 3.6 V			±75	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)		2	10	30	mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV, I_{OH} = −1 mA	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 16 mA		0.4	0.5	V
I_{OS}	Short-circuit output current		−30		−110	mA
r_i	Differential input resistance		2.9			kΩ
I_{CC}	Supply current	V_{ID} = −100 mV, I_O = 0		7	12	mA

†All typical values are at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency	V_{ID} = ±250 mV, $t_r = t_f$ = 4 ns, C_L = 25 pF, Input duty cycle = 50%		50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = ±100 mV, C_L = 25 pF, See Figures 1 and 2		6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			6	12	ns
t_r	Rise time	V_{ID} = ±100 mV, C_L = 25 pF, See Figure 3		4	8	ns
t_f	Fall time			4	8	ns

PARAMETER MEASUREMENT INFORMATION

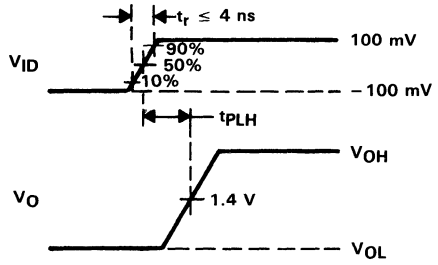


FIGURE 1. PROPAGATION DELAY TIME, LOW TO HIGH (t_{PLH})

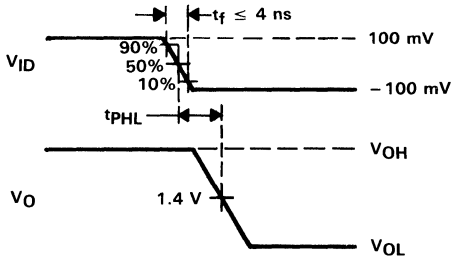


FIGURE 2. PROPAGATION DELAY TIME, HIGH TO LOW (t_{PHL})

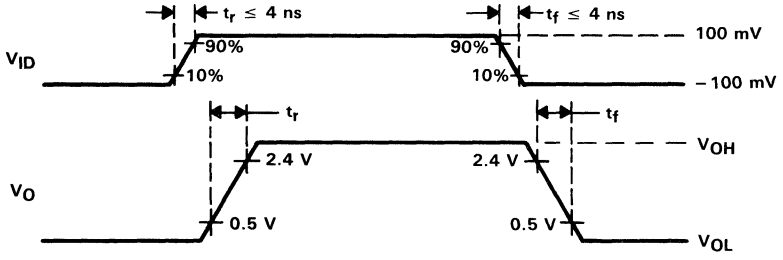
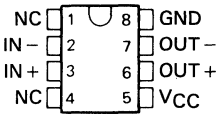


FIGURE 3. RISE AND FALL TIMES (t_r, t_f)

D2781, FEBRUARY 1984—REVISED OCTOBER 1988

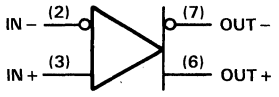
- **Operates from a −5.2-V Power Supply**
- **Self-Biased Inputs**
- **Common-Mode Input Voltage Range 0 V to −5.2 V**
- **MECL III and MECL 10 000 Compatible**
- **Complementary ECL-Compatible Outputs**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 10 ns Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



description

The TL721 is a high-speed voltage comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary ECL-compatible logic outputs with symmetrical switching characteristics. The device operates from a single −5.2-volt supply and is useful as a disk memory read-chain data comparator.

The TL721 is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Low-level output current . . . . . 50 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		−5.2		V
Common-mode input voltage, V_{IC}			±7	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at T_A = 25°C, V_{CC} = −5.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_T+ and V_T-)	V_{IC} = V_{ICR} min		−100†		100	mV
V_{hys}	Hysteresis ($V_T+ - V_T-$)				5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 50 Ω to −2 V	−0.96†		−0.81	V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	R_L = 50 Ω to −2 V	−1.85†		−1.65	V
V_{ICR}	Common-mode input voltage range			0 to −5.2			V
r_{in}	Input resistance			4			kΩ
I_{CC}	Supply current	V_{ID} = 0,	No load		−13	−17	mA

† The algebraic convention, in which the more negative limit is designated as minimum, is used in this data sheet for input threshold and output voltage levels only.

switching characteristics at T_A = 25°C, V_{CC} = −5.2 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_{ID} = +200 mV to −200 mV or −200 mV to +200 mV, R_L = 50 Ω to −2 V		18		ns
t_{PHL}	Propagation delay time, high-to-low-level output			18		ns

TYPICAL CHARACTERISTICS

OUTPUT RESPONSES FOR VARIOUS
INPUT OVERDRIVES

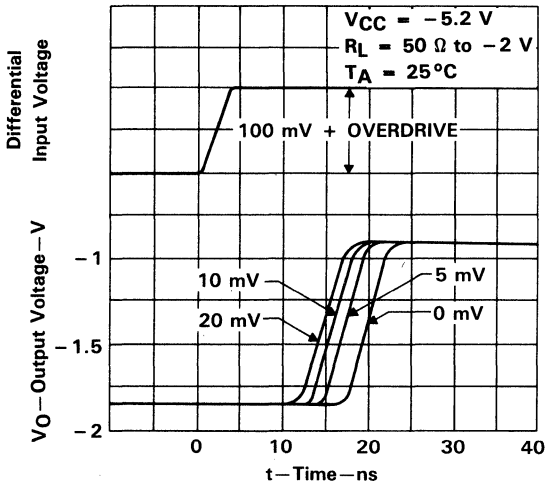


FIGURE 1

OUTPUT RESPONSES FOR VARIOUS
INPUT OVERDRIVES

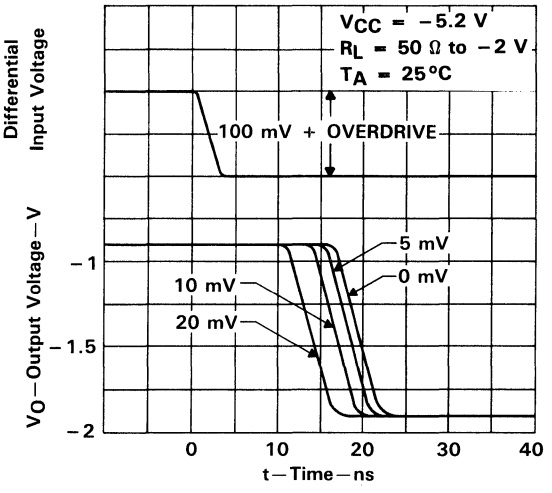


FIGURE 2

COMMON-MODE
PULSE RESPONSE

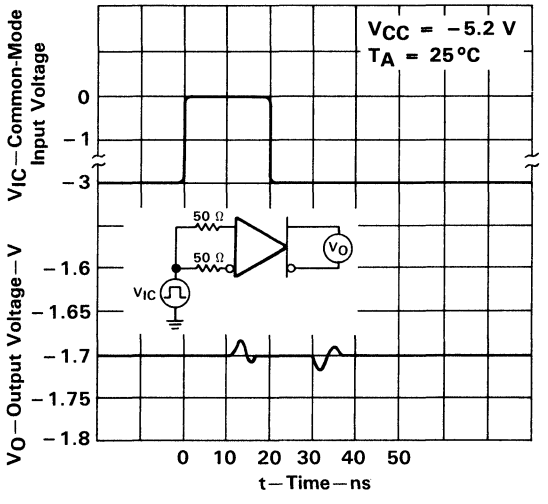
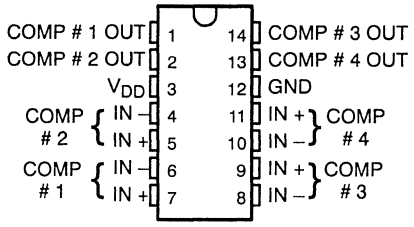


FIGURE 3

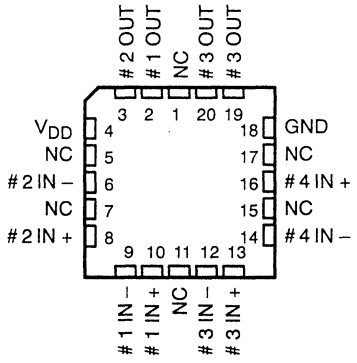
D3135, DECEMBER 1986 – REVISED JANUARY 1991

- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  TLC139M . . . 4 V to 16 V
  TLC339M . . . 4 V to 16 V
  TLC339C . . . 3 V to 16 V
  TLC339I . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



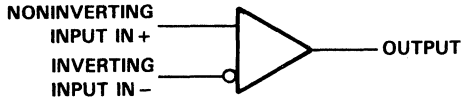
NC – No internal connection

description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC339CD	–	–	TLC339CN
– 40°C to 85°C	5 mV	TLC339ID	–	–	TLC339IN
– 40°C to 125°C	5 mV	TLC339QD	–	–	TLC339QN
– 55°C to 125°C	5 mV	TLC339MD	TLC139MFK	TLC139MJ	TLC339MN

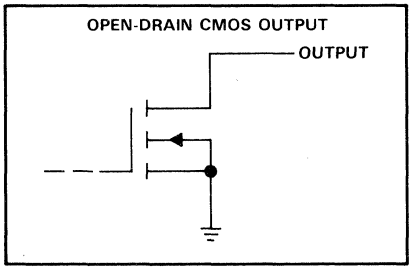
The D package is available taped and reeled. Add the suffix R to the device type, (e.g., TLC339CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of – 40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of – 40°C to 125°C.

output schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 18 V
Differential input voltage (see Note 2) ..... ± 18V
Input voltage range, V_I ..... – 0.3 V to V_{DD}
Output voltage range, V_O ..... – 0.3 V to V_{DD}
Input current, I_I ..... ± 5mA
Output current, I_O (each output) ..... 20 mA
Total supply current into V_{DD} terminal ..... 40 mA
Total current out of ground terminal ..... 60 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC139M ..... – 55°C to 125°C
TLC339C ..... 0°C to 70°C
TLC339I ..... – 40°C to 85°C
TLC339M ..... – 55°C to 125°C
TLC339Q ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	μA
			−55°C to 125°C			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	μA
			0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 85°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			−40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OH} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 VmA	25°C		0.8	40	nA
			85°C			1	μA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	μA
			−40°C to 85°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−40°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			−40°C to 125°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

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switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

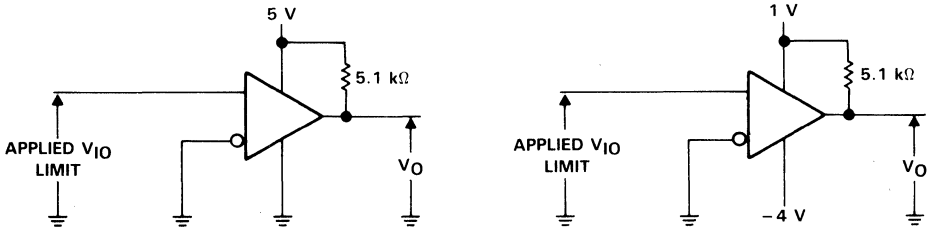
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{PHL}	Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{THL}	Transition time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input ofset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} with V_{IC} = 0 V (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output will change state.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

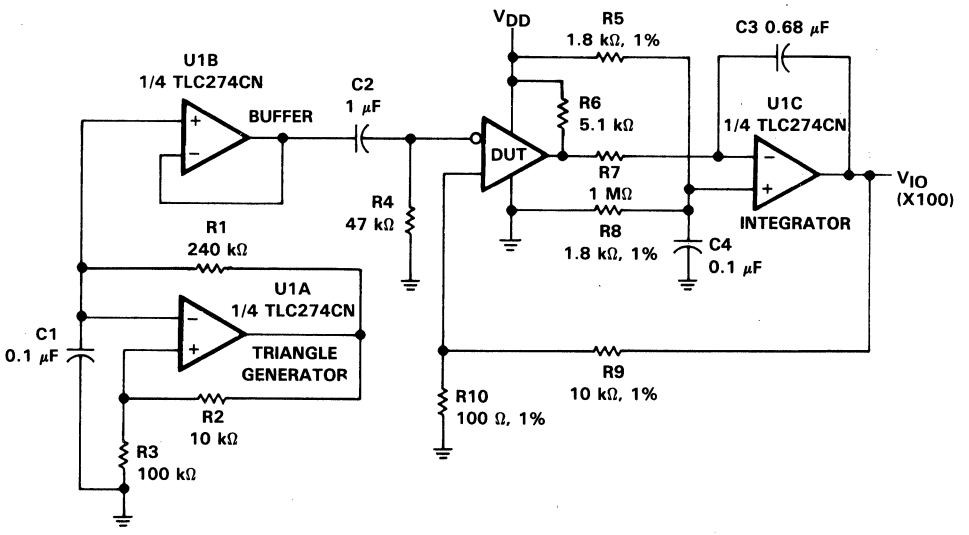
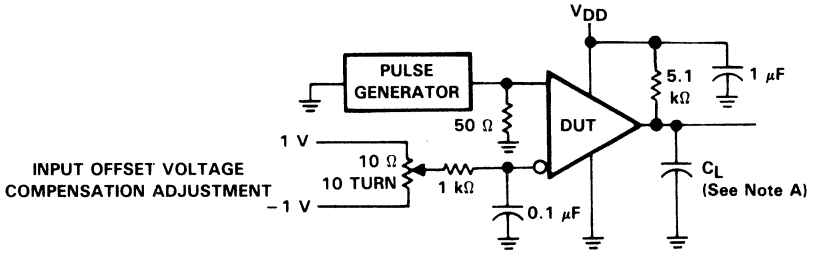


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

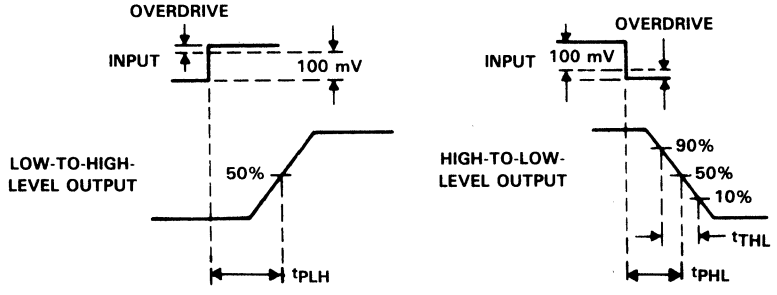
Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. PROPAGATION DELAY, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

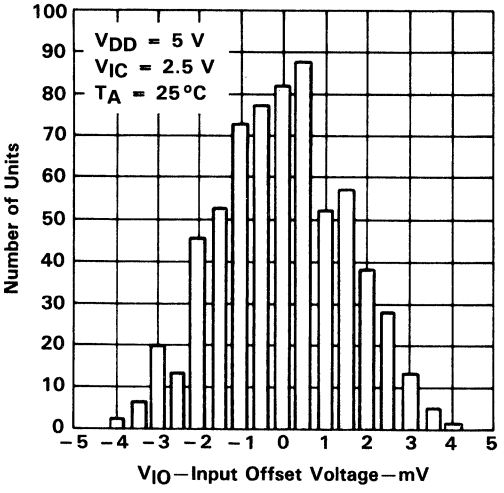


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

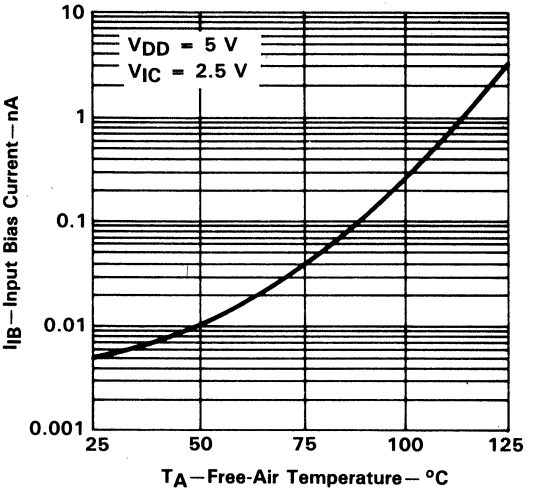


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

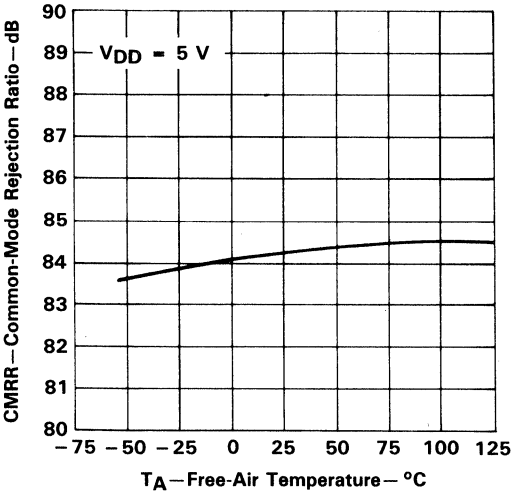


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

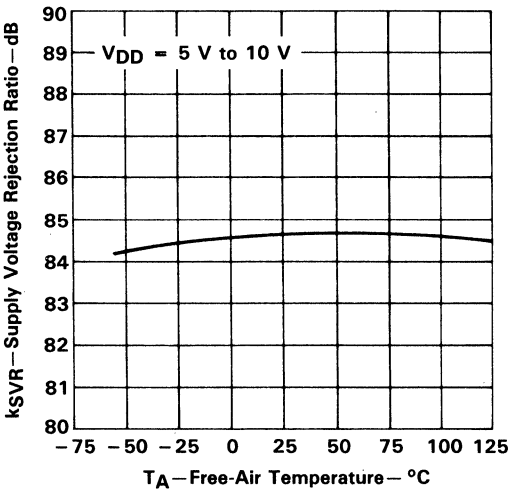


FIGURE 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

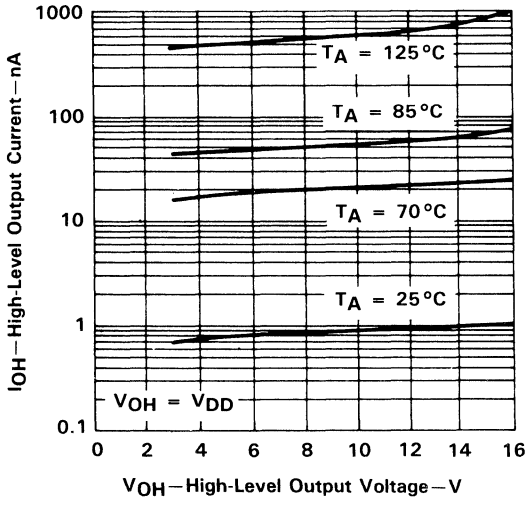


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

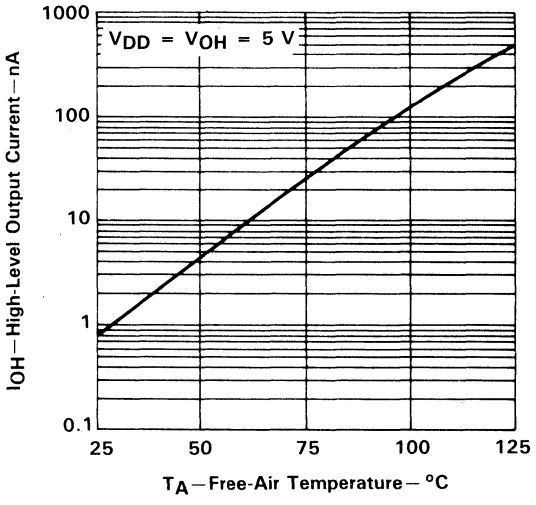


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

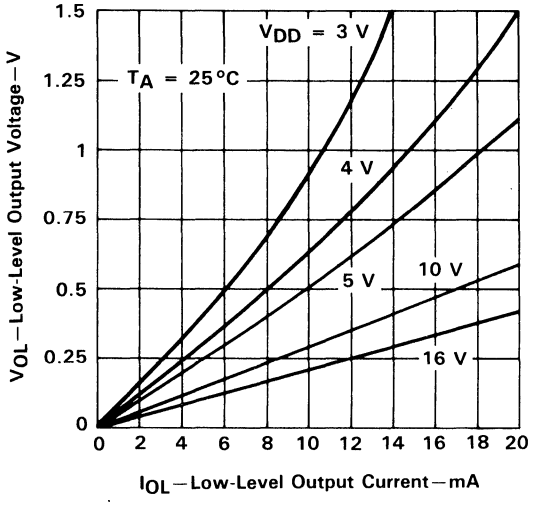


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

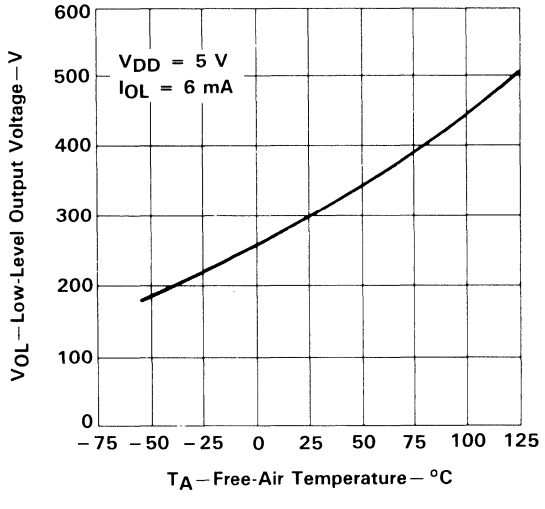


FIGURE 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

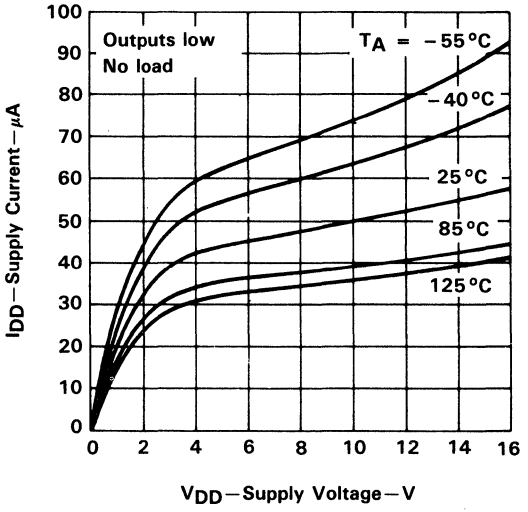


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

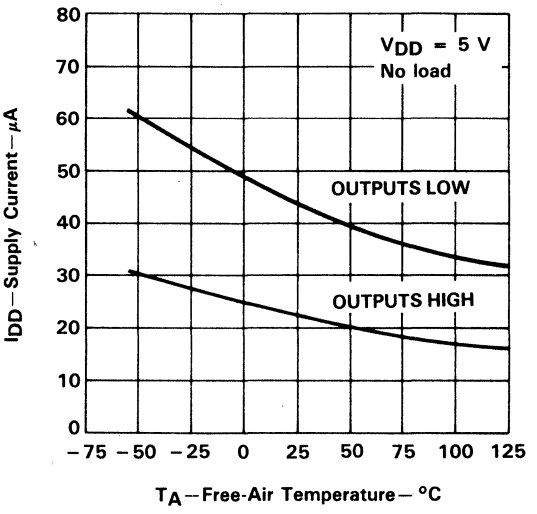


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

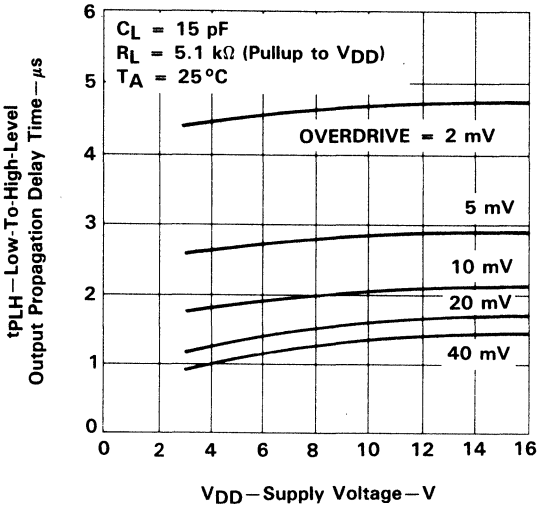


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

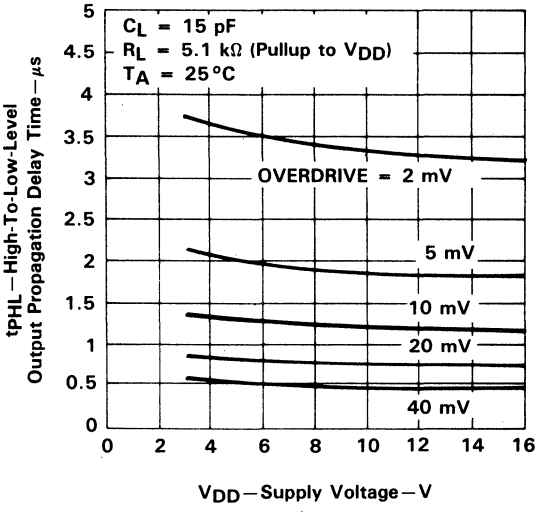


FIGURE 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

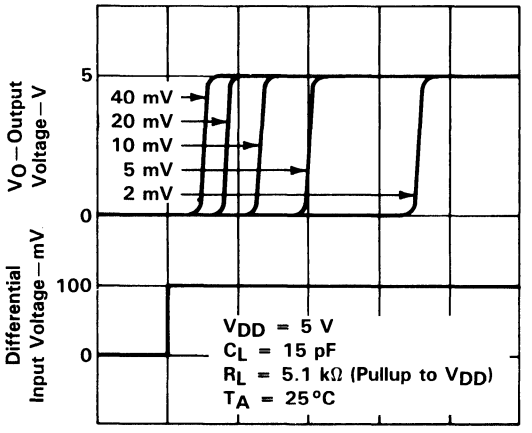


FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

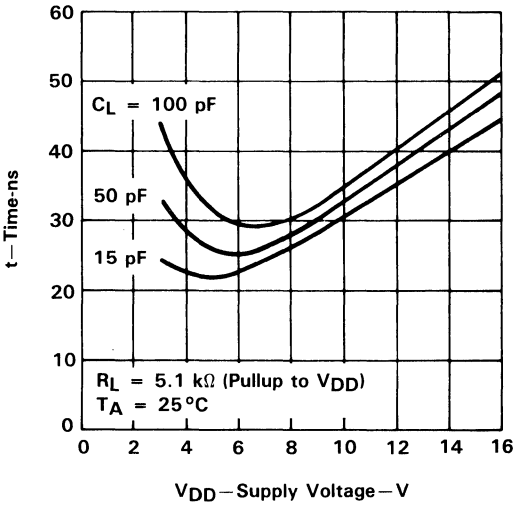


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

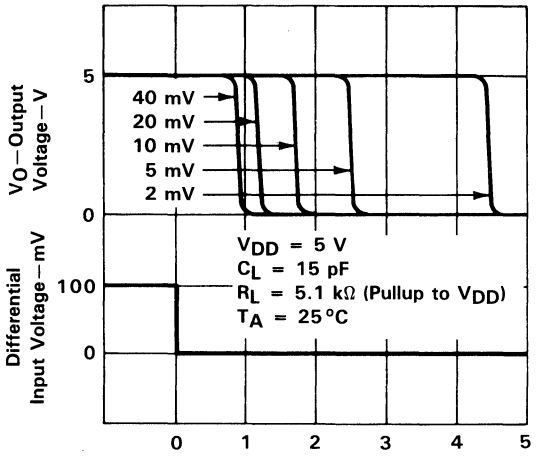


FIGURE 18

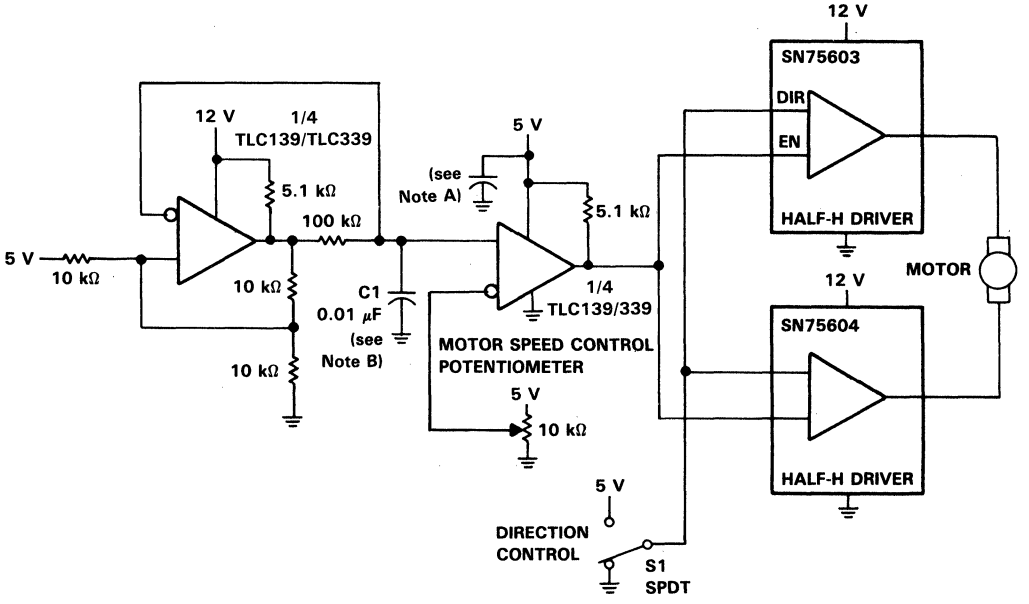
APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between − 0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

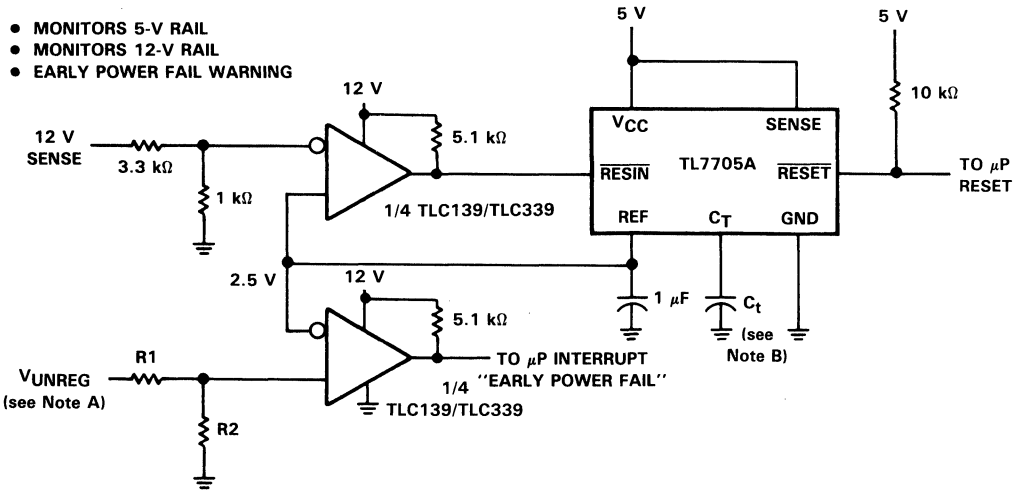
The TLC139 and TLC339 have internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

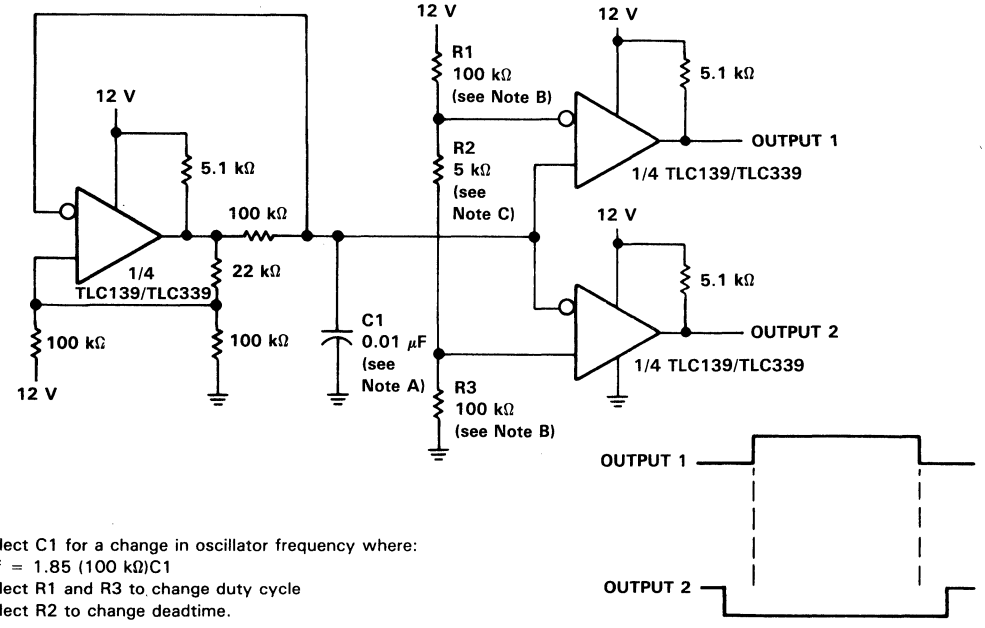
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 20. ENHANCED SUPPLY SUPERVISOR



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$

B. Select R1 and R3 to change duty cycle

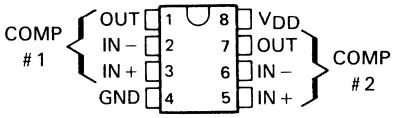
C. Select R2 to change deadtime.

FIGURE 21. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

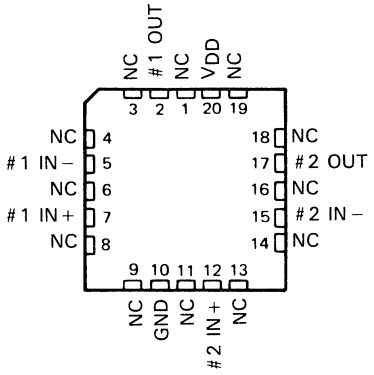
D2901, SEPTEMBER 1985—REVISED OCTOBER 1990

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 1.4 V to 18 V**
- **Very Low Supply Current Drain**
  150 μA Typ at 5 V
  65 μA Typ at 1.4 V
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM393**

TLC352C, TLC352I . . . D OR P PACKAGE
TLC352M . . . JG PACKAGE
(TOP VIEW)

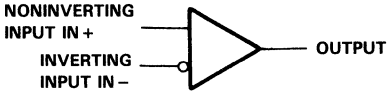


TLC352M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0 °C to 70 °C. The TLC352I is characterized for operation over the industrial temperature range of −40 °C to 85 °C. The TLC352M is characterized for operation over the full military temperature range of −55 °C to 125 °C.

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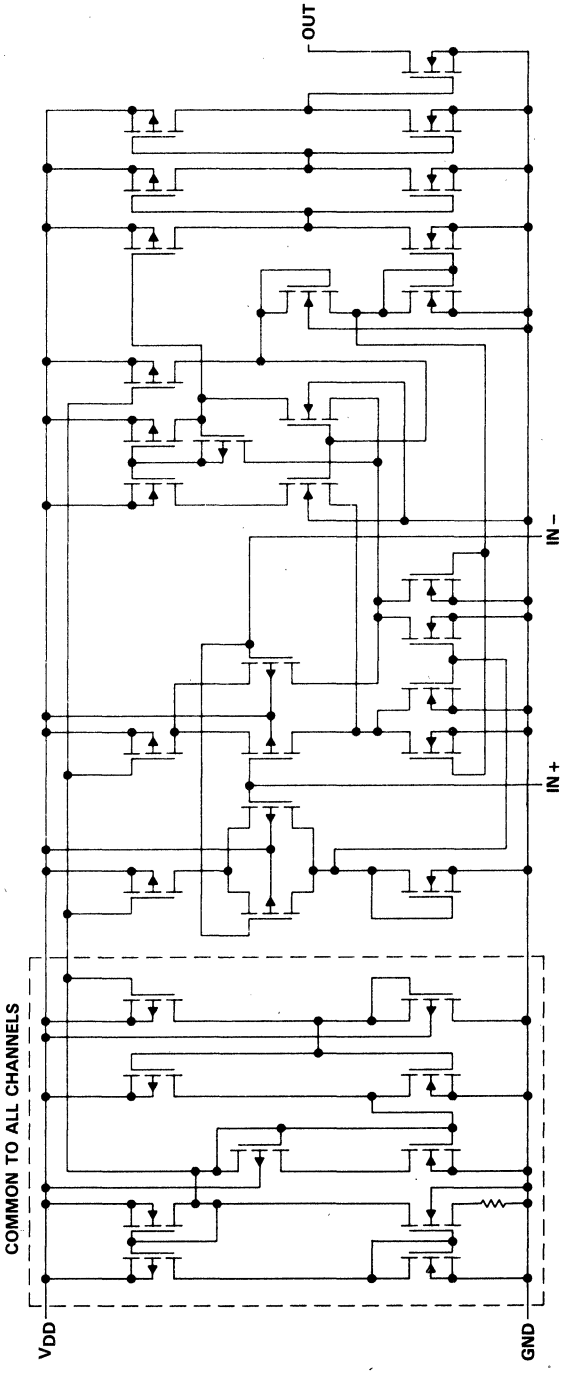
equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	–	–	TLC352CP
−40°C to 85°C	5 mV	TLC352ID	–	–	TLC352IP
−55°C to 125°C	5 mV	–	TLC352MFK	TLC352MJG	–

D packages are availabe taped and reeled. Add "R" suffix to device type, (e.g., TLC352CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC352C . . . . . 0°C to 70°C
TLC352I . . . . . −40°C to 85°C
TLC352M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	1.4		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC352C			TLC352I			TLC352M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			Full range	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V,	I_{OL} = 0.6 mA	25°C		100	200		100	200		100	200	mV
				Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5 V,	V_{OL} = 0.3 V	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 0.5 V,	No load	25°C		65	150		65	150		65	150	μA
				Full range			200			200			200	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, −40°C to 85°C for TLC352I, and −55°C to 125°C for TLC352M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC352C			TLC352I			TLC352M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 5		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		0.15	0.3		0.15	0.3		0.15	0.3	mA
				Full range			0.4			0.4			0.4	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, −40°C to 85°C for TLC352I, and −55°C to 125°C for TLC352M. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

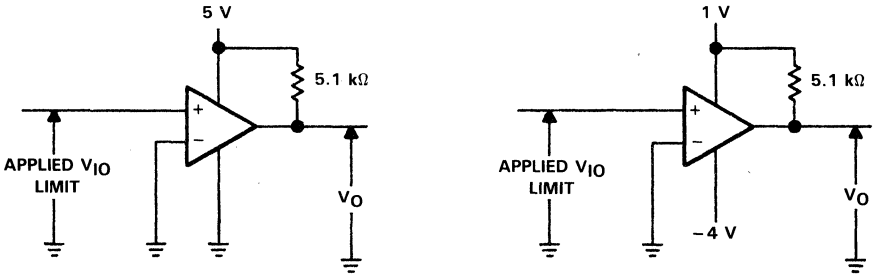
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is ''sliced'' symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

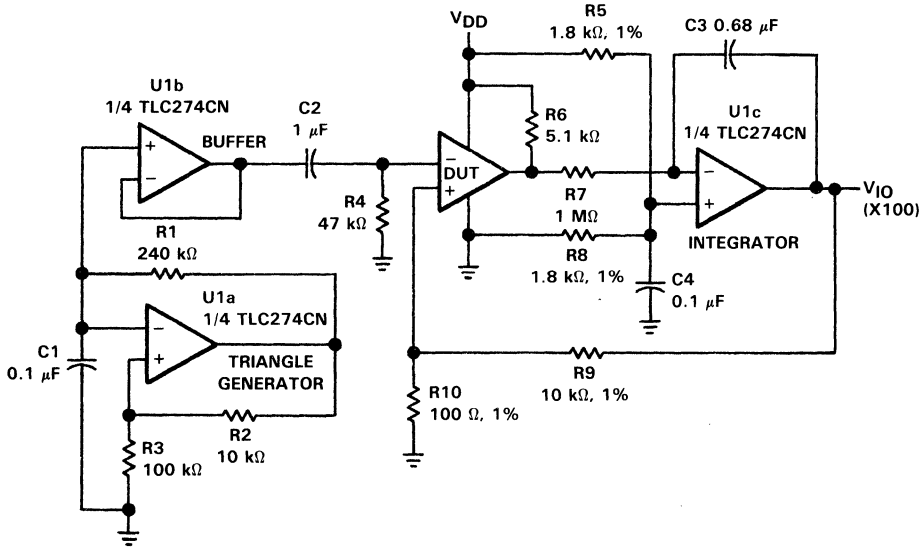
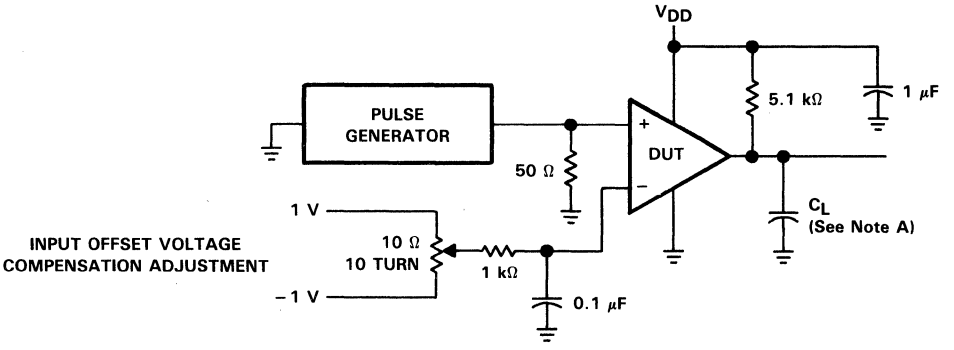


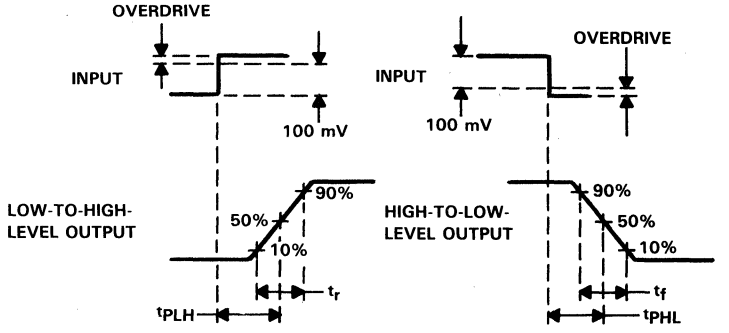
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

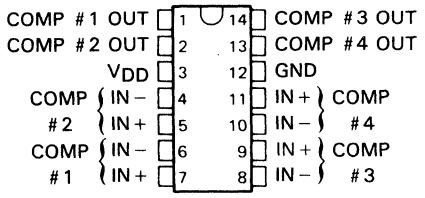
NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

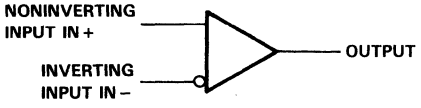
D2901, SEPTEMBER 1985—REVISED NOVEMBER 1990

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 1.4 V to 18 V**
- **Very Low Supply Current Drain**
  300 μA Typ at 5 V
  130 μA Typ at 1.4 V
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM339**

D OR N PACKAGE
(TOP VIEW)



symbol (each comparator)



description

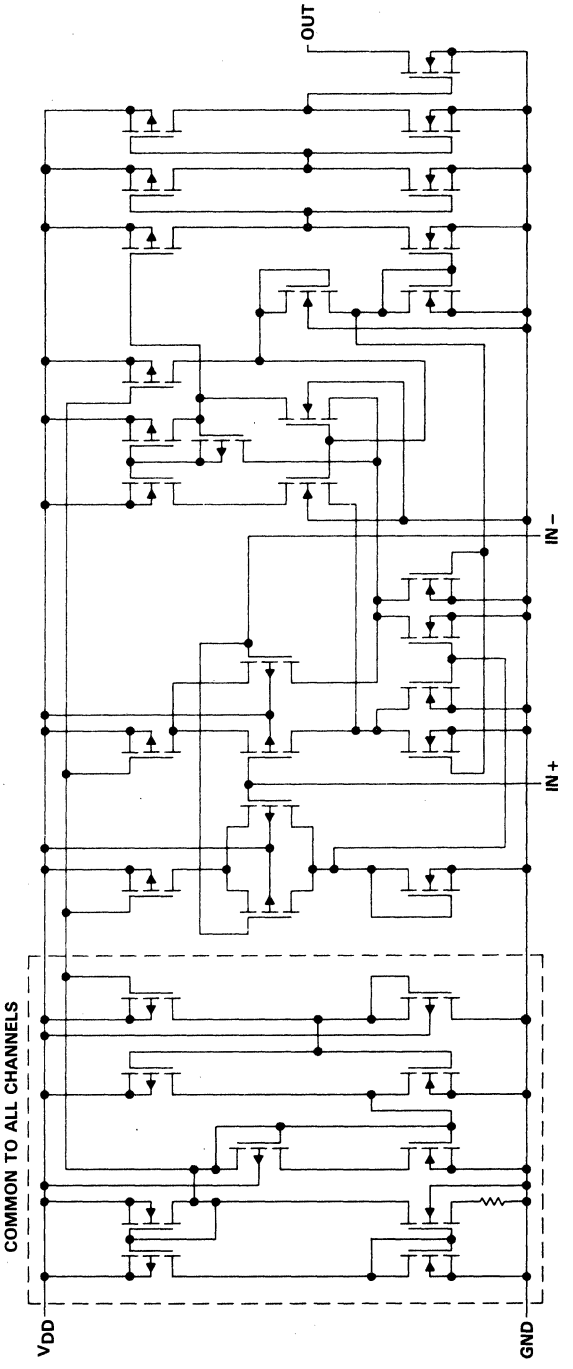
This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators; each is designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC354 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC354C is characterized for operation from 0 °C to 70 °C. The TLC354I is characterized for operation over the industrial temperature range of −40 °C to 85 °C. The TLC354M is characterized for operation over the full military temperature range of −55 °C to 125 °C.

LinCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC354CD	TLC354CN
−40°C to 85°C	5 mV	TLC354ID	TLC354IN
−55°C to 125°C	5 mV	TLC354MD	TLC354MN

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLC354CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC354C . . . . . 0°C to 70°C
TLC354I . . . . . −40°C to 85°C
TLC354M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	494 mW	190 mW
N	500 mW	9.2 mW/°C	96°C	500 mW	500 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	1.4		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	0		0.2	0		0.2	V
	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC354C			TLC354I			TLC354M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V,	I_{OL} = 0.6 mA	25°C		100	200		100	200		100	200	mV
				Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5 V,	V_{OL} = 300 mV	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 0.5 V,	No load	25°C		130	300		130	300		130	300	μA
				Full range			400			400			400	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for the TLC354C, −40°C to 85°C for the TLC354I, and −55°C to 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC354C			TLC354I			TLC354M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.3	0.6		0.3	0.6		0.3	0.6	mA
				Full range			0.8			0.8			0.8	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for the TL354C, −40°C to 85°C for the TLC354I, and −55°C to 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

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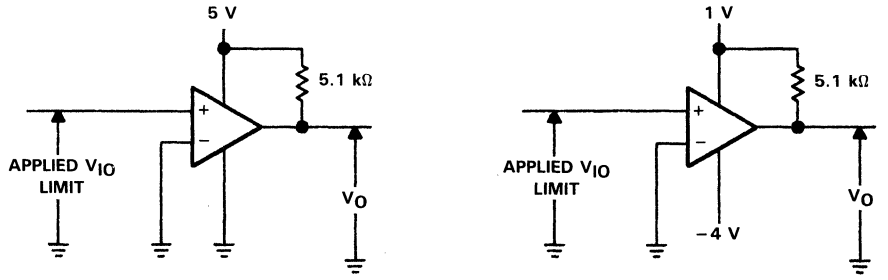


(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

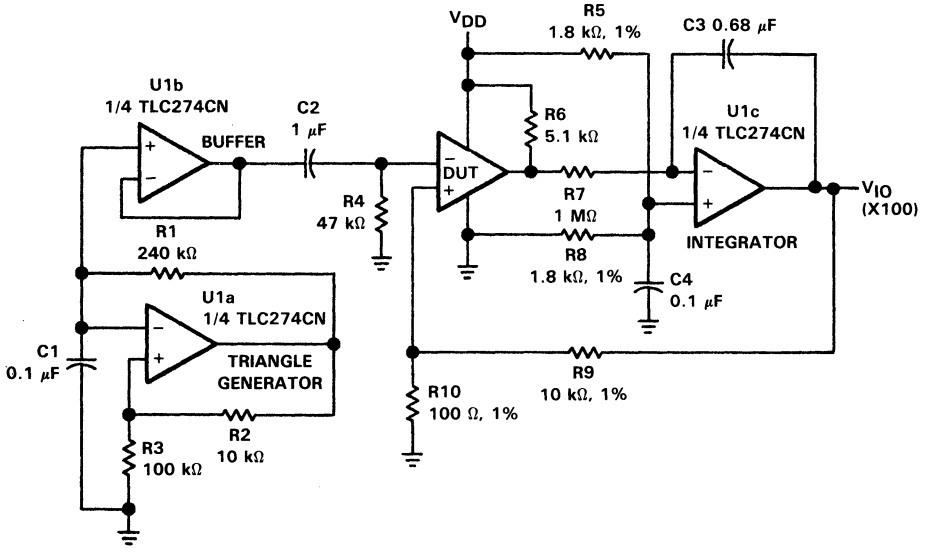
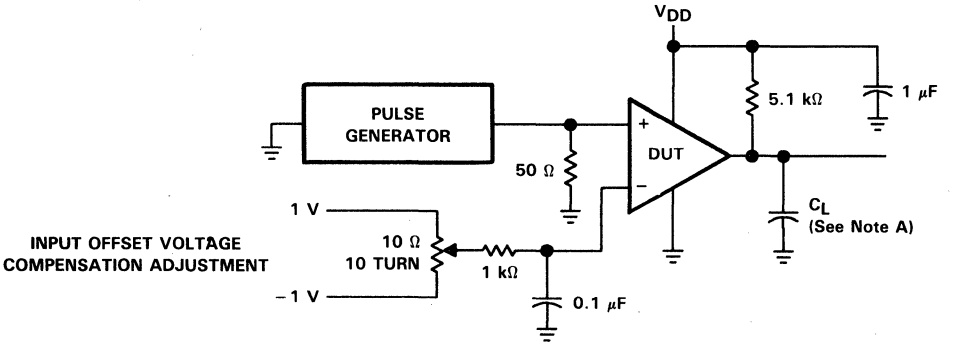


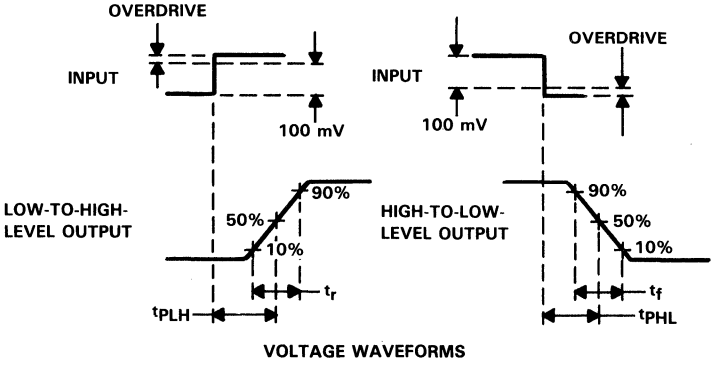
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



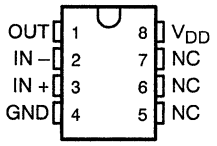
VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

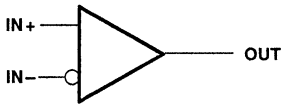
- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages**
  3 V to 16 V
- **Very Low Supply Current Drain**
  75 μA Typ at 5 V
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Bulit-In ESD Protection**
- **Extremely Low Input Bias Current**
  5 pA Typ
- **Ultrastable Low Input Offset Voltage**
- **Common-Mode Input Voltge Range Includes Ground**
- **Output Compatible with TTL, MOS, and CMOS**

D OR P PACKAGE
(TOP VIEW)



NC — No internal connection

symbol



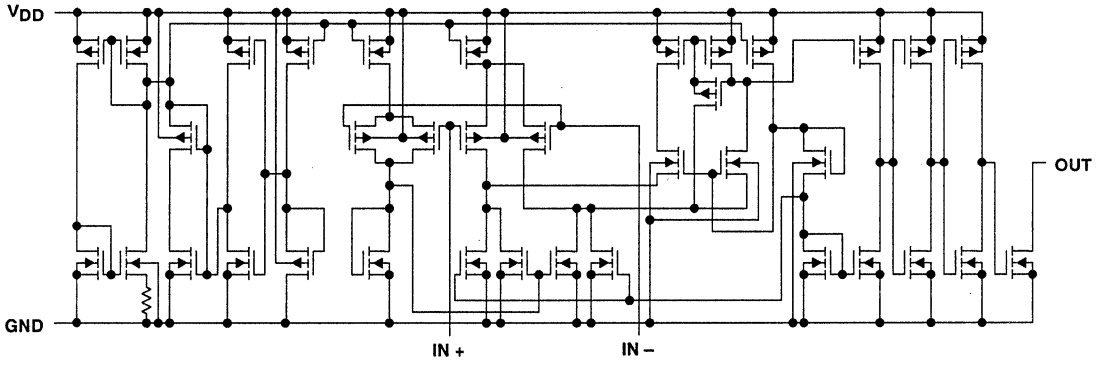
description

The TLC371 is a voltage comparator fabricated using LinCMOS™ technology and designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. The TLC371 features extremely high input impedance, allowing direct interfacing with high-impedance sources. The output is in n-channel open-drain configuration.

The TLC371 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC371C is characterized for operation from 0°C to 70°C. The TLC371I is characterized for operation from – 40°C to 85°C. The TLC371M is characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each comparator)

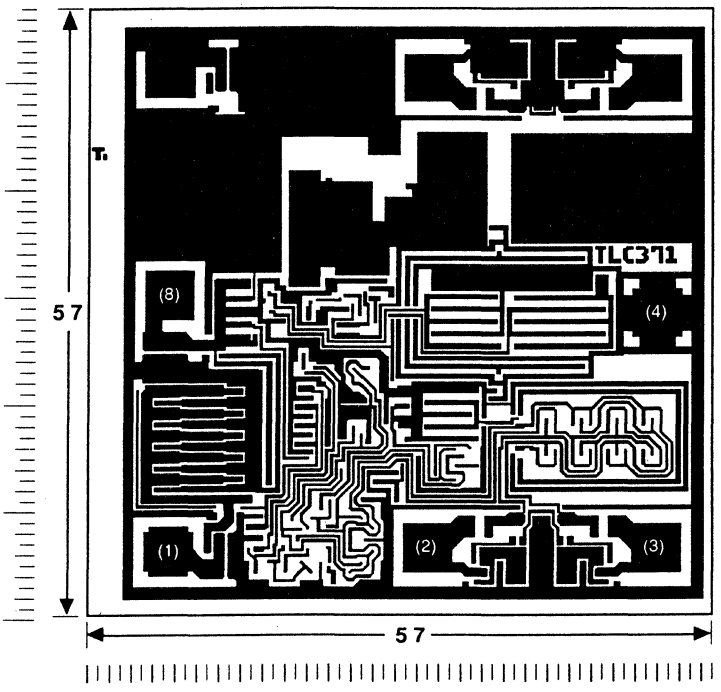


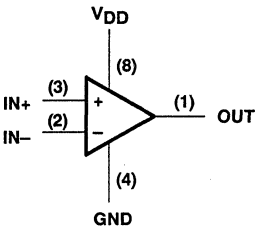
LinCMOS is a trademark of Texas Instruments Incorporated.

chip information

These chips, properly assembled, display characteristics similar to the TLC371 (see electrical table on TLC371Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

NO BACKSIDE METALIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	5 mV	TLC371CD	TLC371CP	TLC371Y†
– 40°C to 85°C	5 mV	TLC371ID	TLC371IP	
– 55°C to 125°C	5 mV	TLC371MD	TLC371MP	

† Chips are tested at T_A = 25°C. See TLC371Y for electrical characteristics.
The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC371CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... – 0.3 to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ± 5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC371C ..... 0 to 70°C
TLC371I ..... – 40°C to 85°C
TLC371M ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
P	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	3		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	–40		85	–55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC371C			TLC371I			TLC371M			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			3	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		75	150		75	150		75	150	μA
				Full range			200			200			200	

† All characateristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC371C, −40°C to 85°C for TLC371I, and −55°C to 125°C for TLC371M. IMPORTANT: See Parameter Measurement Information.

‡ All typical values are at T_A = 25°C.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650		μs
		TTL-level input step		200		

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

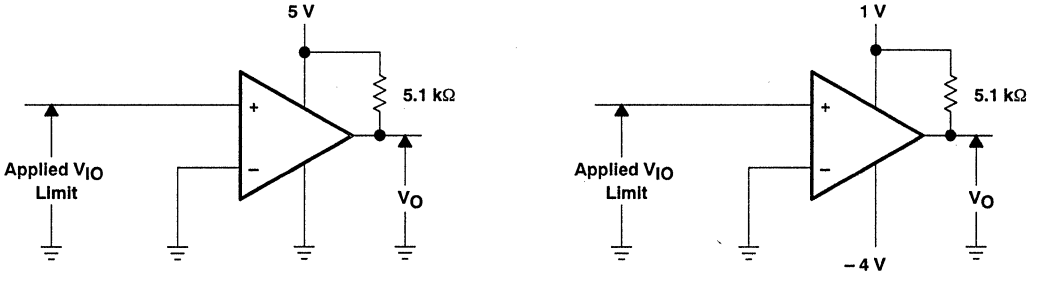
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min		1	5	mV
I_{IO}	Input offset current			1	100	pA
I_{IB}	Input bias current			5	100	pA
V_{ICR}	Common-mode input voltge range		0 to V_{DD} – 1			V
I_{OH}	High-level output current			0.1		nA
V_{OL}	Low-level output voltage			150	400	mV
I_{OL}	Low-level output current		6	16		mA
I_{DD}	Supply current			75	150	μA

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC371 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} With V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASURMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo-loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

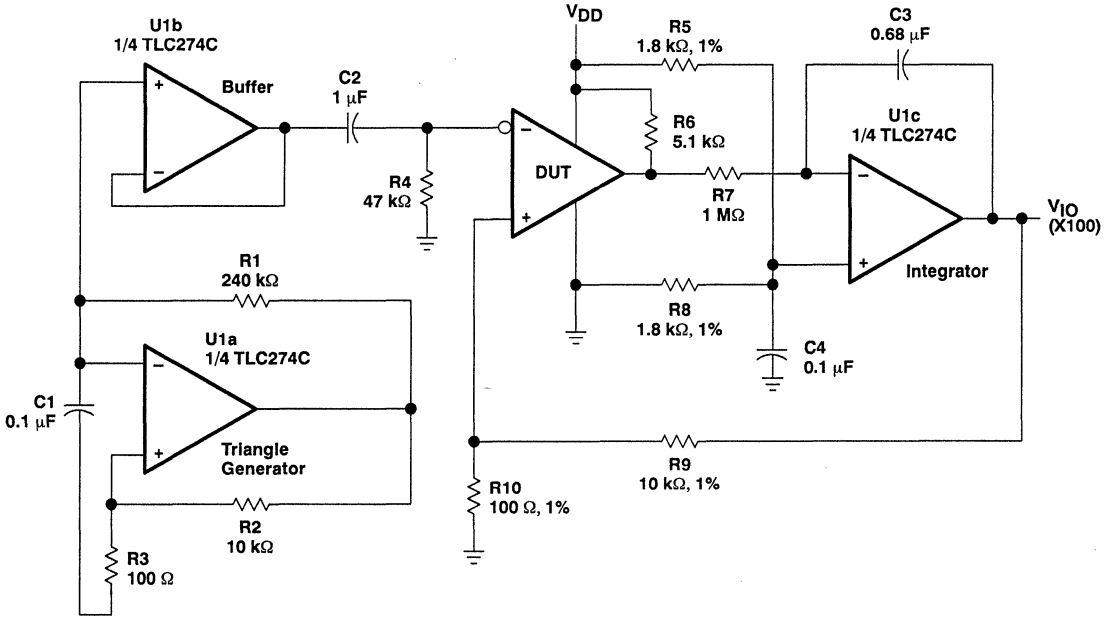
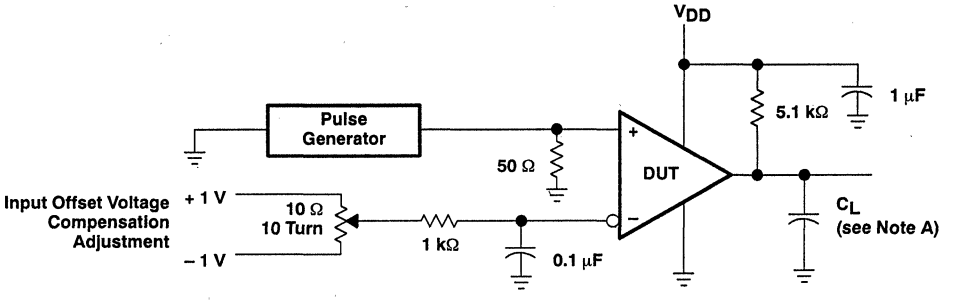


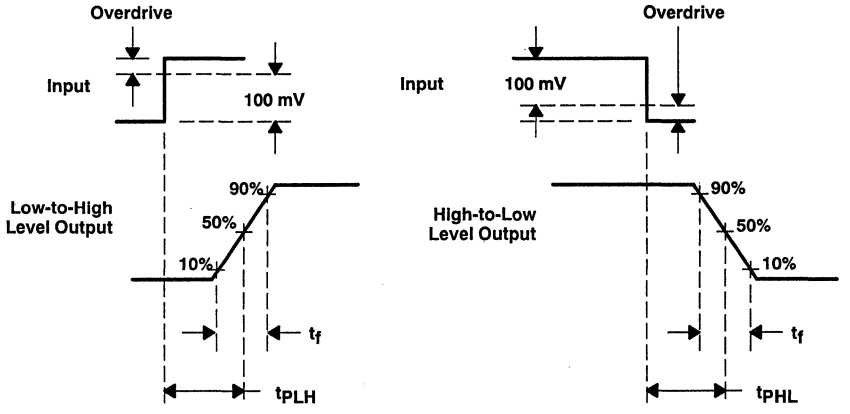
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single- supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. If you have any further questions, please contact your local TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages will tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build-up, each pin is protected by internal circuitry.

Standard ESD protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

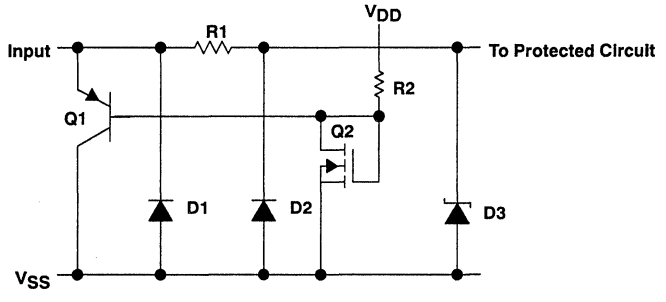


Figure 4. LinCMOS™ ESD Protection Schematic

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input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 will force the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power-up or power-down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it will saturate and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current will be directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

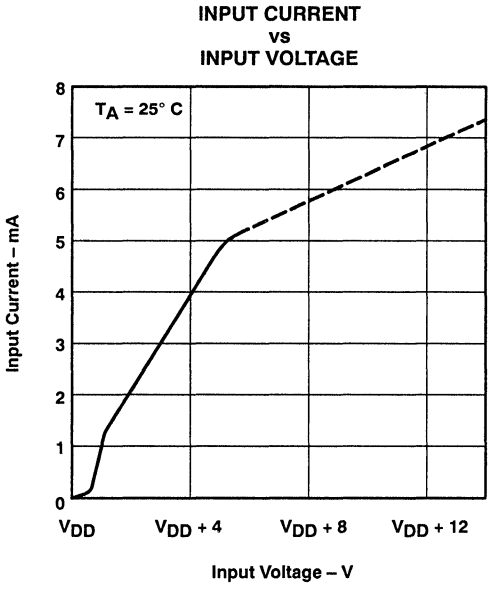


Figure 5

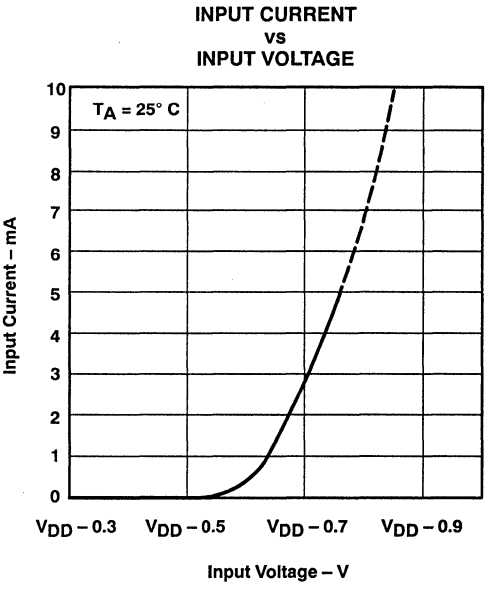
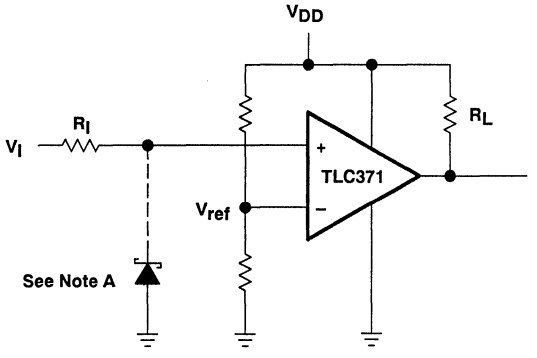


Figure 6



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

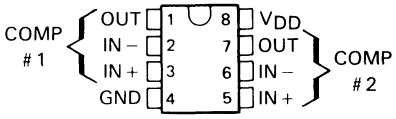
NOTE A: If the correct input state is required when the negative input exceeds V_{SS}, a Schottky clamp is required.

Figure 7. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

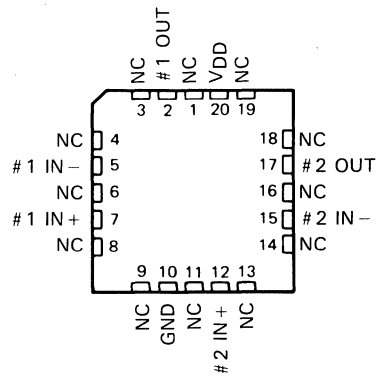
D2821, NOVEMBER 1983—REVISED OCTOBER 1990

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 2 V to 18 V**
- **Very Low Supply Current Drain 150 μA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . $10^{12}\ \Omega$ Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM393**

TLC372C, TLC372I, TLC372M, TLC372Q
D OR P PACKAGE
TLC372M . . . JG PACKAGE
(TOP VIEW)



TLC372M . . . FK PACKAGE
(TOP VIEW)

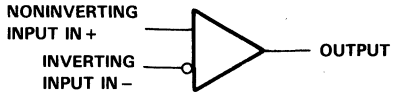


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features extremely high input impedance (typically greater than $10^{12}\ \Omega$), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372C is characterized for operation from 0°C to 70°C. The TLC372I is characterized for operation from −40°C to 85°C. The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372Q is characterized for operation from −40°C to 125°C.

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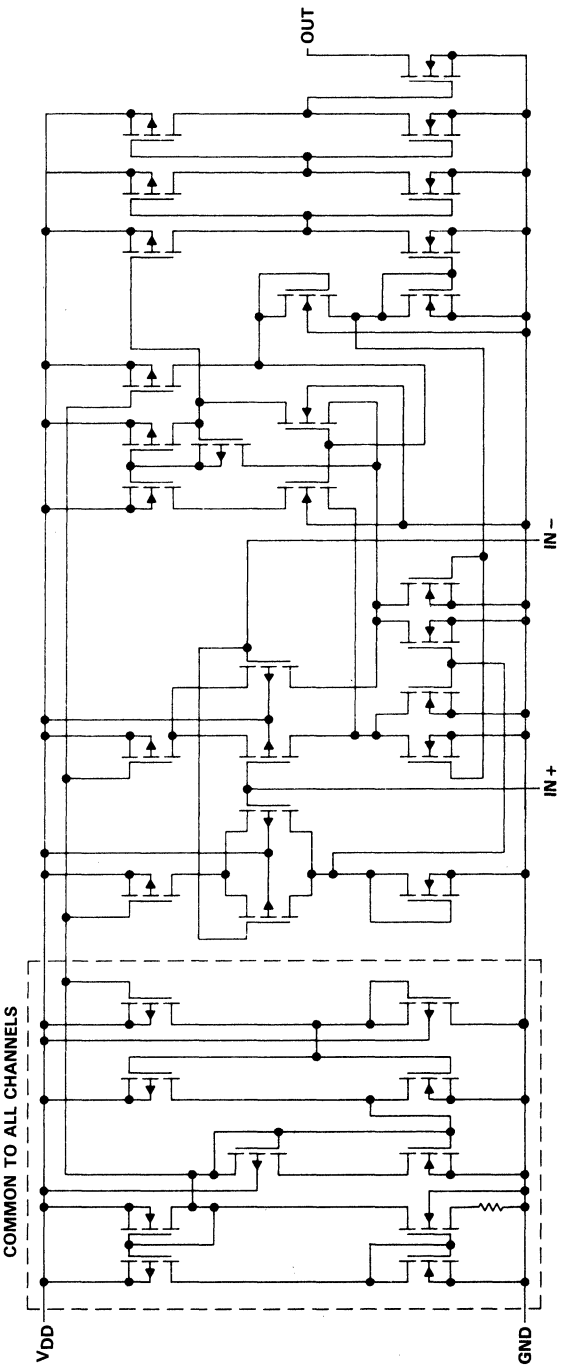
equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC372CD	–	–	TLC372CP
−40°C to 85°C	5 mV	TLC372ID	–	–	TLC372IP
−55°C to 125°C	5 mV	TLC372MD	TLC372MFK	TLC372MJG	TLC372MP
−40°C to 125°C	5 mV	TLC372QD	–	–	TLC372QP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g., TLC372CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage range, V_I . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC372C . . . . . 0°C to 70°C
TLC372I . . . . . −40°C to 85°C
TLC372M . . . . . −55°C to 125°C
TLC372Q . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			Q-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	3		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	−40		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC372C			TLC372I			TLC372M/Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD}−1			0 to V_{DD}−1			0 to V_{DD}−1			V
				Full range	0 to V_{DD}−1.5			0 to V_{DD}−1.5			0 to V_{DD}−1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			3	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		150	300		150	300		150	300	μA
				Full range			400			400			400	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC372C, −40°C to 85°C for TLC372I, −55°C to 125°C for TLC372M, and −40°C to 125°C for TLC372Q. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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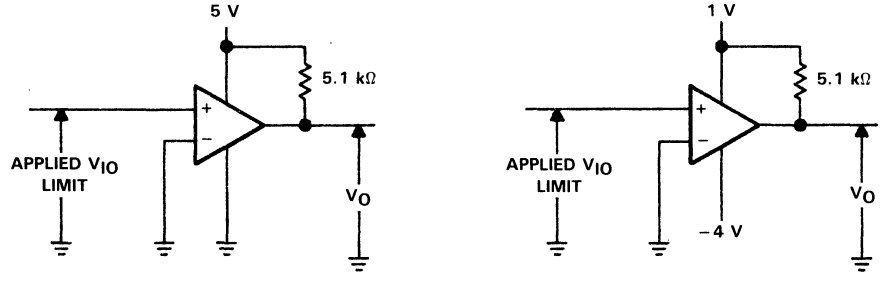
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC372 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

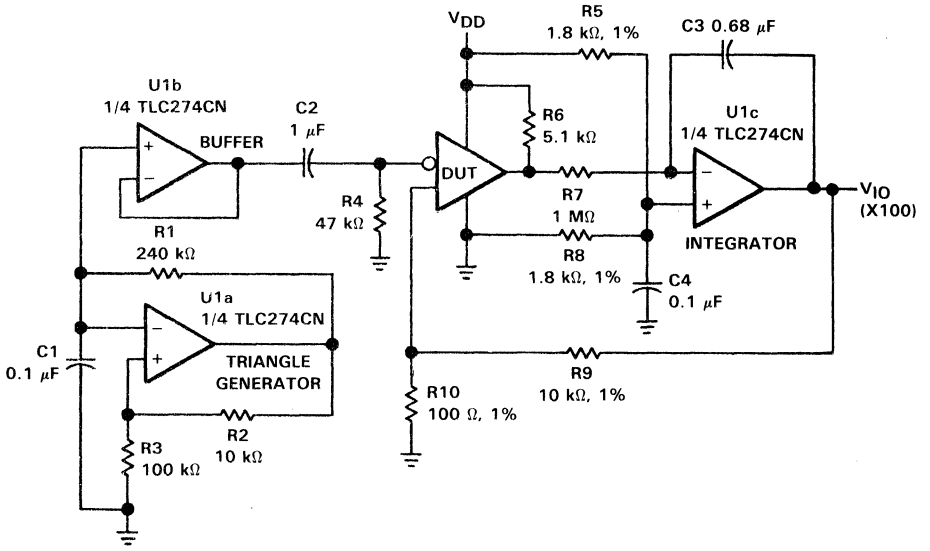
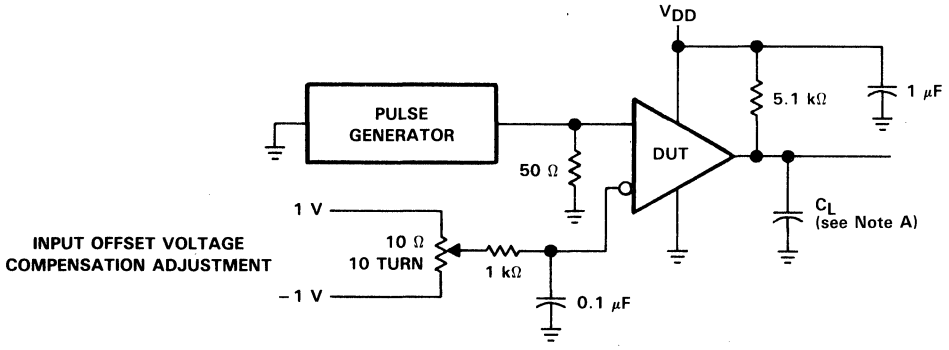


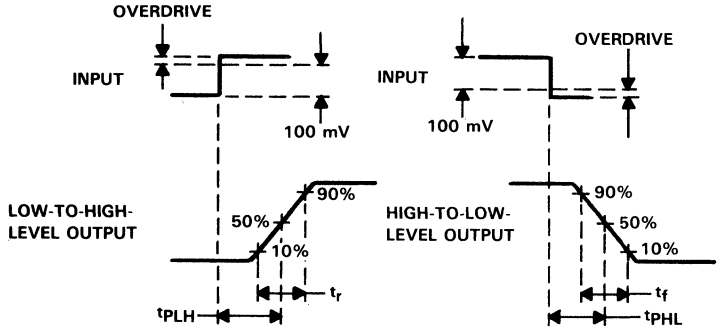
FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

LinCMOS™ process

LinCMOS™ process is a Linear polysilicon-gate Complementary-MOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions, from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. If you have any further questions, please contact your local TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g. during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages will tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build-up, each pin is protected by internal circuitry.

Standard ESD protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

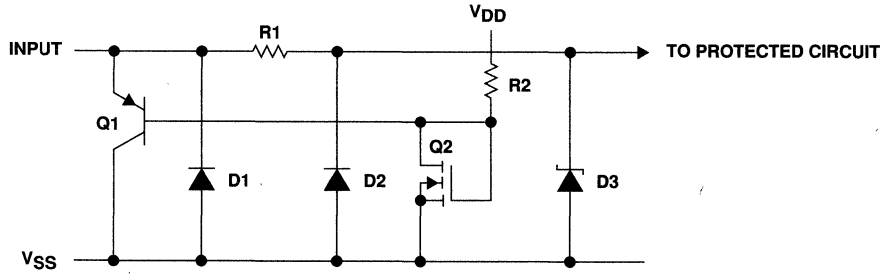


FIGURE 4. LinCMOS™ ESD PROTECTION SCHEMATIC

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 will force the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded, and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is -0.3 V to -1 V, (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under "normal" operation, these conditions occur during circuit power-up or power-down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ± 5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it will saturate and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current will be directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

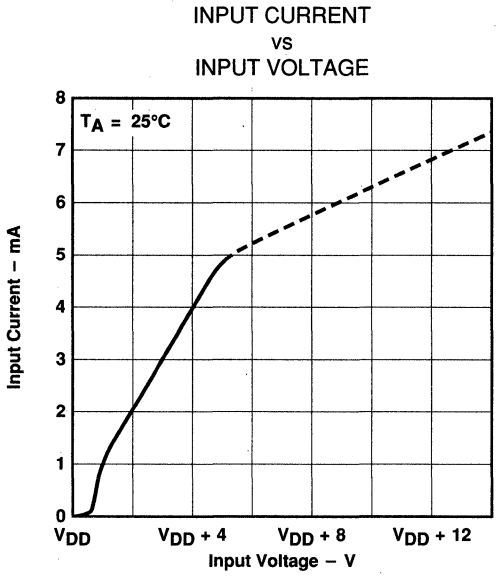


FIGURE 5

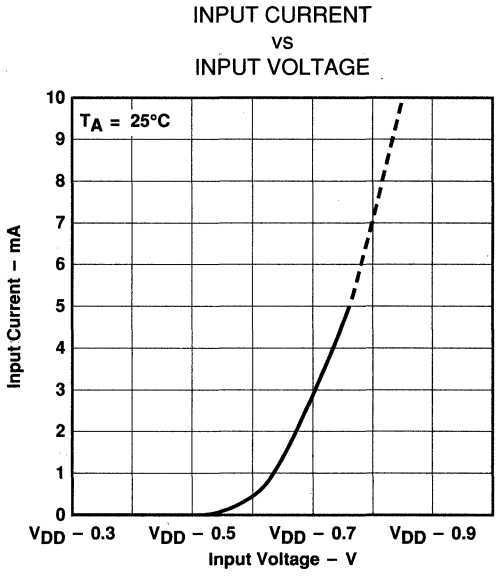
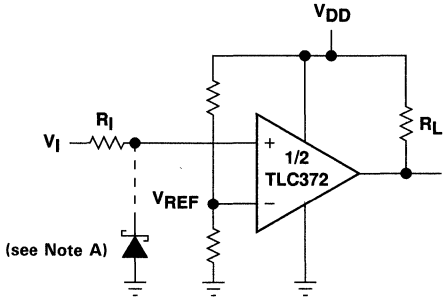


FIGURE 6



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

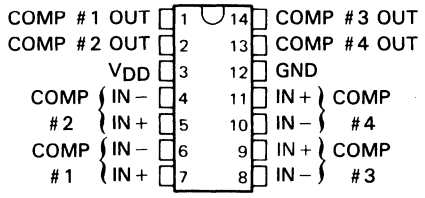
Note A: If the correct output state is required when the negative input exceeds V_{SS}, a schottky clamp is required.

FIGURE 7. TYPICAL INPUT CURRENT-LIMITING CONFIGURATION FOR A LinCMOS™ COMPARATOR

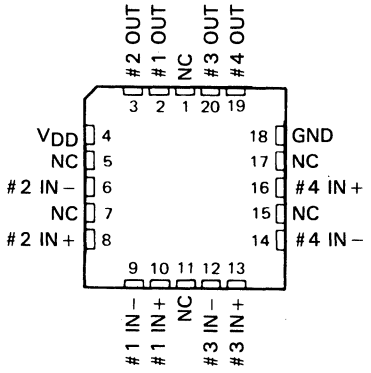
D2783, NOVEMBER 1983—REVISED MAY 1990

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 2 V to 18 V**
- **Very Low Supply Current Drain 0.3 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM339**

TLC374C, TLC374I, TLC374Q . . . D OR N PACKAGE
TLC374M . . . J PACKAGE
(TOP VIEW)



TLC374M . . . FK PACKAGE
(TOP VIEW)

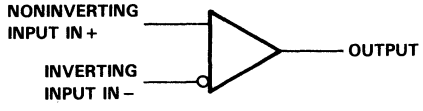


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features extremely high input impedance (typically greater than $10^{12}\ \Omega$) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374C is characterized for operation from 0 °C to 70 °C. The TLC374I is characterized for operation from −40 °C to 85 °C. The TLC374M is characterized for operation over the full military temperature range of −55 °C to 125 °C. The TLC374Q is characterized for operation from −40 °C to 125 °C.

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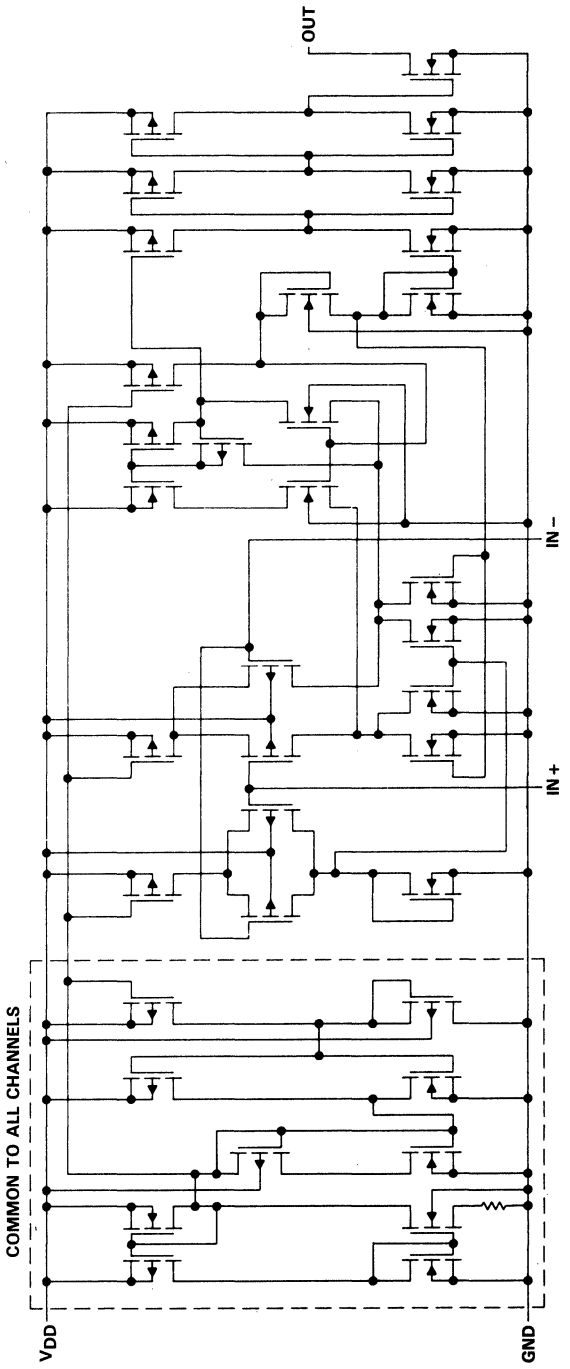
equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC374CD	–	–	TLC374CN
−40°C to 85°C	5 mV	TLC374ID	–	–	TLC374IN
−55°C to 125°C	5 mV	TLC374MD	TLC374MFK	TLC374MJ	TLC374MN
−40°C to 125°C	5 mV	TLC374QD	–	–	TLC374QN

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TLC374CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC374C . . . . . 0°C to 70°C
TLC374I . . . . . −40°C to 85°C
TLC374M . . . . . −55°C to 125°C
TLC374Q . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	494 mW	190 mW
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
N	500 mW	9.2 mW/°C	95°C	500 mW	500 mW	230 mW

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			Q-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	−40		85	−55		125	−40		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC374C			TLC374I			TLC374M/Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD}−1			0 to V_{DD}−1			0 to V_{DD}−1			V
				Full range	0 to V_{DD}−1.5			0 to V_{DD}−1.5			0 to V_{DD}−1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		300	600		300	600		300	600	μA
				Full range			800			800			800	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC374C, −40°C to 85°C for TLC374I, −55°C to 125°C for TLC374M, and −40°C to 125°C for TLC374Q. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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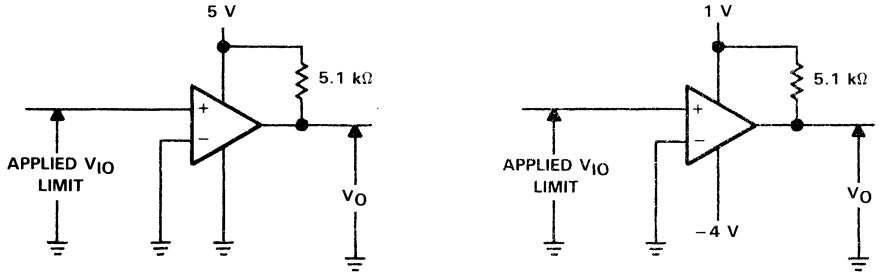
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC374 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity to the input offset voltage, the output will change state.



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is ''sliced'' symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

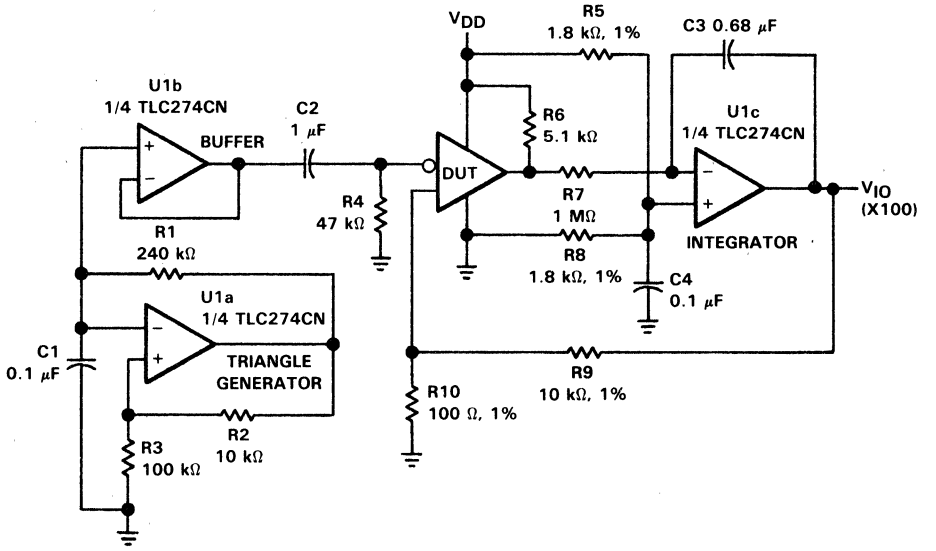
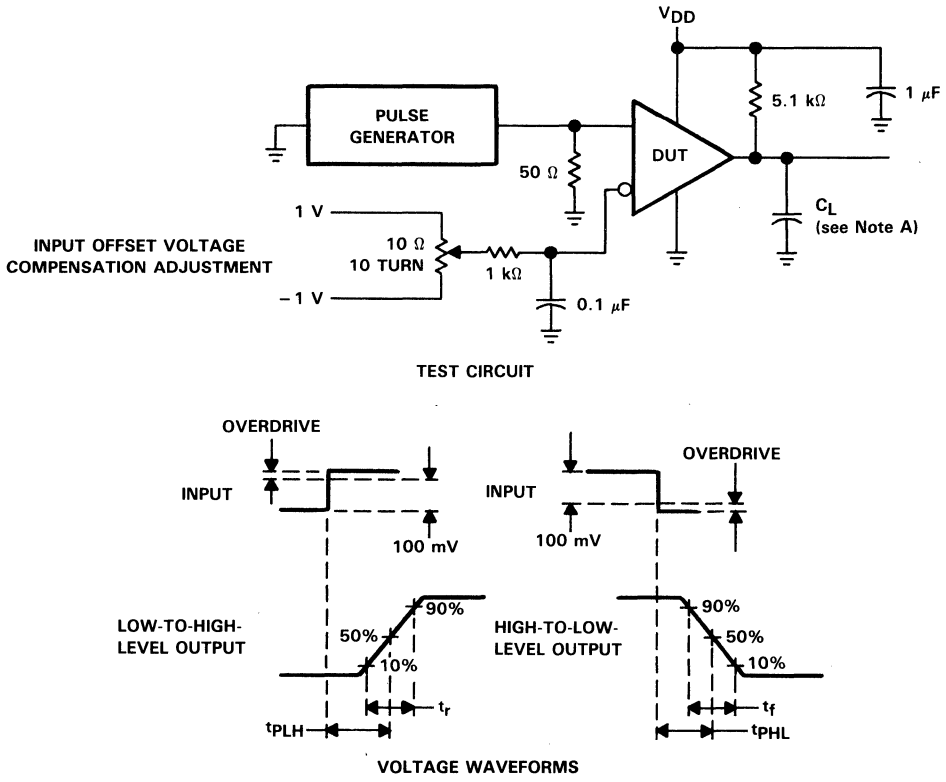


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

PRINCIPLES OF OPERATION

LinCMOS™ process

LinCMOS™ process is a Linear polysilicon-gate Complementary-MOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions, from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. If you have any further questions, please contact your local TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages will tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build-up, each pin is protected by internal circuitry.

Standard ESD protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

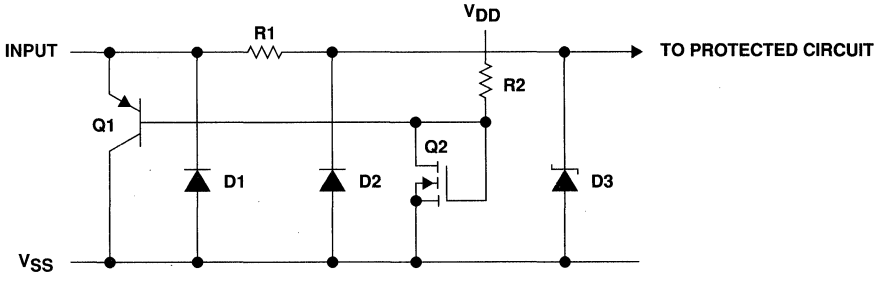


FIGURE 4. LinCMOS™ ESD PROTECTION SCHEMATIC

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 as Q1 saturates forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn on Q2. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward-biased. The voltage seen by the protected circuit is -0.3 V to -1.0 V, (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under "normal" operation, these conditions occur during circuit power-up or power-down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ± 5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. The input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it will saturate and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current will be directly shunted by D1 and D2, and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

TYPICAL CHARACTERISTICS

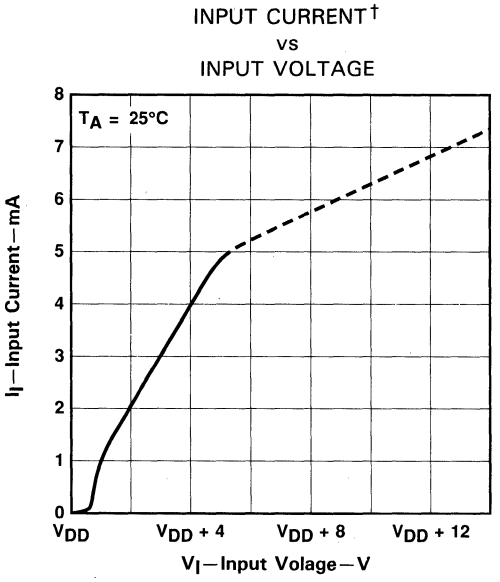


FIGURE 5

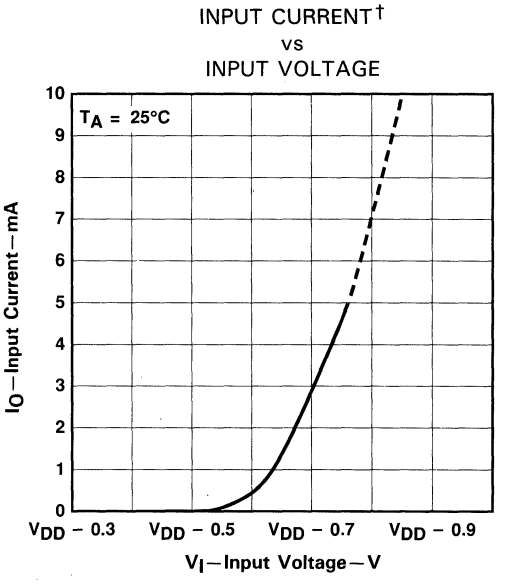
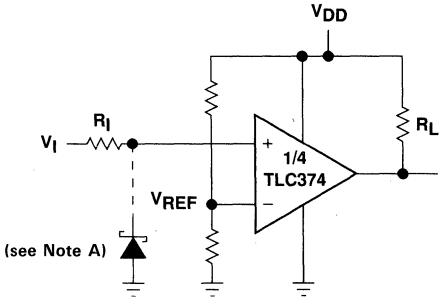


FIGURE 6

†The dashed line identifies an area of operation where some degradation of parametric performance may be experienced.



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

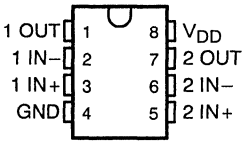
Note A: If the correct output state is required when the negative input exceeds V_{SS}, a schottky clamp is required.

FIGURE 7. TYPICAL INPUT CURRENT-LIMITING CONFIGURATION FOR A LinCMOS™ COMPARATOR

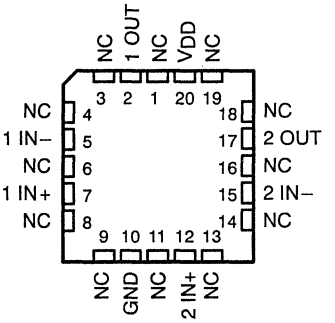
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Very Low Power . . . 110 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  TLC393C . . . 3 V to 16 V
  TLC393I . . . 3 V to 16 V
  TLC393M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



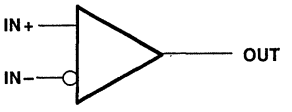
NC — No internal connection

description

The TLC393 consists of dual independent micropower voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies. For a similar device with a push-pull output configuration, see the TLC3702 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



The TLC393C is characterized for operation over the commercial temperature range of 0°C to 70°C.
The TLC393I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C.
The TLC393M is characterized for operation over the full military temperature range of – 55°C to 125°C.

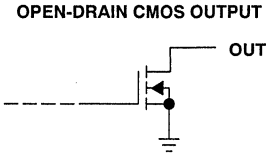
AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC393CD	—	—	TLC393CP
– 40°C to 85°C	5 mV	TLC393ID	—	—	TLC393IP
– 55°C to 125°C	5 mV	TLC393MD	TLC393MFK	TLC393MJG	TLC393MP

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC393CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (see Note 1) ..... −0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... −0.3 V to V_{DD}
Output voltage range, V_O ..... −0.3 V to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... 20 mA
Total supply current into V_{DD} terminal ..... 40 mA
Total current out of ground terminal ..... 40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC393C ..... 0°C to 70°C
TLC393I ..... −40°C to 85°C
TLC393M ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			0°C to 70°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 85°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			−40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OH} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 VmA	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	µA
			−40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			−55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

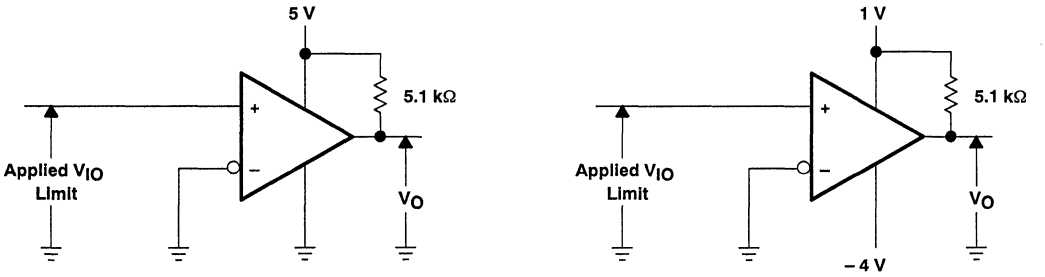
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.1		
t_{PHL}	Propagation delay time, high-to-low-level output	V_I = 1.4-V step at IN+ pin			1.1		
		f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4-V step at IN+ pin			0.10		
t_f	Fall time, output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		22		ns

PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection ratio, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V (b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

The voltage divider formed by R9 and R10 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASURMENT INFORMATION

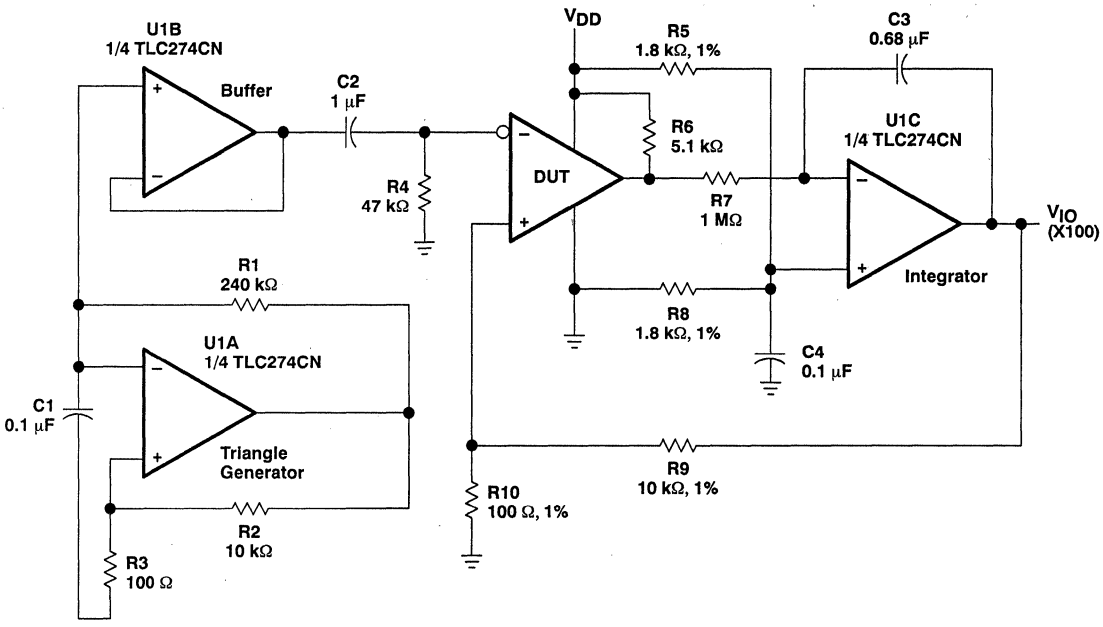
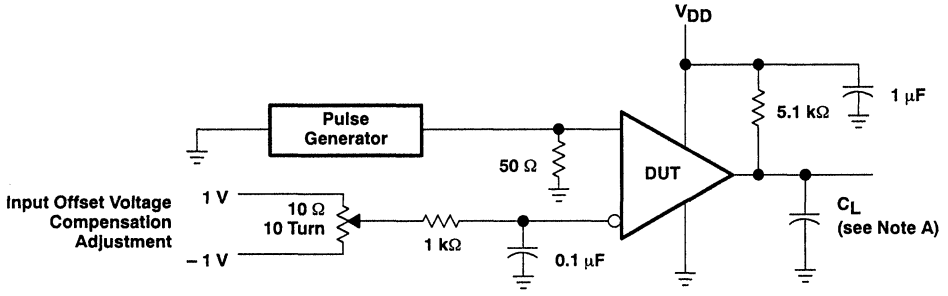


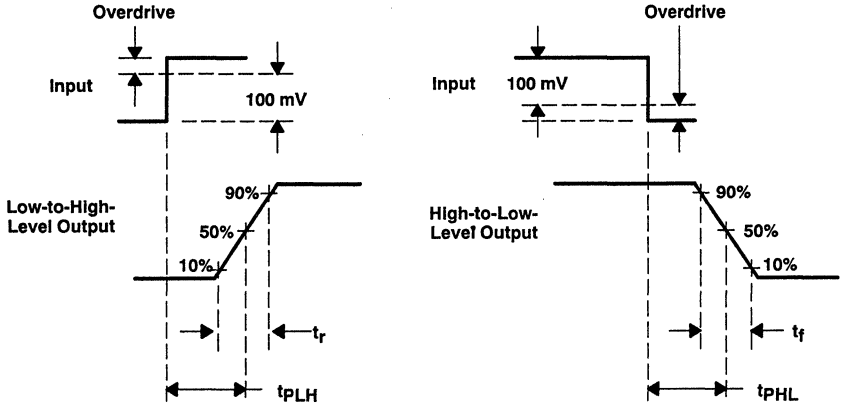
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105 mV or 5 mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise Time, and Fall Time Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

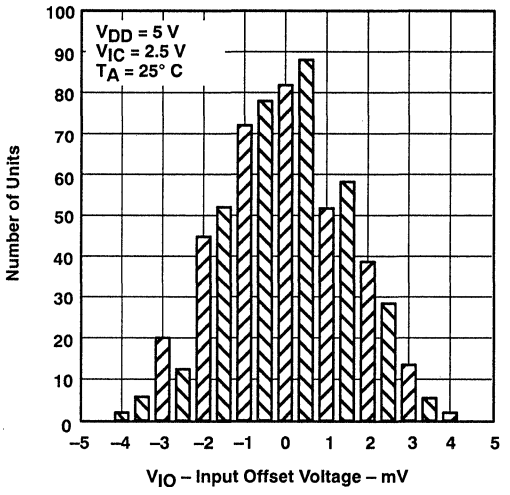


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

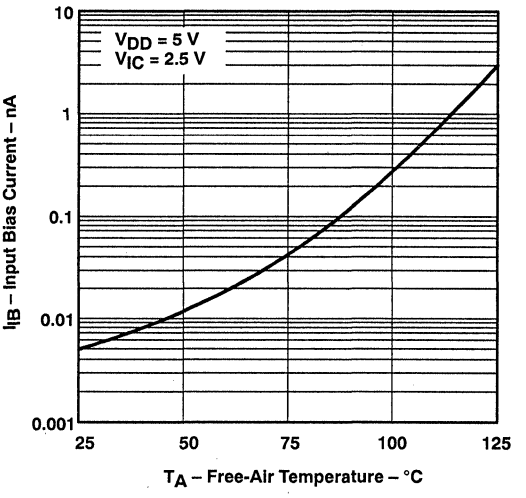


Figure 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

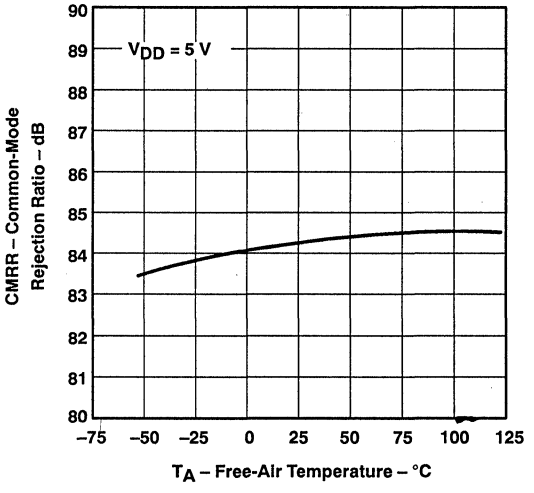


Figure 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

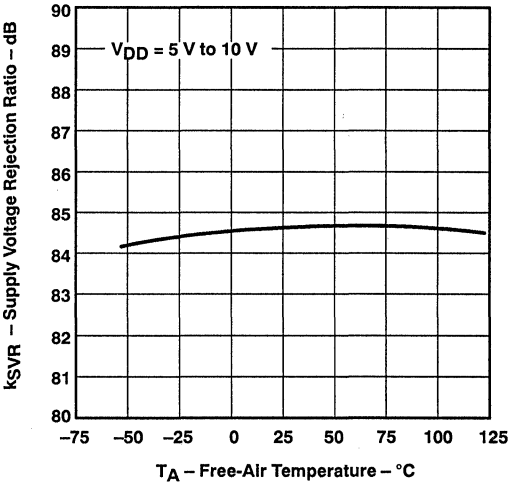


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

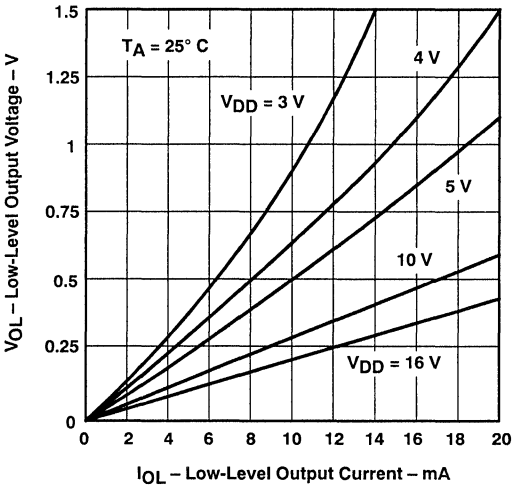


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

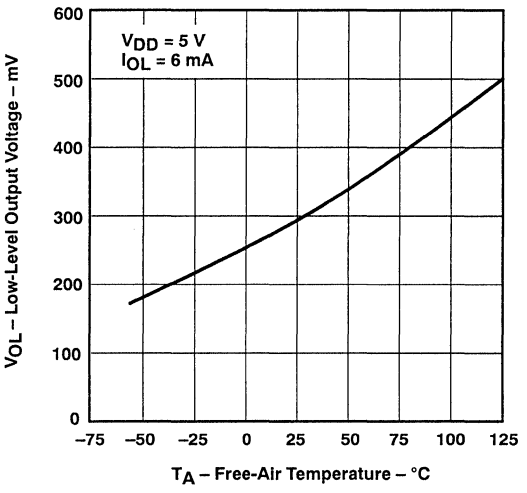


Figure 9

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

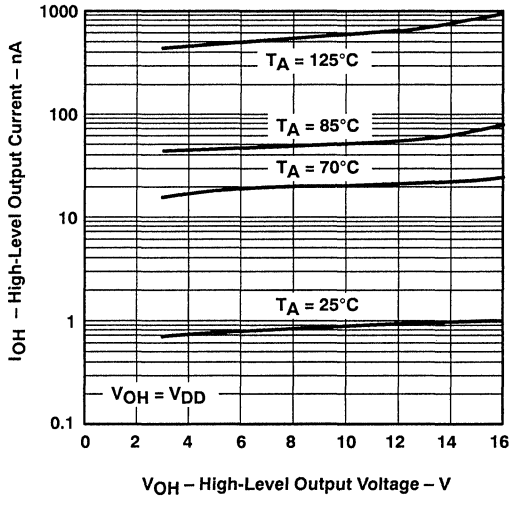


Figure 10

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

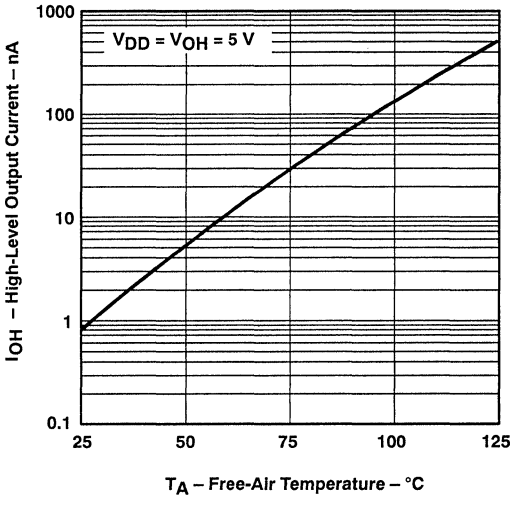


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

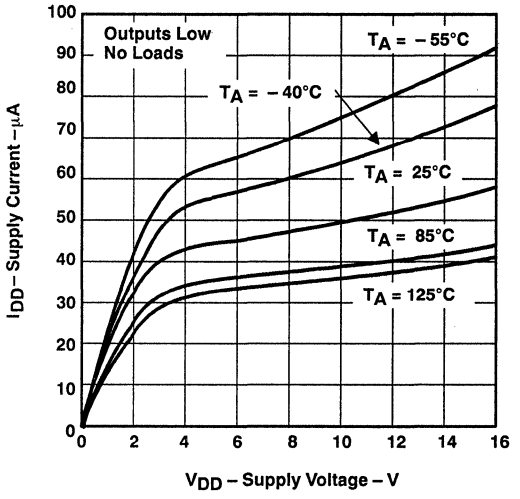


Figure 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

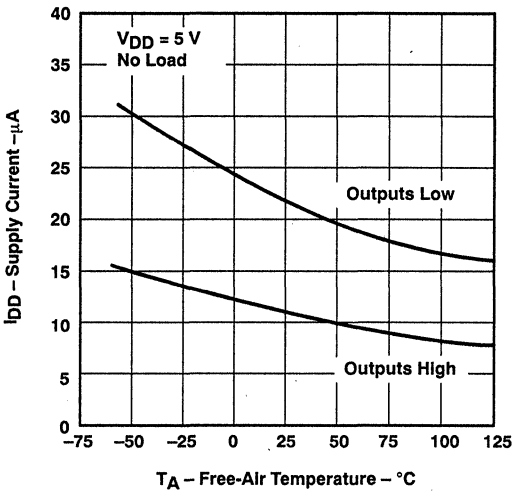


Figure 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

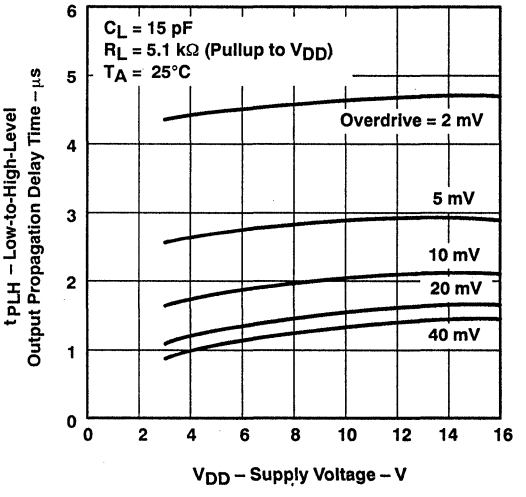


Figure 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

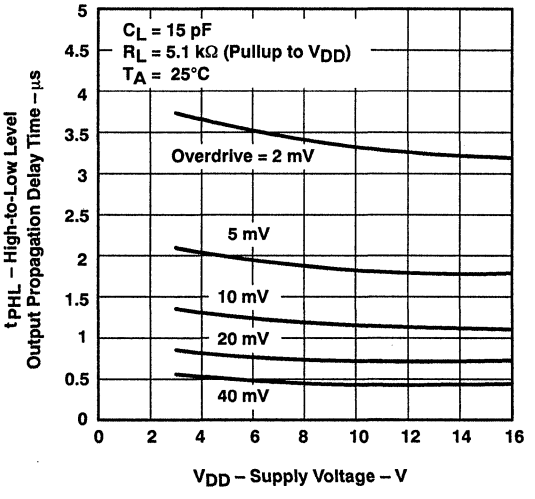


Figure 15

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS INPUT OVERDRIVES

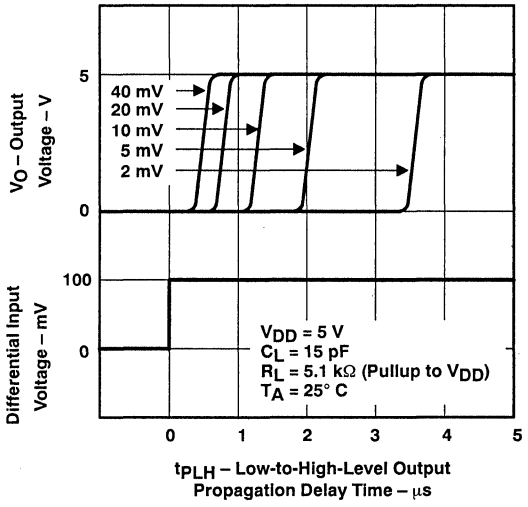


Figure 16

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS INPUT OVERDRIVES

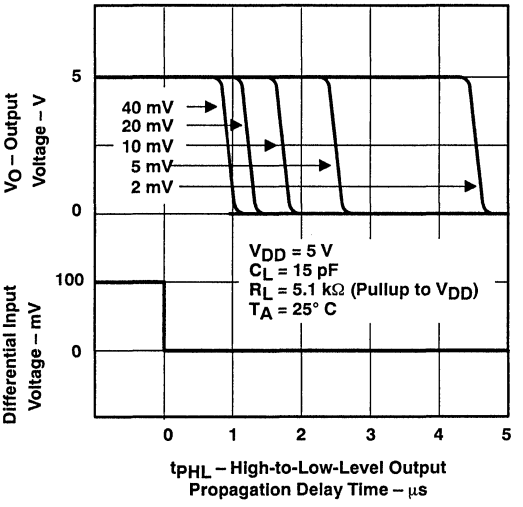


Figure 17

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

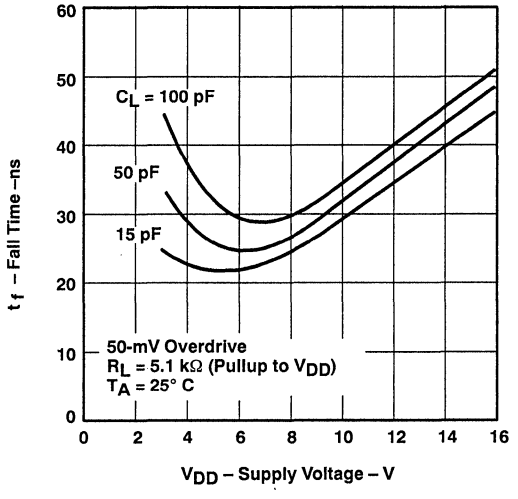


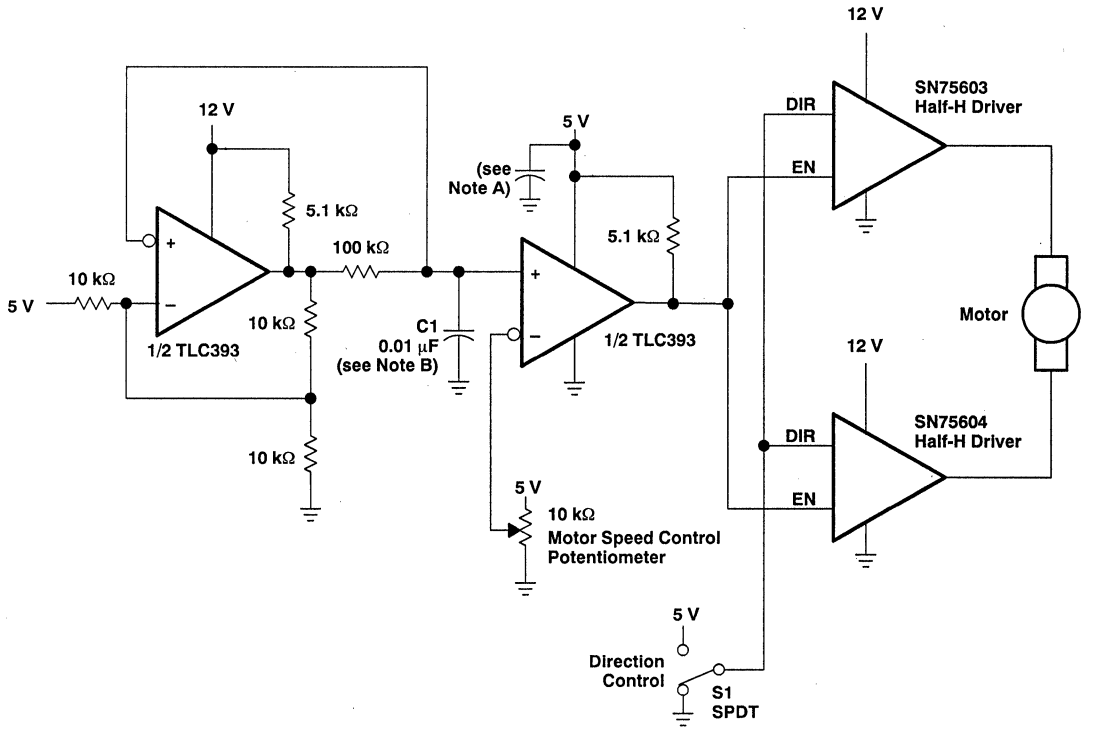
Figure 18.

APPLICATION INFORMATION

The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input cuurent is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1-μF) positioned as close to the device as possible.

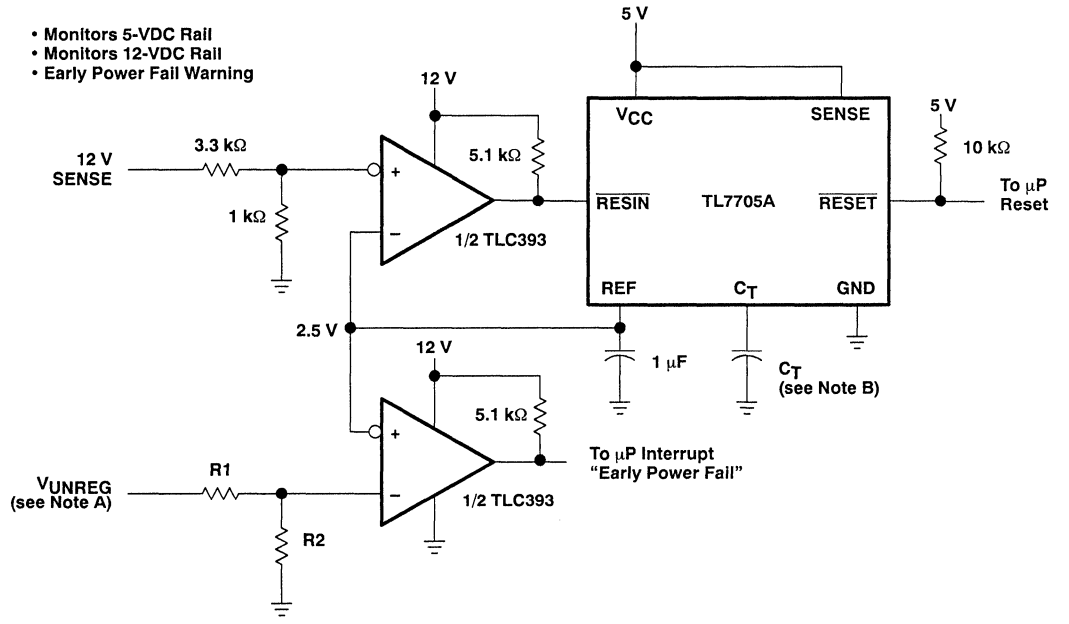
The TLC393 has internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

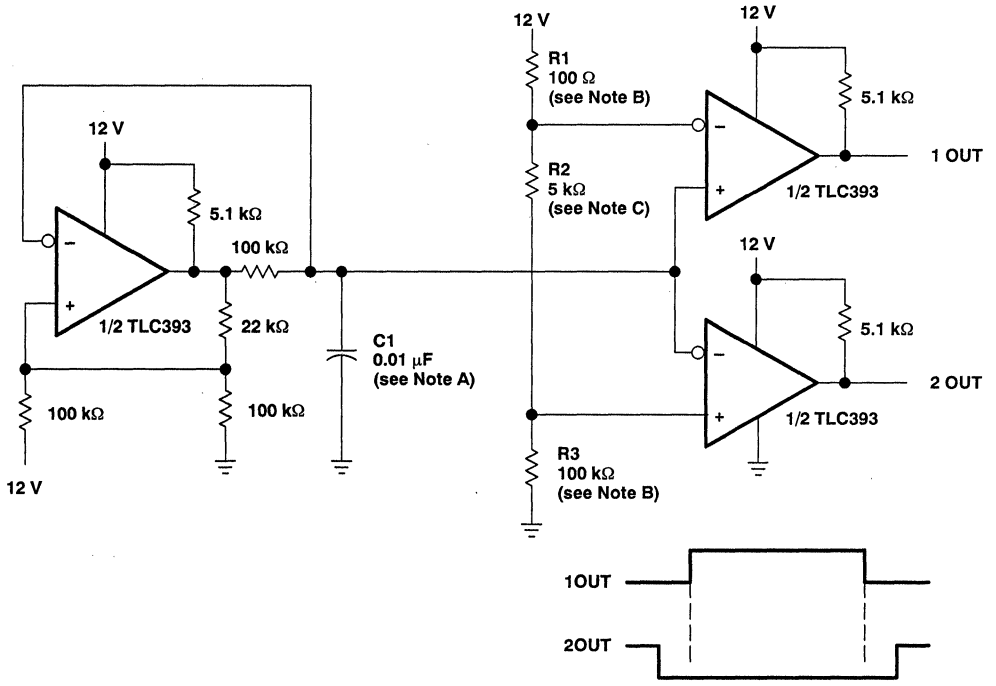


NOTES: A. $V_{UNREG} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor

APPLICATION INFORMATION



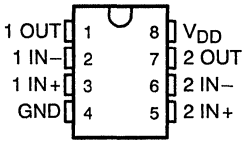
NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\ k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle.
C. Adjust R2 to change deadtime.

Figure 21. Two-Phase Nonoverlapping Clock Generator

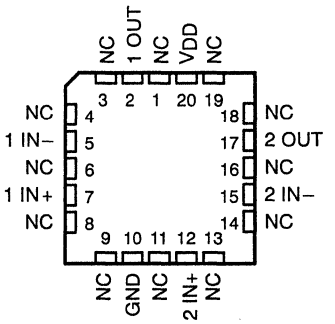
D3209, NOVEMBER 1986 — REVISED NOVEMBER 1991

- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 100 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single-Supply Operation . . . 3 V to 16 V**
  TLC3702M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



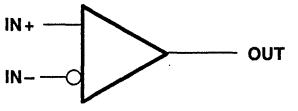
NC–No internal connection

description

The TLC3702 consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC3702CD	—	—	TLC3702CP
– 40°C to 85°C	5 mV	TLC3702ID	—	—	TLC3702IP
– 55°C to 125°C	5 mV	—	TLC3702MFK	TLC3702MJG	—
– 40°C to 125°C	5 mV	—	—	TLC3702QJG	—

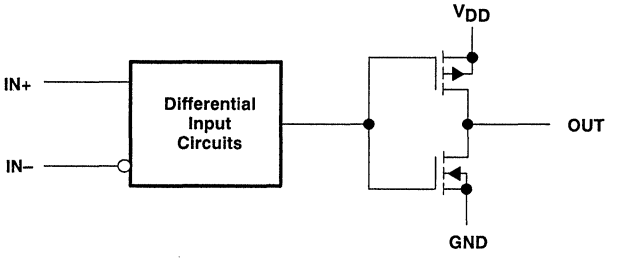
The D package is available taped and reeled. Add "R" suffix to the device type (e.g., TLC3702CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3702I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC3702M is characterized for operation over the full military temperature range of − 55°C to 125°C. The TLC3702Q is characterized for operation from − 40°C to 125°C.

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (see Note 1) ..... − 0.3 V to 18 V
Differential input voltage (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... − 0.3 to V_{DD}
Output voltage range, V_O ..... − 0.3 to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... ± 20 mA
Total supply current into V_{DD} terminal ..... 40 mA
Total current out of ground terminal ..... 40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC3702C ..... 0 to 70°C
TLC3702I ..... − 40°C to 85°C
TLC3702M ..... − 55°C to 125°C
TLC3702Q ..... − 40°C to 125°C
Storage temperature range ..... − 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			0°C to 70°C				
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			0°C to 70°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = – 4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = – 1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		18	40	μA
			0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				−40°C to 85°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				85°C		84		
				−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				85°C			400	
I_{DD}	Supply current (both comparators)	No load,	Outputs low	25°C		18	40	μA
				−40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			−55°C to 125°C				
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		83		
			−55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		18	40	µA
			−55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				−40°C to 125°C				
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1			V
				−40°C to 125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		83		
				−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (both comparators)	No load,	Outputs low	25°C		18	40	μA
				−40°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	V_I = 1.4 V step at IN + pin			1.1		µs
		f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN + pin			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs will cause degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. If you have any further questions, please contact your local TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages will tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

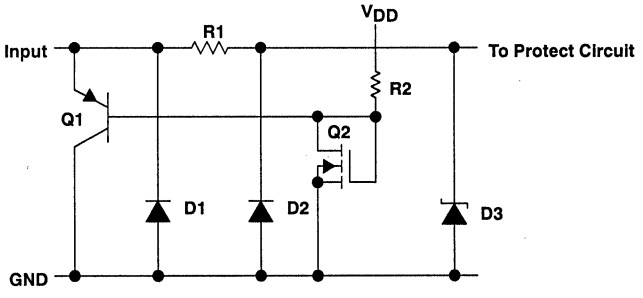


Figure 1. LinCMOS™ ESD-Protection Schematic

LinCMOS and Advanced LinCMOS are trademarks of Texas Instruments Incorporated.

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 will force the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 2 and 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it will saturate and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current will be directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

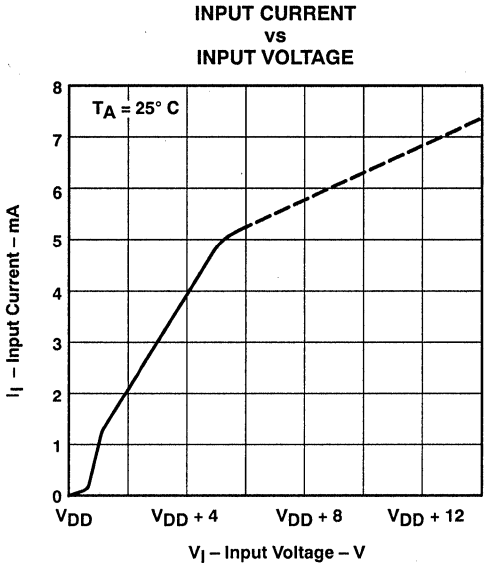


Figure 2

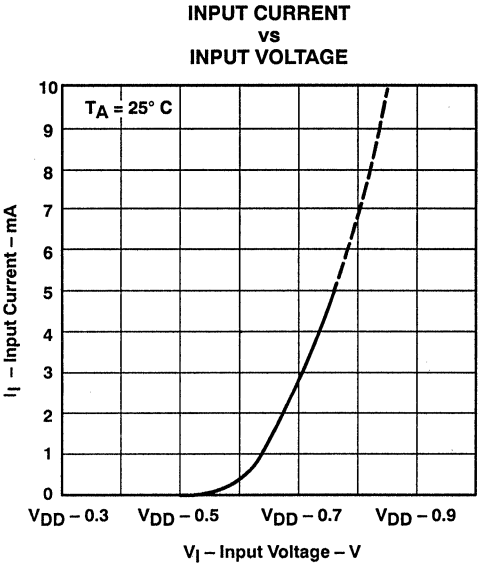
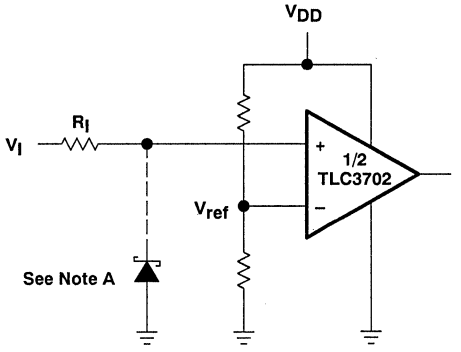


Figure 3



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

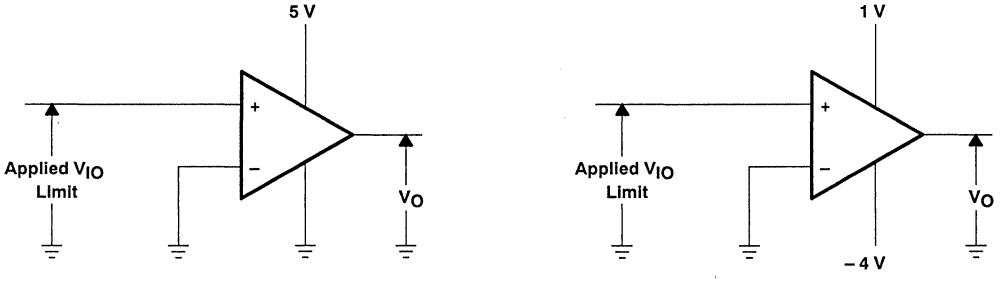
A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.



(a) V_{IO} WITH V_{IC} = 0 V (b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASURMENT INFORMATION

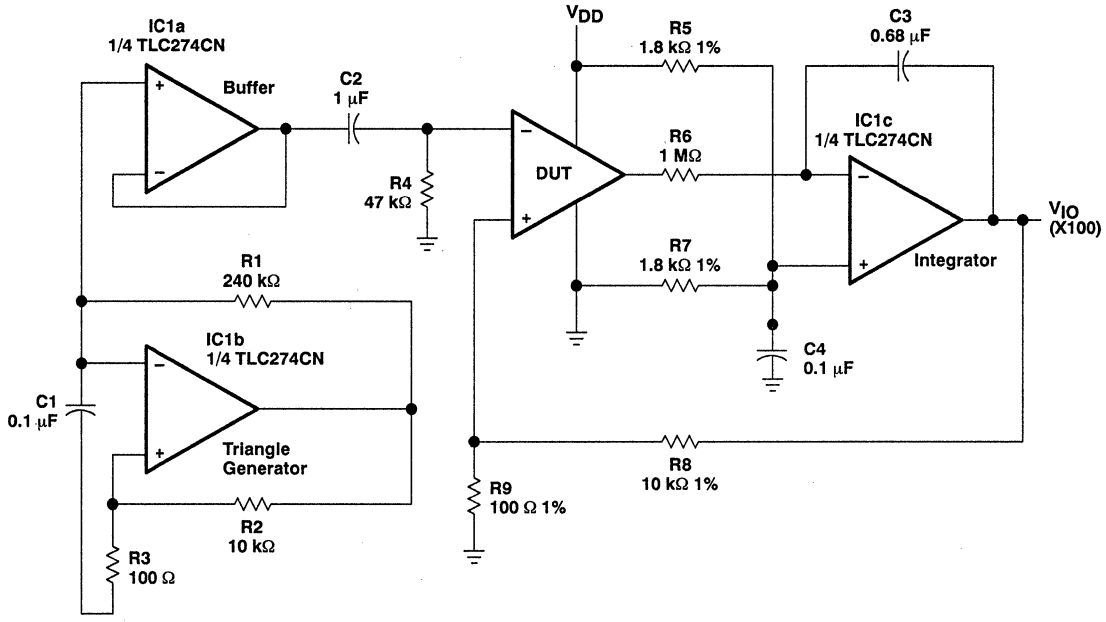
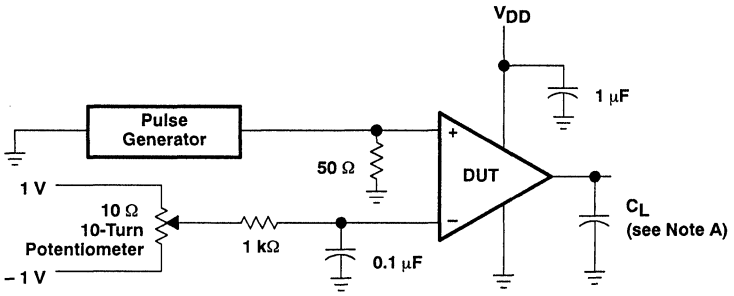


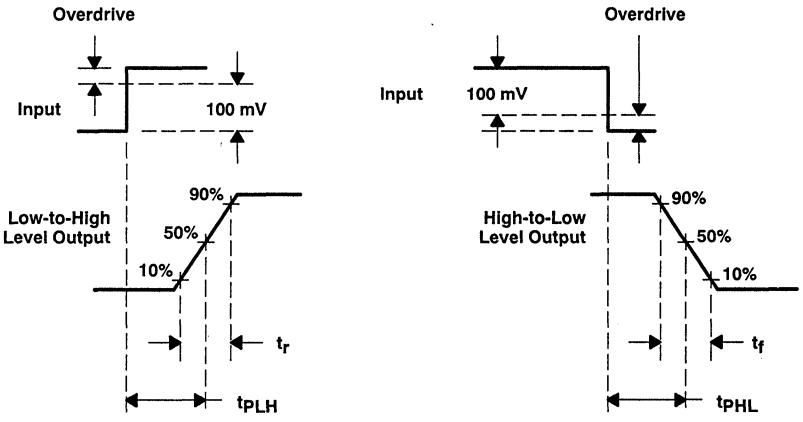
Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 7) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.

PARAMETER MEASURMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

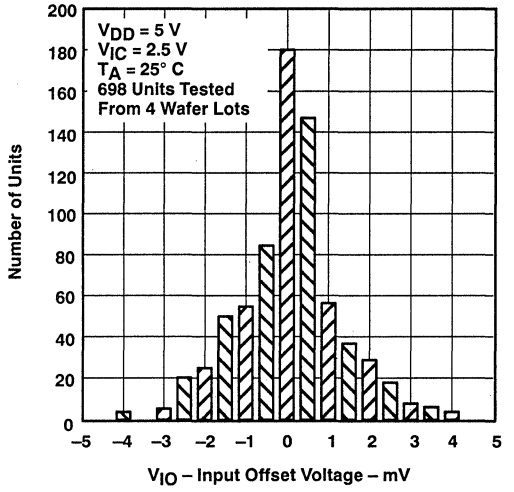


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

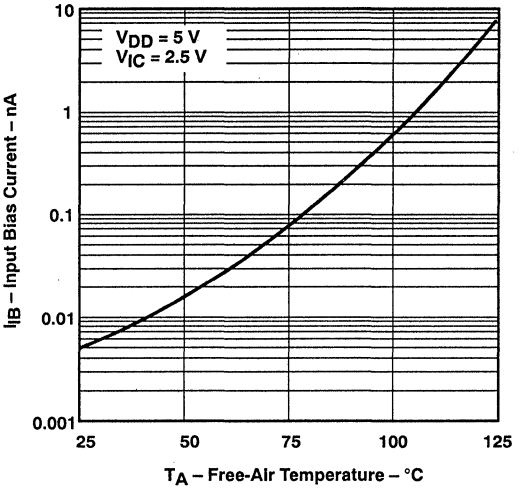


Figure 9

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

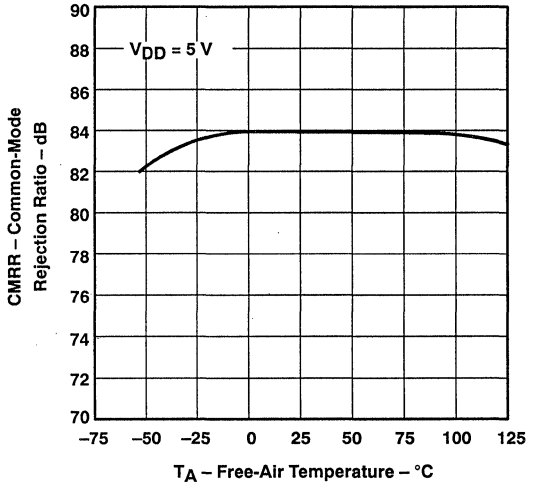


Figure 10

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

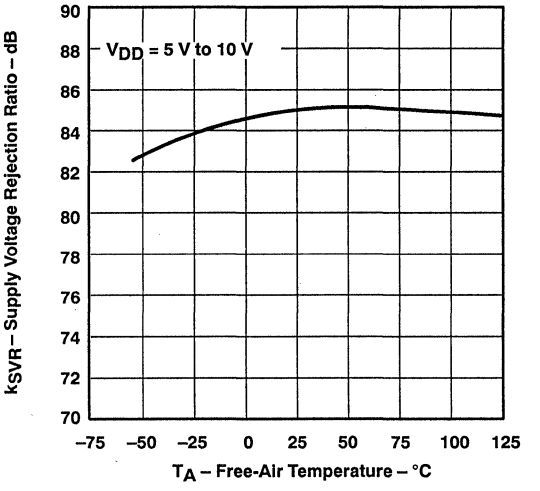


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

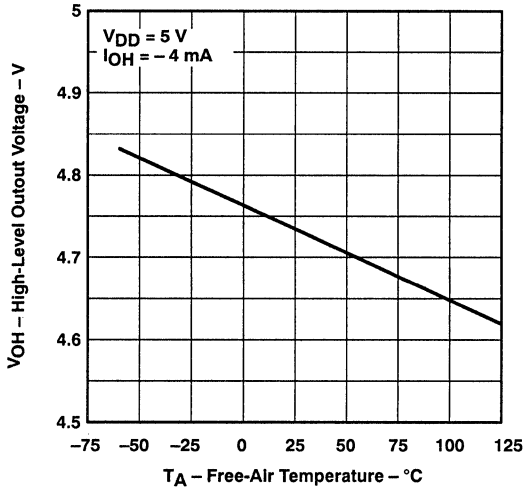


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

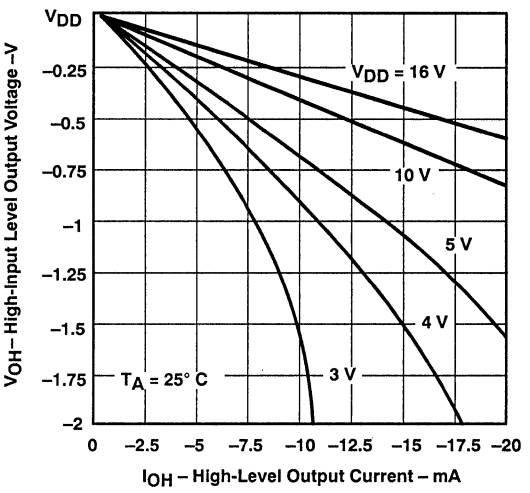


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

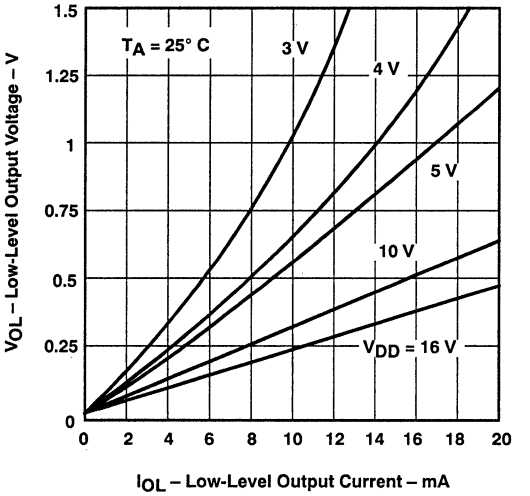


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

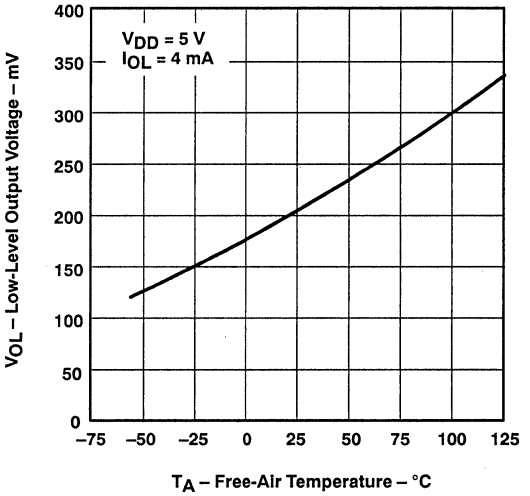


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT TRANSITION TIME
vs
LOAD CAPACITANCE

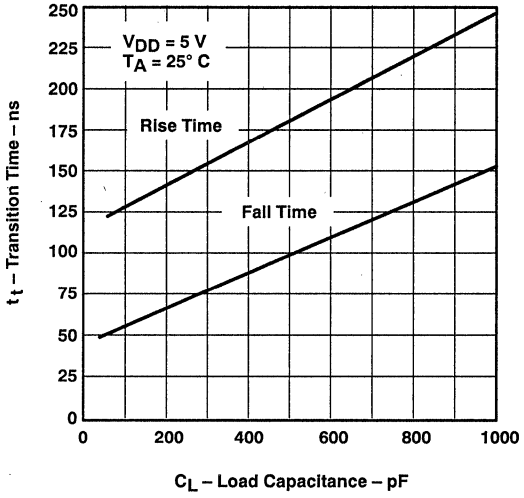


Figure 16

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

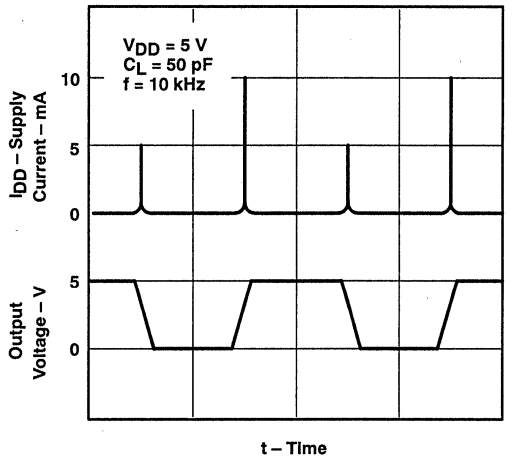


Figure 17

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

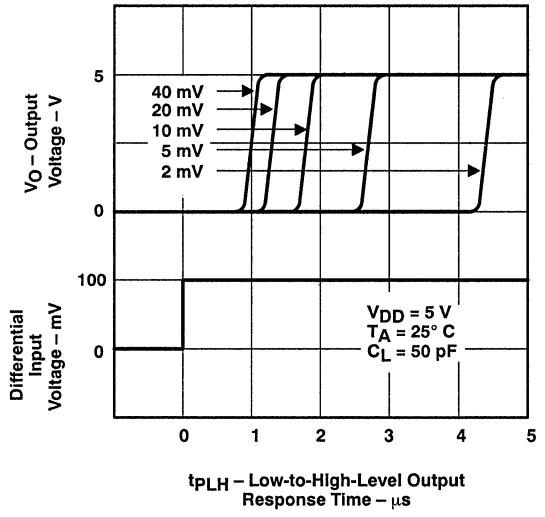


Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

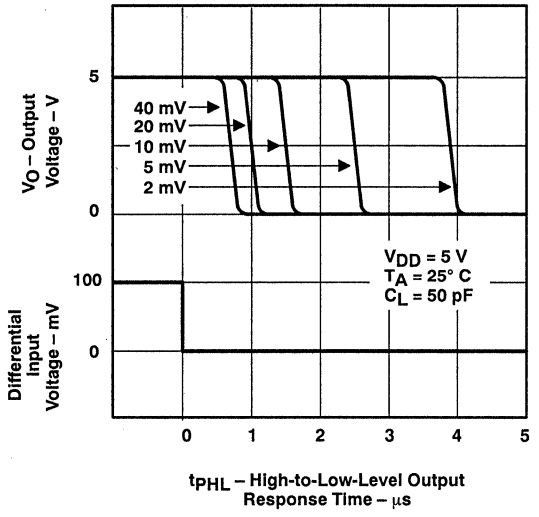


Figure 19

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

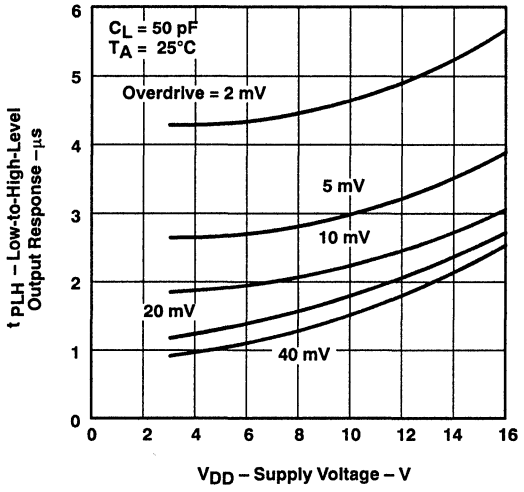


Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

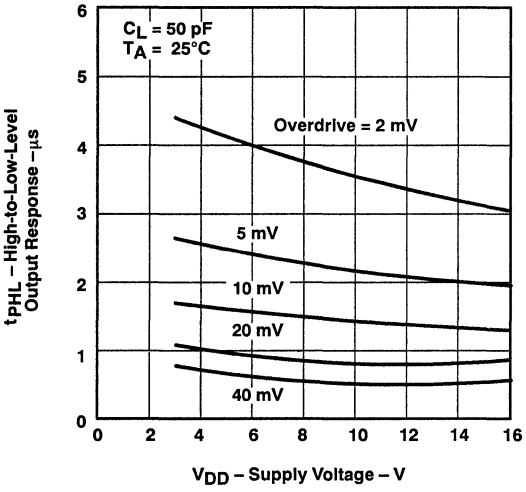


Figure 21

AVERAGE SUPPLY CURRENT
(PER COMPARATOR)
vs
FREQUENCY

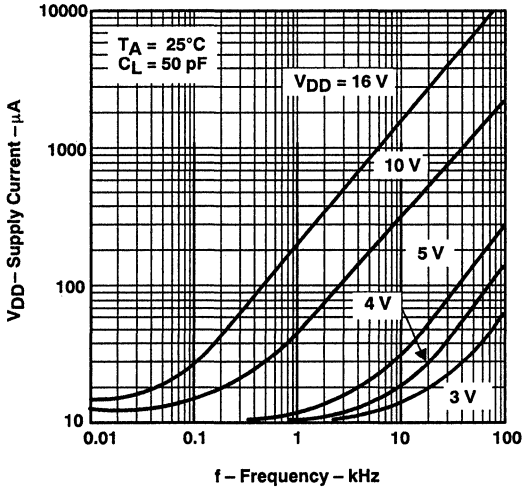


Figure 22

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

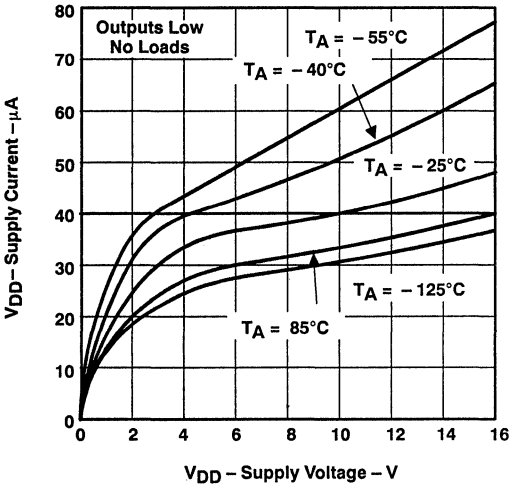


Figure 23

TYPICAL CHARACTERISTICS†

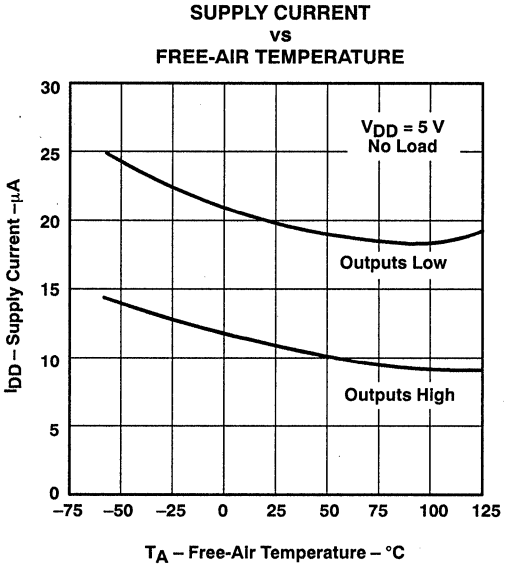


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

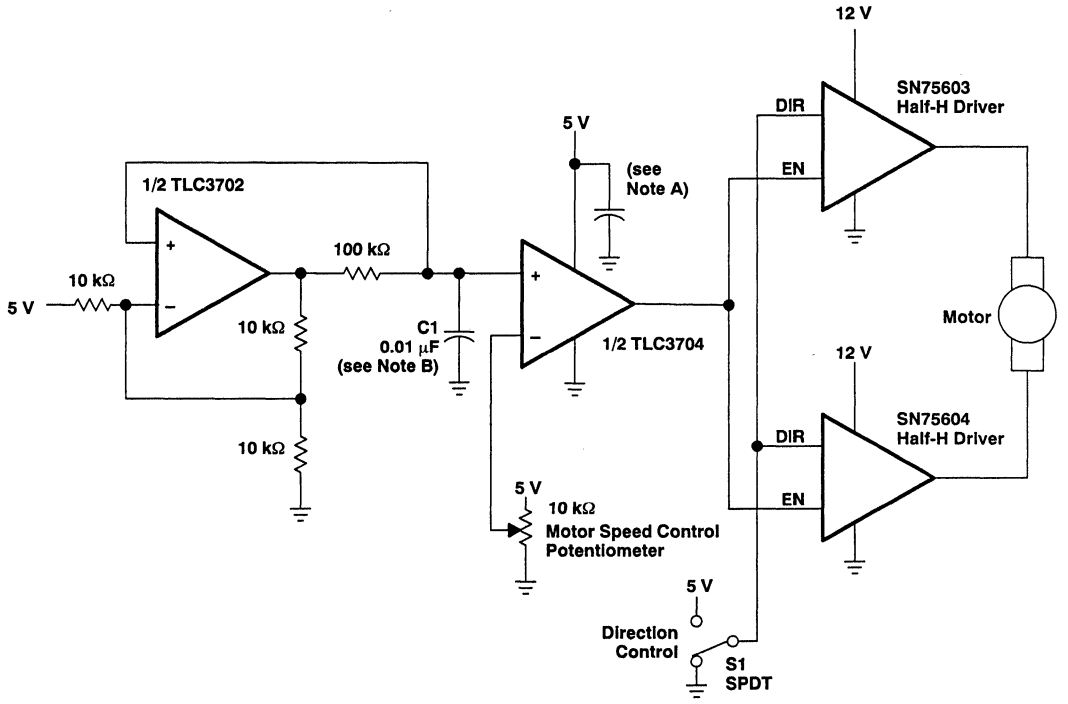
APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

The TLC3702 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

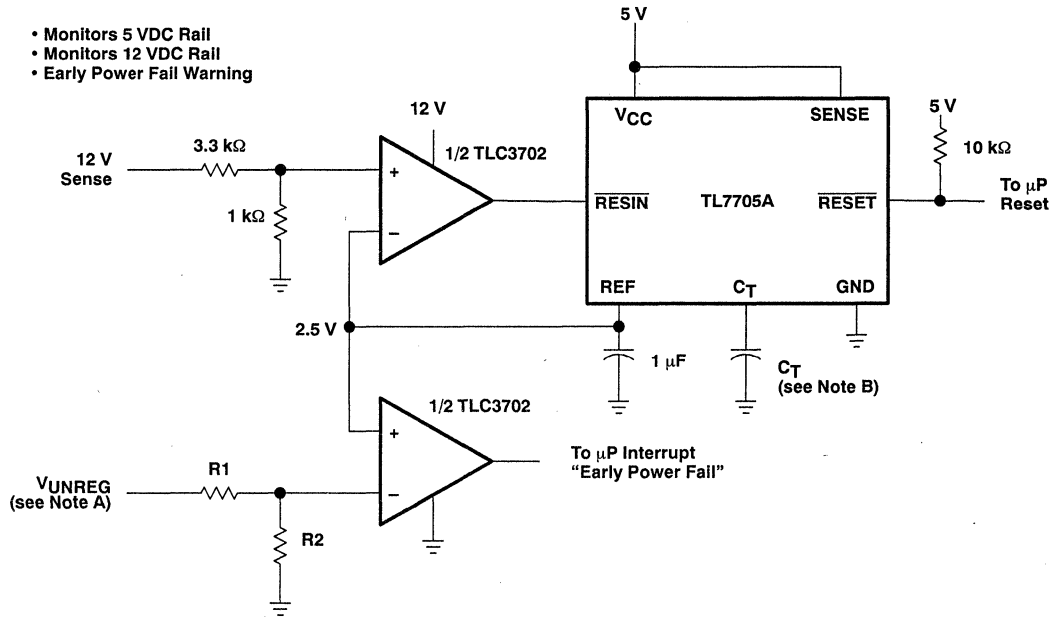
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

Figure 25. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

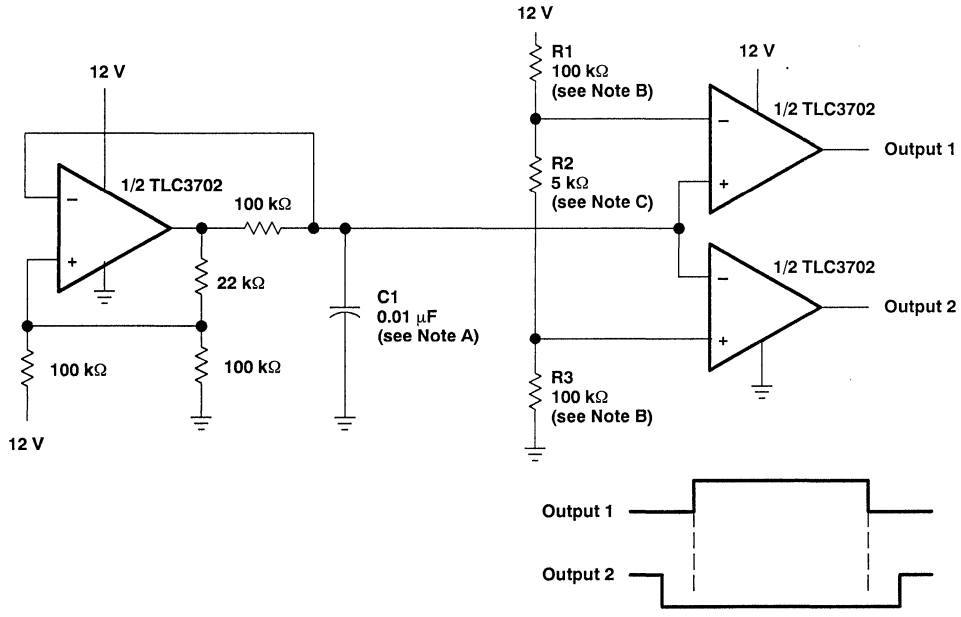


NOTES: A. $V_{UNREG} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor

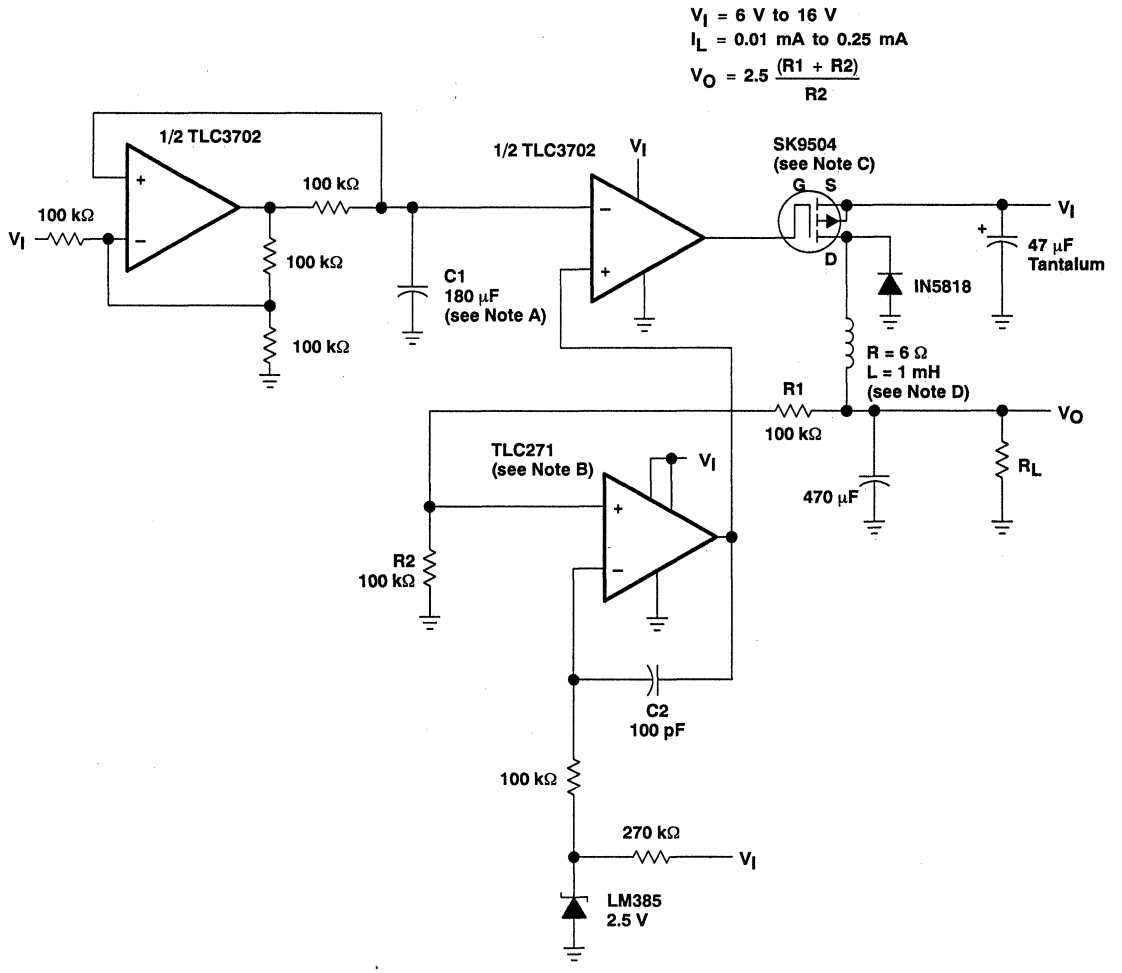
APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator

APPLICATION INFORMATION

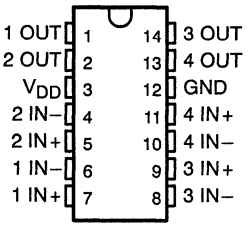


NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

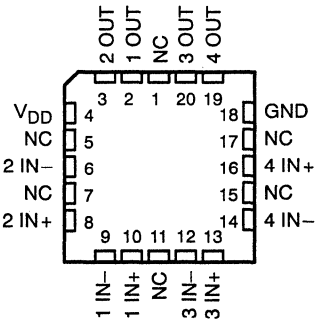
Figure 28. Micropower Switching Regulator

- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, I_O = ± 8 mA**
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single Supply Operation . . . 3 V to 16 V**
  TLC3704M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



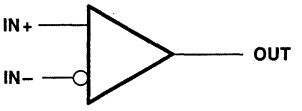
NC — No internal connection

description

The TLC3704 consists of four independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC3704CD	—	—	TLC3704CN
– 40°C to 85°C	5 mV	TLC3704ID	—	—	TLC3704IN
– 55°C to 125°C	5 mV	—	TLC3704MFK	TLC3704MJ	—
– 40°C to 125°C	5 mV	—	—	TLC3704QJ	—

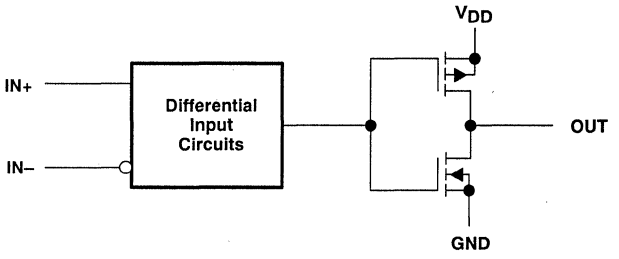
The D package is available taped and reeled. Add "R" suffix to the device type (e.g., TLC3704CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3704I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC3704M is characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC3704Q is characterized for operation from – 40°C to 125°C.

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 18 V
Differential input voltage (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... – 0.3 to V_{DD}
Output voltage range, V_O ..... – 0.3 to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... ± 20 mA
Total supply current into V_{DD} terminal ..... 40 mA
Total current out of ground terminal ..... 60 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC3704C ..... 0 to 70°C
TLC3704I ..... – 40°C to 85°C
TLC3704M ..... – 55°C to 125°C
TLC3704Q ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				70°C			375	
I_{DD}	Supply current (four comparators)	No load,	Outputs low	25°C		35	80	μA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1			V
				−40°C to 85°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				85°C		84		
				−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				85°C			400	
I_{DD}	Supply current (four comparators)	No load,	Outputs low	25°C		35	80	μA
				−40°C to 85°C			125	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		83		
				−55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				−55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (four comparators)	No load,	Outputs low	25°C		35	80	μA
				−55°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3		25°C		1.2	5	mV
				−40°C to 125°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} − 1			V
				−40°C to 125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		83		
				−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = −4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (four comparators)	No load,	Outputs low	25°C		35	80	μA
				−40°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4-V step at IN + pin			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4-V step at IN + pin			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs will cause degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. If you have any further questions, please contact your local TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages will tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

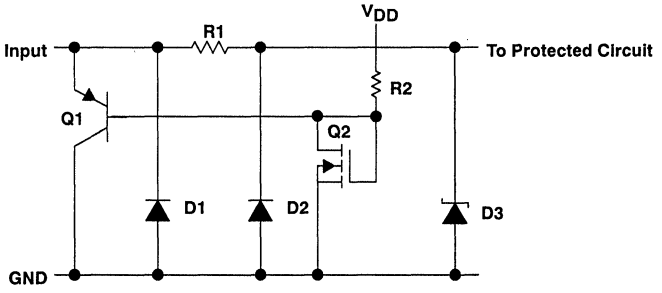


Figure 1. LinCMOS™ ESD-Protection Schematic

LinCMOS and Advanced LinCMOS are trademarks of Texas Instruments Incorporated.

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 will force the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 2 and 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it will saturate and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current will be directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

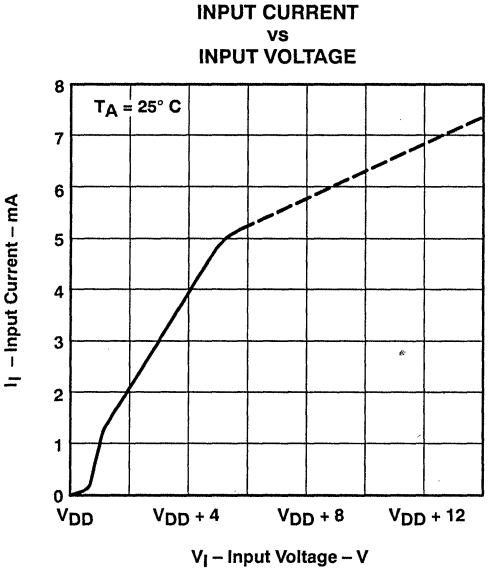


Figure 2

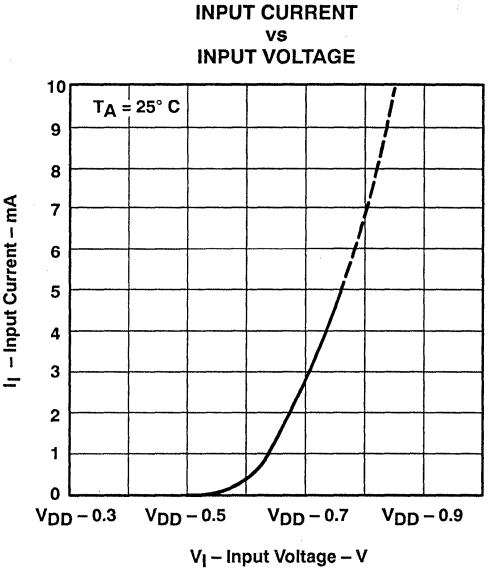
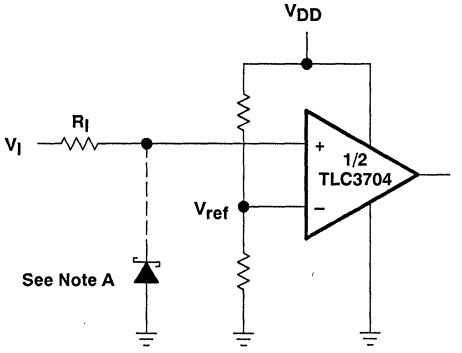


Figure 3



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

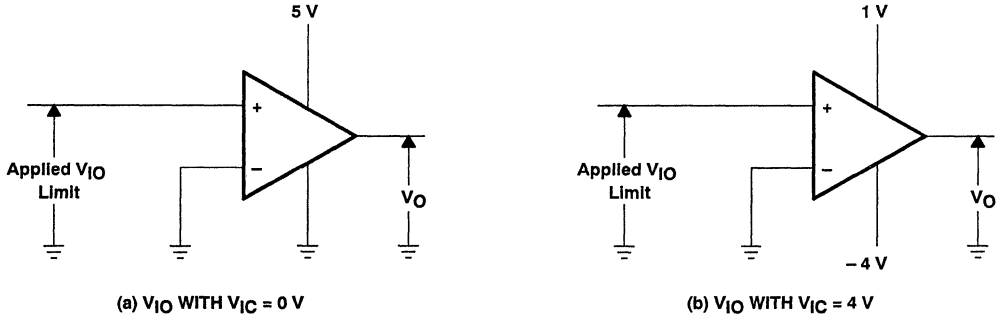
Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V (b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASURMENT INFORMATION

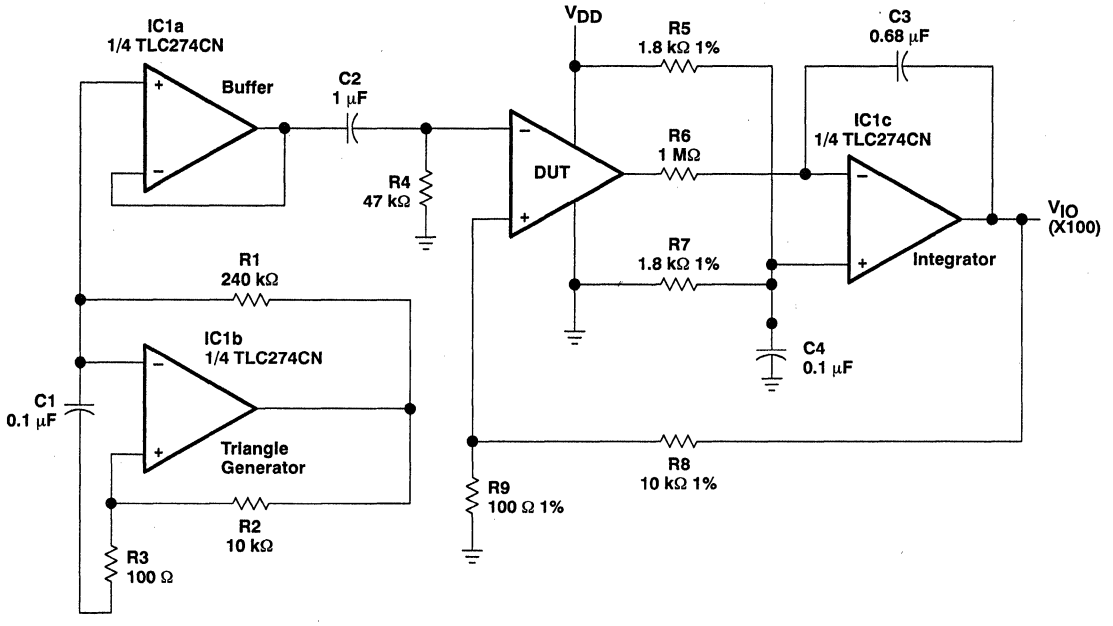
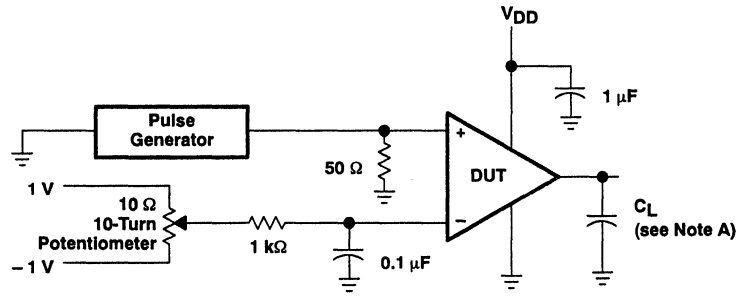


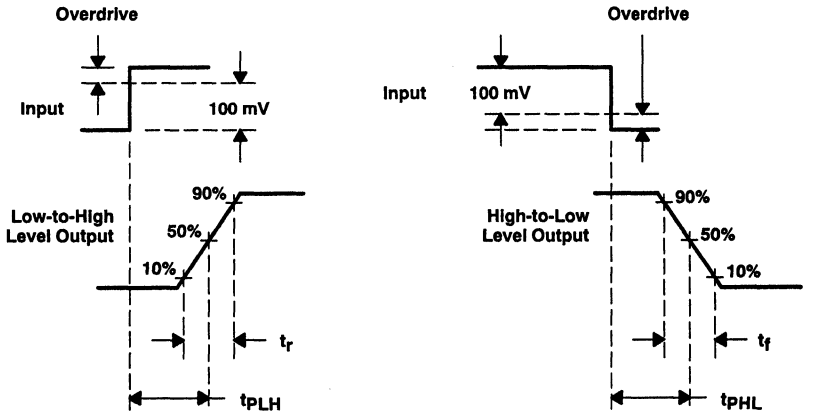
Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 7) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.

PARAMETER MEASURMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

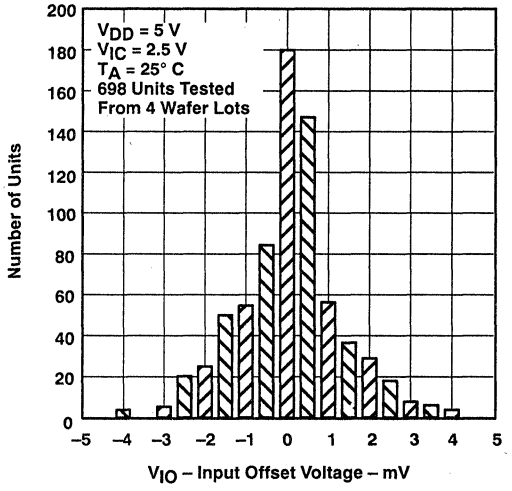


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

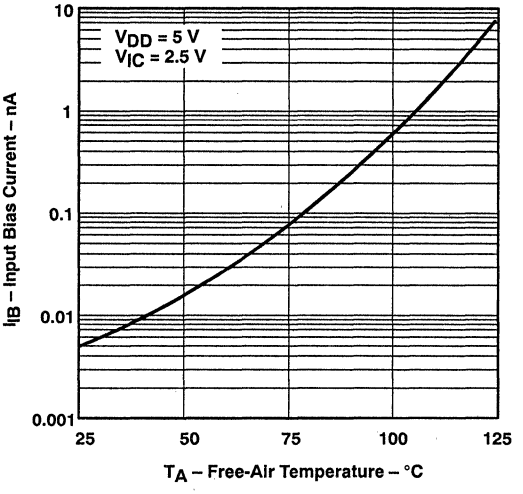


Figure 9

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

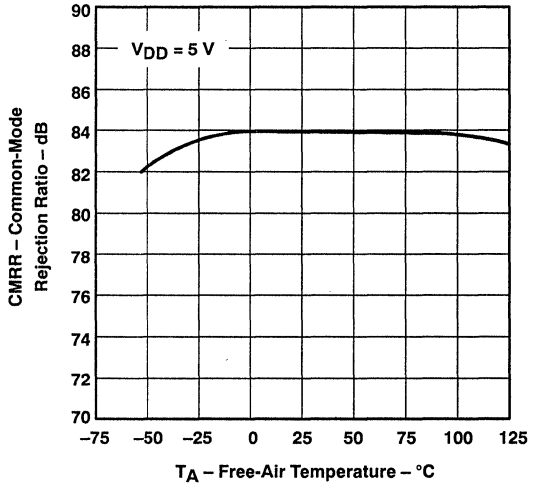


Figure 10

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

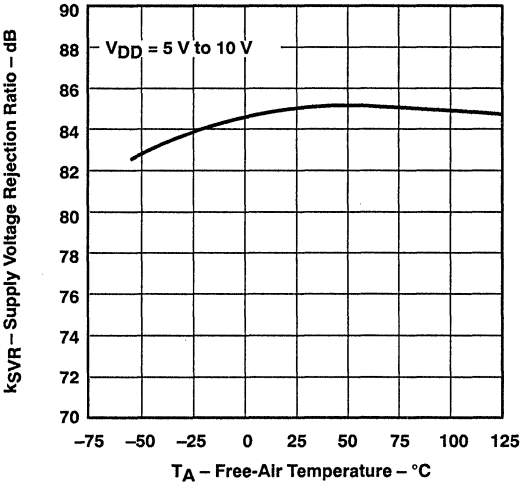


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

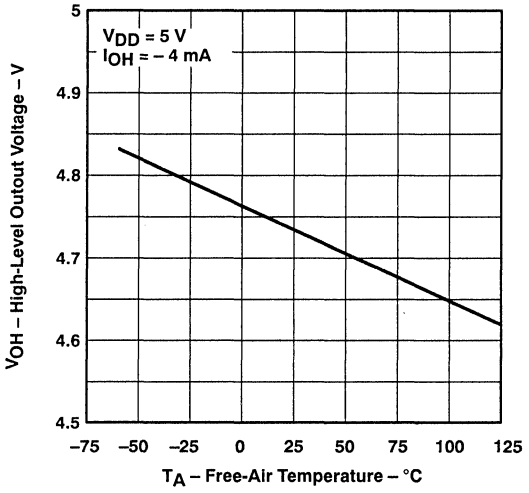


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

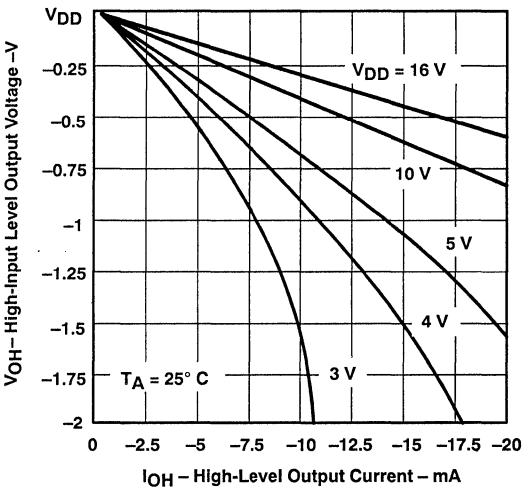


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

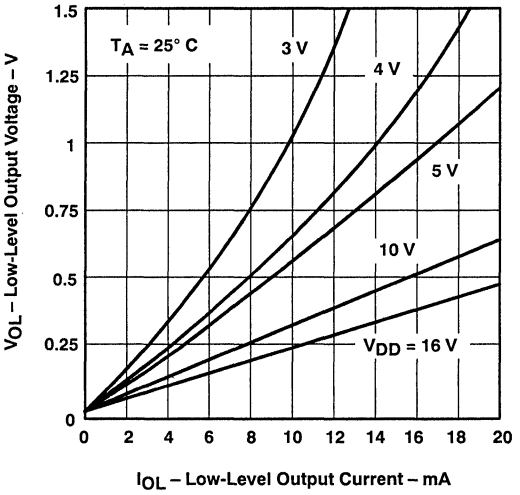


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

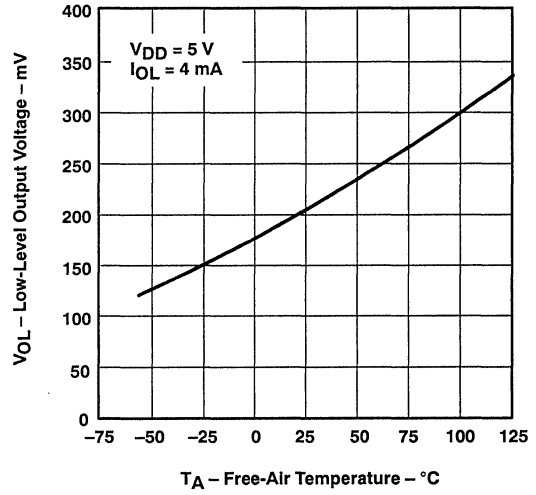


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT TRANSITION TIME
vs
LOAD CAPACITANCE

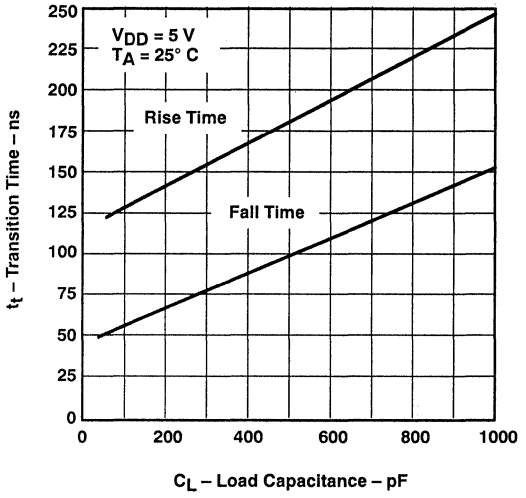


Figure 16

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

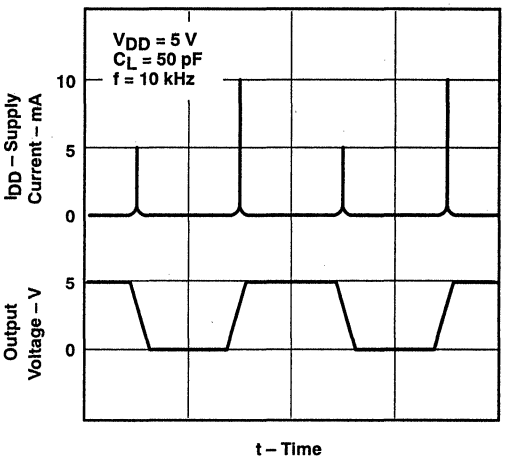


Figure 17

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

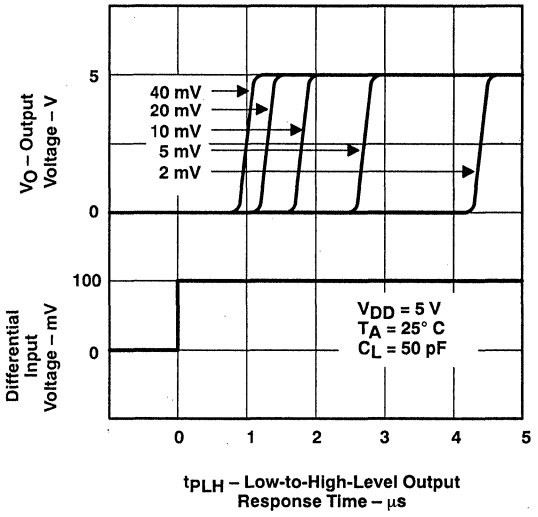


Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

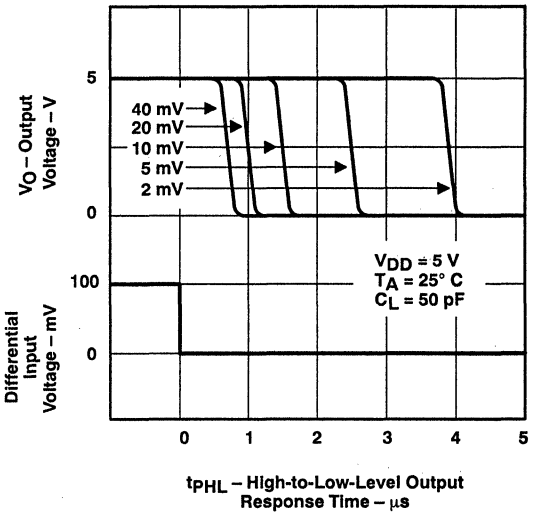


Figure 19

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

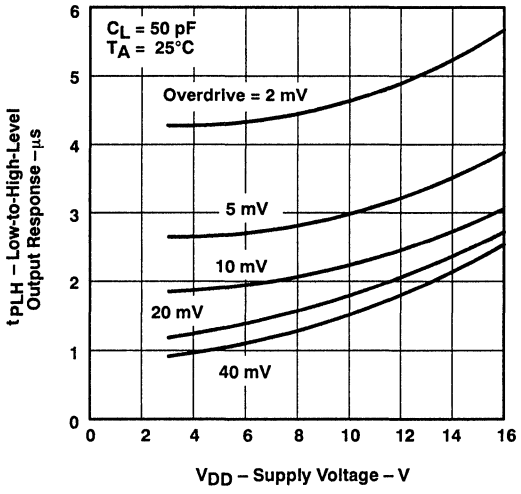


Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

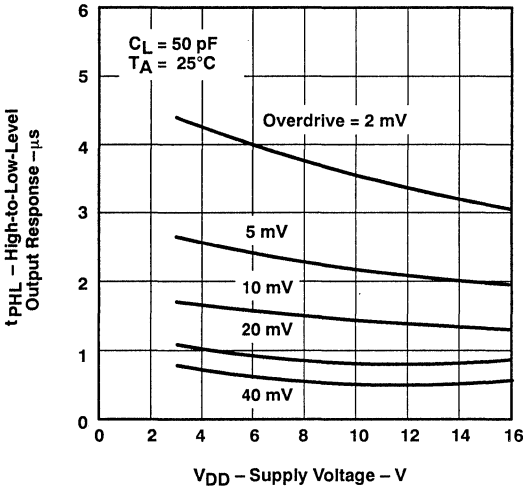


Figure 21

AVERAGE SUPPLY CURRENT
(PER COMPARATOR)
vs
FREQUENCY

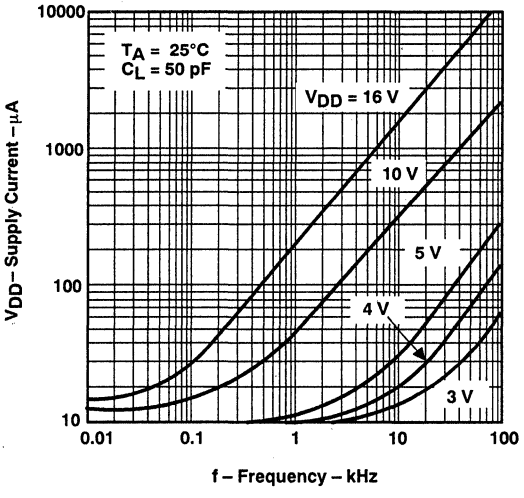


Figure 22

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

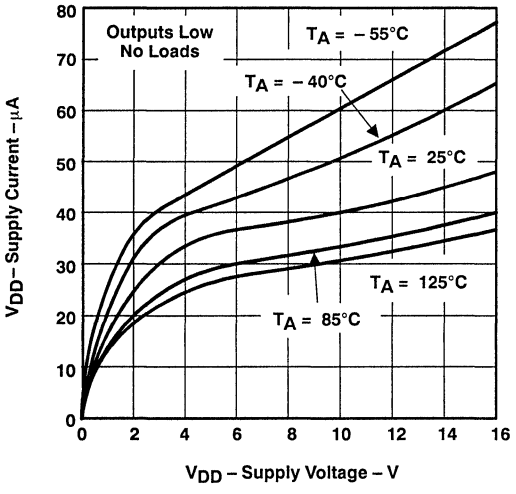


Figure 23

TYPICAL CHARACTERISTICS†

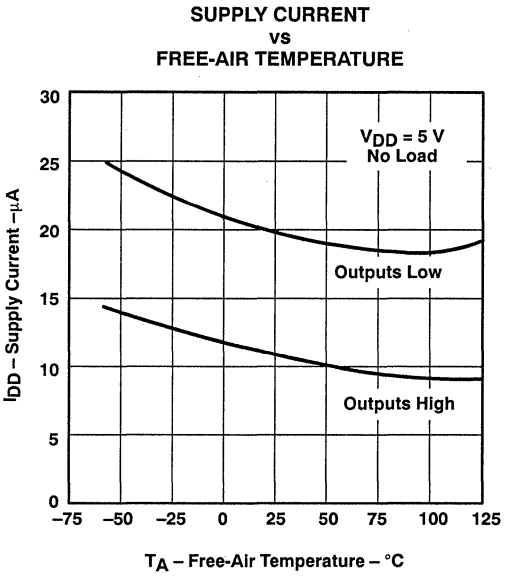


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

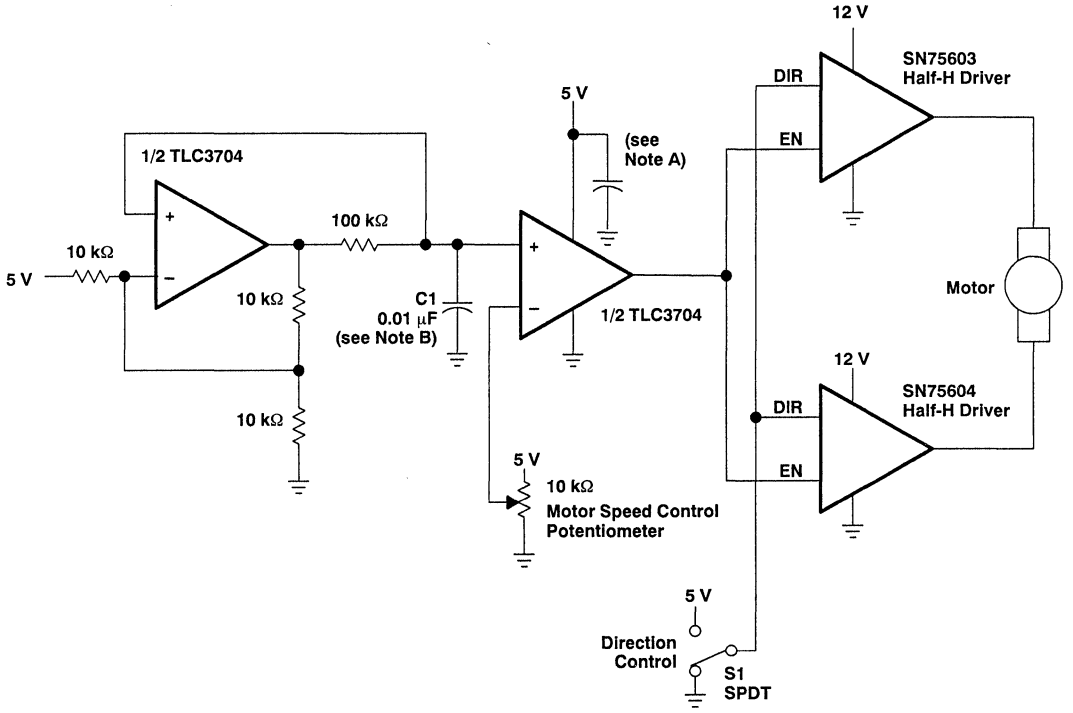
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC3704 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

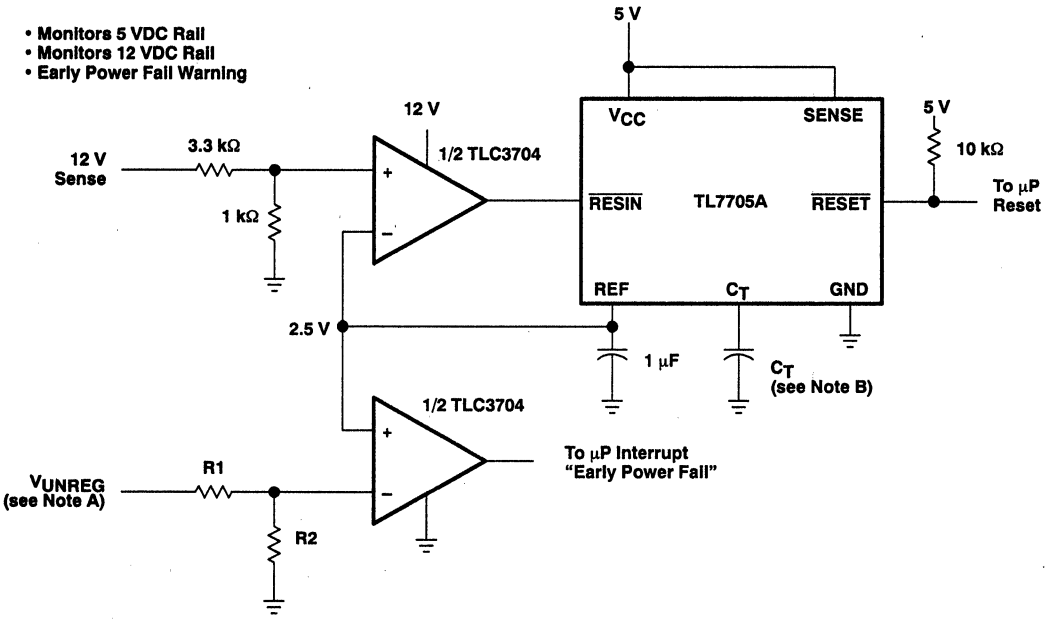
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency

Figure 25. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

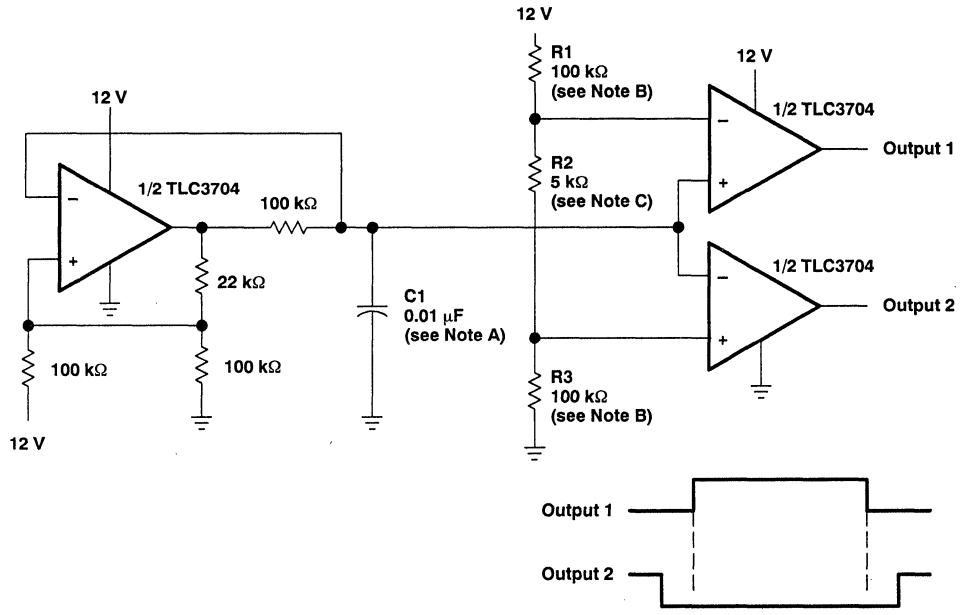


NOTES: A. $V_{UNREG} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor

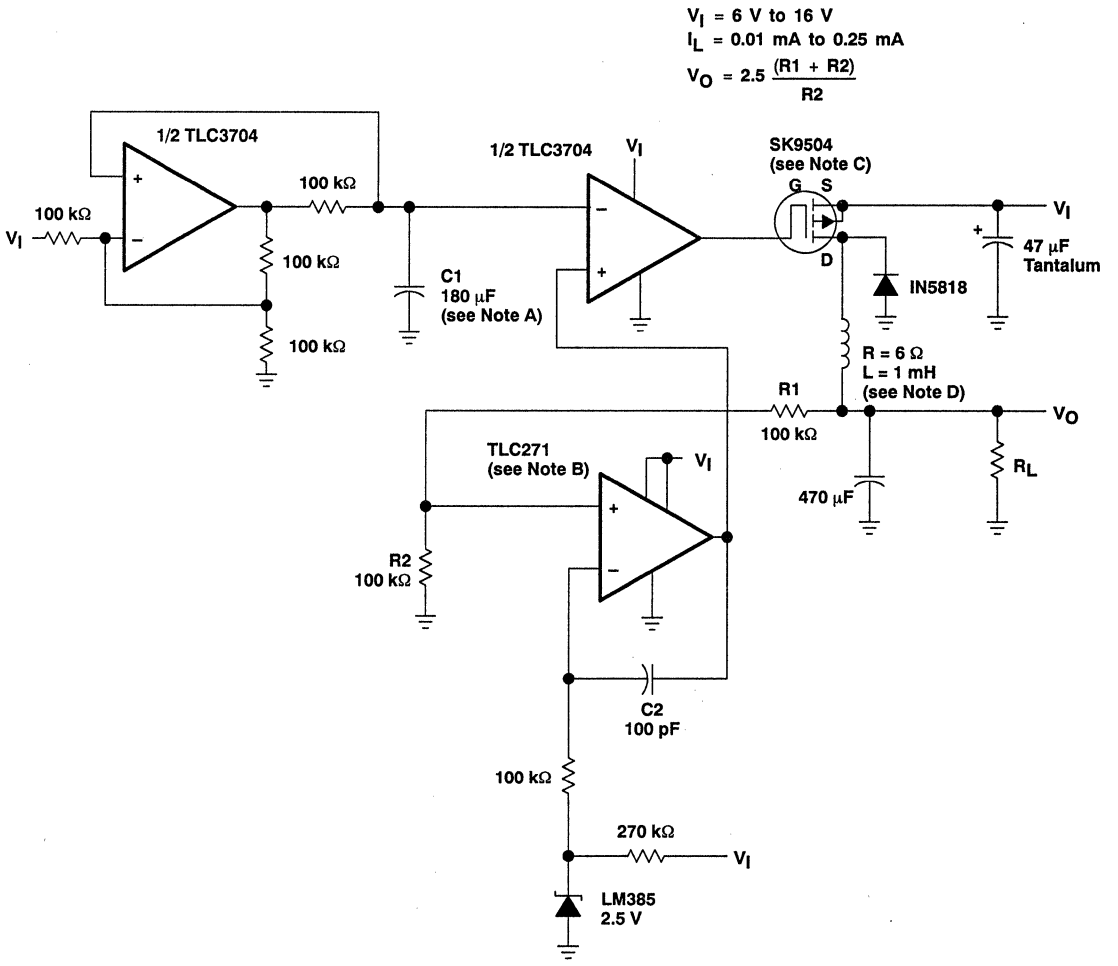
APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\ k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator

APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator

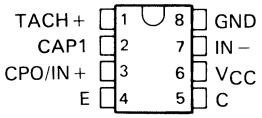
General Information 1
VRegs/Supervisors and Bldg Blocks 2
Comparators 3
Special Functions 4
Thermal Design Considerations 5
Mechanical Data 6

4 Special Functions

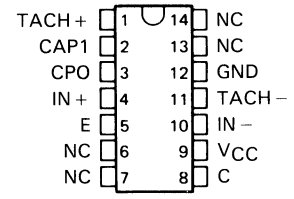
D3003, MARCH 1986—REVISED OCTOBER 1988

- **Output Swings to Ground for Zero-Frequency Input**
- **Only One RC Network Provides Frequency Doubling for Low Ripple**
- **8-Pin Versions Interface Directly to Variable-Reluctance Magnetic Pickups**
- **Uncommitted Collector and Emitter Outputs Provide 40-mA Sink or Source Current to Operate Relays, Solenoids, Meters, or LEDs**
- **Built-In Hysteresis for Noise Immunity**
- **Linearity Typically ±0.3%**
- **8-Pin Versions are Fully Protected from Damage Due to TACH Input Swing Above V_{CC} and Below Ground**

LM2907, LM2917 . . . D OR P PACKAGE
(TOP VIEW)



LM2907, LM2917 . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

applications

Over/under speed sensing
Frequency-to-voltage conversion
Speedometers
Breaker-point dwell meters
Hand-held tachometers
Speed governors
Cruise control
Automotive door-lock control
Clutch control
Horn control
Touch or sound switches

description

The LM2907 and LM2917 are monolithic frequency-to-voltage converters with an output circuit designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The converter (tachometer) section consists of a comparator driving a charge pump and offers frequency doubling for low ripple, full input protection in 8-pin versions, and an output swing to ground for a zero-frequency input. The output section consists of an operational amplifier, normally operating as a comparator, that drives an output transistor with both the collector and emitter floating. The circuit can either sink or source 40 mA of load current.

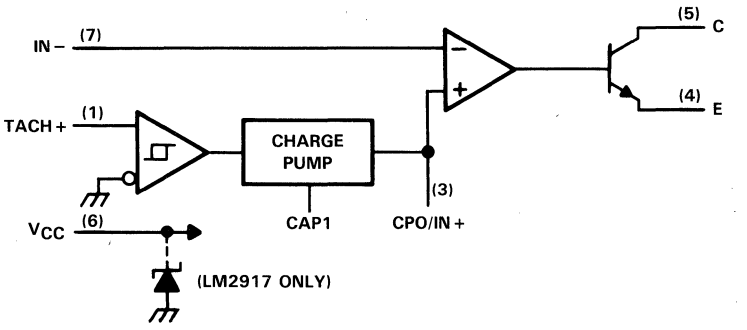
Two basic configurations of the devices are offered; an 8-pin version and a 14-pin version. The 8-pin versions have a ground-referenced tachometer input and an internal connection between the tachometer output and the operational amplifier input. The 8-pin version is well suited to single-speed or single-frequency switching or fully buffered frequency-to-voltage conversion applications. The more versatile 14-pin versions provide differential tachometer inputs and uncommitted operational amplifier inputs. In the 14-pin versions, the tachometer input can be floated and the operational amplifier becomes suitable for active filter conditioning of the tachometer output.

The LM2917 has an active shunt regulator connected across the power leads. The regulator clamps the supply voltage so that stable frequency-to-voltage and frequency-to-current conversions are possible with any supply voltage and a suitable resistor.

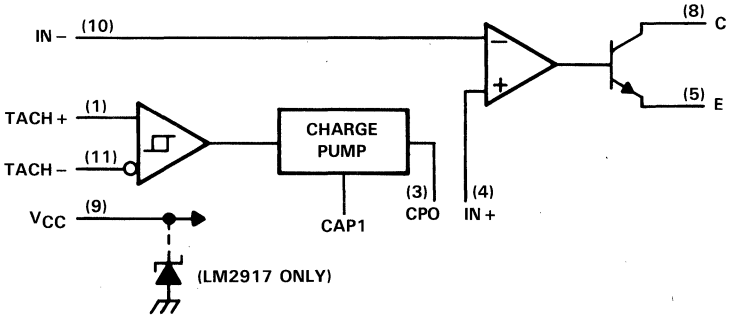
The LM2907 and LM2917 are designed for operation from −40°C to 85°C.

functional block diagrams

8-PIN VERSIONS



14-PIN VERSIONS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}: LM2907 . . . . . 28 V
Supply current, I_{CC}: LM2917 . . . . . 25 mA
Collector-to-emitter voltage . . . . . 28 V
Operational amplifier input voltage, IN+ and IN– . . . . . 0 V to V_{CC}
Tachometer input voltage: 8-pin version TACH+ . . . . . 0 V to 28 V
14-pin version TACH+ and TACH– . . . . . 0 V to V_{CC}
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperture range 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D (8 pins)	725 mW	5.8 mW/°C	377 mW
D (14 pins)	900 mW	7.2 mW/°C	468 mW
N	1000 mW	7.7 mW/°C	500 mW
P	900 mW	7.2 mW/°C	468 mW

electrical characteristics, V_{CC} = 12 V (LM2907), V+ = 12 V through 470 Ω (LM2917), T_A = 25°C

converter (tachometer) section

PARAMETER			TEST CONDITIONS	LM2907			LM2917			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_I = 250 mV, f = 1 kHz	±10	±15	±40	±10	±15	±40	mV
V_{hys}	Input hysteresis (see Note 1)		V_I = 250 mV, f = 1 kHz		30			30		mV
V_{IO}	Input offset voltage (see Note 1)	8-pin versions	V_I = 250 mV, f = 1 kHz		5	15		5	15	mV
		14-pin versions	V_{ID} = 250 mV, f = 1 kHz		3.5	10		3.5	10	
I_{IB}	Input bias current		V_I = ±50 mV		0.1	1		0.1	1	μA
V_{OH}	High-level output voltage, CAP1		V_I or V_{ID} = 125 mV		8.3			5.0		V
V_{OL}	Low-level output voltage, CAP1		V_I or V_{ID} = −125 mV		2.3			1.2		V
I_O	Output current, CAP1, CPO		CAP1 and CPO at 6 V	140	180	240				μA
			CAP1 and CPO at 3.8 V				140	180	240	
	Leakage current, CPO		CAP1 open, CPO at 0 V, See Note 3			0.1			0.1	μA
	Gain constant			0.9	1	1.1	0.9	1	1.1	
	Nonlinearity (see Note 2)		f = 1 kHz, 5 kHz, or 10 kHz		0.3	±1		0.3	±1	%

output section

PARAMETER		TEST CONDITIONS	LM2907			LM2917			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_I = 6 V, See Note 3		3	10				mV
		V_I = 3.8 V, See Note 3					3	10	
I_{IB}	Bias current	V_I = 6 V		50	500				nA
		V_I = 3.8 V					50	500	
A_V	Voltage amplification			200			200		V/mV
I_C	Collector output (sink) current	V_C = 1 V, V_E = 0	40	50		40	50		mA
I_E	Emitter output (source) current	V_C = V_{CC}, V_E = V_{CC} − 2		−10			−10		mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 5 mA		0.1	0.5		0.1	0.5	V
		I_C = 20 mA			1			1	
		I_C = 50 mA		1	1.5		1	1.5	

NOTES: 1. Hysteresis is the algebraic difference $V_{T+} - V_{T-}$; offset voltage is the difference in magnitudes $|V_{T+}| - |V_{T-}|$. See parameter measurement information test circuits.
2. Nonlinearity is defined as the deviation of V_O at CPO for f = 5 kHz from a straight line defined by the V_O at 1 kHz and V_O at 10 kHz, with C1 = 1000 pF, R1 = 68 kΩ, C2 = 0.22 μF.
3. Pin 2 must be bypassed with a 0.001-μF capacitor to prevent oscillation for these tests.

electrical characteristics

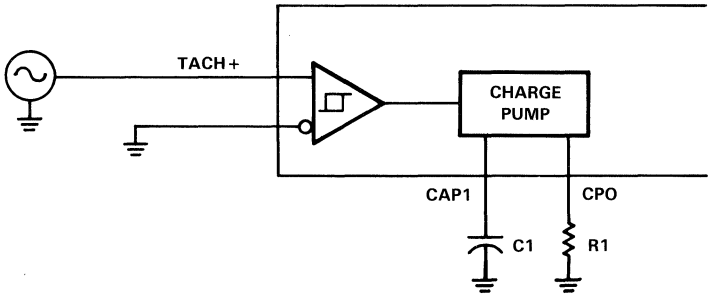
zener regulator (LM2917 only) V+ = 12 V through 470 Ω, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Regulated supply voltage		7.56		V
r_s	Series resistance		10.5	15	Ω
αV_{CC}	Temperature coefficient of regulated supply voltage		1		mV/°C

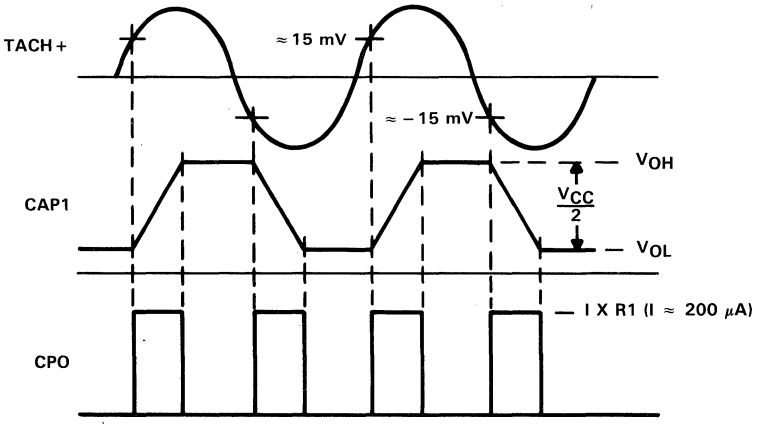
total device (LM2907 only) V_{CC} = 12 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current		3.8	6	mA

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

FIGURE 1. TEST CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION DATA

The LM2907 and LM2917 frequency-to-voltage converter circuits are designed for maximum versatility with a minimum of external parts. The first stage of these devices is a differential comparator. The single-input 8-pin versions have one input grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This version is specifically for magnetic variable-reluctance pickups, which typically provide a single-ended ac output. These single-ended inputs are fully protected against voltage swings to ±28 V, which are easily attained by these types of pickups.

The differential-input 14-pin versions provide the option of setting the input reference level and still having hysteresis around that level to provide excellent noise rejection in any application. The input protection is removed in the 14-pin versions. Therefore, neither of the differential inputs should exceed the limits of the supply voltage. An input must not go below ground without a resistance in the lead to limit the current that will flow in the epi-substrate diode. The charge pump circuit that follows the input stage produces a dc output voltage proportional to the input frequency. The charge pump circuit (see Figure 2) consists of a timing capacitor (C1), an output resistor (R1), and an integrating or filter capacitor (C2). When the input changes state (due to a suitable zero crossing or differential voltage on the input), the timing capacitor is either charged or discharged linearly with a constant current of 200 μA through CAP1 between two voltages whose difference is $V_{CC}/2$. Within one-half cycle of the input frequency or a time equal to 1/2f, the change in charge on C1 is equal to (VCC/2)C1. The average amount of current pumped into or out of the capacitor is:

$$\text{CAP1 current (average)} = \frac{Q}{T} = C1 \cdot \frac{V_{CC}}{2} \cdot 2f = V_{CC} \cdot f \cdot C1$$

The output of the charge pump accurately mirrors the CAP1 current into the load resistor (R1) connected to CPO. If the pulses of current are integrated with a filter capacitor, the output voltage is the average CAP1 current times R1, and the total equation becomes:

$$V_O = V_{CC} \cdot f \cdot C1 \cdot R1 \cdot K$$

where K is the gain factor, which is typically 1.

The size of C2 is dependent only on the amount of ripple allowable and the required response time.

selection of R1, C1, and C2

To achieve optimum performance, there are some limitations to be considered in the selection of R1 and C1. The timing capacitor controls the RC time and provides internal compensation for the charge pump circuit. For very accurate operation it should be 100 pF or greater. Smaller values, especially at lower temperatures, can cause an error current through R1. $V_O/R1$ must be less than or equal to the output current at CPO, which is fixed typically at 180 μA. If R1 is too large it becomes a significant fraction of the output impedance at CPO, which degrades the linearity. In addition, ripple voltage must be considered when selecting R1. The size of C2 is directly affected by the size of R1. An expression that describes the ripple content at CPO is:

$$V_{ripple} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \cdot \left(1 - V_{CC} \cdot f \cdot \frac{C1}{200}\right) \quad \text{volts peak-to-peak}$$

where

C1 and C2 are in farads
V_{CC} is in volts
f is in hertz.

TYPICAL APPLICATION DATA

R1 cannot be chosen independently of ripple because response time or the time it takes V_O to stabilize at a new level increases as the size of C2 increases. A compromise between ripple, response time, and linearity must be chosen carefully. As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1, and I_{cap} (current through CAP1).

$$f_{max} = \frac{I_{cap}}{C1 \cdot V_{CC}} \quad \text{hertz}$$

where

I_{cap} is typically 200 μA
C1 is in farads
V_{CC} is in volts.

zener regulator options (LM2917)

For those applications in which an output voltage or current must be obtained independently of supply voltage variations, the LM2917 can be used. The most important factor in selecting a dropping resistor for the unregulated supply is that the frequency-to-voltage converter circuit and the operational amplifier alone require approximately 3 mA at the voltage level set by the zener diode. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the supply voltage varies between 9 and 16 V, a resistance of 470 Ω will minimize the zener voltage variation to typically 160 mV. If the resistance goes under 400 Ω or above 600 Ω, the zener variation quickly rises above 200 mV for the same input variation.

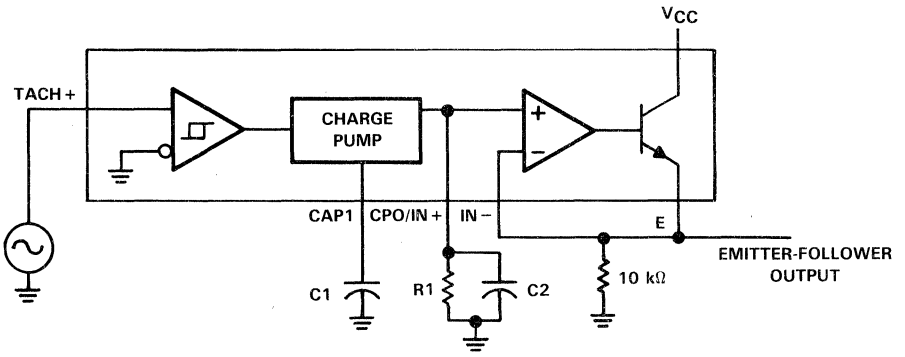
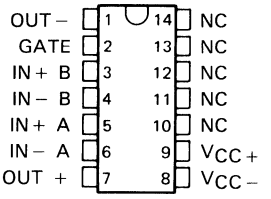


FIGURE 2. MINIMUM-COMPONENT TACHOMETER

D2572, JANUARY 1980—REVISED APRIL 1988

- **Differential Inputs and Outputs**
- **Channel Select Time . . . 20 ns Typ**
- **Bandwidth Typically 50 MHz**
- **16-dB Minimum Gain**
- **Common-Mode Rejection Typically 85 dB**
- **Broadband Noise Typically 25 μV**

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

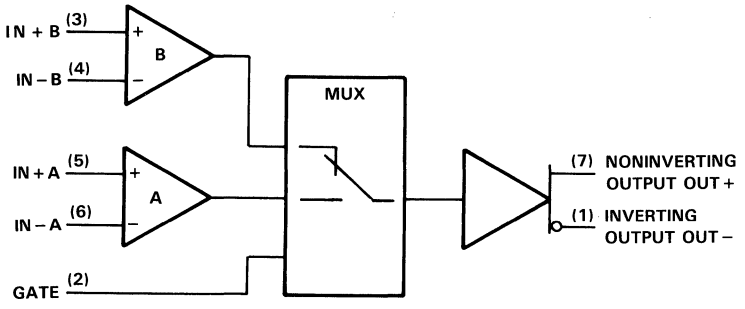
The MC1445 is a general-purpose, gated, dual-channel wideband amplifier designed for use in video-signal mixing and switching. Channel selection is accomplished by control of the voltage level at the gate. A high logic level selects channel A; a low logic level selects channel B. The unselected channel will have a gain of one or less.

The MC1445 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

GATE INPUT	SELECT
H	Channel A
L	Channel B

block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 12 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Output current, I_O . . . . . ±25 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values, except differential input voltage, are with respect to the midpoint of V_{CC+} and V_{CC-}.
2. Differential input voltages are measured at a noninverting input terminal with respect to the appropriate inverting input terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 75°C$ POWER RATING
J	626 mW	8.2 mW/°C	74°C	615 mW
N	625 mW	N/A	N/A	625 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		5	8	V
Supply voltage, V_{CC-}		−5	−8	V
Operating free-air temperature range, T_A	0		75	°C

electrical characteristics at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

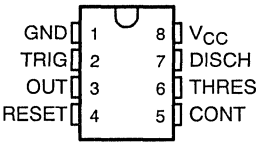
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{VS}	Large-signal single-ended voltage amplification	f = 125 kHz,	V_i = 20 mV	16	19.5	23	dB
BW	Bandwidth	V_i = 20 mV			50		MHz
V_{IO}	Input offset voltage					7.5	mV
I_{IO}	Input offset current				2		μA
I_{IB}	Input bias current				15	30	μA
V_{ICR}	Common-mode voltage range				±2.5		V
V_{OQ}	Quiescent output voltage				0.1		V
ΔV_{OQ}	Change in quiescent output voltage	Gate input change from 5 V to 0 V			±15		mV
V_{OPP}	Maximum peak-to-peak output voltage swing	f = 125 kHz,	R_L = 1 kΩ	1.5	2.5		V
z_i	Input impedance	f = 125 kHz		3	10		kΩ
z_o	Output impedance	f = 50 kHz			25		Ω
CMRR	Common-mode rejection ratio	f = 50 kHz			85		dB
V_n	Broadband equivalent input noise voltage	BW = 5 Hz to 10 MHz, R_S = 50 Ω			25		μV
V_{TH}	High-level gate threshold voltage	$A_{VS(A)} \geq$ 16 dB,	$A_{VS(B)} \leq$ 0 dB		1.3	3	V
V_{TL}	Low-level gate threshold voltage	$A_{VS(B)} \geq$ 16 dB,	$A_{VS(A)} \leq$ 0 dB	0.2	0.4		V
I_{IH}	High-level gate current	V_I = 5 V				4	μA
I_{IL}	Low-level gate current	V_I = 0				4	mA
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_I = 20 mV,	50% to 50%		6.5		ns
t_{PHL}	Propagation delay time, high-to-low-level output	ΔV_I = 20 mV,	50% to 50%		6.3		ns
t_{TLH}	Transition time, low-to-high-level output	ΔV_I = 20 mV,	10% to 90%		6.5		ns
t_{THL}	Transition time, high-to-low-level output	ΔV_I = 20 mV,	10% to 90%		7		ns
I_{CC+}	Supply current from V_{CC+}	No load,	No signal		7	15	mA
I_{CC-}	Supply current from V_{CC-}	No load,	No signal		−7	−15	mA
P_D	Power dissipation	No load,	No signal		70	150	mW

D1669, SEPTEMBER 1973—REVISED FEBRUARY 1992

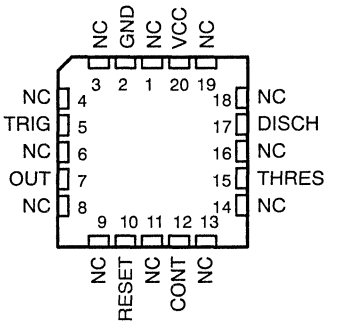
- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source up to 200 mA**
- **Functionally Interchangeable With the Signetics NE555, SA555, SE555, SE555C; Have Same Pinout**

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

These devices are precision monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. RESET can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between DISCH and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The NE555 is characterized for operation from 0°C to 70°C. The SA555 is characterized for operation from −40°C to 85°C. The SE555 and SE555C are characterized for operation over the full military range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE					CHIP FORM (Y)
	V_{THRES} max V_{CC} = 15 V	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)	
0°C to 70°C	11.2 V	NE555D			NE555P	NE555Y
−40°C to 85°C	11.2 V	SA555D			SA555P	
−55°C to 125°C	10.6 V	SE555D	SE555FK	SE555JG	SE555P	
	11.2 V	SE555CD	SE555CFK	SE555CJG	SE555CP	

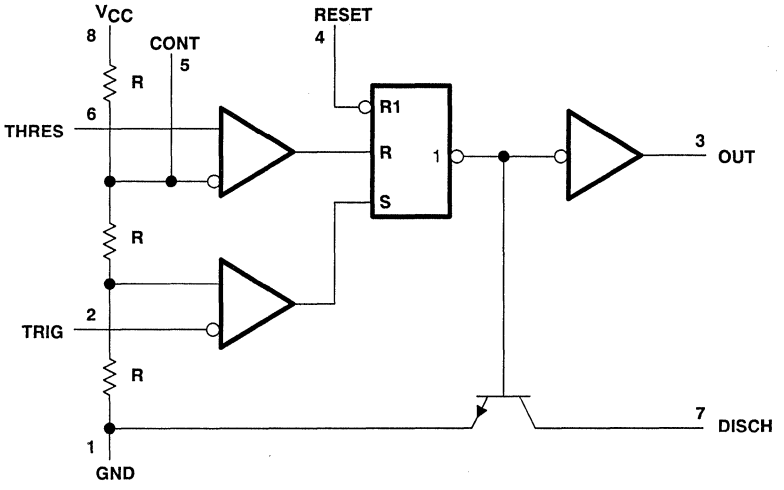
The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

† Voltage levels shown are nominal.

functional block diagram

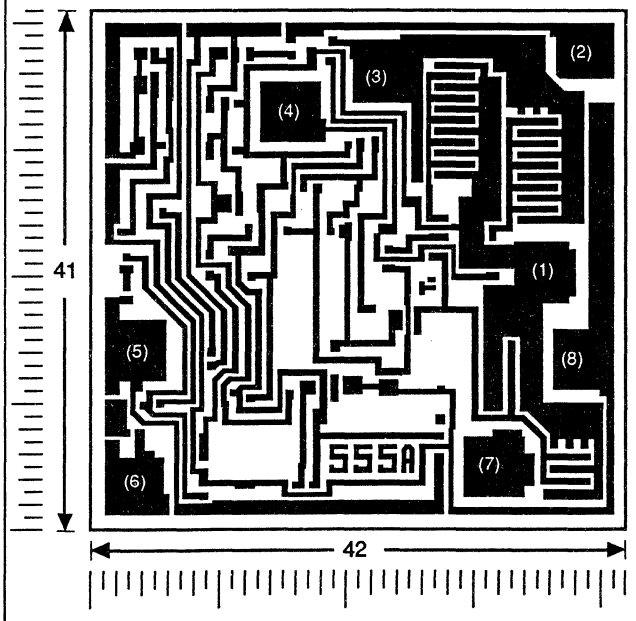


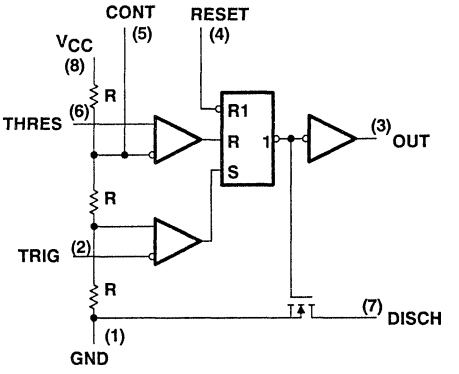
RESET can override TRIG, which can override THRES.
Pin numbers shown are for the D, JG, and P packages only.

chip information

These chips, properly assembled, display characteristics similar to the NE555 (see electrical table for NE555Y). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150° C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (1) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) ..... 18 V
Input voltage (CONT, RESET, THRES, and TRIG) ..... V_{CC}
Output current ..... ±225 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: NE555 ..... 0°C to 70°C
SA555 ..... −40°C to 85°C
SE555, SE555C ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555C)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	NE555		SA555		SE555		SE555C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	16	4.5	16	4.5	18	4.5	16	V
Input voltage (CONT, RESET, THRES, and TRIG)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	0	70	−40	85	−55	125	−55	125	°C

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NE555, SA555, SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current (see Note 2)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			−0.4	−1		−0.4	−1.5	
DISCH switch off-state current				20	100		20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.2		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		mA
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is R = R_A + R_B ≈ 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			NE555, SA555, SE555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5%	1.5%		1%	3%	
	Each timer, astable¶			1.5%			2.25%		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§ Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶ Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

electrical characteristics, V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
THRES voltage level	V_{CC} = 15 V		8.8	10	11.2	V
	V_{CC} = 5 V		2.4	3.3	4.2	
THRES current (see Note 2)				30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.5	5	5.6	V
	V_{CC} = 5 V		1.1	1.67	2.2	
TRIG current	TRIG at 0 V			0.5	2	μA
RESET voltage level			0.3	0.7	1	V
RESET current	RESET at V_{CC}			0.1	0.4	mA
	RESET at 0 V			−0.4	−1.5	
DISCH switch off-state current				20	100	nA
CONT voltage (open circuit)	V_{CC} = 15 V		9	10	11	V
	V_{CC} = 5 V		2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.75	
		I_{OL} = 100 mA		2	2.5	
		I_{OL} = 200 mA		2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	12.75	13.3		V
		I_{OH} = −200 mA		12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	15	mA
		V_{CC} = 5 V		3	6	
	Output high, No load	V_{CC} = 15 V		9	13	
		V_{CC} = 5 V		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ

operating characteristics, V_{CC} = 5 V and 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval†	Each timer, monostable‡			1%	3%	
	Each timer, astable§			2.25%		
Supply voltage sensitivity of timing interval	Each timer, monostable‡			0.1	0.5	%/V
	Each timer, astable§			0.3		
Output pulse rise time		C_L = 15 pF		100	300	ns
Output pulse fall time				100	300	

† Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
‡ Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
§ Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

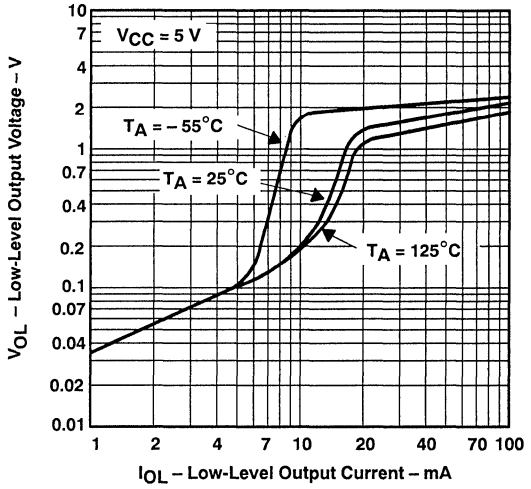


Figure 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

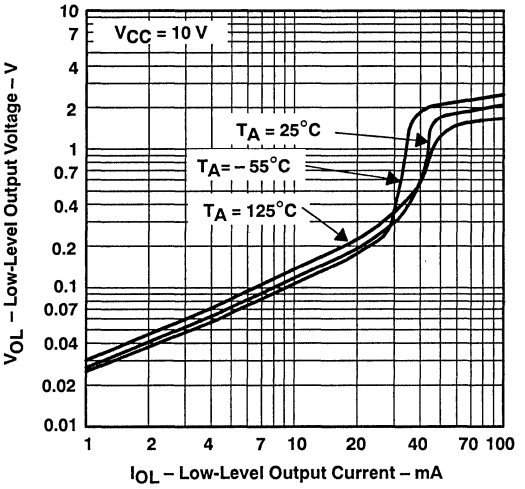


Figure 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

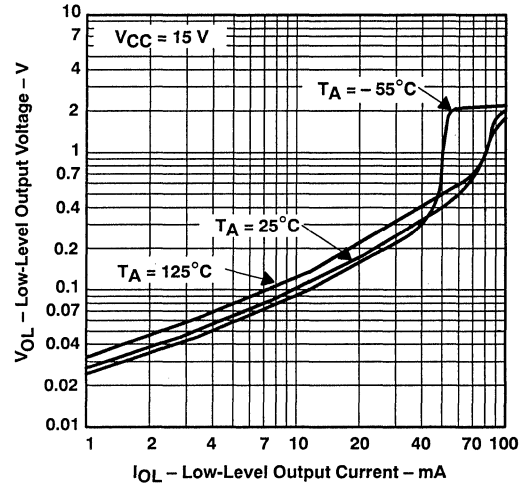


Figure 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

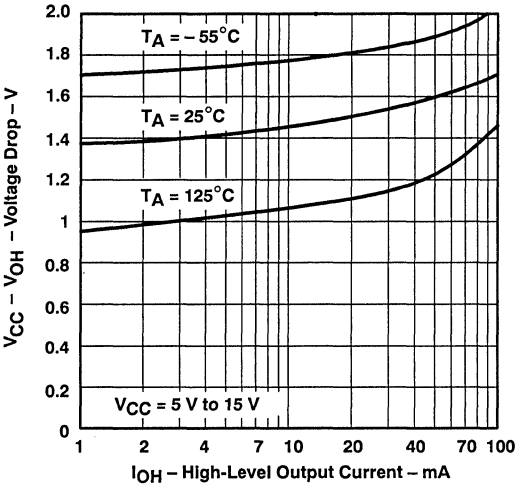


Figure 4

† Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

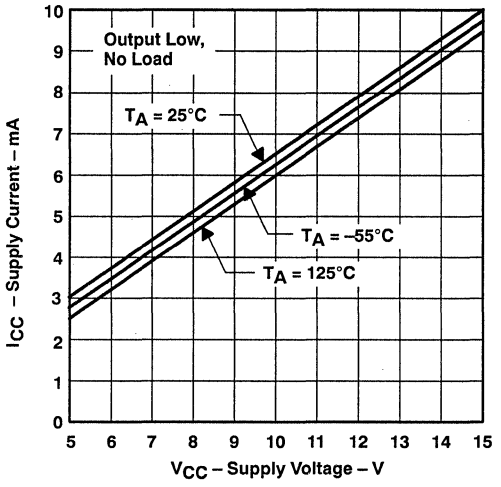


Figure 5

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

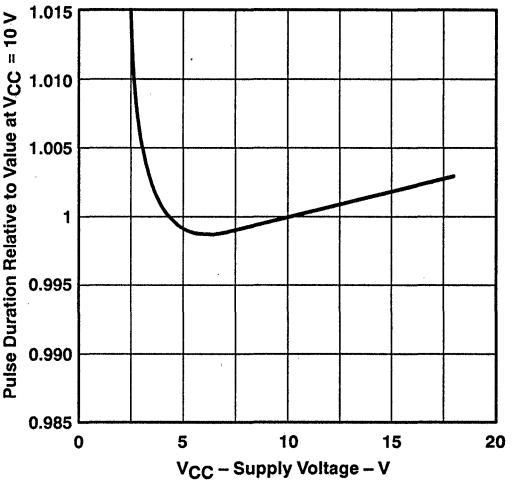


Figure 6

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

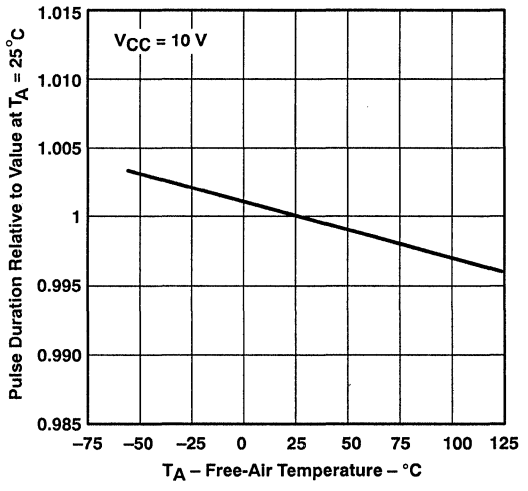


Figure 7

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

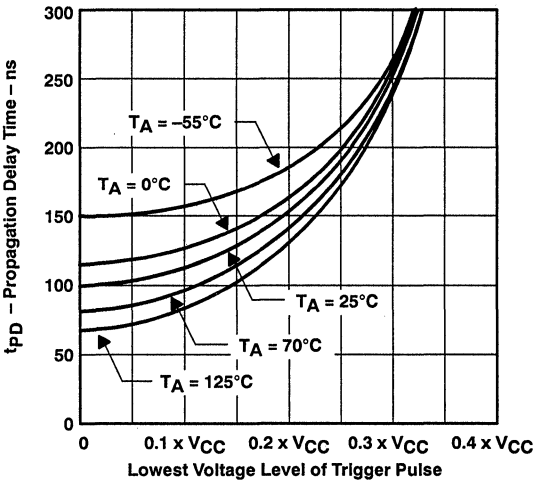


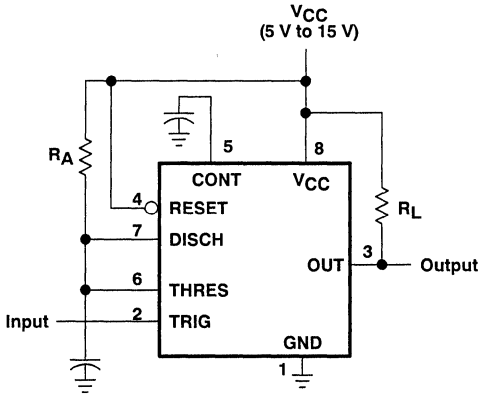
Figure 8

† Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

APPLICATION INFORMATION

monostable operation

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to TRIG sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of THRES input. If TRIG has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.



Pin numbers shown are for the D, JG, and P packages.

Figure 9. Circuit for Monostable Operation

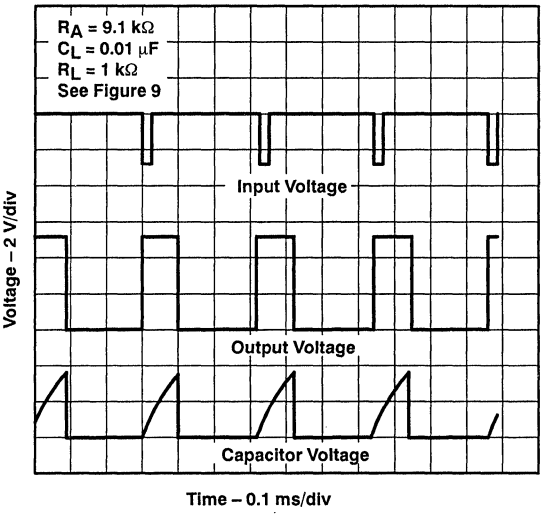


Figure 10. Typical Monostable Waveforms

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1 R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

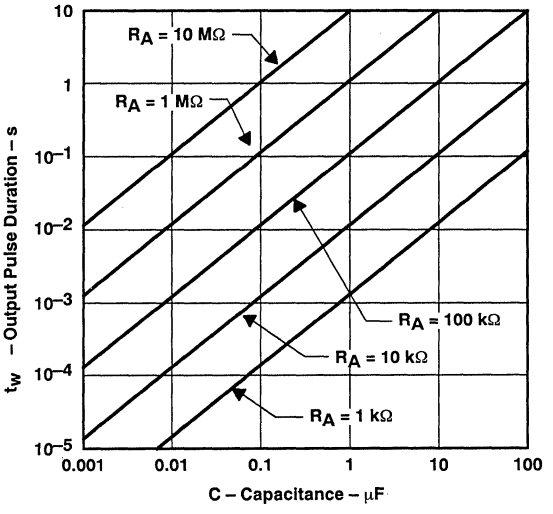


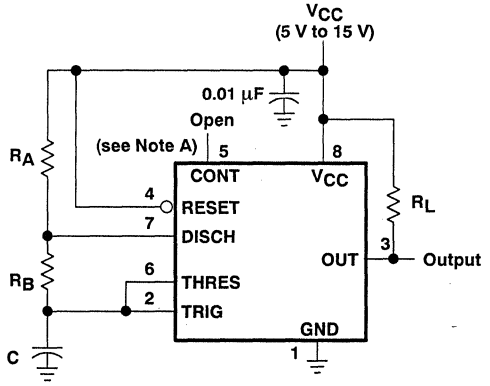
Figure 11. Output Pulse Duration vs Capacitance

APPLICATION INFORMATION

astable operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B and then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.



Pin numbrs shown are for the D, JG, and P packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor may improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

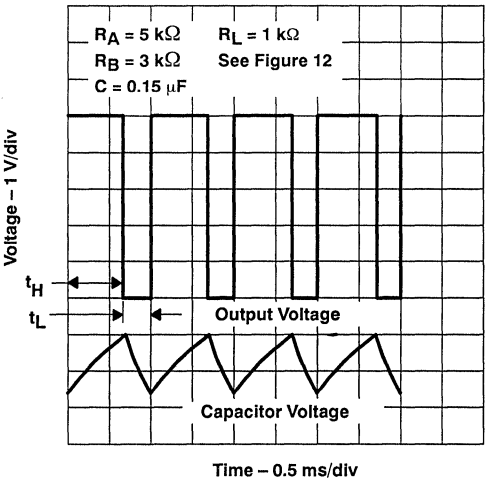


Figure 13. Typical Astable Waveforms

APPLICATION INFORMATION

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

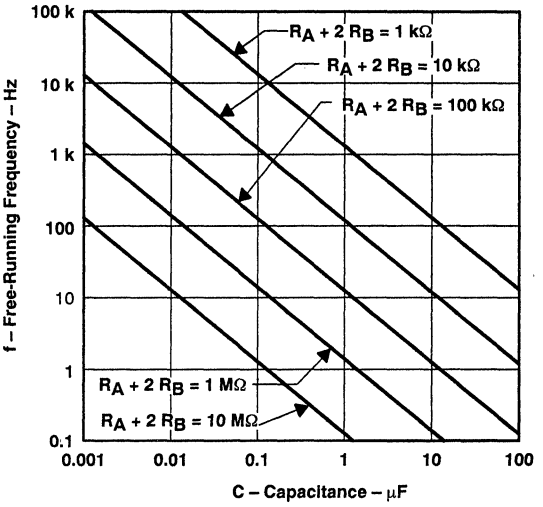
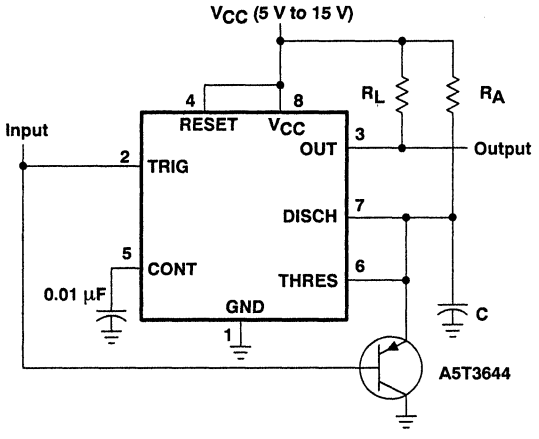


Figure 14. Free-Running Frequency

missing-pulse detector

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.



Pin numbers shown are shown for the D, JG, and P packages.

Figure 15. Circuit for Missing-Pulse Detector

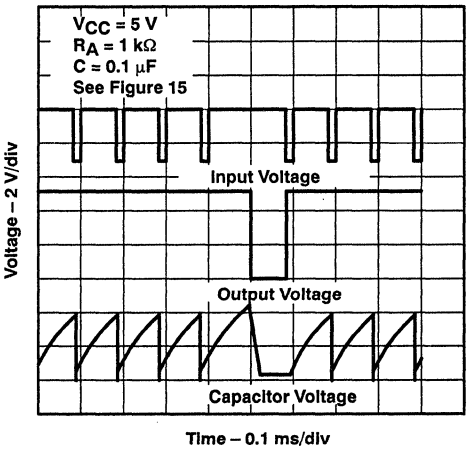


Figure 16. Missing-Pulse Detector Waveform

APPLICATION INFORMATION

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

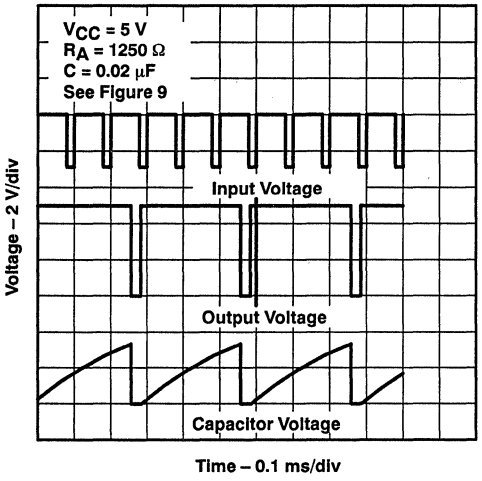
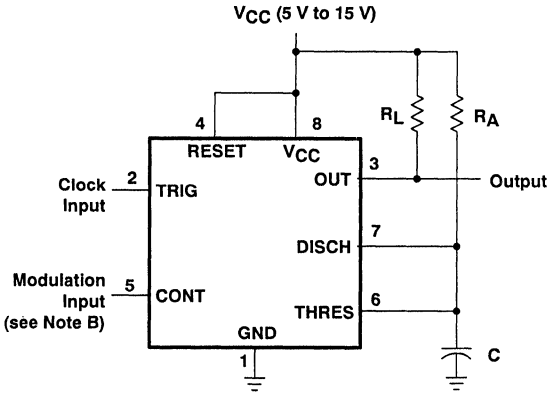


Figure 17. Divide-By-Three Circuit Waveforms

pulse-width modulation

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, and P packages only.

NOTE B: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit For Pulse-Width Modulation

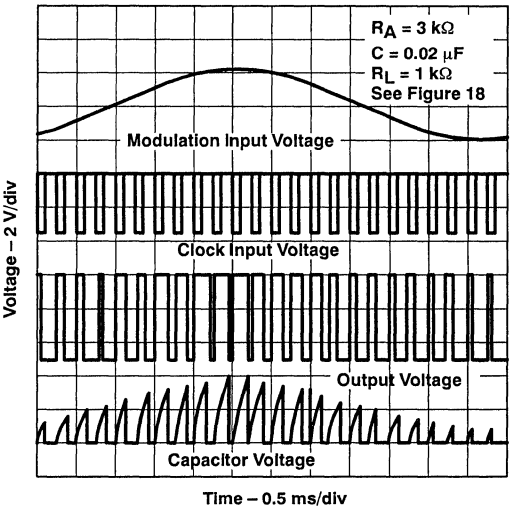
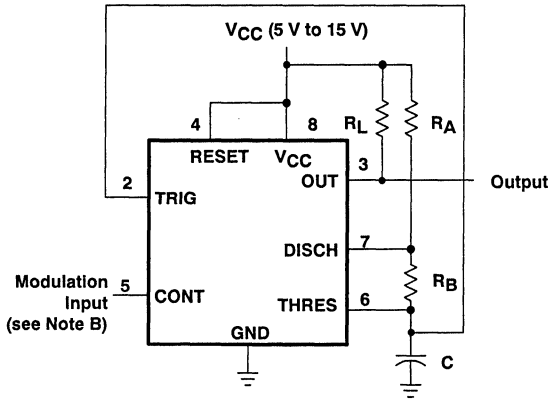


Figure 19. Pulse-Width Modulation Waveforms

pulse-position modulation

As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrates a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, and P packages only.

NOTE B: The modulating signal may be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

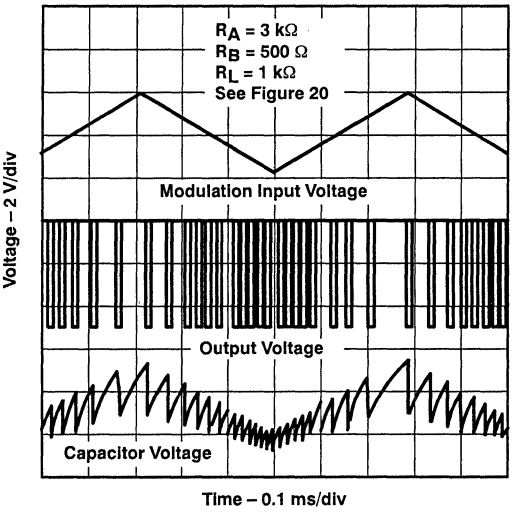
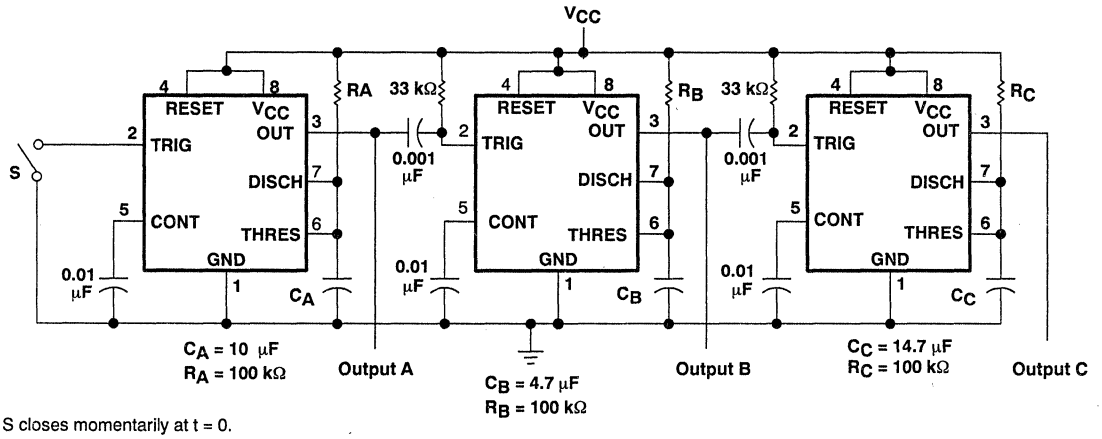


Figure 21. Pulse Position-Modulation Waveforms

APPLICATION INFORMATION

sequential timer



S closes momentarily at t = 0.
Pin numbers shown are for the D, JG, and P packages only.

Figure 22. Sequential Timer Circuit

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

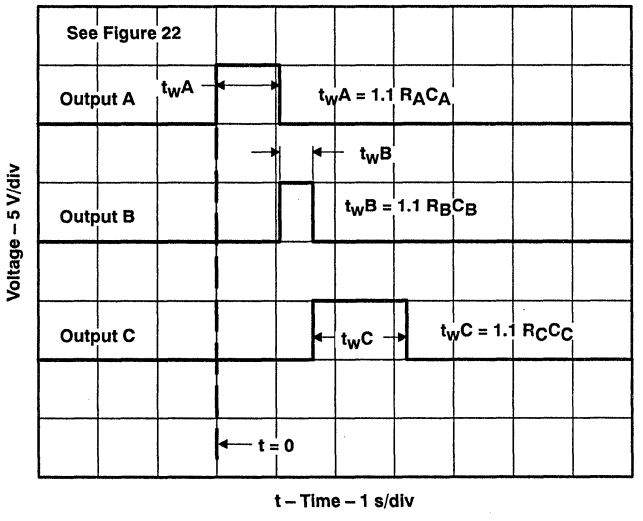


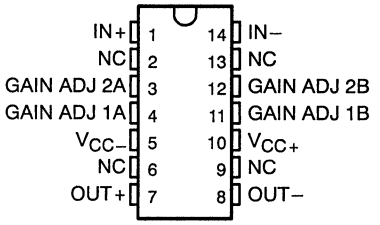
Figure 23. Sequential Timer Waveforms

D2667, FEBRUARY 1984–REVISED NOVEMBER 1991

- **90-MHz Bandwidth**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Pass Band**
- **Designed to Be Interchangeable With Signetics SE592 and NE592**

DEVICE TYPE	TEMPERATURE RANGE	A_{VD} RANGE (GAIN OPTION 1)
NE592	0°C to 70°C	250–600
SE592	−55°C to 125°C	300–500

NE592 . . . D OR N PACKAGE
SE592 . . . J PACKAGE
(TOP VIEW)



NC–No internal connection

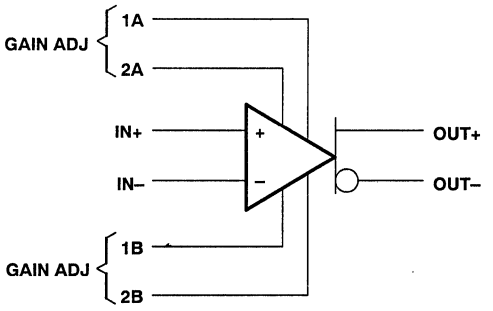
description

These devices are monolithic two-stage video amplifiers with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of nominally 100 or 400 may be selected without external components, or amplification may be adjusted from 0 to 400 by the use of a single external resistor connected between the gain-adjustment pins 1A and 1B. External frequency-compensating components are required for any gain option.

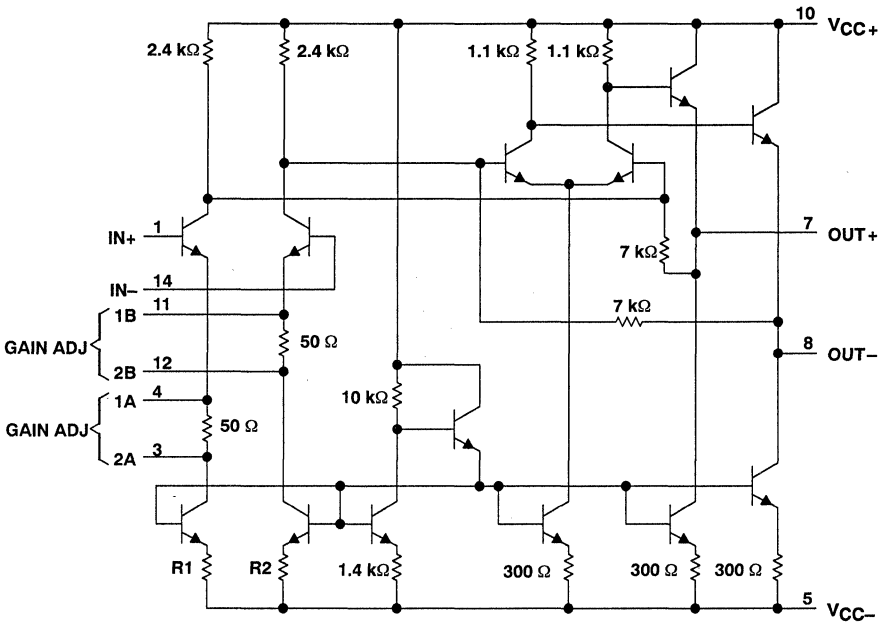
symbol



The devices are particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required..

The NE592 is characterized for operation from 0°C to 70°C. The SE592 is characterized for operation over the full military temperature range of −55°C to 125°C.

schematic



All resistor values shown are in ohms and nominal.
In NE592 or SE592, R1 = 500 Ω, R2 = 500 Ω.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 8 V
Supply voltage, V_{CC-} (see Note 1) ..... –8 V
Differential input voltage ..... ±5 V
Common-mode input voltage ..... ±6 V
Output current ..... 10 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: NE592 ..... 0°C to 70°C
SE592 ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	
J	500 mW	11 mW/°C	105°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	

recommended operating conditions

	NE592			SE592			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	3	6	8	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	−55		125	°C

electrical characteristics, $V_{CC\pm} = \pm 6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	300	400	500	V/V
				2	90	100	110	
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V	1		40		MHz
				2		90		
I_{IO}	Input offset current			1, 2, or 3		0.4	3	μA
I_{IB}	Input bias current			1, 2, or 3		9	20	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			V
V_{OC}	Common-mode output voltage	1	$R_L = \infty$	1, 2, or 3	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{IO} = 0, $R_L = \infty$	1			1.5	V
				2			1	
				3		0.35	0.75	
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		V
r_i	Input resistance			1		4		kΩ
				2	20	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5		ns
				2		4.5	10	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24	mA

† The gain option is selected as follows:
Gain Option 1 . . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . . All Gain Adjust pins are open.

electrical characteristics, $V_{CC\pm}$ = ±6 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	250	400	600	V/V
				2	80	100	120	
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V	1		40		MHz
				2		90		
I_{IO}	Input offset current		V_{IC} = 0	1, 2, or 3		0.4	5	μA
I_{IB}	Input bias current		V_{IC} = 0	1, 2, or 3		9	30	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞		2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{IO} = 0, R_L = ∞	1 or 2			1.5	V
				3		0.35	0.75	
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		V
r_i	Input resistance			1		4		kΩ
				2	10	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5		ns
				2		4.5	12	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24	mA

† The gain option is selected as follows:
Gain Option 1 . . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . . All Gain Adjust pins are open.

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V	1	250		600	V/V
				2	80		120	
I_{IO}	Input offset current			1 or 2			6	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{IO} = 0, R_L = ∞	1 or 2			1.5	V
				3			1	
$V_{O(PP)}$	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.8			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3				mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27	mA

† The gain option is selected as follows:
Gain Option 1 . . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . . All Gain Adjust pins are open.

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V	1	250		600	V/V
				2	80		120	
I_{IO}	Input offset current			1 or 2			5	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1			1.5	V
				2			1.2	
				3			1	
$V_{O(PP)}$	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.5			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	2.5			mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27	mA

† The gain option is selected as follows:
Gain Option 1 . . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . . All Gain Adjust pins are open.

PARAMETER MEASUREMENT INFORMATION

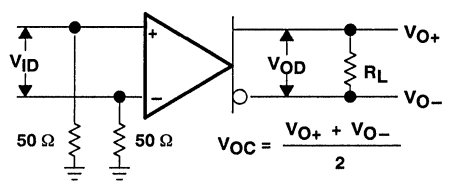


Figure 1

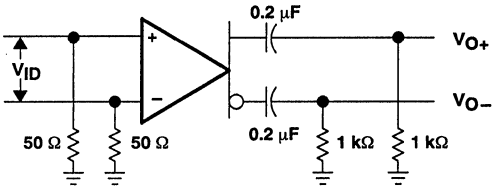


Figure 2

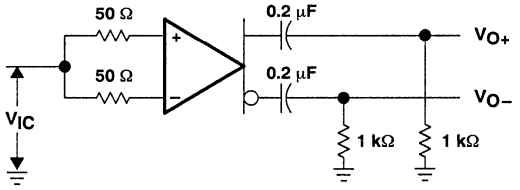


Figure 3

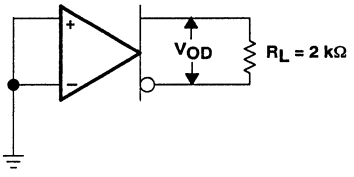


Figure 4

D2440, APRIL 1978—REVISED OCTOBER 1988

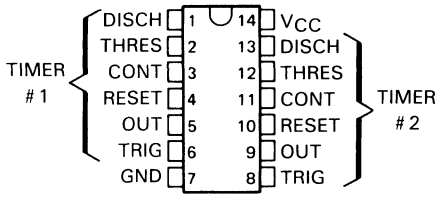
- **Two Precision Timing Circuits per Package**
- **Astable or Monstable Operation**
- **TTL-Compatible Output Can Sink or Source Up to 150 mA**
- **Active Pull-Up or Pull-Down**
- **Designed to be Interchangeable with Signetics SE556, SE556C, SA556, NE556**

APPLICATIONS

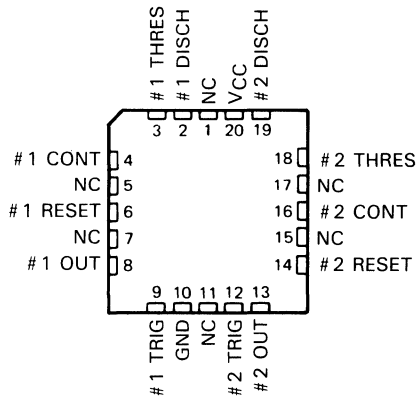
Precision Timer from Microseconds to Hours	**Sequential Timer**
Pulse-Shaping Circuit	**Pulse Generator**
Missing-Pulse Detector	**Time-Delay Circuit**
Tone-Burst Generator	**Frequency Divider**
Pulse-Width Modulator	**Appliance Timer**
Pulse-Position Modulator	**Industrial Controls**
	Touch-Tone Encoder

SE556C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

SE556, SE556C . . . J PACKAGE
SA556, NE556 . . . D, J, OR N PACKAGE
(TOP VIEW)



SE556, SE556C . . . FK PACKAGE
(TOP VIEW)



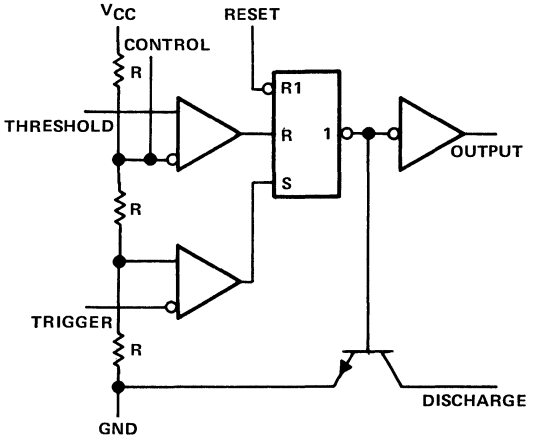
NC—No internal correction

description

These devices provide two monolithic, independent timing circuits of the SE555, SE555C, SA555, or NE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor timing control. The basic timing provided by the RC time constant may be actively controlled by modulating the bias of the control voltage input.

The threshold and trigger levels are normally two-thirds and one-third respectively of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level,, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

The SE556 and SE556C are characterized for operation over the full military range of −55°C to 125°C. The SA556 is characterized for operation from −40°C to 85°C, and the NE556 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A RANGE	V_{thres} MAX V_{CC} = 15 V	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	11.2 V	NE556D		NE556J	NE556N
−40°C to 85°C	11.2 V	SA556D		SA556J	SA556N
−55°C to 125°C	10.6 V 11.2 V		SE556FK SE556CFK	SE556J SE556CJ	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE556DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 18 V
Input voltage (control, reset, threshold, and trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: SE556, SE556C . . . . . −55°C to 125°C
SA556 . . . . . −40°C to 85°C
NE556 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SE556, SE556C)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SA556, NE556)	1025 mW	8.2 mW/°C	656 mW	533 mW	N/A
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N/A

recommended operating conditions

	SE556		SE556C		SA556		NE556		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.15		0.1	0.25	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.3	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		20	24		20	30	mA
		V_{CC} = 5 V		6	10		6	12	
	Output high, No load	V_{CC} = 15 V		18	20		18	26	
		V_{CC} = 5 V		4	8		4	10	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 1. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is ≈ 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
	Timer 1 — Timer 2			±0.5			±1		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
	Timer 1 — Timer 2			±10			±10		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0 5	%/V
	Each timer, astable¶			0.15			0.3		
	Timer 1 — Timer 2			±0.1			±0.2		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§Values specified are for a device in a monostable circuit similar to Figure 2, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 1, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL APPLICATION DATA

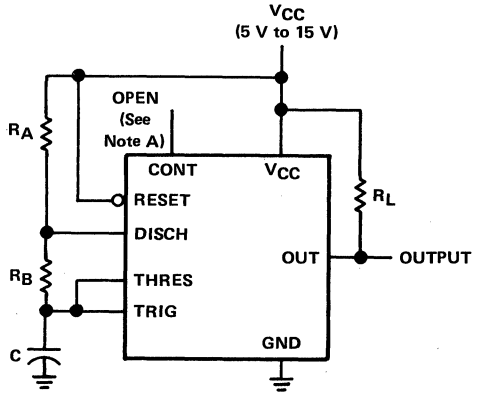


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

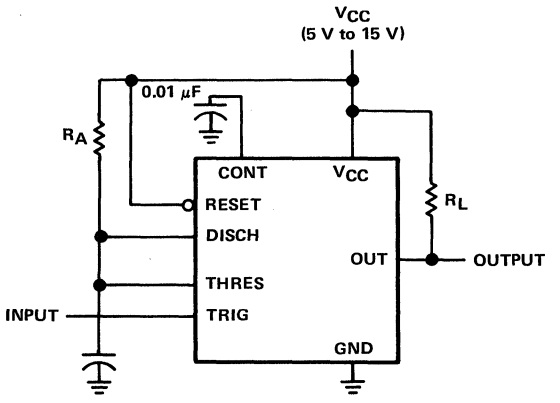


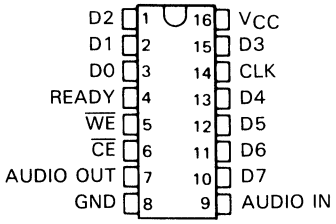
FIGURE 2. CIRCUIT FOR MONOSTABLE OPERATION

NOTE A: Bypassing the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

D2801, JUNE 1984—REVISED JANUARY 1989

- **Each Circuit Contains 3 Programmable Tone Generators**
- **Programmable White-Noise Generator**
- **Programmable Attenuation**
- **Simultaneous Sounds**
- **Up to 500 kHz Clock Input for SN76494 and 4 MHz for SN76496**
- **External Audio Input for SN76496 May Be Summed with Internally Generated Tones**
- **The SN76494A and SN76496A are Interchangeable with the SN76494 and SN76496, Respectively**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

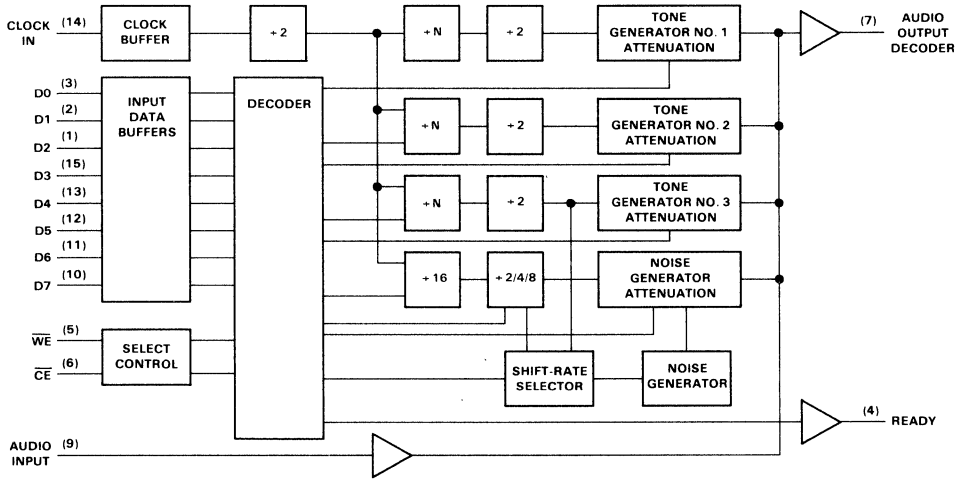
The SN76494 and SN76494A digital complex sound generators are integrated injection logic (I^2L) tone generators designed to provide low-cost tone or noise generation capability in microprocessor systems. The SN76494 and SN76494A are data-bus-based input-output peripheral devices that interface the microprocessor through 8 data lines and 3 control lines.

The SN76494 and SN76494A are identical to the SN76496 and SN76496A except that the maximum clock input frequency for SN76494 and SN76494A is 500 kHz and for SN76496 and SN76496A, it is 4 MHz. A "divide-by-eight" stage is deleted from the SN76496 and SN76496A circuitry so that only 4 clock pulses are required to load the data into the SN76494 and SN76494A, compared to 32 pulses for the SN76496 and SN76496A.

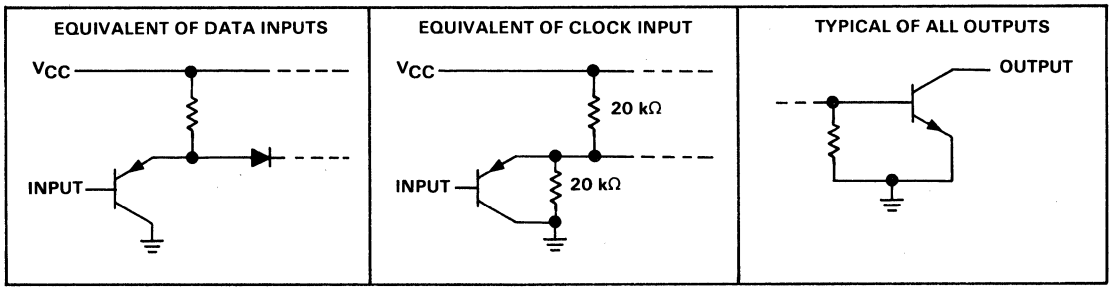
Either of these devices may also be used as a replacement for the SN76489A in all applications if pin 9 is left open or grounded. The output load must be limited to 10 mA.

When audio input is not desired in the SN76494, SN76494A, SN76496 or SN76496A, the audio input pin should be grounded.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: Audio input . . . . . 0.9 V
All other inputs . . . . . 7 V
Output current at pin 7 . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		SN76494, SN76494A			SN76496, SN76496A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_I	Audio input current	0		1.8	0		1.8	mA
V_{OH}	High-level output voltage (pin 4)			5.5			5.5	V
I_{OL}	Low-level output current (pin 4)			2			2	mA
f_{clock}	Input clock frequency			0.5			4	MHz
$t_{d(WE)}$	Delay time, $\overline{CE}$ low to $\overline{WE}$ low	0			0			ns
t_{su}	Setup time, data before $\overline{WE}\downarrow$ or $\overline{CE}\downarrow$	0			0			ns
t_h	Hold time, data after READY↑	0			0			ns
T_A	Operating free-air temperature	0		70	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current (pin 4)		V_O = 5.5 V			10	μA
I_{IH}	High-level input current (All digital inputs)		$V_I = V_{CC}$			10	μA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_I = 0		−25	−175	μA
		All other digital inputs			−10	−70	
V_{IB}	Input bias voltage, audio (pin 9)		R = 4.7 kΩ to V_{CC}	0.5	0.7	0.9	V
V_{OH}	High-level output voltage (pin 7)					5.5	V
V_{OL}	Low-level output voltage (pin 4)		I_{OL} = 2 mA		0.25	0.4	V
V_{OPP}	Peak-to-peak output voltage (pin 7)		V_{CC} = 5 V, Attenuation: Generator under test = 0 dB, All other generators = 30 dB	260			mV
I_{CC}	Supply current				30	50	mA
	Attenuation	2 dB NOM	See Table 1	1	2	3	dB
		4 dB NOM		3	4	5	
		8 dB NOM		7	8	9	
		16 dB NOM		15	16	17	
C_i	Input capacitance					15	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level RDY output from $\overline{CE}$	C_L = 225 pF, R_L = 2 kΩ to V_{CC}		90	150	ns
t_{PHL}	Propagation delay time high-to-low level, RDY output from $\overline{WE}$			90		ns
t_{PLH}	Propagation delay time low-to-high level, RDY output from CLK			90		ns

PARAMETER MEASUREMENT INFORMATION

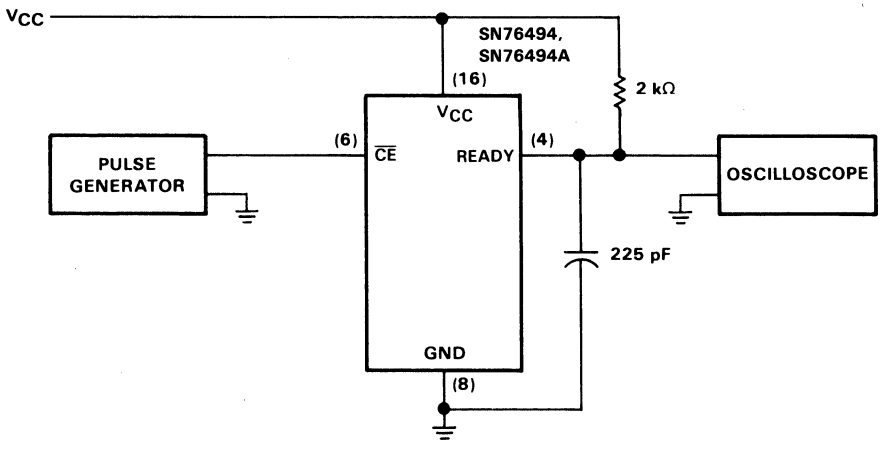


FIGURE 1. t_{PHL} TEST CIRCUIT

pin assignments and functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{CE}$	6	I	Chip Enable. When chip enable is low, the device is operational, input terminals are enabled, and data may be entered.
D0 (MSB)	3	I	D0 through D7 – Input data bus
D1	2	I	
D2	1	I	
D3	15	I	
D4	13	I	
D5	12	I	
D6	11	I	
D7 (LSB)	10	I	
V_{CC}	16	I	Supply voltage (5 V nom)
GND	8	O	Ground reference
CLOCK	14	I	Input Clock
$\overline{WE}$	5	I	Write Enable. When $\overline{CE}$ is enabled and $\overline{WE}$ is active (low), input on the data bus is accepted. $\overline{CE}$ and $\overline{WE}$ must be held low until READY returns high (four clock cycles for the SN76494 and SN76494A or 32 clock cycles for the SN76496 and SN76496A). If $\overline{WE}$ remains low throughout four additional clock cycles for the SN76494 and SN76494A (32 clock cycles for the SN76496 and SN76496A) a new write cycle will be initiated.
READY	4	O	When low, READY indicates that a write cycle is in progress; data on the input bus must remain valid until READY returns high.
AUDIO IN	9	I	Audio input from external source
AUDIO OUT	7	O	Audio Drive Out

PRINCIPLES OF OPERATION

tone generators

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (f). F0 is the most significant bit and F9 is the least significant bit. This information is loaded into a 10-stage tone counter, which counts down at an N/2 rate where N is the input clock frequency. When the tone counter counts down to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{4n} \text{ for SN76494 and SN76494A, or } f = \frac{N}{32n} \text{ for SN76496 and SN76496A}$$

where N = clock in Hz
n = 10-bit binary number

The output level of each tone/noise generator may be selected by programming a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 30 dB.

TABLE 1. ATTENUATION CONTROL

BIT POSITION				WEIGHT
A0	A1	A2	A3	(In dB)
0	0	0	1	2
0	0	1	0	4
0	1	0	0	8
1	0	0	0	16
1	1	1	1	OFF

noise generator

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR-feedback network. The feedback network has provisions to protect the shift register from being locked in the zero state.

TABLE 2. NOISE FEEDBACK CONTROL

FEEDBACK	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 3. NOISE GENERATOR FREQUENCY CONTROL

BITS		SHIFT RATE
NF0	NF1	
0	0	N/64
0	1	N/128
1	0	N/256
1	1	Tone generator #3 output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

output buffer/amplifier

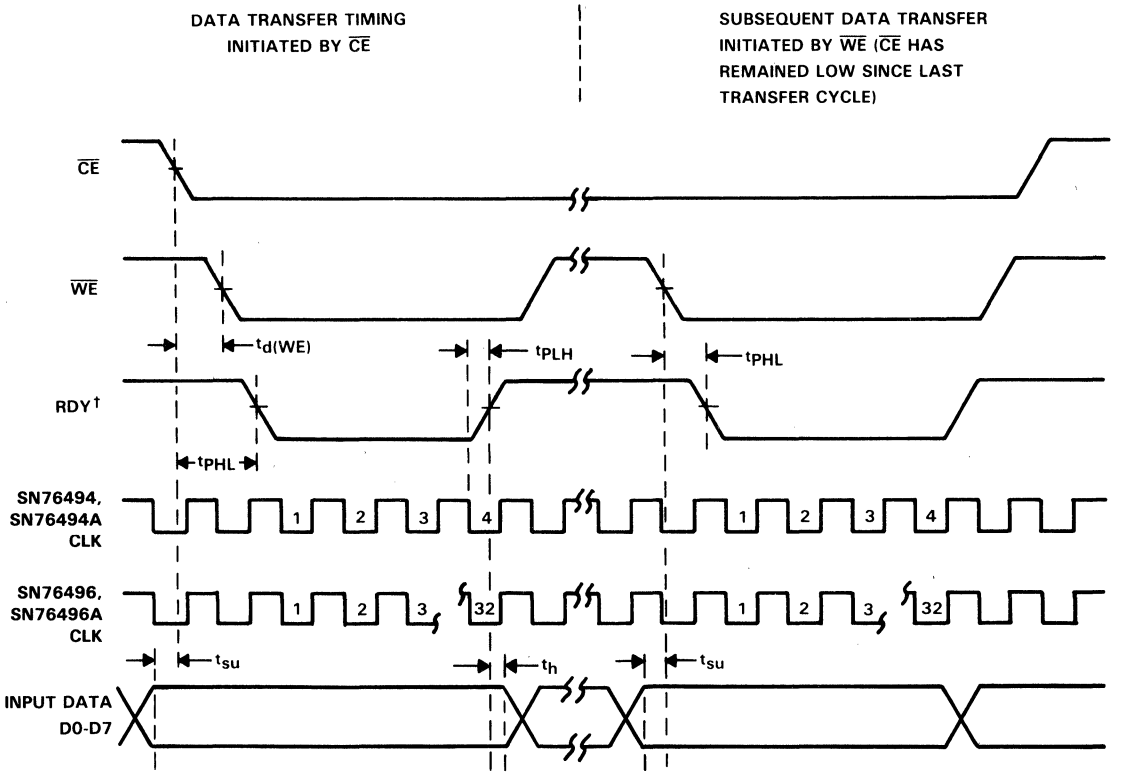
The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, the noise generator output, and any audio input through pin 9. The output buffer will generate up to 10 mA.

To prevent oscillations in the output buffer, the output (pin 7) should be decoupled. This is done by putting 10 ohms in series with 0.1 μF from pin 7 to ground (see Figure 3).

data transfer

The microprocessor selects the SN76494, SN76494A, SN76496, or SN76496A by taking $\overline{CE}$ low (low voltage). Unless $\overline{CE}$ is low, no data transfer can occur. When $\overline{CE}$ is low, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

The SN76494 and SN76494A require approximately 4 clock cycles to load the data into the control register. The SN76496 and SN76496A require approximately 32 clock cycles. The open-collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low) immediately following the falling edge of $\overline{CE}$ (or $\overline{WE}$ when data transfer is initiated by $\overline{WE}$). READY will go high upon completion of the data transfer cycle. The data transfer timing is shown below.



† $\overline{WE}$ must be returned high (inactive) within 4 clock pulses for the SN76494 and SN76494A (32 clock pulses for the SN76496 and SN76496A) after RDY returns high. Otherwise, a new data transfer cycle will be initiated.

FIGURE 2. DATA TRANSFER TIMING

TABLE 4. FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

This table is valid when the device is:
(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

CPU interface to SN76494, SN76494A, SN76496 or SN76496A

The microprocessor interfaces with the SN76494, SN76494A, SN76496, or SN76496A by means of the 8 data lines and 3 control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and four bits of information to select the attenuation. A frequency selection requires a double-byte transfer, while an attenuator selection requires a single-byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the six most significant bits to be quickly modified for frequency sweeps.

control registers

The devices have 8 internal registers that are used to control the 3 tone generators and the noise source. During all data transfers to the devices, the first byte contains a 3-bit field that determines the destination control register. The register address codes are shown in Table 5.

TABLE 5. REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

data formats

The formats required to transfer data are shown below.

	REG ADDR			DATA			
1	R0	R1	R2	F6	F7	F8	F9

BIT 0 FIRST BYTE BIT 7

	DATA						
0	x	F0	F1	F2	F3	F4	F5

BIT 0 SECOND BYTE BIT 7

UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)

	REG ADDR					SHIFT	
1	R0	R1	R2	x	FB	NF0	NF1

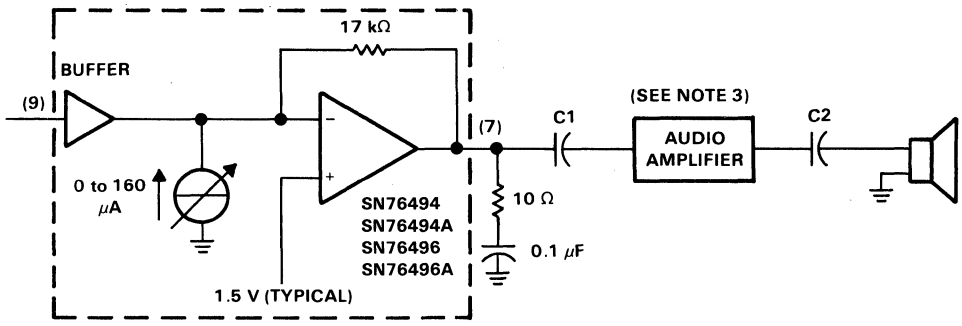
BIT 0 BIT 7

UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)

	REG ADDR			DATA			
1	R0	R1	R2	A0	A1	A2	A3

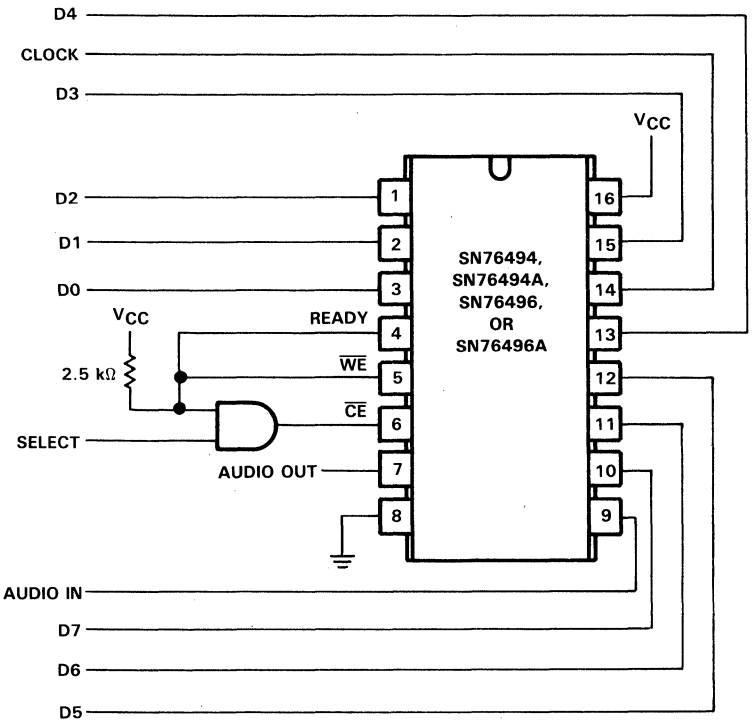
BIT 0 BIT 7

TYPICAL APPLICATION DATA



NOTE 3: The capacitance values of C1 and C2 are determined by the frequency response desired and the audio amplifier used.

FIGURE 3. EXTERNAL AUDIO OUTPUT INTERFACE



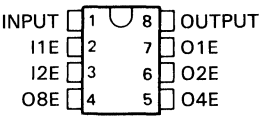
NOTES: 4. The data lines must be latched so that the data remains on them at least 32 clock cycles for the SN76496 and SN76496A or (4 clock cycles for the SN76494 and SN76494A) after the select line goes low.
5. The select pulse should be a negative-going pulse with minimum duration of 150 ns.

FIGURE 4. MICROCOMPUTER PARALLEL PORT INTERFACE

D2738, SEPTEMBER 1983—REVISED APRIL 1988

- **33 Distinct Input-to-Output Emitter Ratios from 3:1 to 1:15**
- **Wide Input current Range: 1 μA to 3 mA**
- **35-Volt Output Capability**
- **High Output Impedance**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL010 is a Wilson current mirror that provides output current in a selectable fixed ratio to the input current. The ratio is substantially independent of changes in load, voltages, and temperature. Selecting the ratio consists of connecting appropriate input-emitter pins and output-emitter pins to ground as shown in Figure 1.

The TL010 is designed to operate with up to 3 mA input current if all three input-emitter pins are used. It will also operate at voltages up to 35 V.

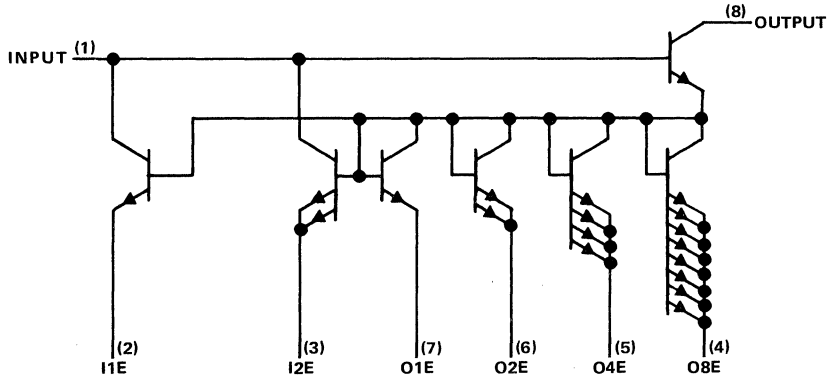
The TL010I is characterized for operation from −40°C to 85°C. The TL010C is characterized for operation from 0°C to 70°C.

typical values of current ratio at T_A = 25°C†

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$	EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$	EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:15	14.1	1:6	5.78	3:8	2.61
1:14	13.2	2:11	5.34	2:5	2.43
1:13	12.3	1:5	4.82	3:7	2.26
1:12	11.4	3:14	4.53	1:2	1.98
1:11	10.5	2:9	4.38	3:5	1.64
1:10	9.55	3:13	4.21	2:3	1.45
1:9	8.62	1:4	3.89	3:4	1.32
1:8	7.72	3:11	3.57	1:1	0.99
2:15	7.23	2:7	3:40	3:2	0.663
1:7	6:71	3:10	3:25	2:1	0.50
2:13	6.29	1:3	2.90	3:1	0.332

†m is the number of input emitters used, n is the number of output emitters used.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 725 mW
Operating free-air temperature range: TL010I . . . . . −40°C to 85°C
TL010C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8.0 mW/°C.

recommended operating conditions

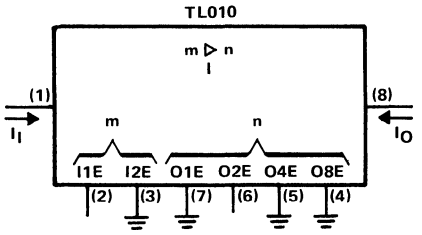
	TL010I		TL010C		UNIT
	MIN	MAX	MIN	MAX	
Output voltage, V_O	5	35	5	35	V
Input voltage, V_I	0.6	1.7	0.65	1.6	V
Input current per input emitter, I_I	0.001	1	0.001	1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL010I			TL010C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = m × 1 μA			1			1		V
		I_I = m × 10 μA			1.1			1.1		
		I_I = m × 100 μA			1.25			1.25		
		I_I = m × 1 mA			1.4			1.4		
h_F	Current ratio (I_O/I_I)	I_I = MIN to MAX	m:n = 1:8	6.97	7.72	8.13	7.05	7.72	8.13	
			m:n = 1:4	3.61	3.89	4.05	3.64	3.89	4.05	
			m:n = 1:2	1.84	1.98	2.07	1.88	1.98	2.07	
			m:n = 1:1	0.89	0.99	1.08	0.94	0.99	1.04	
			m:n = 2:1	0.46	0.50	0.56	0.475	0.50	0.525	
α_{hF}	Temperature coefficient of current ratio	I_I = MIN to MAX			300			300		ppm/°C
	Output-to-input isolation	I_I = MIN to MAX,	f = 1 kHz	60			60			dB
$V_{O(th)}$	Output threshold voltage§	I_I = MIN to MAX	T_A = MIN			1.1			1.05	V
			T_A = 25°C			1			1	
r_o	Output resistance¶	F = 1 kHz	I_I = m × 10 μA		200 m/n			200 m/n		MΩ
			I_I = m × 100 μA		20 m/n			20 m/n		
			I_I = m × 1 mA		2 m/n			2 m/n		
f_{max}	Maximum operating frequency#	I_I = m × 1 mA, R_L = 500 Ω			10			10		MHz

† m is the number of input emitters, n is the number of output emitters. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C.
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶The output resistance is directly proportional to the number of input emitters divided by the number of output emitters (m/n).
#Maximum operating frequency is the frequency at which the output current is down 3 dB from its low-frequency value.

TYPICAL APPLICATION INFORMATION



See Notes 3 and 4

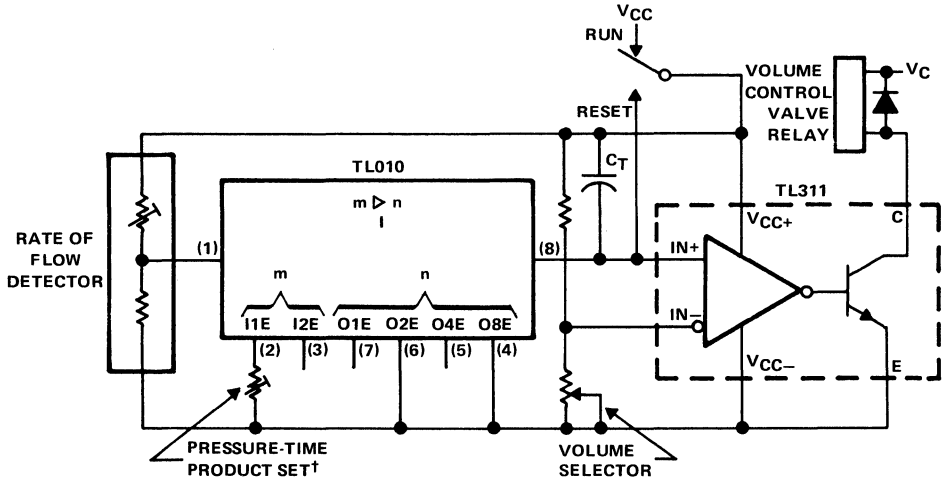
NOTES: 3. Selected emitters must be grounded as close as possible to the package to avoid unstable device behavior.
Using the fixed-Beta model, the current ratio for a current mirror of m input emitters and n output emitters may be calculated as

$$\frac{I_O}{I_I} = \frac{\beta^2 n + \beta(n + m)}{\beta^2 m + (\beta + 1)(m + n)}$$

Second-order effects, such as on-chip self-heating, may slightly perturb the observed ratio from the calculated value.

4. At high current levels, a small capacitor (270 pF) may be required between the input and output terminals to improve stability.

FIGURE 1. CURRENT MIRROR SET FOR A CURRENT RATIO OF 2:13



†Adjust for a mirror of 11.9

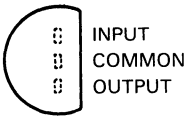
FIGURE 2. TYPICAL APPLICATION CIRCUIT

In the application shown in Figure 2, the problem is to measure a precise volume of liquid flowing through a line and shut off the flow with a relay when limit is reached. For the particular volume to be measured and the pressure detector used, a current gain of 11.9 is required. By setting the TL010 for a gain of 10 with the emitter selection, the exact gain of 11.9 may be obtained by adjusting the pressure-time product control.

D2614, FEBRUARY 1984—REVISED OCTOBER 1988

- **Wide Input Current Range: 1 μA to 1 mA**
- **35-Volt Output Capability**
- **High Output Impedance**
- **Current-Ratio Tolerances Over Full Temperature Range; ±8% for I Suffix ±7% for C Suffix**
- **Typically Less Than ±1% Error at 25°C**

LP PACKAGE
(TOP VIEW)



TEMPERATURE RANGE	INPUT-TO-OUTPUT CURRENT RATIO			
	1:1	1:2	1:4	2:1
−40°C to 85°C	TL011I	TL012I		TL021I
0°C to 70°C	TL011C	TL012C	TL014AC	TL021C

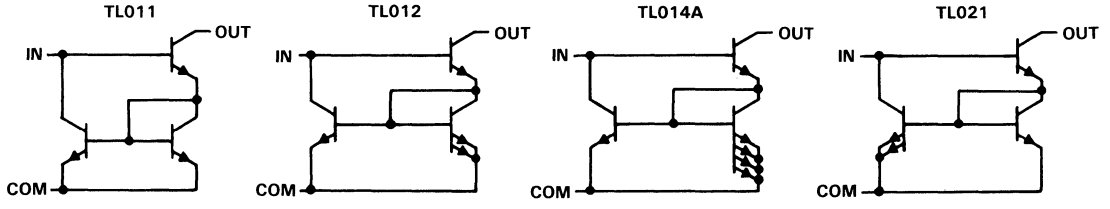
description

The TL011, TL012, TL014A, and TL021 are Wilson current mirrors with output currents in fixed proportion to the input currents and substantially independent of changes in voltage, load, and temperature. These devices make use of the tight matching properties of identical bipolar transistors on a monolithic integrated circuit chip to achieve current-ratio accuracy typically better than 98%.

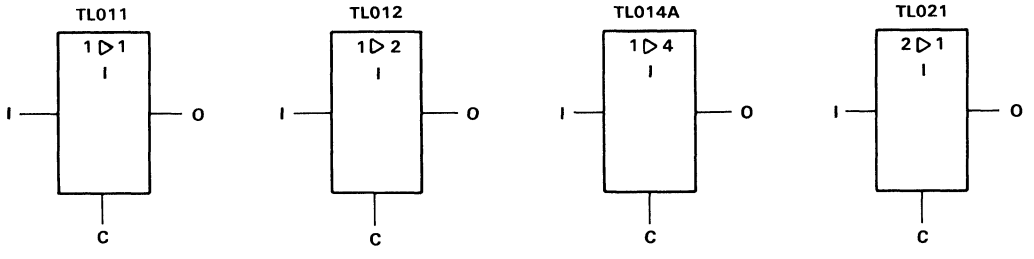
Current mirrors are used extensively in linear integrated circuit designs as active loads for operational-amplifier stages and as current sources for other stages. The TL011 family gives the designer this same capability with no sacrifice in accuracy or stability.

The TL011, TL012, and TL014A are designed to operate with input currents up to 1 mA and output voltage up to 35 V. The TL021 is designed for 2 mA and 35 V.

schematics



symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 775 mW
Operating free-air temperature range: TL011I, TL012I, TL021I . . . . . −40°C to 85°C
TL011C, TL012C, TL014AC, TL021C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C. The LP package dissipation rating was based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

recommended operating conditions

		TL0__I		TL0__C, AC		UNIT
		MIN	MAX	MIN	MAX	
Output voltage, V_O		5	35	5	35	V
Input current, I_O	TL021	0.002	2	0.002	2	mA
	All others	0.001	1	0.001	1	
Operating free-air temperature, T_A		−40	85	0	70	°C

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL011			TL012			TL014A			TL021			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage		I_I = 1 μA			1			1			1					V
			I_I = 2 μA												1		
			I_I = 10 μA			1.1			1.1			1.1					
			I_I = 20 μA												1.1		
			I_I = 100 μA			1.25			1.25			1.25					
			I_I = 200 μA												1.25		
			I_I = 1 mA			1.4			1.4			1.4					
			I_I = 2 mA												1.4		
h_F	Current ratio (I_O/I_I)	TLO_I	I_I = MIN to MAX‡		0.92	1	1.08	1.84	2	2.16	3.68	4	4.32	0.46	0.5	0.54	
		TLO_C, AC			0.93	1	1.07	1.86	2	2.14	3.72	4	4.28	0.465	0.5	0.535	
α_{hF}	Temperature coefficient of current ratio		I_I = MIN to MAX			50			100			200			200		ppm/°C
	Output-to-input isolation		I_I = MIN to MAX,	f = 1 kHz	80			80			80			80			dB
$V_{O(th)}$	Output threshold voltage§	TLO_I	I_I = MIN to MAX	T_A = −40°C			1.35			1.35			1.35			1.35	V
		TLO_C, AC		T_A = 0°C			1.25			1.25			1.25			1.25	
		All		T_A = 25°C			1.2			1.2			1.2			1.2	
r_o	Output resistance		f = 1 kHz	I_I = 10 μA		200			100			50					MΩ
				I_I = 20 μA											200		
				I_I = 100 μA		20			10			5					
				I_I = 200 μA											20		
				I_I = 1 mA		2			1			0.5					
				I_I = 2 mA											2		
f_{max}	Maximum operating frequency¶		I_I = MAX	R_L = 500 Ω		10			10			10			10		MHz

†All typical values are at T_A = 25°C.
‡For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶Maximum operating frequency is the frequency at which the output current is down 3 dB from its low frequency value.

TYPICAL CHARACTERISTICS

TL011
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

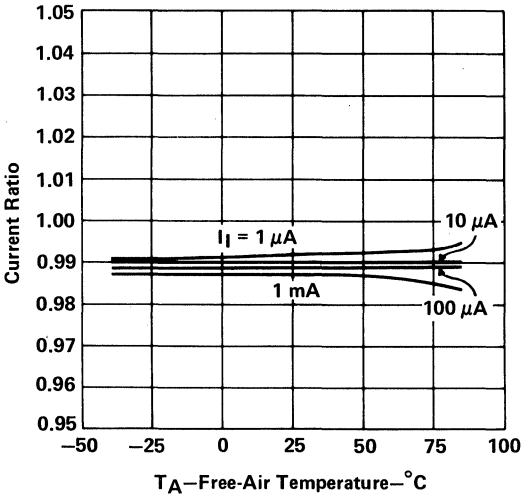


FIGURE 1

TL012
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

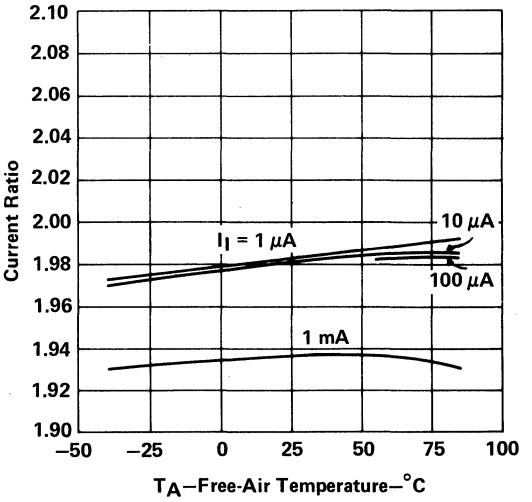


FIGURE 2

TL014A
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

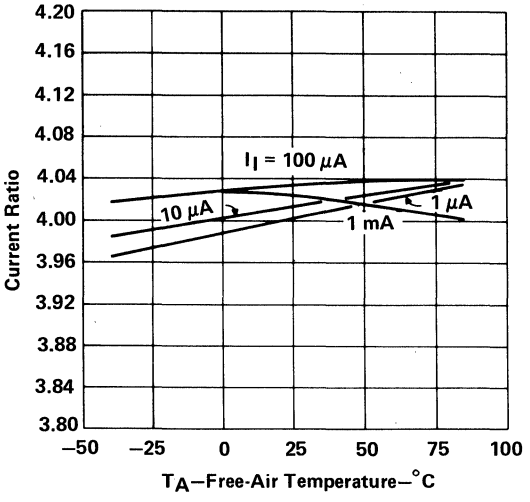


FIGURE 3

TL021
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

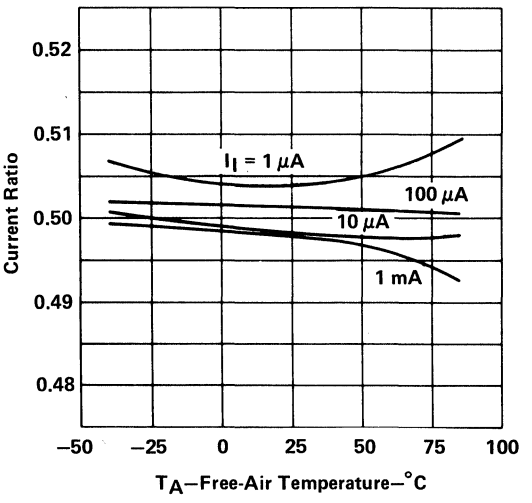


FIGURE 4

TYPICAL APPLICATIONS INFORMATION

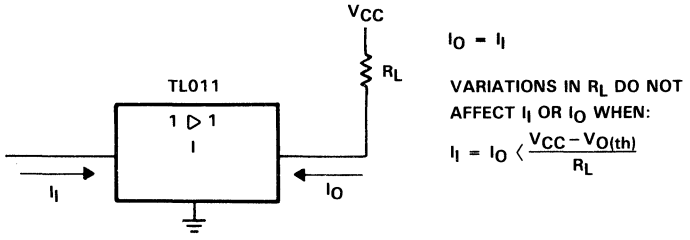
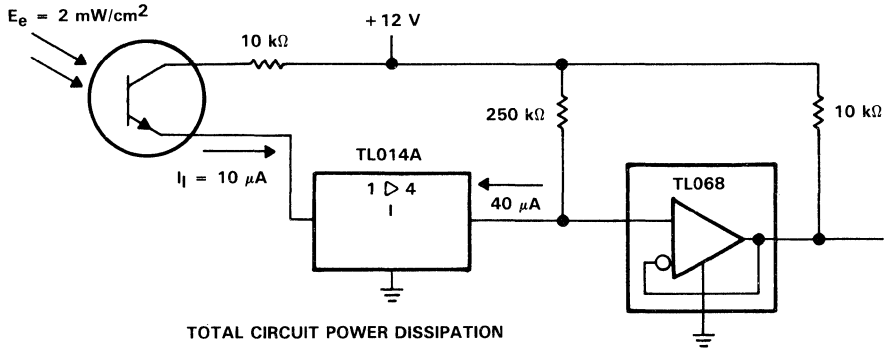


FIGURE 5. BASIC CURRENT BUFFER



Idle condition: P_D = 1.5 mW typical
On condition: P_D = 12.5 mW typical
10 μA from phototransistor provides a V_O swing of 10 V at 1 mA.

FIGURE 6. PHOTOTRANSISTOR PREAMPLIFIER

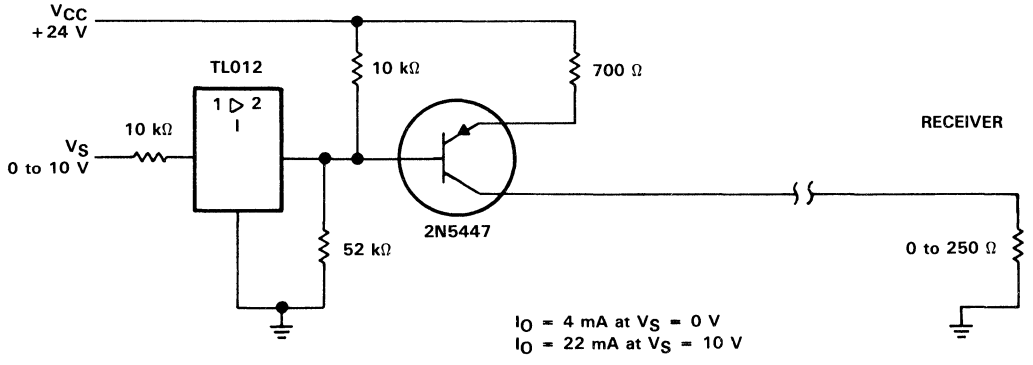
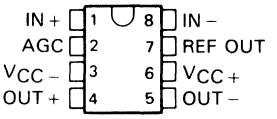


FIGURE 7. TWO-WIRE LINEAR CURRENT-MODE TRANSMITTER

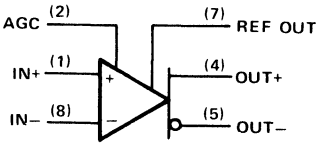
D2790, JUNE 1985—REVISED JULY 1990

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Peak Gain . . . 38 dB Typ**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D OR P PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage high-frequency amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pin. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers where a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL026C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25 °C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	65	85	105	V/V
ΔA_{VD}	Change in voltage amplification	1	V_{IPP} = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = −1 mA to 100 μA	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV		50		MHz
I_{IO}	Input offset current				0.4	5	μA
I_{IB}	Input bias current				10	30	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	3	4		V
r_i	Input resistance at AGC, IN+, or IN−			10	30		kΩ
r_o	Output resistance				20		Ω
CMRR	Common-mode rejection ratio	3 3	V_{IC} = ±1 V, f = 100 kHz V_{IC} = ±1 V, f = 5 mHz	60	86 60		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		6	10	ns
t_r	Rise time	2	ΔV_O = 1 V		4.5	12	ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	3	4		mA
I_{CC}	Supply current		No load, No signal		22	27	mA

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	55		115	V/V
I_{IO}	Input offset current					6	μA
I_{IB}	Input bias current					40	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	2.8			V
r_i	Input resistance at AGC, IN+, or IN−			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal			30	mA

PARAMETER MEASUREMENT INFORMATION

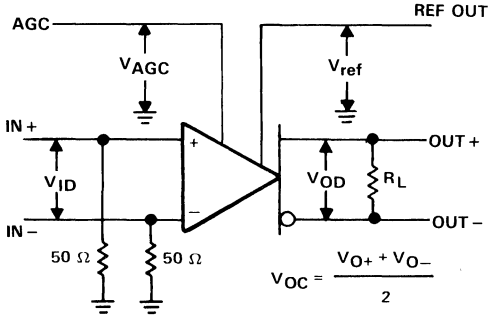


FIGURE 1

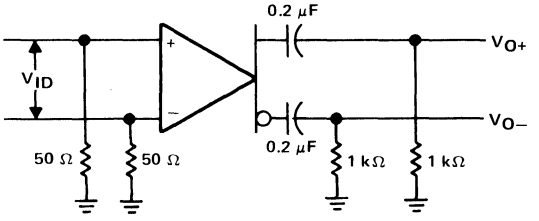


FIGURE 2

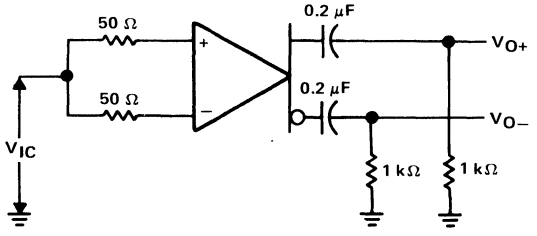


FIGURE 3

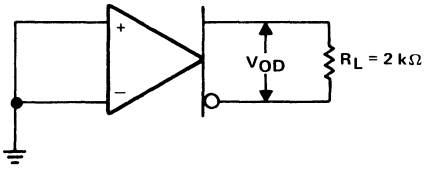


FIGURE 4

TYPICAL CHARACTERISTICS

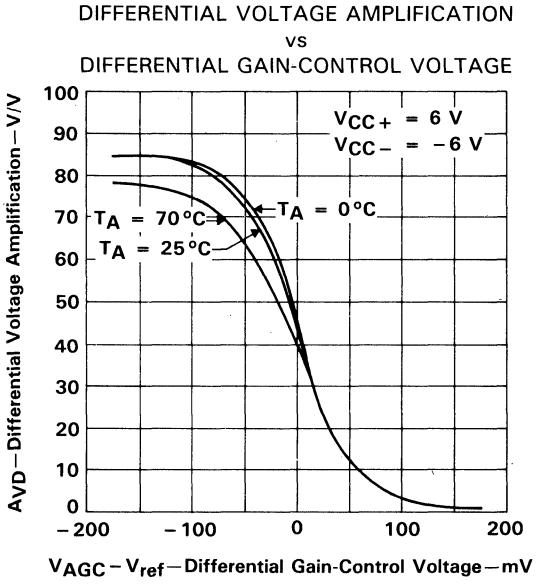


FIGURE 5

TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 shows the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL026C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 6 and 7 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC026C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 6 and 7) from the OUT output through the feedback amplifiers to the AGC input produces the following equation:

1. AC output to diode D1, assuming sinusoidal signals

$$V_o = V_{OP}\ (\sin\ (wt)) \quad (2)$$

where:

V_{OP} = peak voltage of V_o

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_C \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_C + 2 \frac{R6}{R5 + R6} V_{ref} \quad (5)$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL026C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_C \quad (6)$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7)$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL026C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 6 and 7)

The output voltage level desired must fall within the following limits.

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_C = V_{OP} - V_d$), V_C is calculated as follows:

$$V_C = 1 \text{ V} - 0.7 \text{ V}$$

$$V_C = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL026C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_C} = \frac{\Delta V_{AGC}}{V_C} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 6 and 7 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

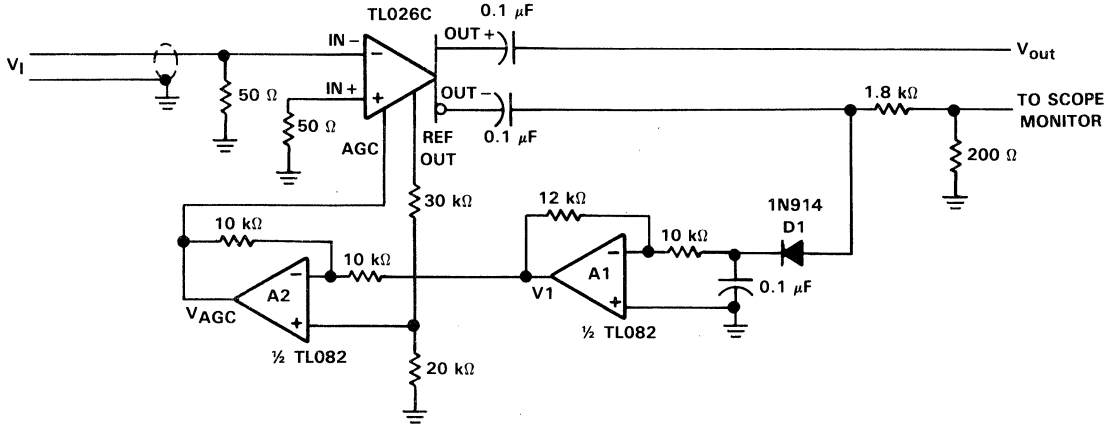
The circuit values in Figures 6 and 7 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 6 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 7 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL026C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL026C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL026C and, while the circuit is in the AGC mode, the output signal may become distorted.

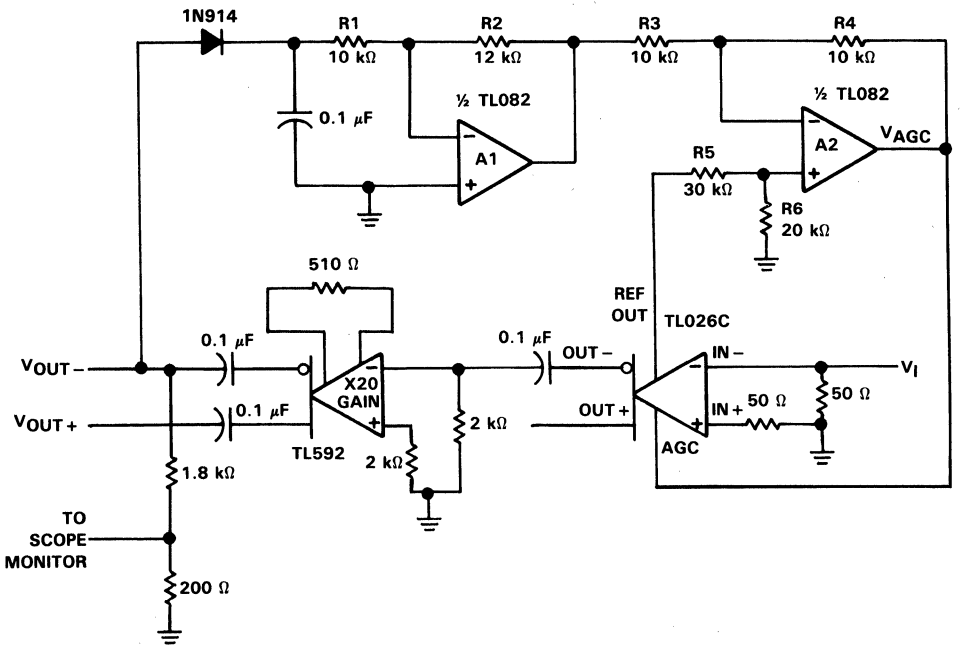
To observe the output signal of TL026C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 6 should be used.



NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 6. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



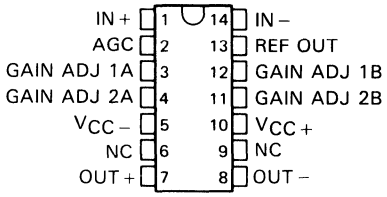
NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

D2888, JUNE 1985—REVISED JULY 1990

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D, J, OR N PACKAGE
(TOP VIEW)

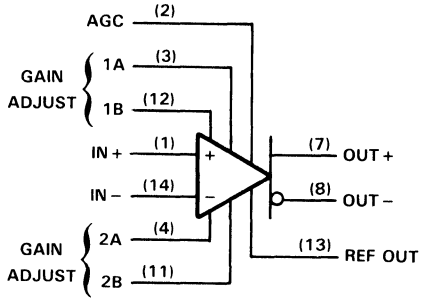


NC — No internal connection

DEVICE FEATURES

	GAIN	AGC
Gain Option 1	50 dB	50 dB
Gain Option 2	38 dB	50 dB

symbol



description

This device is a monolithic two-stage high-frequency amplifier with differential inputs and outputs. Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pins. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers for which a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL027C is characterized for operation from 0°C to 70°C. The TL027M is characterized for operation over the full military temperature range of −55°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature: TL027C . . . . . 0°C to 70°C
TL027M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	190 mW
J (C-SUFFIX)	500 mW	8.2 mW/°C	89°C	500 mW	205 mW
J (M-SUFFIX)	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
N	500 mW	9.2 mW/°C	95°C	500 mW	230 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		3	6	8	V
Supply voltage, V_{CC-}		−3	−6	−8	V
Operating free-air temperature, T_A	TL027C	0		70	°C
	TL027M	−55		125	

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	150		450	V/V
				2	55		115	
I_{IO}	Input offset current			1 or 2			6	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	2.8			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1 or 2			30	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

electrical characteristics, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, T_A = 25°C, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	200	300	400	V/V
				2	65	85	105	
ΔA_{VD1}	Change in voltage amplification	1	$V_{I(PP)}$ = 7.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	1		−50		dB
ΔA_{VD2}	Change in voltage amplification	1	$V_{I(PP)}$ = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	2		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = 1 mA to 100 μA	1	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV	1		20		MHz
				2		50		
I_{IO}	Input offset current			1 or 2		0.4	5	μA
I_{IB}	Input bias current			1 or 2		10	30	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1 or 2	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞	1 or 2			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	3	4		V
r_i	Input resistance			1		4		kΩ
				2	10	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1 or 2		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = ±1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = ±1 V	1		10.5		ns
				2		4.5	12	
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	3	4		mA
I_{CC}	Supply current		No load, No signal	1 or 2		22	27	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

PARAMETER MEASUREMENT INFORMATION

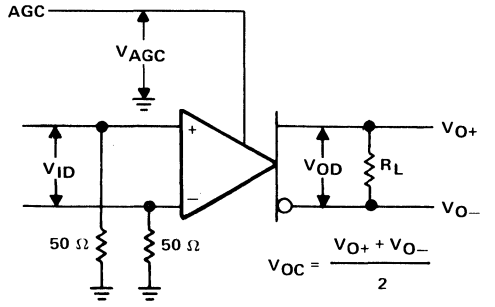


FIGURE 1

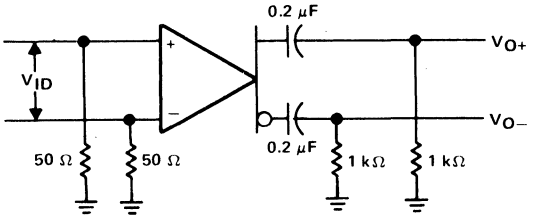


FIGURE 2

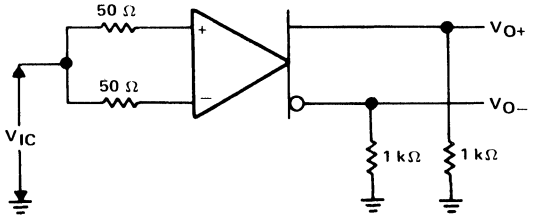


FIGURE 3

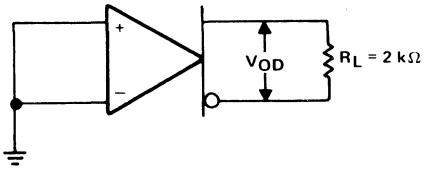


FIGURE 4

TYPICAL CHARACTERISTICS

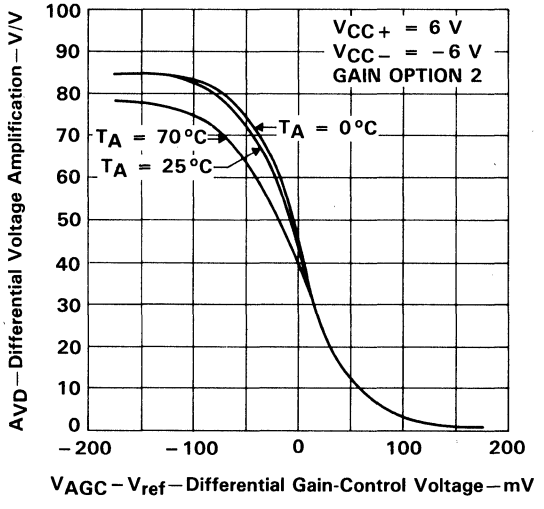


FIGURE 5

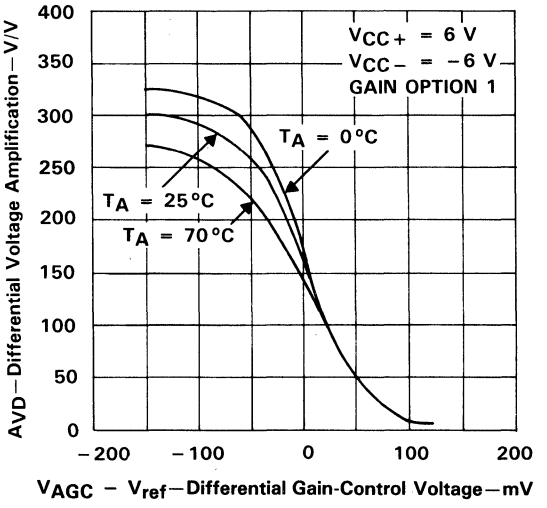


FIGURE 6

TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 and 6 show the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL027C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 7 and 8 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC027C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 7 and 8) from the OUT – through the feedback amplifiers to the AGC input produces the following equations.

1. AC output to diode D1, assuming sinusoidal signals

$$V_O = V_{OP}(\sin(\omega t)) \quad (2)$$

where:

V_{OP} = peak voltage of V_O

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_C \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_C + 2 \frac{R1}{R5 + R6} V_{ref} \quad (5)$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL027C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_C \quad (6)$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7)$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL027C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 7 and 8)

The output voltage level desired must fall within the following limits:

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_C = V_{OP} - V_d$), V_C is calculated as follows:

$$V_C = 1 \text{ V} - 0.7 \text{ V}$$

$$V_C = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL027C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_C} = \frac{\Delta V_{AGC}}{V_C} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 7 and 8 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

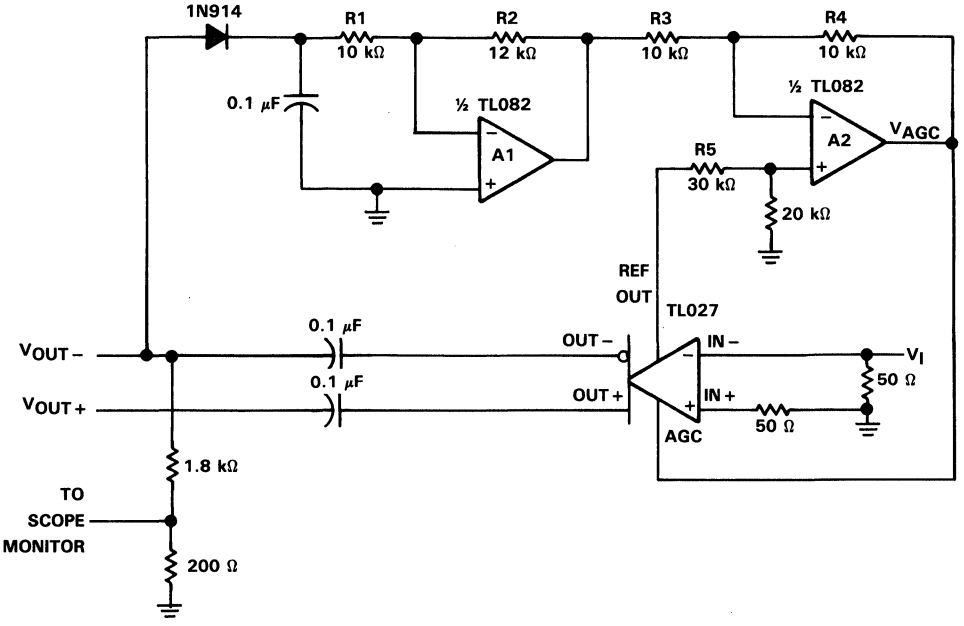
The circuit values in Figures 7 and 8 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 7 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 8 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL027C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL027C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL027C and, while the circuit is in the AGC mode, the output signal may become distorted.

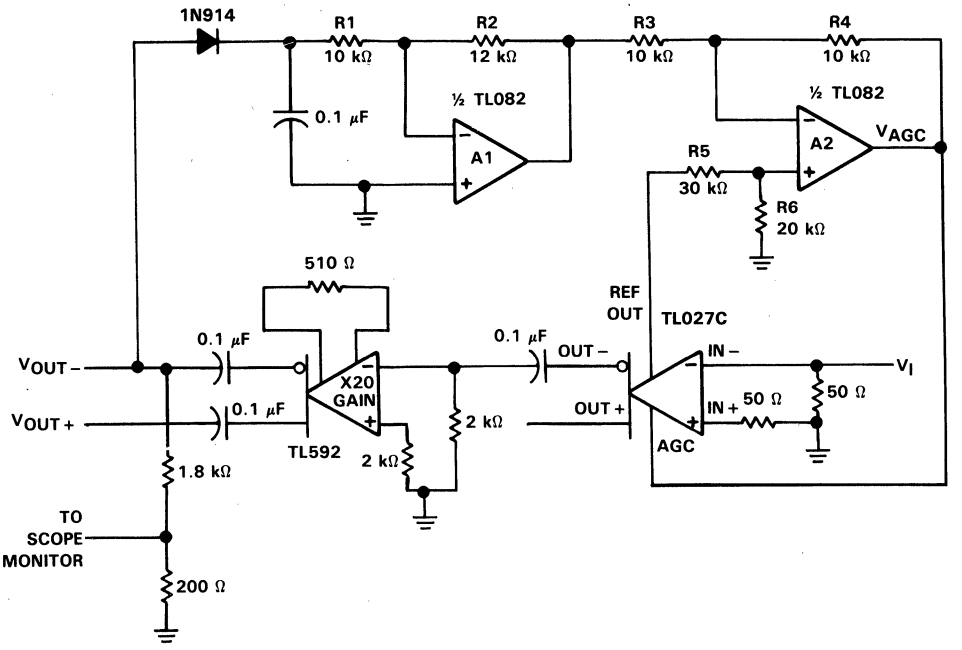
To observe the output signal of TL027C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 7 should be used.



NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On the TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



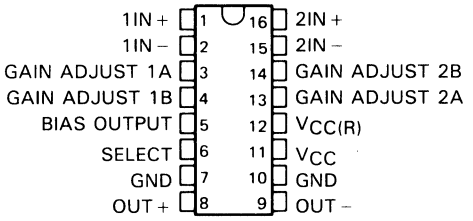
NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 8. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

D3002, MARCH 1986—REVISED DECEMBER 1988

- **Designed for Use with the TL041 Magnetic Field Pulse Detector**
- **Wide Bandwidth . . . 20 MHz Typ**
- **Low Noise . . . Less than 8 μV Typ**
- **Independently Adjustable Channel Gains . . . Up to 450 Typ**
- **No Frequency Compensation Required**
- **Internal Voltage Source Eliminates External Components**
- **Input Channel Select Pin is Compatible with TTL and CMOS**
- **Low Power Dissipation . . . 150 mW Typ**

D OR N PACKAGE
(TOP VIEW)



CHANNEL SELECT TABLE

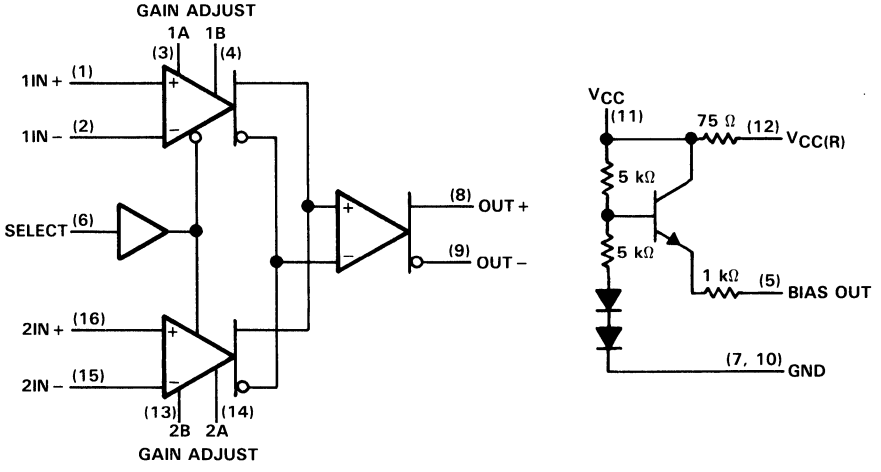
SELECT	CHANNEL
L	1
H	2

description

The TL040 is a two-channel multiplexed video amplifier designed for use with magnetic pulse detectors in streaming tape drives. The circuit design eliminates many external components, and the D package allows substantial reduction in circuit board area. The gain of each channel is a function of the resistance across its gain-adjust pins (A-B) with maximum gain occurring when the terminals are shorted.

The $V_{CC(R)}$ pin provides supply voltage decoupling required by some designs. The BIAS OUT pin provides a voltage source for other circuits that is approximately equal to 1/2 V_{CC}.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) . . . . . 14 V
Input voltage range . . . . . −0.2 V to V_{CC} + 0.2 V
Continuous total power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages except differential voltages are with respect to the ground terminals.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	10.8	12	13.2	V
Common-mode input voltage (diff inputs), V_{IC}	5	6	7	V
High-level input voltage, SELECT input, V_{IH}	2			V
Low-level input voltage, SELECT input, V_{IL}			0.8	V
Output sink current (diff outputs), I_{sink}			1.5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics of selected channel at T_A = 25°C, V_{CC} = 12 V, R_{AB} = 0, R_L = 2 kΩ (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1		300	530	600	V/V
	Channel amplification mismatch	1			1%		
	Large-signal differential voltage attenuation	1	Δ V_I = 50 mV on unselected input		60		dB
V_{OC}	Common-mode output voltage	1	R_L = ∞		8.5		V
V_{OPP}	Maximum peak-to-peak output voltage swing	1			4		V
BW	Bandwidth (−3 dB)	2			20		MHz
I_{IO}	Input offset current	1			0.1	3	μA
I_{IB}	Input bias current	1			6	17	μA
V_{OD}	Differential output voltage	1	R_L = ∞, V_{ID} = 0		0.2		V
r_i	Input resistance (differential inputs)				4		kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = 5 V to 7 V	60	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	V_{CC} = 10.8 V to 13.2 V	50	70		dB
V_n	Broadband equivalent input noise voltage	4			<5		μV
I_{IH}	High-level input current, Select input		V_{IH} = 2.7 V			−0.4	mA
I_{IL}	Low-level input current, Select input		V_{IL} = 0.4 V			20	μA
t_{pd}	Propagation delay time (differential inputs)	2	ΔV_O = 1 V		15		ns
t_r	Output rise time	2	ΔV_O = 1 V		20		ns
I_{CC}	Supply current	1			12	15	mA
	Bias output voltage	1		5	6	7	V

PARAMETER MEASUREMENT INFORMATION

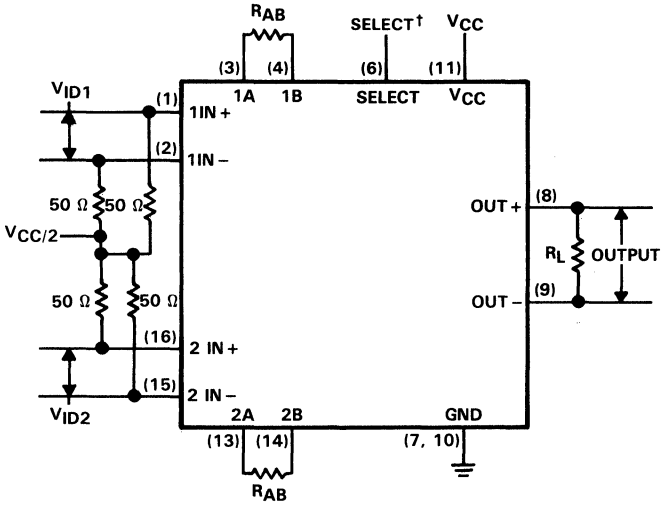


FIGURE 1

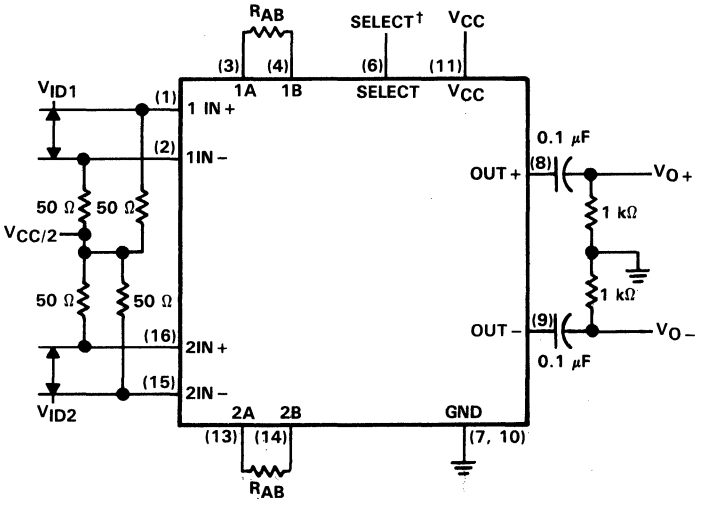


FIGURE 2

†Select input must be at proper logic level to select desired input channel.

PARAMETER MEASUREMENT INFORMATION (continued)

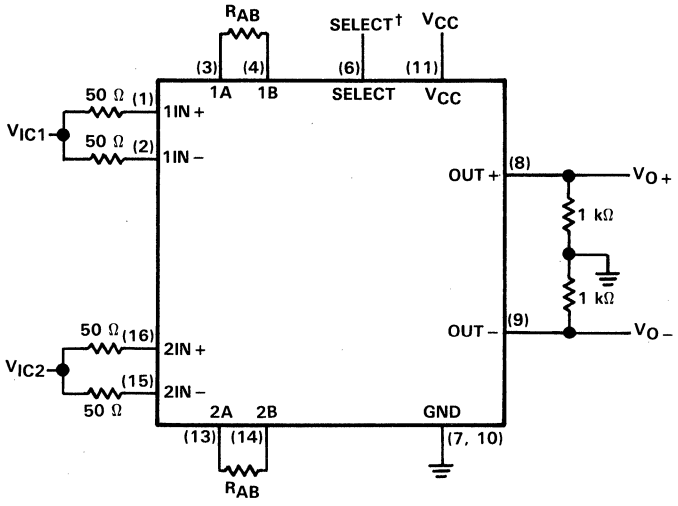


FIGURE 3

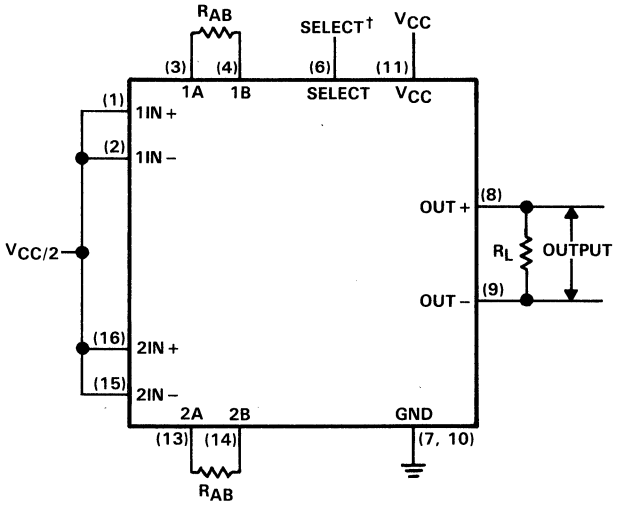


FIGURE 4

†Select input must be at proper logic level to select desired input channel.

TYPICAL CHARACTERISTICS

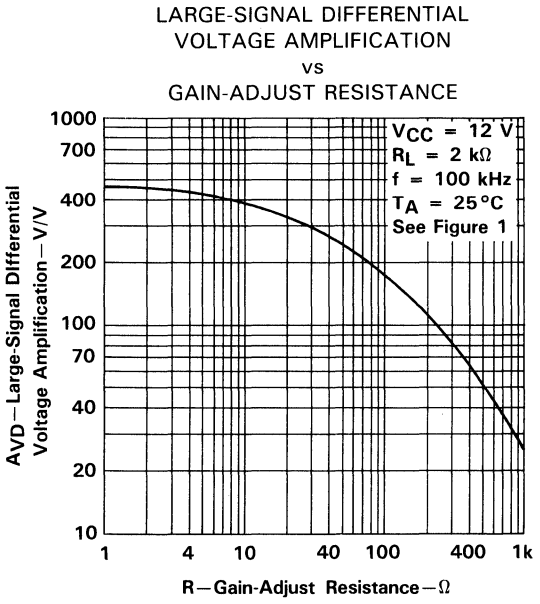


FIGURE 5

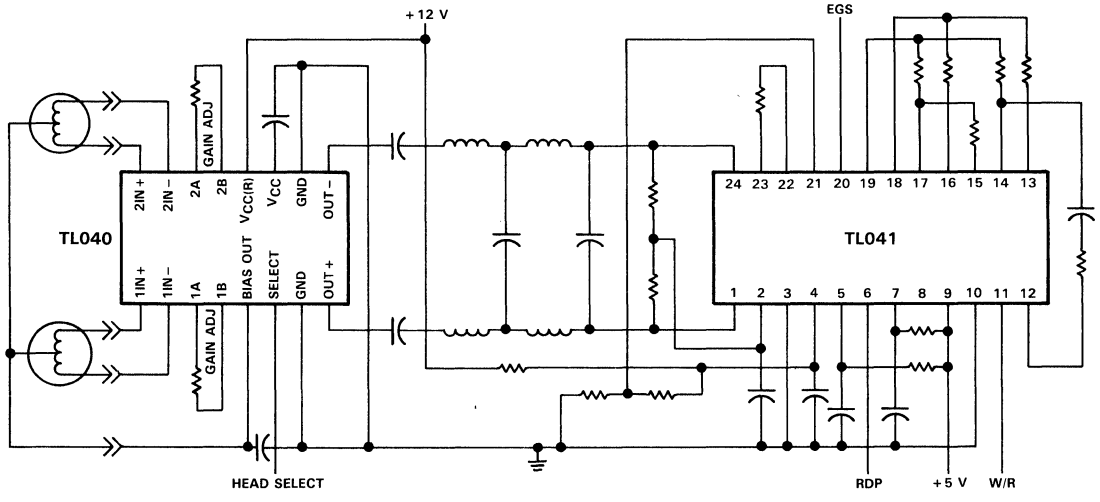
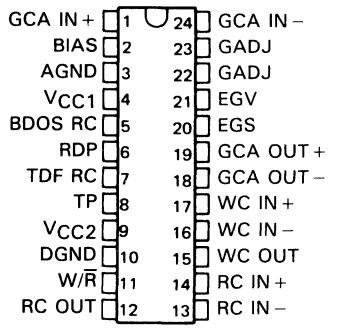


FIGURE 6. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

D3024, AUGUST 1987—REVISED SEPTEMBER 1989

- **Designed for Signal Processing in Streaming-Tape Memory Units in Combination with TL040 Two-Channel Video Amplifier**
- **Space-Saving LSI Circuits Include:**
  - **Two High-Speed Differential Comparators**
  - **Time-Domain Filter**
  - **Bidirectional One-Shot Multivibrator**
  - **Gain-Controlled Video Amplifier with Differential Inputs and Outputs**
- **Amplifier and Comparator Bandwidth . . . 20 MHz Typical**
- **Maximum Data Rate at Read Data Pulse (RDP) . . . 1.4 Mb/s Typical**
- **Available in 300-mil Dual-In-Line and "Small Outline" Plastic Packages**

DW OR NT PACKAGE
(TOP VIEW)



description

The TL041AC is a magnetic tape read signal conditioner designed for use with the TL040 video amplifier. When combined, these devices amplify the low-signal output from a streaming-tape playback head and reconstruct the data as originally written on the tape. The TL041AC includes a gain-controlled amplifier, two comparators, read/write select logic, a time-domain filter, and a bidirectional one-shot multivibrator.

The amplifier has differential inputs, differential outputs, and electronic gain control. A special feature of the electronic gain control is the Electronic Gain Select (EGS). When the EGS input is high, the Electronic Gain Voltage (EGV) input is driven low and amplifier gain is determined by the value of the resistor connected between the Gain Adjust (GADJ) pins. When the EGS input is low, the gain set by the resistor is increased by an amount determined by the voltage applied to the EGV pin.

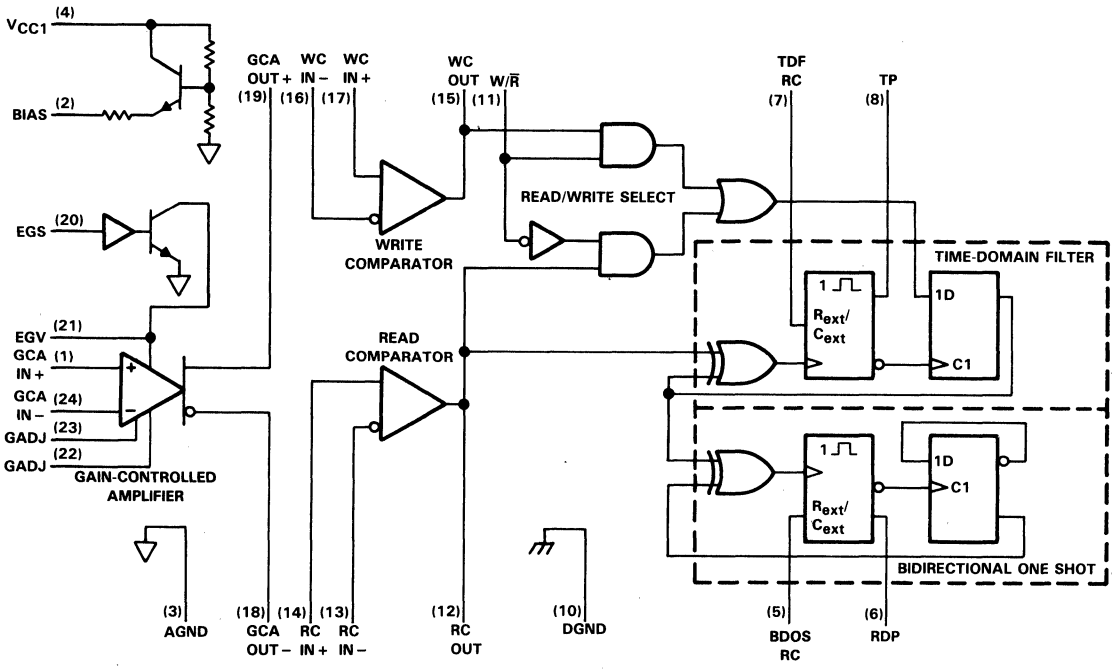
To accommodate different magnetic tape output signal levels, the amplifier gain may be switched by logic at the EGS input, controlled manually with an adjustable voltage at the EGV input, or automatically adjusted with an automatic gain control (AGC) circuit applying a control voltage to the EGV input.

The comparator functions are controlled by a logic input to the Write/Read (W/$\overline{R}$) select input. With the W/$\overline{R}$ input low, the read comparator output (usually connected as a zero-crossing detector) is sent to the time-domain filter. When W/$\overline{R}$ is high, the write comparator output is used to provide write amplitude verification in a typical read-after-write function.

The time-domain filter helps to ensure the input data is valid. A capacitor in series with a resistor, connected to the time-domain filter pin (TDF RC), begins charging at the leading edge of an input pulse from the read comparator. If the input pulse does not remain high for one RC time constant, the pulse is considered invalid and no signal is passed to the bidirectional one-shot multivibrator (BDOS). However, if the input pulse remains high for longer than one RC time constant, the pulse is considered valid and the signal is passed through the time-domain filter to trigger the BDOS. When triggered, the BDOS provides a pulse to the Read Data Pulse (RDP) output. The RDP output pulse duration is determined by a resistor-capacitor network connected to the BDOS RC pin.

The TL041AC is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

INPUT CONDITONS			I/O NAME	I/O CONDITION
EGS	W/R̄	DIFFERENTIAL INPUTS WRITE OR READ COMPARATOR		
	X	RC IN+ > RC IN−	RC OUT	H
	X	RC IN− > RC IN+	RC OUT	L
	L	X	RC OUT	Input to time-domain filter
	X	WC IN+ > WC IN−	WC OUT	H
	X	WC IN− > WC IN+	WC OUT	L
	H	X	WC OUT	Input to time-domain filter
H		X	EGV	L
L		X	EGV	Input

PIN NAME	PIN NO.	DESCRIPTION
AGND	3	Analog ground
BDOS RC	5	Bidirectional one-shot resistor and capacitor
BIAS	2	Output bias voltage
DGND	10	Digital ground
EGS	20	Electronic gain select
EGV	21	Electronic gain voltage
GCA IN−	24	Gain-controlled amplifier, inverting input
GCA IN+	1	Gain-controlled amplifier, noninverting input
GADJ	22	Gain adjust
GADJ	23	Gain adjust
GCA OUT−	18	Gain-controlled amplifier, inverting output
GCA OUT+	19	Gain-controlled amplifier, noninverting output
RC IN−	13	Read comparator, inverting input
RC IN+	14	Read comparator, noninverting input
RC OUT	12	Read comparator out
RDP	6	Read data pulse
TDF RC	7	Time-domain filter resistor and capacitor
TP	8	Test point
V_{CC1}	4	Analog collector supply voltage
V_{CC2}	9	Digital collector supply voltage
WC IN−	16	Write comparator, inverting input
WC IN+	17	Write comparator, noninverting input
WC OUT	15	Write comparator out
W/$\overline{R}$	11	Write/read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC1} (see Note 1) . . . . . 14 V
V_{CC2} . . . . . 7 V
Input voltage range: Amplifier and comparators . . . . . AGND − 0.2 V to V_{CC1} + 0.2 V
Multivibrators and logic . . . . . AGND − 0.2 V to V_{CC2} + 0.2 V
Input current: EGV (see Note 2) . . . . . ±2 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages except differential voltages are with respect to network ground terminals (AGND and DGND tied together).
2. Driving EGV high from a low-impedance source (> ±2 mA capability) with EGS high can result in damage to the device.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW/°C
NT	1700 mW	13.6 mW/°C	1088 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
High-level input voltage, V_{IH}	EGS or W/$\overline{R}$	2			V
Low-level input voltage, V_{IL}	EGS or W/$\overline{R}$			0.8	V
Input voltage, V_I	EGS	0		10	V
	EGV	0		$0.8V_{CC1}$	
Common-mode input voltage to gain-control amplifier, V_{IC}			4		V
High-level output current, I_{OH}	WC OUT, RC OUT, TP, or RDP			−400	μA
Low-level output current, I_{OL}	WC OUT, RC OUT, TP, or RDP			8	mA
Pulse duration, t_w	TP or RDP	40			ns
External timing resistance, (see Note 3)	TDF or BDOS RC	5		25	kΩ
External timing capacitance	TDF or BDOS RC)	0.01	0.1	1000	nF
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Some high resistance and capacitance combinations may produce abnormal output waveforms.

electrical characteristics at V_{CC1} = 12 V, V_{CC2} = 5 V, $V_{IC(GIC)}$ = V_{bias}, R_{ADJ} = 5 kΩ, EGS at high level, EGV at 0 V, r_i = 50 Ω, R_L = 2 kΩ, T_A = 25°C (unless otherwise noted)

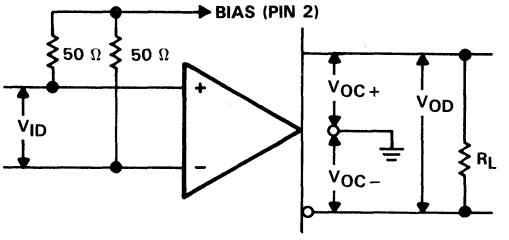
gain-controlled amplifier

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	1	V_{ID} = 0,	V_{OD} = V_O		0.35	0.75	V
V_{OPP}	Maximum differential output voltage	1	V_{ID} = 1 V,	V_{OPP} = V_O	3	6		V
A_{VD}	Large-signal differential voltage amplification	1	V_{ID} = 20 mV,	EGS high	8	14	20	V/V
			V_{id} = 20 mV, EGS low, f = 455 kHz	EGV at 4 V		19		V/V
				EGV at 9.6 V		90		
CMRR	Common-mode rejection ratio	2	V_{IC} = 2 V to 5 V		60	80		dB
V_{IC}	Common-mode input voltage	2			2		5	V
V_{OC}	Common-mode output voltage	1	V_{ID} = 0		4	5.8	6.4	V
I_{IO}	Input offset current	1	I_{IB+} − I_{IB-}			0.2	3	μA
I_O	Output current, sink				1.5	2		mA
I_{IB}	Input bias current	1	(I_{IB+} + I_{IB-})/2			5	17	μA
$V_{O(BIAS)}$	Bias output voltage	1			3	4	5	V
$z_{o(BIAS)}$	Bias output impedance					1		kΩ
z_i	Input impedance					30		kΩ
BW	Bandwidth (−3 dB)	3				20		MHz
k_{SVR}	Supply voltage rejection ratio	4	V_{CC1} = 10.8 V to 13.2 V		50	70		dB
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	No signal		32	45	mA

logic section

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC2} = 4.5 V, I_{OH} = −400 μA	V_{ID} = 0.1 V,	2.7	3.5		V
V_{OL}	Low-level output voltage			V_{CC2} = 4.5 V, I_{OL} = 8 mA	V_{ID} = 0.1 V,		260	500	mV
V_{ICR}	Common-mode input voltage, comparators					2		7	V
I_{IH}	High-level input current	EGS		$V_{I(EGS)}$ = 2.7 V			120	200	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 2.7 V				20	
I_{IL}	Low-level input current	EGS		$V_{I(EGS)}$ = 0.4 V				−20	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 0.4 V				−400	
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 5.5 V,	No signal		22	31	mA
	Response time			100-mV step,	5-mV overdrive		50		ns
t_w	Pulse duration of one-shots (TP, RDP)			R_{ext} = 5 kΩ,	C_{ext} = 100 pF		360		ns
				R_{ext} = 20 kΩ,	C_{ext} = 33 pF		460		

PARAMETER MEASUREMENT INFORMATION



$V_{OO} = V_{OD}$ with $V_{ID} = 0$

$V_{OPP} = V_{OD}$ with $V_{ID} = 1$ V

$A_{VD} = \frac{V_{OD}}{V_{ID}}$ with $V_{ID} = 20$ mV

$V_{OC} = \frac{V_{OC+} + V_{OC-}}{2}$ with $V_{ID} = 0$

FIGURE 1

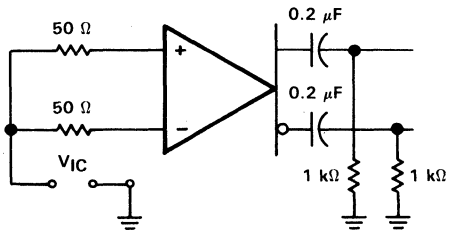


FIGURE 2

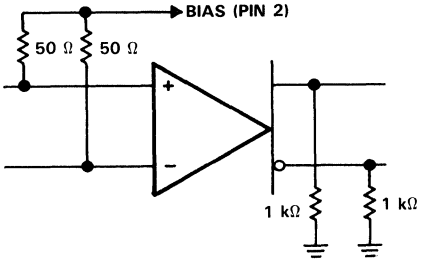


FIGURE 3

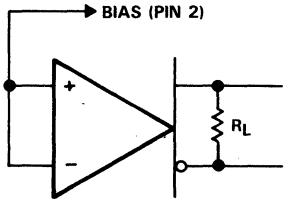


FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

READ DATA PULSE DURATION
vs
CAPACITANCE

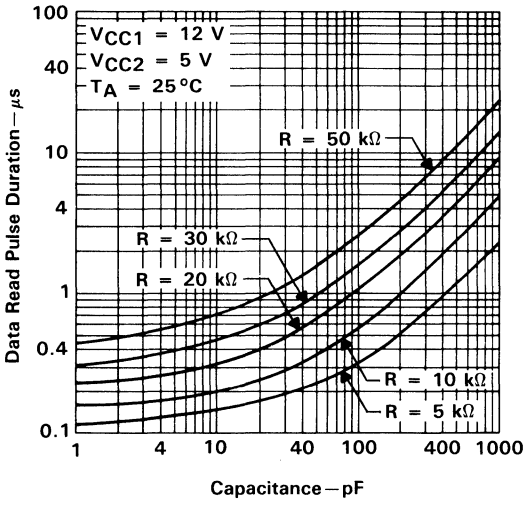


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
ELECTRONIC GAIN VOLTAGE

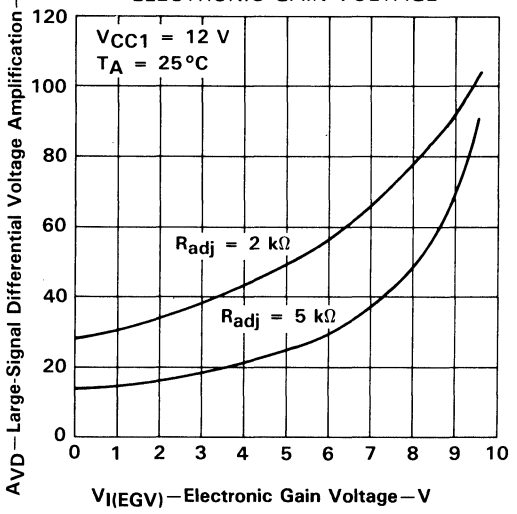


FIGURE 6

TYPICAL APPLICATION DATA

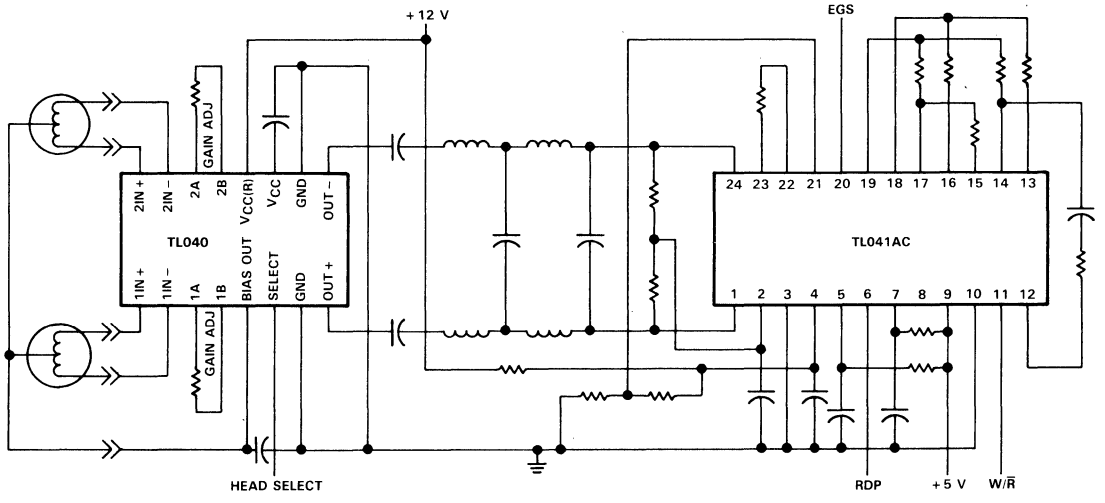


FIGURE 7. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

D956, JUNE 1976—REVISED FEBRUARY 1989

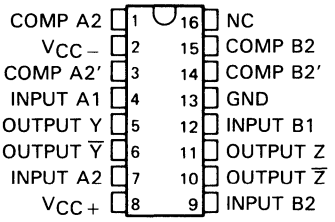
- **Excellent Dynamic Range**
- **Wide Bandwidth**
- **Built-In Temperature Compensation**
- **Log Linearity (30 dB Sections) . . . 1 dB Typ**
- **Wide Input Voltage Range**

description

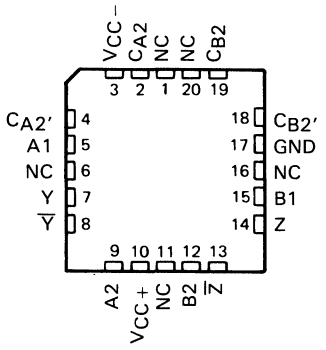
This monolithic amplifier circuit contains four 30-dB logarithmic stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dB input voltage range. Each half of the circuit contains two of these 30-dB stages summed together in one differential output that is proportional to the sum of the logarithms of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dB. In practice, this permits the input voltage range to be typically greater than 80 dB with log linearity of ± 0.5 dB (see application data). Bandwidth is from dc to 40 MHz.

This circuit is useful in military weapons systems, broadband radar, and infrared reconnaissance systems. It serves for data compression and analog compensation. This logarithmic amplifier is used in log IF circuitry as well as video and log amplifiers. The TL441AM is characterized for operation over the full military temperature range of −55°C to 125°C.

J PACKAGE
(TOP VIEW)

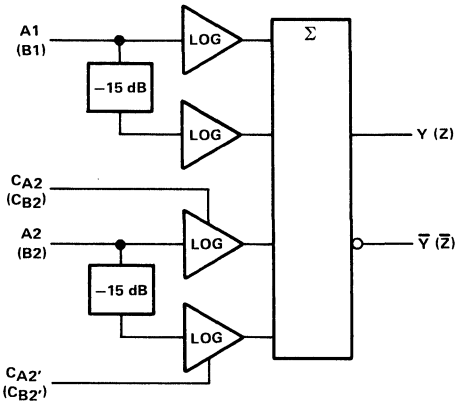


FK PACKAGE
(TOP VIEW)



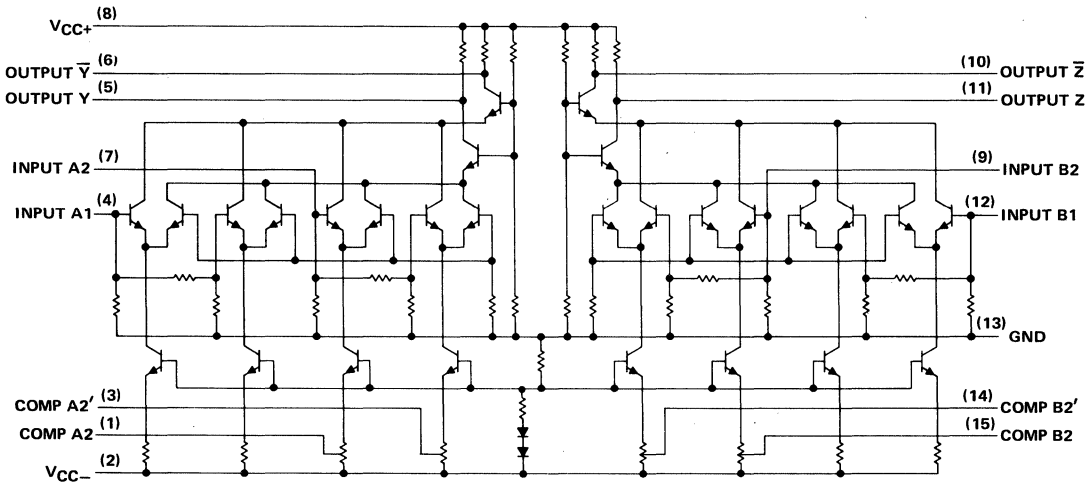
NC—No internal connection

functional block diagram (one half)



Y ∝ log A1 + log A2; Z ∝ log B1 + log B2
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$ are detector compensation inputs.

schematic



Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1): V_{CC+} . . . . . 8 V
V_{CC-} . . . . . −8 V
Input voltage (see Note 1) . . . . . 6 V
Output sink current (any one output) . . . . . 30 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE: 1. All voltages, except differential output voltages, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
J	500 mW	11.0 mW/°C	104°C	500 mW	275 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Peak-to-peak input voltage for each 30-dB stage	0.01		1	V
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage	1		±25	±70	mV
Quiescent output voltage	2	5.45	5.6	5.85	V
DC scale factor (differential output), each 3-dB stage, −35 dBV to −5 dBV	3	7	8	11	mV/dB
AC scale factor (differential output)			8		mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2.6	dB
Input impedance			500		Ω
Output impedance			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	35	ns
Supply current from V_{CC+}	2	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	mW

electrical characteristics over operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage		1			±100	mV
Quiescent output voltage		2	5.3		5.85	V
DC scale factor (differential output) each 30-dB stage, −35 dBV to −5 dBV		3	7		11	mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	T_A = −55°C	3			4	dB
	T_A = 125°C				3	
Supply current from V_{CC+}		2	10		31	mA
Supply current from V_{CC-}		2	−4.5		−15	mA
Power dissipation		2	87		276	mW

PARAMETER MEASUREMENT INFORMATION

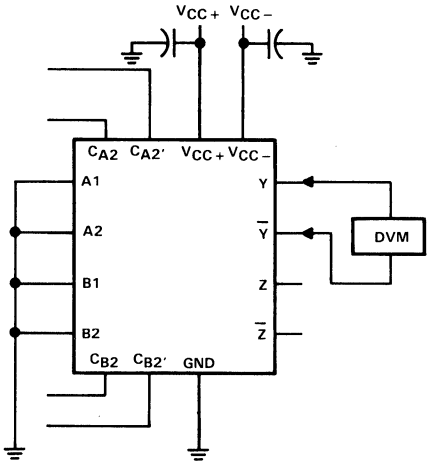


FIGURE 1

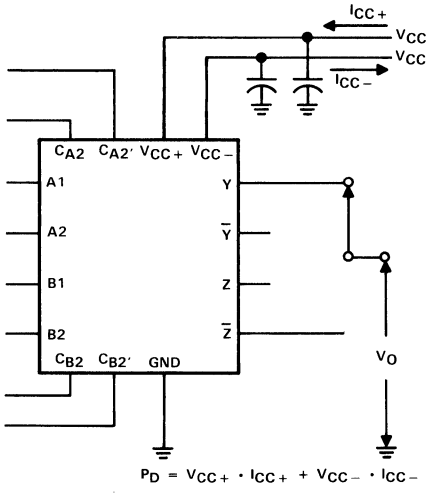
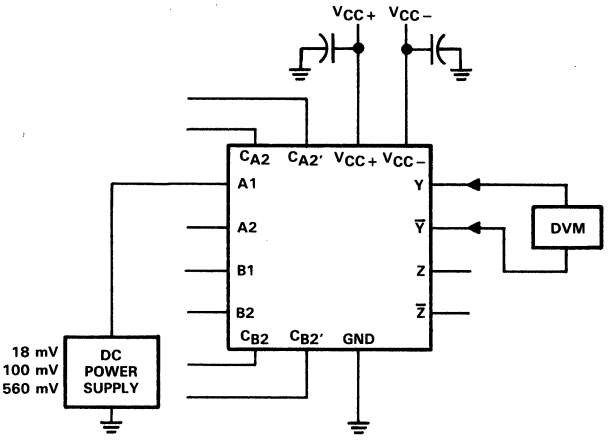


FIGURE 2

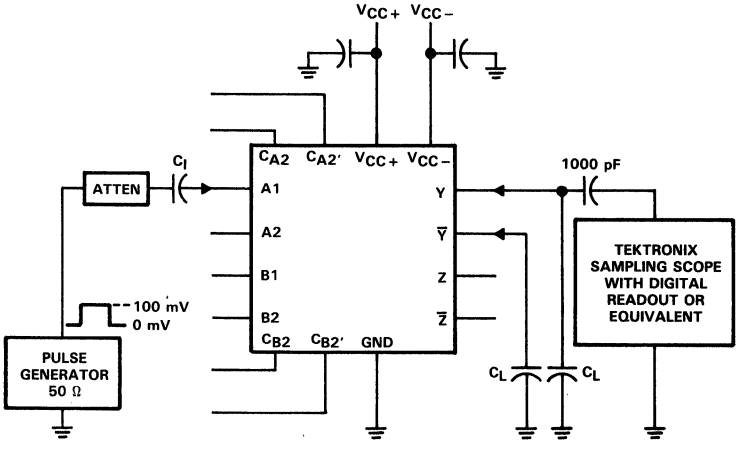
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dB}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_w = 200 ns, $t_r \leq 2$ ns, $t_f \leq 2$ ns, PRR ≤ 10 MHz.
B. Capacitor C_i consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.
C. C_L includes probe and jig capacitance.

FIGURE 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

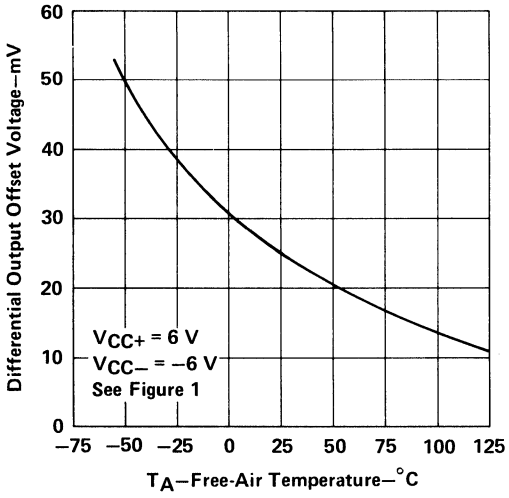


FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

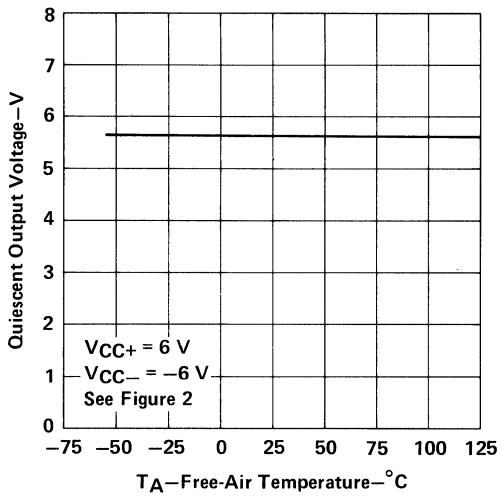


FIGURE 6

DC SCALE FACTOR
vs
FREE-AIR TEMPERATURE

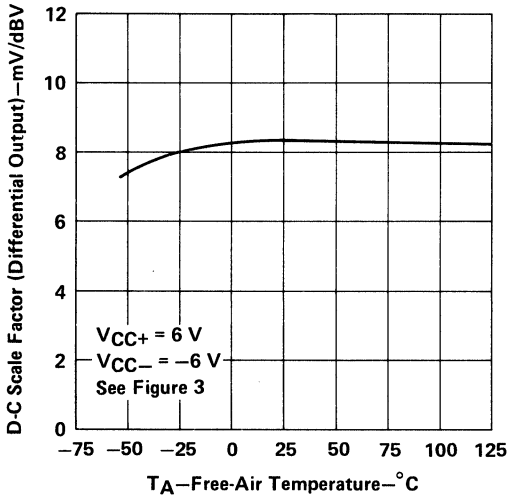


FIGURE 7

DC ERROR
vs
FREE-AIR TEMPERATURE

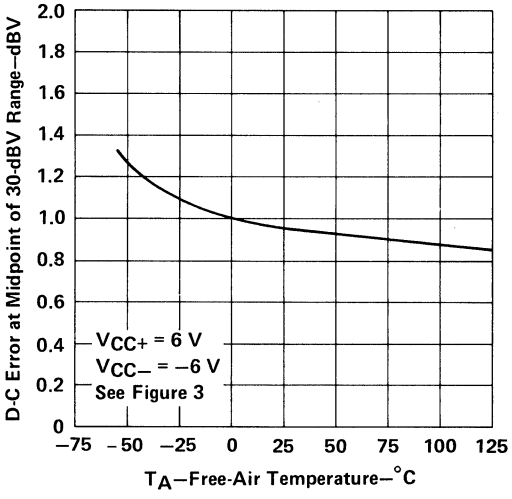


FIGURE 8

TYPICAL CHARACTERISTICS

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

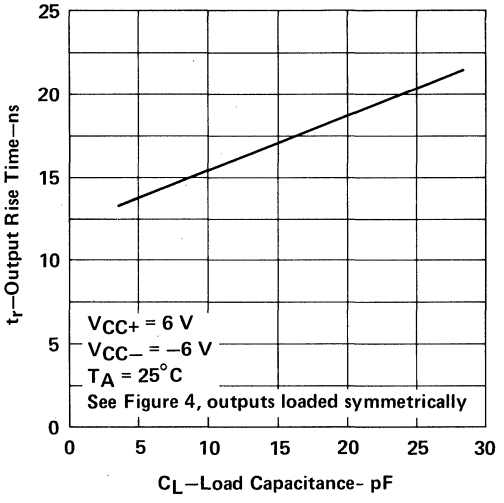


FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

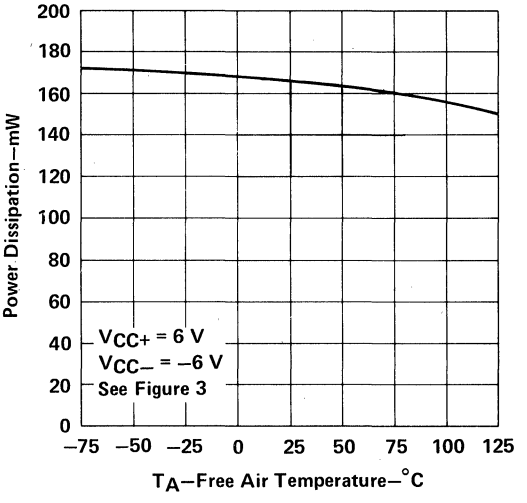


FIGURE 10

TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic logarithmic function

The basic logarithmic response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where:

I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to common-mode noise.

functional block diagram

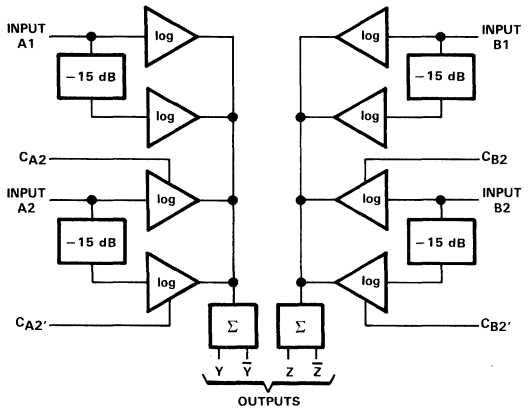


FIGURE 11

logarithmic sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dB log subsection, and each input feeds two pairs for a range of 30-dB per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dB stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dB stage can be adjusted to match the other 15-dB stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 V to 1 V. Input levels in excess of 1 V may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 V, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 V to ensure a clean output.

output levels

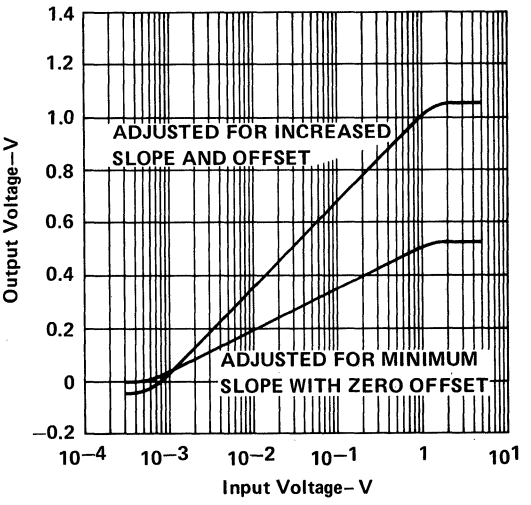
Differential-output-voltage levels are low, generally less than 0.6 V. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using this logarithmic amplifier. Operational amplifiers not otherwise designated are TLC271. For operation at higher frequencies, the TL592 is recommended instead of the TLC271.

TYPICAL TRANSFER
CHARACTERISTICS



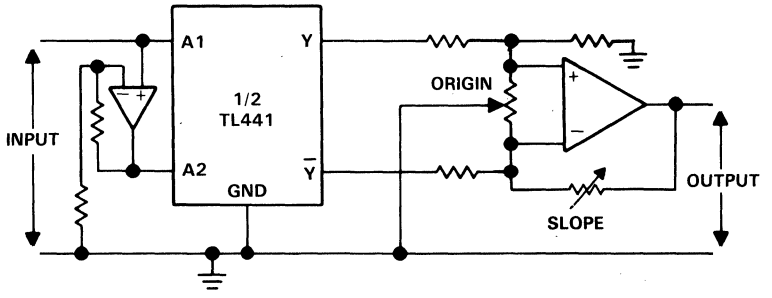
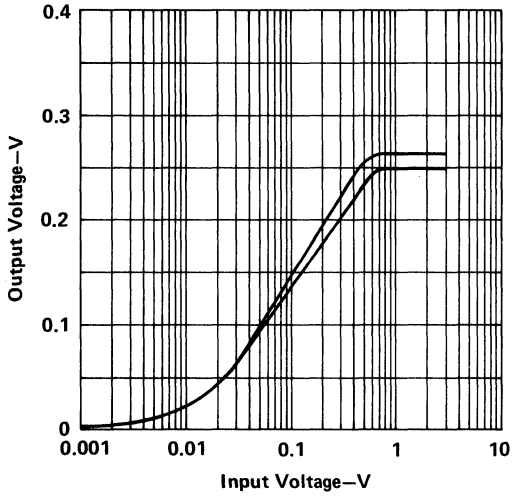


FIGURE 12. OUTPUT SLOPE AND ORIGIN ADJUSTMENT

TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
OF TWO TYPICAL INPUT STAGES



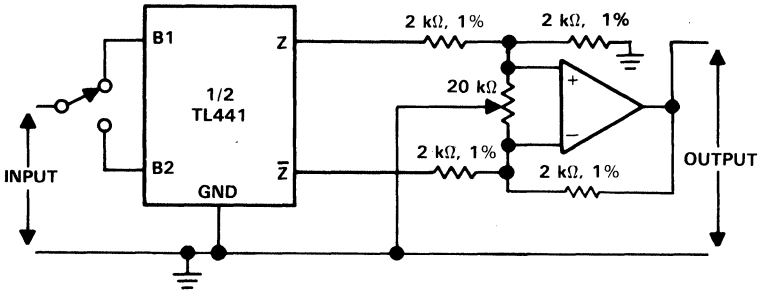
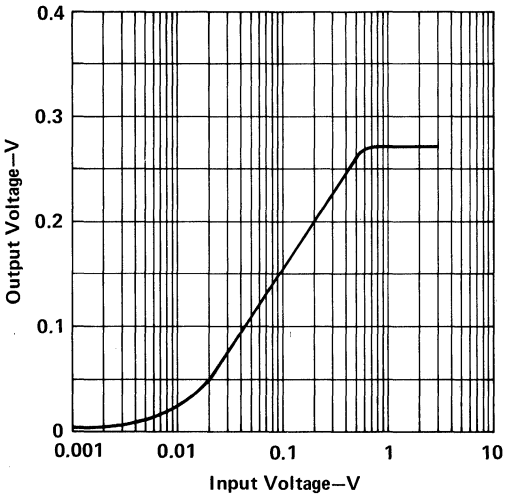


FIGURE 13. UTILIZATION OF SEPARATE STAGES

TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
WITH BOTH SIDES PARALLELED



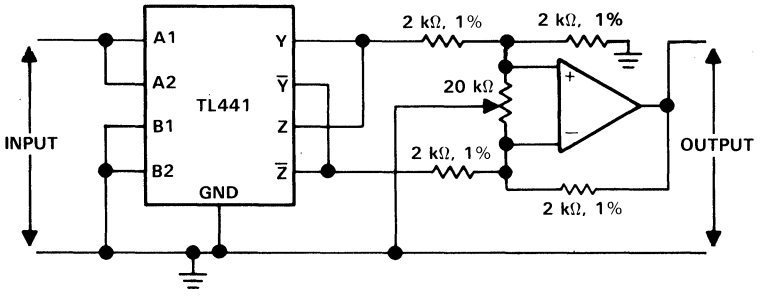
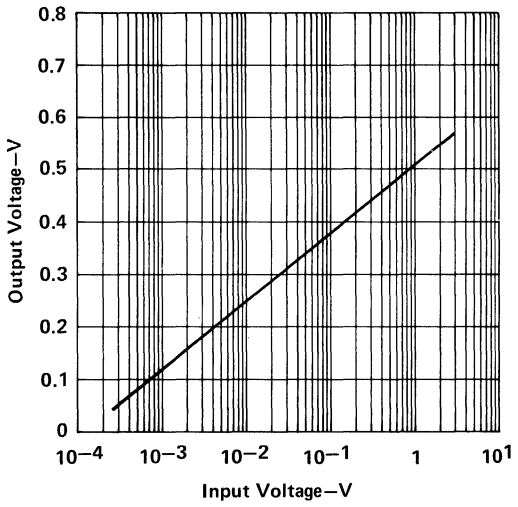
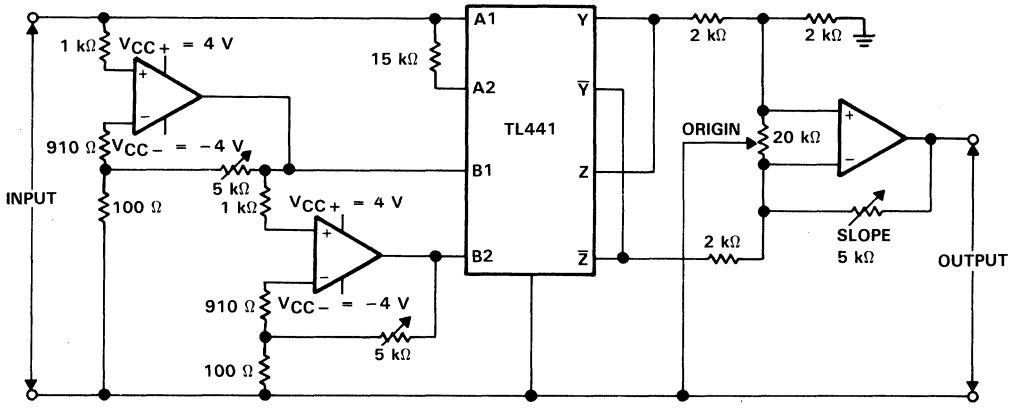


FIGURE 14. UTILIZATION OF PARALLELED INPUTS

TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS

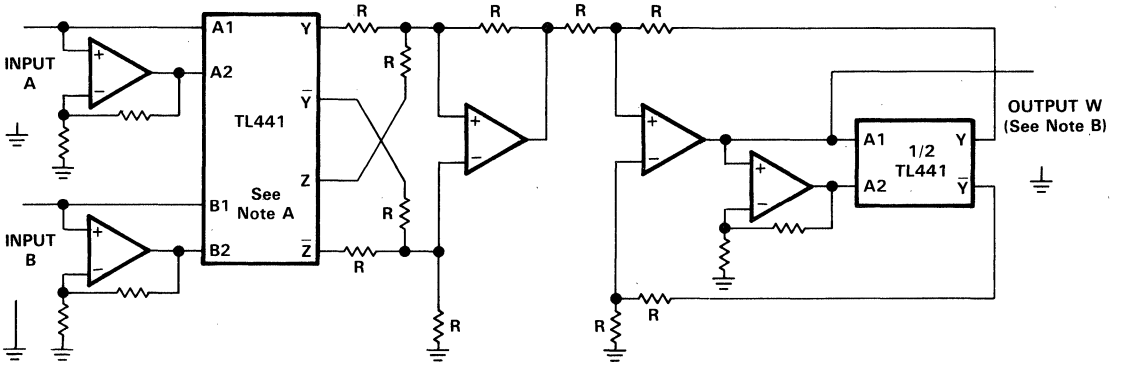




NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transistions.

Figure 15. LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dB

TYPICAL APPLICATION DATA

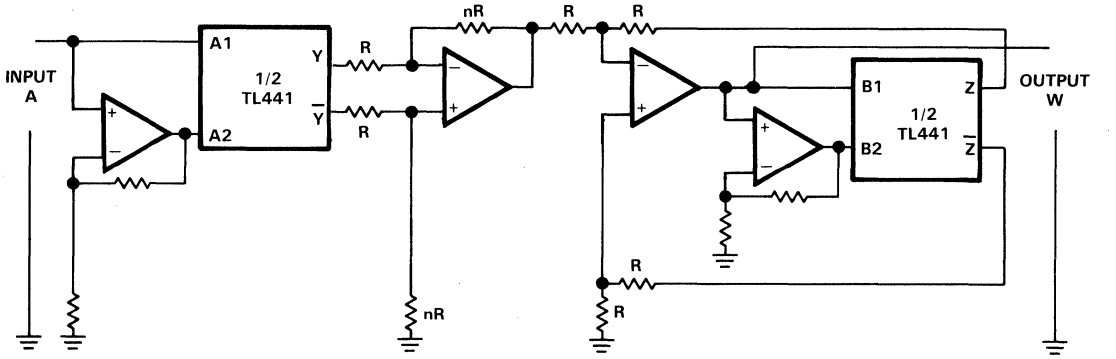


NOTES: A. Connections shown are for multiplication. For division, Z and $\overline{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A + \log_a B)}$

FIGURE 16. MULTIPLICATION OR DIVISION

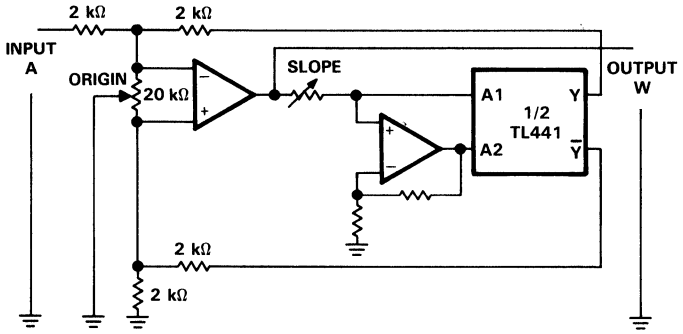


NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17. RAISING A VARIABLE TO A FIXED POWER

TYPICAL APPLICATION DATA



NOTE: Adjust the slope to correspond to the base "a".
Exponential to any base: W = a

FIGURE 18. RAISING A FIXED NUMBER TO A VARIABLE POWER

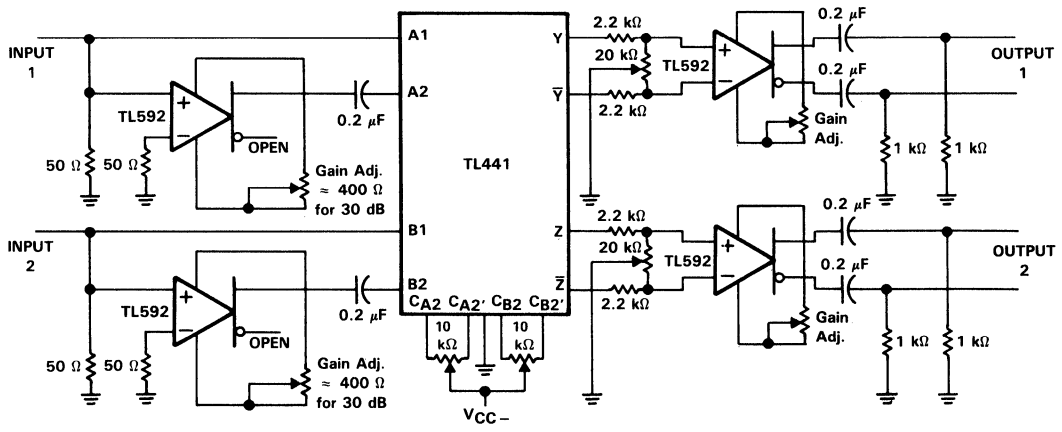
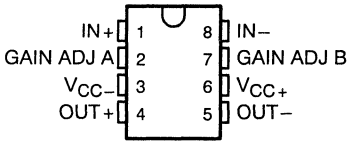


FIGURE 19. DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

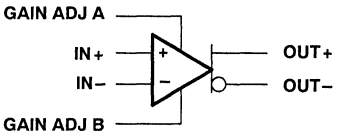
D2668, NOVEMBER 1983–REVISED NOVEMBER 1991

- **8-Pin Version of NE592 . . . Saves Printed Circuit Board Space**
- **Adjustable Gain to Typically 400 V/V**
- **No Frequency Compensation Required**
- **Adjustable Pass Band**
- **A_{VD} Range . . . 250–600 V/V**

D OR P PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs.

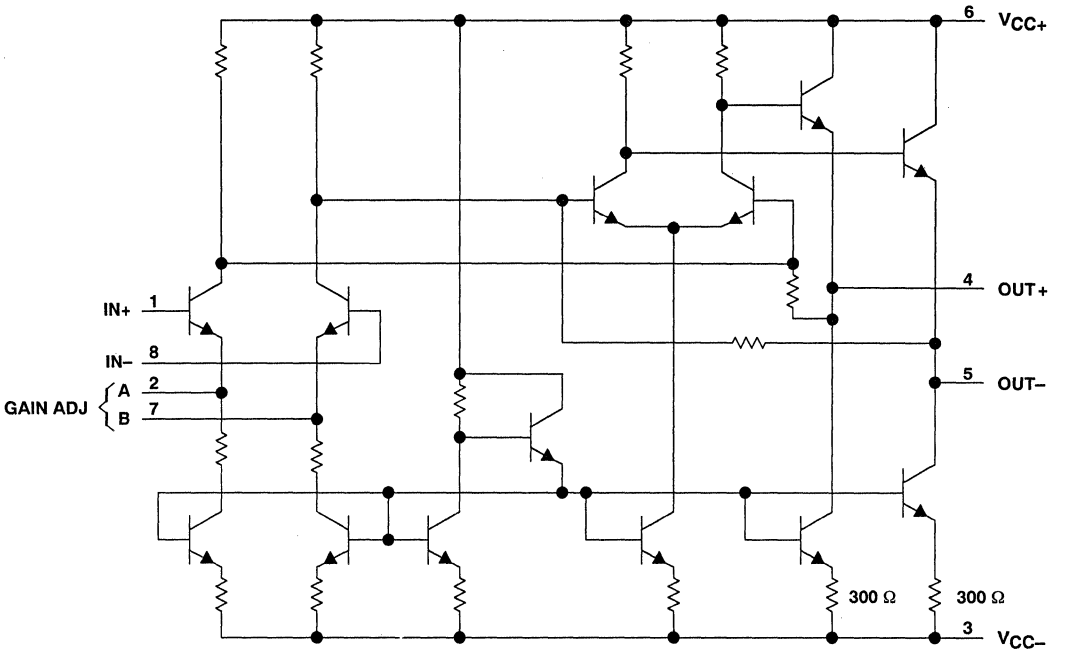
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of nominally 400 V/V can be selected without external components, or amplification may be adjusted from 0 to approximately 400 V/V by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The TL592 is characterized for operation from 0°C to 70°C.

schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation at 70°C . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		T_A†	GAIN OPTION‡	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ		25°C	1	250	400	600	V/V
					Full range		250		600	
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V		25°C	1		50		MHz
I_{IO}	Input offset current		V_{IC} = 0		25°C	1 or 2		0.4	5	μA
					Full range				6	
I_{IB}	Input bias current		V_{IC} = 0		25°C	1 or 2		9	30	μA
					Full range				40	
V_{ICR}	Common-mode input voltage	3			25°C	1 or 2	±1			V
					Full range		±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞		25°C	2		0.35	0.75	V
					Full range				1.5	
$V_{O(PP)}$	Peak-to-peak output voltage swing	1	R_L = 2 kΩ		25°C	1	3	4		V
					Full range		2.8			
z_i	Input impedance		V_{OD} = 1 V, f = 1 kHz to 10 MHz		25°C	1		4		kΩ
					Full range			3.6		
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V	f = 100 kHz	25°C	1	60	86		dB
				f = 5 MHz				60		
				f = 100 kHz	Full range		50			
				f = 5 MHz				60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V		25°C	1	50	70		dB
					Full range		50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C	1 or 2		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C	2		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C	2		10.5		ns
$I_{sink(max)}$	Maximum output sink current					1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal		25°C	1 or 2		18	24	mA
					Full range				27	

† Full range is 0°C to 70°C.
‡ The gain option is selected as follows:
Gain Option 1 . . . Gain adjust pin A is connected to pin B.
Gain Option 2 . . . Gain adjust pins A and B are open.

PARAMETER MEASUREMENT INFORMATION

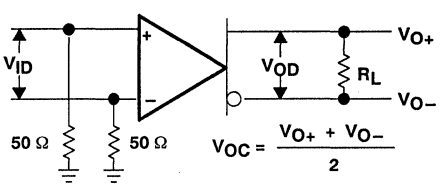


Figure 1

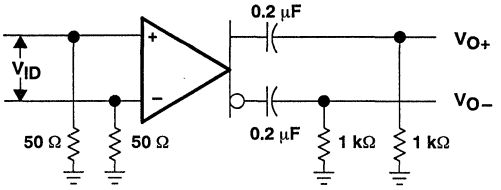


Figure 2

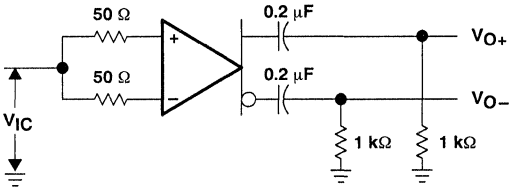


Figure 3

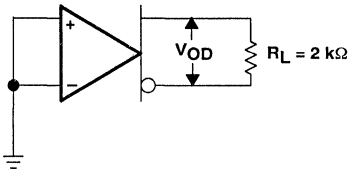


Figure 4

D2668, JUNE 1985—REVISED APRIL 1988

- **Adjustable Gain to 400 Typ**
- **No Frequency Compensation Required**
- **Low Noise . . . 3 μV Typ V_n**

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

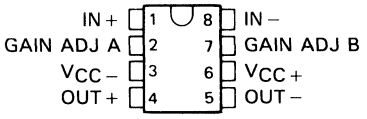
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted from near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

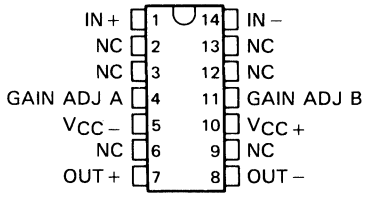
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

D8† OR P PACKAGE
(TOP VIEW)



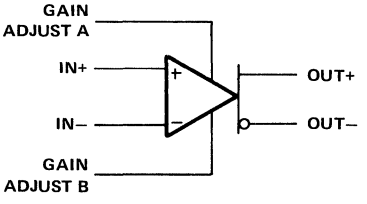
D14† OR N PACKAGE
(TOP VIEW)



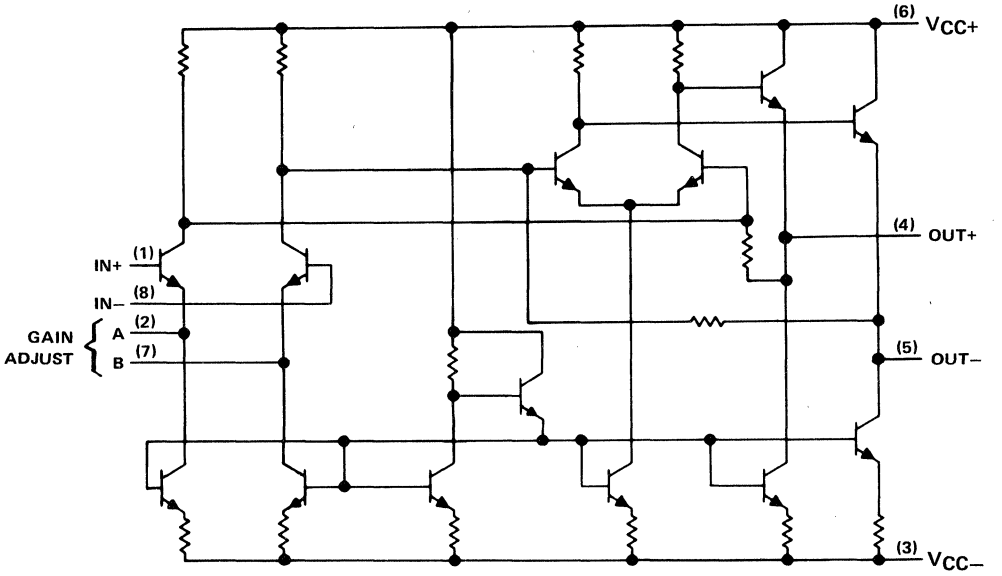
NC—No internal connection

†D8 and D14 are the codes used to differentiate the 8-pin and 14-pin versions, respectively.

symbol



schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D8	530 mW	5.8 mW/°C	59°C	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 0	R_L = 2 kΩ,	25°C	300	400	500	V/V
					0°C to 70°C	250		600	
A_{VD2}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 1 kΩ	R_L = 2 kΩ,	25°C		13		V/V
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V,	R_{AB} = 0	25°C		50		MHz
I_{IO}	Input offset current				25°C		0.4	5	μA
					0°C to 70°C			6	
I_{IB}	Input bias current				25°C		9	30	μA
					0°C to 70°C			40	
V_{ICR}	Common-mode input voltage range	3			25°C	±1			V
					0°C to 70°C	±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_{AB} = ∞, R_L = ∞		25°C		0.35	0.75	V
					0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ	R_{AB} = 0	25°C	3	4		V
					0°C to 70°C	2.8			
r_i	Input resistance		V_{OD} = 1 V,	R_{AB} = 0	25°C		4		kΩ
					0°C to 70°C		3.6		
r_o	Output resistance				0°C to 70°C			30	Ω
C_i	Input capacitance				25°C		5		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, R_{AB} = 0	f = 100 kHz	25°C	60	86		dB
				f = 5 MHz			60		
				f = 100 kHz	0°C to 70°C	50			
				f = 5 MHz			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V, R_{AB} = 0		25°C	50	70		dB
					0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V,	V_O = 3 V		3	4		mA
I_{CC}	Supply current		No load,	No signal	25°C		18	24	mA
					0°C to 70°C			27	

†R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

PARAMETER MEASUREMENT INFORMATION

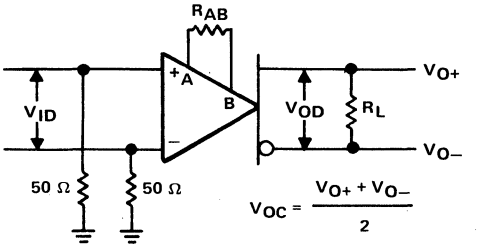


FIGURE 1

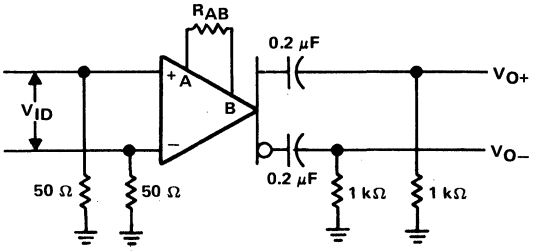


FIGURE 2

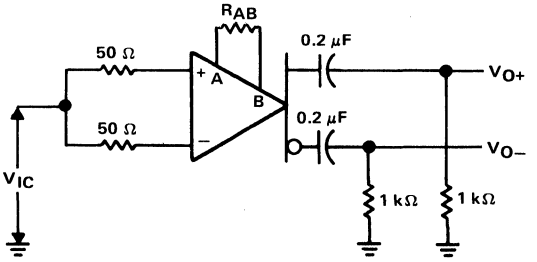


FIGURE 3

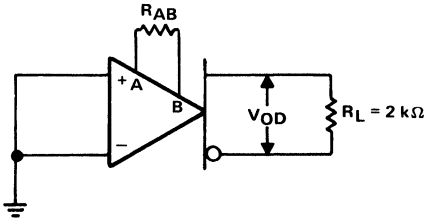


FIGURE 4

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

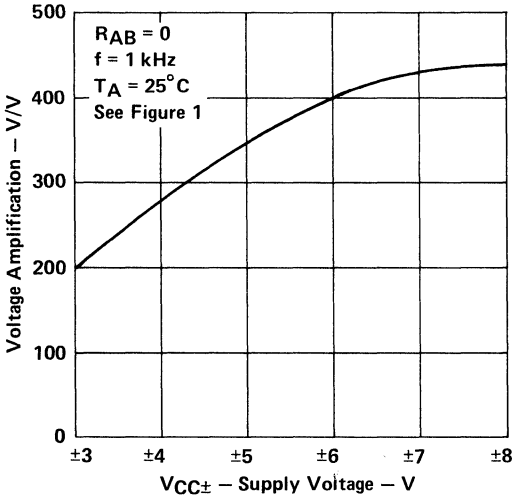


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs GAIN-ADJUSTMENT RESISTANCE

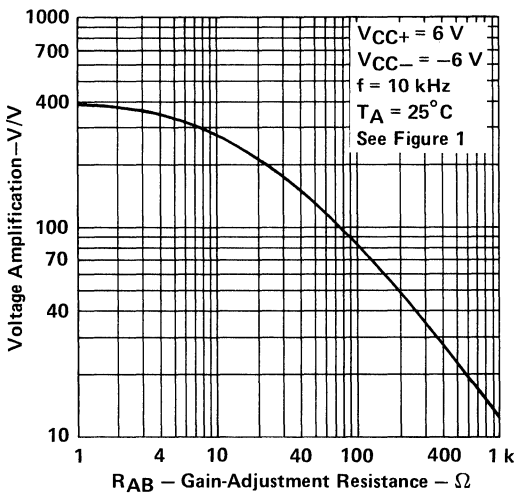


FIGURE 6

SUPPLY CURRENT vs SUPPLY VOLTAGE

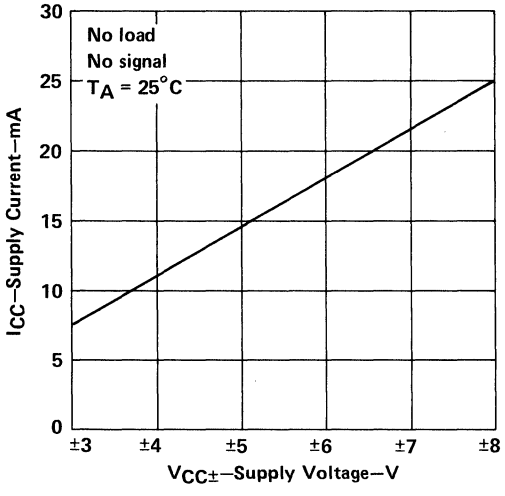
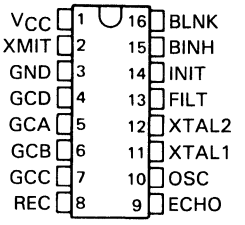


FIGURE 7

D2760, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28827**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interfaces to Electrostatic or Piezoelectric Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL851 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL851 is designed for distance measurement from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 50-kHz electrostatic transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 8.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420 kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 3.8 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.3 feet from the transducer. If it is necessary to detect objects closer than 1.3 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

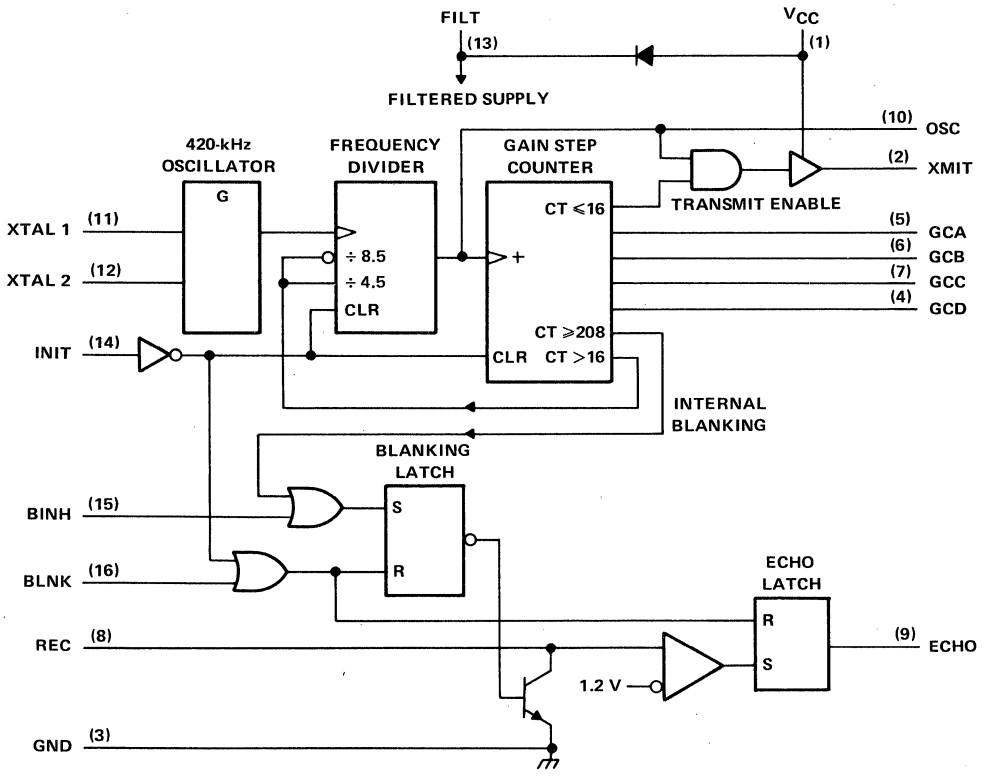
The threshold of the internal receive level detector is 1.2 volts. The TL851 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	GCD	GCC	GCB	GCA	TIME (ms) FROM INITIATE ↑†
0	L	L	L	L	2.38 ms
1	L	L	L	H	5.12 ms
2	L	L	L	L	7.87 ms
3	L	L	H	H	10.61 ms
4	L	H	L	L	13.35 ms
5	L	H	L	H	16.09 ms
6	L	H	H	L	18.84 ms
7	L	H	H	H	21.58 ms
8	H	L	L	L	27.07 ms
9	H	L	L	H	32.55 ms
10	H	L	H	L	38.04 ms
11	H	L	H	H	INIT ↓

† This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

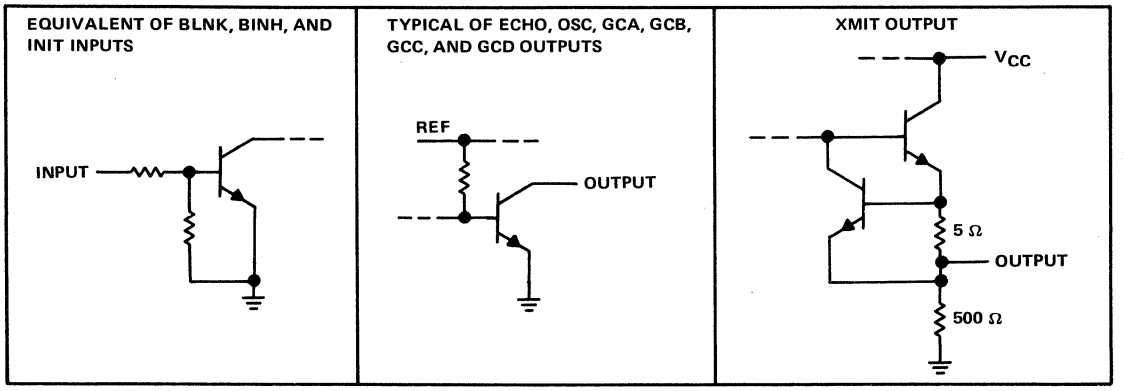
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to INIT high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC, GCA, GCB, GCC, GCD	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC, GCA, GCB, GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current	SMIT output	V_O = 1 V		−140		mA
Internal blanking interval	REC input			2.38‡		ms
Frequency during 16-pulse transmit period	OSC output			49.4‡		kHz
	XMIT output			49.4‡		
Frequency after 16-pulse transmit period	OSC output			93.3‡		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				260	mA
	After transmit period				55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



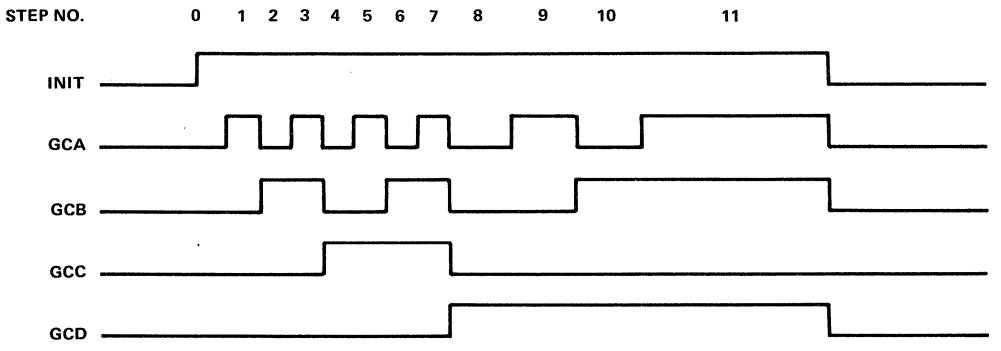


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

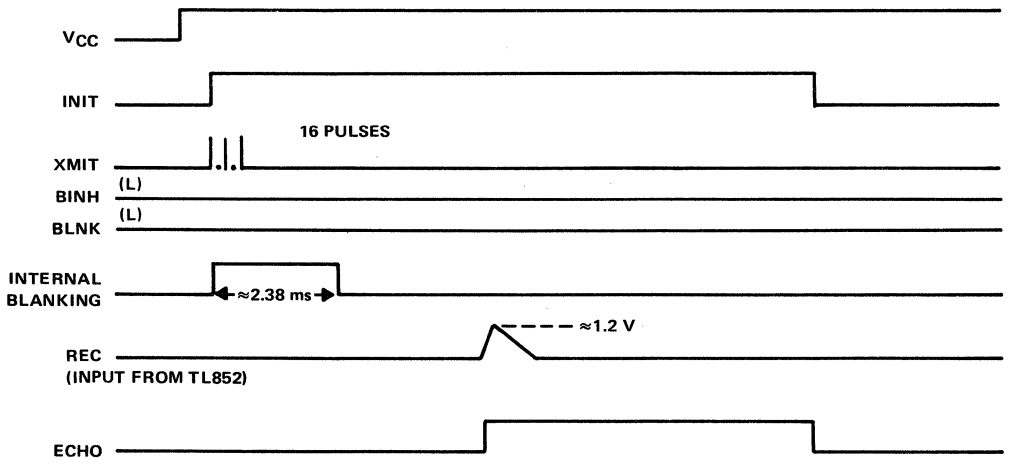
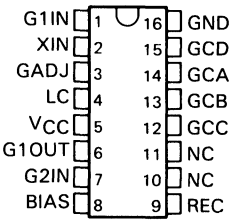


FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

D2779, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL851 in Sonar Ranging Modules Like the SN28827**
- **Digitally Controlled Variable-Gain Variable-Bandwidth Amplifier**
- **Operational Frequency Range of 20 kHz to 90 kHz**
- **TTL-Compatible**
- **Operates from Power Sources of 4.5 V to 6.8 V**
- **Interfaces to Electrostatic or Piezoelectric Transducers**
- **Overall Gain Adjustable with One External Resistor**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL852 is an economical sonar ranging receiver integrated circuit for use with the TL851 control integrated circuit. A minimum of external components is required for operation, and this amplifier easily interfaces to Polaroid's 50-kilohertz electrostatic transducer. An external 68-kilohm ±5% resistor from pin 8 (Bias) to pin 16 (GND) provides the internal biasing reference. Amplifier gain can be set with a resistor from pin 1 (G1IN) to pin 3 (GADJ). Required amplifier gain will vary for different applications. Using the detect-level measurement circuit of Figure 1, a nominal peak-to-peak value of 230 millivolts input during gain step 2 is recommended for most applications. For reliable operation, a level no lower than 50 millivolts should be used. The recommended detect level of 230 millivolts can be obtained for most amplifiers with an R1 value between 5 kilohms and 20 kilohms.

Digital control of amplifier gain is provided with gain control inputs on pins 12 through 15. These inputs must be driven synchronously (all inputs stable within 0.1 microsecond) to avoid false receive output signals due to invalid logic counts. This can be done easily with the TL851 control IC. A plot showing relative gain for the various gain steps versus time can be seen in Figure 2. To dampen ringing of the 50-kilohertz electrostatic transducer, a 5-kilohm resistor from pin 1 (GAIN) to pin 2 (XIN) is recommended.

An external parallel combination of inductance and capacitance between pin 4 (LC) and pin 5 (V_{CC}) provides an amplifier with an externally controlled gain and Q. This not only allows control of gain to compensate for attenuation of signal with distance, but also maximizes noise and sidelobe rejection. Care must be taken to accurately tune the L-C combination at operating frequency or gain and Q will be greatly reduced at higher gain steps.

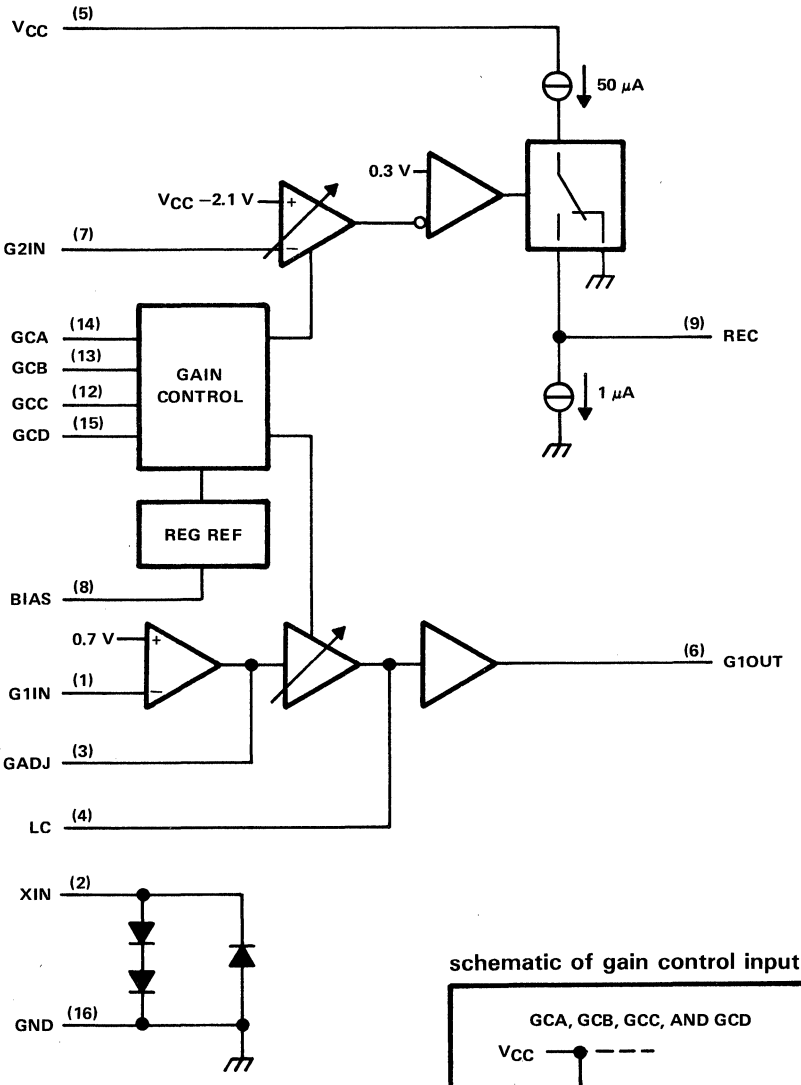
AC coupling between stages of the amplifier is accomplished with a 0.01-microfarad capacitor for proper biasing.

The receive output is normally held at a low level by an internal 1-microampere current source. When an input of sufficient amplitude is received, the output is driven alternately by the 1-microampere discharge current and a 50-microampere charging current. A 1000-picofarad capacitor is required from the receive output (pin 9) to ground (pin 16) to integrate the received signal so that one or two noise pulses will not be recognized.

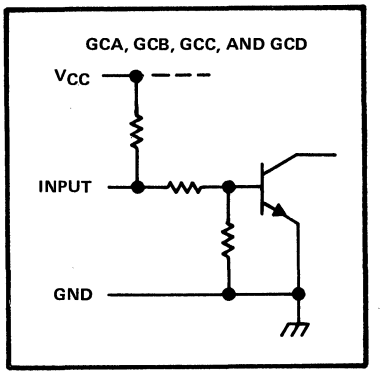
Pin 2 (XIN) provides clamping for the transformer secondary when used for transducer transmit drive as shown in Figure 4 of the SN28827 data sheet.

The TL852 is characterized for operation from 0°C to 40°C

functional block diagram



schematic of gain control inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
XIN input current (50% duty cycle) . . . . . ±60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	GCA, GCB, GCC, GCD	2.1		V
Low-level input voltage, V_{IL}			0.6	V
Bias resistor between pins 8 and 16		64	72	kΩ
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

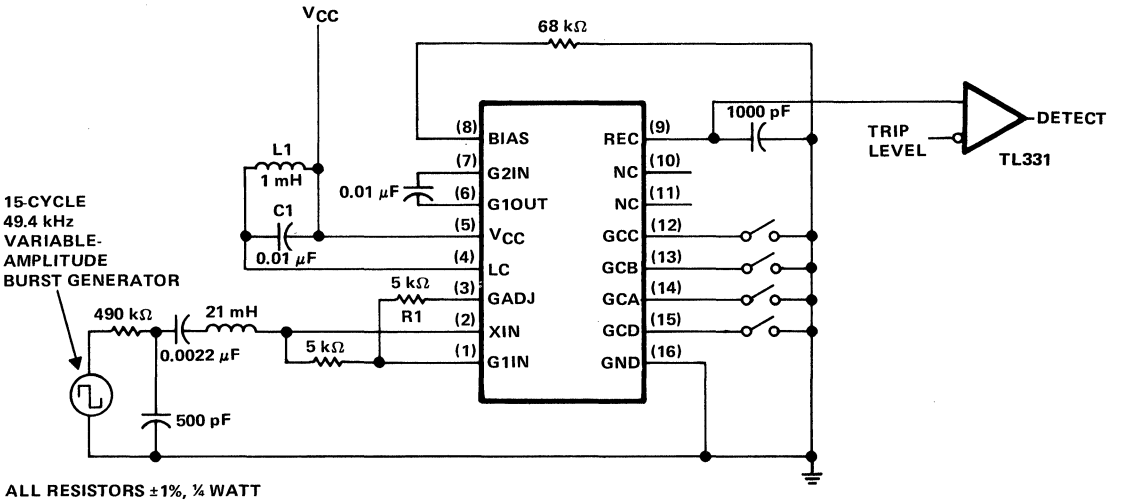
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input clamp voltage at XIN	I_I = 40 mA				2.5	V
	I_I = −40 mA				−1.5	
Open-circuit input voltage at GCA, GCB, GCC, GCD	V_{CC} = 5 V,	I_I = 0		2.5		V
High-level input current, I_{IH}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IH} = 2 V		−0.5		mA
Low-level input current, I_{IL}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IL} = 0			−3	mA
Receive output current	I_{G2IN} = −100 μA,	V_O = 0.3 V		1		μA
	I_{G2IN} = 100 μA,	V_O = 0.1 V		−50		
Supply current, I_{CC}					45	mA

†Typical values are at V_{CC} = 5 V and T_A = 25°C.

TYPICAL APPLICATION INFORMATION

detect level vs gain step

Detect level is measured by applying a 15-cycle burst of 49.4 kilohertz square wave just after the beginning of the gain step to be tested. The least burst amplitude that makes the REC pin reach the trip level is defined to be the detect level. System gain is then inversely proportional to detect level. See the test circuit in Figure 1.



ALL RESISTORS ±1%, ¼ WATT
ALL CAPACITORS ±1%, FILM
L1 Q > 60 at 50 kHz
C1 Q > 500 at 50 kHz

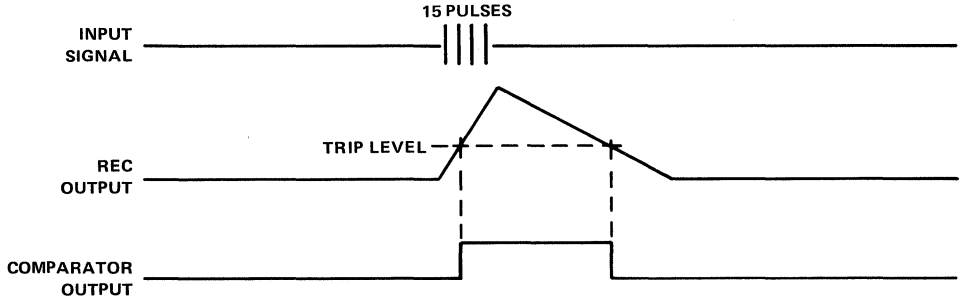


FIGURE 1. DETECT-LEVEL MEASUREMENT CIRCUIT AND WAVEFORMS

TYPICAL APPLICATION INFORMATION

GAIN STEP TABLE

GCD	GCC	GCB	GCA	STEP NUMBER
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11

RECEIVER GAIN
vs
GAIN STEP NUMBERS

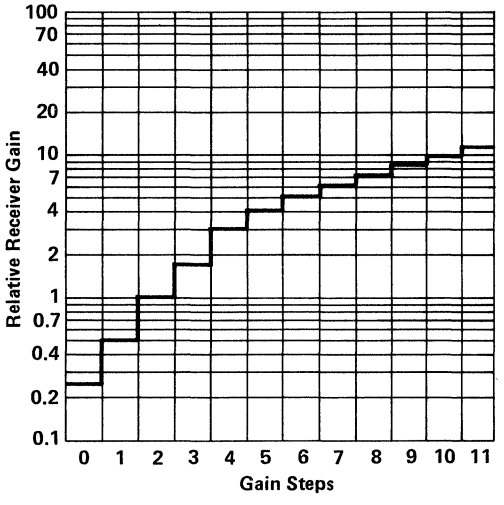
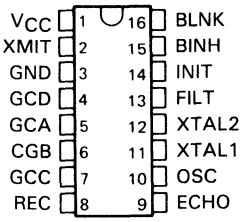


FIGURE 2

D2843, DECEMBER 1984—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28828**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interface to 40-kHz Piezoelectric or Electrostatic Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL853 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL853 is designed for distance measurement ranging from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 40-kHz piezoelectric transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 10.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420-kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 2.46 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.37 feet from the transducer. If it is necessary to detect objects closer than 1.37 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

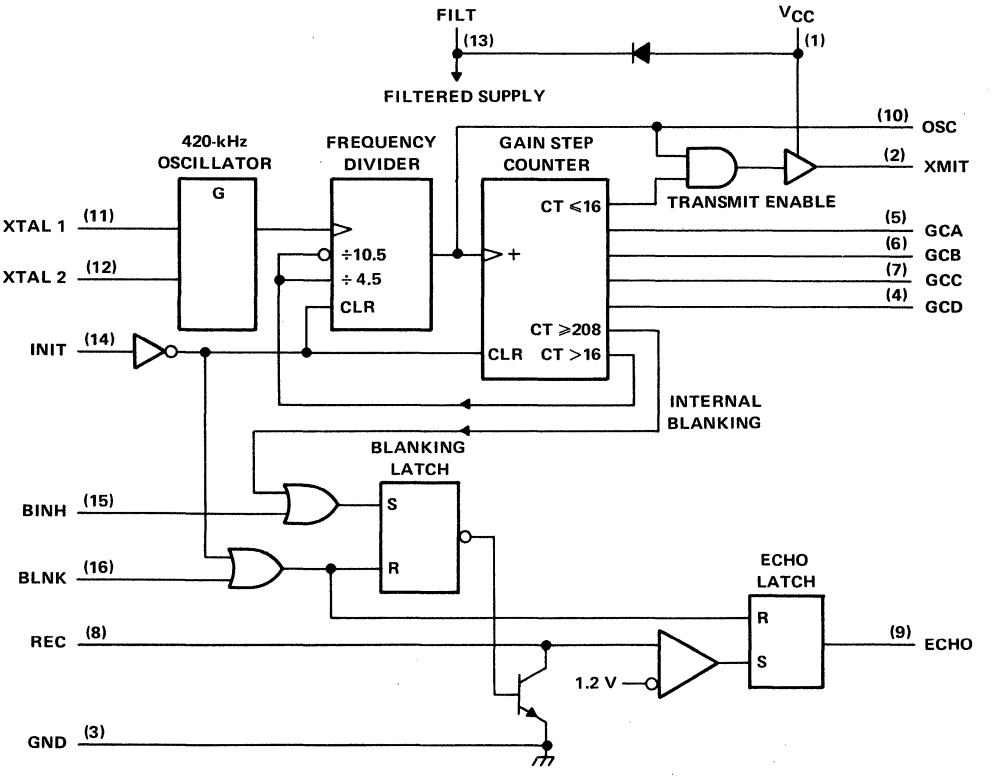
The threshold of the internal receive level detector is 1.2 volts. The TL853 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	CGD	GCC	GCB	GCA	TIME (ms) FROM INITIATE↑†
0	L	L	L	L	2.46 ms
1	L	L	L	H	5.2 ms
2	L	L	H	L	7.94 ms
3	L	L	H	H	10.69 ms
4	L	H	L	L	13.43 ms
5	L	H	L	H	16.17 ms
6	L	H	H	L	18.91 ms
7	L	H	H	H	21.66 ms
8	H	L	L	L	27.14 ms
9	H	L	L	H	32.63 ms
10	H	L	H	L	38.11 ms
11	H	L	H	H	INIT ↓

†This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

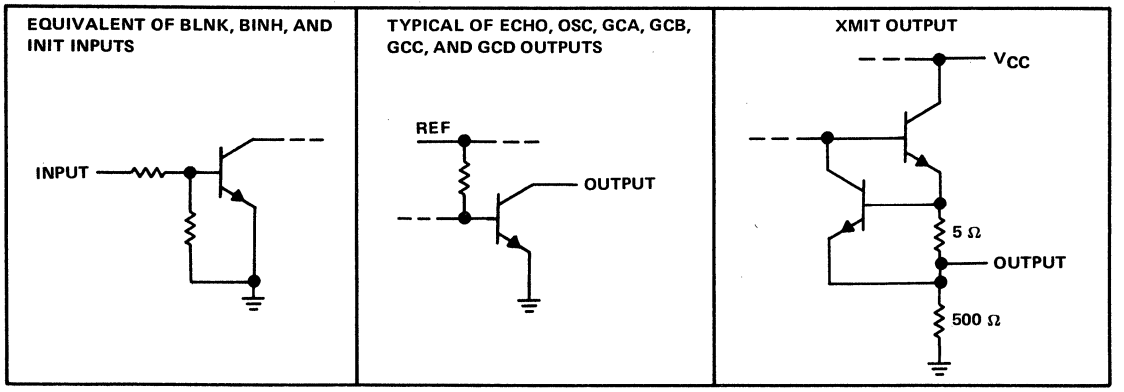
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to INIT high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC, GCA, GCB, GCC, GCD	V_{OH} = 5.5 mA			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC, GCA, GCB, GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current	XMIT output	V_O = 1 V		−140		mA
Internal blanking interval	REC input			2.46‡		ms
Frequency during 16-pulse transmit period	OSC output			40‡		kHz
	XMIT output			40‡		
Frequency after 16-pulse transmit period	OSC output			93.3‡		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				260	mA
	After transmit period				55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



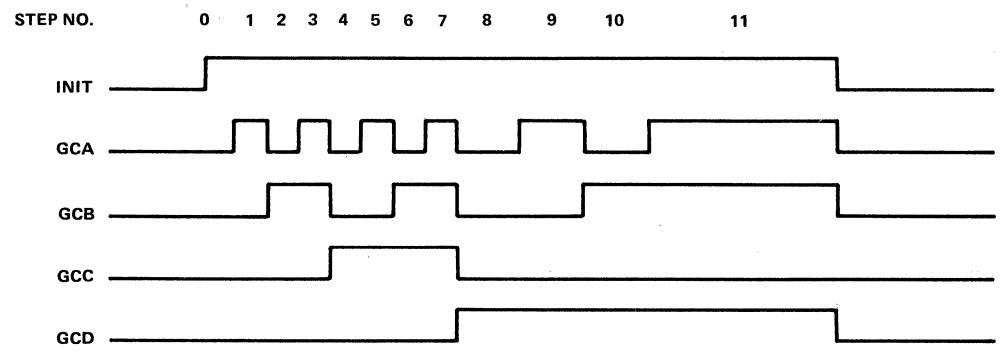


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

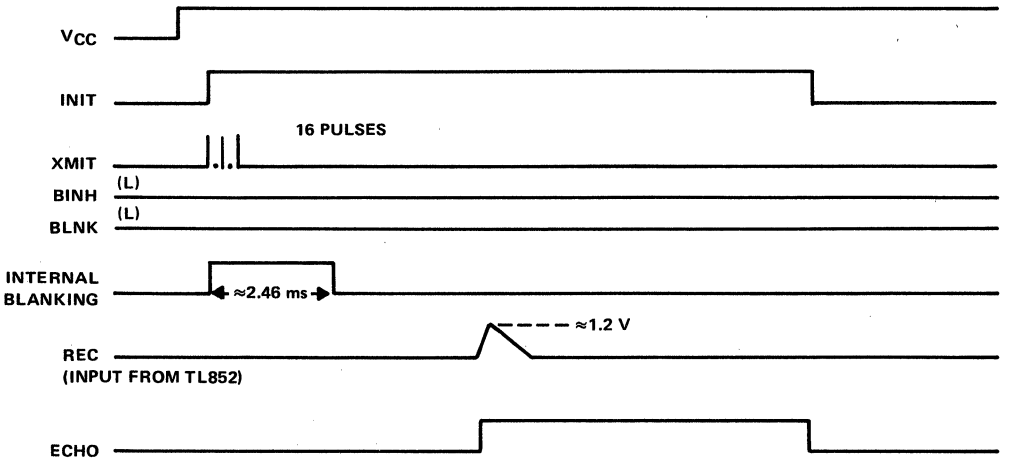
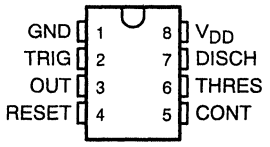


FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

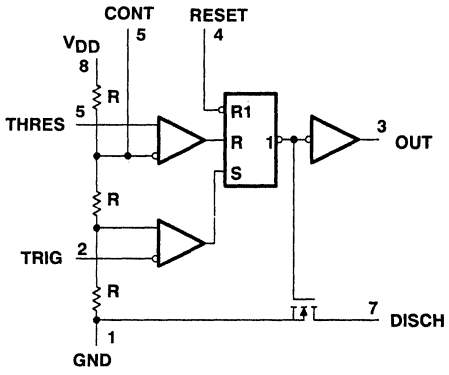
DD2791, FEBRUARY 1984–REVISED NOVEMBER 1991

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 1 V to 15 V**
- **Functionally Interchangeable With the NE555; Has Same Pinout**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2**

D, DB, P, OR PW PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit that is fabricated using TI's LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Compared to the NE555 timer, this device uses smaller timing capacitors because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC551 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized for operation from 0°C to 70°C.

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AVAILABLE OPTIONS

T_A	V_{DD} RANGE	PACKAGE				
		SMALL OUTLINE (D)	SSOP (DB)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	1 V to 18 V	TLC551CD	TLC551CDBLE	TLC551CP	TLC551CPWLE	TLC551Y

The D package is available taped and reeled. Add the suffix R (e.g., TLC551CDR).
The DB and PW packages are only available left-end taped and reeled.
Chips are tested at 25°C.

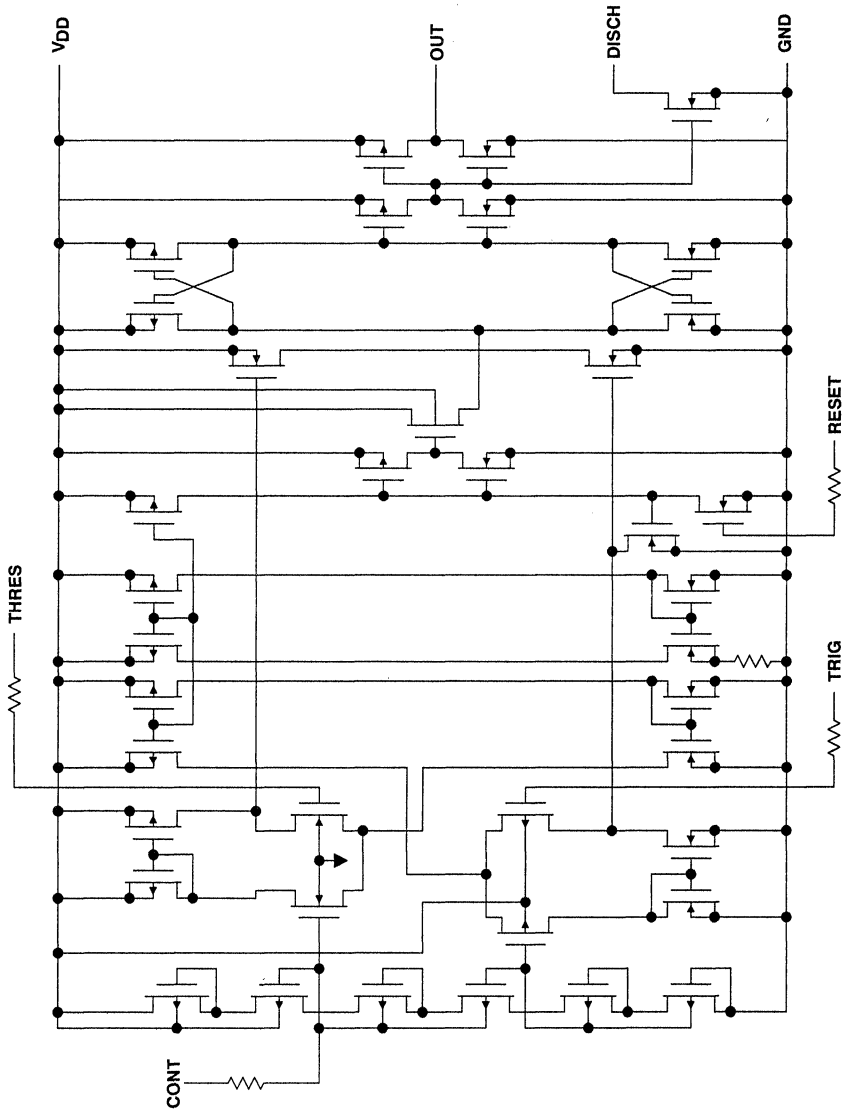
FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

ACTUAL DEVICE COMPONENT COUNT	
Transistors	39
Resistors	5

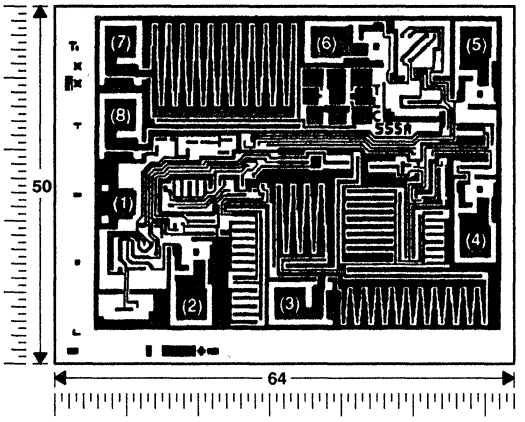
equivalent schematic (each channel)

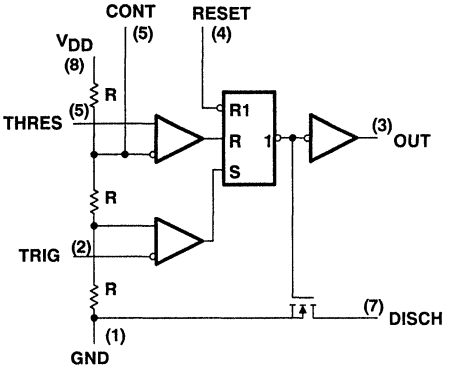


chip information

These chips, properly assembled, display characteristics similar to the TLC551. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Reset can override Trigger, which can override Threshold.

CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150° C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (1) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Input voltage range (any input) ..... −0.3 to V_{DD}
Sink current, discharge or output ..... 150 mA
Source current, output ..... 15 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
DB or PW	525 mW	4.2 mW/°C	336 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	15	V
Operating free-air temperature range, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		25°C	0.475	0.67	0.85	V
			Full range	0.45		0.875	
I_T	Threshold current		25°C		10		pA
			MAX		75		
$V_{trigger}$	Trigger voltage		25°C	0.15	0.33	0.425	V
			Full range	0.1		0.45	
$I_{trigger}$	Trigger current		25°C		10		pA
			MAX		75		
V_{reset}	Reset voltage		25°C	0.4	0.7	1	V
			Full range	0.3		1	
I_{reset}	Reset current		25°C		10		pA
			MAX		75		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
			Full range			0.2	
	Discharge switch off-stage current		25°C		0.1		nA
			MAX		0.5		
V_{OH}	High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
			Full range	0.6			
V_{OL}	Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
			Full range			0.25	
I_{DD}	Supply current	See Note 2	25°C		15	100	μA
			Full range			150	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		25°C	0.95	1.33	1.65	V
			Full range	0.85		1.75	
I_T	Threshold current		25°C		10		pA
			MAX		75		
$V_{trigger}$	Trigger voltage		25°C	0.4	0.67	0.95	V
			Full range	0.3		1.05	
$I_{trigger}$	Trigger current		25°C		10		pA
			MAX		75		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
I_{reset}	Reset current		25°C		10		pA
			MAX		75		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
			Full range			0.25	
	Discharge switch off-stage current		25°C		0.1		nA
			MAX		0.5		
V_{OH}	High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
			Full range	1.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
			Full range			0.35	
I_{DD}	Supply current	See Note 2	25°C		65	250	μA
			Full range			400	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		25°C	2.8	3.3	3.8	V
			Full range	2.7		3.9	
I_T	Threshold current		25°C		10		pA
			MAX		75		
$V_{trigger}$	Trigger voltage		25°C	1.36	1.66	1.96	V
			Full range	1.26		2.06	
$I_{trigger}$	Trigger current		25°C		10		pA
			MAX		75		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
I_{reset}	Reset current		25°C		10		pA
			MAX		75		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
			Full range			0.6	
	Discharge switch off-state current		25°C		0.1		nA
			MAX		0.5		
V_{OH}	High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
			Full range	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
			Full range			0.5	
		I_{OL} = 5 mA	25°C		0.13	0.3	
			Full range			0.4	
		I_{OL} = 3.2 mA	25°C		0.08	0.3	
			Full range			0.35	
I_{DD}	Supply current	See Note 2	25°C		170	350	μA
			Full range			500	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		25°C	9.45		10.55	V
			Full range	9.35		10.65	
I_T	Threshold current		25°C		10		pA
			MAX		75		
$V_{trigger}$	Trigger voltage		25°C	4.65	5	5.35	V
			Full range	4.55		5.45	
$I_{trigger}$	Trigger current		25°C		10		pA
			MAX		75		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	V
			Full range	0.3		1.8	
I_{reset}	Reset current		25°C		10		pA
			MAX		75		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%		
	Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
			Full range			1.8	
	Discharge switch off-state current		25°C		0.1		nA
			MAX		0.5		
V_{OH}	High-level output voltage	I_{OH} = – 10 mA	25°C	12.5	14.2		V
			Full range	12.5			
		I_{OH} = – 5 mA	25°C	13.5	14.6		
			Full range	13.5			
		I_{OH} = – 1 mA	25°C	14.2	14.9		
			Full range	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
			Full range			3.6	
		I_{OL} = 50 mA	25°C		0.63	1	
			Full range			1.3	
		I_{OL} = 10 mA	25°C		0.12	0.3	
			Full range			0.4	
I_{DD}	Supply current	See Note 2	25°C		360	600	μA
			Full range			800	

† Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Initial error of timing interval‡	V_{DD} = 5 V to 15 V,	$R_A = R_B$ = 1 kΩ to 100 kΩ,		1%	3%	
	Supply voltage sensitivity of timing interval	C_T = 0.1 μF,	See Note 3		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ,	C_L = 10 pF		20	75	ns
t_f	Output pulse fall time				15	60	
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF,	R_B = 200 Ω, See Note 3	1.2	1.8		MHz

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		2.8	3.3	3.8	V
I_T	Threshold current			10		pA
$V_{trigger}$	Trigger voltage		1.36	1.66	1.96	V
$I_{trigger}$	Trigger current			10		pA
V_{reset}	Reset voltage		0.4	1.1	1.5	V
I_{reset}	Reset current			10		pA
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA		0.14	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.21	0.4	V
		I_{OL} = 5 mA		0.13	0.3	
		I_{OL} = 3.2 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		170	350	μA

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

APPLICATION INFORMATION

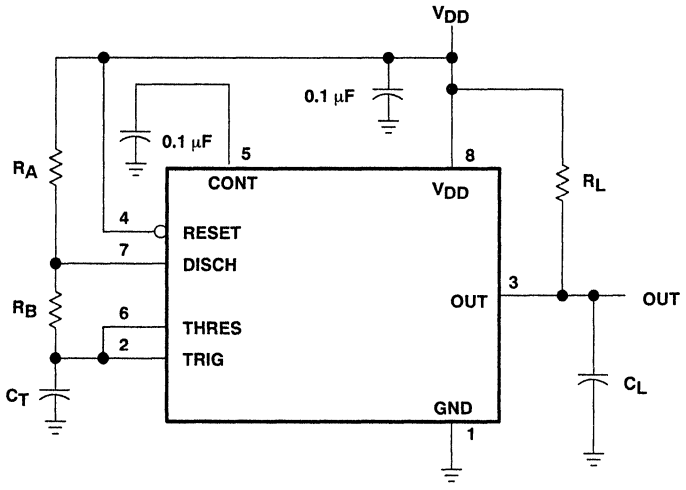
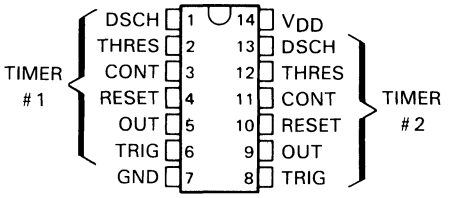


Figure 1. Circuit for Astable Operation

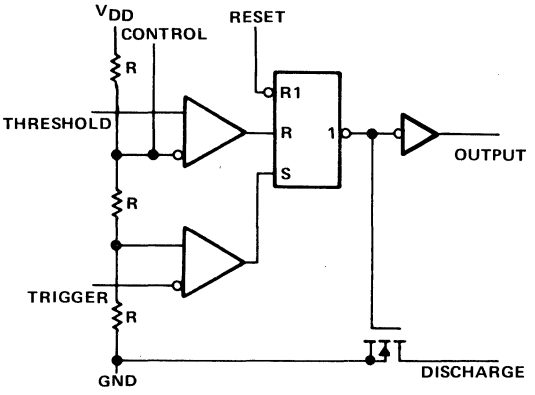
D2796, FEBRUARY 1984—REVISED MAY 1988

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

D OR N PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
TLC552C	D,N	0°C to 70°C	3.8 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. TLC552CDR)

LinCMOS is a trademark of Texas Instruments.

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		1.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0,95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	μA
		Full range			1000	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		0.72	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		0.84	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2	1.2	2.8		MHz

NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

‡ Timing interval error is defined as the difference between the measured value and the nominal value of a random sample.

TYPICAL APPLICATION DATA

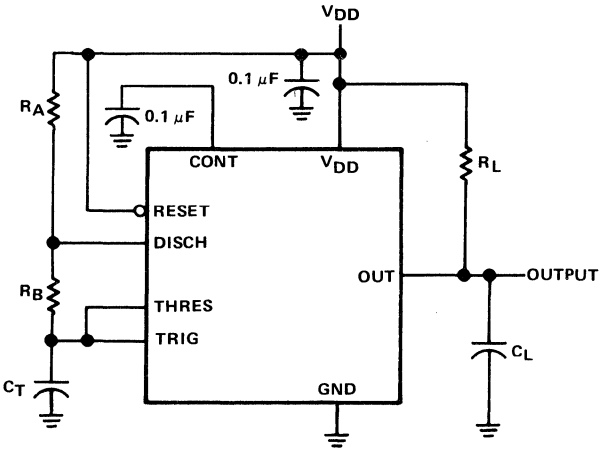
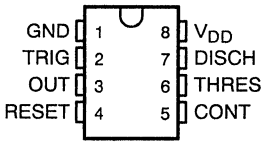


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

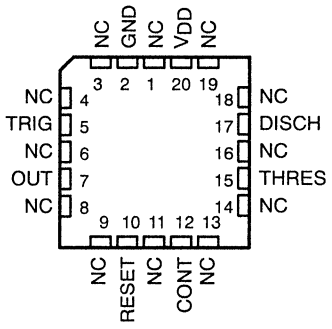
D2784, SEPTEMBER 1983 — REVISED NOVEMBER 1991

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 2 V to 15 V**
- **Functionally Interchangeable With the NE555; Has Same Pinout**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC555 is a monolithic timing circuit that is fabricated using TI's LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Compared to the NE555 timer, this device uses smaller timing capacitors because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC555C is characterized for operation from 0°C to 70°C. The TLC555I is characterized for operation from – 40°C to 85°C. The TLC555M is characterized for operation over the full military temperature range of – 55°C to 125°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	V_{DD} RANGE	PACKAGE						
		SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	2 V to 15 V	TLC555CD	TLC555CDBLE			TLC555CP	TLC555CPWLE	TLC555Y
– 40°C to 85°C	3 V to 15 V	TLC555ID				TLC555IP		
– 55°C to 125°C	5 V to 15 V	TLC555MD		TLC555MFK	TLC555MJG	TLC555MP		

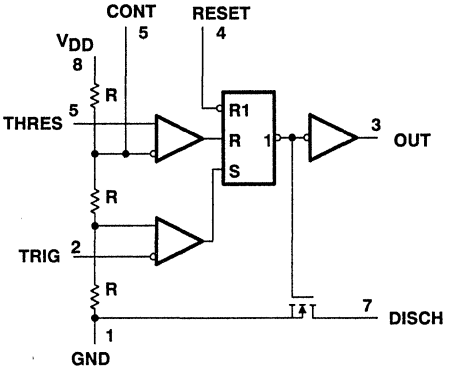
The D package is available taped and reeled. Add the suffix R (e.g., TLC555CDR).
The DB and PW packages are only available left-end taped and reeled.
Chips are tested at 25°C.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	L	On
>MAX	<MIN	Irrelevant	H	Off
>MAX	>MAX	>MAX	L	On
>MAX	>MAX	<MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

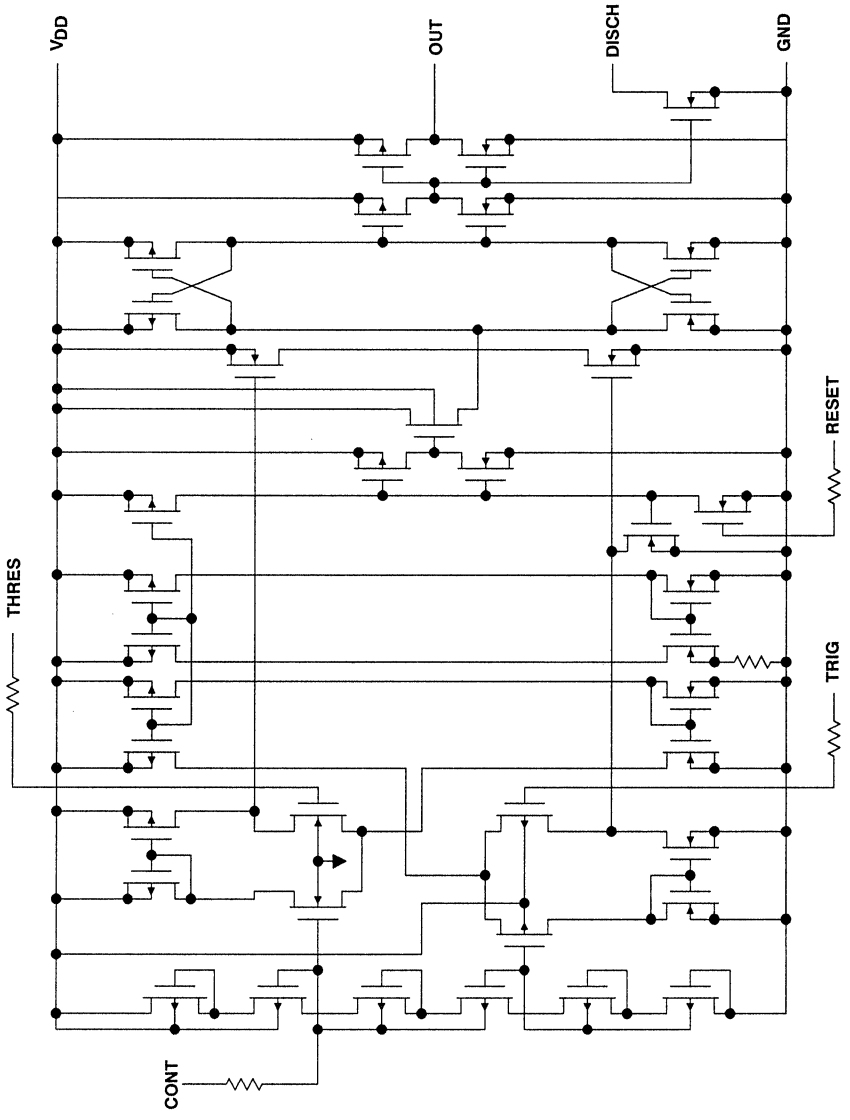
functional block diagram



Pin numbers are for all packages except FK.
Reset can override TRIG, which can override THRES.

equivalent schematic (each channel)

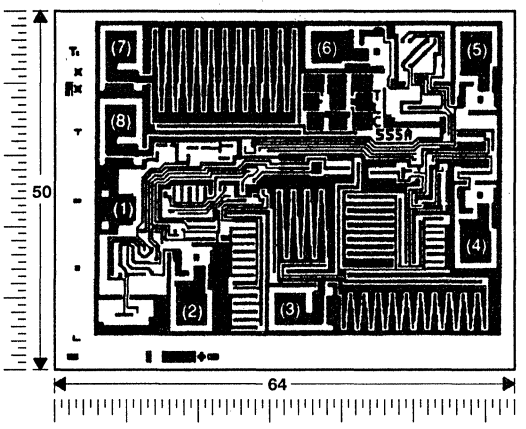
ACTUAL DEVICE COMPONENT COUNT	
Transistors	39
Resistors	5

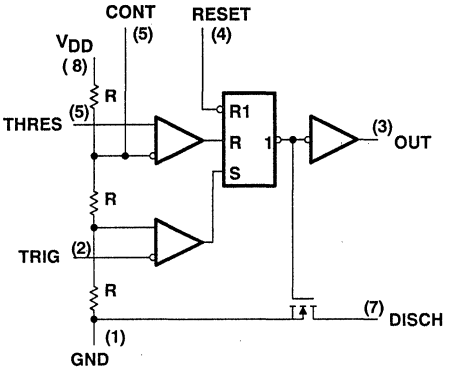


chip information

These chips, properly assembled, display characteristics similar to the TLC555. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Reset can override Trigger, which can override Threshold.

CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150° C

TOLERANCES ARE ± 10%

ALL DIMENSIONS ARE IN MILS

PIN (1) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Input voltage range (any input) ..... −0.3 to V_{DD}
Sink current, discharge or output ..... 150 mA
Source current, output ..... 15 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
M-suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
DB or PW	525 mW	4.2 mW/°C	336 mW	—	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	15	V
Operating free-air temperature range, T_A	TLC555C	0	70	°C
	TLC555I	−40	85	
	TLC555M	−55	125	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V for TLC555I, V_{DD} = 2 V for TLC555C

PARAMETER		TEST CONDITIONS	T_A†	TLC555C			TLC555I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	0.95	1.33	1.65	1.6		2.4	V
			Full range	0.85		1.75	1.5		2.5	
I_T	Threshold current		25°C		10			10		pA
			MAX		75			150		
$V_{trigger}$	Trigger voltage		25°C	0.4	0.67	0.95	0.71	1	1.29	V
			Full range	0.3		1.05	0.61		1.39	
$I_{trigger}$	Trigger current		25°C		10			10		pA
			MAX		75			150		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		2	0.3		1.8	
I_{reset}	Reset current		25°C		10			10		pA
			MAX		75			150		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
	Discharge switch on-stage voltage	I_{OL} = 1 mA	25°C		0.03	0.2		0.03	0.2	V
			Full range			0.25			0.375	
	Discharge switch off-stage current		25°C		0.1			0.1		nA
			MAX		0.5			120		
V_{OH}	High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		1.5	1.9		V
			Full range	1.5			2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
			Full range			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C			250			250	μA
			Full range			400			500	

† Full range is 0°C to 70°C for TLC555C and – 40°C to 85°C for TLC555I.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC555C			TLC555I			TLC555M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
			Full range	2.7		3.9	2.7		3.9	2.7		3.9	
I_T	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{trigger}$	Trigger voltage		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
			Full range	1.26		2.06	1.26		2.06	1.26		2.06	
$I_{trigger}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
I_{reset}	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
Control voltage (open circuit) as a percentage of supply voltge			MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5		0.14	0.5		0.14	0.5	V
			Full range			0.6			0.6			0.6	
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			120			120		
V_{OH}	High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
			Full range	4.1			4.1			4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
			Full range			0.5			0.5			0.6	
		I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
			Full range			0.4			0.4			0.45	
		I_{OH} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
			Full range			0.35			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C		170	350		170	350		170	350	μA
			Full range			500			600			700	

† Full range is 0°C to 70°C for TLC555C, – 40°C to 85°C for TLC555I, and – 55°C to 125°C for TLC555M.

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER		TEST CONDITIONS	T_A†	TLC555C			TLC555I			TLC555M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
			Full range	9.35		10.65	9.35		10.65	9.35		10.65	
I_T	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{trigger}$	Trigger voltage		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
			Full range	4.55		5.45	4.55		5.45	4.55		5.45	
$I_{trigger}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
I_{reset}	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7		0.77	1.7		0.77	1.7	V
			Full range			1.8			1.8			1.8	
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			120			120		
V_{OH}	High-level output voltage	I_{OH} = – 10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
			Full range	12.5			12.5			12.5			
		I_{OH} = – 5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
			Full range	13.5			13.5			13.5			
		I_{OH} = – 1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
			Full range	14.2			14.2			14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
			Full range			3.6			3.7			3.8	
		I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
			Full range			1.3			1.4			1.5	
		I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
			Full range			0.4			0.4			0.45	
I_{DD}	Supply current	See Note 2	25°C		360	600		360	600		360	600	μA
			Full range			800			900			1000	

† Full range is 0°C to 70°C for TLC555C, – 40°C to 85°C for TLC555I, and – 55°C to 125°C for TLC555M.

NOTE 2These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Initial error of timing interval‡	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		1%	3%	
	Supply voltge sensistivity of timing interval					
t_r	Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
t_f	Output pulse fall time			15	60	
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

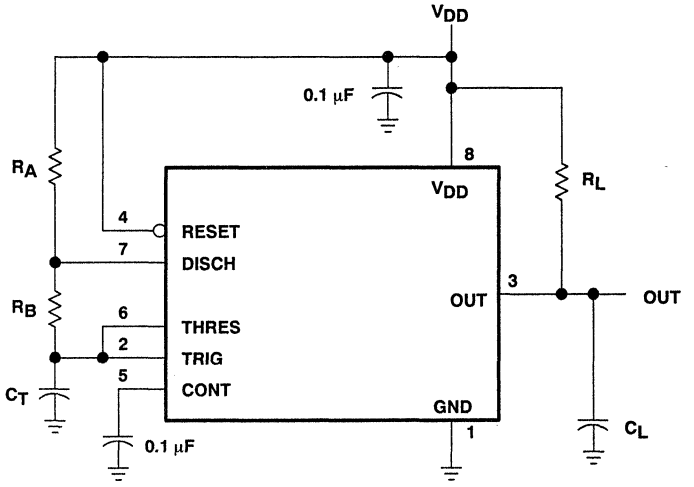
NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

electrical characteristics at V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		2.8	3.3	3.8	V
I_T	Threshold current			10		pA
$V_{trigger}$	Trigger voltage		1.36	1.66	1.96	V
$I_{trigger}$	Trigger current			10		pA
V_{reset}	Reset voltage		0.4	1.1	1.5	V
I_{reset}	Reset current			10		pA
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA		0.14	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.21	0.4	V
		I_{OL} = 5 mA		0.13	0.3	
		I_{OL} = 3.2 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		170	350	μA

NOTE 2: These values apply for the expected operating configurations in which the THRES terminal is connected directly to the DISCH terminal or to the TRIG terminal.

APPLICATION INFORMATION



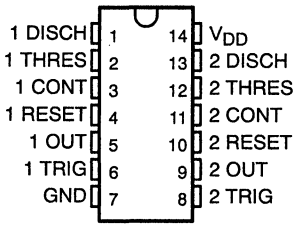
Pin numbers are for all packages except FK.

Figure 1. Circuit for Astable Operation

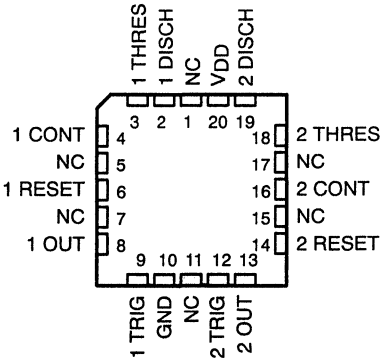
D2796, FEBRUARY 1984 –REVISED FEBRUARY 1992

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  Sink 100 mA Typ
  Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 2 V to 15 V**
- **Functionally interchangeable With the NE556; Has Same Pinout**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The TLC556 series are monolithic timing circuits fabricated using the TI LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556C is characterized for operation from 0°C to 70°C. The TLC556I is characterized for operation from –40°C to 85°C. The TLC556M is characterized for operation over the full military temperature range of –55°C to 125°C.

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AVAILABLE OPTIONS

T_A RANGE	V_{DD} RANGE	PACKAGE				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	2 V to 18 V	TLC556CD			TLC556CN	TLC556Y
−40°C to 85°C	3 V to 18 V	TLC556ID			TLC556IN	
−55°C to 125°C	5 V to 18 V	TLC556MD	TLC556MFK	TLC556MJ	TLC556MN	

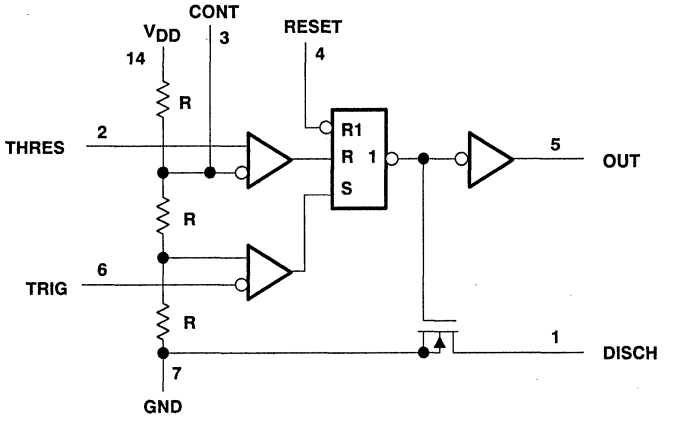
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC556CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
< MIN	Irrelevant	Irrelevant	L	On
> MAX	< MIN	Irrelevant	H	Off
>MAX	>MAX	>MAX	L	On
> MAX	> MAX	< MIN	As previously established	

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram (each timer)



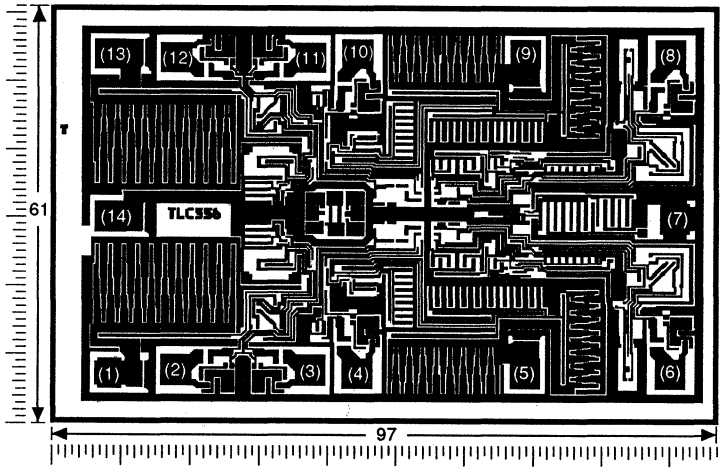
RESET can override TRIG and THRES.
TRIG can override THRES.

Pin numbers shown are for the D, J, or N packages.

chip information

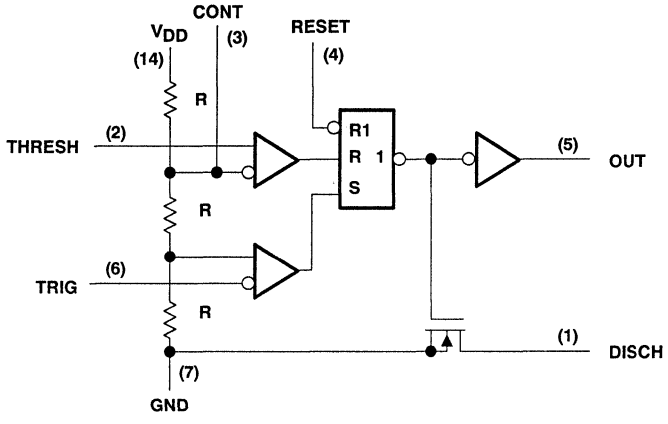
These chips, properly assembled, display characteristics similar to the TLC556 (see electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL
BONDING PADS: 4 × 4 MINIMUM
T_J max = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS
NO BACKSIDE METALLIZATION
PIN (7) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

FUNCTIONAL BLOCK DIAGRAM (EACH TIMER)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

		TLC556C	TLC556I	TLC556M	UNIT
Supply voltage, V_{DD} (see Note 1)		18	18	18	V
Input voltage range, V_I		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package			300	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260		

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	15	V
Operating free-air temperature range, T_A	TLC556C	0	70	°C
	TLC556I	−40	85	
	TLC556M	−55	125	

electrical characteristics at specified free-air temperature, V_{DD} = 2 V for TLC556C, V_{DD} = 3 V for TLC556I

PARAMETER		TEST CONDITIONS	T_A†	TLC556C			TLC556I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	0.95	1.33	1.65	1.6	2	2.4	V
			Full range	0.85		1.75	1.5		2.5	
I_T	Threshold current		25°C		10			10		pA
			MAX		75			150		
$V_{trigger}$	Trigger voltage		25°C	0.4	0.67	0.95	0.71	1	1.29	V
			Full range	0.3		1.05	0.61		1.39	
$I_{trigger}$	Trigger current		25°C		10			10		pA
			MAX		75			150		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	
I_{reset}	Reset current		25°C		10			10		pA
			MAX		75			150		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.04	0.2		0.03	0.2	V
			Full range			0.25			0.375	
	Discharge switch off-state current		25°C		0.1			0.1		nA
			MAX		0.5			120		
V_{OH}	High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		1.5	1.9		V
			Full range	1.5			2.5			
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
			Full range			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C		130	500		130	500	μA
			Full range			800			1000	

† Full range is 0°C to 70°C for TLC556C and −40°C to 85°C for TLC556I.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	T_A†	TLC556C			TLC556I			TLC556M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
			Full range	2.7		3.9	2.7		3.9	2.7		3.9	
I_T	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{trigger}$	Trigger voltage		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
			Full range	1.26		2.06	1.26		2.06	1.26		2.06	
$I_{trigger}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
I_{reset}	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
			Full range			0.6			0.6		0.6		
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			2			120		
V_{OH}	High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
			Full range	4.1			4.1			4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
			Full range			0.5			0.5			0.6	
		I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
			Full range			0.4			0.4			0.45	
		I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
			Full range			0.35			0.35			0.4	
I_{DD}	Supply current	See Note 2	25°C		340	700		340	700		340	700	μA
			Full range			1000			1200			1400	

† Full range is 0°C to 70°C for TLC556C, −40°C to 85°C for TLC556I, and −55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER		TEST CONDITIONS	T_A†	TLC555C			TLC555I			TLC555M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Threshold voltage		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
			Full range	9.35		10.65	9.35		10.65	9.35		10.65	
I_T	Threshold current		25°C		10			10			10		pA
			MAX		75			150			5000		
$V_{trigger}$	Trigger voltage		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
			Full range	4.55		5.45	4.55		5.45	4.55		5.45	
$I_{trigger}$	Trigger current		25°C		10			10			10		pA
			MAX		75			150			5000		
V_{reset}	Reset voltage		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
			Full range	0.3		1.8	0.3		1.8	0.3		1.8	
I_{reset}	Reset current		25°C		10			10			10		pA
			MAX		75			150			5000		
	Control voltage (open circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
	Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
			Full range			1.8			1.8			1.8	
	Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
			MAX		0.5			2			120		
V_{OH}	High-level output voltage	I_{OH} = – 10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
			Full range	12.5			12.5			12.5			
		I_{OH} = – 5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
			Full range	13.5			13.5			13.5			
		I_{OH} = – 1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
			Full range	14.2			14.2			14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
			Full range			3.6			3.7			3.8	
		I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
			Full range			1.3			1.4			1.5	
		I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
			Full range			0.4			0.4			0.45	
I_{DD}	Supply current	See Note 2	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
			Full range			1.6			1.8			2	

† Full range is 0°C to 70°C for TLC556C, – 40°C to 85°C for TLC556I, and – 55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage		2.8	3.3	3.8	V
I_T	Threshold current			10		pA
$V_{trigger}$	Trigger voltage		1.36	1.66	1.96	V
$I_{trigger}$	Trigger current			10		pA
V_{reset}	Reset voltage		0.4	1.1	1.5	V
I_{reset}	Reset current			10		pA
	Discharge switch on-state voltage	I_{OL} = 10 mA		0.15	0.5	V
	Discharge switch off-state current			0.1		nA
V_{OH}	High-level output voltage	I_{OH} = −1 mA	4.1	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.21	0.4	V
		I_{OL} = 5 mA		0.13	0.3	
		I_{OL} = 2.1 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		3.40	700	µA

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Initial error of timing interval †	V_{DD} = 5 V to 15 V,	$R_A = R_B$ = 1 kΩ to 100 kΩ		1%	3%	
	Supply voltage sensitivity of timing interval	C_T = 0.1 μF,	See Note 3		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ,	C_L = 10 pF		20	75	ns
t_f	Output pulse fall time				15	60	
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF,	R_B = 200 Ω, See Note 3	1.2	2.1		MHz

† Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
NOTE 3: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

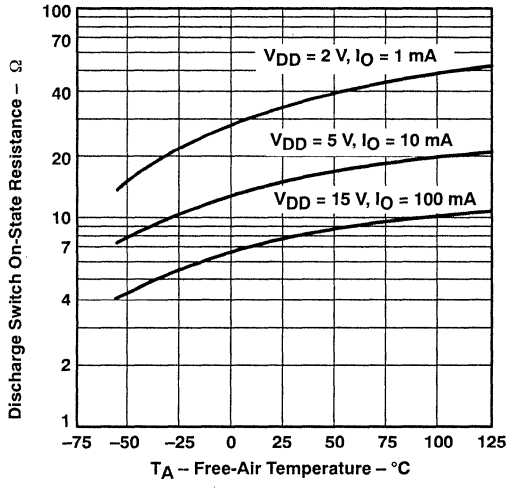
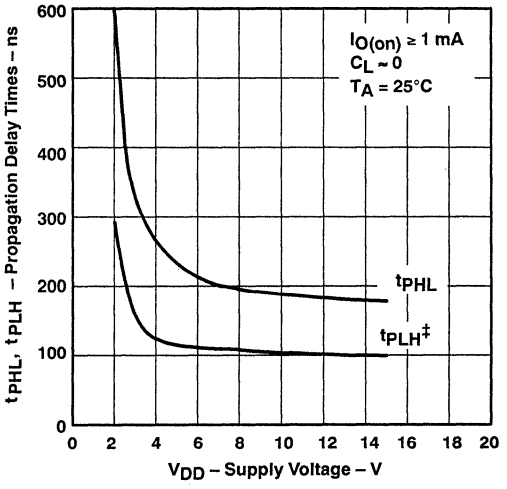


Figure 1

PROPAGATION DELAY TIMES
TO DISCHARGE OUTPUT
FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER
vs
SUPPLY VOLTAGE



‡ The effects of the load resistance on these values must be taken into account separately.

Figure 2

APPLICATION INFORMATION

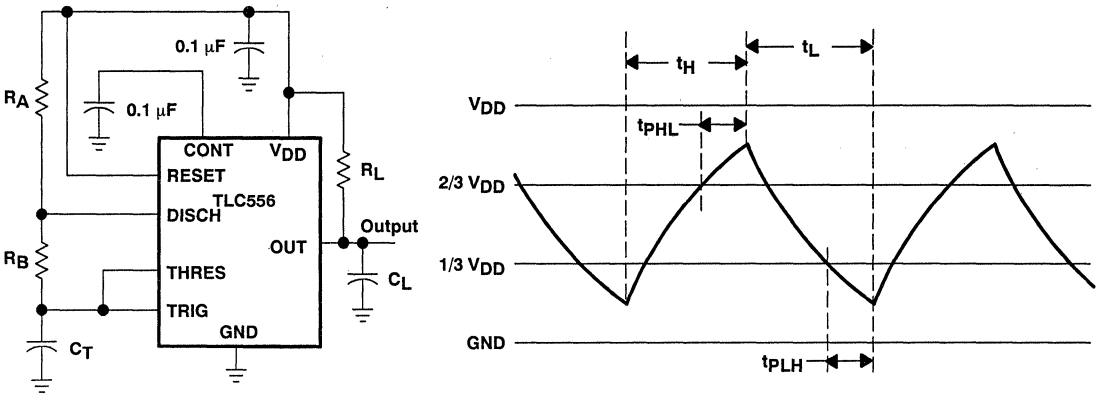


Figure 3. Astable Operation

Connecting the trigger input to the threshold input, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the trigger voltage level (approximately 0.67 V_{DD}) and then discharges through R_B only to the value of the threshold voltage level (approximately 0.33 V_{DD}). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, and R_B, and C_T, as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})} \right) \right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)} \right) \right] + t_{PLH}$$

APPLICATION INFORMATION

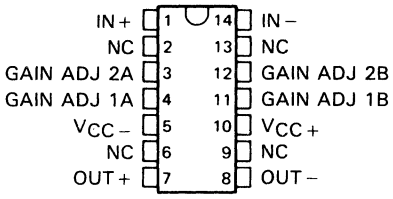
The preceding equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_H}{t_H + t_L}$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500-μA bias provides good results.

D922, NOVEMBER 1970—REVISED APRIL 1988

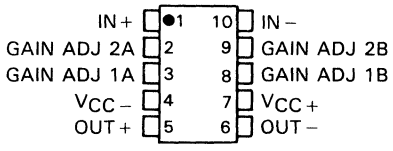
- **200-MHz Bandwidth**
- **250-kΩ Input Resistance**
- **Selectable Nominal Amplification of 10, 100, or 400**
- **No Frequency Compensation Required**
- **Designed to be Interchangeable with Fairchild μA733M and μA733C**

uA733M . . . J DUAL-IN-LINE PACKAGE
uA733C . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

UA733M . . . U FLAT PACKAGE
(TOP VIEW)



description

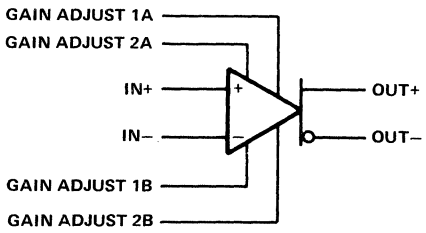
The uA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

symbol



The uA733M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA733C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA733M	UA733C	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	°C

NOTE 1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	N/A
J (uA733M)	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

electrical characteristics, $V_{CC+} = 6$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M MIN	uA733M TYP	uA733M MAX	uA733C MIN	uA733C TYP	uA733C MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	V/V
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \le 1$ V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \le 1$ V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, No signal	Any		16	24		16	24	mA

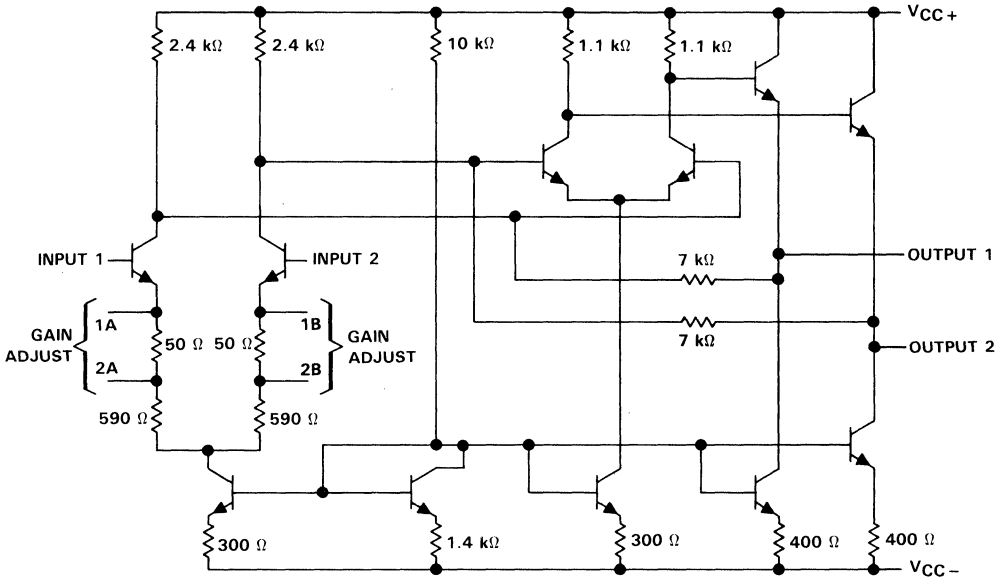
† The gain option is selected as follows:
Gain Option1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = −55°C to 125°C for uA733M, 0°C to 70°C for uA733C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M MIN	uA733M MAX	uA733C MIN	uA733C MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	200	600	250	600	V/V
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		5		6	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.2		1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.5		2.8		V
r_i	Input resistance	3	V_{OD} ≤ 1 V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	50		50		dB
			V_{IC} = ±1 V, f = 5 MHz	2					
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.2		2.5		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

†The gain option is selected as follows:
Gain Option 1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

schematic



Component values shown are nominal.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio (k_{SVR}) The absolute value of the ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

Equivalent Input Noise Voltage (V_n) The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents I_{CC1} and I_{CC2}.

PARAMETER MEASUREMENT INFORMATION

test circuits

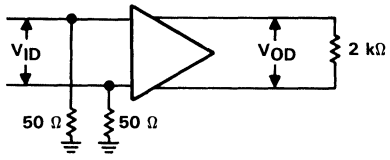


FIGURE 1

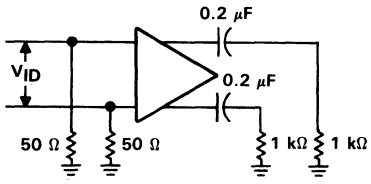


FIGURE 2

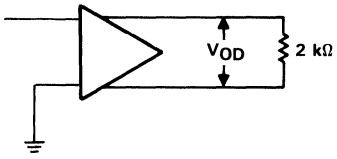


FIGURE 3

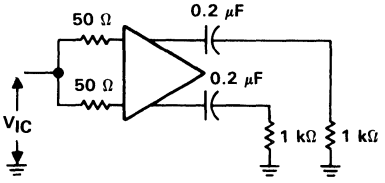


FIGURE 4

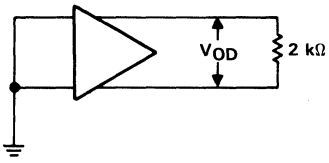
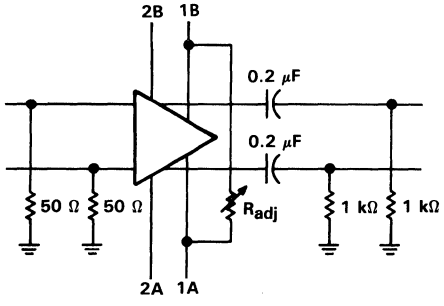


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

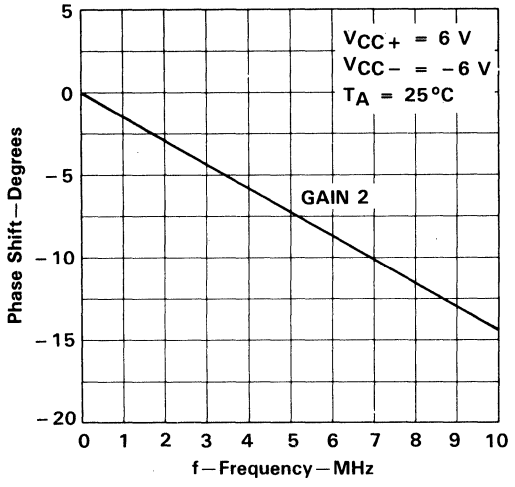


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

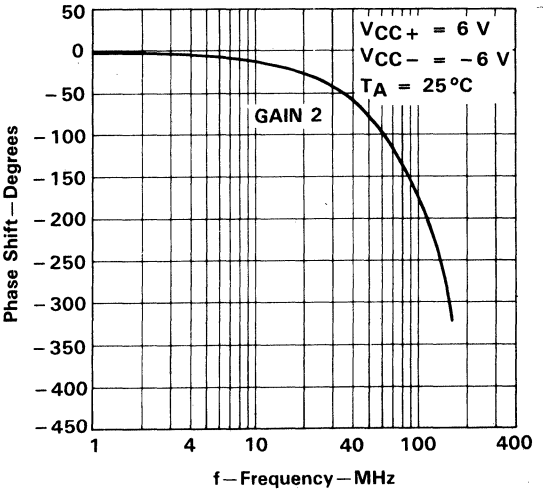


FIGURE 8

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

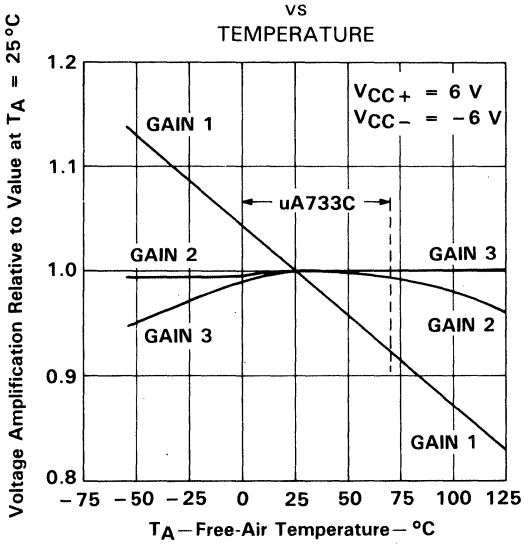


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

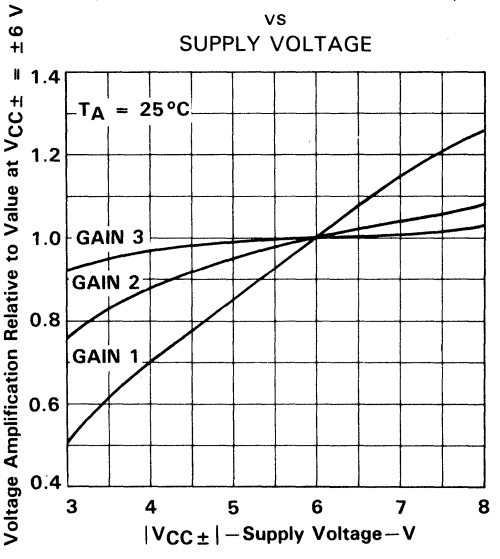


FIGURE 10

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

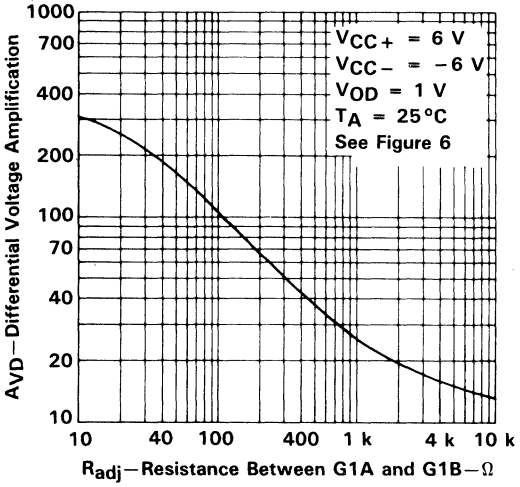


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

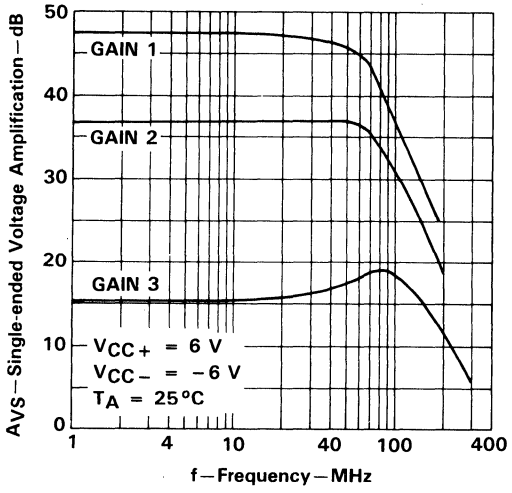


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

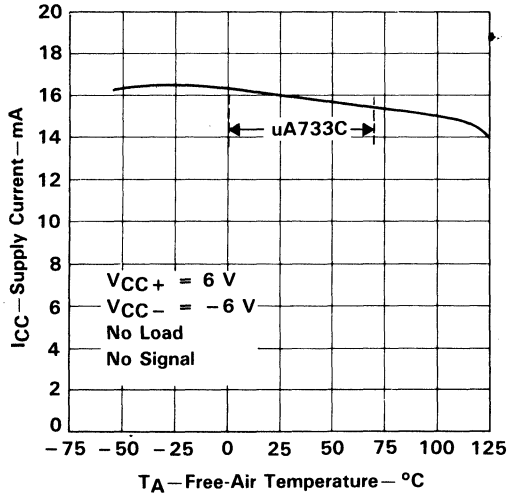


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

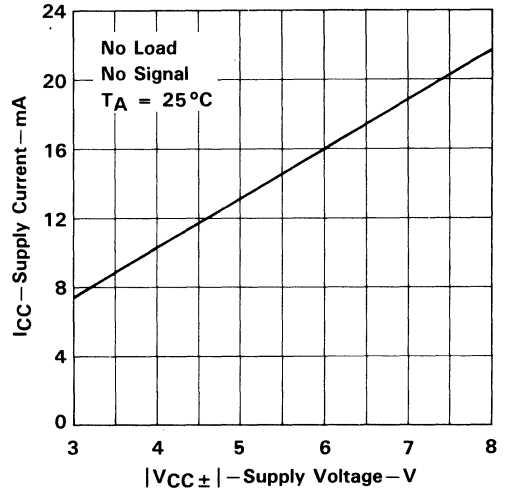


FIGURE 14

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

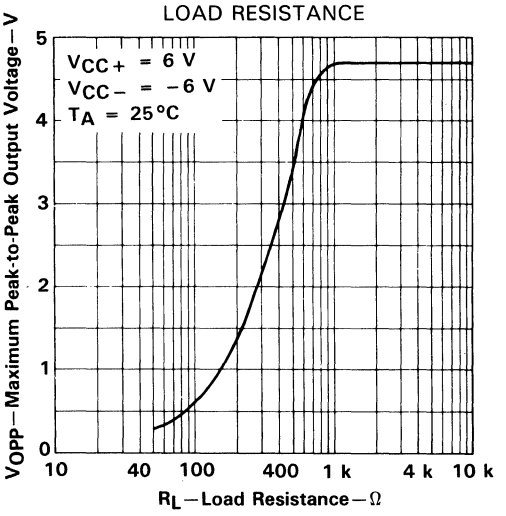


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

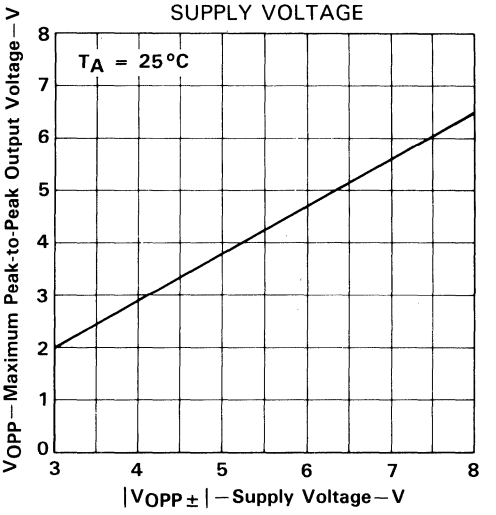


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

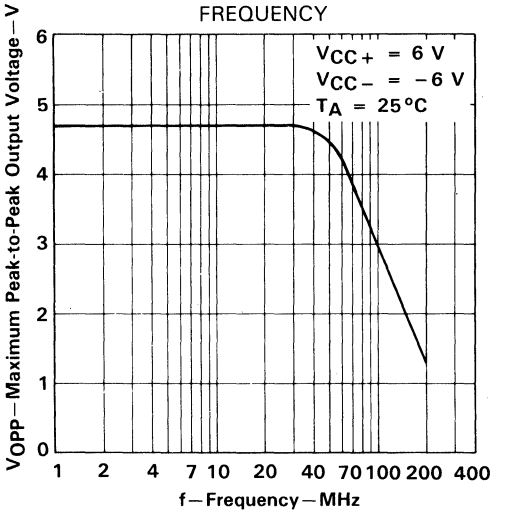


FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

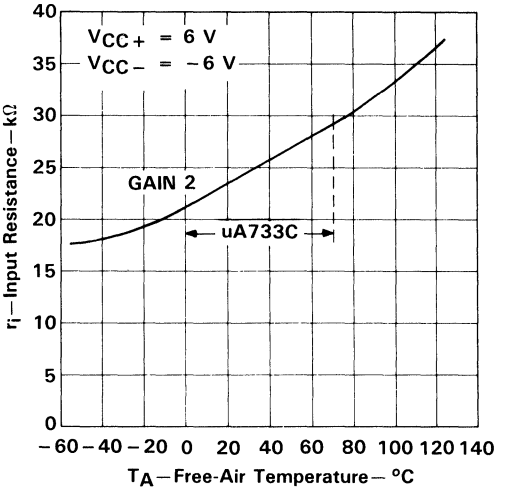
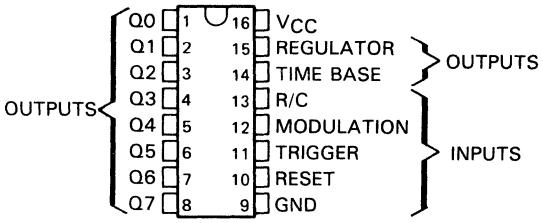


FIGURE 18

D2442, JUNE 1978—REVISED MAY 1988

- **Accurate Timing from Microseconds to Days**
- **Programmable Delays from 1 Time Constant to 255 Time Constants**
- **Outputs Compatible with TTL and CMOS**
- **Wide Supply-Voltage Range**
- **External Sync and Modulation Capability**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These circuits consist of a time-base oscillator, and eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at pin 13 and can be synchronized or modulatd by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at pin 14 (time base). The time-base pin may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0 through Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240C will ignore any signals at the trigger input until it is reset.

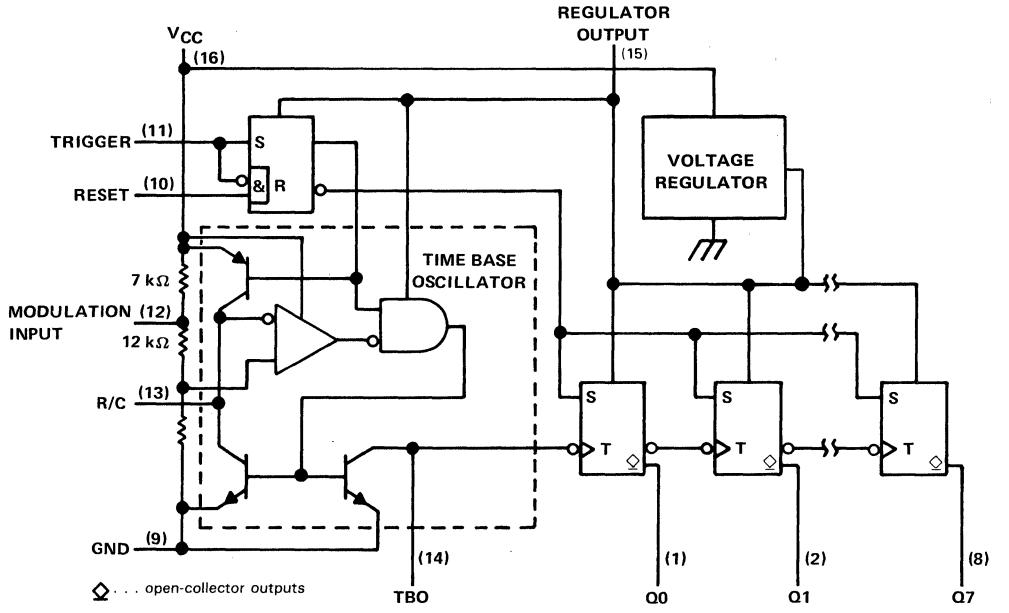
The uA2240C timer/counter may be operated in the free-running mode or with output-signal feedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

The uA2240C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
uA2240C	N	0°C to 70°C	2 V

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Output voltage: Q0 thru Q7 . . . . . 18 V
Output current: Q0 thru Q7 . . . . . 10 mA
Regulator output current . . . . . −5 mA
Continuous dissipation at (or below) 25°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4		14	V
Timing resistor	0.001		10	MΩ
Timing capacitor	0.01		1000	μF
Counter input frequency (Pin 14)		1.5		MHz
Pull-up resistor, time-base output		20		kΩ
Trigger and reset input pulse voltage	2	3		V
Trigger and reset input pulse duration	2			μs
External clock input pulse voltage	3			V
External clock input pulse duration	1			μs

NOTE 2: For operation with $V_{CC} \leq 4.5$ V, short regulator output to V_{CC}.

electrical characteristics at 25°C free-air temperature

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator output voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	3.9	4.4		V
	2	V_{CC} = 15 V, Trigger and reset open or grounded	5.8	6.3	6.8	
Modulation input open circuit voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	2.8	3.5	4.2	V
		V_{CC} = 15 V, Trigger and reset open or grounded		10.5		
Trigger threshold voltage	1	V_{CC} = 5 V, Reset at 0 V		1.4	2	V
High-level trigger current	1	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V		10		μA
Reset threshold voltage	1	V_{CC} = 5 V, Trigger at 0 V		1.4	2	V
High-level reset current	1	V_{CC} = 5 V, Trigger at 0 V		10		μA
Counter input (time base) threshold voltage	2	V_{CC} = 5 V, Trigger and reset open or grounded	1	1.4		V
Low-level output current, Q0 thru Q7	2	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V, V_{OL} < 0.4 V	2	4		mA
High-level output current, Q0 thru Q7	2	V_{OH} = 15 V, Reset at 2 V, Trigger at 0 V		0.01	15	μA
Supply current	1	V_{CC} = 5 V, Trigger at 0 V, Reset at 5 V		4	7	mA
	1	V_{CC} = 15 V, Trigger at 0 V, Reset at 5 V		13	18	
	3	V+ = 4 V		1.5		

operating characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Initial error of time base‡	1	V_{CC} = 5 V, Trigger at 5 V, Reset at 0 V			±0.5	±5	%
Temperature coefficient of time-base period	1	T_A = 0°C to 70°C	V_{CC} = 5 V		−200		ppm/°C
			V_{CC} = 15 V		−80		
Supply voltage sensitivity of time-base period	1	V_{CC} ≥ 8 V			−0.08	−0.3	%/V
Time-base output frequency	1	V_{CC} = 5 V, R = MIN, C = MIN			130		kHz
Propagation delay time		see Note 3	From trigger input		1		μs
			From reset input		0.8		
Output rise time	2	R_L = 3 kΩ, C_L = 10 pF	Q0 thru Q7		180		ns
Output fall time					180		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This is the time-base period error due only to the uA2240C and expressed as a percentage of nominal (1.00 RC).
NOTE 3: Propagation delay time is measured from the 50% point on the leading edge of an input pulse to the 50% point on the leading edge of the resulting change of state at Q0.

PARAMETER MEASUREMENT INFORMATION

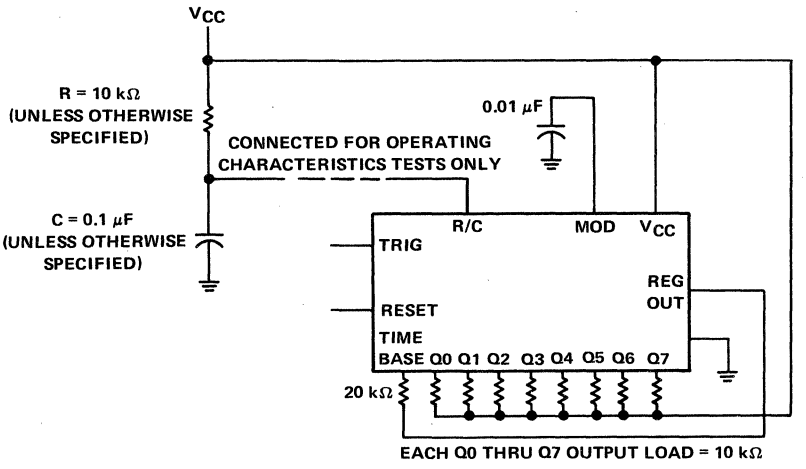


FIGURE 1. GENERAL TEST CIRCUIT

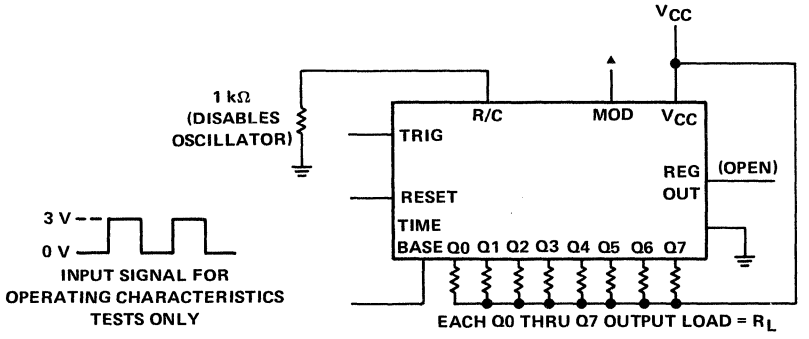


FIGURE 2. COUNTER TEST CIRCUIT

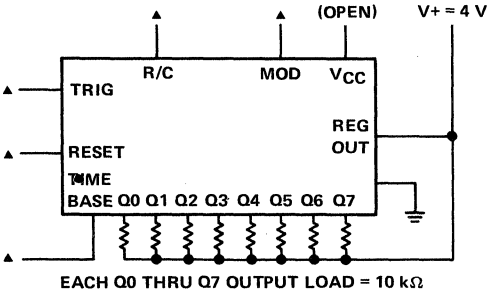


FIGURE 3. REDUCED-POWER TEST CIRCUIT (TIME BASE DISABLED)

▲These connections may be open or grounded for this test.

TYPICAL CHARACTERISTICS

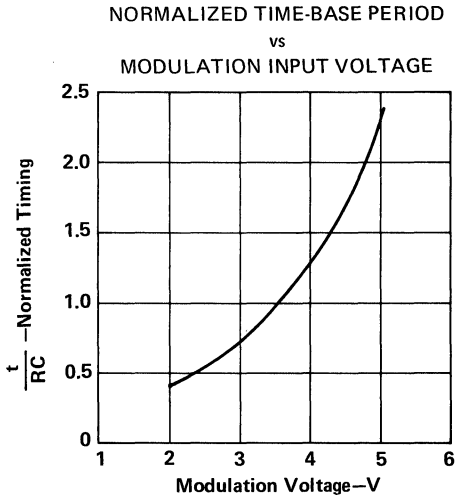


FIGURE 4

TYPICAL APPLICATION INFORMATION

Figure 5 shows voltage waveforms for typical operation of the uA2240C. If both reset and trigger inputs are low during power-up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240C will ignore any further signals at the trigger input until after a reset signal is applied to the reset input. With the trigger input low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while the trigger input is high, the reset is ignored. If the reset input remains high when the trigger input goes low, the uA2240C will reset.

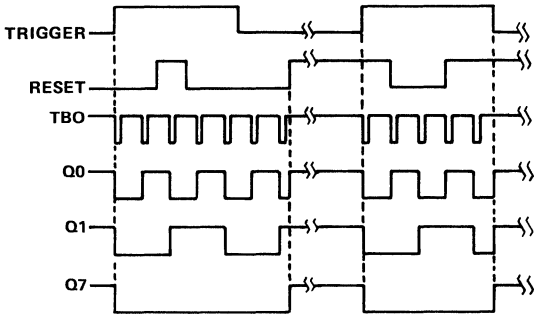


FIGURE 5. TIMING DIAGRAM OF OUTPUT WAVEFORMS

TYPICAL APPLICATION INFORMATION

In monostable applications of the uA2240C, one or more of the binary outputs will be connected to the reset terminal as shown in Figure 6. The binary outputs are open-collector stages that can be connected together to a common pull-up resistor to provide a "wired-OR" function. The combined output will be low as long as any one of the outputs is low. This type of arrangement can be used for time delays that are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the reset input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 are connected to reset, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240C will free-run from the time it is triggered until it receives an external reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitor connected as shown in Figure 6 when the modulation input is open (approximately 3.5 V internal, see Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitor ($C < 0.1\ \mu F$), the pulse duration of the time-base oscillator may be too short to properly trigger the counters. This situation can be corrected by adding a 300-pF capacitor between the time-base output and ground. The time-base output (TBO) is an open-collector output that requires a 20-kΩ pull-up resistor to Pin 15 for proper operation. The time-base pin may also be used as an input to the counters for an external time-base or as an active-low inhibit input to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function of the dc bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external clock or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This terminal can also be used to supply voltage to additional uA2240C devices to minimize power dissipation when several timer circuits are cascaded. For circuit operation with an external clock, the regulator output can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time base, Pin 15 should be shorted to Pin 16.

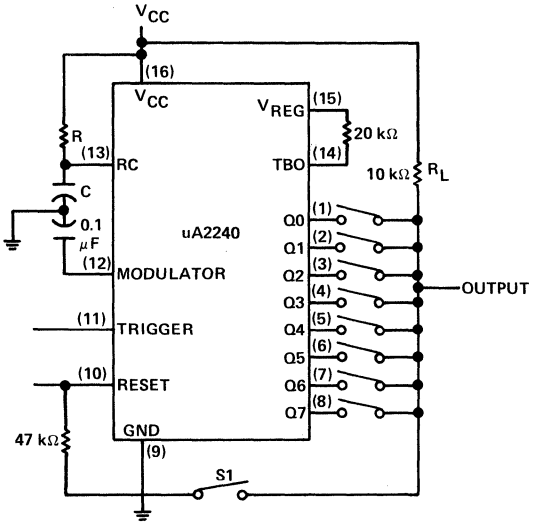


FIGURE 6. BASIC CONNECTIONS FOR TIMING APPLICATIONS

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Thermal Design Considerations 5
Mechanical Data 6

5 Thermal Design Considerations

Thermal Considerations in Design of Power Supplies Application Report

TEXAS INSTRUMENTS

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Thermal Considerations in Design of Power Supplies

Introduction

Power supply circuit designers place emphasis on suppressing transients, improving regulation, and increasing efficiency, yet minimum effort is concentrated toward thermal considerations and packaging of the power supply. Serious efforts must be given to thermal design and packaging to minimize power supply failures in the field. If sufficient attention is given to the important parameters supplied by the semiconductor manufacturers (e.g., maximum junction temperature, junction-to-case, and junction-to-ambient thermal resistance), proper heat removal can be achieved. Thermal resistance is the temperature difference between two points divided by the power dissipation, normally stated in °C/W. The reference temperature can be the ambient temperature or the temperature of a heat sink that is attached to the integrated circuit (IC) package.

Heat can be transferred from the transistor or integrated circuit package by three methods: conduction, convection, and radiation.

Conduction is the transmission of energy by a medium not involving movement of the medium itself. This method is predominant in junction to the case or from the case to a heat sink heat transfer from the semiconductor. Length, cross-section, and temperature differential of the medium are key parameters that determine conduction.

Convection is the transmission of energy or mass by a medium involving movement of the medium itself. This method is predominant in the transfer of heat from the case to ambient or a heat sink to ambient. Surface conditions, convecting fluids, velocity, and temperature difference are dominant factors in convection.

Radiation is the emission and propagation of waves transmitting energy through space or some medium. This method is important in heat transfer from the cooling-fin surface of a heat sink. Thermal emissivity, surface area, and temperature difference between radiating and adjacent mediums are key factors that determine radiation.

Basic Thermal Circuit and Symbols

Figure 1 illustrates the various heat flow paths, temperatures, and thermal resistances of a steady-state thermal model using a KC package with formed leads. A popular concept is to display this thermal model as a network of series resistors as shown in Figure 2, comparing the thermal circuit analogy to an electric circuit. Extending this Ohm's-law concept of this thermal circuit, temperature is analogous to voltage and thermal resistance to ohmic resistance. Figure 2 provides an expression for:

$$T_J = T_A + P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (1)$$

or $T_J = T_A + P_D(R_{\theta JA})$ for a regulator without external heat sink

where

T_J = junction temperature in °C
T_A = ambient air temperature in °C
$R_{\theta JC}$ = thermal resistance, junction-to-case in °C/W
$R_{\theta CS}$ = thermal resistance, case-to-heat sink °C/W
$R_{\theta SA}$ = thermal resistance, heat sink-to-ambient in °C/W
$R_{\theta JA}$ = thermal resistance, junction to ambient °C/W
P_D = power dissipated by semiconductor device in W

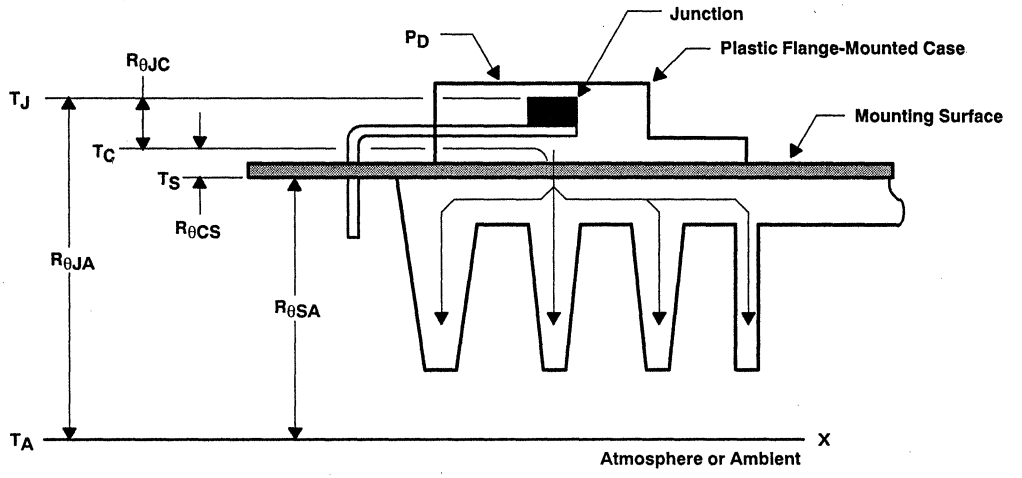

Figure 1. Semiconductor Thermal Model

The junction-to-ambient thermal resistance, $R_{\theta JA}$, can be expressed as a sum of thermal resistances listed below:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (2)$$

Equation 2 is applicable only when an external heat sink is used. If only a mounting (internal) heat sink is used, or the device does not have a heat sink, the $R_{\theta JA}$ is equal to the $R_{\theta JA}$ specified on the product data sheet. $R_{\theta JC}$ normally is given on the data sheet also, and the junction-to-case thermal resistance is a function of the material, size of the package, die area and thickness, and integrity of the die bond to the case, lead frame, or chip carrier. $R_{\theta CS}$ depends on the package, heat-sink-interface (mounting of the regulator to the heat sink) area, and integrity of the contact surface. Typical values for $R_{\theta CS}$ for different packages are shown in Table 1.

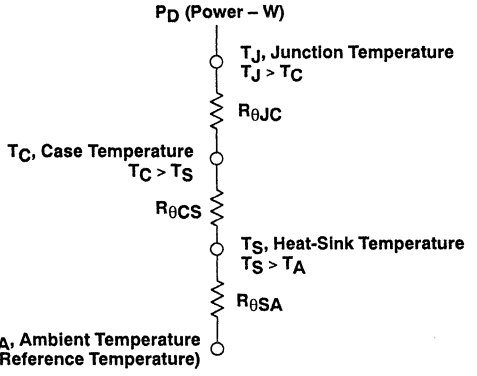

Figure 2. Basic Semiconductor Heat Sink Steady State Thermal Circuit

Table 1. $R_{\theta CS}$ for Different Types of Packages and Mounting Conditions

PACKAGE	METAL-TO-METAL	METAL-TO-METAL WITH THERMAL COMPOUND	CONTACT WITH MICA WASHER AND THERMAL COMPOUND†
TO-3	0.52°C/W	0.14°C/W	0.36°C/W
KC (TO-220)	1.1°C/W	1°C/W	1.7°C/W

† Typical values extracted from heat-sink manufacturers curves.

The $R_{\theta SA}$ found on the heat sink data sheets depends on the attributes of the heat sink and the ambient conditions. Convection and radiation are heat flow methods affecting the heat sink to ambient thermal resistance.

Typically, the ambient temperature (T_A), maximum junction temperature (T_J), power dissipation (P_D), and thermal resistance from junction-to-case ($R_{\theta JC}$) are known. To ensure safe operations of any semiconductor, the device junction temperature must be maintained below the maximum value given on the product data sheet. As with any semiconductor component, these devices have thermal and electrical limitations that must be adhered to if desired performance and service time are to be achieved. In addition, improved reliability can be obtained by selecting conservative operating procedures and thermal ranges. Normally, the electrical and thermal characteristics are interrelated with the actual operating ranges that are heavily dependent on the component application.

Thermal Design Examples

The following examples are given to illustrate the design procedure in:

1. Ascertaining the maximum allowable power dissipation of a semiconductor device
2. Determining the maximum junction-to-ambient air temperature ($T_A$max) using a mounting (internal) heat sink, or regulator without internal heat sink
3. Selecting an external heat sink by calculating the heat sink-to-ambient thermal resistance ($R_{\theta SA}$).

To ascertain the maximum allowable power dissipation of a semiconductor device, use equation 3:

$$P_D = \frac{T_J\,\text{max} - T_A}{R_{\theta JA}} \tag{3}$$

$$P_D = \frac{150°C - 75°C}{121.95°C/W} = 0.62\ W$$

where

$T_J$max = 150°C (design limit)
T_A = 75°C
$R_{\theta JA}$ = 1/derating value = 1/8.2 mW/°C (DW package) = 121.95°C/W
$T_J$max = $T_A + P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$

To ascertain the maximum T_A for an uA78M12C regulator with an internal heat sink, use equation 4:

$$T_J = T_A + P_D(R_{\theta JA}) \tag{4}$$
$$T_A = T_J - P_D(R_{\theta JA})$$
$$T_A = 125 - (0.8 \times 62.5)$$
$$T_A = 75°C$$

where

P_D = 0.8 W

T_J = 125°C

$R_{\theta JA}$ = 1/derating factor = 1/0.016 = 62.5°C/W

Derating factor of KC (TO-220) package is 16 mW/°C (from uA78M12C data sheet)

To ascertain the heat sink-to-ambient thermal resistance ($R_{\theta SA}$) for selection of an external heat sink using the uA7915C regulator, the heat sink should be mounted metal-to-metal using a thermal compound.

$$R_{\theta SA} = \frac{T_J - T_A}{P_D} - R_{\theta JC} - R_{\theta CS} \quad (5)$$

$$R_{\theta SA} = \frac{125 - 75}{3} - 4 - 1 = 11.7°C/W$$

where

P_D = 3 W

T_J = 125°C

T_A = 75°C

$R_{\theta JC}$ = 4°C/W (from the uA7915C data sheet)

$R_{\theta CS}$ = 1°C/W from Table 1 (KC or TO-220 case)

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

A Thermalloy 7019 or Staver V3-5 heat sink meets the desired requirements (see Table 3).

Table 2. Available Heat Sinks for TO-3 Packages

$R_{\theta SA}$ RANGE† °C/W	MANUFACTURER‡	
	STAVER	THERMALLOY
3 to 5	V3-5-2	6004, 6053, 6054, 6214, 6216
5 to 8	V3-3-2	6002, 6003, 6015, 6016, 6052, 6060, 6061, 6213
8 to 13	V1-3, V1-5, V3-3, V3-5, V3-7-96	6001, 6013, 6014, 6051

Table 3. Available Heat Sinks for KC (TO-220) Packages

$R_{\theta SA}$ RANGE† °C/W	MANUFACTURER‡	
	STAVER	THERMALLOY
3 to 5	V3-5-2	6072/6071
5 to 8	V3-3-2	6072, 7021, 7025
8 to 13	V3-3, V3-5	6021, 6030, 6032, 7019, 7020

† All values are typical as determined from characteristic curves received from manufacturers.

‡ This table is representative of two heat sink manufacturers; many others are available.

General Suggestions for Efficient Thermal Management

Suggestions are as follows:

1. Place regulator components away from heat-dissipating components and mount hardware in an area that provides a good heat-dissipation path for the regulator.
2. For applications requiring electrical insulation of the heat sink from the regulator, use a thin (0.003-inch) mica washer. A thermal lubricant must be placed on both sides of the washer.
3. If a heat sink with fins is used with the regulator, align the fins in a vertical plane for a more efficient transfer of heat.
4. Select a heat sink with a mounting surface that has a finish and flatness comparable to the regulator package. Use thermal compounds to minimize voids, scratches, and imperfections between the mating surfaces. Use of thermal compounds with an insulating washer is more significant than with a metal-to-metal contact.
5. Attach a regulator heat sink to the regulator before soldering and mounting on the PC board. Maximum lead temperatures are 260°C for ten seconds with plastic packages or 300°C for sixty seconds for ceramic packages at a distance of 1/16th inch from case.

Conclusion

Thermal considerations in the design of power supplies are straight-forward, and with emphasis on heat reduction and conservative operating techniques, more efficient and reliable designs will be realized. The design parameters are normally under the control of the circuit designer and, with compromises, the variables can be controlled to achieve a product that will experience fewer failures in the field. On the other hand, if the thermal design considerations are overlooked or minimized, many of the power supply failures in the field may result from an inadequate thermal design approach.

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Mechanical Data	**6–5**

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example:	TL	598M	J	/883B

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN ..... TI Special Functions or Interface Products
TL, TLE ..... TI Linear Products
TLC ..... TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD ..... Analog Devices
ADC, LF, LM, LP, or MP ..... National
LT or LTC ..... Linear Technology
MC ..... Motorola
NE, SA, or SE ..... Signetics
OP ..... PMI
RC, RM, or RV ..... Raytheon
uA ..... Fairchild/National
UC ..... Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(From Individual Data Sheets)

Examples:		
	10	34070
	592	1451AC
	7757	2217-285

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FK, FN, J, JD, JG, KC, KK, KV, LP, N, NS, NT, NW, P, PK, PW, U
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

Omit /883B When Not Applicable

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JD, JG, N, NT, NS, NW, P)
– A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
– Tape and Reel
– Antistatic or Conductive Plastic Tubing

Shrink Small Outline (DB)
– Tape and Reel

Thin Shrink Small Outline (PW)
– Tape and Reel

Chip Carriers (FK, FN)
– Antistatic or Conductive Plastic Tubing

Flat (U)
– Milton Ross Carriers

Plug-In (LP)
– Plastic Bag
– Tape and Reel

Power Tab (KC, KK, KV)
– A-Channel Antistatic or Conductive Plastic Tubing

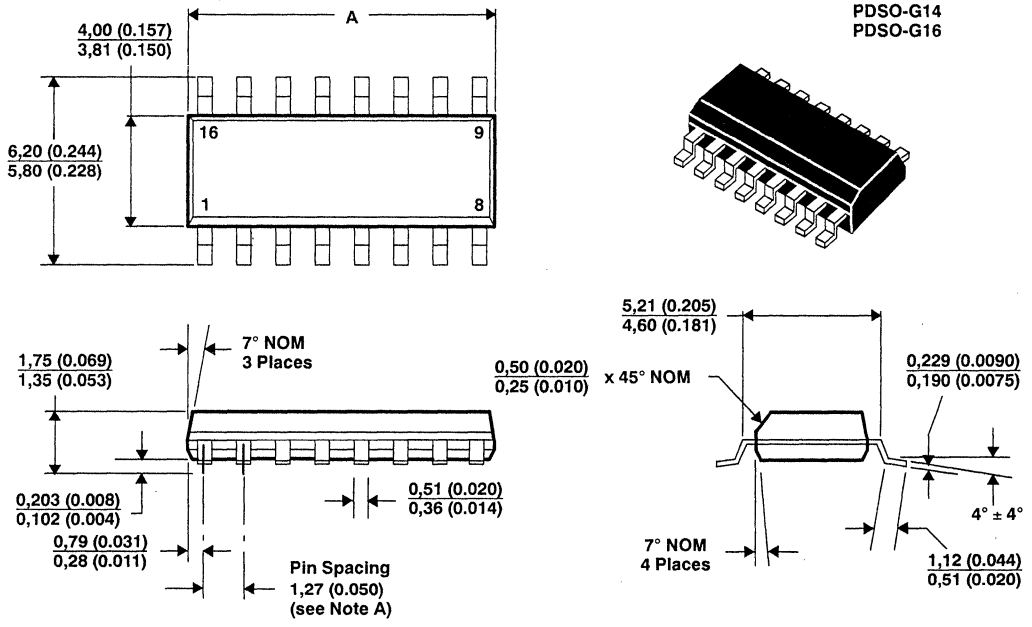
D008, D014, and D016
plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)

Designation per JEDEC Std 30:

PDSO-G8
PDSO-G14
PDSO-G16



DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

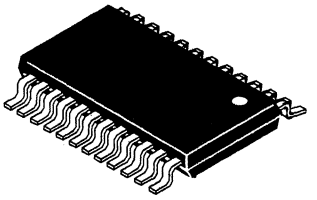
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DB008, DB014, DB016, DB020, and DB024
shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DB008, DB014, DB016, DB020, and DB024
(24-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G8
PDSO-G14
PDSO-G16
PDSO-G20
PDSO-G24



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold or flash end protrusion shall not exceed 0,15 mm.
D. Interlead flash shall be controlled by TI statistical process control (additional information available through TI field office).
E. Lead tips to be planar within ±0,05 mm exclusive of solder.

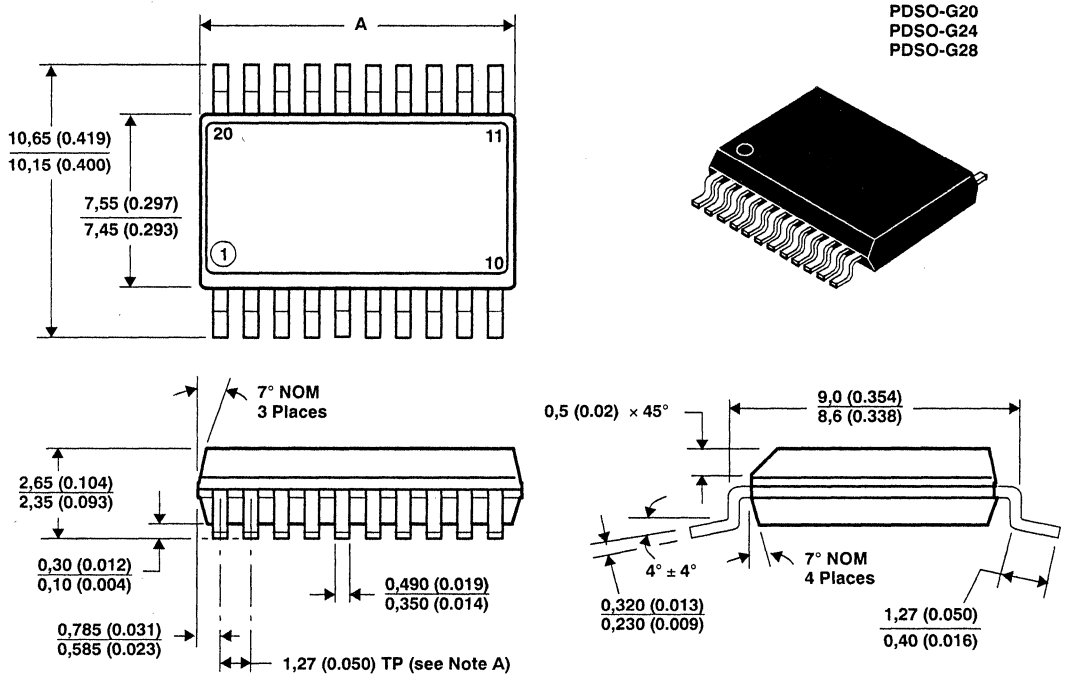
DIM \ PINS	8	14	16	20	24
A MIN	2,70	5,90	5,90	6,90	7,90
A MAX	3,30	6,50	6,50	7,50	8,50
B MAX	0,68	1,30	0,98	0,83	0,68

DW016, DW020, DW024, and DW028
plastic small-outline packages

Each of these small-outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G16
PDSO-G20
PDSO-G24
PDSO-G28



DIM \ PINS	16	20	24	28
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

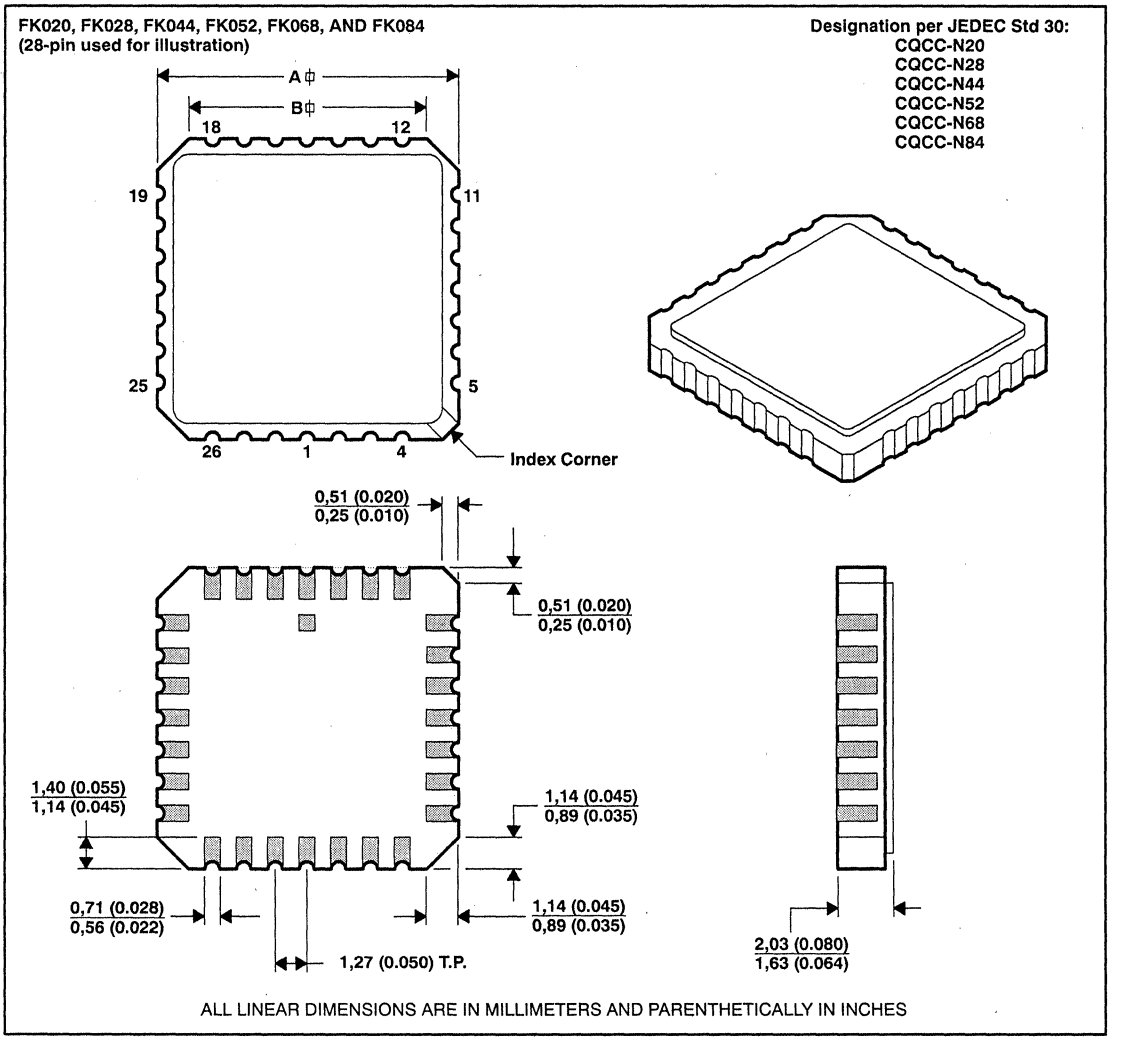
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed, 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. These packages are intended for surface mounting on solder leads on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.



NOTES: A. See next page for A and B dimensions.

FK020, FK028, FK044, FK052, FK068, and FK084 ceramic chip carrier (continued)

JEDEC OUTLINE DESIGNATION†	NUMBER OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS-004-CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS-004-CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS-004-CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS-004-CE	52	18,78 (0.740)	19,32 (0.760)	12,58 (0.495)	14,22 (0.560)
MS-004-CF	68	23,83 (0.938)	24,43 (0.962)	21,60 (0.850)	21,80 (0.858)
MS-004-CG	84	28,99 (1,141)	29,59 (1.164)	26,60 (1.047)	27,00 (1,063)

† All dimensions and notes for the specified JEDEC outline apply.

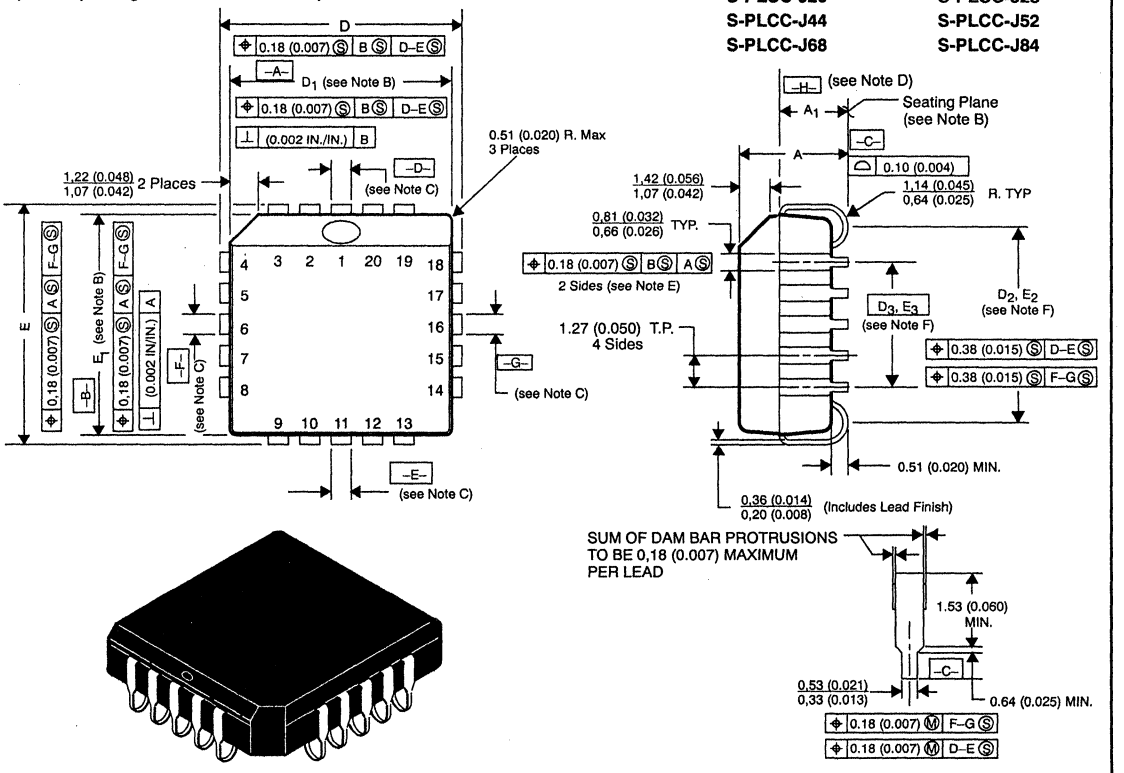
FN020, FN028, FN044, FN052, FN068, and FN084
plastic J-leaded chip carrier

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-PIN package used for illustration)

Designation per JEDEC Std 30:

S-PLCC-J20	**S-PLCC-J28**
S-PLCC-J44	**S-PLCC-J52**
S-PLCC-J68	**S-PLCC-J84**



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: B. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

C. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

D. Datums [D – E] and [F – G] for center leads are determined at datum [– H –].

E. Datum [– H –] is located at top of leads where they exit plastic body.

F. Location of datums [– A –] and [– B –] to be determined at datum [– H –].

G. Determined at seating plane [– C –].

FN020, FN028, FN044, FN052, FN068, and FN084 plastic J-leaded chip carrier (continued)

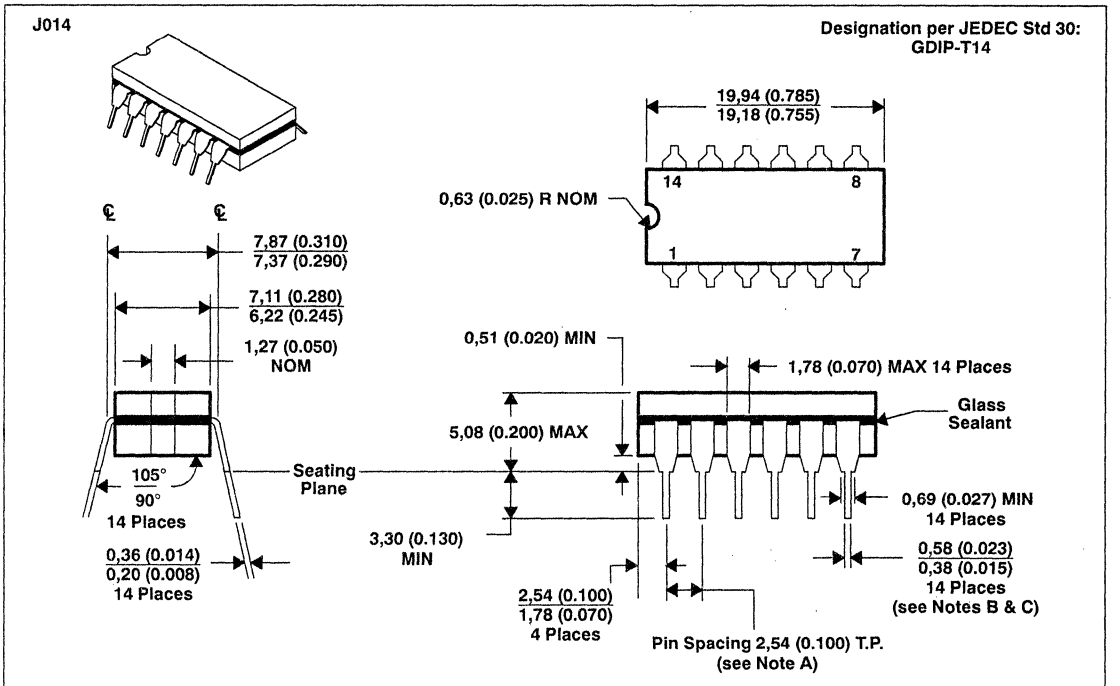
JEDEC	NO.OF	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
OUTLINE	PINS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 90.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.141)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES A: All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

F: Determined at seating plane $\boxed{-C-}$.

J014
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



Falls within JEDEC TO–116 and EIA MO–001AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

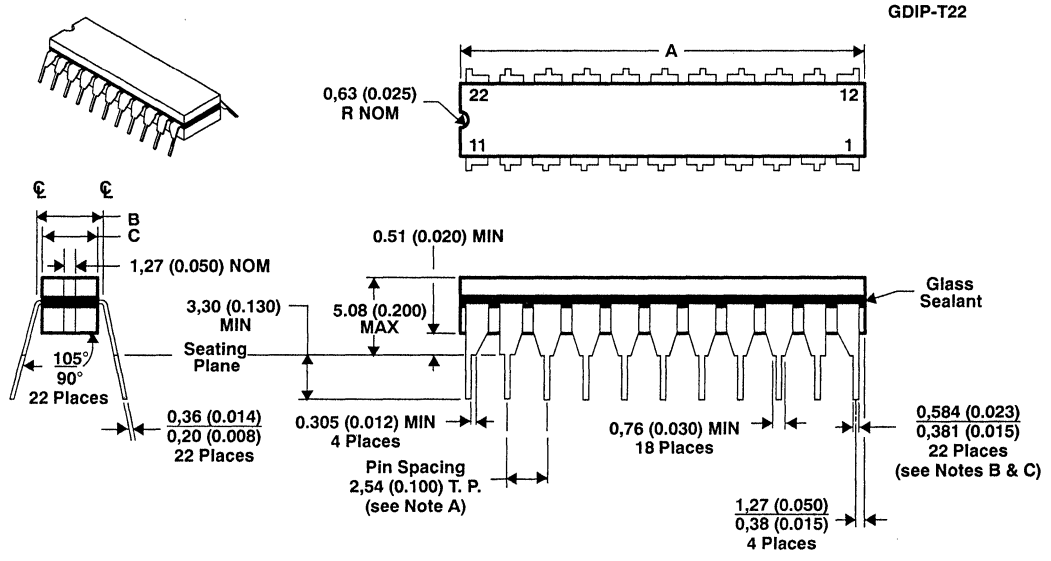
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

J016, J018, J020, and J022 ceramic dual-in-line

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. These packages are intended for insertion in mounting-hole rows of 7,62 (0.300) centers for the J016, J018, J020, and 10,16 (0.400) centers for the J022, respectively. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (bright-dipped) leads require no additional cleaning or processing when used in solder assembly.

J016, J018, J020, and J022
(22-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP-T16
GDIP-T18
GDIP-T20
GDIP-T22



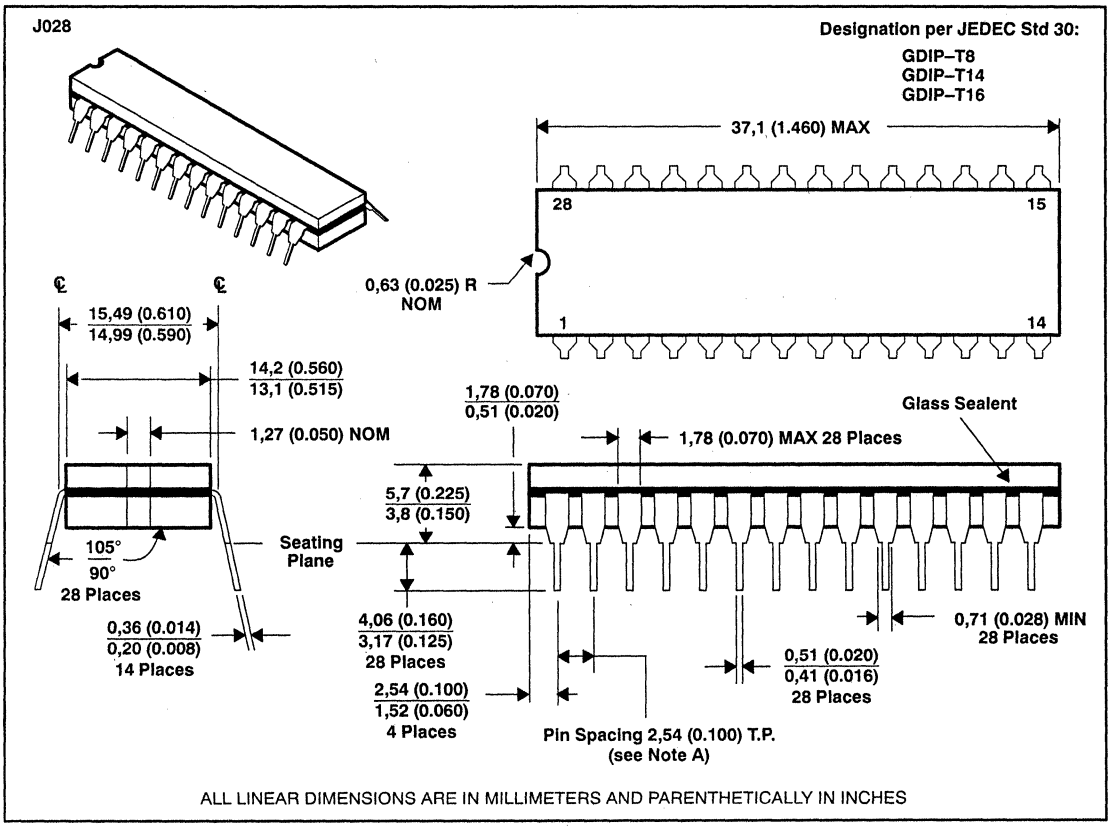
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

DIM / PINS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
16	19,18 (0.755)	19,94 (0.785)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
18		23,1 (0.910)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
20	23,62 (0.930)	24,76 (0.975)	7,37 (0.290)	7,87 (0.310)	6,22 (0.245)	7,62 (0.300)
22		28,0 (1.100)	9,91 (0.390)	10,41 (0.410)		9,65 (0.388)

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J028
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



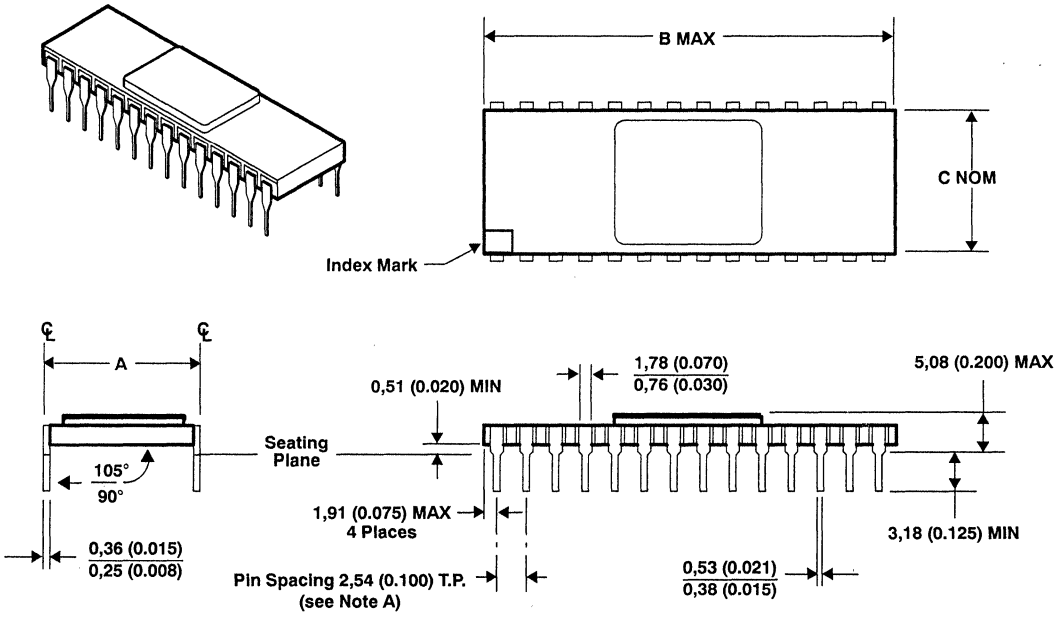
NOTES: D. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
E. This dimension does not apply for solder-dipped leads.
F. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

JD024 and JD028
ceramic side-braze dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, metal cap, and side-brazed tin-plated leads. These packages are intended for insertion in mounting-hole rows of 15,24 (0.600) centers. Leads require no additional cleaning or processing when used in solder assembly.

JD024 and JD028
(28-pin package used for illustration)

Designation per JEDEC Std 30:
GDIP–T24
GDIP–T28



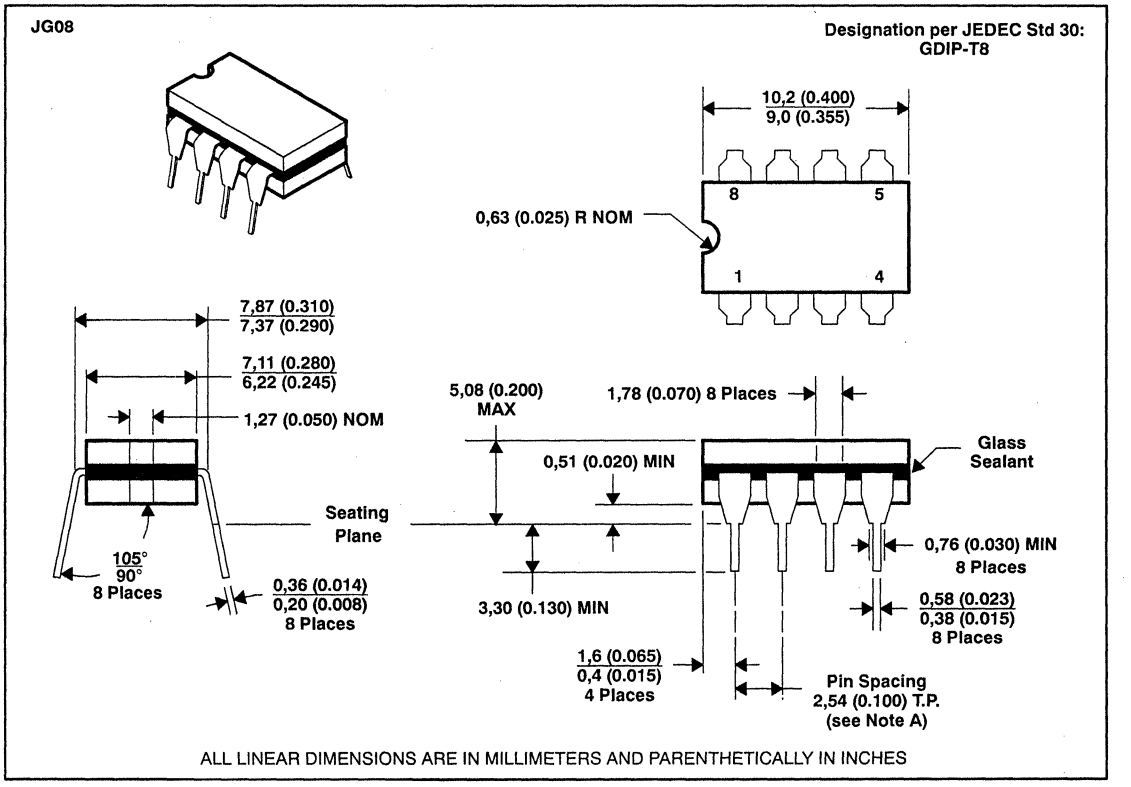
DIM \ PINS	24	28
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0.600)	15,24 (0.600)
B (MAX)	31,8 (1.250)	36,8 (1.450)
C (NOM)	15,0 (0.590)	15,0 (0.590)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

JG008
ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



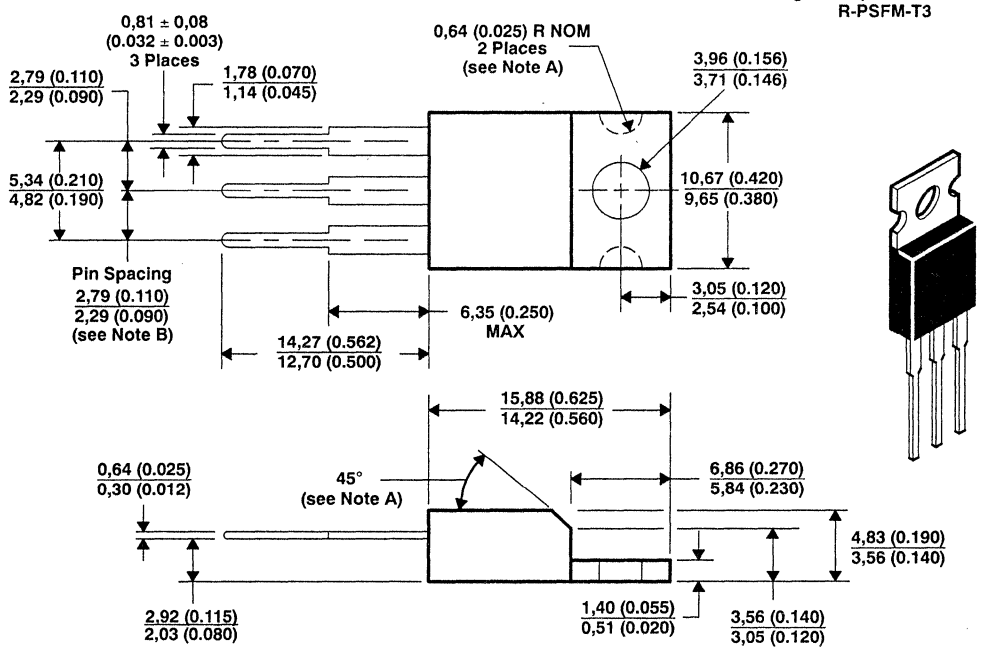
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

KC003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC003

Designation per JEDEC Std 30:
R-PSFM-T3



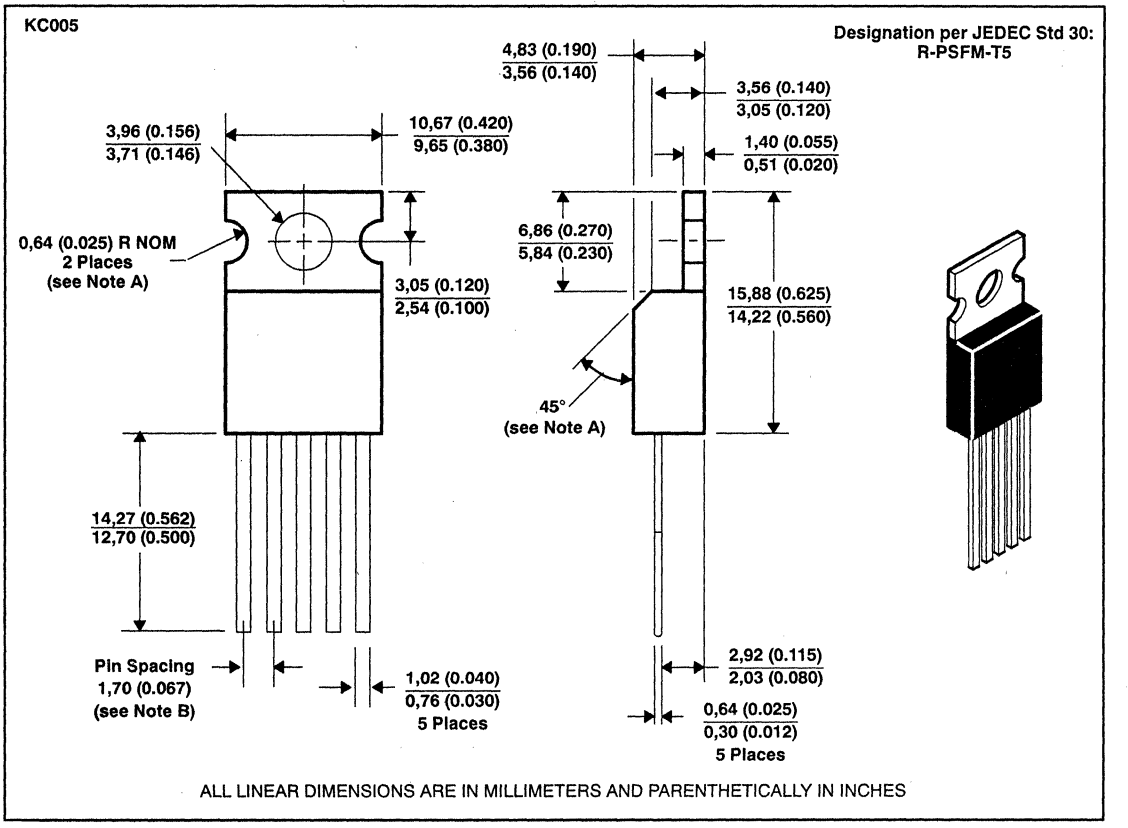
The center terminal is in electrical contact with the mounting tab.
Falls within JEDEC TO-220AB dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Notches and/or mold chamfer may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KC005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



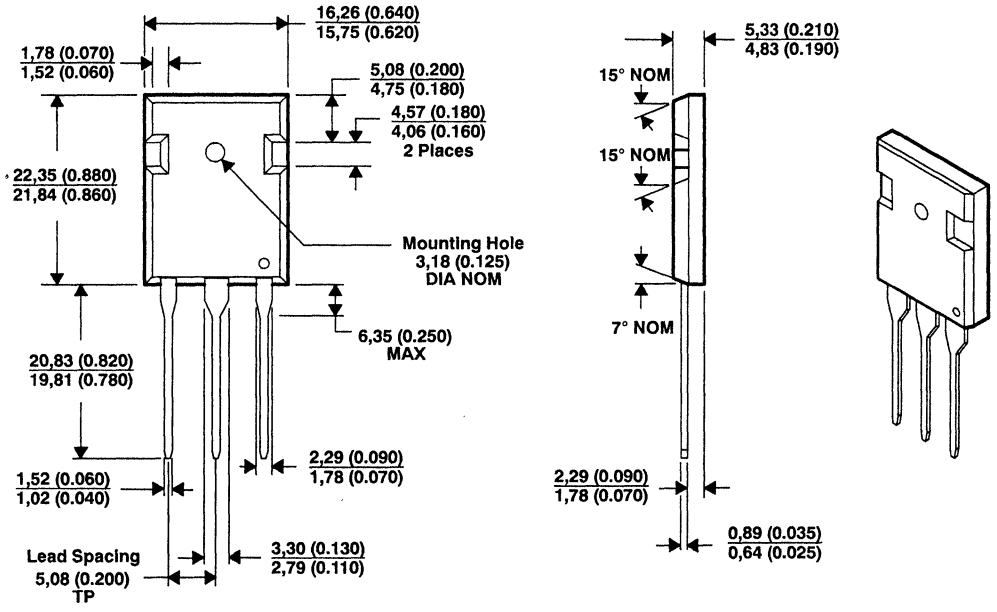
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KK003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KK003

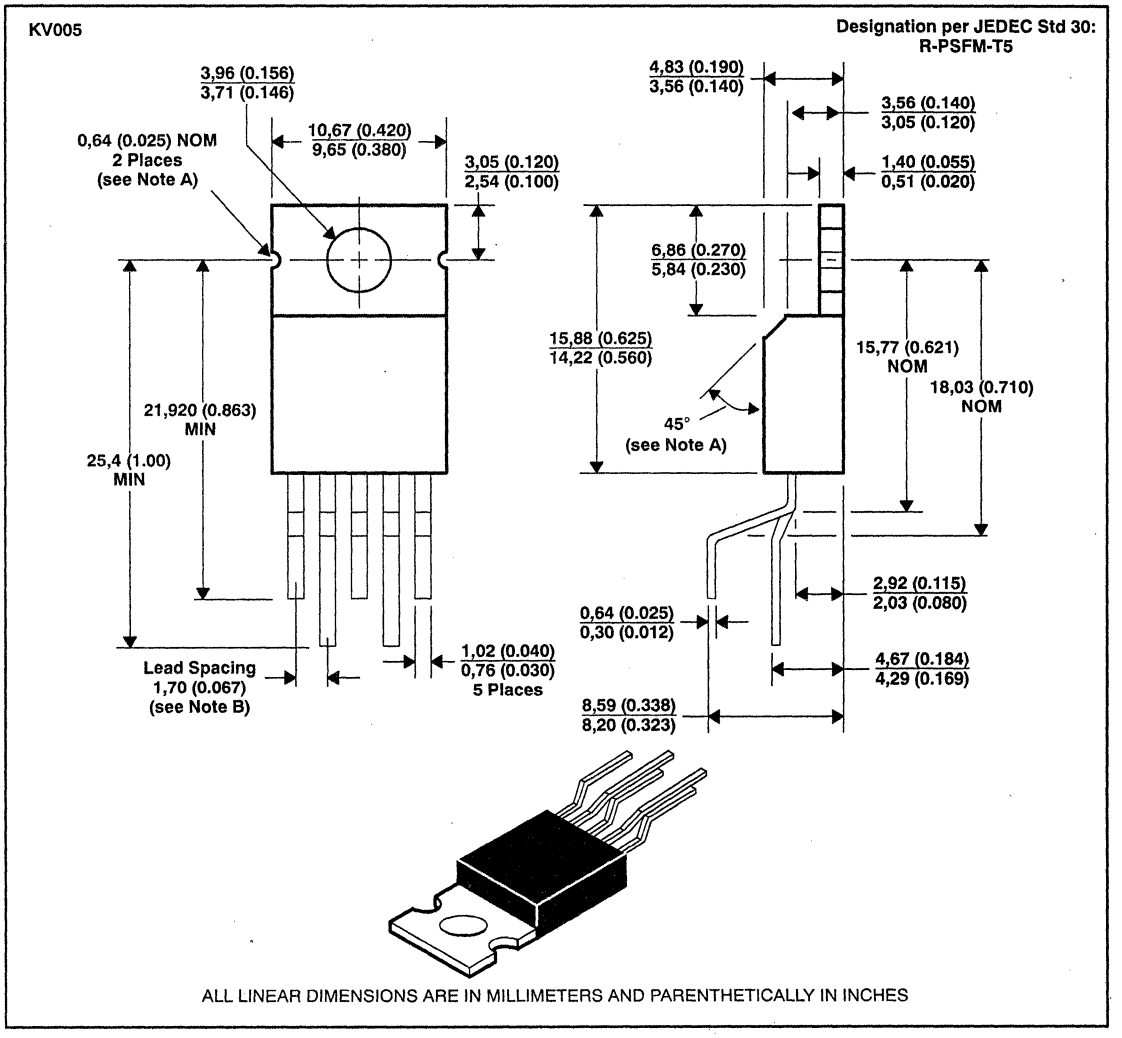
Designation per JEDEC Std 30:
X-PSFM-T3



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

KV005
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.



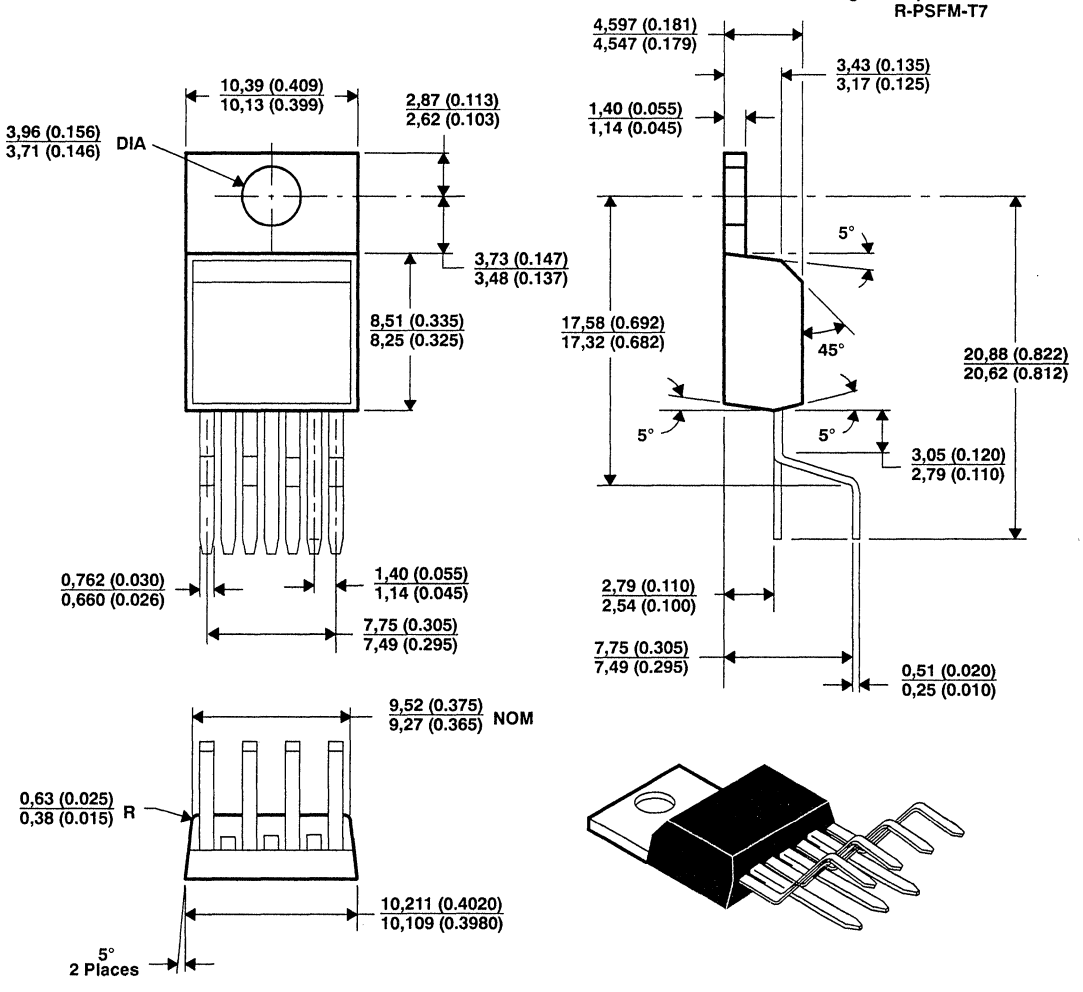
NOTES: A. Notches and chamfer may or may not be present.
B. Leads are with 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

KV007 plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KV007

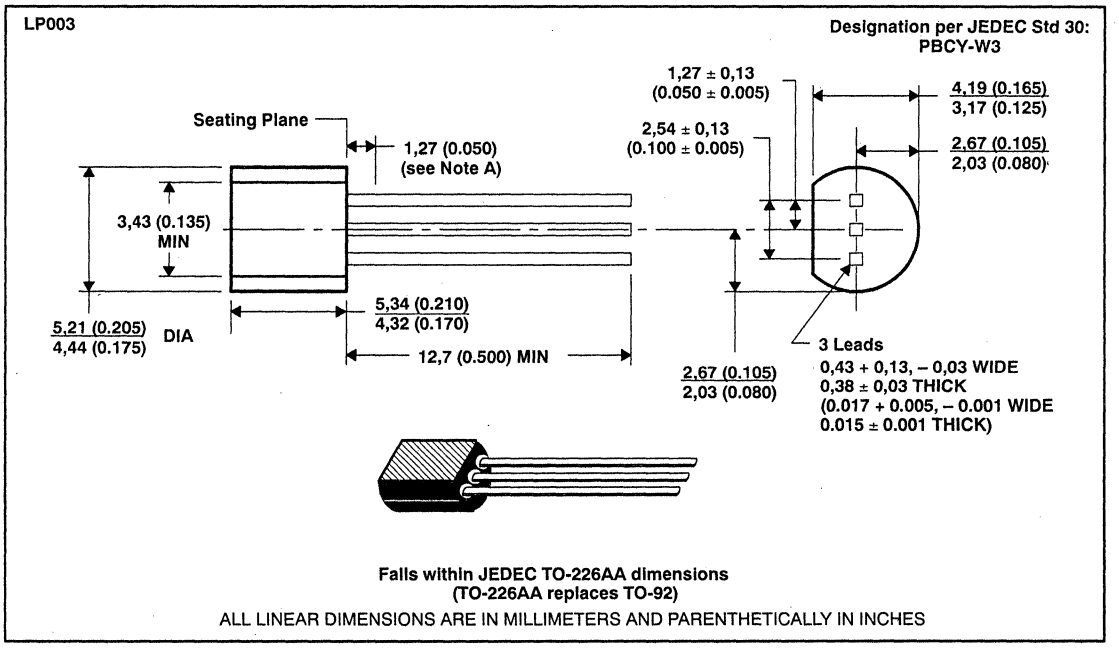
Designation per JEDEC Std 30:
R-PSFM-T7



ALL LINEAR DIMENSIONS ARE IN MILLILMETERS AND PARENTHETICALLY IN INCHES.

LP003
plastic cylindrical package

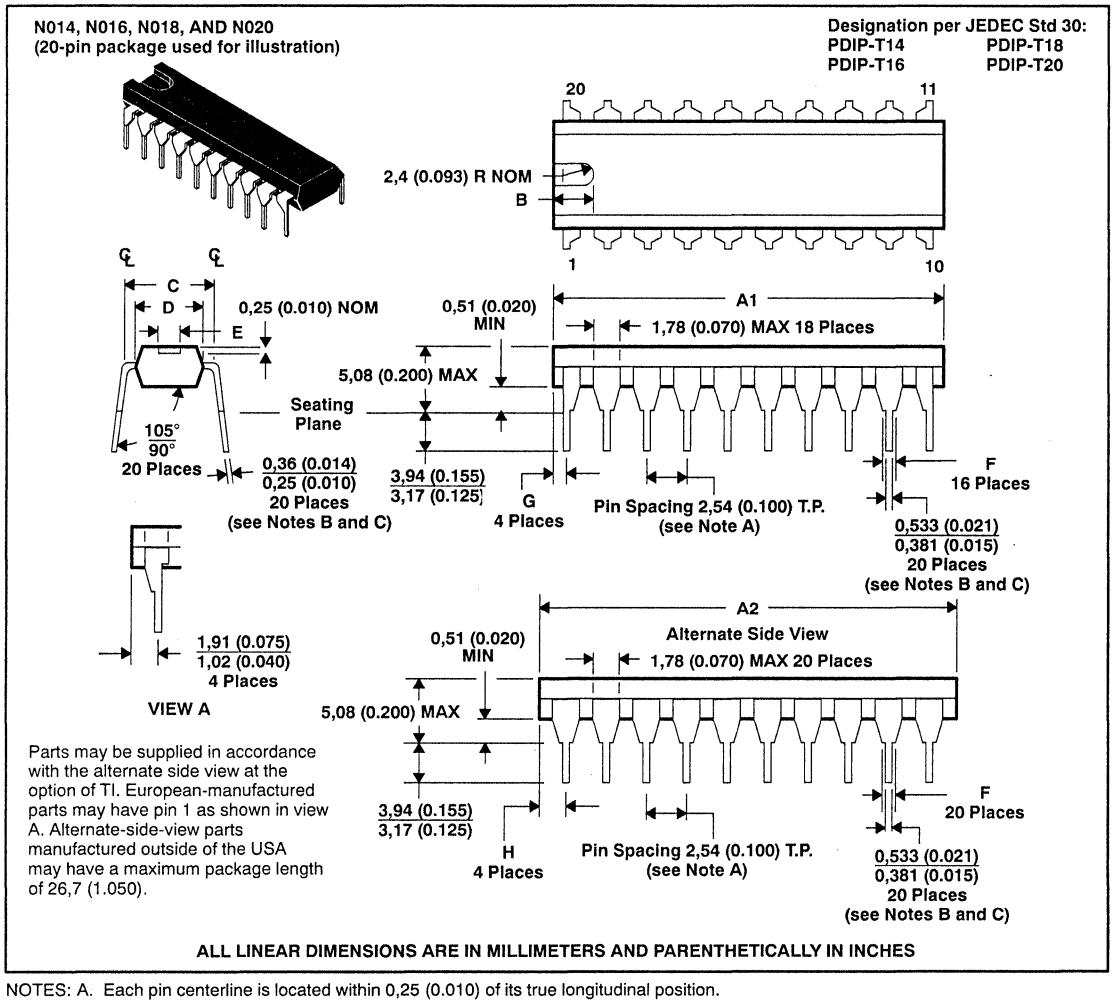
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Lead dimensions are not controlled within this area.

N014, N016, N018, and N020
300-mil plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

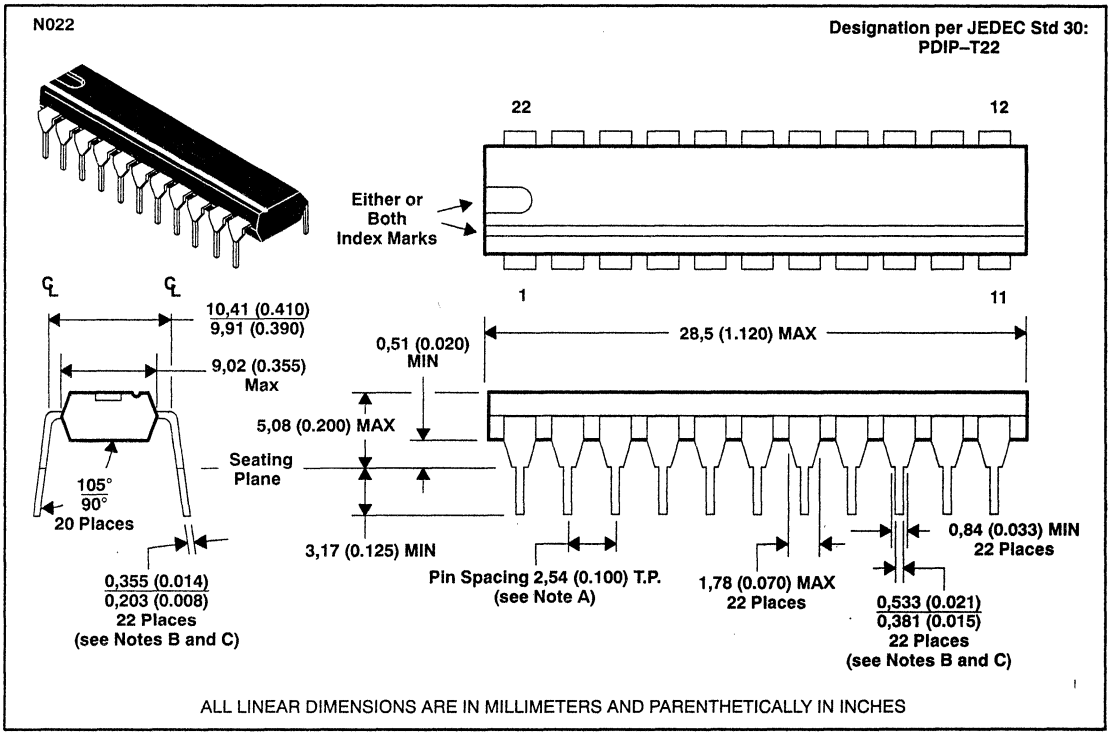
N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

DIM \ PIN		14	16	18	20
A1	MIN	18,0 (0.710)			23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
A2	MIN	18,0 (0.710)			23,62 (0.930)
	MAX	19,8 (0.780)			25,4 (1.000)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)		6,60 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	(see Note A)	0,38 (0.015)	(See Note A)	1,68 (0.066)
	MAX	(see Note A)	1,65 (0.065)	(see Note A)	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTES: A. The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety, and do not have alternate side view dimensions.

N022
400-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

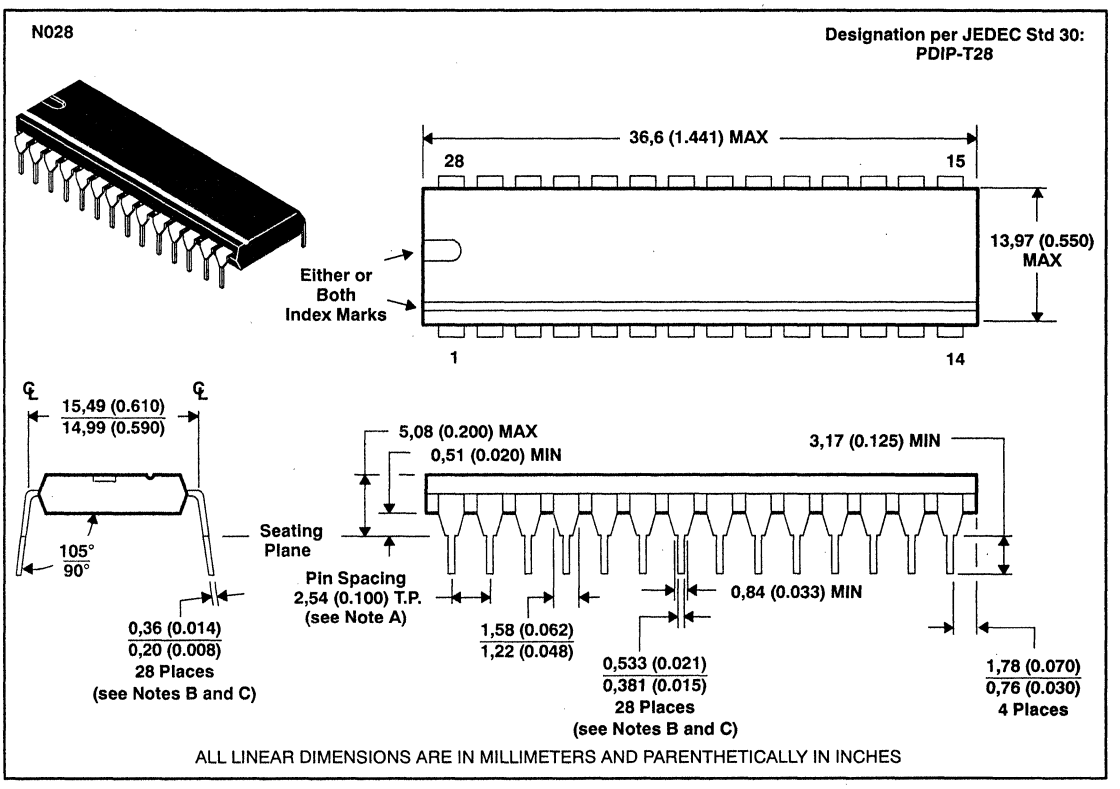


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: B. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028
600-mil plastic dual-in-line package

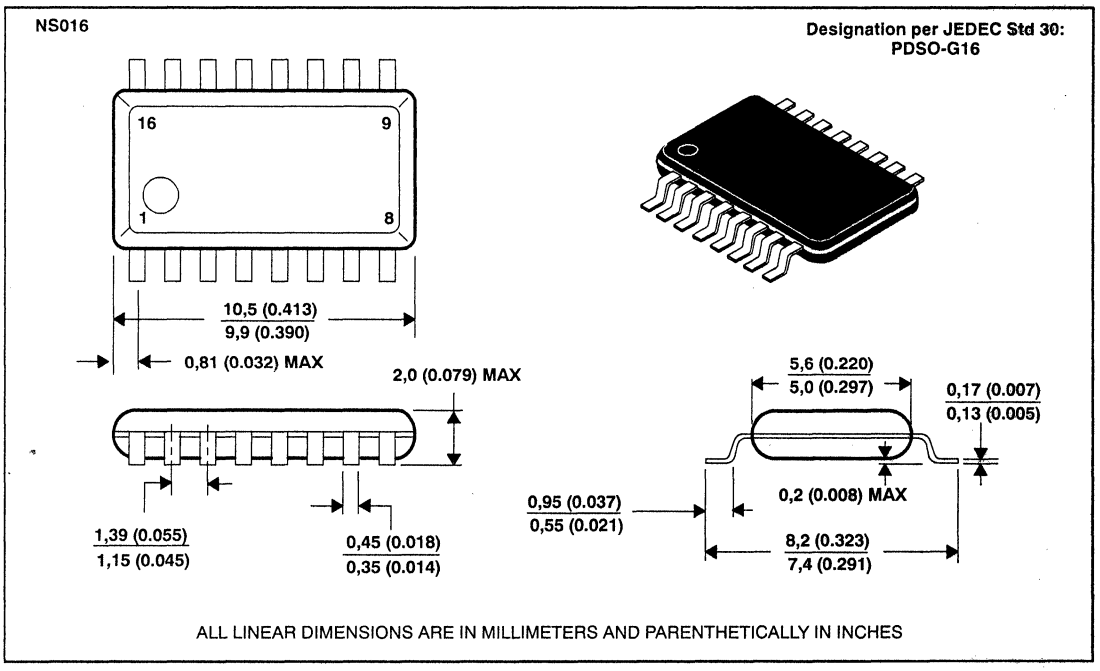
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NS016
plastic package

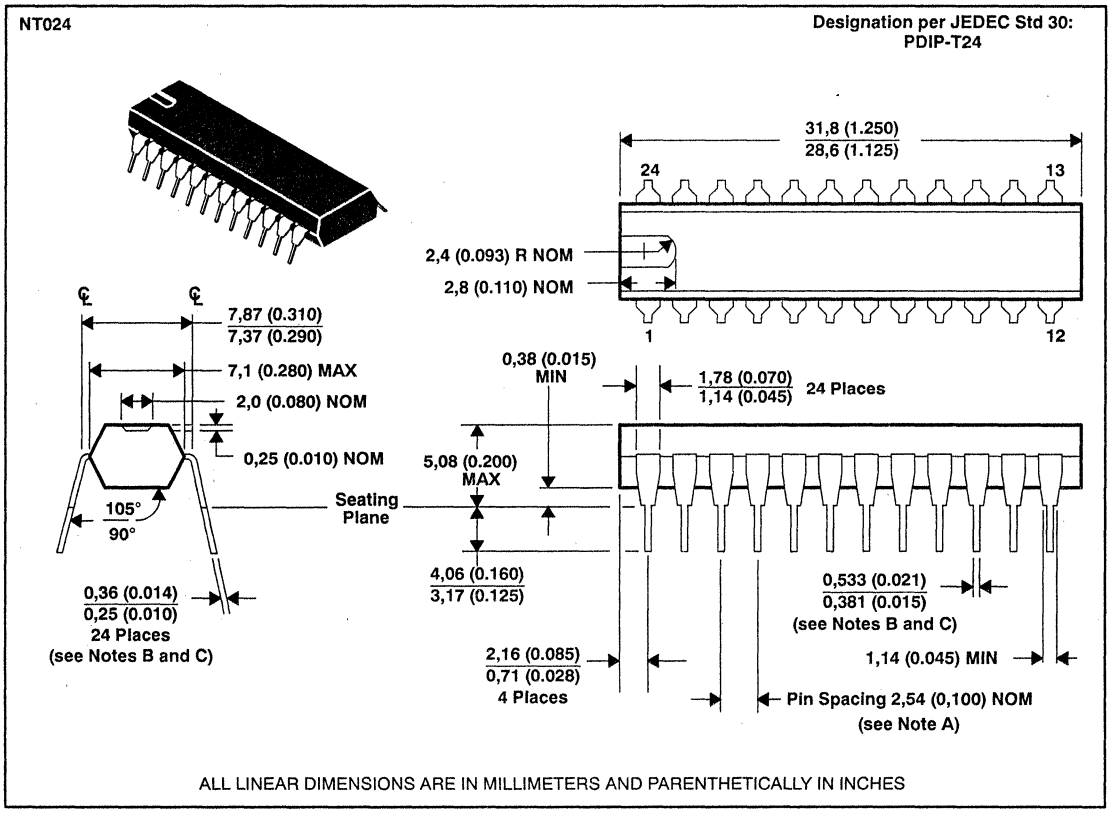
This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound withstands soldering temperature with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NT024
300-mil plastic dual-in-line packages

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers . Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin package, the letter N is used by itself since the 24-pin package may be available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

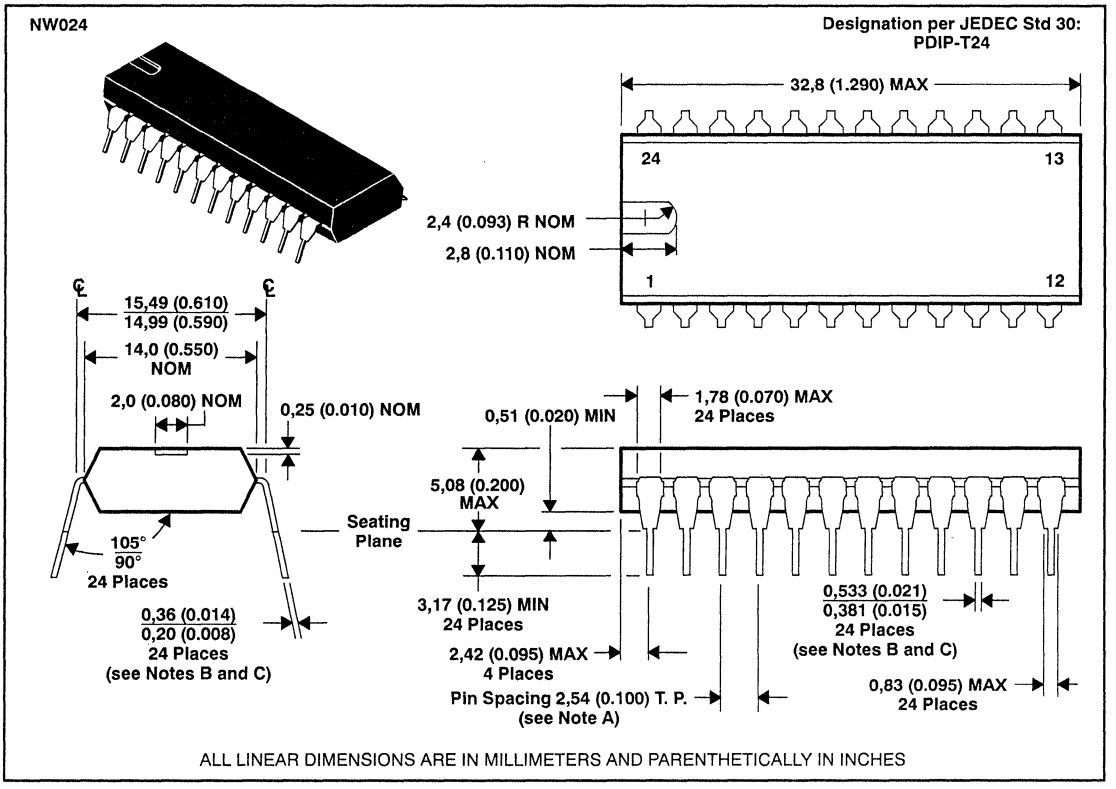


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NW024
600-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. This package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

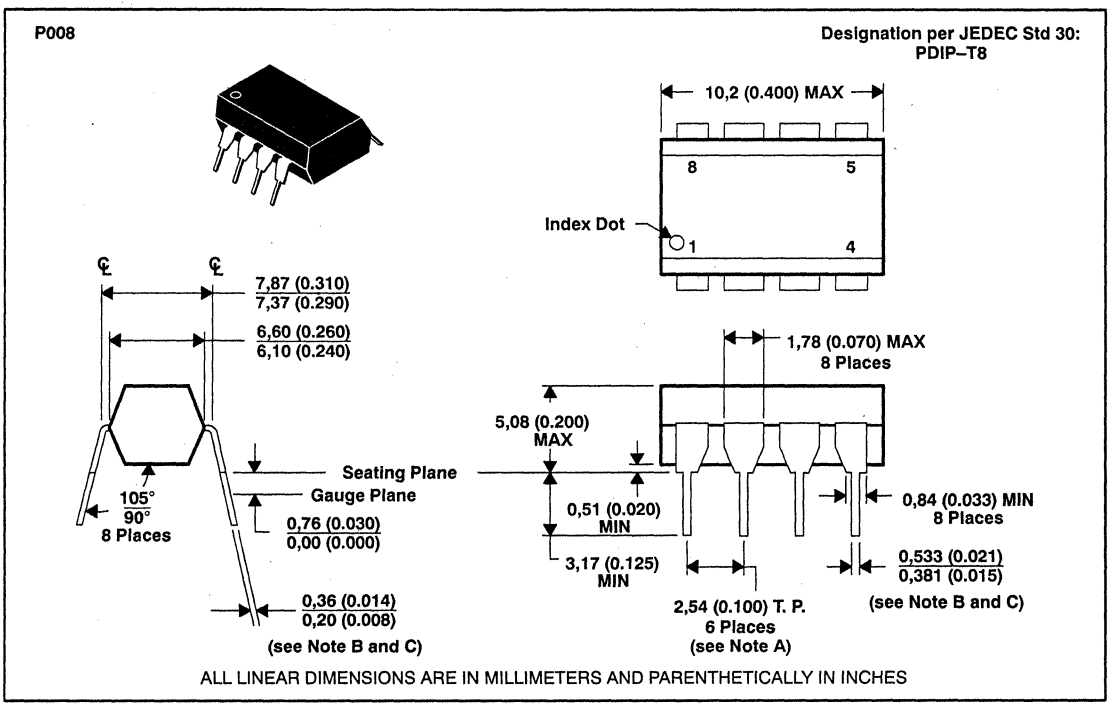
NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P008
plastic dual-in-line package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound.The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated lead require no additional cleaning or processing when used in soldered assembly.



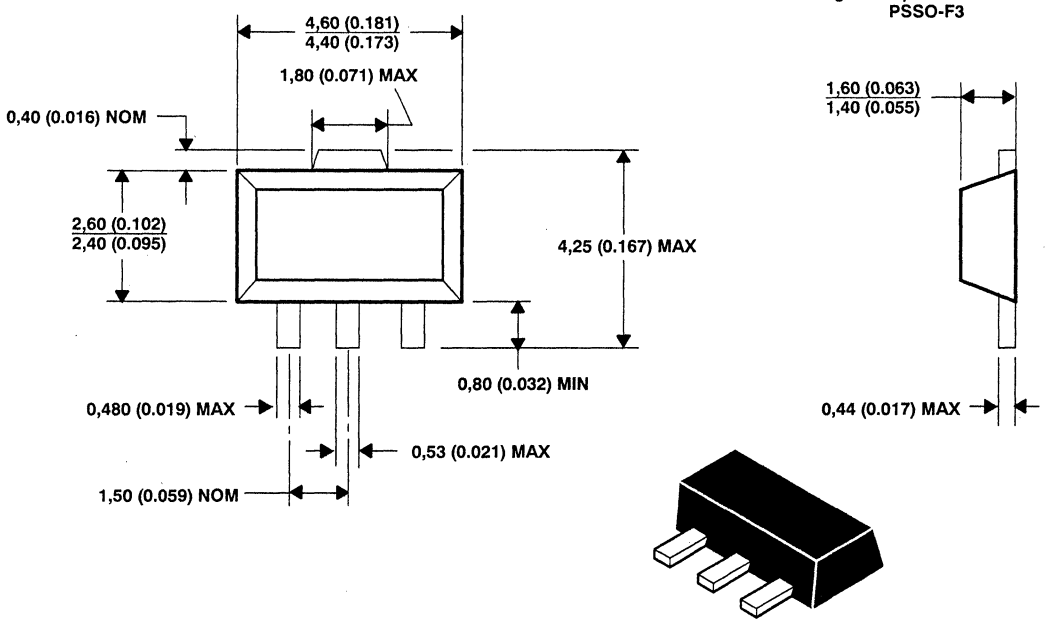
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

PK003
plastic lead-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions.

PK003

Designation per JEDEC Std 30:
PSSO-F3



The center lead is in electrical contact with the tab

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

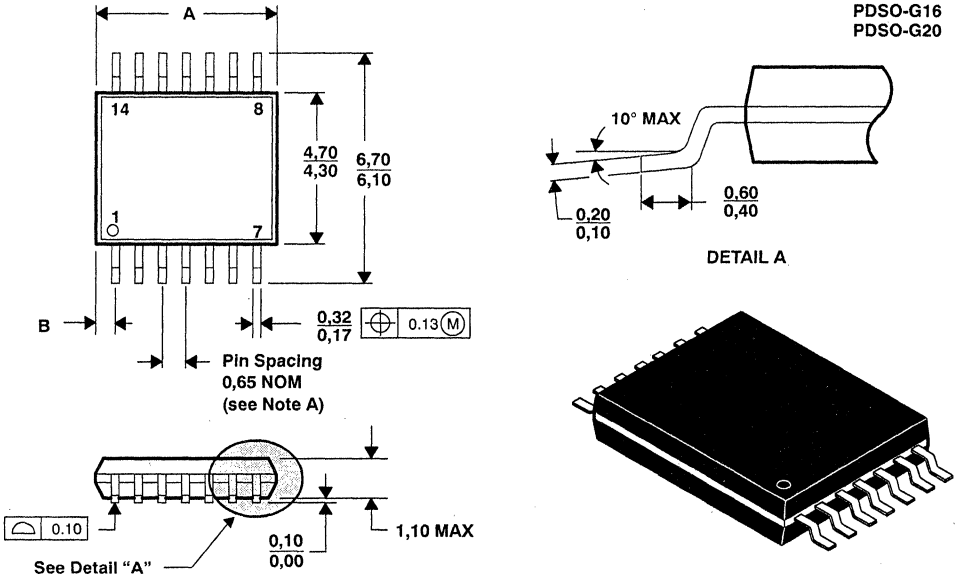
PW008, PW014, PW016, PW020
shrink small-outline packages

These shrink small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

PW008, PW014, PW016, PW020
(14-pin package used for illustration)

Designation per JEDEC Std 30:

PDSO-G8
PDSO-G14
PDSO-G16
PDSO-G20



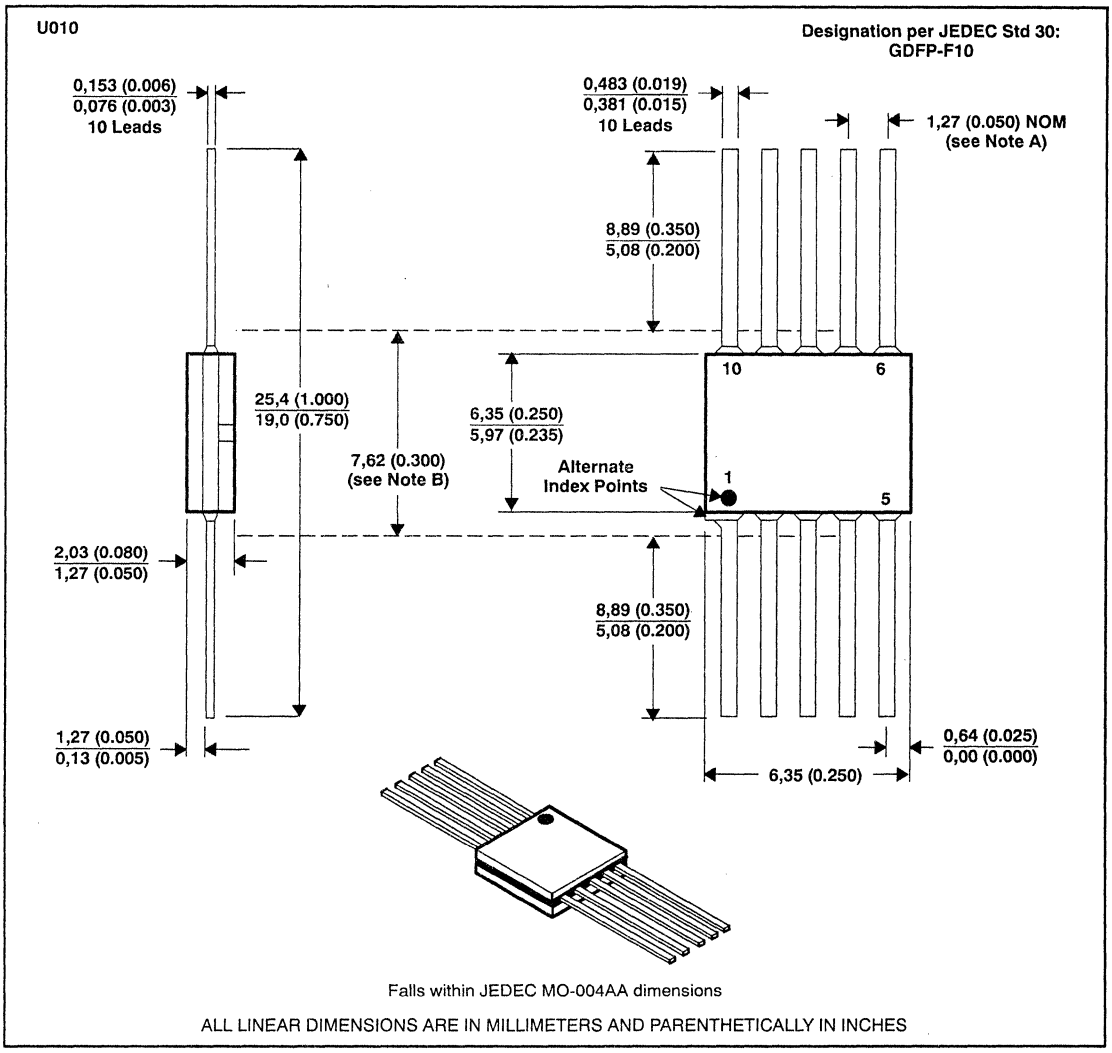
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

DIM \ PINS	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

U010
ceramic flat package

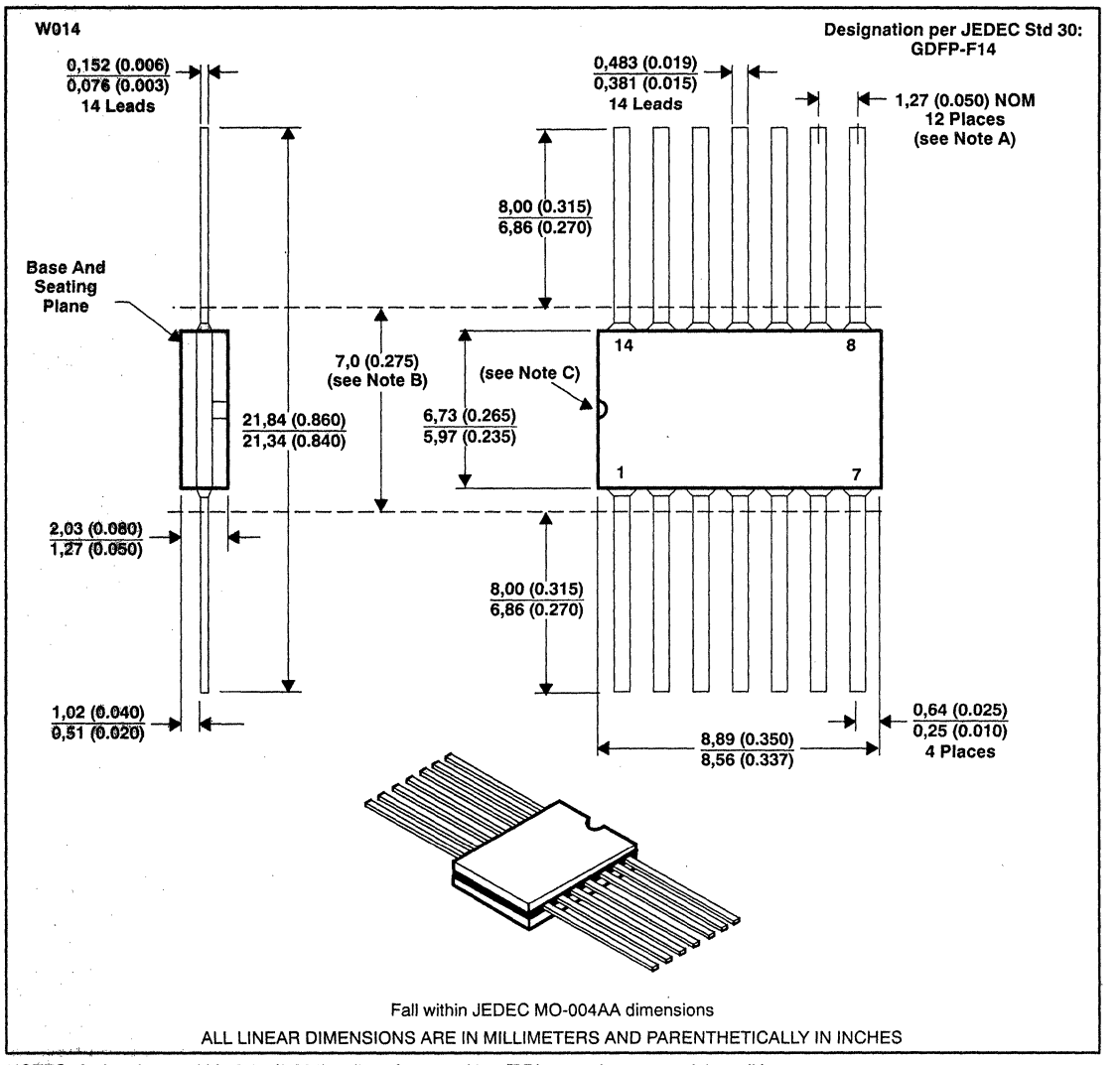
This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

W014
ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



Fall within JEDEC MO-004AA dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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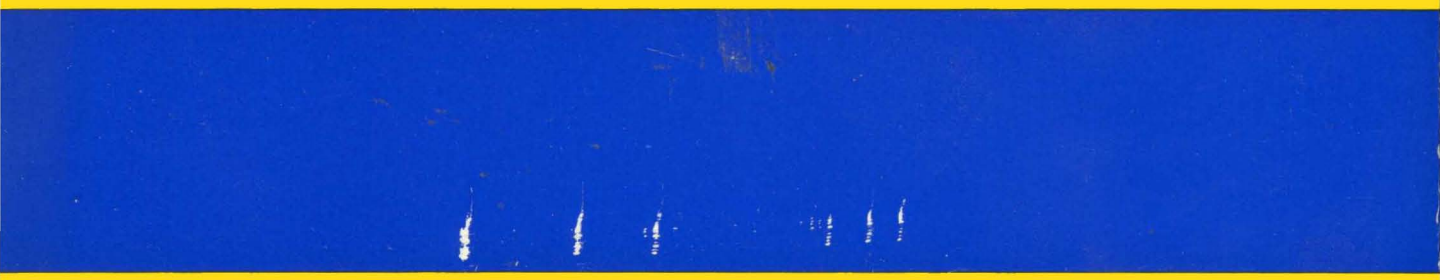

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