TEXAS INSTRUMENTS

Advanced CMOS Logic

Data Book

Data Book

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1993

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Advanced System Logic Products

Advanced CMOS Logic Data Book

TEXAS INSTRUMENTS

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INTRODUCTION

Benefits of the 1-micron EPIC™ Advanced CMOS Logic (ACL) family (54/74AC/ACT11XXX) from Texas Instruments include:

- Advanced bipolar propagation delays
- Low CMOS power consumption
- 24-mA output drive
- Significant reduction in output voltage noise

Featuring both CMOS- (AC) and TTL- (ACT) compatible functions, the new devices enhance the performance of high-speed CMOS designs or reduce power requirements in advanced bipolar designs without sacrificing the advantages of either technology.

EPIC™ ACL ensures reliable system operation by reducing simultaneous switching noise, voltage noise generated when multiple outputs are switched. A function of package inductance and the rate of change in current (di/dt), switching noise is of greater concern for ACL than for bipolar designs because of the wider swings of CMOS transistors.

Because the *end-pin* location of power and ground maximizes package inductance, conventionally-packaged ACL creates noise spikes that can lead to the loss of stored data, output glitching, and performance degradation. To ensure system reliability, the designer is forced to use noise-control techniques that detract from system performance, such as adding series resistors to device outputs.

EPIC™ ACL power and ground pins have been assigned to package center to reduce overall package inductance. Combined with a new circuit design technique called OEC™ (output edge control), which softens the edges of the output wave without compromising overall speed, center-pin packaging significantly reduces system-level noise.

The TI EPIC™ ACL family provides the following:

- 50% noise level reduction over end-pin ACL; 10% reduction over advanced bipolar devices
- Flow-through architecture that simplifies design
- Lower design cost due to lower parts count (no space sacrificed to passive components)
- A broad range of over 100 devices

This data book presents pertinent technical information on available EPIC™ ACL devices. In addition, the General Information section contains a functional index of all EPIC™ ACL devices.

Further information on TI's EPIC™ ACL and other advanced bus-interface products is available from your nearest TI field sales office, local authorized distributor, or by calling the Advanced System Logic hotline at 1-214-997-5202.

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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device

C_o **Output capacitance**
The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**
The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

I_{CEX} **Output high leakage current**
The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V.

$I_{I(hold)}$ **Input hold current**
Input current that holds the input at the previous state when the driving device goes to a high-impedance state.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{off} **Input/output power-off leakage current**
The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

*Current out of a terminal is given as a negative value.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**
The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_{dis} **Disable time (of a 3-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**
The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**
The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎏	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register (e.g., type SN74194).

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_A 0	Q_B 0	Q_C 0	Q_D 0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_A n	Q_B n	Q_C n
H	L	H	↑	X	L	L	L	L	L	L	Q_A n	Q_B n	Q_C n
H	H	L	↑	H	X	X	X	X	X	Q_B n	Q_C n	Q_D n	H
H	H	L	↑	L	X	X	X	X	X	Q_B n	Q_C n	Q_D n	L
H	L	L	X	X	X	X	X	X	X	Q_A 0	Q_B 0	Q_C 0	Q_D 0

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

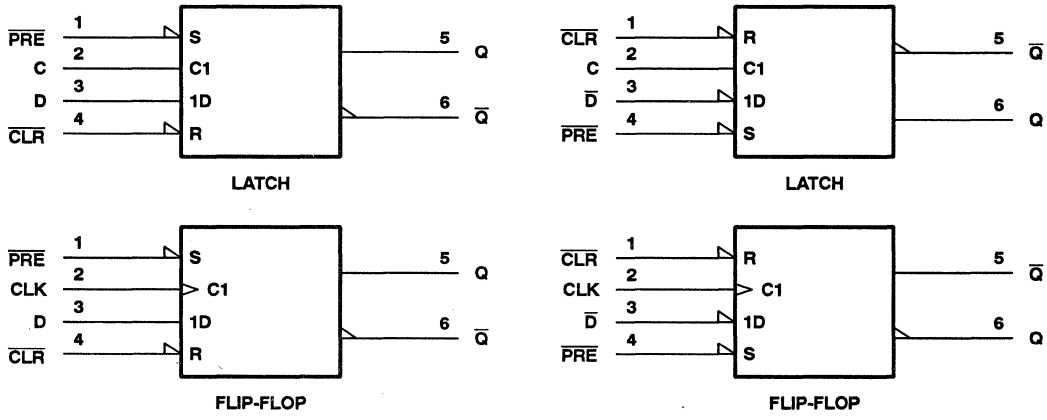
The function table does not reflect all possible combinations or sequential operating modes.

D FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the EPIC™ ACL family. In general, the junction temperature for any device can be calculated using Equation 1.

$$T_J = R_{\theta JA} \times P_T + T_A \quad (1)$$

where:

- T_J = virtual junction temperature
- $R_{\theta JA}$ = thermal resistance, junction to free air
- P_T = total power dissipation of the device
- T_A = free-air temperature

The total power consumption can be determined from Equation 2 for an AC device and Equation 3 for an ACT device.

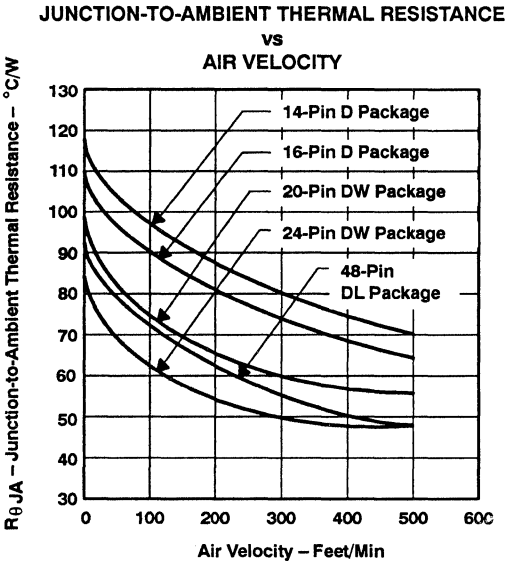


Figure 1

$$P_T = V_{CC} \times I_{CC} + N_{SW}[(C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_o)] \quad (2)$$

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + N_{SW}[(C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_o)] \quad (3)$$

where:

- V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum) (see Note 1)
- I_{CC} = quiescent supply current (specified on device data sheet)
- C_{pd} = power dissipation capacitance (from the device data sheet)
- f_i = input frequency
- C_L = output load capacitance
- f_o = output frequency
- N = number of inputs driven by a TTL device
- N_{SW} = number of outputs switching
- dc = duty cycle
- ΔI_{CC} = increase in supply current (specified on device data sheet)

NOTE 1: In system applications, I_{CC} can be minimized by keeping input voltage levels less than 1 V for V_{IL} and greater than V_{CC}–1 V for V_{IH} and input rise and fall times less than 15 ns.

The following tables outline the logic functions Texas Instruments offers in a variety of technologies. The tables are organized by function type and list all available or planned options of that function. The technology columns identify the appropriate family and a particular data book where more information can be found. The applicable literature number, composed of either seven or eight alphanumeric characters, can be found at the lower right-hand corner on the back cover of each publication.

List of additional Advanced System Logic data books:

ABT Devices	Advanced BiCMOS Technology Data Book	SCBD002A
ALS and AS Devices†	ALS/AS Logic Data Book	SDAD001B
BCT Devices†	BiCMOS Bus-Interface Logic Data Book	SCBD001B
F Devices†	F Logic (SN54/74F) Data Book	SDFD001A
FIFO Devices†	High-Performance FIFO Memories Data Book	SCAD003
HC and HCT Devices	High-Speed CMOS Logic Data Book	SCLD001C
LV, LVC, LVT, and ALVC Devices†	Low-Voltage Logic Data Book	SCBD003
SCOPE™ Devices	SCOPE™ Product Information	SSYV001
Std TTL, LS, and S Devices	TTL Logic Data Book	SDLD001A

† Updated data book planned for this technology.

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Contents (continued)

GATES

Positive-NAND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
8-Input		'30	✔	✔	✔								
		'11030						✔	✔				
13-Input		'133	✔			✔							
Dual 2-Input		'8003	✔										
Dual 4-Input		'20	✔	✔	✔	✔							
		'40	✔										
		'11020						✔	✔				
Triple 3-Input		'10	✔	✔	✔	✔							+
		'1010	✔										
		'11010						✔	✔				
Quad 2-Input		'00	✔	✔	✔	✔	✔					✔	+
		'11000						✔	✔				
		'37	✔										
	OC	'38	✔		✔								
		'132				✔							
		'11132						✔	✔				
		'1000		✔									
Hex 2-Input		'804	✔	✔									
Quad 2-Input	OC	'01	✔			✔							
		'03	✔			✔							

Positive-AND Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input	OC	'09	✔			✔							
		'7001				✔							
Dual 4-Input		'21	✔	✔	✔	✔							
		'11021						✔	✔				
Triple 3-Input		'11	✔	✔	✔	✔							
		'11011						✔	✔				
Quad 2-Input		'08	✔	✔	✔	✔	✔					✔	+
		'1008		✔									
		'11008						✔	✔				
Hex 2-Input		'808		✔									

✔ Product available in technology indicated
+ New product planned in technology indicated

GATES

Positive-OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Triple 3-Input		'4075				✔							
Quad 2-Input		'32	✔	✔	✔	✔	✔					✔	+
		'1032		✔									
		'11032						✔	✔				
		'7032				✔							
Hex 2-Input		'832	✔	✔		✔							
Dual 5-Input		'260			✔								
Triple 3-Input		'27	✔	✔	✔	✔							
		'11027						✔	✔				
Quad 2-Input		'02	✔	✔	✔	✔	✔					✔	+
	OC	'33	✔										
		'7002				✔							
		'11002						✔	✔				
Hex 2-Input		'805	✔	✔		✔							

OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs		'86	✔	✔	✔	✔							+
		'11086						✔	✔				
Quad 2-Input Exclusive-OR Gates	OC	'136	✔										
Quad 2-Input Exclusive-NOR Gates	OD	'266				✔							
		'810	✔										
	OC	'811	✔										

AND-OR Gates

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 2-Wide 2-Input, 3-Input		'51			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Hex Inverters		'04	✔	✔	✔	✔	✔					✔	+
		'U04				✔						✔	+
		'11004						✔	✔				
	OC	'05	✔			✔							
		'14				✔						✔	+
		'11014						✔	✔				
		'1004	✔	✔									
		'1005	✔										
Hex Noninverters		'11034						✔	✔				
	OC	'35	✔										
		'1034	✔	✔									
	OC	'1035	✔										

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Quad Buffers/Drivers	3S	'125			✔	✔	✔			✔	✔	✔		+	
		'126			✔	✔				✔	✔				
Noninverting Hex Buffers/Drivers	3S	'365				✔									
		'367				✔									
Inverting Hex Buffers/Drivers	3S	'368				✔									
Noninverting Octal Buffers/Drivers	3S	'241	✔	✔	✔	✔	✔			✔	✔				
		'11241						✔	✔						
		'25241									+				
		'244	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'11244						✔	✔						
		'1244	✔												
		'25244								✔	+				
		'541	✔		✔	✔	✔			✔	✔			+	
	OC	'757		✔						✔					
		'760	✔	✔						✔					
		'25760								+					
Inverting Octal Buffers/Drivers	3S	'240	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'11240						✔	✔						
		'1240	✔												
		'25240								✔					
		'466	✔												
		'540	✔			✔	✔			✔	✔			+	
	OC	'756	✔	✔						✔					
		'763	✔	✔											
Inverting and Noninverting Octal Buffers/Drivers	3S	'230		✔											
	OC	'762		✔											
Triple 4-Input OR/NOR Drivers		'11802							✔						
Noninverting 10-Bit Buffers/Drivers	3S	'827									✔				
		'11827						✔	✔						
		'29827	✔							✔					
Inverting 10-Bit Buffers/Drivers	3S	'828									+				
		'11828						✔	✔						
		'29828	✔							✔					
Noninverting 16-Bit Buffers/Drivers	3S	'16241							✔		✔				
		'16244						✔	✔		✔	✔		+	+
		'16541							✔		✔				

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY											
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Inverting 16-Bit Buffers/Drivers	3S	'16240						✔	✔		✔			+	+
		'16540							✔		✔				
Noninverting 18-Bit Buffers/Drivers	3S	'16825							✔		✔				
Inverting 18-Bit Buffers/Drivers	3S	'16826									+				
Noninverting 20-Bit Buffers/Drivers	3S	'16827							✔		✔				+
Inverting 20-Bit Buffers/Drivers	3S	'16828									+				+
Octal Buffers/Drivers With Input Pullup Resistors		'746	✔												

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY							
			AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16500					+			+
		'16500B				✔				
Noninverting 18-Bit Universal Bus Transceivers (UBT™)	3S	'16501				✔	+		+	+
		'16600				✔				+
		'16601				✔				+
Noninverting 36-Bit Universal Bus Transceivers (UBT™)	3S	'32501				✔				
Noninverting 16-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32316				✔				
Noninverting 18-Bit Tri-Port Universal Bus Exchangers (UBE™)	3S	'32318				✔				
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500				+				
		'162501				+				
		'162600				+				
		'162601				✔				
SCOPE™ 18-Bit Universal Bus Transceivers (UBT™)	3S	'18502				✔	+			
SCOPE™ 20-Bit Universal Bus Transceivers (UBT™)	3S	'18504				✔	+			

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting Quad Transceivers	3S	'243	✔		✔										
Inverting Quad Transceivers	OC	'758	✔												
	3S	'242			✔										
Noninverting Octal Transceivers	3S	'245	✔	✔	✔	✔	✔			✔	✔	✔	✔	+	
		'1245	✔												
		'11245						✔	✔						
		'25245								✔	✔				
		'645	✔	✔		✔	✔								
		'1645	✔												
	OC	'621	✔		✔										
		'641	✔	✔											
	OC/3S	'639	✔	✔											
Inverting Octal Transceivers	3S	'620	✔							✔	✔				
		'623	✔	✔	✔	✔	✔			✔	✔				
		'11623							✔						
		'640	✔	✔		✔				✔	✔				
		'1640	✔												
		'11640							✔						
	OC	'642	✔												
		'25642								✔					
	OC/3S	'638	✔	✔											
Noninverting 9-Bit Transceivers	3S	'863									✔			+	
		'29863	✔							✔					
Inverting 9-Bit Transceivers	3S	'29864								✔					
Noninverting 10-Bit Transceivers	3S	'861									+				
		'29861								✔					
Inverting 10-Bit Transceivers	3S	'29862								✔					
Noninverting 16-Bit Transceivers	3S	'16245						✔	✔		✔	✔		+	+
		'16623						✔	✔		✔				
Inverting 16-Bit Transceivers	3S	'16640						✔	✔		✔				
		'16620						✔	✔		+				
Noninverting 18-Bit Transceivers	3S	'16863							✔		✔				
Inverting 18-Bit Transceivers	3S	'16864									+				

✔ Product available in technology indicated
+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 20-Bit Transceivers	3S	'16861							✔		+				
Inverting 20-Bit Transceivers	3S	'16862									+				
Noninverting Octal Registered Transceivers	3S	'11470							✔						
		'543			✔					✔	✔	✔		+	
		'11543							✔						
		'646	✔	✔		✔	✔			✔	✔	✔		+	
		'646A									✔				
		'11646						✔	✔						
		'652	✔	✔		✔	✔			✔	✔	✔		+	
		'11652						✔	✔						
		'2952								✔	+	✔		+	
		'2952A									✔				
	OC/3S	'653	✔												
		'654	✔												
Inverting Octal Registered Transceivers	3S	'544								✔	+				
		'11544							✔						
		'648	✔	✔						✔	+				
		'11648							✔						
		'651	✔	✔						✔	✔				
		'2953								✔	+				
Noninverting 16-Bit Registered Transceivers	3S	'16470							✔		✔				
		'16543						✔	✔		✔	+		+	+
		'16646						✔	✔		✔	+		+	+
		'16652						✔	✔		✔	+		+	+
		'16952							✔		✔	+		+	+
Inverting 16-Bit Registered Transceivers	3S	'16471									+				
		'16544							✔		+				
		'16648							✔		+				
		'16651							✔		+				
		'16953									+				

✔ Product available in technology indicated
\+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Noninverting 18-Bit Registered Transceivers	3S	'16472						✔							
		'16474							✔						
		'16500									✔	+		+	+
		'16501									✔	+		+	+
		'16600									✔				+
		'16601									✔				+
Inverting 18-Bit Registered Transceivers	3S	'16475							✔						
Noninverting 36-Bit Transceivers	3S	'32245									+				
Noninverting 36-Bit Registered Transceivers	3S	'32501									✔				
		'32543									✔				
8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'657			✔					✔	+				
		'659					✔								
		'833									+				
		'834									+				
		'853									+				
		'854									+				
		'899								✔					
	3S/OC	'29833	✔							✔					
		'29834								✔					
		'29853	✔							✔					
		'29854	✔							✔					
Dual 8-/9-Bit Bus Transceivers With Parity Checkers/ Generators	3S	'16833							✔		✔				
		'16657							✔		✔				
		'16853									✔				
Universal Transceivers/Port Controllers	3S	'856		✔											
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	3S	'32316									✔				
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	3S	'32318									✔				

✔ Product available in technology indicated
\+ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

MOS Memory Drivers/Transceivers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Octal Transceivers With Series Resistors on Output	3S	'2623		✔							
Octal Buffers/Drivers With Series Resistors on Output	3S	'2240	✔							✔	✔
		'2241								✔	✔
		'2244								✔	✔
		'2541	✔								
Octal Transceivers With Series Resistors on B Port	3S	'2245								✔	+
Octal Latches With Series Resistors on Output	3S	'2574								+	
10-Bit Buffers/Drivers With Series Resistors	3S	'2827								✔	
		'2828								✔	
11-Bit Buffers/Drivers With Series Resistors	3S	'2410								✔	
		'2411								+	
		'5400									✔
		'5401									✔
12-Bit Buffers/Drivers With Series Resistors	3S	'5402									✔
		'5403									✔
16-Bit Buffers/Drivers With Series Resistors	3S	'162240									+
		'162244									✔
16-Bit Transceivers With Series Resistors	3S	'162245									+
18-Bit Universal Bus Transceivers (UBT™) With Series Resistors on B Port	3S	'162500									+
		'162501									+
		'162600									+
		'162601									✔
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	3S	'162260									✔

✔ Product available in technology indicated
+ New product planned in technology indicated

TESTABILITY BUS-INTERFACE CIRCUITS

JTAG/IEEE 1149.1 Testability Circuits

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY							
				F	HC	HCT	AC	ACT	BCT	ABT	LVT
Buffers/Drivers	8	3S	'8240A						✔		
			'8244A						✔		
Transceivers	8	3S	'8245							✔	
			'8245A						✔		
	18	3S	'18245							✔	+
Transparent Latches	8	3S	'8373A						✔		
Flip-Flops	8	3S	'8374A						✔		
Registered Transceivers	8	3S	'8543							✔	
			'8646							✔	
			'8652							✔	
			'8952							✔	
	18	3S	'18502							✔	+
			'18646							✔	
			'18652							+	
	20	3S	'18504							✔	+
Test Bus Controllers		3S	'8990					✔			
Digital Bus Monitors		3S	'8994					✔			
Scan Path Linkers	4	3S	'8997					✔			
With Identification Buses	8	3S	'8999					✔			

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Dual J-K Edge Triggered		'73				✔									
		'76				✔									
		'109	✔	✔	✔	✔									
		'11109						✔	✔						
		'112	✔		✔	✔								+	
		'11112						✔	✔						
		'113	✔			✔									
		'114	✔												
Dual D-Type		'74	✔	✔	✔	✔	✔						✔	+	
		'11074						✔	✔						
Dual D-Type With 2-Input NAND/NOR Gates		'7074				✔									
		'7075				✔									
		'7076				✔									
Dual 4-Bit D-Type Edge Triggered	3S	'874	✔	✔											
		'11874							✔						
		'876	✔	✔											
		'879	✔	✔											
Quad D-Type		'173				✔									
		'175	✔	✔	✔	✔									
		'11175						✔	✔						
Hex D-Type		'174	✔	✔	✔	✔							✔		
		'11174						✔	✔						
		'378			✔	✔									
Octal D-Type True Data	3S	'374	✔	✔	✔	✔	✔			✔	✔		+	+	
		'11374						✔	✔						
		'574	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
Octal D-Type True Data With Clear		'273	✔			✔	✔				✔	✔	+		
		'11273						✔	✔						
	3S	'575	✔	✔											
		'874	✔	✔											
Octal D-Type True Data With Clock Enable		'377			✔	✔	✔				✔				
		'11377						✔	✔						
Octal D-Type Inverting	3S	'534	✔	✔		✔				✔	✔				
		'11534						✔	✔						
		'564	✔												
		'576	✔	✔											
		'29826								✔					

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Flip-Flops (continued)

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY												
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Octal Dual-Ranked True Data	3S	'4374		✔											
Octal Inverting With Clear	3S	'577	✔												
		'879	✔	✔											
Octal Inverting With Preset	3S	'876	✔	✔											
Octal True Data	3S	'825		✔											
		'11825							✔						
		'29825								✔					
9-Bit True Data	3S	'823		✔							+			+	
		'29823	✔							✔					
9-Bit Inverting	3S	'824		✔											
		'29824	✔												
10-Bit True Data	3S	'821		✔							✔			+	
		'1821		✔											
		'11821							✔						
		'29821	✔							✔					
10-Bit Inverting	3S	'29822								✔					
16-Bit D-Type True Data With Clock Enable		'16377									+				
16-Bit Noninverting	3S	'16374						✔	✔		✔	+		+	+
16-Bit Inverting	3S	'16534									+				
18-Bit Noninverting	3S	'16823							✔		✔				+
20-Bit Noninverting	3S	'16821							✔		✔				+

✔ Product available in technology indicated
\+ New product planned in technology indicated

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FLIP-FLOPS AND LATCHES

Latches

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
Bistable	4		'75				✔									
			'375				✔									
D-Type Edge Triggered Inverting and Noninverting	8		'996	✔												
D-Type Transparent Readback Latch, True	8	3S	'990	✔												
	9	3S	'992	✔												
	10	3S	'994	✔												
D-Type Transparent With Clear, True Outputs	8	3S	'666	✔												
D-Type Transparent With Clear, Inverting Outputs	8	3S	'667	✔												
D-Type Transparent True	8	3S	'373	✔	✔	✔	✔	✔			✔	✔		+	+	
			'11373						✔	✔						
			'573	✔	✔	✔	✔	✔			✔	✔	✔	+	+	
	16	3S	'16373						✔	✔		✔	+		+	+
			'16373A									✔				
	32	3S	'32373									+				
D-Type Dual 4-Bit Transparent True	8	3S	'873	✔	✔											
			'11873						✔							
D-Type Transparent Inverting	8	3S	'533	✔	✔						✔	✔				
			'11533						✔	✔						
			'563	✔			✔									
			'580	✔	✔											
	16	3S	'16533									+				
Dual 4-Bit Transparent Inverting	8	3S	'880	✔	✔											
2-Input Multiplexed	8	3S	'604				✔									
Addressable	8	2S	'259	✔			✔									
		Q	'4724				✔									

✔ Product available in technology indicated
+ New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Latches (continued)

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY												
				ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LVT	LV	LVC	ALVC
D-Type True Inputs	8	3S	'845	✔												
			'29845	✔												
	9	3S	'843	✔	✔							+			+	
			'1843		✔											
			'29843								✔					
	10	3S	'841	✔	✔							+			+	
			'29841	✔							✔					
	18	3S	'16843									+				+
	20	3S	'16841							✔		✔				+
D-Type Inverting Inputs	8	3S	'846	✔												
			'29846								✔					
	9	3S	'29844								✔					
	10	3S	'842	✔	✔											
			'29842	✔												

✔ Product available in technology indicated
+ New product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY								
				ALS	AS	F	HC	HCT	AC	ACT	BCT	LV
Parallel In, Parallel Out, Bidirectional	4		'194		✔							
			'11194						✔	✔		
	8		'299	✔		✔						
			'323	✔								
Parallel In, Parallel Out	4		'195		✔							
Serial In, Parallel Out	8		'164	✔			✔					+
Parallel In, Serial Out	8		'165	✔			✔					
			'166	✔			✔					
Serial In, Parallel Out With Output Latches	8	3S	'594				✔					
			'595				✔					
Parallel Out	10		'11898						✔	✔		
Noninverting	8	3S	'299	✔								
	9	3S	'29823	✔								

Register Files

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Dual 16 Word × 4 Bits	3S	'870	✔								
		'871		✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

COUNTERS

Synchronous Counters – Positive Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
4-Bit Decade Up/Down	Sync	'568	✔							
4-Bit Binary	Sync	'161	✔	✔	✔	✔				
		'163	✔	✔	✔	✔				
		'561	✔							
4-Bit Binary Up/Down	Sync	'169	✔	✔	✔					
		'569	✔							
		'8169	✔							
	Async	'191	✔			✔				
		'11191						✔	✔	
		'193	✔			✔				
8-Bit Up/Down	Sync Clear	'869	✔	✔						
	Async Clear	'867	✔	✔						
		'11867							✔	
Divide-by-10 Counter	Sync	'4017				✔				

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Dual 4-Bit Binary	None	'393				✔				
12-Bit Binary	Sync	'4040				✔				
14-Bit Binary	Sync	'4020				✔				
		'4060				✔				
		'4061				✔				

8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							
			ALS	AS	F	HC	HCT	AC	ACT	BCT
Parallel Register Outputs	3S	'590				✔				
		'11590						✔	✔	
Parallel Register Inputs	3S	'11593						✔	✔	

✔ Product available in technology indicated
✚ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Quad 2-to-1		'157	✔	✔	✔	✔	✔						+
		'11157						✔	✔				
		'158	✔	✔	✔	✔							
		'11158						✔	✔				
		'298		✔									
	3S	'257	✔	✔	✔	✔	✔						+
		'11257						✔	✔				
		'258	✔	✔	✔	✔							
		'11258							✔				
Dual 4-to-1		'153	✔	✔	✔	✔							
		'11153						✔	✔				
		'352	✔										
	3S	'253	✔	✔	✔	✔							
		'11253						✔	✔				
		'353		✔									
		'11353							✔				
Hex 2-to-1 Universal Multiplexer	3S	'857	✔										
8-to-1		'151	✔	✔	✔	✔							
		'11151						✔	✔				
	3S	'251	✔		✔	✔							
		'11251						✔					
		'354				✔							
16-to-1	3S	'250		✔									
		'850		✔									
		'851		✔									
Full BCD		'147				✔							
Cascadable Octal		'148				✔							

✔ Product available in technology indicated
+ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Decoders/Demultiplexers

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY										
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT	LV	LVC
Dual 2-to-4		'239				✔							
Dual 2-to-4		'139	✔			✔	✔						+
		'11139						✔	✔				
	OC	'156	✔										
3-to-8		'138	✔	✔	✔	✔	✔					✔	+
		'11138						✔	✔				
		'238					✔						
		'11238						✔	✔				
3-to-8 With Address Registers		'131		✔									
		'137	✔			✔							+
3-to-8 With Address Latches		'237				✔							
4-to-10 BCD-to-Decimal		'42				✔							
4-to-16		'154				✔							
4-to-16 With Address Latches		'4514				✔							
		'4515				✔							
Dual 2-to-4 for Battery Backed-Up Memories		'2414								✔			

Shifters

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Shifter	3S	'350			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

DESCRIPTION								TYPE	TECHNOLOGY							
INPUT	P=Q	$\overline{P=Q}$	P>Q	$\overline{P>Q}$	P<Q	OUTPUT	ENABLE		ALS	AS	F	HC	HCT	AC	ACT	BCT
8-Bit With 20-kΩ Pullup	Yes	No	No	No	No	OC	Yes	'518	✔							
	No	Yes	No	No	No	2S	Yes	'520	✔		✔					
								'11520						✔	✔	
	No	Yes	No	No	No	OC	Yes	'522	✔							
	No	Yes	No	Yes	No	2S	No	'682				✔				
8-Bit Standard	Yes	No	No	No	No	OC	Yes	'519	✔							
	No	Yes	No	No	No	2S	Yes	'521	✔		✔					
								'11521						✔	✔	
	No	Yes	No	Yes	No	2S	No	'684				✔				
	No	Yes	No	No	No	2S	Yes	'688	✔			✔				
8-Bit Latched P	No	No	Yes	No	Yes	2S	Yes	'885		✔						
8-Bit Latched P and Q	Yes	No	Yes	No	Yes	L	Yes	'866		✔						

Address Comparators

DESCRIPTION	OUTPUT ENABLE	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16-Bit to 4-Bit	Yes	'677	✔								
12-Bit to 4-Bit	Yes	'679	✔								

Parity Generators/Checkers

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
Odd/Even Generators/Checkers	9	'280	✔	✔	✔	✔					
		'11280						✔	✔		
		'286		✔							
		'11286						✔	✔		

✔ Product available in technology indicated
+ New product planned in technology indicated

BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

Crossbar Technology (CBT)

DESCRIPTION	TYPE	TECHNOLOGY
		CBT
Dual 4-Bit With '244 Pinout	'3244	+
8-Bit With '245 Pinout	'3245	+
10-Bit Bus Exchanger	'3383	+
Dual 5-Bit	'3384	+
10-Bit With Precharged Outputs for Live Insertion	'6800	+
18-Bit Bus Exchanger	'16209	+
24-Bit Bus Exchanger	'16212	+
12-Bit 3-to-1 Bus Select	'16214	+

ARITHMETIC CIRCUITS

Parallel Binary Adders

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit		'283			✔	✔					

Accumulators, Arithmetic Logic Units, Look-Ahead Carry Generators

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY								
			ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
4-Bit Arithmetic Logic Units: Function Generator		'181		✔							
		'11181							✔		
		'881		✔							
4-Bit Arithmetic Logic Units With Ripple Carry		'382			✔						

✔ Product available in technology indicated
+ New product planned in technology indicated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FIFO MEMORIES

First-In, First-Out Memories (FIFOs)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
16 Words × 4 Bits	U	3S	'232B			✔								
16 Words × 5 Bits	U	3S	'225		✔									
			'229B			✔								
			'233B			✔								
32 Words × 9 Bits	B	3S	'2238			✔								
64 Words × 4 Bits	U	3S	'234			✔								
			'236			✔								
64 Words × 5 Bits	U	3S	'235			✔								
64 Words × 8 Bits	U	3S	'2232A			✔								
64 Words × 9 Bits	U	3S	'2233A			✔								
64 Words × 18 Bits	U, C	3S	'7813									✔		
	U	3S	'7814									✔		
64 Words × 36 Bits	B, C	3S	'3612											+
			'3614											+
	U, C	3S	'3611											+
			'3613											+
Dual 64 × 1	C	3S	'2226									✔		
			'2227									✔		
Dual 256 × 1	C	3S	'2228									✔		
			'2229									✔		
256 Words × 9 Bits	U	3S	'7200									✔		
256 Words × 18 Bits	U, C	3S	'7805									✔		
	U	3S	'7806									✔		
256 × 36 × 2 Bits	B, C	3S	'3622									+		
512 Words × 9 Bits	U	3S	'7201									✔		
	U, S	3S	'72211									✔		
512 Words × 18 Bits	U, C	3S	'7803									✔		
	U	3S	'7804									✔		
	B, C	3S	'7819											✔
	B	3S	'7820											✔
512 Words × 32 Bits	B, C	3S	'3638									+		
512 Words × 36 Bits	U, C	3S	'3631									+		
	B, C	3S	'3632									✔		

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

FIFO MEMORIES

First-In, First-Out Memories (FIFOs) (continued)

DESCRIPTION		OUTPUT	TYPE	TECHNOLOGY										
SIZE	TYPE†			LS	S	ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
1K Words × 9 Bits	B	3S	'2235									✔		
			'2236									✔		
	U	3S	'7202									✔		
	U, S	3S	'72221									✔		
1K Words × 18 Bits	U, C	3S	'7801									✔		
			'7811									✔		
			'7881									+		
	U	3S	'7802									✔		
1K Words × 36 Bits	U, C	3S	'3641									+		
1K × 36 × 2 Bits	B, C	3S	'3642									+		
2K Words × 9 Bits	U, C	3S	'7807									✔		
	U	3S	'7203									+		
			'7808									✔		
	U, S	3S	'72231									✔		
2K Words × 18 Bits	U, C	3S	'7882									+		
2K Words × 36 Bits	U, C	3S	'3651									+		
4K Words × 9 Bits	U	3S	'7204									✔		
	U, S	3S	'72241									✔		
4K Words × 18 Bits	U, C	3S	'7884									+		

† U = Unidirectional
B = Bidirectional
C = Clocked
S = Synchronized
✔ Product available in technology indicated
+ New product planned in technology indicated

CLOCK DISTRIBUTION CIRCUITS

Clock Distribution Circuits (CDC)

DESCRIPTION	TYPE	TECHNOLOGY								
		ALS	AS	F	HC	HCT	AC	ACT	BCT	ABT
3.3-V Hex Inverting Clock Drivers/Buffers	'203						✔			
Hex Inverting Clock Drivers/Buffers	'204						✔			
Dual 1-to-4 Clock Drivers/Buffers	'208							✔		
	'209						✔			
Octal Divide-by-2 Clock Drivers (6 Inverting, 2 Noninverting)	'303		✔							
Octal Divide-by-2 Clock Drivers (8 Noninverting)	'305		✔							
Octal Divide-by-2 Clock Drivers (4 Inverting, 4 Noninverting)	'304		✔							
1-to-6 Clock Drivers	'328									✔
	'328A									✔
	'329									✔
	'329A									✔
1-to-6 Clock Drivers With Output Enable	'391									✔
	'392									✔
1-to-8 Clock Drivers	'340									✔
	'341									✔
1-to-8, Divide-by-2 Clock Drivers	'337									✔
	'339									✔
Phase-Lock Loop 1-to-12 Clock Drivers	'582									+
	'586									+
	'2586									+

✔ Product available in technology indicated
+ New product planned in technology indicated

ECL TRANSLATORS

ECL-to-TTL or TTL-to-ECL Translators

DESCRIPTION	LEVEL TRANSLATION	OUTPUT	TYPE
Octal Bus Driver, Inverting	ECL-to-TTL	3S	10KHT5540
	TTL-to-ECL	OE	10KHT5542
Octal Bus Driver, Noninverting	ECL-to-TTL	3S	10KHT5541
	TTL-to-ECL	OE	10KHT5543
			100KT5543
Octal D-Type Latch, True	ECL-to-TTL	3S	10KHT5573
			100KT5573
Octal D-Type Flip-Flop, True	ECL-to-TTL	3S	10KHT5574
	TTL-to-ECL	OE	10KHT5578
			100KT5578

ADVANCED CMOS LOGIC

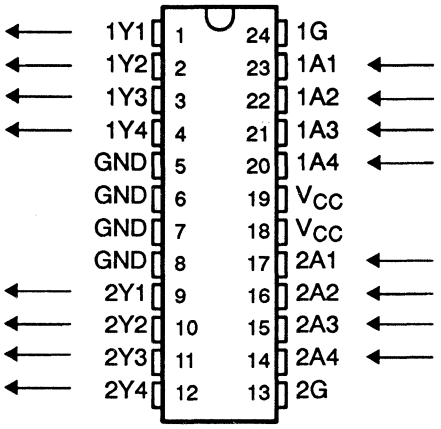
Features

- Advanced Bipolar Speed Performance
- Low CMOS Power Consumption
- 24-mA Output Drive Capability
- AC/ACT Versions
- Flow-Through/Center-Pin Architecture
- Output Edge Control (OEC™)
- DIP, SOIC, and SSOP Packages

Benefits

- Reduced Output Glitching
- No Loss of Stored Data
- No Speed Degradation of System Performance
- Reduced Power Supply Requirements
- Improves System Throughout Without Bipolar Penalty
- Center Pin V_{CC}/GND Provides Minimal Package Inductance
- Flow-Through Architecture Provides Design and Manufacturing Simplification of PCB

Pinout Benefits

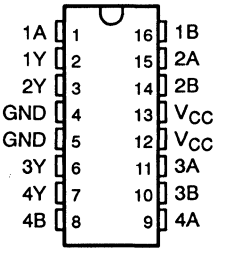


AC11240

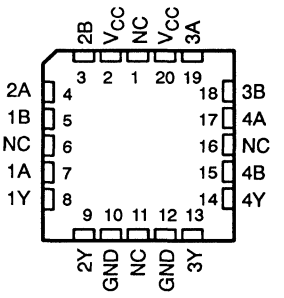
D2957, APRIL 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11000 . . . J PACKAGE
74AC11000 . . . D OR N PACKAGE
(TOP VIEW)



54AC11000 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54AC11000 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11000 is characterized for operation from −40°C to 85°C.

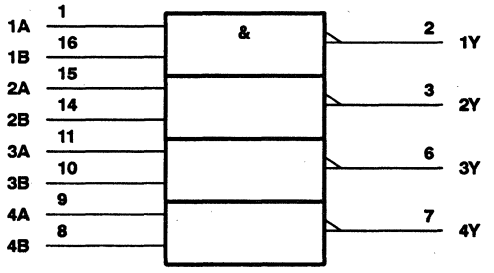
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

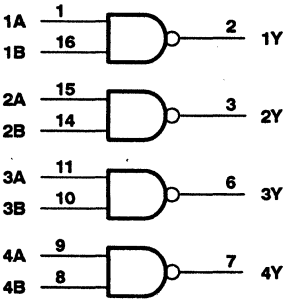
EPIC is a trademark of Texas Instruments Incorporated.

D2957, APRIL 1987 - REVISED APRIL 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11000			74AC11000			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11000		74AC11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11000		74AC11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7.2	9.8	1.5	11.9	1.5	11.1	ns
t_{PHL}			1.5	5.8	8.6	1.5	10.2	1.5	9.6	

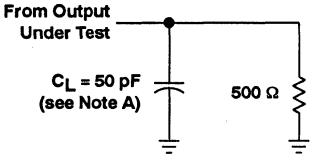
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11000		74AC11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5	6.5	1.5	8.1	1.5	7.4	ns
t_{PHL}			1.5	4.4	6.1	1.5	7.3	1.5	6.8	

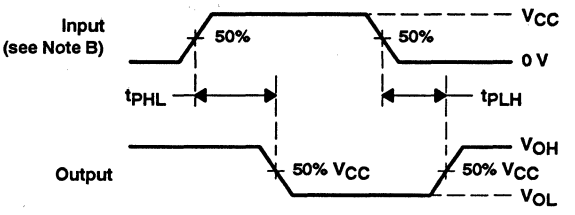
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	33	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

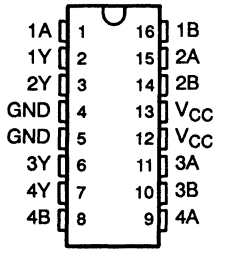
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

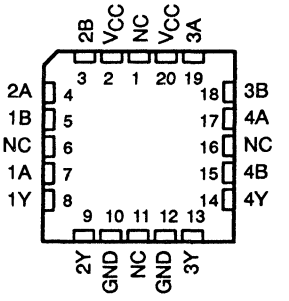
SCAS002A – D2957, JUNE 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11000 . . . J PACKAGE
74ACT11000 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11000 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

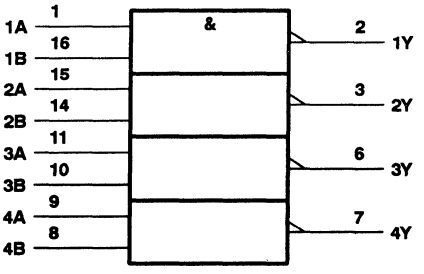
These devices contain four independent 2-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54ACT11000 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11000 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each gate)

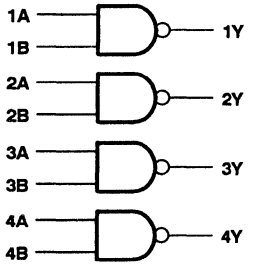
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11000		74ACT11000		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

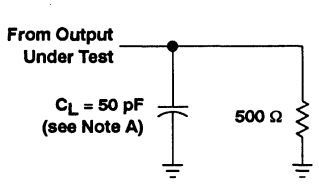
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11000		74ACT11000		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7.2	10.9	1.5	13.3	1.5	12.3	ns
t_{PHL}			1.5	5.8	8	1.5	9.5	1.5	8.8	

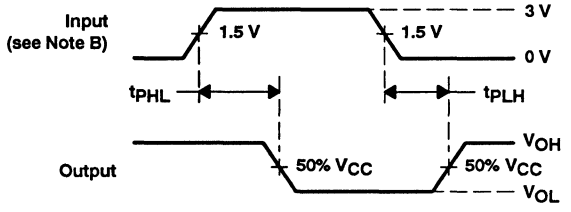
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

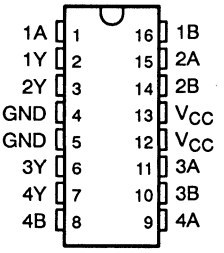
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

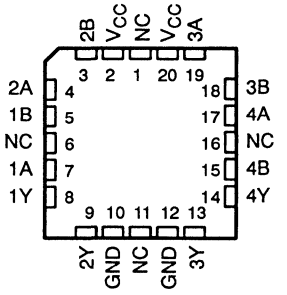
D2957, JUNE 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11002 . . . J PACKAGE
74AC11002 . . . D OR N PACKAGE
(TOP VIEW)



54AC11002 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

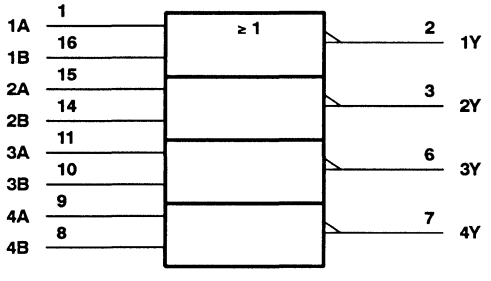
These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54AC11002 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11002 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

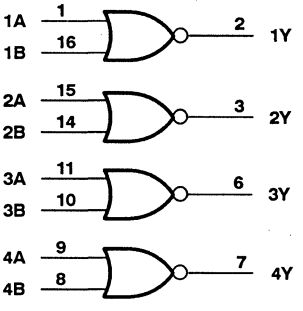
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11002			74AC11002			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11002		74AC11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11002		74AC11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7	8.6	1.5	10.7	1.5	9.9	ns
t_{PHL}			1.5	6	7.5	1.5	9	1.5	8.4	

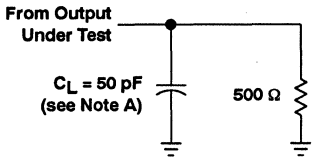
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11002		74AC11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	4.5	6.1	1.5	7.4	1.5	6.9	ns
t_{PHL}			1.5	4	5.7	1.5	6.8	1.5	6.4	

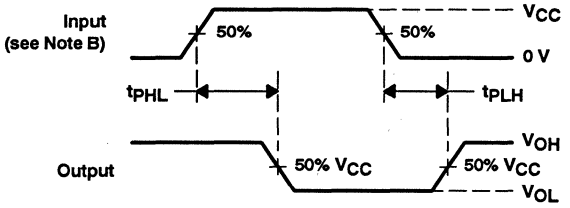
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



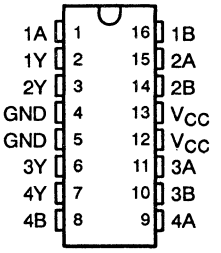
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

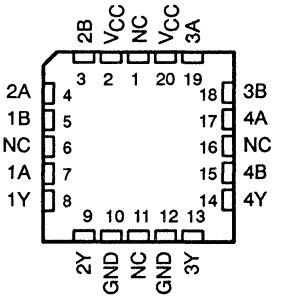
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11002 . . . J PACKAGE
74ACT11002 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11002 . . . FK PACKAGE
(TOP VIEW)



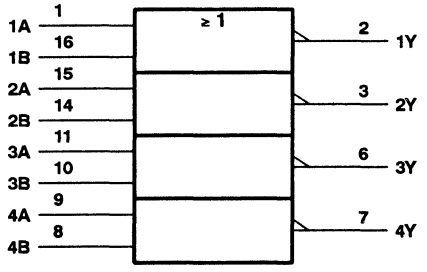
NC – No internal connection

description

These devices contain four independent 2-input NOR gates. They perform the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A + B}$ in positive logic.

The 54ACT11002 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11002 is characterized for operation from − 40°C to 85°C.

logic symbol†

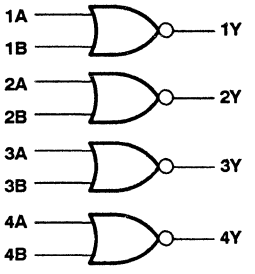


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11002		74ACT11002		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA‡	5.5 V				3.85				
	I_{OH} = – 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

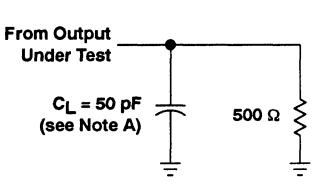
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11002		74ACT11002		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.1	9.4	1.5	11.3	1.5	10.6	ns
t_{PHL}			1.5	5.3	7.8	1.5	9.5	1.5	8.7	

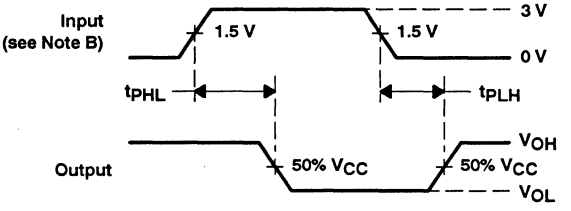
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

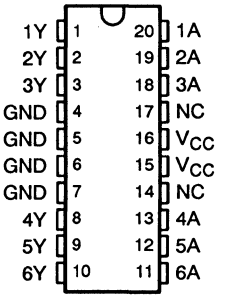
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

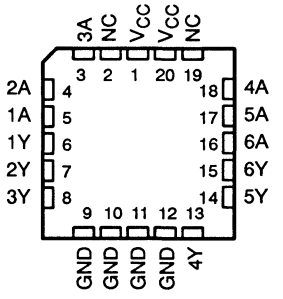
D2957, JANUARY 1988 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11004 . . . J PACKAGE
74AC11004 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11004 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

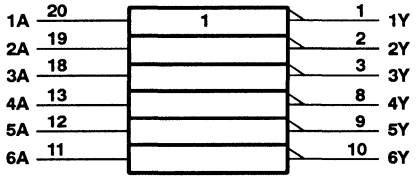
These devices contain six independent inverters. They perform the Boolean functions $Y = \overline{A}$.

The 54AC11004 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11004 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

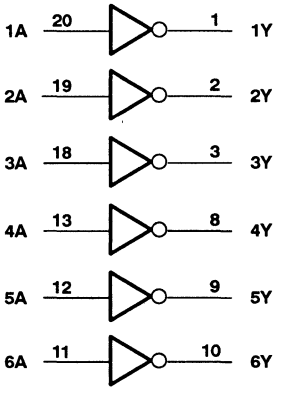
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11004			74AC11004			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11004		74AC11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11004		74AC11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6.1	9	1.5	10.4	1.5	10	ns
t_{PHL}			1.5	5.2	7.4	1.5	8.9	1.5	8.2	

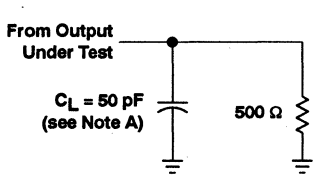
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11004		74AC11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4.2	6.3	1.5	7.5	1.5	7.1	ns
t_{PHL}			1.5	3.8	5.5	1.5	6.4	1.5	6	

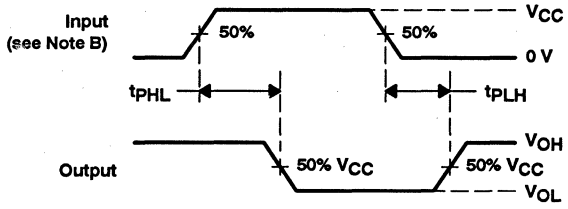
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

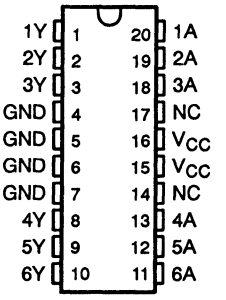
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

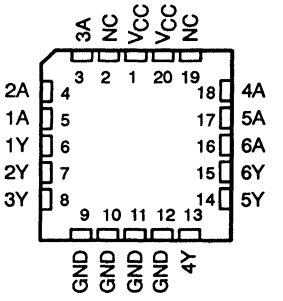
SCAS215 – D2957, JANUARY 1988 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11004 . . . J PACKAGE
74ACT11004 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11004 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

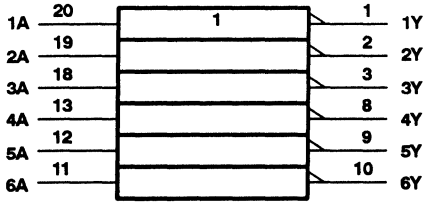
These devices contain six independent inverters. They perform the Boolean functions $Y = \overline{A}$.

The 54ACT11004 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11004 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each inverter)

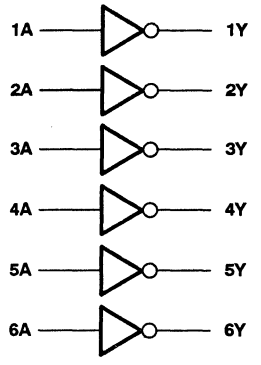
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11004		74ACT11004		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11004		74ACT11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ns.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

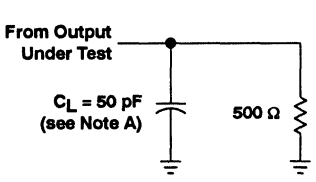
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11004		74ACT11004		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5.3	9	1.5	10.2	1.5	9.7	ns
t_{PHL}			1.5	6.4	8.7	1.5	10.3	1.5	9.6	

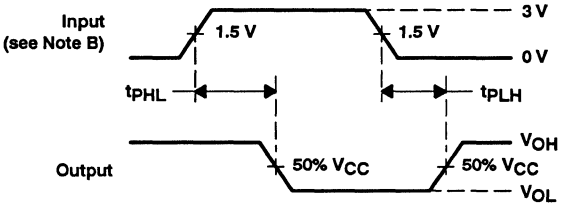
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	C_L = 50 pF, f = 1 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

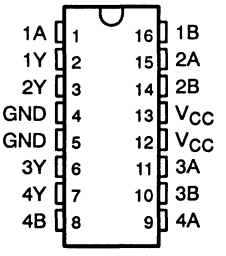
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

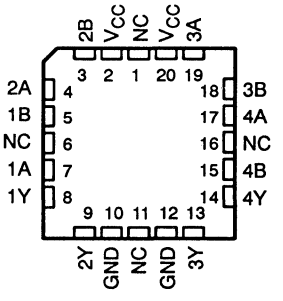
D2957, AUGUST 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11008 . . . J PACKAGE
74AC11008 . . . D OR N PACKAGE
(TOP VIEW)



54AC11008 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

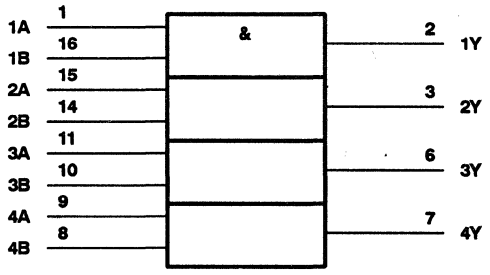
The 54AC11008 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11008 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

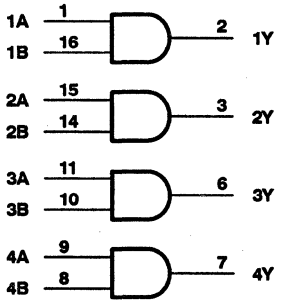
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11008			74AC11008			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11008		74AC11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11008		74AC11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.3	9	1.5	11	1.5	10.2	ns
t_{PHL}			1.5	5.6	7.8	1.5	9	1.5	8.6	

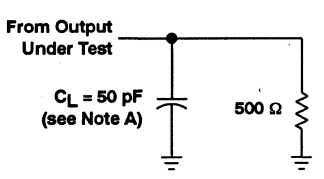
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11008		74AC11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	4.3	6.2	1.5	7.3	1.5	6.9	ns
t_{PHL}			1.5	5.6	5.9	1.5	6.8	1.5	6.5	

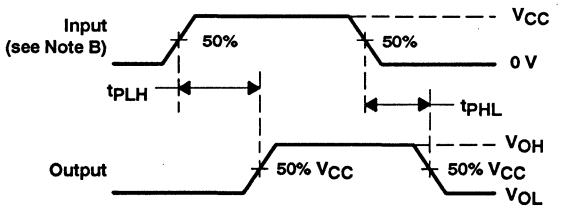
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



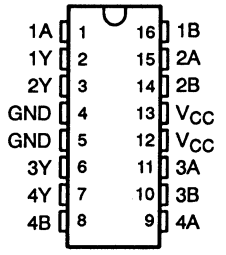
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

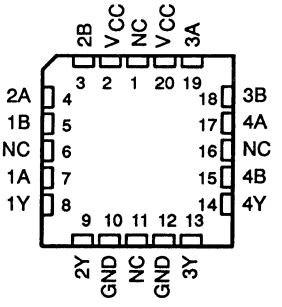
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11008 . . . J PACKAGE
74ACT11008 . . . D, N, OR PW PACKAGE
(TOP VIEW)



54ACT11008 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

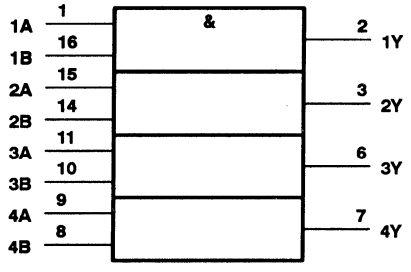
These devices contain four independent 2-input AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 54ACT11008 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11008 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

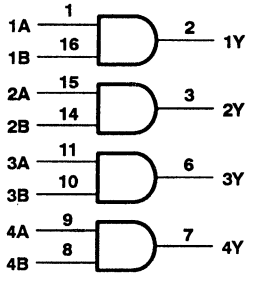
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11008		74ACT11008		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4		4.4		4.4			V
		5.5 V	5.4		5.4		5.4			
	I_{OH} = −24 mA	4.5 V	3.94		3.7		3.8			
		5.5 V	4.94		4.7		4.8			
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
I_{OH}‡	V_O = 3.85 V	5.5 V				−50		−75		mA
I_{OL}‡	V_O = 1.65 V	5.5 V				50		75		mA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1			μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 1 second.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

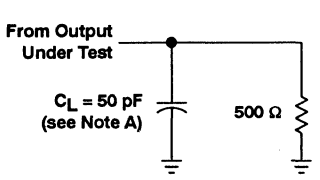
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11008		74ACT11008		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	5.8	8	1.5	9.4	1.5	9	ns
t_{PHL}			1.5	5.2	7.7	1.5	8.6	1.5	8.2	

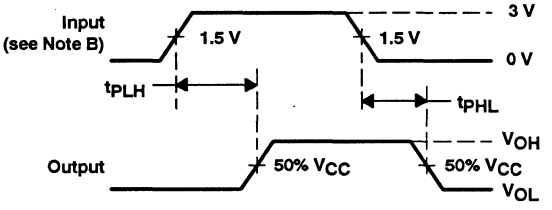
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

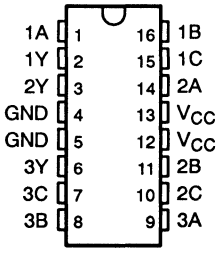
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

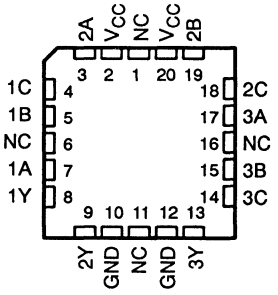
D2957, MAY 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11010 . . . J PACKAGE
74AC11010 . . . D OR N PACKAGE
(TOP VIEW)



54AC11010 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The 54AC11010 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11010 is characterized for operation from −40°C to 85°C.

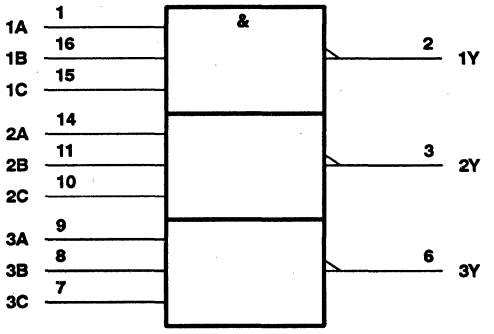
FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

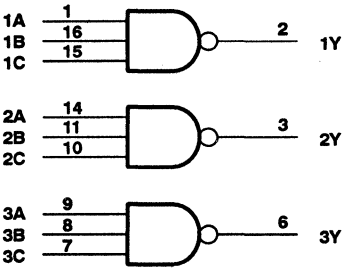
EPIC is a trademark of Texas Instruments Incorporated.

D2957, MAY 1987 – REVISED APRIL 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11010			74AC11010			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11010		74AC11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11010		74AC11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.9	8.5	1.5	10	1.5	9.3	ns
t_{PHL}			1.5	5.8	9	1.5	10.4	1.5	9.9	

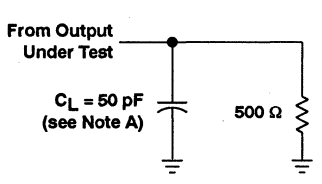
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11010		74AC11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4.4	6.2	1.5	7.1	1.5	6.7	ns
t_{PHL}			1.5	4.6	6.4	1.5	7.4	1.5	7	

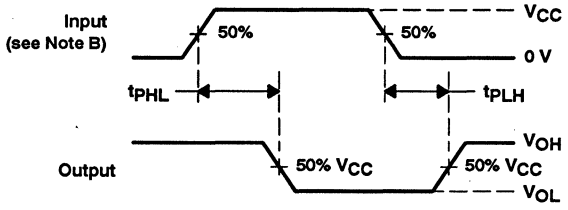
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

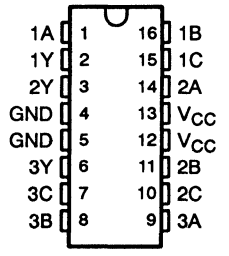
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

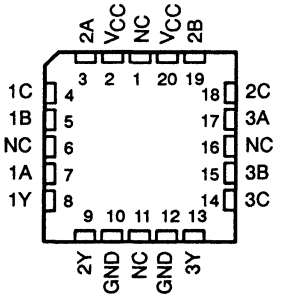
SCAS018A – D2957, JULY 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11010 . . . J PACKAGE
74ACT11010 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11010 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

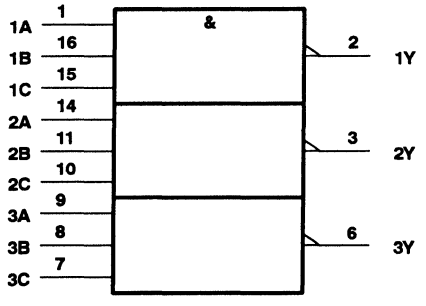
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The 54ACT11010 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11010 is characterized for operation from − 40°C to 85°C.

FUNCTION TABLE
(each gate)

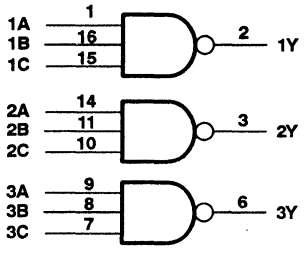
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11010		74ACT11010		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA‡	5.5 V				3.85				
	I_{OH} = – 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

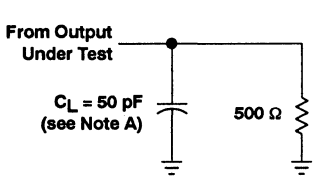
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11010		74ACT11010		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.8	8.2	1.5	9.3	1.5	8.9	ns
t_{PHL}			1.5	5.7	7.4	1.5	8.7	1.5	8.2	

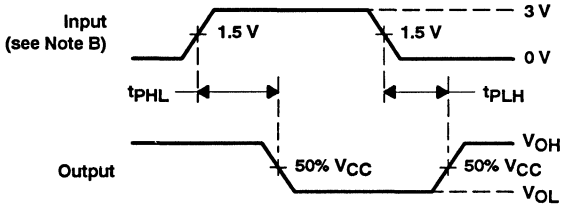
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

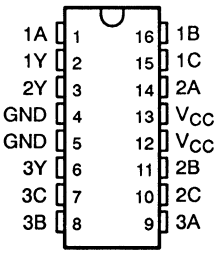
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

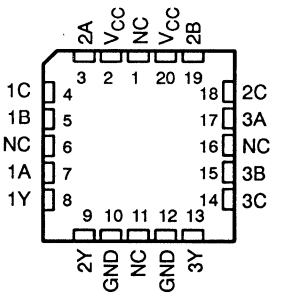
D2957, JULY 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11011 . . . J PACKAGE
74AC11011 . . . D OR N PACKAGE
(TOP VIEW)



54AC11011 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

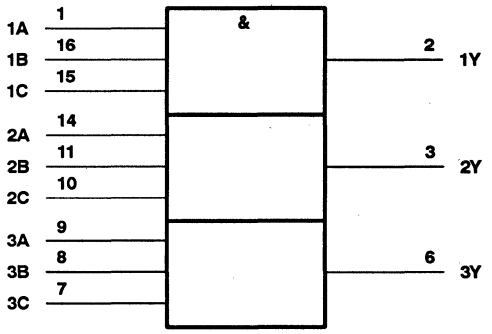
The 54AC11011 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11011 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

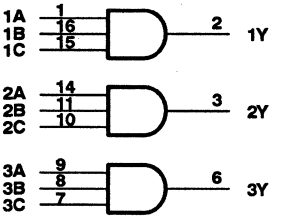
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11011			74AC11011			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11011		74AC11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11011		74AC11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
t_{PHL}			1.5	6	8.2	1.5	9.6	1.5	9	

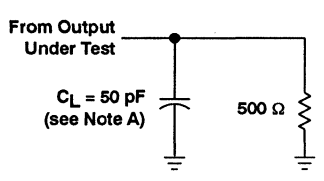
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11011		74AC11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4	5.9	1.5	6.9	1.5	6.5	ns
t_{PHL}			1.5	4.5	6.4	1.5	7.3	1.5	6.9	

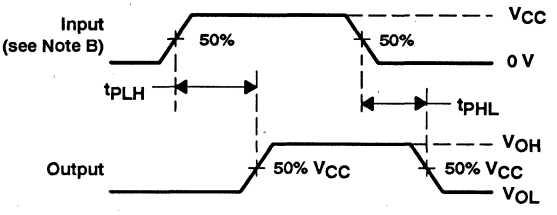
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS028A – D2957, JULY 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

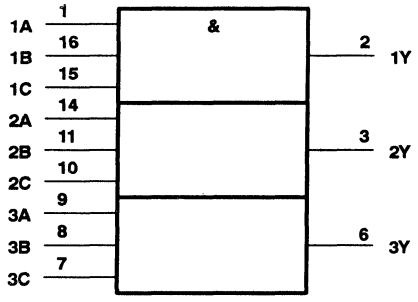
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The 54ACT11011 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11011 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each gate)

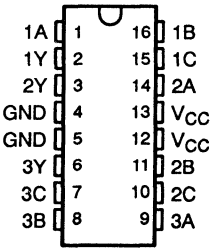
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol†

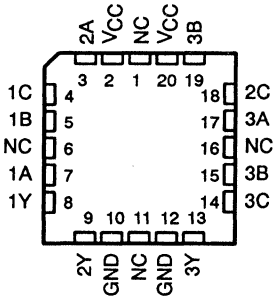


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

54ACT11011 . . . J PACKAGE
74ACT11011 . . . D OR N PACKAGE
(TOP VIEW)

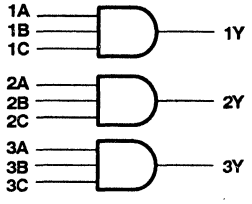


54ACT11011 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11011		74ACT11011		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

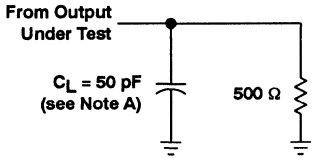
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11011		74ACT11011		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	1.5	6.5	8.6	1.5	10.2	1.5	9.6	ns
t_{PHL}			1.5	5.5	7.9	1.5	9.2	1.5	8.7	

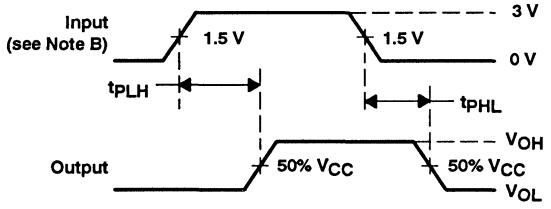
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	28	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

AUGUST 1989 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

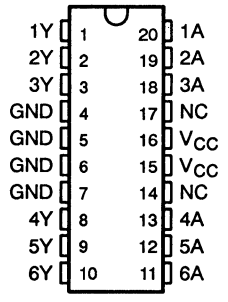
description

These Schmit-tigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$. Because of the Schmitt action they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

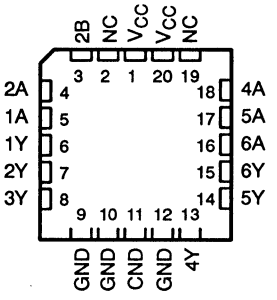
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals and also have greater noise margin than conventional inverters.

The 54AC11014 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11014 is characterized for operation from −40°C to 85°C.

54AC11014 . . . J PACKAGE
74AC11014 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11014 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

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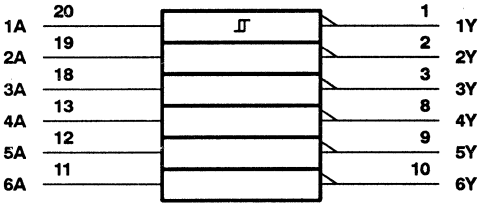
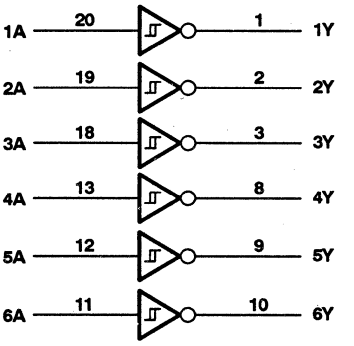
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11014			74AC11014			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		VCC = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 3 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	0		100	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11014		74AC11014		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}		3 V			2.2		2.2		2.2	V
		4.5 V			3.2		3.2		3.2	
		5.5 V			3.9		3.9		3.9	
V_{T-}		3 V	0.5			0.5		0.5		V
		4.5 V	0.9			0.9		0.9		
		5.5 V	1.1			1.1		1.1		
ΔV_T ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11014		74AC11014		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	5.4	9.2	1.2	10.3	1.2	9.8	ns
t_{PHL}			1.7	6	8.5	1.7	9.9	1.7	9.3	

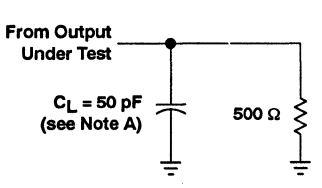
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11014		74AC11014		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3.6	6.8	1.1	7.6	1.1	7.1	ns
t_{PHL}			1.5	4.1	6.7	1.5	7.6	1.5	7.4	

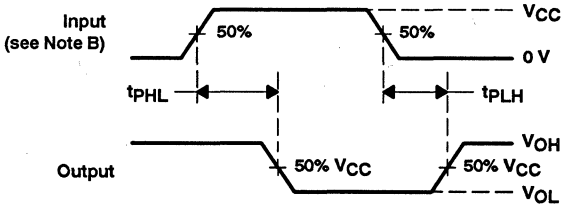
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



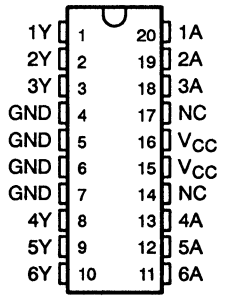
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11014 is a Schmitt-trigger device that contains six independent inverters. It performs the Boolean function $Y = \overline{A}$. Because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

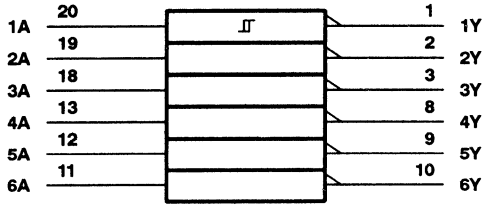
The 74ACT11014 is temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It also has a greater noise margin than conventional inverters.

The 74ACT11014 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

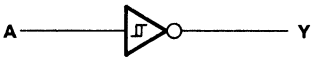
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+}		4.5 V			2		2	V
		5.5 V			2		2	
V_{T-}		4.5 V			0.8		0.8	V
		5.5 V			0.8		0.8	
ΔV_T		4.5 V	0.4		1.2	0.4	1.2	V
		5.5 V	0.4		1.2	0.4	1.2	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

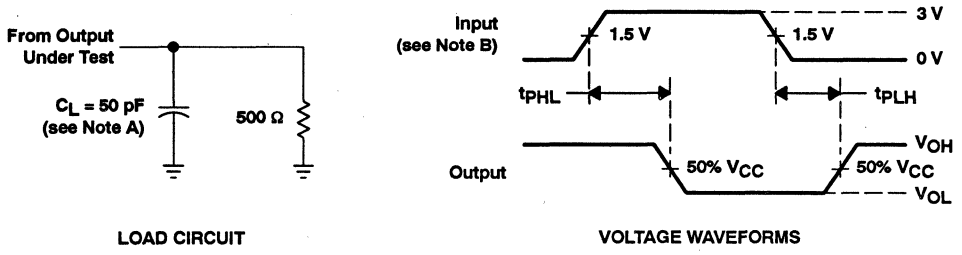
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	2.3	5.6	8.4	2.3	9.2	ns
t_{PHL}			3.3	6.4	8.3	3.3	9.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	30	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D2957, MARCH 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
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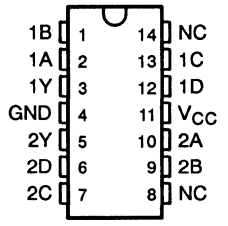
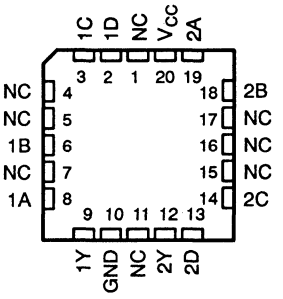
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11020 . . . J PACKAGE
74AC11020 . . . D OR N PACKAGE
(TOP VIEW)



54AC11020 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The 54AC11020 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11020 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

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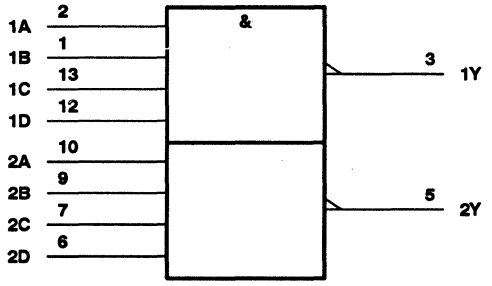
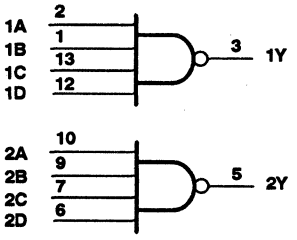
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11020			74AC11020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.4	8.6	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	6.4	9.2	1.5	10.7	1.5	10.1	

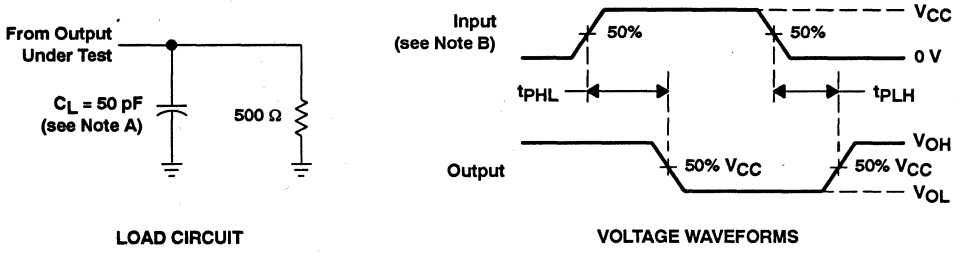
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11020		74AC11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4.3	8.1	1.5	7	1.5	6.7	ns
t_{PHL}			1.5	4.4	7.8	1.5	7.7	1.5	7.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	19	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

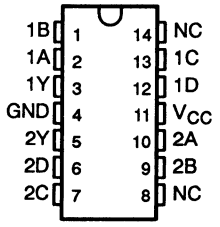
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

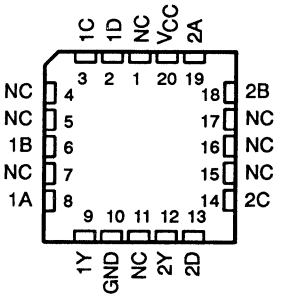
SCAS016A – D2957, JUNE 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11020 . . . J PACKAGE
74ACT11020 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11020 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

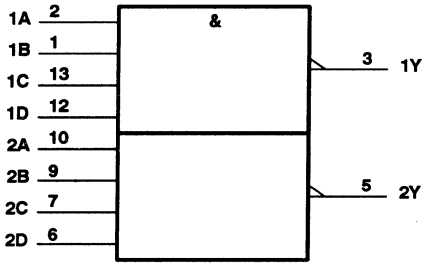
These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The 54ACT11020 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11020 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each gate)

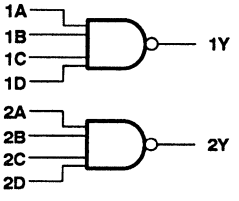
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11020		74ACT11020		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA‡	5.5 V				3.85				
	I_{OH} = – 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

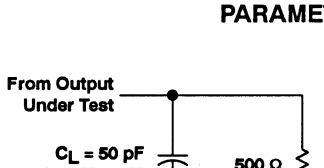
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11020		74ACT11020		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.6	8.5	1.5	9.5	1.5	9.1	ns
t_{PHL}			1.5	6.1	8.4	1.5	9.8	1.5	9.2	

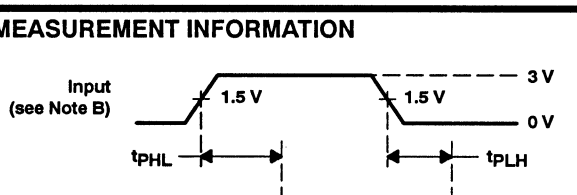
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

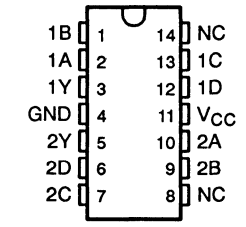
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

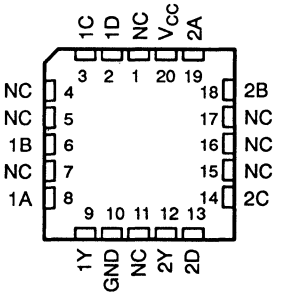
D2957, JULY 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11021 . . . J PACKAGE
74AC11021 . . . D OR N PACKAGE
(TOP VIEW)



54AC11021 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

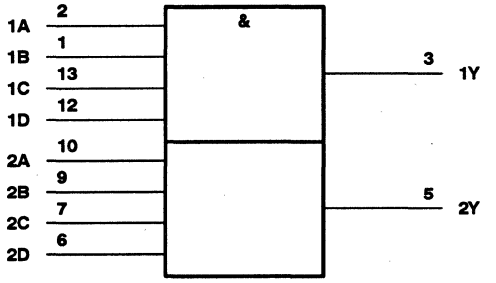
The 54AC11021 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11021 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

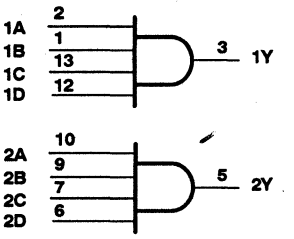
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11021			74AC11021			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11021		74AC11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11021		74AC11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	8.2	11.4	1.5	13.9	1.5	13	ns
t_{PHL}			1.5	6.4	8.7	1.5	9.9	1.5	9.3	

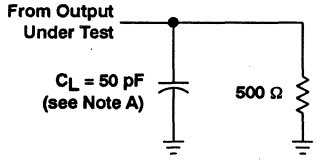
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11021		74AC11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5.6	7.8	1.5	9.4	1.5	8.8	ns
t_{PHL}			1.5	4.6	6.5	1.5	7.4	1.5	6.9	

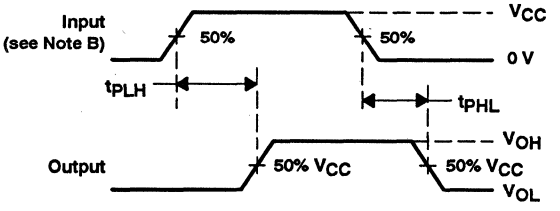
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	38	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS012B – D2957, JULY 1978 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

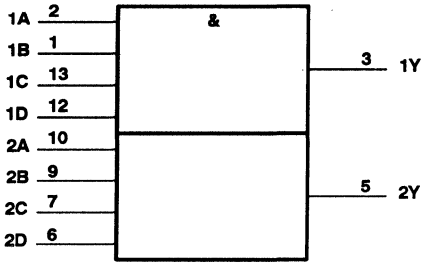
These devices contain two independent 4-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$ in positive logic.

The 54ACT11021 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11021 is characterized for operation from − 40°C to 85°C.

FUNCTION TABLE
(each gate)

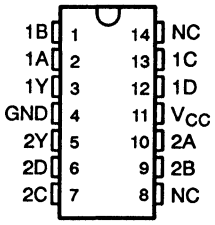
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†

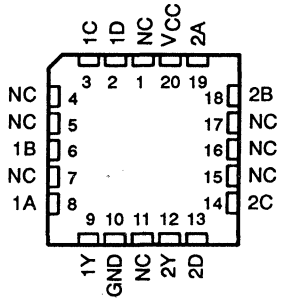


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

54ACT11021 . . . J PACKAGE
74ACT11021 . . . D OR N PACKAGE
(TOP VIEW)

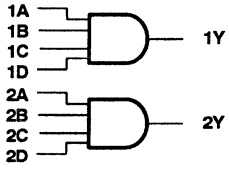


54ACT11021 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11021		74ACT11021		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA‡	5.5 V				3.85				
	I_{OH} = – 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

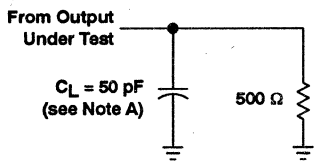
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11021		74ACT11021		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.7	8.8	1.5	10.4	1.5	9.8	ns
t_{PHL}			1.5	5.4	8.3	1.5	9.5	1.5	8.9	

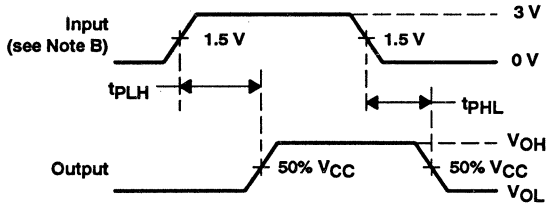
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	37	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

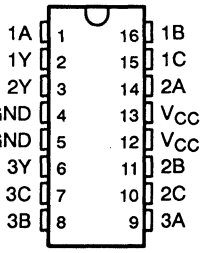
Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

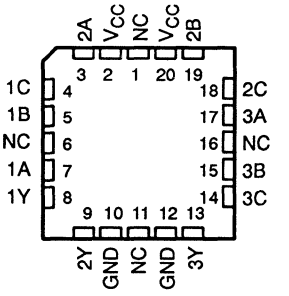
D2957, JULY 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11027 . . . J PACKAGE
74AC11027 . . . D OR N PACKAGE
(TOP VIEW)



54AC11027 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

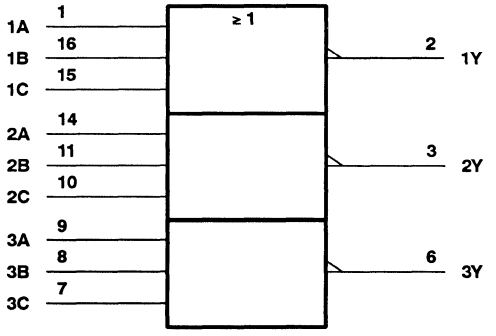
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The 54AC11027 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11027 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

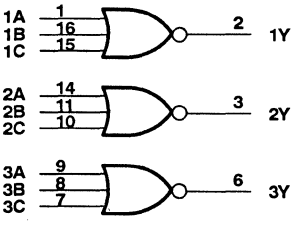
INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11027			74AC11027			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11027		74AC11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11027		74AC11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.3	9.8	1.5	11.7	1.5	10.9	ns
t_{PHL}			1.5	7.6	10.9	1.5	12.9	1.5	12	

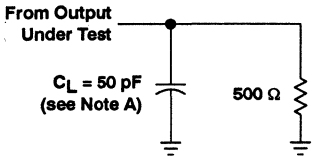
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11027		74AC11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4.3	6.8	1.5	8.1	1.5	7.7	ns
t_{PHL}			1.5	4.5	7.5	1.5	8.9	1.5	8.1	

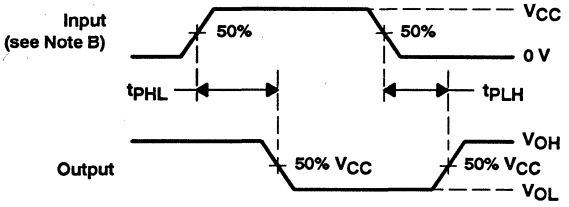
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	CL = 50 pF, f = MHz	24	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

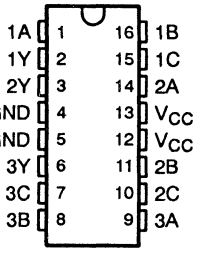
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

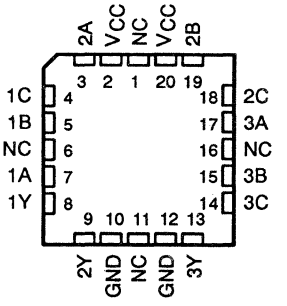
SCAS020A – D2957, JULY 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11027 . . . J PACKAGE
74ACT11027 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11027 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

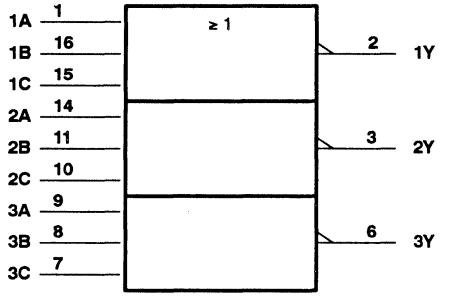
These devices contain three independent 3-input NOR gates. They perform the Boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A \cdot B \cdot C}$ in positive logic.

The 54ACT11027 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11027 is characterized for operation from − 40°C to 85°C.

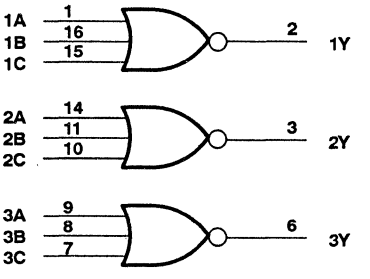
FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11027		74ACT11027		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = − 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = − 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = − 50 mA‡	5.5 V				3.85				
	I_{OH} = − 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

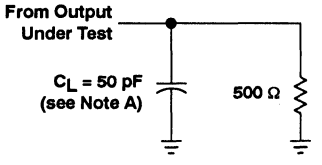
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11027		74ACT11027		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	5	9.2	1.5	10.6	1.5	10.1	ns
t_{PHL}			1.5	6	8.6	1.5	10	1.5	9.4	

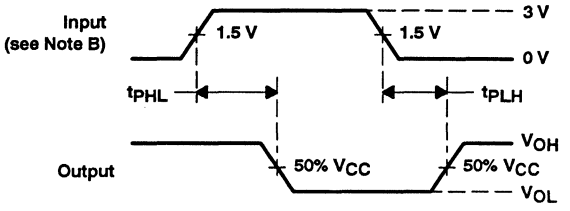
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

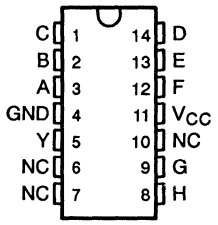
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

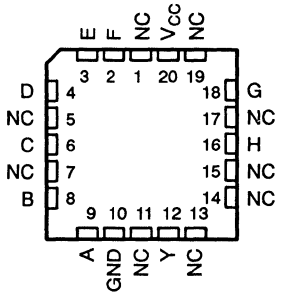
D2957, JUNE 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11030 . . . J PACKAGE
74AC11030 . . . D OR N PACKAGE
(TOP VIEW)



54AC11030 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

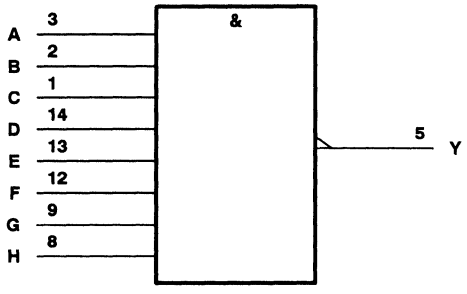
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ or}$$
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The 54AC11030 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11030 is characterized for operation from −40°C to 85°C.

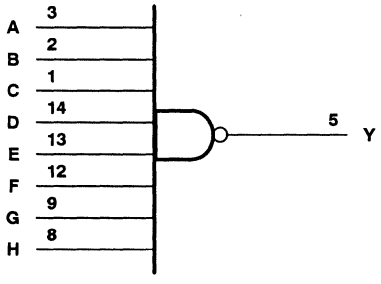
FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11030			74AC11030			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11030		74AC11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11030		74AC11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.9	9.1	1.5	10.6	1.5	9.9	ns
t_{PHL}			1.5	6.4	8.8	1.5	10.6	1.5	9.8	

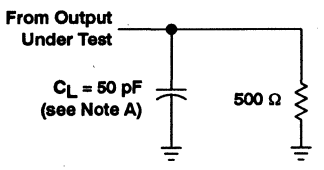
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11030		74AC11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	4.8	6.7	1.5	7.7	1.5	7.2	ns
t_{PHL}			1.5	4.8	6.7	1.5	8	1.5	7.4	

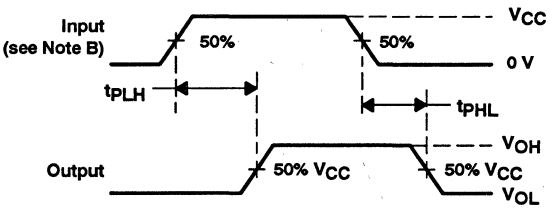
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

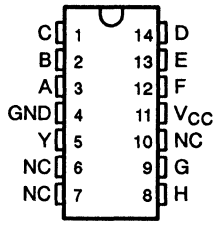
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

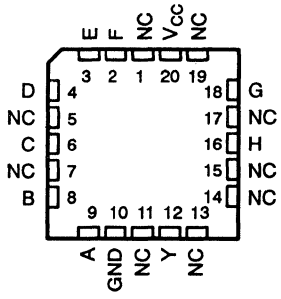
D2957, MARCH 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11030 . . . J PACKAGE
74ACT11030 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11030 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

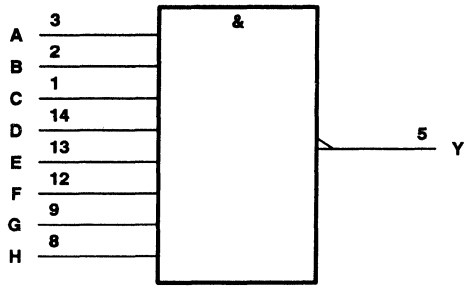
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ or}$$
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The 54ACT11030 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11030 is characterized for operation from −40°C to 85°C.

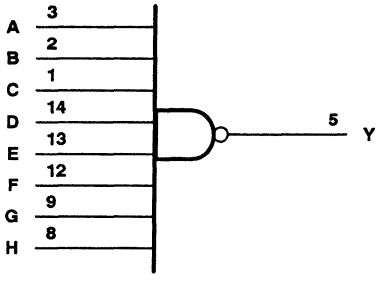
FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		54ACT11030		74ACT11030		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

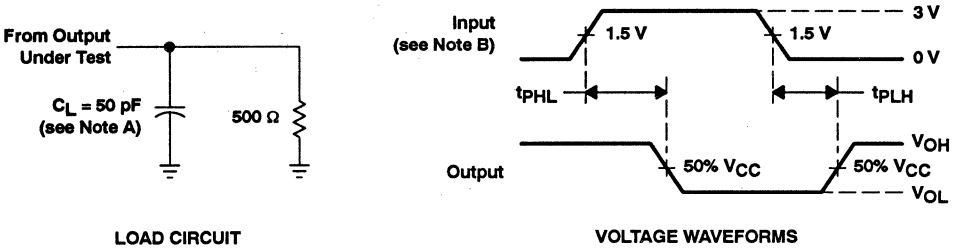
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11030		74ACT11030		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A thru H	Y	1.5	5.4	8.1	1.5	8.8	1.5	8.5	ns
t_{PHL}			1.5	5.9	7.8	1.5	9.3	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	41	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

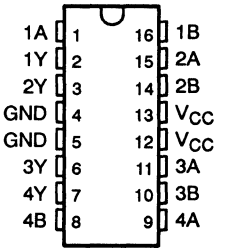
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

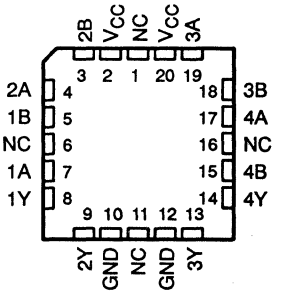
D2957, JULY 1987 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11032 . . . J PACKAGE
74AC11032 . . . D, DB OR N PACKAGE
(TOP VIEW)



54AC11032 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

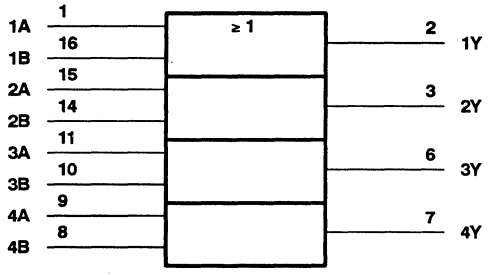
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The 54AC11032 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11032 is characterized for operation from −40°C to 85°C.

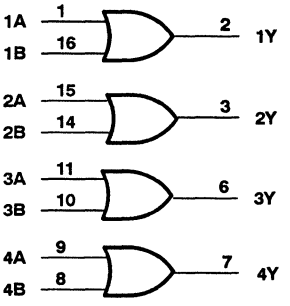
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11032			74AC11032			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11032		74AC11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = –50 mA†	5.5 V				3.85				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11032		74AC11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.3	8.7	1.5	10.7	1.5	9.7	ns
t_{PHL}			1.5	5.4	7.4	1.5	8.5	1.5	8	

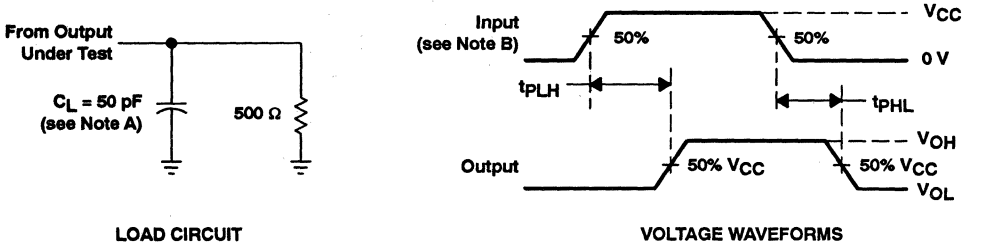
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11032		74AC11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	4.3	6.2	1.5	7.3	1.5	6.7	ns
t_{PHL}			1.5	3.8	5.5	1.5	6.3	1.5	5.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	24	pF

PARAMETER MEASUREMENT INFORMATION



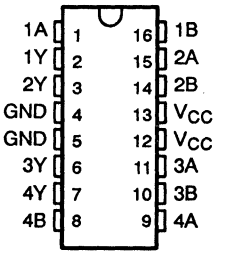
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

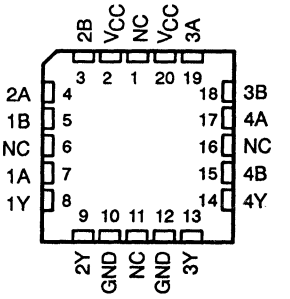
SCAS008B – D2957, JULY 1987 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11032 . . . J PACKAGE
74ACT11032 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



54ACT11032 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

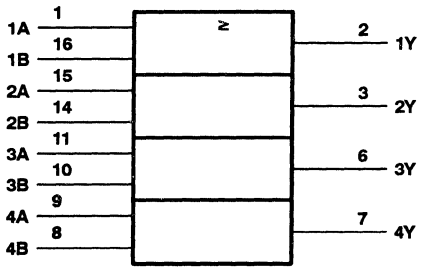
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The 54ACT11032 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11032 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

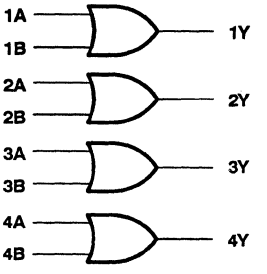
INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11032		74ACT11032		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

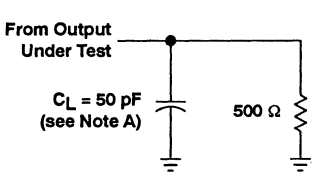
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11032		74ACT11032		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.2	8.1	1.5	9.6	1.5	9	ns
t_{PHL}			1.5	4.9	7.4	1.5	8.4	1.5	8	

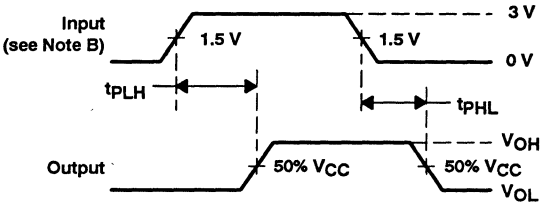
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

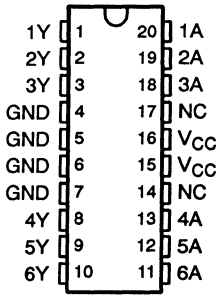
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

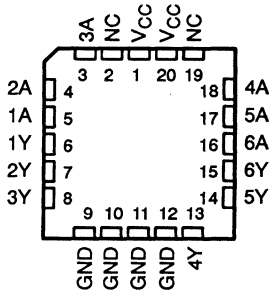
D2957, FEBRUARY 1988 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11034 . . . J PACKAGE
74AC11034 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11034 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

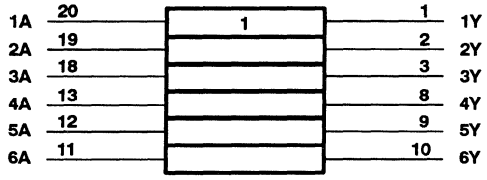
These devices contain six independent noninverters. They perform the Boolean function Y = A.

The 54AC11034 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11034 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each inverter)

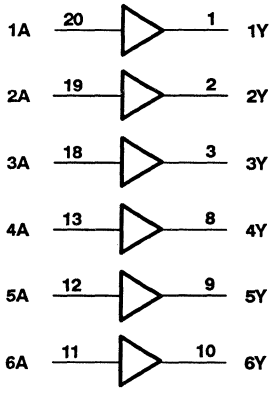
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11034			74AC11034			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11034		74AC11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = –50 mA†	5.5 V				3.85				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11034		74AC11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5.7	9.1	1.5	10.7	1.5	10.1	ns
t_{PHL}			1.5	5.5	8.3	1.5	9.9	1.5	9.2	

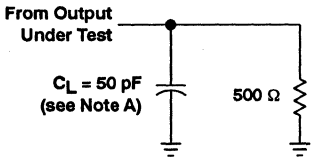
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11034		74AC11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4	6.3	1.5	7.4	1.5	6.9	ns
t_{PHL}			1.5	4	6.2	1.5	7.3	1.5	6.8	

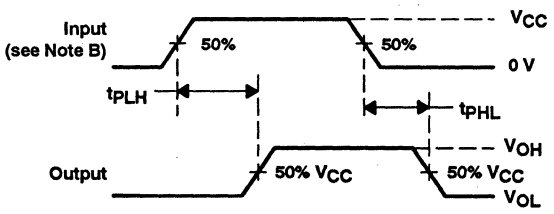
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

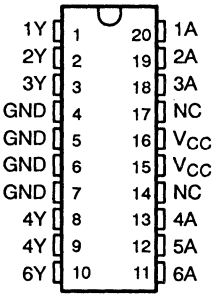
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

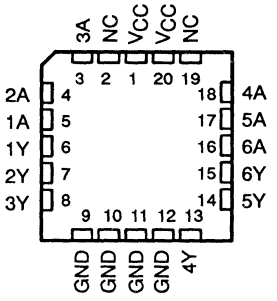
SCAS035A – D2957, FEBRUARY 1988 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11034 . . . J PACKAGE
74ACT11034 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11034 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

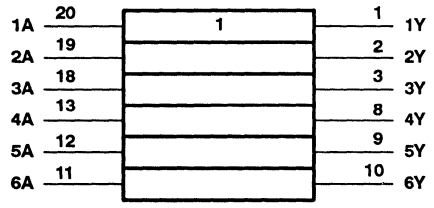
These devices contain six independent noninverters. They perform the Boolean function Y = A.

The 54ACT11034 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11034 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

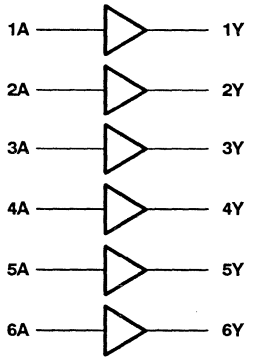
INPUT A	OUTPUT Y
H	H
L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, and N packages.

logic diagram (positive)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11034		74ACT11034		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11034		74ACT11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

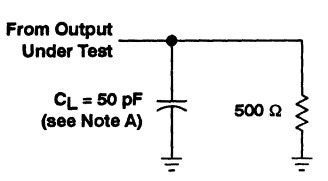
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11034		74ACT11034		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1.5	6.1	8.9	1.5	10.5	1.5	9.9	ns
t_{PHL}			1.5	5.2	8	1.5	9.6	1.5	8.9	

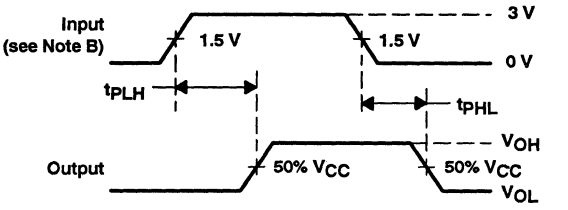
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



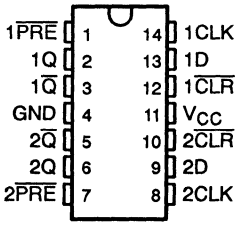
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

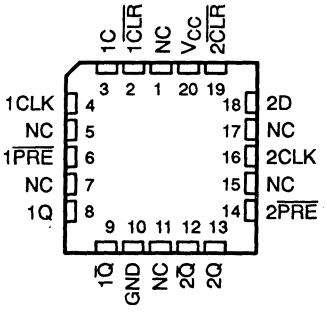
Figure 1. Load Circuit and Voltage Waveforms

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11074 . . . J PACKAGE
74AC11074 . . . D, N, OR PW PACKAGE
(TOP VIEW)



54AC11074 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input that meets the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

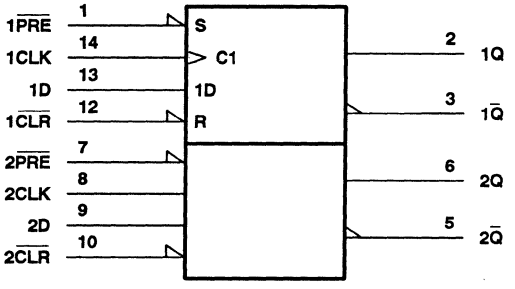
The 54AC11074 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11074 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11074			74AC11074			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11074		74AC11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

			T_A = 25°C		54AC11074		74AC11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time, before CLK↑	Data high or low	5		5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	1		1		1		
t_h	Hold time, after CLK↑		0		0		0		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		54AC11074		74AC11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low or CLK high	4		4		4		
t_{su}	Setup time, before CLK↑	Data high or low	3.5		3.5		3.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	1		1		1		
t_h	Hold time, after CLK↑		0		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11074		74AC11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	5.8	9.3	1.5	10.5	1.5	10	ns
t_{PHL}			1.5	6.5	11.4	1.5	12.9	1.5	12.2	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	7.7	10.5	1.5	12.1	1.5	11.3	ns
t_{PHL}			1.5	7.3	9.7	1.5	11.3	1.5	10.6	

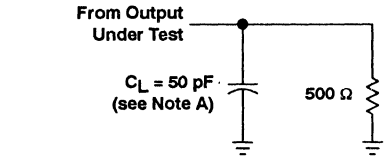
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11074		74AC11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	150		125		125		
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	4.2	6.6	1.5	7.5	1.5	7.1	ns
t_{PHL}			1.5	4.7	8.2	1.5	9.6	1.5	9	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	5.4	7.5	1.5	8.7	1.5	8.2	ns
t_{PHL}			1.5	5	6.9	1.5	8	1.5	7.5	

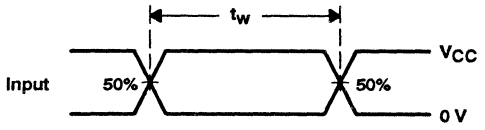
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	30	pF

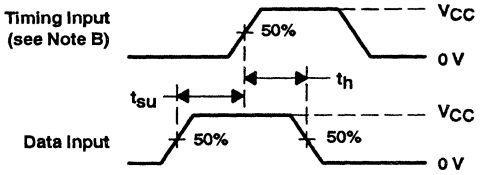
PARAMETER MEASUREMENT INFORMATION



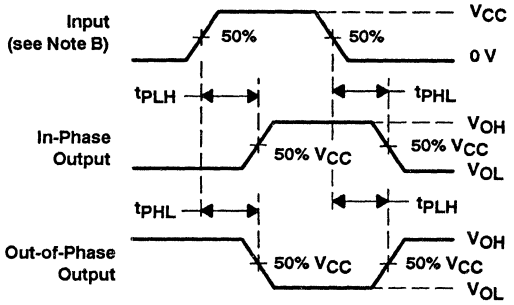
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



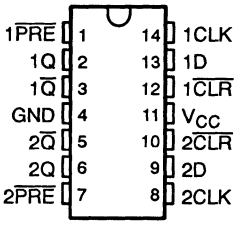
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

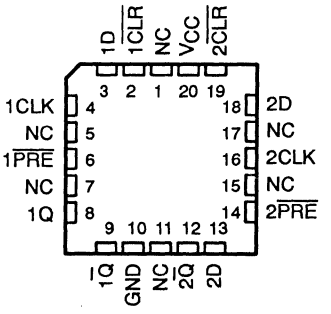
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11074 . . . J PACKAGE
74ACT11074 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11074 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

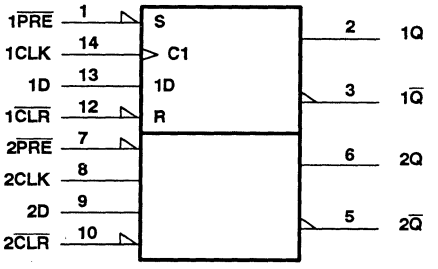
The 54ACT11074 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11074 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11074		74ACT11074		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = − 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = − 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = − 50 mA‡	5.5 V				3.85				
	I_{OH} = − 75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT11074		74ACT11074		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time before CLK↑	Data high or low	4.5		4.5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK↑		0		0		0		ns

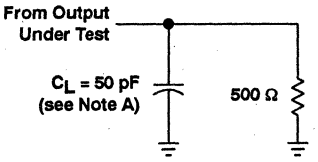
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	5.7	8.9	1.5	10.1	1.5	9.6	ns
t_{PHL}			1.5	6.6	11.3	1.5	13.3	1.5	12.5	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	6	8.5	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	5.7	8	1.5	9.4	1.5	8.8	

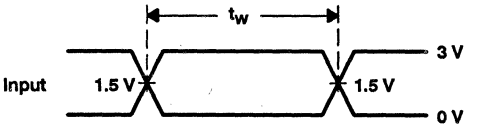
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz	30	pF

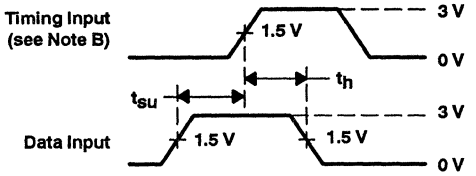
PARAMETER MEASUREMENT INFORMATION



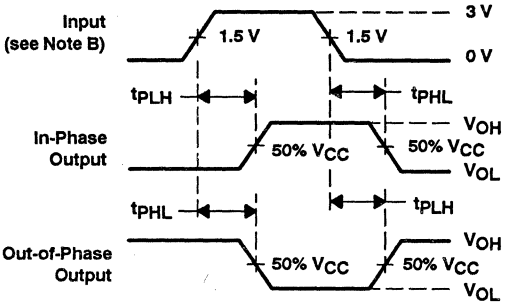
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

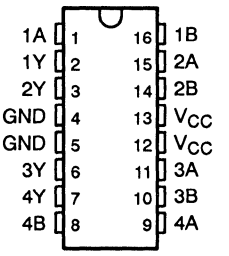
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3375, NOVEMBER 1989 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This device contains four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

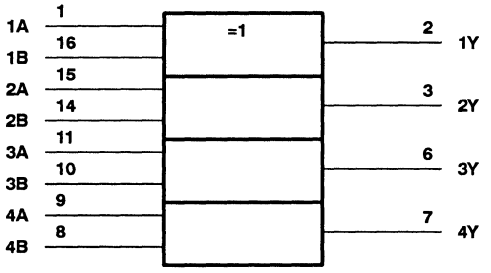
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The 74AC11086 is characterized for operation from –40°C to 85°C.

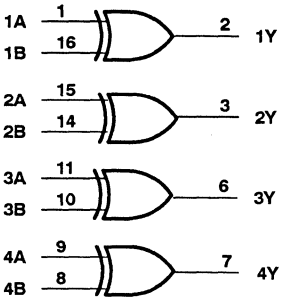
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

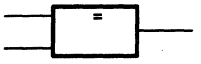
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

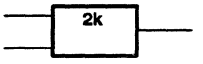
These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



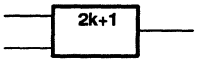
The output is active (high) if all inputs stand at the same logic level (i.e., A=B).

EVEN-PARITY ELEMENT



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active (high).

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active (high).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5.6	9.4	1.5	10.6	ns
t_{PHL}			1.5	5.1	7.4	1.5	8.2	

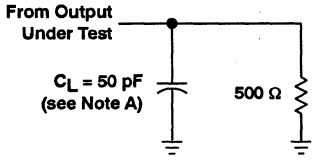
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	3.8	6.8	1.5	7.6	ns
t_{PHL}			1.5	3.8	6.2	1.5	6.8	

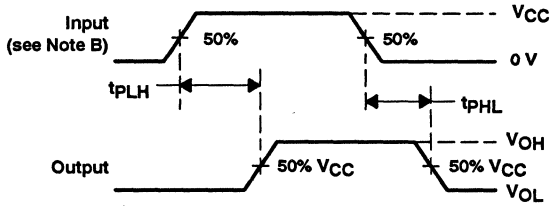
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

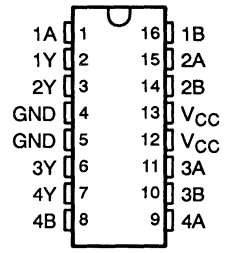
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS091 – D3990, NOVEMBER 1989 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This device contains four independent 2-input exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

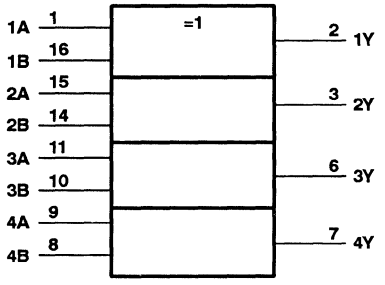
A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The 74ACT11086 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

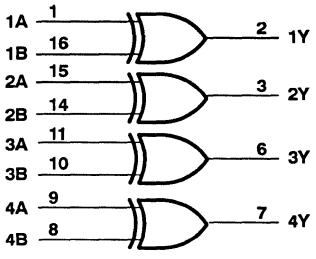
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

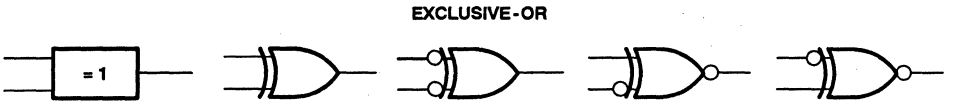
logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage		2	V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

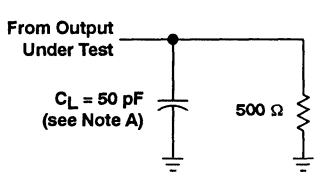
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5.1	8.7	1.5	9.6	ns
t_{PHL}			1.5	5.1	8	1.5	9	

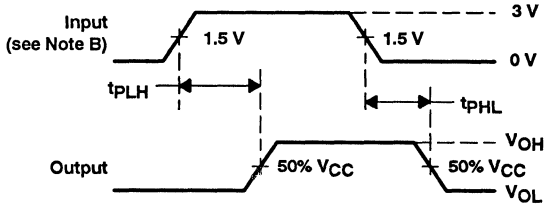
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	26	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



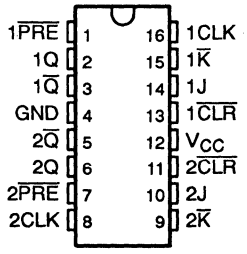
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

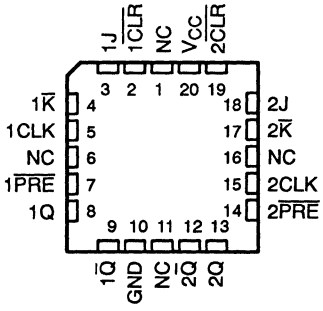
Figure 1. Load Circuit and Voltage Waveforms

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **ESD Protection Exceeds 2000 V, MIL STD-883C Method 3015**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11109 . . . J PACKAGE
74AC11109 . . . D OR N PACKAGE
(TOP VIEW)



54AC11109 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops by tying the J and $\overline{K}$ inputs together.

The 54AC11109 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11109 is characterized for operation from −40°C to 85°C.

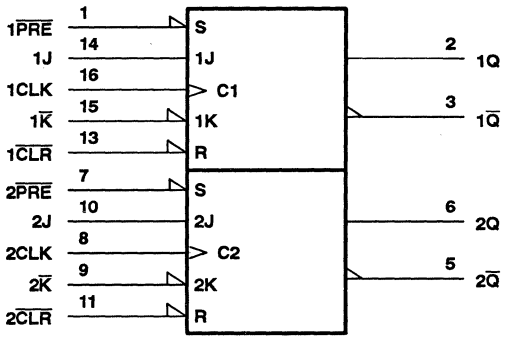
FUNCTION TABLE
(each gate)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11109			74AC11109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

			T_A = 25°C		54AC11109		74AC11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	70	0	70	0	70	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK low or CLK high	7.2		7.2		7.2		
t_{su}	Setup time before CLK↑	Data high or low	5.5		5.5		5.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2.5		2.5		2.5		
t_h	Hold time after CLK↑		0		0		0		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		54AC11109		74AC11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time, before CLK↑	Data high or low	4.5		4.5		2.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, after CLK↑		0		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70	100		70		70		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	6.5	9	1.5	10.5	1.5	9.9	ns
t_{PHL}			1.5	8	12.6	1.5	14.4	1.5	13.7	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	8	11.4	1.5	13.5	1.5	12.7	ns
t_{PHL}			1.5	7.5	10.5	1.5	12.7	1.5	11.8	

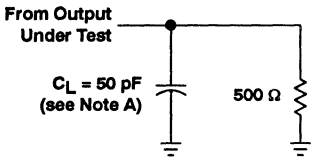
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11109		74AC11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	4.5	6.5	1.5	7.6	1.5	7.1	ns
t_{PHL}			1.5	5	8.6	1.5	10.2	1.5	9.6	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	5.5	7.9	1.5	9.4	1.5	8.8	ns
t_{PHL}			1.5	5	7.3	1.5	8.6	1.5	8.1	

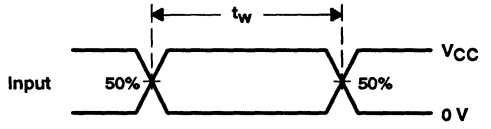
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	32	pF

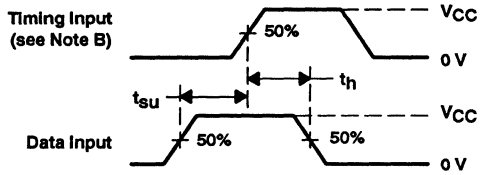
PARAMETER MEASUREMENT INFORMATION



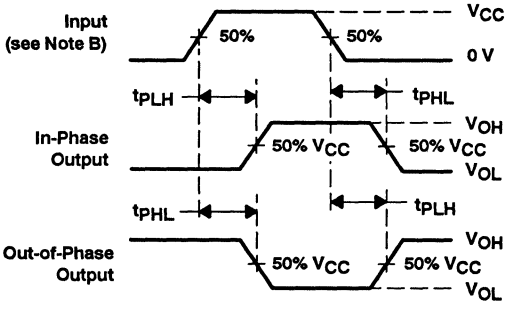
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



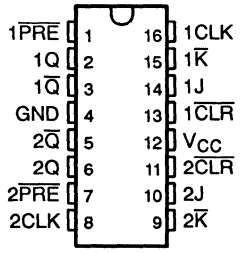
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

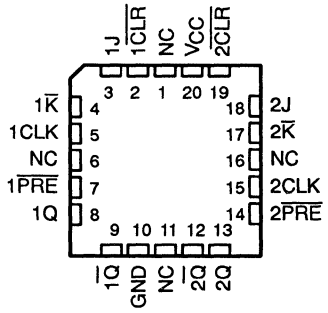
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11109 . . . J PACKAGE
74ACT11109 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11109 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset (1$\overline{PRE}$ or 2$\overline{PRE}$) or clear (1$\overline{CLR}$ or 2$\overline{CLR}$) input sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The 54ACT11109 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11109 is characterized for operation from −40°C to 85°C.

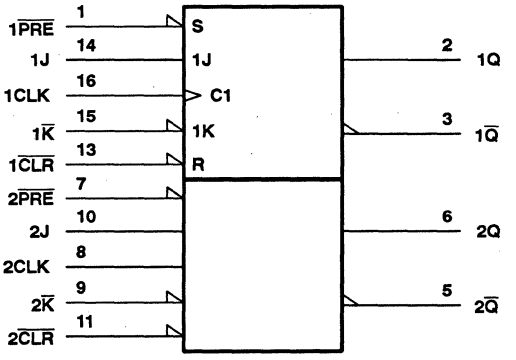
FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		54ACT11109		74ACT11109		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT11109		74ACT11109		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.5		5.5		5.5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time before CLK↑	Data high or low	5.5		5.5		5.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time, data after CLK↑		0		0		0		ns

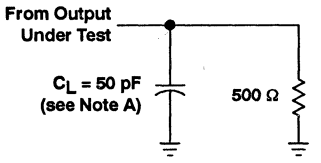
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11109		74ACT11109		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	PRE or CLR	Q or $\overline{Q}$	1.5	5.5	8.6	1.5	9.8	1.5	9.2	ns
t_{PHL}			1.5	6	10.8	1.5	12.6	1.5	11.8	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	6	8.3	1.5	9.7	1.5	9.1	ns
t_{PHL}			1.5	5.5	7.6	1.5	9	1.5	8.3	

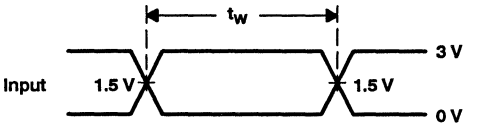
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF, f = 1 MHz	31	pF

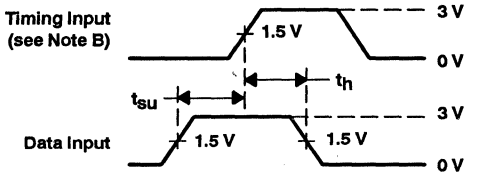
PARAMETER MEASUREMENT INFORMATION



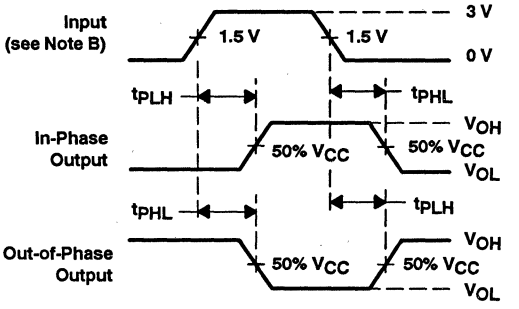
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



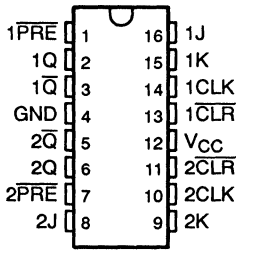
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

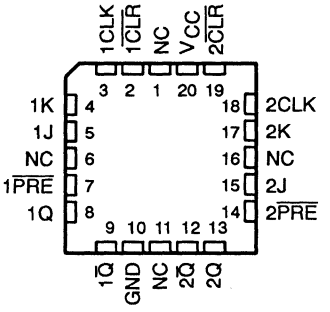
Figure 1. Load Circuit and Voltage Waveforms

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **ESD Protection Exceeds 2000 V, MIL STD-883C Method 3015**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11112 . . . J PACKAGE
74AC11112 . . . D OR N PACKAGE
(TOP VIEW)



54AC11112 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 54AC11112 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11112 is characterized for operation from −40°C to 85°C.

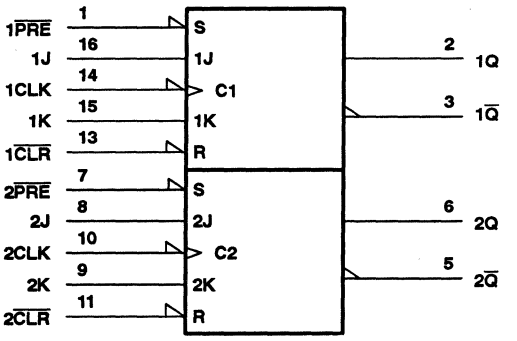
FUNCTION TABLE
(each gate)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_O	$\overline{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_O	$\overline{Q}_O$

† This configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

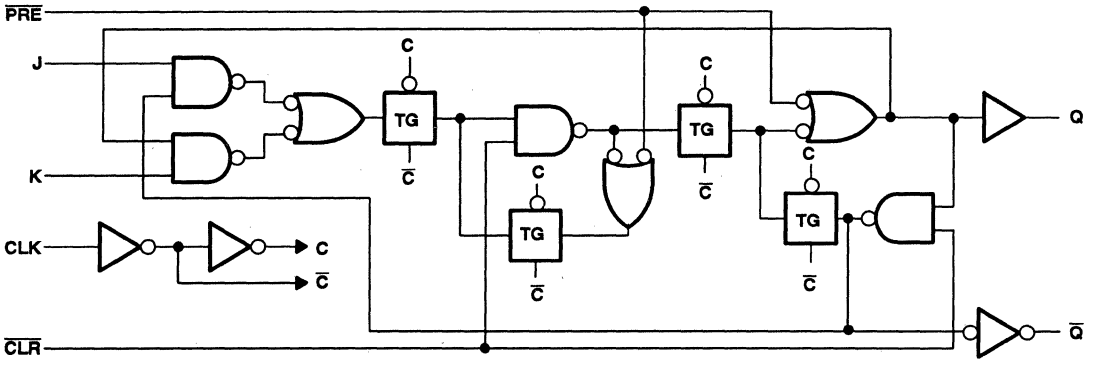
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11112			74AC11112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

			T_A = 25°C		54AC11112		74AC11112		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	70	0	70	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5		5		5		ns
		CLK low or CLK high	5		5		5		
t_{su}	Setup time before CLK↓	Data high or low	5		5		5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2.5		2.5		2.5		
t_h	Hold time after CLK↓		0.5		0.5		0.5		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		54AC11112		74AC11112		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low or CLK high	4		4		4		
t_{su}	Setup time before CLK↓	Data high or low	3.5		3.5		3.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK↓		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	150		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	4.9	6.7	1.5	7.6	1.5	7.3	ns
t_{PHL}			1.5	7	9.2	1.5	10.3	1.5	9.9	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	5.4	7.1	1.5	7.9	1.5	7.6	ns
t_{PHL}			1.5	6	7.9	1.5	9	1.5	8.5	

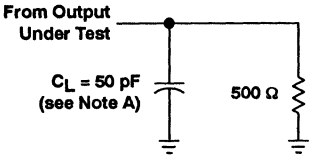
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11112		74AC11112		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	175		125		125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	3.3	5.1	1.5	5.6	1.5	5.4	ns
t_{PHL}			1.5	4.6	6.7	1.5	7.7	1.5	7.3	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	3.4	5.1	1.5	5.8	1.5	5.6	ns
t_{PHL}			1.5	4.2	6.3	1.5	7.4	1.5	7	

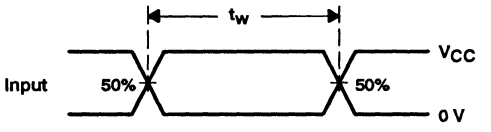
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	37	pF

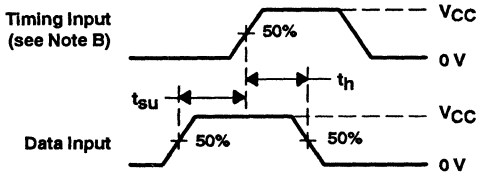
PARAMETER MEASUREMENT INFORMATION



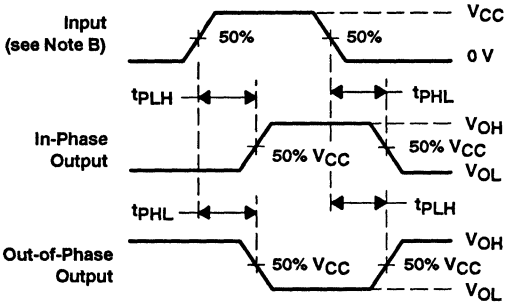
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



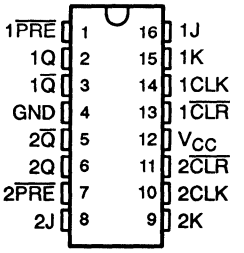
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Fully Buffered to Offer Maximum Isolation From External Disturbance**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This device contains two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{PRE}$ or $\overline{CLR}$ input sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The 74ACT11112 is characterized for operation from – 40°C to 85°C.

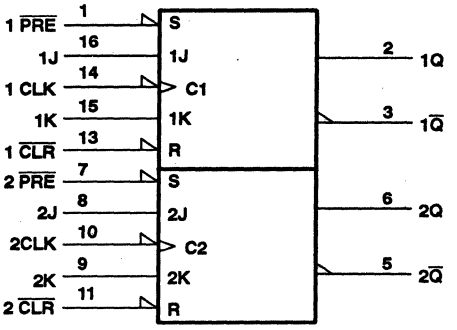
FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to the inactive (high) level.

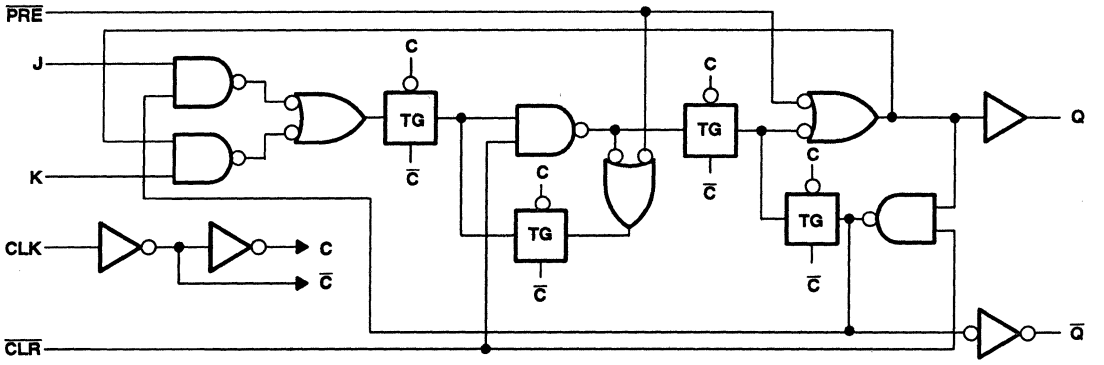
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordnace with ANSI/IEEE Std 91-1984 and IEC Publication 617-42.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		40	μA
ΔI_{CC}‡	$V_I = V_{CC}$ or GND		5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This parameter is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			125		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		4		ns
		CLK high or low	4		4		
t_{su}	Setup time before CLK↓	Data high or low	3.5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		2		
t_h	Hold time after CLK↓		1.5		1.5		ns

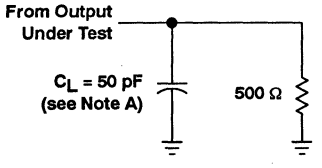
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	3.6	6.3	1.5	6.8	ns
t_{PHL}			1.5	4.6	7.4	1.5	8	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	4.2	7	1.5	7.7	ns
t_{PHL}			1.5	4.7	7.4	1.5	8.4	

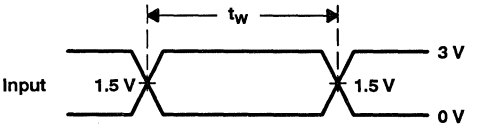
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	C_L = 50 pF,	f = 1 MHz	39	pF

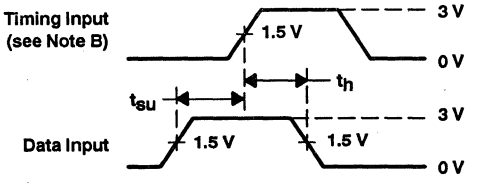
PARAMETER MEASUREMENT INFORMATION



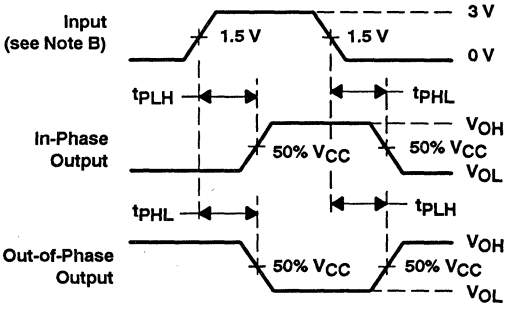
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

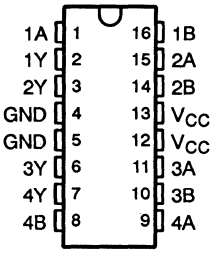
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS113 – D3482, MARCH 1990 – REVISED APRIL 1993

- **Operation From Very Slow Input Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Both Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. It performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

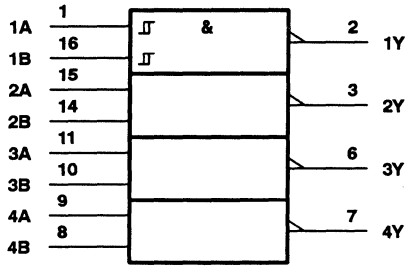
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The 74AC11132 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

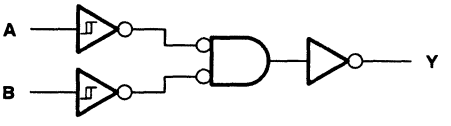
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.2			V
		V_{CC} = 4.5 V	3.2			
		V_{CC} = 5.5 V	3.9			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.5	mA
		V_{CC} = 4.5 V			0.9	
		V_{CC} = 5.5 V			1.1	
V_I	Input voltage				– 24	mA
V_O	Output voltage				– 24	
I_{OH}	High-level output current	V_{CC} = 3 V	0		V_{CC}	V
		V_{CC} = 4.5 V	0		V_{CC}	
		V_{CC} = 5.5 V			–4	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		100	ns/V
T_A	Operating free-air temperature		– 40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+}		3 V			2.2		2.2	V
		4.5 V			3.2		3.2	
		5.5 V			3.9		3.9	
V_{T-}		3 V	0.5			0.5		V
		4.5 V	0.9			0.9		
		5.5 V	1.1			1.1		
V_{hys} ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2.2	6.2	9.2	2.2	10.3	ns
t_{PHL}			2.8	6.8	9.8	2.8	10.5	

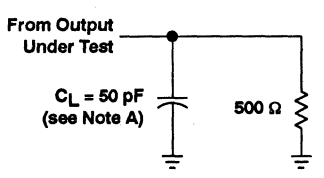
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.8	4.2	6.9	1.8	7.5	ns
t_{PHL}			2.3	4.8	7.3	2.3	8	

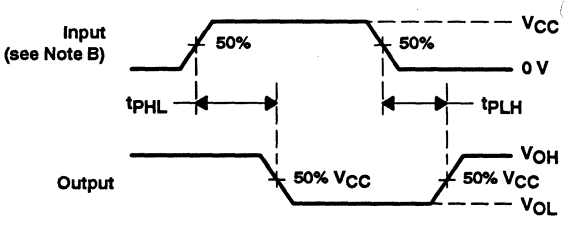
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



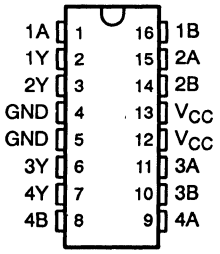
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

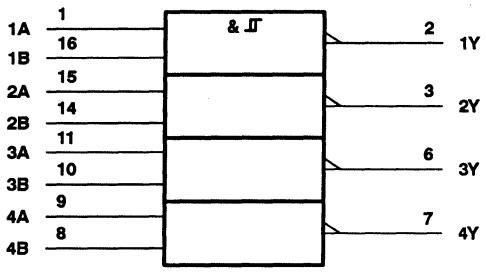
This device contains four independent 2-input NAND gates with Schmitt-trigger inputs. Because of the Schmitt action, they have different input threshold levels for positive- and negative-going signals. Each gate performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 74ACT11132 is characterized for operation from −40°C to 85°C.

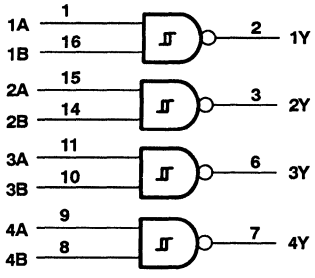
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{T+}			4.5 V			2		2	V
			5.5 V			2		2	
V_{T-}			4.5 V			0.8		0.8	V
			5.5 V			0.8		0.8	
V_{Hys} ($V_{T+} - V_{T-}$)			4.5 V	0.4		1.2	0.4	1.2	V
			5.5 V	0.4		1.2	0.4	1.2	
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

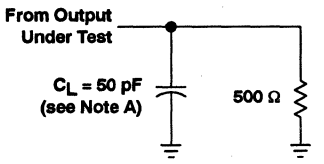
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2.6	5.3	8	2.6	8.8	ns
t_{PHL}			3.7	6.4	8.1	3.7	9.3	

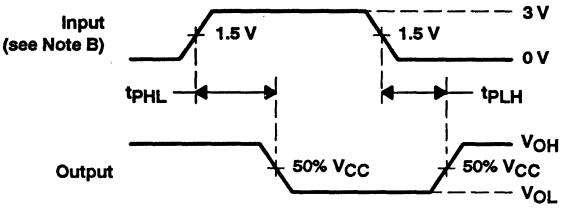
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	29	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

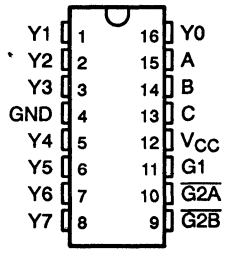
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

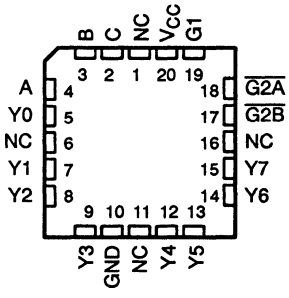
D3102, MAY 1988 – REVISED APRIL 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11138 . . . J PACKAGE
74AC11138 . . . D OR N PACKAGE
(TOP VIEW)



54AC11138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AC11138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

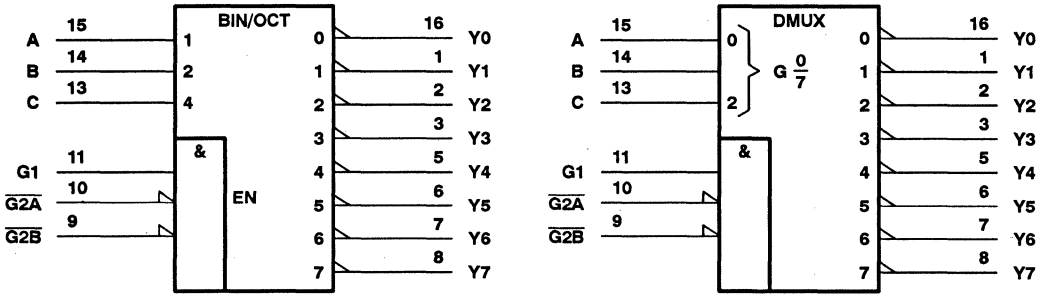
The 54AC11138 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11138 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

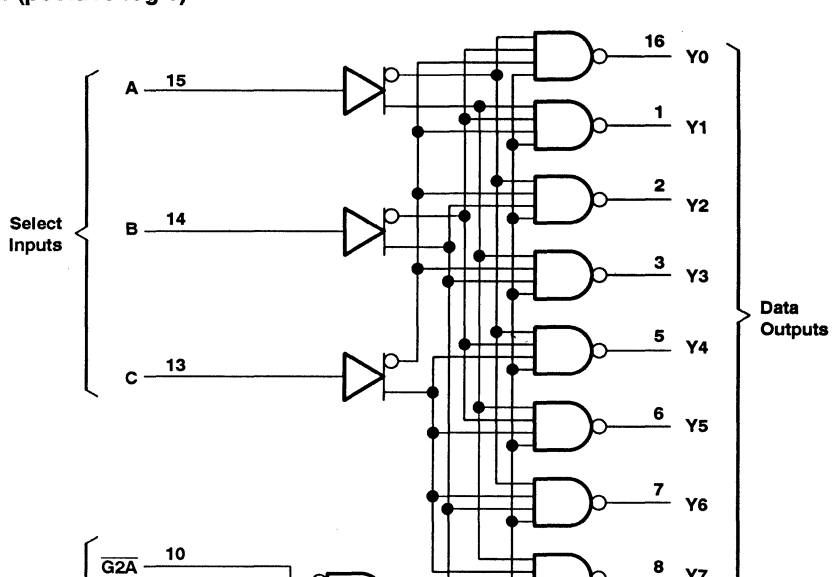
ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			54AC11138			74AC11138			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11138		74AC11138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11138		74AC11138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	8.3	10.2	1.5	12.3	1.5	11.4	ns
t_{PHL}			1.5	8.9	10.9	1.5	13.2	1.5	12.2	
t_{PLH}	G1	Any Y	1.5	7.2	9.2	1.5	10.8	1.5	10.2	ns
t_{PHL}			1.5	7.3	9.4	1.5	11.3	1.5	10.5	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	1.5	8.2	10.4	1.5	12.3	1.5	11.5	ns
t_{PHL}			1.5	8.3	10.4	1.5	12.5	1.5	11.6	

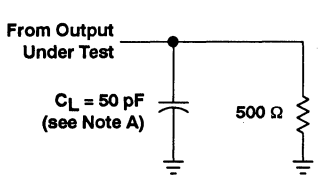
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11138		74AC11138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	5.7	7.3	1.5	8.7	1.5	8.1	ns
t_{PHL}			1.5	6.2	7.9	1.5	9.5	1.5	8.8	
t_{PLH}	G1	Any Y	1.5	5.1	6.9	1.5	7.9	1.5	7.5	ns
t_{PHL}			1.5	5.2	6.9	1.5	8.3	1.5	7.7	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	1.5	5.8	7.6	1.5	8.9	1.5	8.3	ns
t_{PHL}			1.5	5.6	7.5	1.5	9	1.5	8.3	

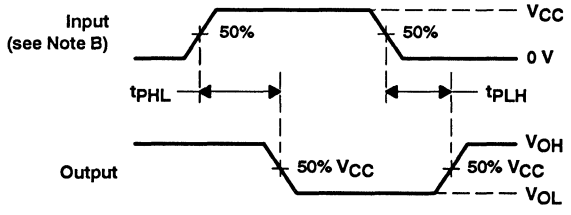
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	51	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

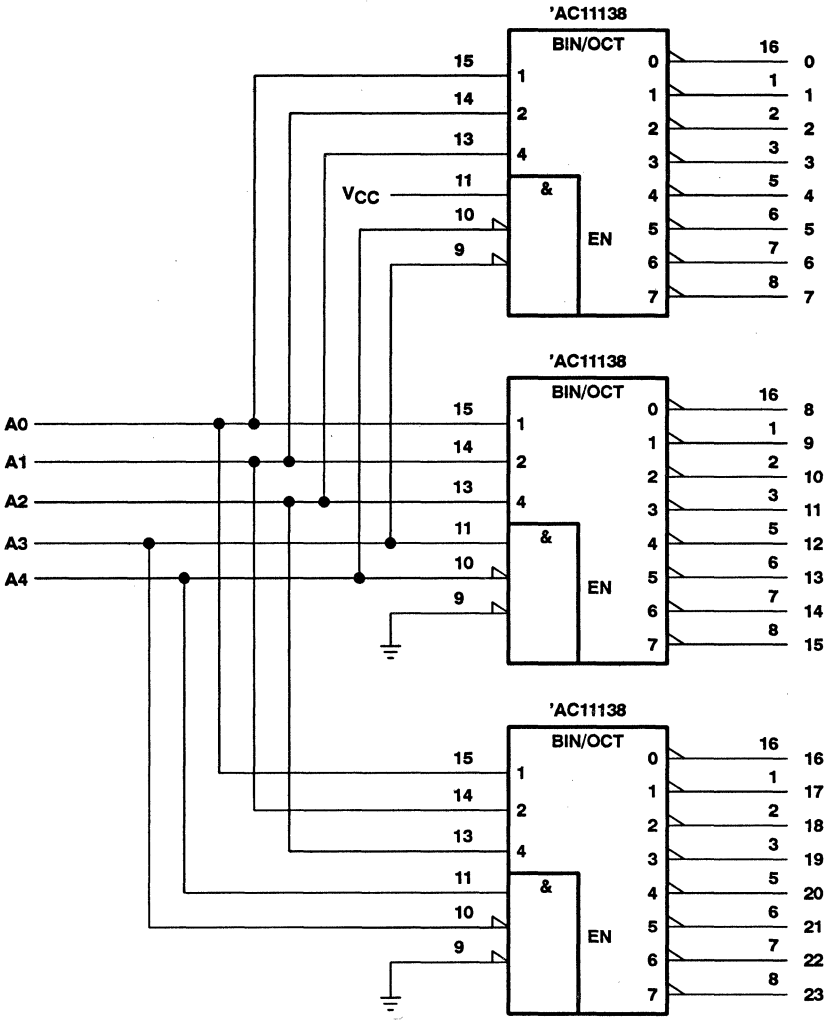


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

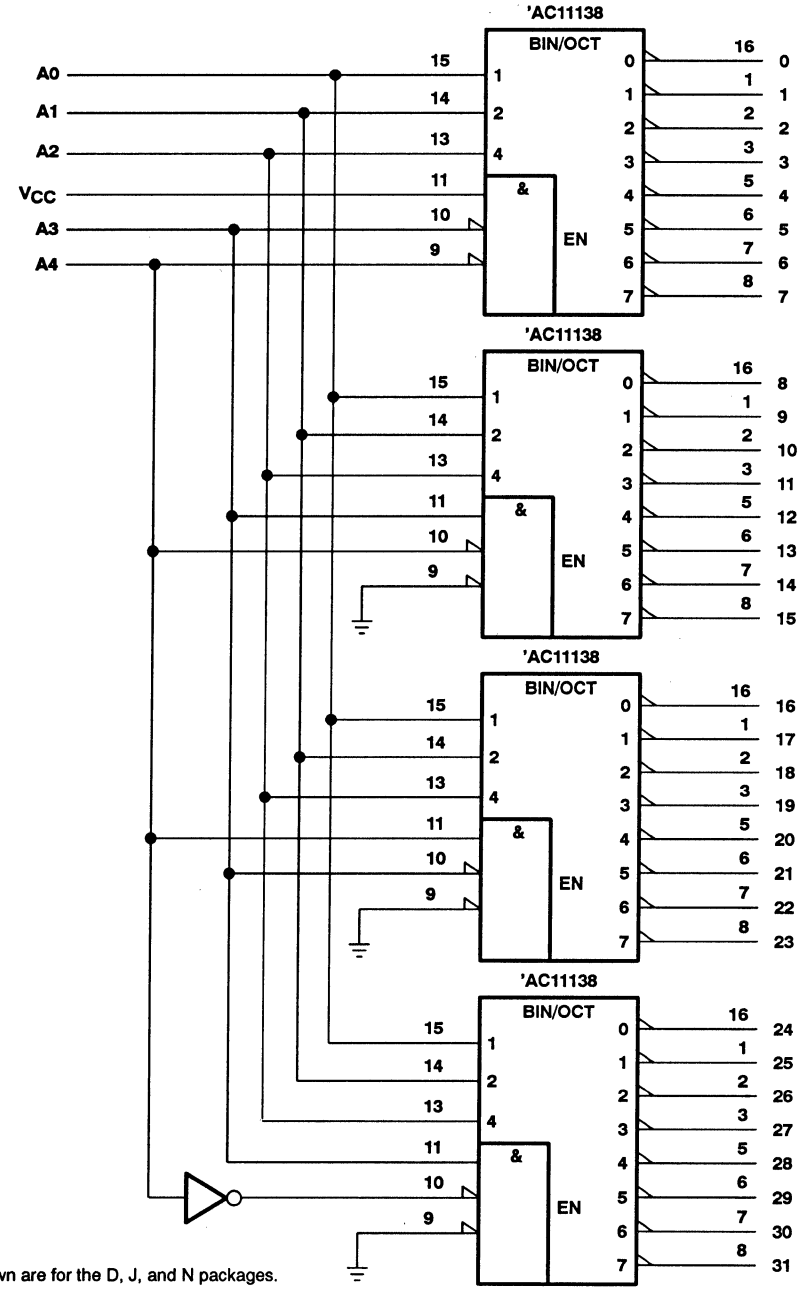
TYPICAL APPLICATION DATA



Pin numbers shown are for the D, J, and N packages.

Figure 2. 24-Bit Decoding Scheme

TYPICAL APPLICATION DATA



Pin numbers shown are for the D, J, and N packages.

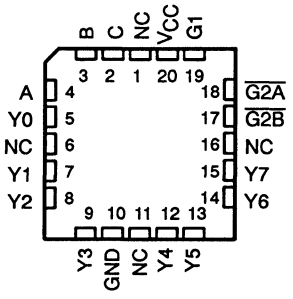
Figure 3. 32-Bit Decoding Scheme

SCAS050A – D3266, JANUARY 1989 – REVISED APRIL 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **650-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11138 . . . J PACKAGE
74ACT11138 . . . D, N, OR PW PACKAGE
(TOP VIEW)

54ACT11138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

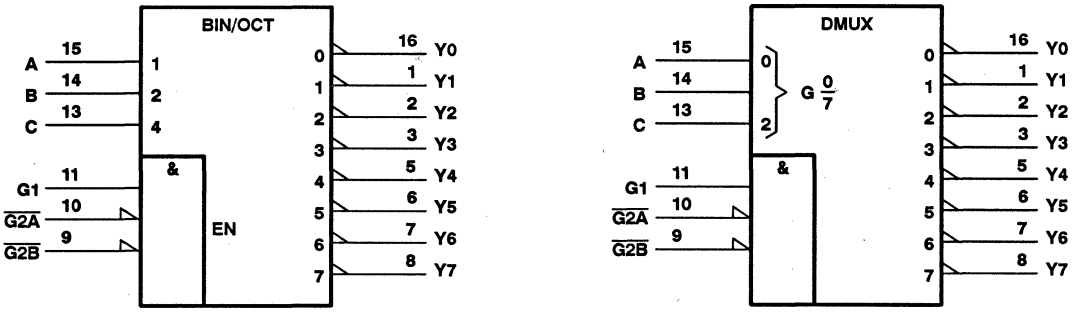
The 'ACT11138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 54ACT11138 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11138 is characterized for operation from – 40°C to 85°C.

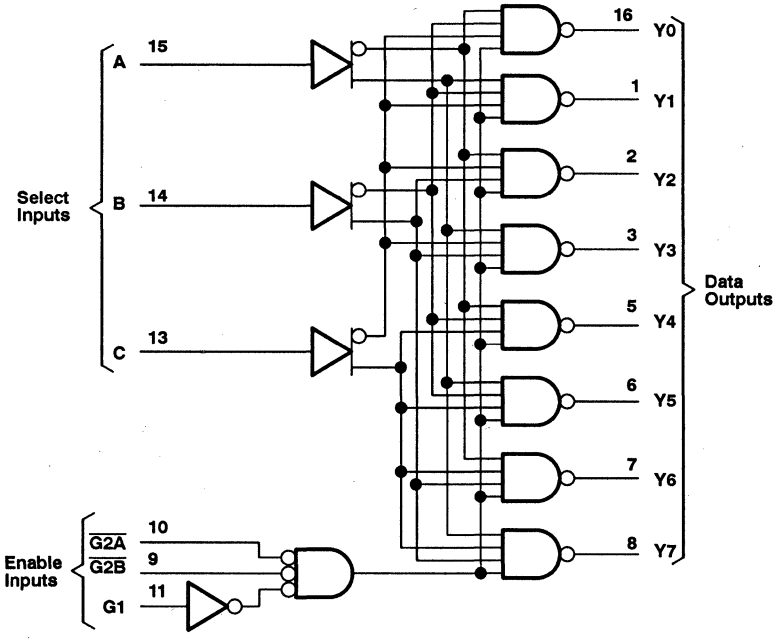
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11138		74ACT11138		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11138		74ACT11138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

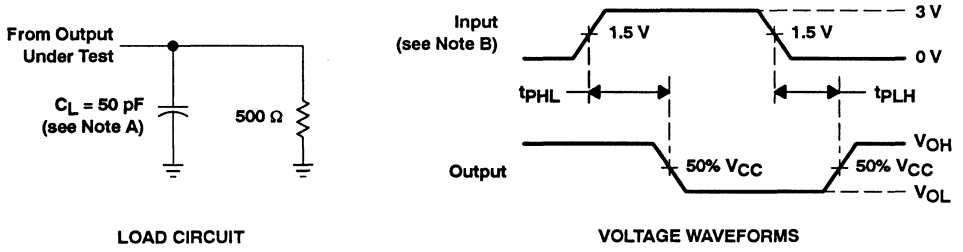
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11138		74ACT11138		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	6.1	8.9	1.5	10.5	1.5	9.8	ns
t_{PHL}			1.5	6	8.7	1.5	10.3	1.5	9.7	
t_{PLH}	G1	Y	1.5	5.5	8	1.5	9.4	1.5	8.9	ns
t_{PHL}			1.5	6	7.9	1.5	9.5	1.5	8.9	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	1.5	6.4	8.3	1.5	9.9	1.5	9.3	ns
t_{PHL}			1.5	6	8.8	1.5	10.5	1.5	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	88	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

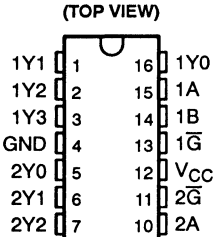
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3318, JULY 1989 – REVISED APRIL 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

D, N, OR PW PACKAGE
(TOP VIEW)



description

The 74AC11139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The 74AC11139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

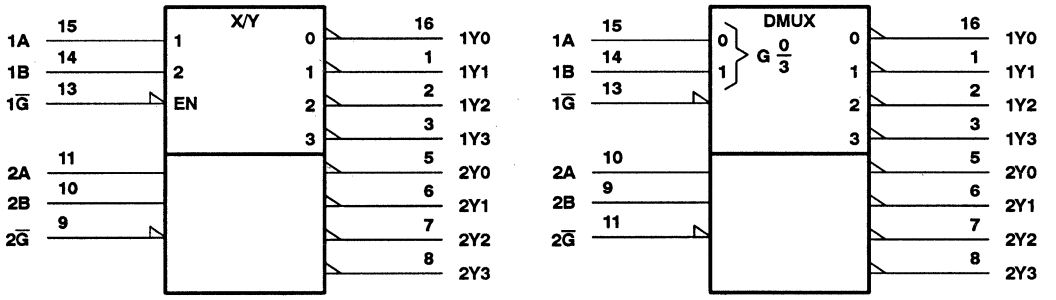
The 74AC11139 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUT $\overline{G}$	SELECT INPUTS		OUTPUTS			
	A	B	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

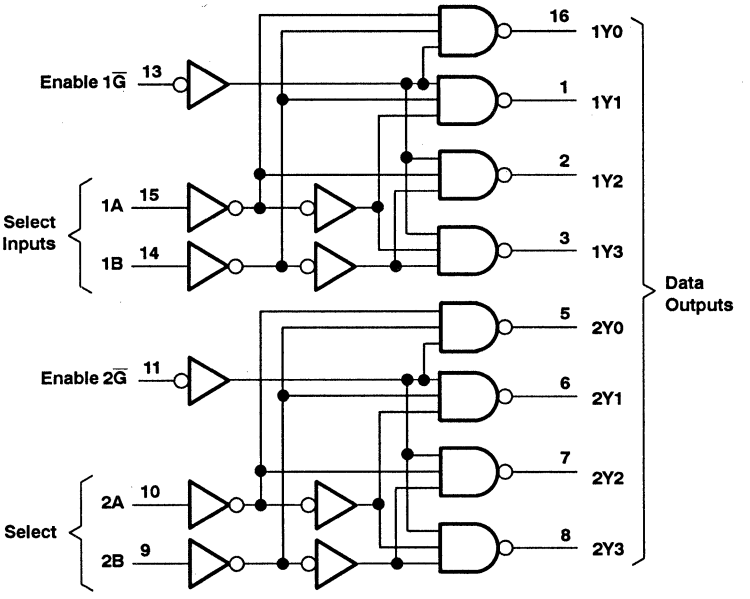
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5.3	8.1	1.5	9	ns
t_{PHL}			1.5	6	8.4	1.5	9.4	
t_{PLH}	$\overline{G}$	Y	1.5	5.3	6.9	1.5	7.6	ns
t_{PHL}			1.5	5.6	7.4	1.5	8.1	

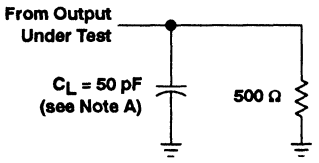
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	3.5	6	1.5	6.6	ns
t_{PHL}			1.5	4.1	6.3	1.5	6.9	
t_{PLH}	$\overline{G}$	Y	1.5	3.8	5.2	1.5	5.7	ns
t_{PHL}			1.5	4	5.6	1.5	6.2	

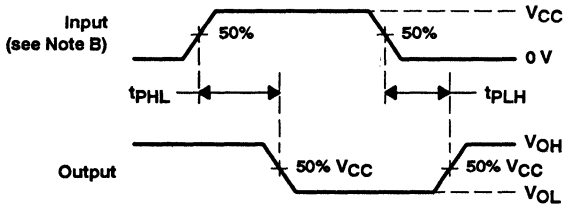
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	47	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

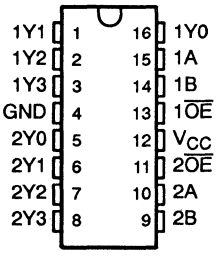
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS175 – D3907, SEPTEMBER 1991 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporate Two Output-Enable Inputs to Simplify Cascading and/or Data Reception**
- **Fully Synchronous Operation for Counting**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

D, N, OR PW PACKAGE
(TOP VIEW)



description

The 74ACT11139 is designed to be used in high-performance memory-decoding or data-routing applications that require very short propagation delay times. In high-performance memory systems, this decoder is used to minimize the effects of system decoding.

The 74ACT11139 is comprised of two individual 2-line to 4-line decoders in a single package. The active-low output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used as a data line in demultiplexing applications. this decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

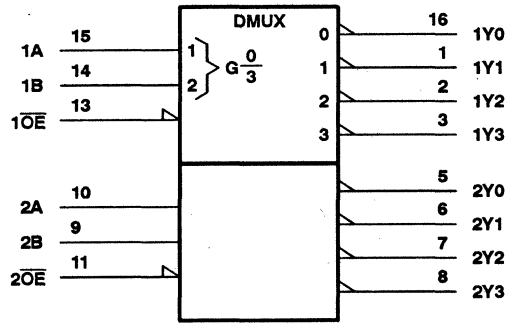
The 74ACT11139 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

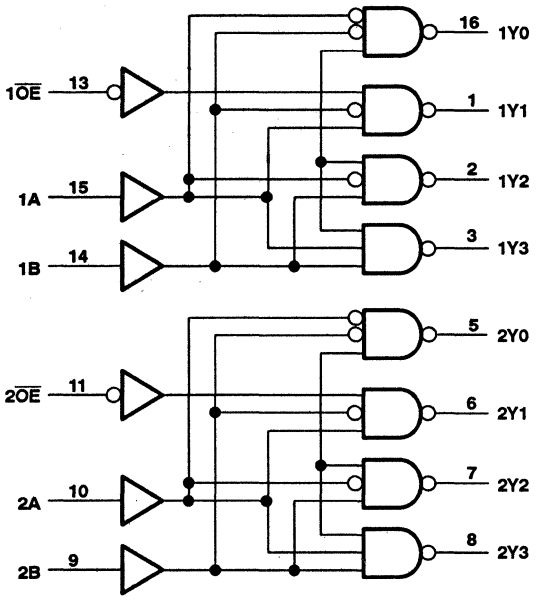
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

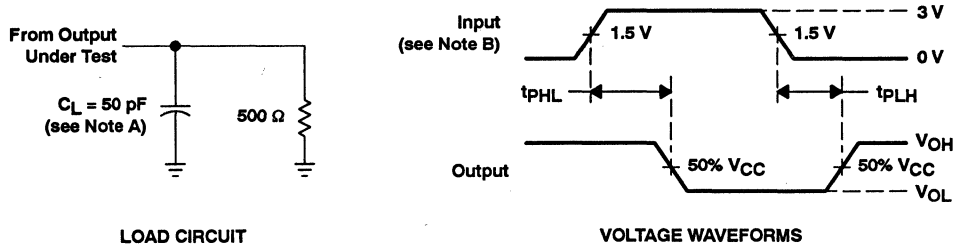
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.7	5.7	7.8	1.7	8.5	ns
t_{PHL}			2.1	5.5	7.4	2.1	8.5	
t_{PLH}	$\overline{OE}$	Y	2.7	5.3	7.2	2.7	7.9	ns
t_{PHL}			1.8	4.3	6.7	1.8	7.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	47	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

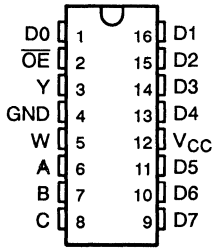
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3348, JUNE 1989 – REVISED APRIL 1993

- **8-Line to 1-Line Multiplexers Can Perform as Boolean Function Generators, Parallel-to-Serial Converters, or Data Source Selectors**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This monolithic data selector/multiplexer provides full binary decoding to select one-of-eight data sources. The strobe output-enable ($\overline{OE}$) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

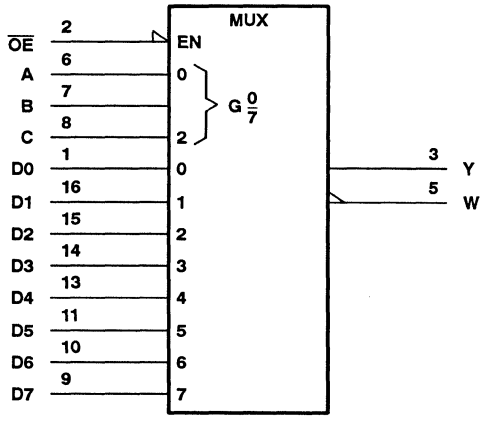
The 74AC11151 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{OE}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L= low level, X = irrelevant
D0, D1, . . . D7 = the level of the respective D input

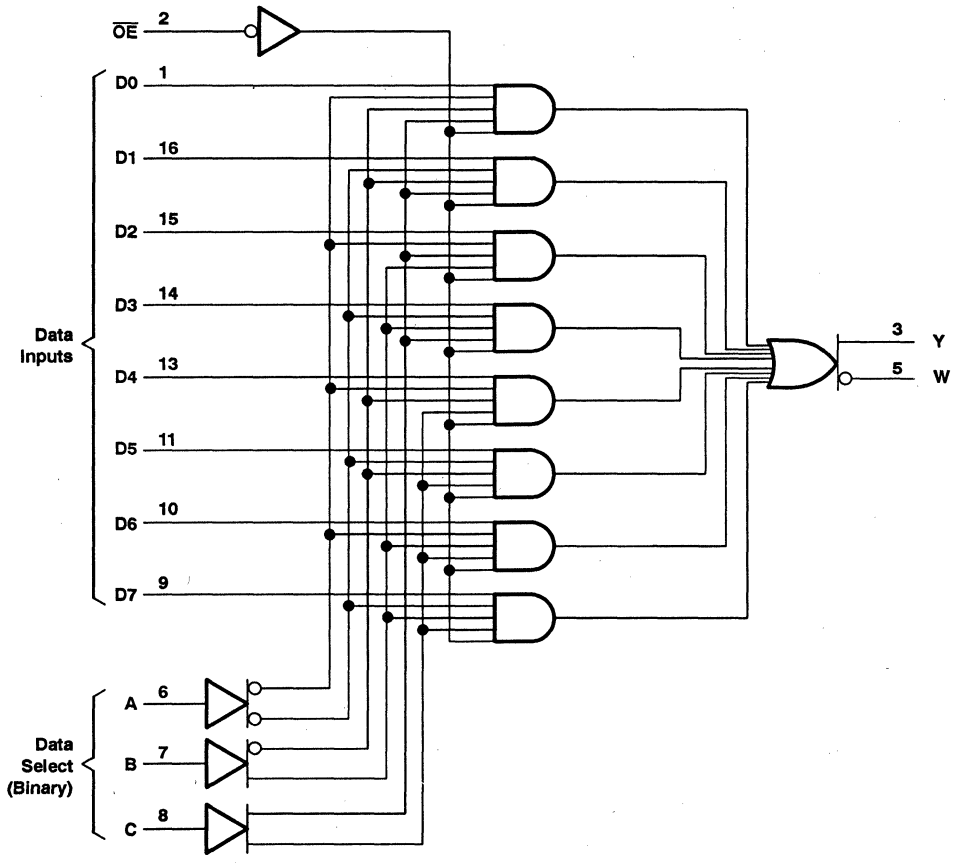
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
t_{PLH}	A, B, or C	Y	3.2	8.9	10.7	3.2	12	ns
t_{PHL}			3.4	8.9	10.8	3.4	12.1	
t_{PLH}	A, B, or C	W	3.2	8.6	10.3	3.2	11.6	ns
t_{PHL}			3.1	8.7	10.7	3.1	12	
t_{PLH}	Any D	Y	1.9	6.5	8.1	1.9	9.2	ns
t_{PHL}			1.9	6.4	8.1	1.9	8.9	
t_{PLH}	Any D	W	1.7	6.1	7.7	1.7	8.6	ns
t_{PHL}			1.9	6.4	8	1.9	8.8	
t_{PLH}	$\overline{OE}$	Y	1.3	4	5.5	1.3	6	ns
t_{PHL}			1.6	4.5	5.9	1.6	6.5	
t_{PLH}	$\overline{OE}$	W	2	5.2	6.7	2	7.4	ns
t_{PHL}			1.7	4.7	6.2	1.7	6.7	

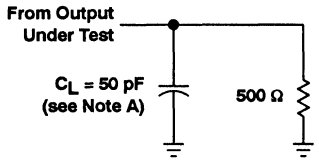
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B, or C	Y	2.5	5.4	7.3	2.5	8.3	ns
t_{PHL}			2.7	5.6	7.5	2.7	8.5	
t_{PLH}	A, B, or C	W	2.6	5.3	7.2	2.6	8.1	ns
t_{PHL}			2.6	5.4	7.4	2.6	8.4	
t_{PLH}	Any D	Y	1.5	4.1	5.8	1.5	6.5	ns
t_{PHL}			1.5	4	5.7	1.5	6.4	
t_{PLH}	Any D	W	1.4	3.7	5.5	1.4	6	ns
t_{PHL}			1.6	4.1	5.8	1.6	6.4	
t_{PLH}	$\overline{OE}$	Y	1.1	2.7	4.2	1.1	4.6	ns
t_{PHL}			1.4	3.1	4.6	1.4	5	
t_{PLH}	$\overline{OE}$	W	1.7	3.5	5.1	1.7	5.6	ns
t_{PHL}			1.4	3.1	4.6	1.4	5	

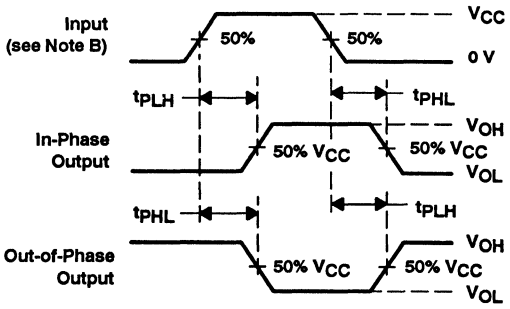
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	52	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

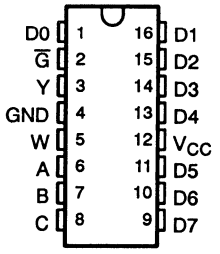
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS067A – D3349, JULY 1989 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **8-Line to 1-Line Multiplexers Can Perform as: Boolean Function Generators, Parallel-to-Serial Converters, Data Source Selectors**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This monolithic data selector/multiplexer provides full binary decoding to select one-of-eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

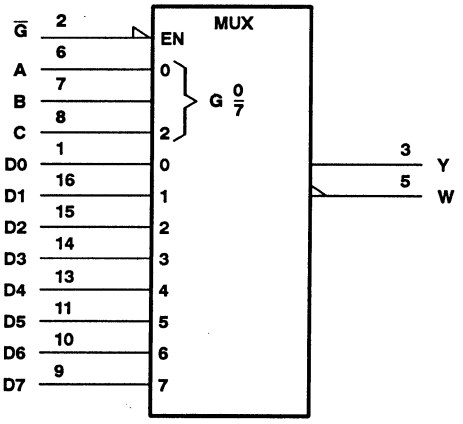
The 74ACT11151 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1, . . . D7 = the level of the respective D input

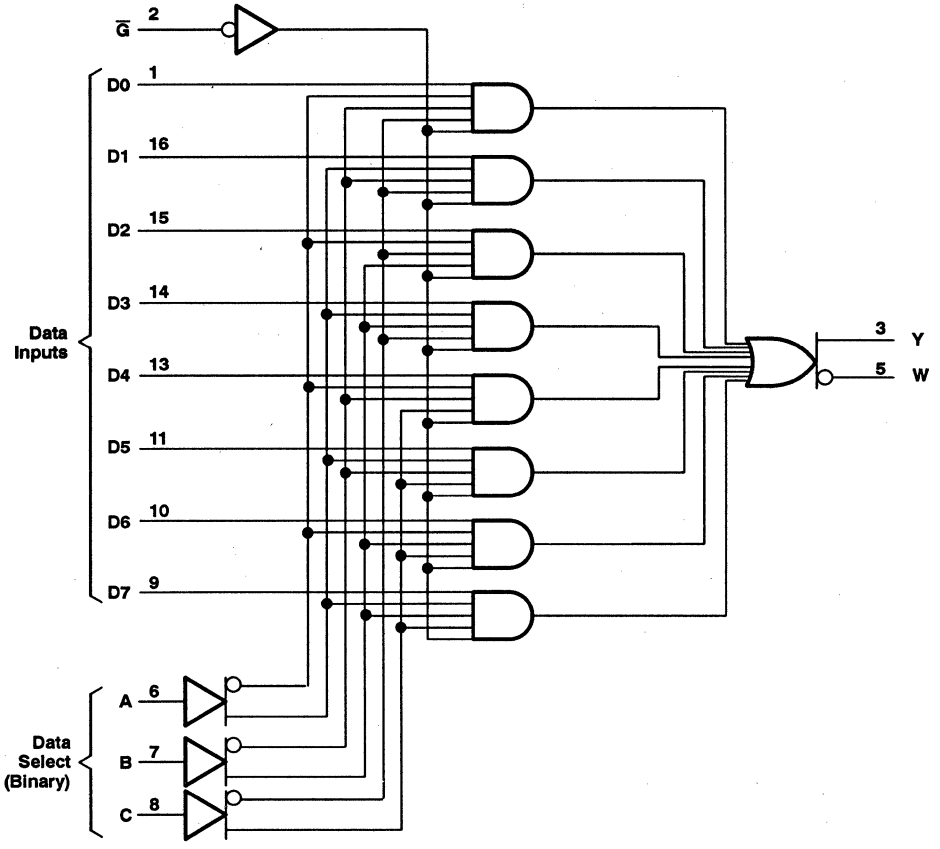
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

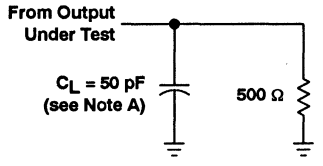
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B, or C	Y	3.6	6.8	9.9	3.6	11	ns
t_{PHL}			3.1	6.7	9.5	3.1	10.5	
t_{PLH}	A, B, or C	W	2.9	6.3	9	2.9	10	ns
t_{PHL}			2.7	6.3	9.3	2.7	10.4	
t_{PLH}	Any D	Y	3.2	5.7	7.5	3.2	8.3	ns
t_{PHL}			2.2	5.2	8	2.2	8.8	
t_{PLH}	Any D	W	2.1	4.7	7.3	2.1	7.8	ns
t_{PHL}			2.7	5.1	6.9	2.7	7.6	
t_{PLH}	$\overline{G}$	Y	1.5	3.7	5.8	1.5	6.3	ns
t_{PHL}			2.1	4.0	5.6	2.1	6.2	
t_{PLH}	$\overline{G}$	W	2.5	4.4	6.1	2.5	6.7	ns
t_{PHL}			1.7	4.1	6.4	1.7	6.9	

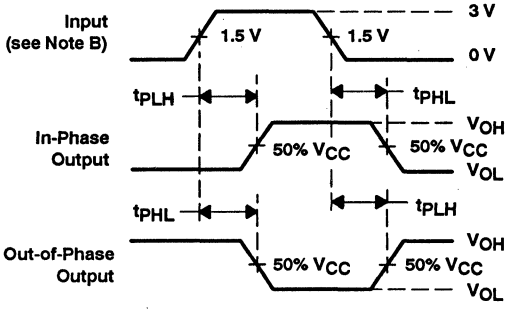
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	56	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

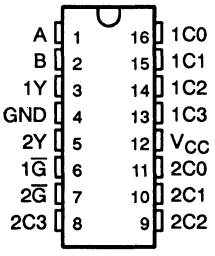
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3582, JUNE 1990 – REVISED APRIL 1993

- **Permits Multiplexing From N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to N Lines)**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This data selector/multiplexer contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The 74AC11153 is characterized for operation from −40°C to 85°C.

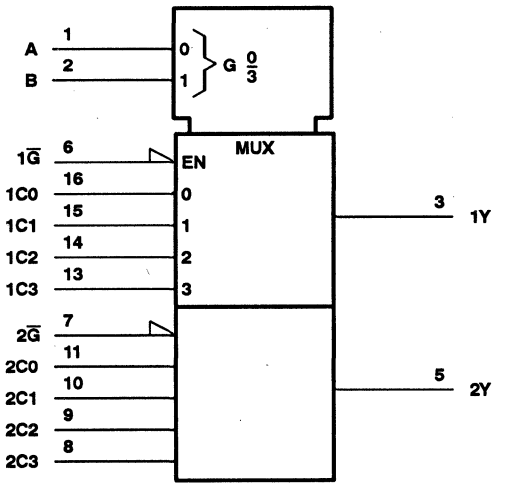
FUNCTION TABLE

INPUTS						STROBE $\overline{G}$	OUTPUT Y
SELECT		DATA					
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level, L = low level, X = irrelevant

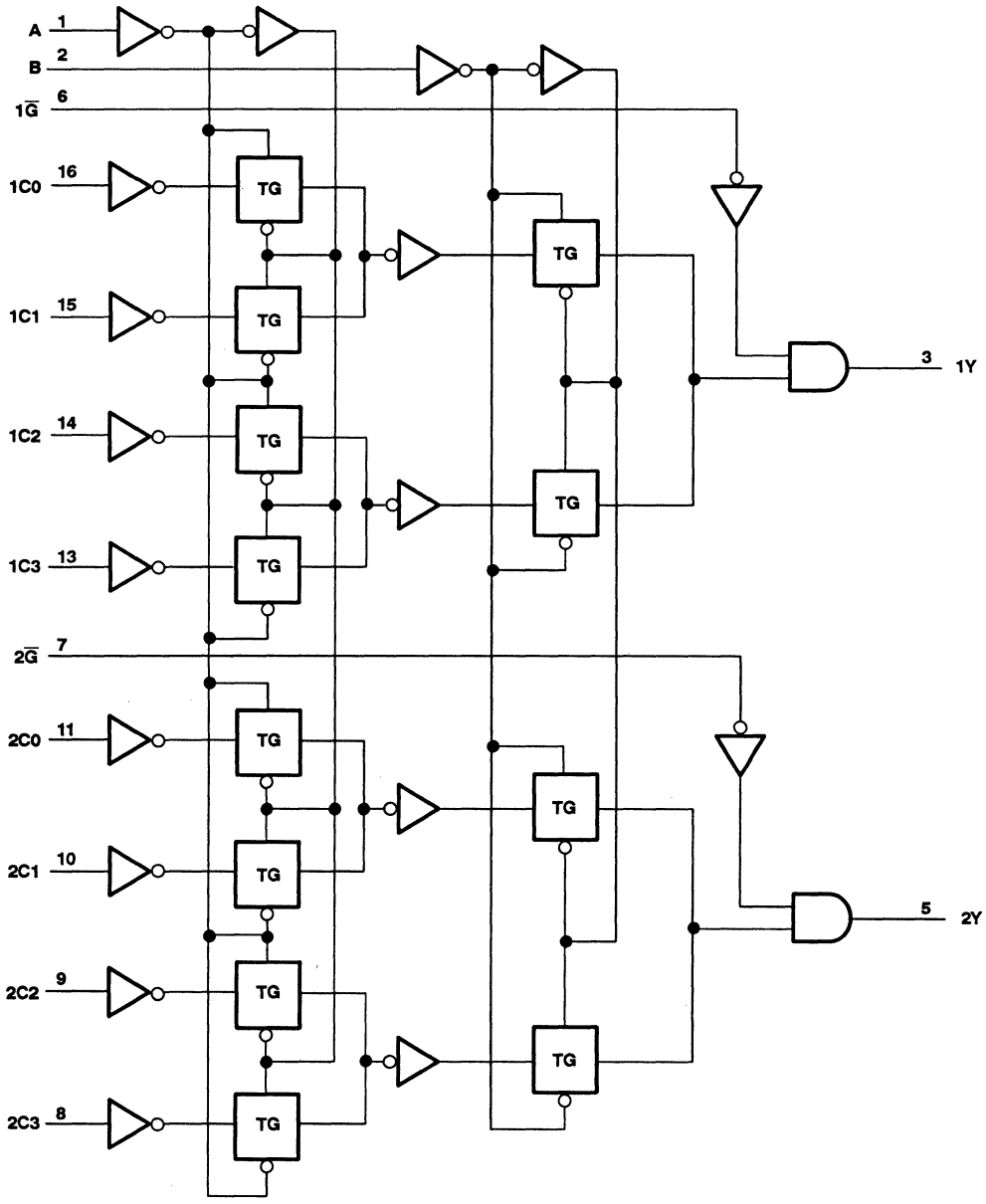
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2.3	7.4	9.5	2.3	10.5	ns
t_{PHL}			2.6	7.6	9.9	2.6	11	
t_{PLH}	Data (Any C)	Y	2.3	6.9	8.4	2.3	9.5	ns
t_{PHL}			2.6	7.1	8.7	2.6	9.9	
t_{PLH}	$\overline{G}$	Y	1.8	5.3	6.7	1.8	7.5	ns
t_{PHL}			1	5.2	7.2	1	8.5	

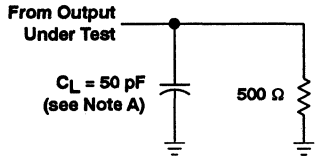
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2	4.7	6.8	2	7.6	ns
t_{PHL}			1.6	5.5	7.7	1.6	8.6	
t_{PLH}	Data (Any C)	Y	1.9	4.5	6.1	1.9	6.9	ns
t_{PHL}			2.5	5	6.9	2.5	7.8	
t_{PLH}	$\overline{G}$	Y	1.4	3.6	5.1	1.4	5.7	ns
t_{PHL}			1.8	4.3	5.8	1.8	6.7	

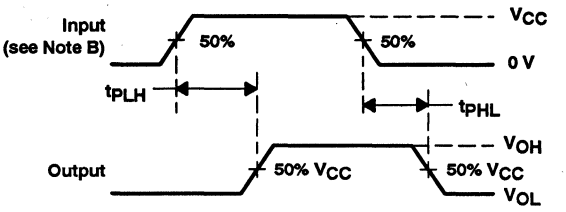
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	30	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

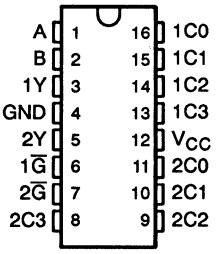
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS118A – D3583, JUNE 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N Lines to N Lines)**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This data selector/multiplexer contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

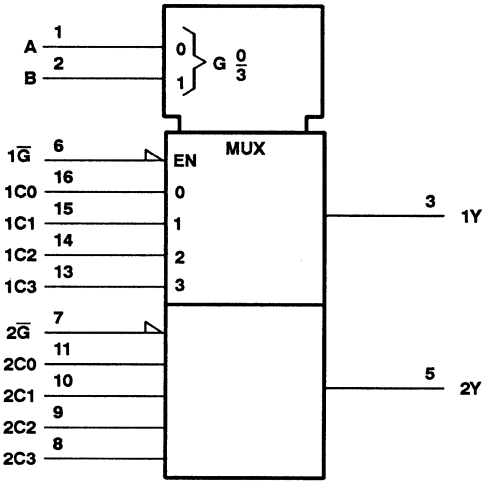
The 74ACT11153 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level, L = low level, X = irrelevant

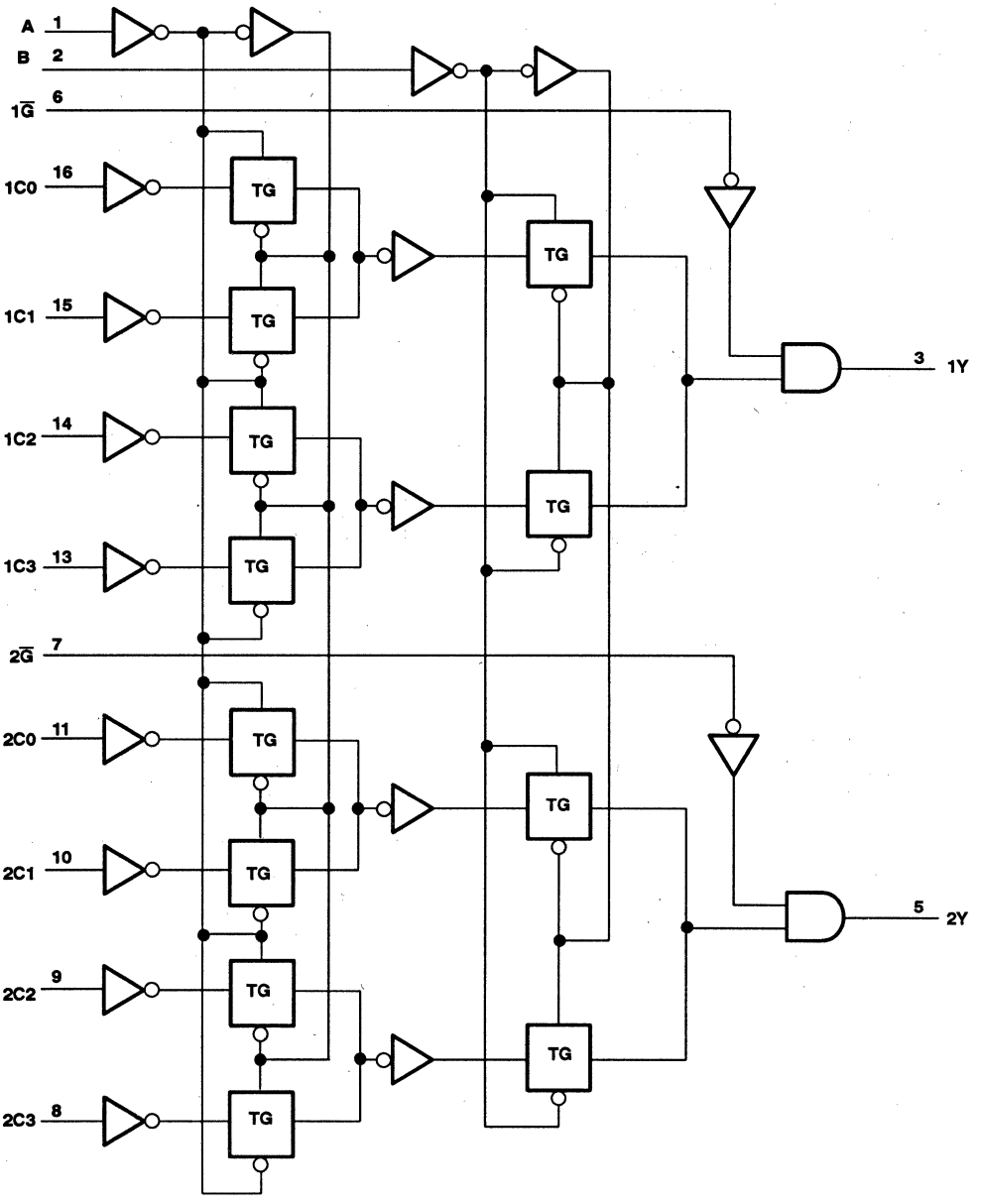
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

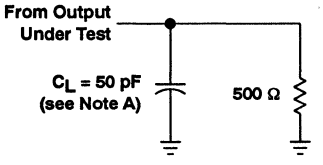
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2.8	6.4	9.8	2.8	10.9	ns
t_{PHL}			3.1	6.8	10	3.1	11	
t_{PLH}	Data (Any C)	Y	2.8	5.4	7.5	2.8	8.3	ns
t_{PHL}			3	6.4	8.8	3	9.8	
t_{PLH}	$\overline{G}$	Y	2.2	5.5	8.6	2.2	9.3	ns
t_{PHL}			2.9	5.6	6.6	2.9	7.6	

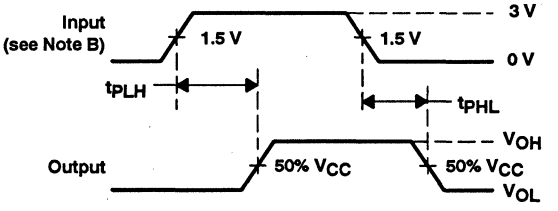
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	34	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

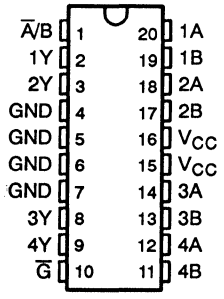
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS183 – D2957, JULY 1989 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

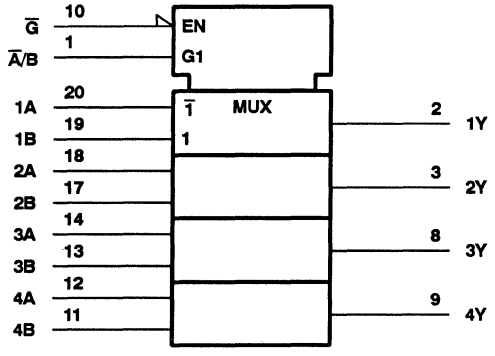
This data selector/multiplexer contains inverters and drivers to supply full data selection to the four output gates. A separate strobe ($\overline{G}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 74AC11157 provides true data.

The 74AC11157 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

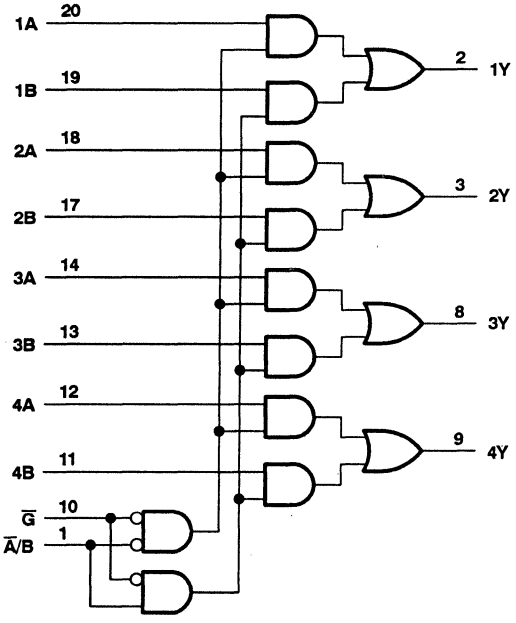
INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.8	6.2	8.5	1.8	9.5	ns
t_{PHL}			2.6	8.3	11.1	2.6	12.5	
t_{PLH}	$\overline{A}$/B	Y	1.9	6.8	8.9	1.9	10	ns
t_{PHL}			2.7	8.7	11.4	2.7	12.9	
t_{PLH}	$\overline{G}$	Y	1.6	6	8.6	1.6	9.2	ns
t_{PHL}			2.8	8.6	11.2	2.8	12.3	

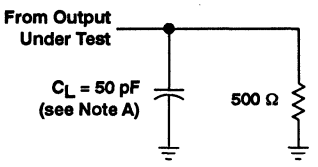
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	3.9	5.8	1.5	6.4	ns
t_{PHL}			2.2	5.3	7.5	2.2	8.6	
t_{PLH}	$\overline{A}$/B	Y	1.7	4.2	6.2	1.7	6.8	ns
t_{PHL}			2.3	5.5	8	2.3	9	
t_{PLH}	$\overline{G}$	Y	1.6	3.8	5.9	1.6	6.5	ns
t_{PHL}			2.3	5.4	7.8	2.3	8.8	

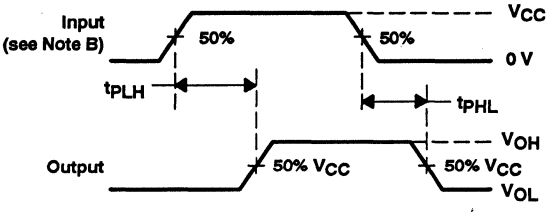
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	36	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

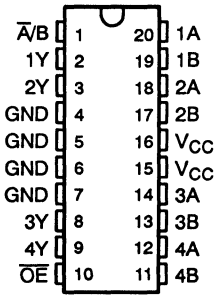
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS180 – D3908, SEPTEMBER 1991 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

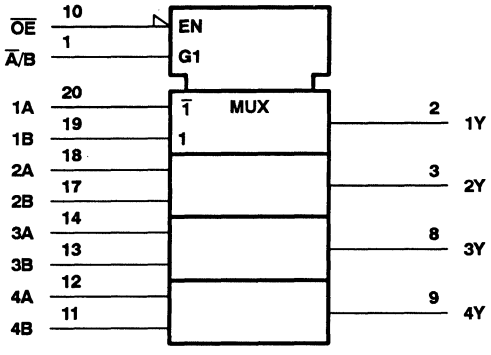
This data selector/multiplexer contains inverters and drivers to supply full data selection to the four output gates. A separate output-enable ($\overline{OE}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 74ACT11157 provides true data.

The 74ACT11157 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

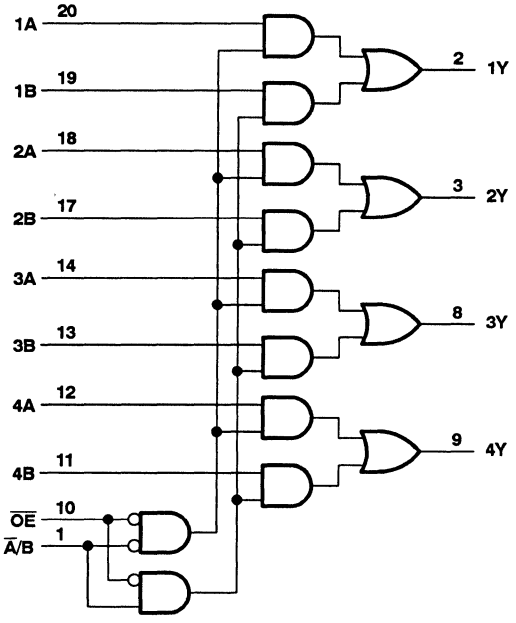
INPUTS				OUTPUT
$\overline{OE}$	A/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		3				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

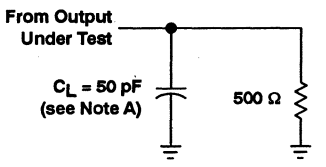
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2.6	5.1	7.1	2.6	7.8	ns
t_{PHL}			3.1	6.6	10.4	3.1	11.3	
t_{PLH}	$\overline{A}$/B	Y	2.3	5.6	8.7	2.3	9.5	ns
t_{PHL}			3.1	6.8	10.5	3.1	11.5	
t_{PLH}	$\overline{OE}$	Y	2.1	5.1	7.9	2.1	8.6	ns
t_{PHL}			3.6	6.9	9.7	3.6	10.8	

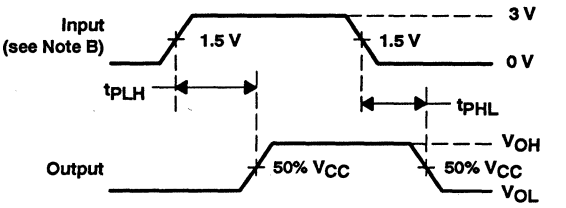
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	37	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

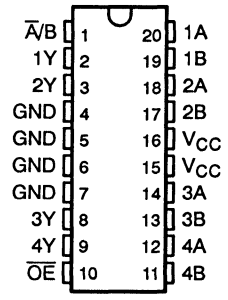
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D2957, JULY 1989 – REVISED APRIL 1993

- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

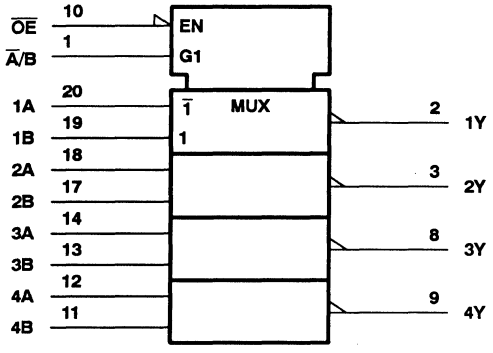
This data selector/multiplexer contains inverters and drivers to supply full data selection to the four output gates. A separate output-enable ($\overline{OE}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 74AC11158 provides true data.

The 74AC11158 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

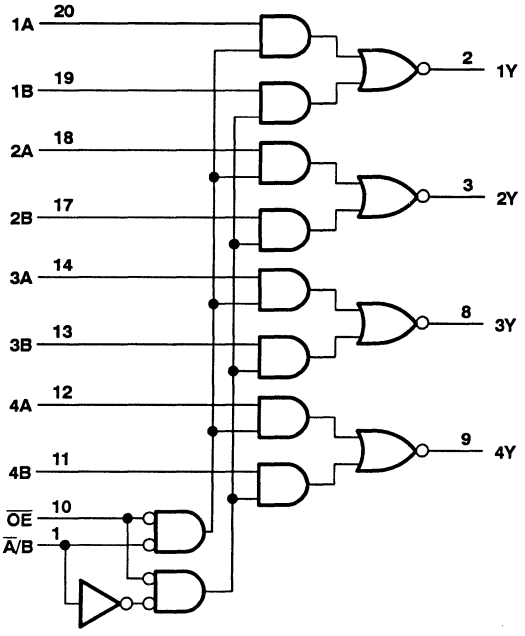
INPUTS				OUTPUT
$\overline{OE}$	A/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{A}$/B	0		5	ns/V
		Except $\overline{A}$/B	0		10	
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5.8	8.3	1.5	9	ns
t_{PHL}			1.5	5.9	8.6	1.5	9.4	
t_{PLH}	$\overline{A}$/B	Y	1.5	6.5	9	1.5	9.8	ns
t_{PHL}			1.5	6.8	9.4	1.5	10.3	
t_{PLH}	$\overline{OE}$	Y	1.5	5.7	8.1	1.5	9	ns
t_{PHL}			1.5	6.3	8.8	1.5	9.7	

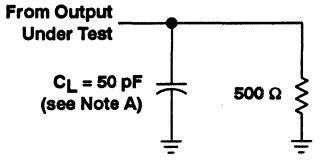
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	3.6	6.4	1.5	6.8	ns
t_{PHL}			1.5	3.9	6.6	1.5	7.4	
t_{PLH}	$\overline{A}$/B	Y	1.5	4.1	6.9	1.5	7.4	ns
t_{PHL}			1.5	4.9	7.2	1.5	7.9	
t_{PLH}	$\overline{OE}$	Y	1.5	3.7	6.4	1.5	6.9	ns
t_{PHL}			1.5	4.2	6.9	1.5	7.5	

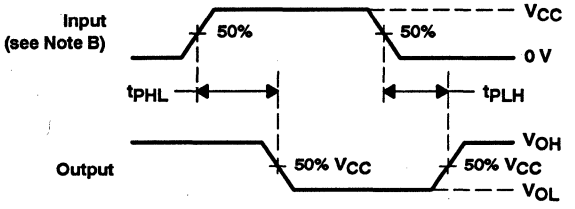
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	33	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

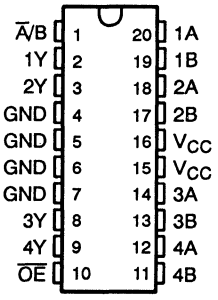
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS181 – D3979, JANUARY 1992 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

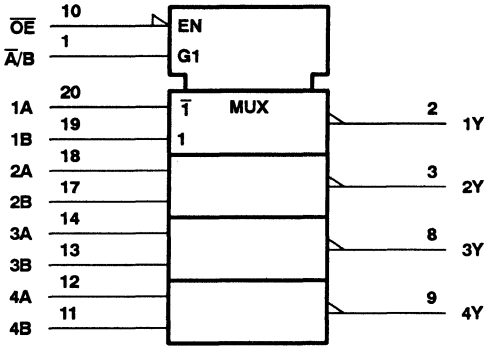
This data selector/multiplexer contains inverters and drivers to supply full data selection to the four output gates. A separate output-enable ($\overline{OE}$) input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 74ACT11158 provides inverted data.

The 74ACT11158 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

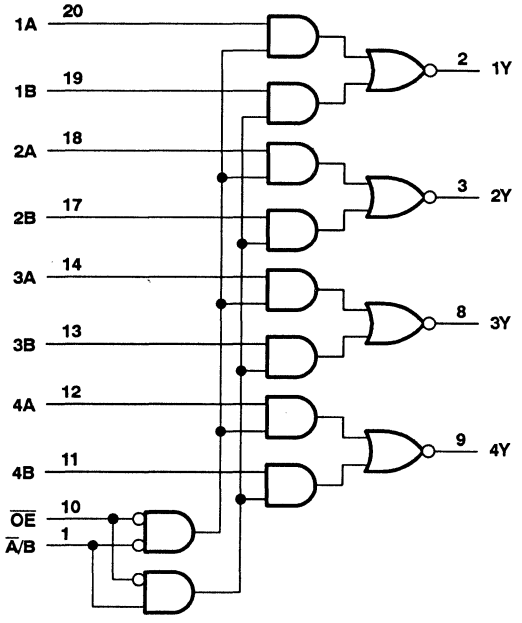
INPUTS				OUTPUT
$\overline{OE}$	A/B	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

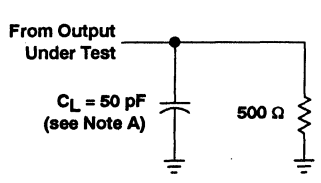
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2	5.1	7.6	2	8.4	ns
t_{PHL}			2.7	5.9	8.3	2.7	9.4	
t_{PLH}	A/B	Y	2.3	5.3	7.7	2.3	8.5	ns
t_{PHL}			2.9	6.7	9.8	2.9	10.8	
t_{PLH}	$\overline{OE}$	Y	2.5	5.1	6.8	2.5	7.5	ns
t_{PHL}			2.5	6.1	8.9	2.5	10	

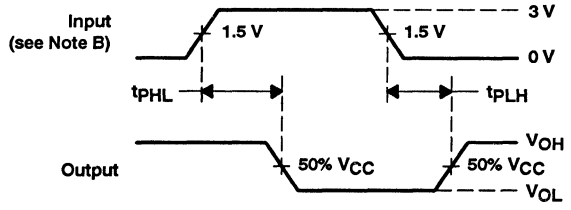
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	37	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

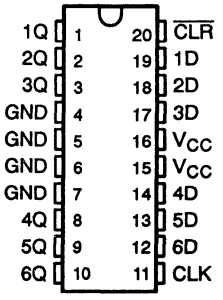
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3434, MARCH 1990 – REVISED APRIL 1993

- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This device contains six D-type flip-flops and is positive-edge-triggered with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

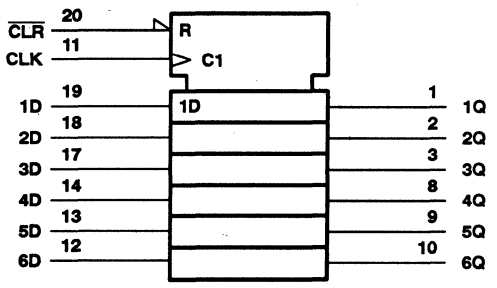
The 74AC11174 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_O

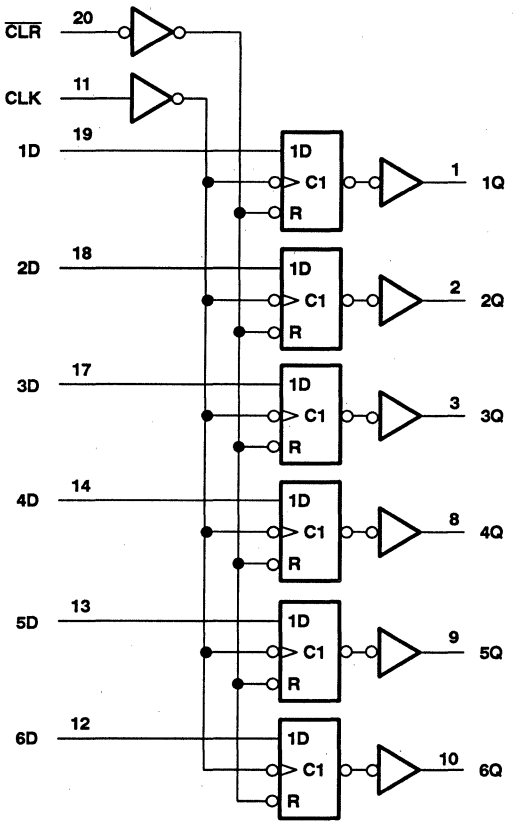
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	80	0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4.5		4.5		ns
		CLK high or low	6		6		
t_{su}	Setup time before CLK↑	Data	7		7		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time after CLK↑		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		ns
		CLK high or low	5		5		
t_{su}	Setup time before CLK↑	Data	4.5		4.5		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time after CLK↑		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			80	105		80		MHz
t_{PHL}	$\overline{CLR}$	Any Q	3.9	10	13.5	3.9	14.8	ns
t_{PLH}	CLK	Any Q	2.4	7.5	9.2	2.4	10.8	ns
t_{PHL}			3.4	9.6	12.7	3.4	14	

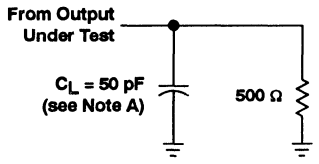
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	125		100		MHz
t_{PHL}	$\overline{CLR}$	Any Q	2.9	6.5	9.8	2.9	10.7	ns
t_{PLH}	CLK	Any Q	2.1	4.9	6.8	2.1	7.6	ns
t_{PHL}			2.7	6.2	9.2	2.7	10.1	

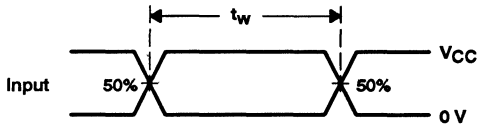
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	29	pF

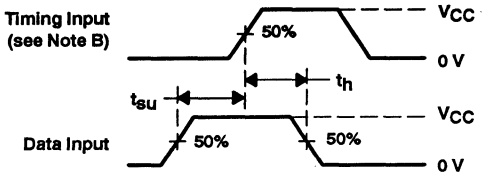
PARAMETER MEASUREMENT INFORMATION



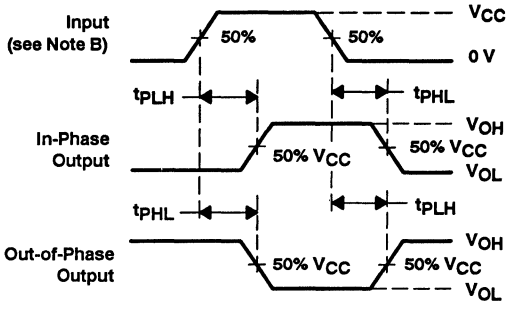
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

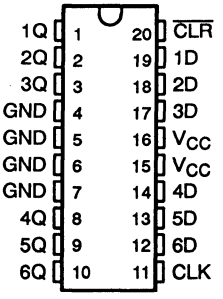
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS145 – D3435, MARCH 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Fully-Buffered Outputs for Maximum Isolation From External Disturbances**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This device contains six D-type flip-flops and is positive-edge-triggered with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

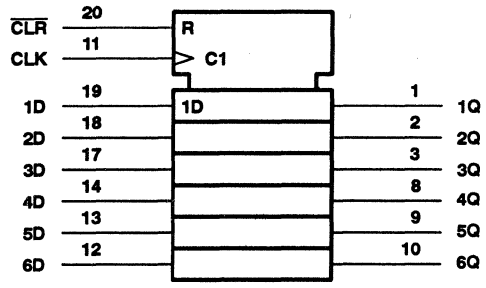
The 74ACT11174 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

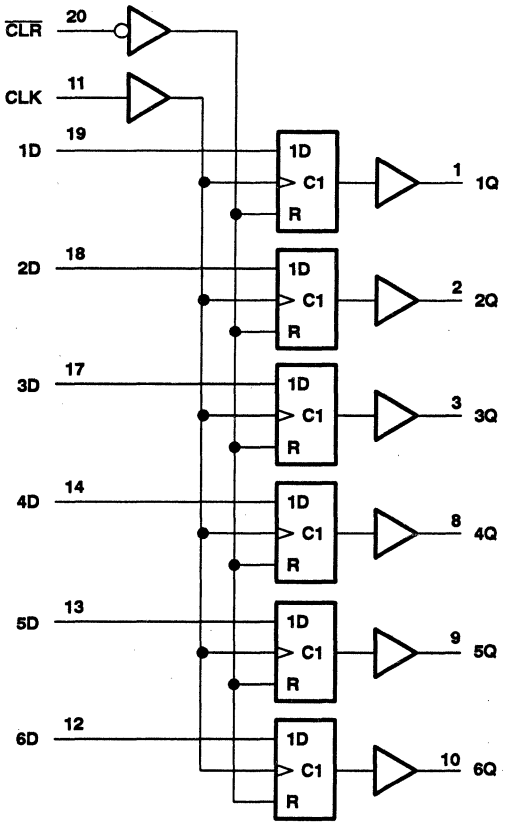
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	110	0	110	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		ns
		CLK high or low	4.5		4.5		
t_{su}	Setup time before CLK↑	Data	4		4		ns
		$\overline{CLR}$ inactive	1		1		
t_h	Hold time after CLK↑		0.5		0.5		ns

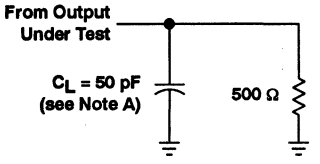
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			110	135		110		MHz
t_{PHL}	$\overline{CLR}$	Any Q	3.4	7.5	11.4	3.4	12.6	ns
t_{PLH}	CLK	Any Q	3.1	5.8	7.9	3.1	8.7	ns
t_{PHL}			3.7	7.2	9.9	3.7	11	

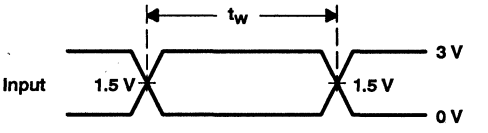
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	30	pF

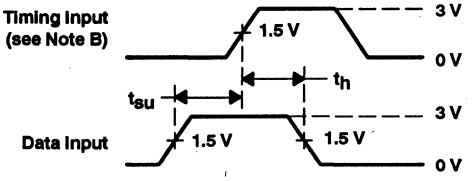
PARAMETER MEASUREMENT INFORMATION



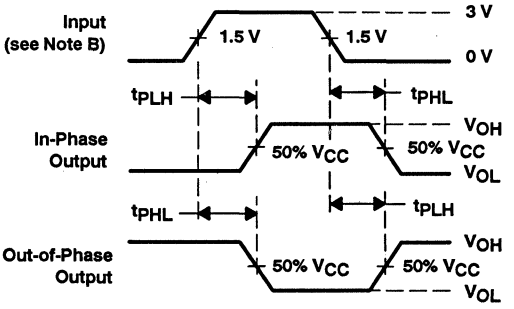
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



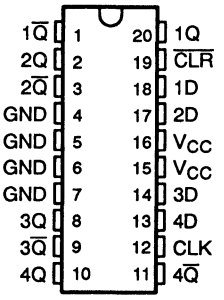
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

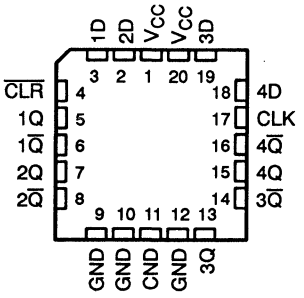
Figure 1. Load Circuit and Voltage Waveforms

- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11175 . . . J PACKAGE
74AC11175 . . . DW or N PACKAGE
(TOP VIEW)



54AC11014 . . . FK PACKAGE
(TOP VIEW)



description

These positive-edge-triggered flipflops implement D-type flip-flop logic with a direct clear input. Information at the D inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

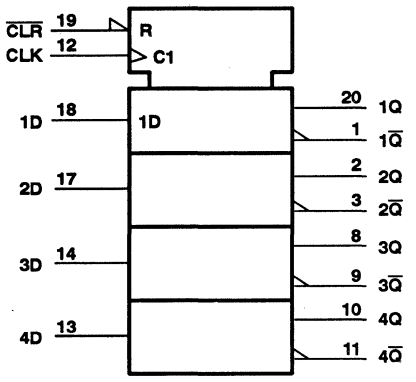
The 54AC11175 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11175 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

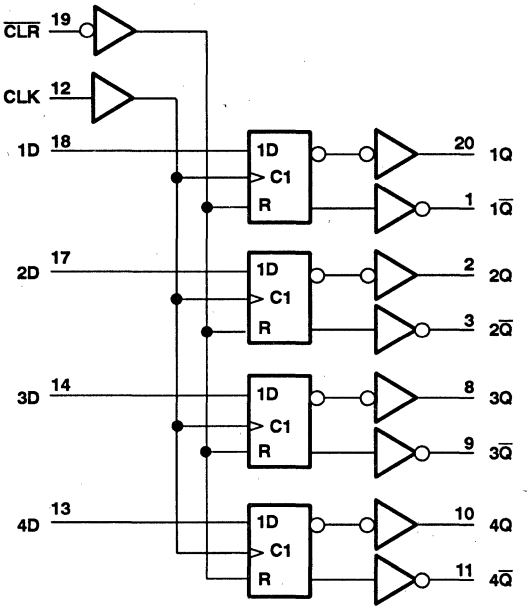
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11175			74AC11175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		VCC = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5.5		5.5		5.5		ns
		CLK high or low	5.5		5.5		5.5		
t_{su}	Setup time before CLK↑	Data	8		8		8		ns
		$\overline{CLR}$ inactive	8		8		8		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11175		74AC11175		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		4		ns
		CLK high or low	4		4		4		
t_{su}	Setup time before CLK↑	Data	5.5		5.5		5.5		ns
		$\overline{CLR}$ inactive	5.5		5.5		5.5		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90	120		90		90		MHz
t_{PLH}	$\overline{CLR}$	Any Q	2.6	7	8.7	2.6	9.9	2.6	9.3	ns
		Any $\overline{Q}$	2.6	7	8.7	2.6	9.9	2.6	9.3	
t_{PHL}	$\overline{CLR}$	Any Q	2.5	10	11.6	2.5	13	2.5	12.4	ns
		Any $\overline{Q}$	2.5	10	11.6	2.5	13	2.5	12.4	
t_{PLH}	CLK	Any Q	2.4	6.8	8.7	2.4	9.4	2.4	9.1	ns
		Any $\overline{Q}$	2.4	6.8	8.7	2.4	9.4	2.4	9.1	
t_{PHL}	CLK	Any Q	1.7	9.4	11.7	1.7	13	1.7	12.5	ns
		Any $\overline{Q}$	1.7	9.4	11.7	1.7	13	1.7	12.5	

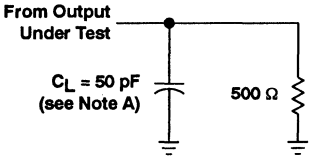
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11175		74AC11175		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125	150		125		125		MHz
t_{PLH}	$\overline{CLR}$	Any Q	2.2	4.5	6.3	2.2	7.1	2.2	6.8	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.1	2.2	6.8	
t_{PHL}	$\overline{CLR}$	Any Q	2.4	6.7	8.5	2.4	9.7	2.4	9.3	ns
		Any $\overline{Q}$	2.4	6.7	8.5	2.4	9.7	2.4	9.3	
t_{PLH}	CLK	Any Q	2.2	4.5	6.3	2.2	7.2	2.2	6.9	ns
		Any $\overline{Q}$	2.2	4.5	6.3	2.2	7.2	2.2	6.9	
t_{PHL}	CLK	Any Q	1.9	6.4	8.5	1.9	9.7	1.9	9.3	ns
		Any $\overline{Q}$	1.9	6.4	8.5	1.9	9.7	1.9	9.3	

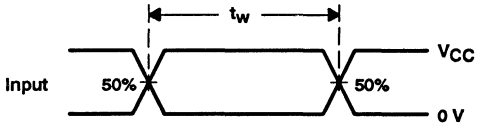
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	48	pF

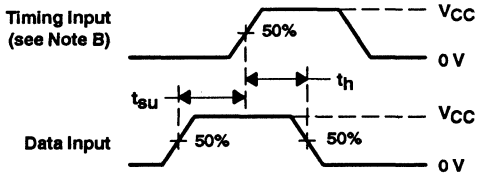
PARAMETER MEASUREMENT INFORMATION



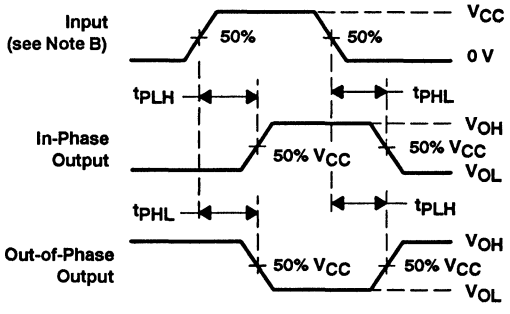
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

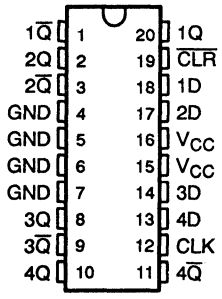
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS089 – D3385, DECEMBER 1989 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Fully-Buffered Outputs for Maximum Isolation From External Disturbances**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This device contains six D-type flip-flops and is positive-edge-triggered with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

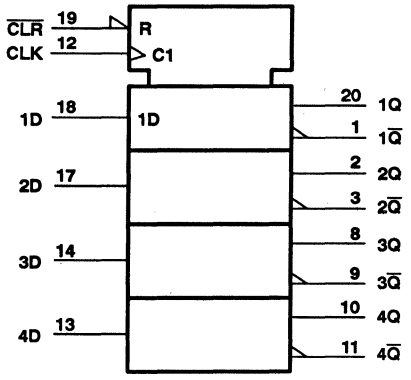
The 74AC11175 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

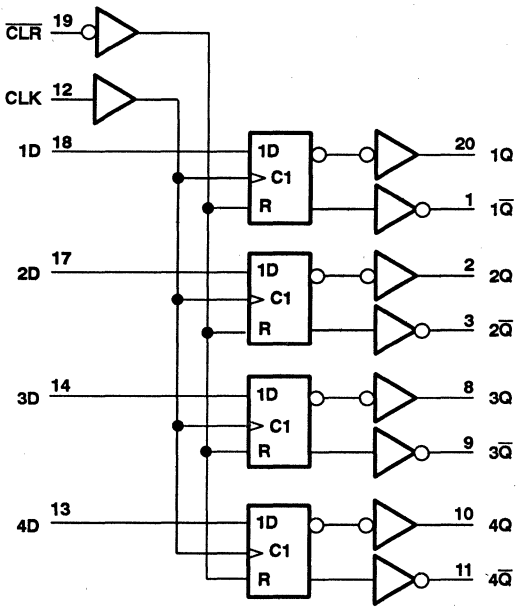
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	5		5		
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{CLR}$ inactive	5		5		
t_h	Hold time, data after CLK↑		0.5		0.5		ns

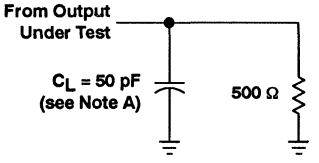
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	130		100		MHz
t_{PLH}	$\overline{CLR}$	Any Q	2.5	5.4	7.4	2.5	8.1	ns
		Any $\overline{Q}$	2.5	5.4	7.4	2.5	8.1	
t_{PHL}	$\overline{CLR}$	Any Q	3.1	7.6	9.9	3.1	10.9	ns
		Any $\overline{Q}$	3.1	7.6	9.9	3.1	10.9	
t_{PLH}	CLK	Any Q	3	5.3	6.9	3	7.5	ns
		Any $\overline{Q}$	3	5.3	6.9	3	7.5	
t_{PHL}	CLK	Any Q	3.3	7.2	9.2	3.3	10.1	ns
		Any $\overline{Q}$	3.3	7.2	9.2	3.3	10.1	

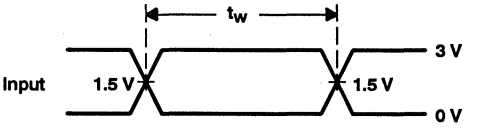
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	42	pF

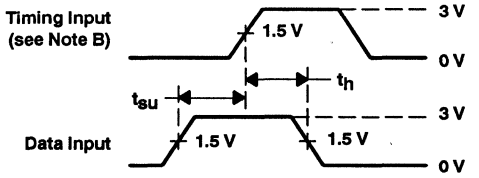
PARAMETER MEASUREMENT INFORMATION



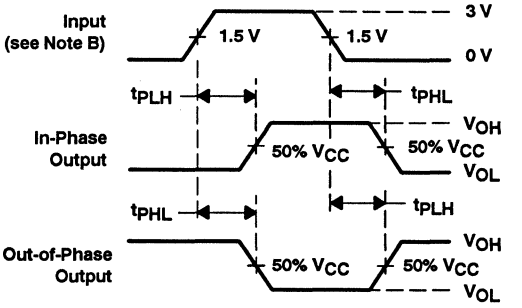
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



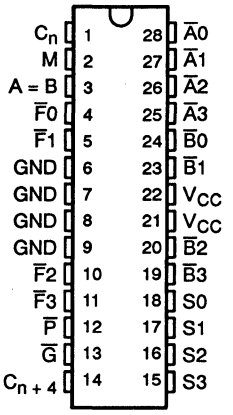
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

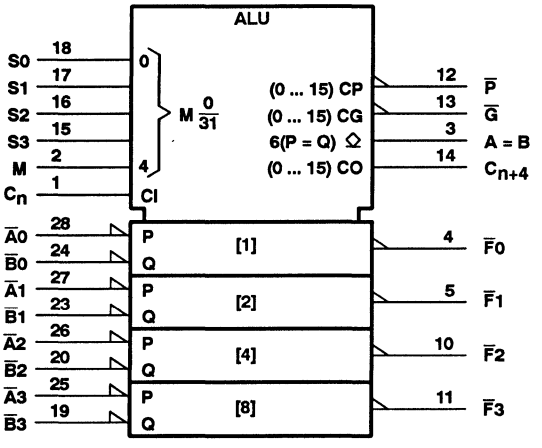
Figure 1. Load Circuit and Voltage Waveforms

- Inputs Are TTL-Voltage Compatible
- New Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Full Look Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR

DW PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

description

The 74ACT11181 is an arithmetic logic unit (ALU)/function generator that has a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs $\overline{G}$ and $\overline{P}$ for the four bits in the package. When used in conjunction with the 'ACT11882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading 'ACT11882 circuits with these ALUs to provide multilevel full-carry look-ahead operation is illustrated under signal designations.

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 74ACT11181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PACKAGE	PIN NUMBERS AND DESIGNATIONS															
DW, JT, or NT	25	26	27	28	19	20	23	24	11	10	5	4	1	14	12	13
FK	4	5	6	7	26	27	2	3	18	17	12	11	8	2	19	20
Active-low data (Table 1)	$\overline{A}3$	$\overline{A}2$	$\overline{A}1$	$\overline{A}0$	$\overline{B}3$	$\overline{B}2$	$\overline{B}1$	$\overline{B}0$	$\overline{F}3$	$\overline{F}2$	$\overline{F}1$	$\overline{F}0$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A3	A2	A1	A0	B3	B2	B1	B0	F3	F2	F1	F0	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A – B – 1, which requires an end-around or forced carry to provide A – B.

The 74ACT11181 can also be used as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). When performing this comparison, the ALU must be in the subtract mode with C_n = H. The A = B output is open drain so that it can be wired-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed not only to incorporate all of the designer's requirements for arithmetic operation but also to provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected using the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

signal designations

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output data is active low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and should be used with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 74ACT11181 and 'ACT11881 together with the 'ACT11882 can be used with the signal designations of either Figure 1 or Figure 2.

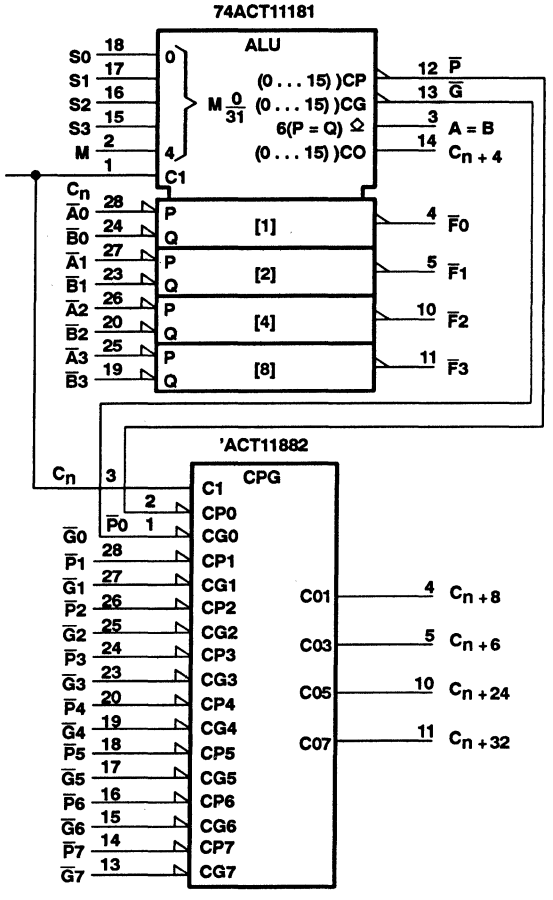


Figure 1
(use with Table 1)

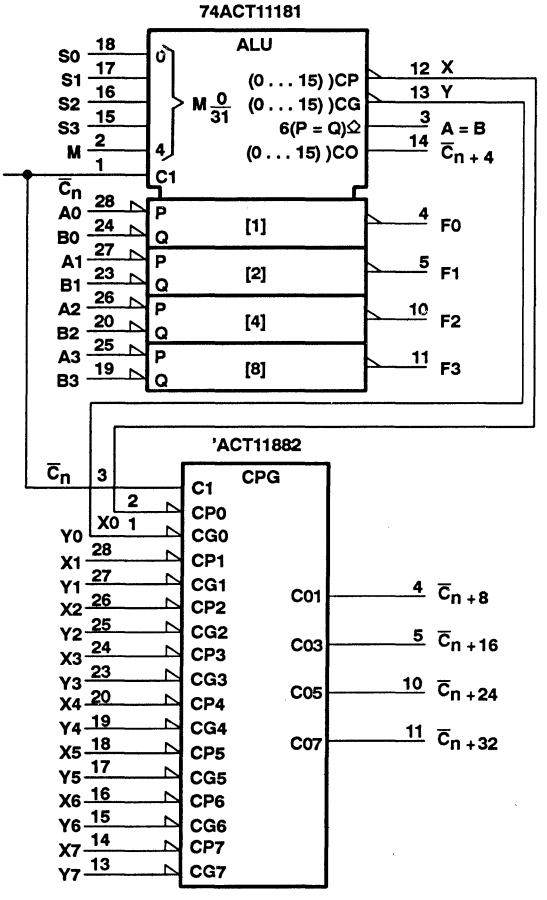


Figure 2
(use with Table 2)

Table 1

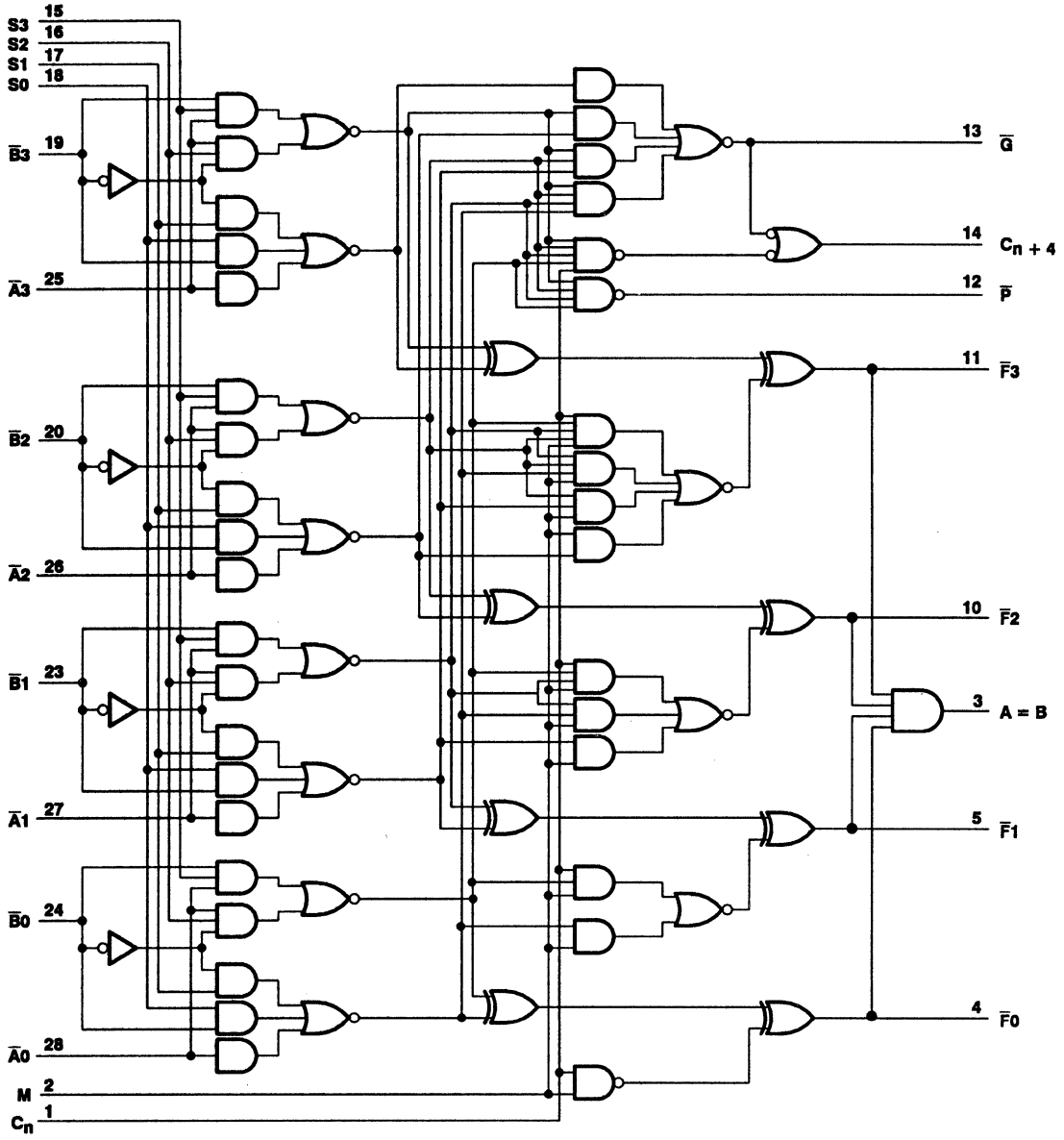
SELECTION				ACTIVE-LOW DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

Table 2

SELECTION				ACTIVE-HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A†	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

† Each bit is shifted to the next more significant position.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	All outputs except A = B		−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	Any output except A = B	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −50 mA‡	5.5 V						
		I_{OH} = −75 mA‡	5.5 V				3.85		
I_{OH}	A = B	V_{CC} = 5.5 V, V_O = V_{CC}	5.5 V			0.5		5	μA
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 50 mA‡	5.5 V						
		I_{OL} = 75 mA‡	5.5 V					1.65	
I_I		V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i		V_I = V_{CC} or GND	5 V		4.5				pF
C_o	A = B	V_O = V_{CC} or GND	5 V		11				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

addition mode; M = S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	C_n	C_{n+4}	1.5	10.7	17.5	1.5	18.6	ns
t_{PHL}			1.5	11.3	16.2	1.5	18.3	
t_{PLH}	Any $\overline{A}$	C_{n+4}	1.5	12.7	20.3	1.5	21.8	ns
t_{PHL}			1.5	14	19.7	1.5	22	
t_{PLH}	Any $\overline{B}$	C_{n+4}	1.5	13.5	21.6	1.5	23.2	ns
t_{PHL}			1.5	13.6	19.7	1.5	22	
t_{PLH}	C_n	Any $\overline{F}$	1.5	11.2	17.1	1.5	18.7	ns
t_{PHL}			1.5	9.9	15.9	1.5	17.4	
t_{PLH}	Any $\overline{A}$	$\overline{G}$	1.5	12.8	20.9	1.5	23.3	ns
t_{PHL}			1.5	12.7	17.8	1.5	20.9	
t_{PLH}	Any $\overline{B}$	$\overline{G}$	1.5	12.7	20.6	1.5	22.1	ns
t_{PHL}			1.5	14.3	19.2	1.5	21.3	
t_{PLH}	Any $\overline{A}$	$\overline{P}$	1.5	11.4	18.4	1.5	19.6	ns
t_{PHL}			1.5	9.6	16.6	1.5	17.4	
t_{PLH}	Any $\overline{B}$	$\overline{P}$	1.5	11.3	18.2	1.5	19.3	ns
t_{PHL}			1.5	10.6	15.6	1.5	16.6	
t_{PLH}	$\overline{A}i$	$\overline{F}i$	1.5	11.8	17.7	1.5	19.5	ns
t_{PHL}			1.5	11	17.7	1.5	18.7	
t_{PLH}	$\overline{B}i$	$\overline{F}i$	1.5	11.6	17.3	1.5	19.1	ns
t_{PHL}			1.5	12	19.4	1.5	20.6	
t_{PLH}	$\overline{A}i$	Any $\overline{F}$ except $\overline{F}i$	1.5	13	18.9	1.5	21	ns
t_{PHL}			1.5	12.4	18.8	1.5	20.2	
t_{PLH}	Any $\overline{B}$	Any $\overline{F}$ except $\overline{F}i$	1.5	13.1	18.7	1.5	21	ns
t_{PHL}			1.5	13.5	19.8	1.5	21.3	

mode switching; S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	M	Any $\overline{F}$	1.5	9.5	15	1.5	16.3	ns
t_{PHL}			1.5	10.6	16.4	1.5	17.5	
t_{PLH}	M	A = B	1.5	15.7	19.3	1.5	20.1	ns
t_{PHL}			1.5	14	18.7	1.5	21.8	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

subtraction mode; M = S0 = S3 = 0 V, S1 = S2 = 4.5 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	C_n	C_{n+4}	1.5	10.7	17.5	1.5	18.6	ns
t_{PHL}			1.5	11.3	16.2	1.5	18.3	
t_{PLH}	Any $\overline{A}$	C_{n+4}	1.5	12.7	20.3	1.5	21.8	ns
t_{PHL}			1.5	13.5	19.7	1.5	20.8	
t_{PLH}	Any $\overline{B}$	C_{n+4}	1.5	13.8	21.1	1.5	22.7	ns
t_{PHL}			1.5	14.8	20.7	1.5	23	
t_{PLH}	C_n	Any $\overline{F}$	1.5	11.2	17.1	1.5	18.7	ns
t_{PHL}			1.5	9.9	15.9	1.5	17.4	
t_{PLH}	Any $\overline{A}$	$\overline{G}$	1.5	12.8	20.8	1.5	22.2	ns
t_{PHL}			1.5	12.7	18.4	1.5	20.7	
t_{PLH}	Any $\overline{B}$	$\overline{G}$	1.5	13.2	20.8	1.5	21.6	ns
t_{PHL}			1.5	11.5	18.5	1.5	19.6	
t_{PLH}	Any $\overline{A}$	$\overline{P}$	1.5	9.6	14.6	1.5	15.5	ns
t_{PHL}			1.5	10.8	18.8	1.5	20	
t_{PLH}	Any $\overline{B}$	$\overline{P}$	1.5	10.4	15.1	1.5	16.3	ns
t_{PHL}			1.5	11.9	17.8	1.5	19.6	
t_{PLH}	$\overline{A}i$	$\overline{F}i$	1.5	11.2	17.2	1.5	19.9	ns
t_{PHL}			1.5	12.1	17.8	1.5	19.5	
t_{PLH}	$\overline{B}i$	$\overline{F}i$	1.5	12	18.6	1.5	20.7	ns
t_{PHL}			1.5	13.2	19	1.5	21.1	
t_{PLH}	Any $\overline{A}$	Any $\overline{F}$	1.5	12.6	18.9	1.5	20.3	ns
t_{PHL}			1.5	13.6	19.4	1.5	21.5	
t_{PLH}	Any $\overline{B}$	Any $\overline{F}$	1.5	13.1	18.7	1.5	20.4	ns
t_{PHL}			1.5	18	21.6	1.5	23.7	
t_{PLH}	Any $\overline{A}$	A = B	1.5	16	21.5	1.5	24.6	ns
t_{PHL}			1.5	18.5	22.7	1.5	23.9	
t_{PLH}	Any $\overline{B}$	A = B	1.5	18.5	22.7	1.5	23.9	ns
t_{PHL}			1.5	16.5	22	1.5	25.4	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

logic and arithmetic modes

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	Any $\overline{A}$	Any $\overline{F}$	M = 4.5 V (logic mode)	1.5	10	15.9	1.5	18.3	ns
t_{PHL}				1.5	11	17.4	1.5	19.6	
t_{PLH}	$\overline{Bi}$	$\overline{Fi}$	M = 4.5 V (logic mode)	1.5	12.2	18	1.5	19.6	ns
t_{PHL}				1.5	11.5	18.3	1.5	19.6	
t_{PLH}	Any S	Any $\overline{F}$	M = 0 V (arithmetic mode)	1.5	12.1	18.3	1.5	20.1	ns
t_{PHL}				1.5	10.6	15.8	1.5	17.4	
t_{PLH}	Any S	A = B	M = 0 V (arithmetic mode)	1.5	18.7	22.1	1.5	23.4	ns
t_{PHL}				1.5	17.2	22.2	1.5	25.4	
t_{PLH}	Any S	C_{n+4}	M = 4.5 V (logic mode)	1.5	13.9	21.8	1.5	23.6	ns
t_{PHL}				1.5	15.3	22.3	1.5	25.2	
t_{PLH}	Any S	$\overline{G}$	M = 0 V (arithmetic mode)	1.5	12.7	20.5	1.5	22.3	ns
t_{PHL}				1.5	13.5	19.7	1.5	22	
t_{PLH}	Any S	$\overline{P}$	M = 4.5 V (logic mode)	1.5	12.4	18.6	1.5	20.5	ns
t_{PHL}				1.5	11.7	17.7	1.5	18	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	119	pF

PARAMETER MEASUREMENT INFORMATION

ADDITION MODE TEST TABLE

FUNCTION INPUTS: M = S1 = S2 = 0 V, S0 = S2 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	Ai	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase

MODE SWITCHING TEST TABLE

FUNCTION INPUTS: S1 = S2 = 0 V, S0 = S3 = 4.5 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}2$, $\overline{A}2$, C_n	Any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	M	—	—	Remaining $\overline{A}$ and $\overline{B}$	$\overline{B}1$, $\overline{A}1$, C_n	A = B	In-Phase

PARAMETER MEASUREMENT INFORMATION

SUBTRACTION MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

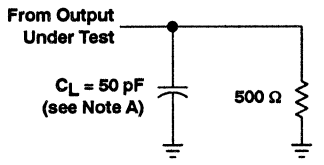
PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining B, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	None	$\overline{B}i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$ or any $\overline{F}$	In-Phase
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	None	$\overline{A}i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$	In-Phase

LOGIC MODE TEST TABLE

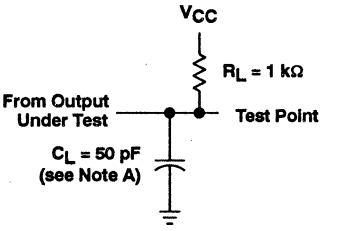
FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Figure 3)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}i$	$\overline{B}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase
t_{PLH} t_{PHL}	$\overline{B}i$	$\overline{A}i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}i$	Out-of-Phase

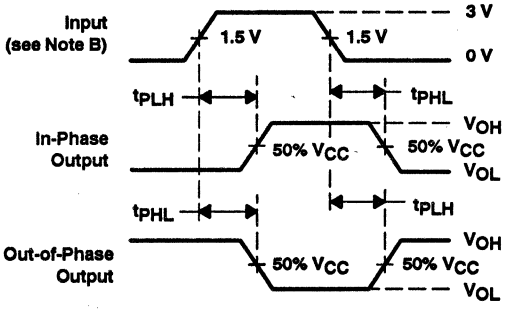
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT, TOTEM-POLE OUTPUTS



LOAD CIRCUIT, OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS

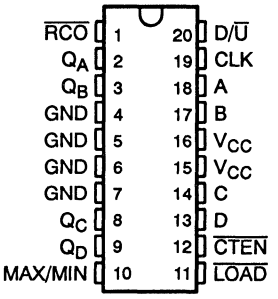
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

SCAS106A – D3455, FEBRUARY 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



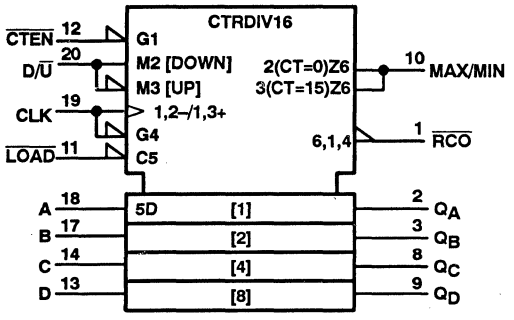
description

The 74ACT11191 is a synchronous, 4-bit binary reversible up/down counter. A synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

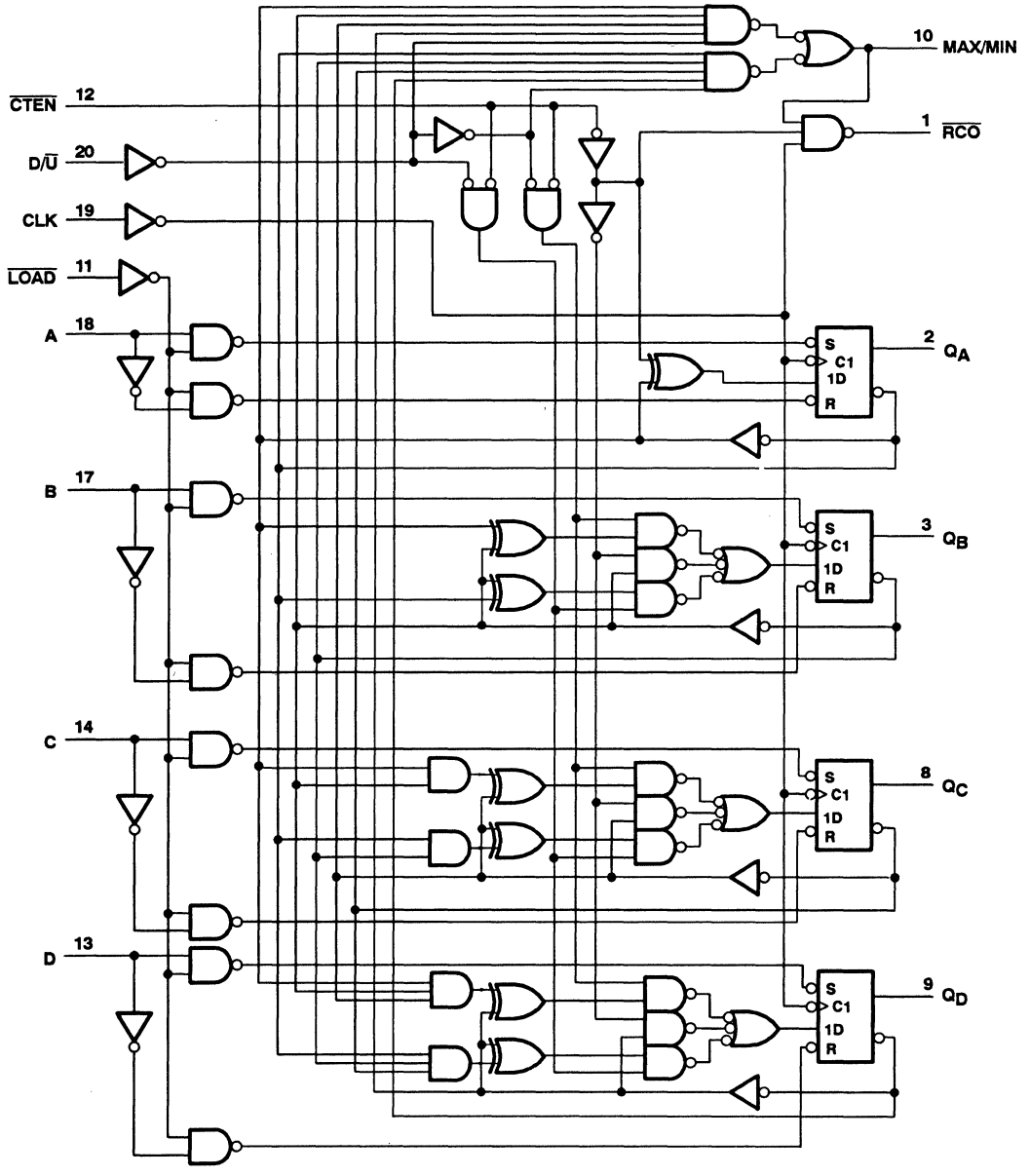
description (continued)

These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counter to be used as a modulo-N divider by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (15) counting up. The ripple clock output ($\overline{ROC}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counter can easily be cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The 74ACT11191 is characterized for operation from – 40°C to 85°C.

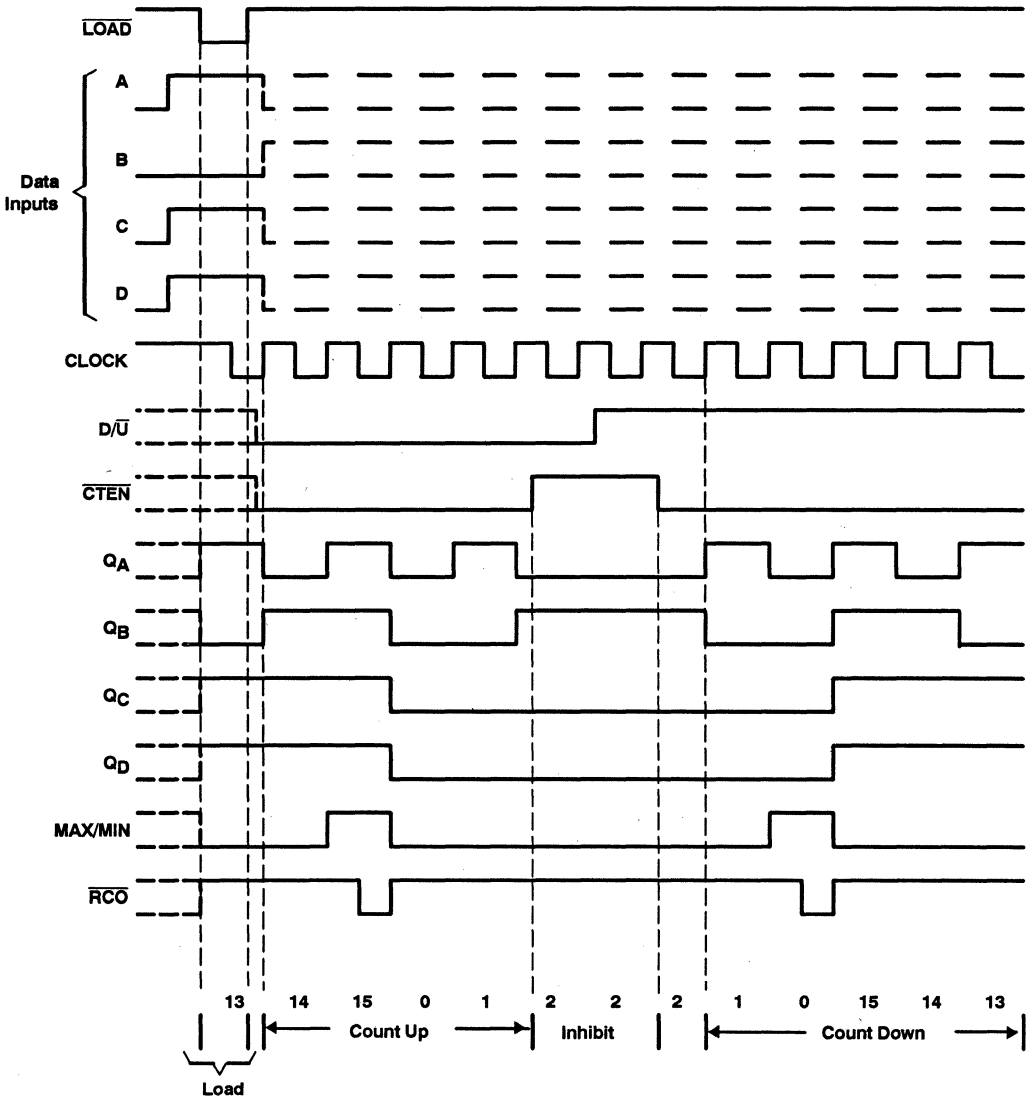
logic diagram (positive logic)



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage		2	V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	65	0	65	MHz
t_w	Pulse duration	$\overline{LOAD}$ low	4		4		ns
		CLK high or low	7.7		7.7		
t_{su}	Setup time	Data before $\overline{LOAD}$↓	3		3		ns
		$\overline{CTEN}$ before CLK↑	7.5		7.5		
		D/$\overline{U}$ before CLK↑	8.5		8.5		
		$\overline{LOAD}$ inactive before CLK↑	2		2		
t_h	Hold time	Data after $\overline{LOAD}$↓	2.5		2.5		ns
		$\overline{CTEN}$ after CLK↑	1.5		1.5		
		D/$\overline{U}$ after CLK↑	0.5		0.5		

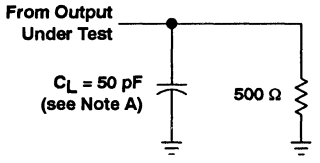
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			65	95		65		MHz
t_{PLH}	$\overline{LOAD}$	Any Q	4	7.6	10.8	4	12.2	ns
t_{PHL}			3.8	7.4	10.5	3.8	11.9	
t_{PLH}	$\overline{LOAD}$	MAX/MIN	5.2	9.7	13.9	5.2	15.8	ns
t_{PHL}			4.7	9.5	13.6	4.7	15.4	
t_{PLH}	$\overline{LOAD}$	$\overline{RCO}$	5.4	10.5	15.1	5.4	17.1	ns
t_{PHL}			5.8	11	15.7	5.8	17.9	
t_{PLH}	A, B, C, or D	Any Q	4.5	7.6	10.1	4.5	11.6	ns
t_{PHL}			3.7	7.1	10.3	3.7	11.7	
t_{PLH}	A, B, C, or D	MAX/MIN	5.1	9.5	13.6	5.1	15.4	ns
t_{PHL}			4.7	9.2	13.4	4.7	15.2	
t_{PLH}	A, B, C, or D	$\overline{RCO}$	5.5	10.3	14.8	5.5	17.2	ns
t_{PHL}			5.9	10.9	15.5	5.9	18	
t_{PLH}	CLK	$\overline{RCO}$	4.4	7.4	9.5	4.4	11	ns
t_{PHL}			3.5	6.7	9.5	3.5	10.8	
t_{PLH}	CLK	Any Q	3.6	6.7	9.2	3.6	10.4	ns
t_{PHL}			4.2	7.1	9.4	4.2	10.8	
t_{PLH}	CLK	MAX/MIN	5	8	10.3	5	11.7	ns
t_{PHL}			5.3	8.6	11.5	5.3	13.1	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	4.4	8.4	11.7	4.4	13.1	ns
t_{PHL}			4.2	8.8	11.3	4.2	13	
t_{PLH}	D/$\overline{U}$	MAX/MIN	3.2	6.9	9.6	3.2	11	ns
t_{PHL}			3.6	7.2	10.3	3.6	11.6	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	3.9	6.4	8.2	3.9	9.2	ns
t_{PHL}			2.8	6	8.4	2.8	9.5	

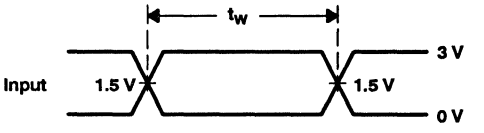
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	68	pF

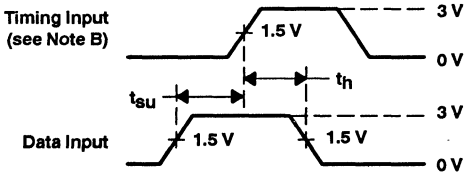
PARAMETER MEASUREMENT INFORMATION



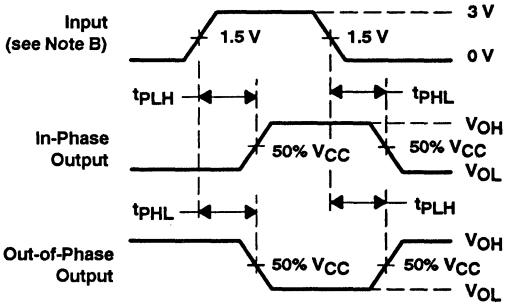
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

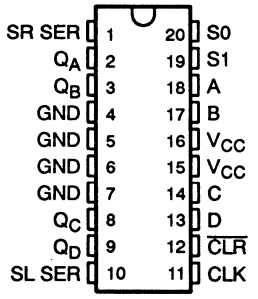
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3391, NOVEMBER 1989 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Left or Right Shifts**
- **Parallel Synchronous Loading**
- **Direct Overriding Clear**
- **Temporary Data Latching Capability**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This bidirectional shift register features parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clocking (do nothing).

Synchronous parallel loading is accomplished by applying the 4 bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode control inputs are low.

The 74ACT11194 is characterized for operation from – 40°C to 85°C.

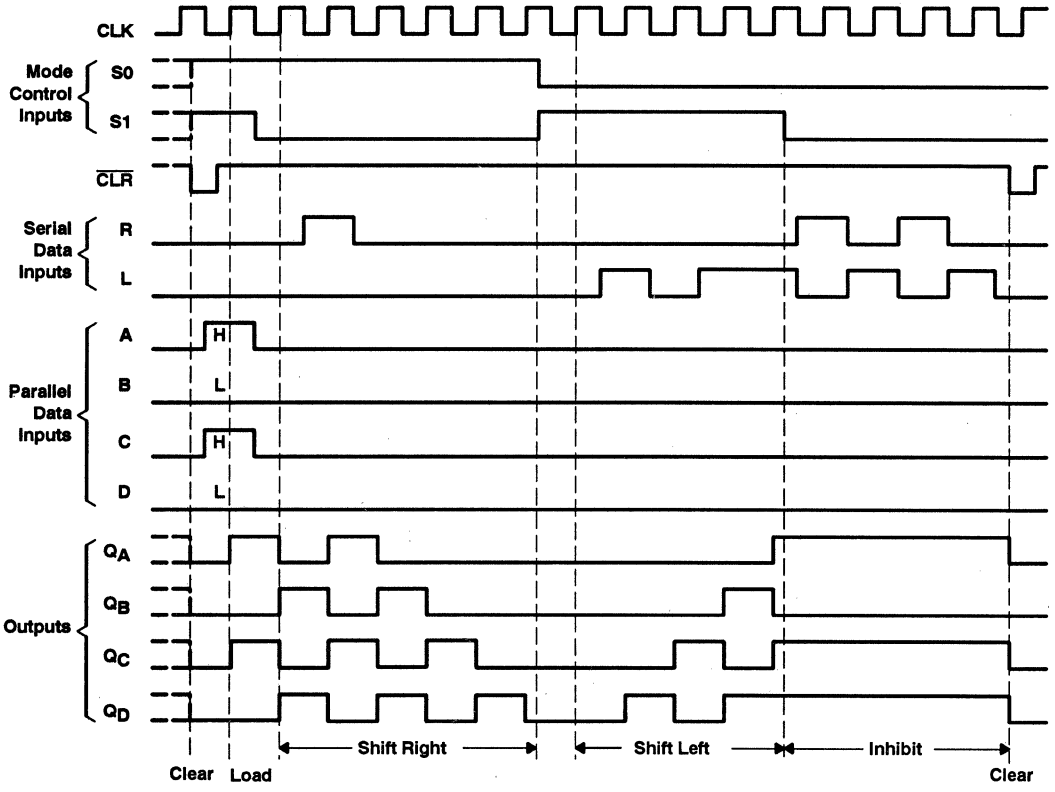
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

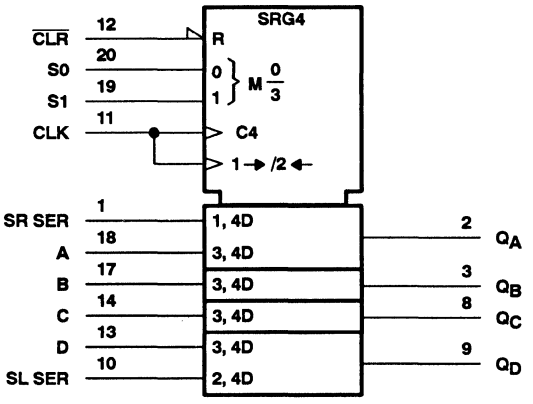
INPUTS										OUTPUTS			
$\overline{CLR}$	MODE		CLK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D respectively, before the most-recent ↑ transition of the clock.

timing clear, load, right-shift, inhibit, and clear sequences

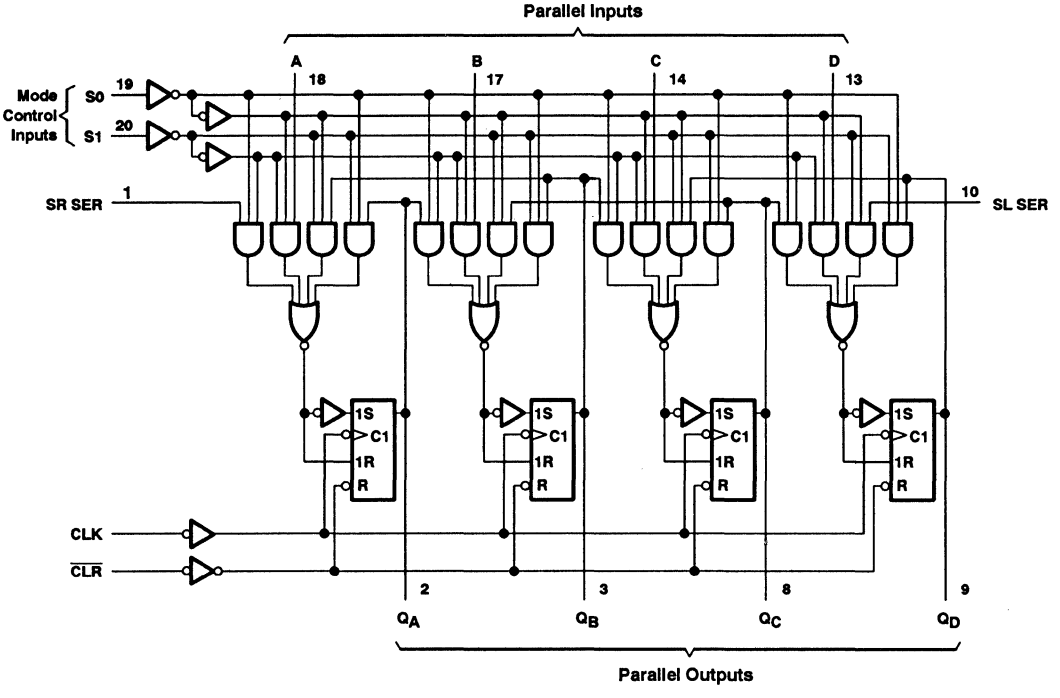


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high or low	5		5		ns
		$\overline{CLR}$ low	4.5		4.5		
t_{su}	Setup time before CLK ↑	Select	6		6		ns
		Data	4		4		
		$\overline{CLR}$ inactive	1		1		
t_h	Hold time after CLK ↑	Select	1.5		1.5		ns
		Data	1		1		

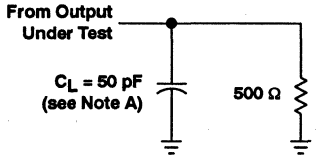
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	130		100		MHz
t_{PLH}	CLK	Any Q	2.2	5.8	6.9	2.2	7.7	ns
t_{PHL}			2.6	6.6	7.7	2.6	8.8	
t_{PLH}	$\overline{CLR}$	Any Q	2.9	7.1	9.1	2.9	10.3	ns

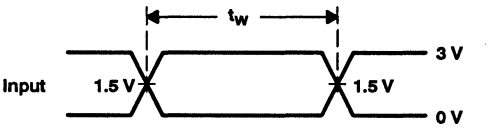
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	69	pF

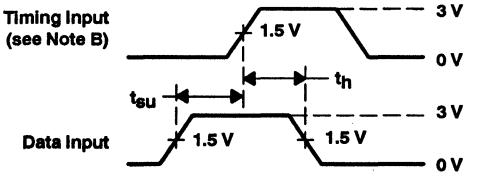
PARAMETER MEASUREMENT INFORMATION



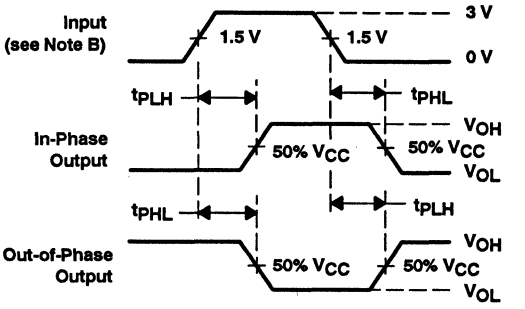
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

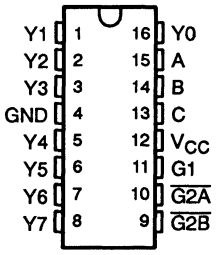
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

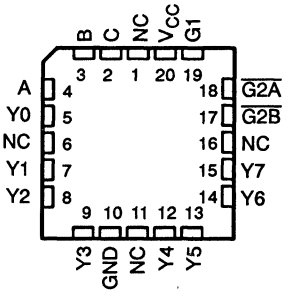
D3103, APRIL 1988 – REVISED APRIL 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Noninverting Version of 'AC11138**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11238 . . . J PACKAGE
74AC11238 . . . D OR N PACKAGE
(TOP VIEW)



54AC11238 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AC11238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

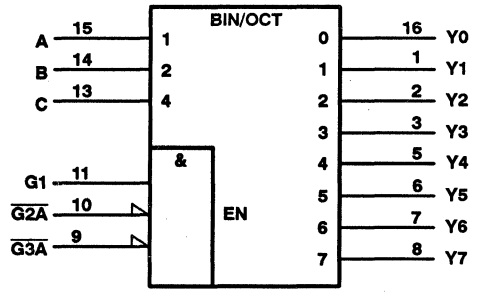
The 54AC11238 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11238 is characterized for operation from – 40°C to 85°C.

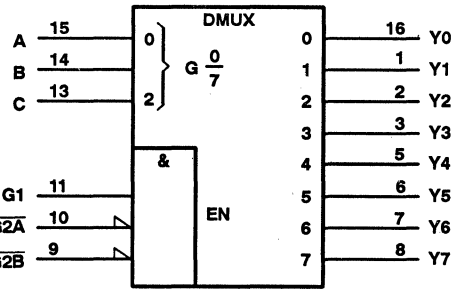
EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

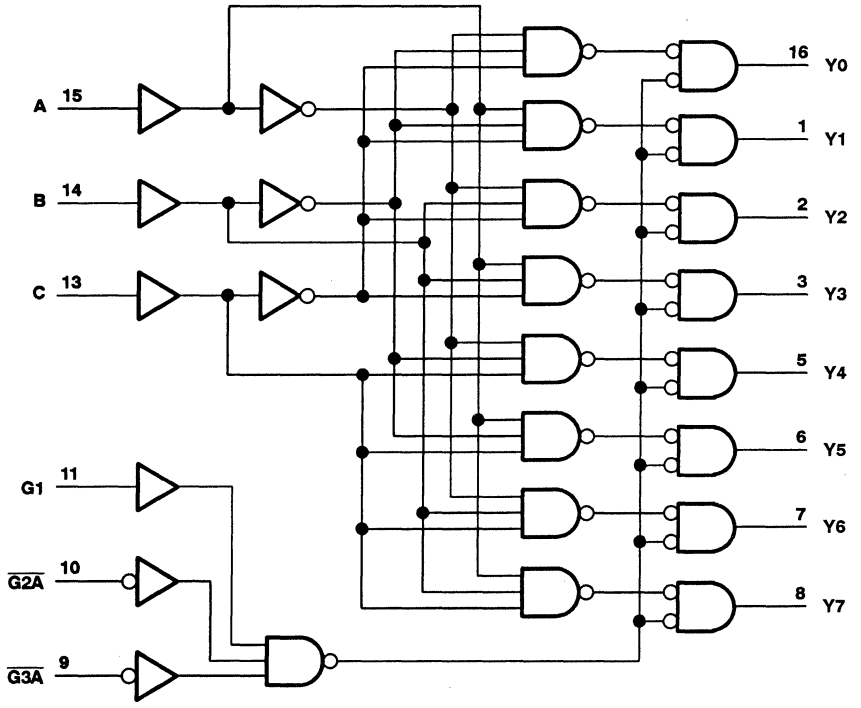
logic symbols (alternatives)†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11238			74AC11238			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	8.5	10.6	1.5	12.7	1.5	11.7	ns
t_{PHL}			1.5	9.6	11.9	1.5	14.3	1.5	13.3	
t_{PLH}	G1	Any Y	1.5	8.2	10.3	1.5	12.3	1.5	11.4	ns
t_{PHL}			1.5	9.6	11.7	1.5	14	1.5	13	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	1.5	9.1	11.2	1.5	13.4	1.5	12.5	ns
t_{PHL}			1.5	10.7	12.9	1.5	15.6	1.5	14.5	

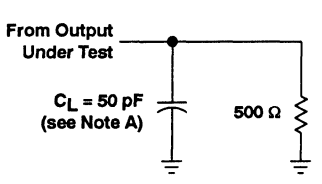
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11238		74AC11238		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	1.5	5.4	7.3	1.5	9	1.5	8.5	ns
t_{PHL}			1.5	6.3	8.6	1.5	10.9	1.5	10.2	
t_{PLH}	G1	Any Y	1.5	5.2	6.9	1.5	8.7	1.5	8.1	ns
t_{PHL}			1.5	6.5	8.5	1.5	10.6	1.5	9.9	
t_{PLH}	$\overline{G2A}$, $\overline{G2B}$	Any Y	1.5	5.6	7.5	1.5	9.6	1.5	8.9	ns
t_{PHL}			1.5	7.2	9.3	2.5	11.8	1.5	11	

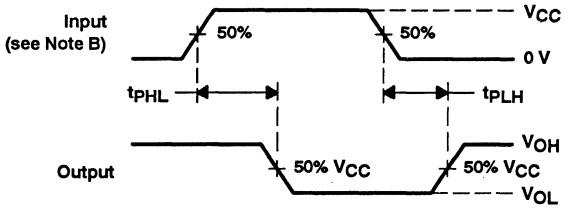
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	44	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

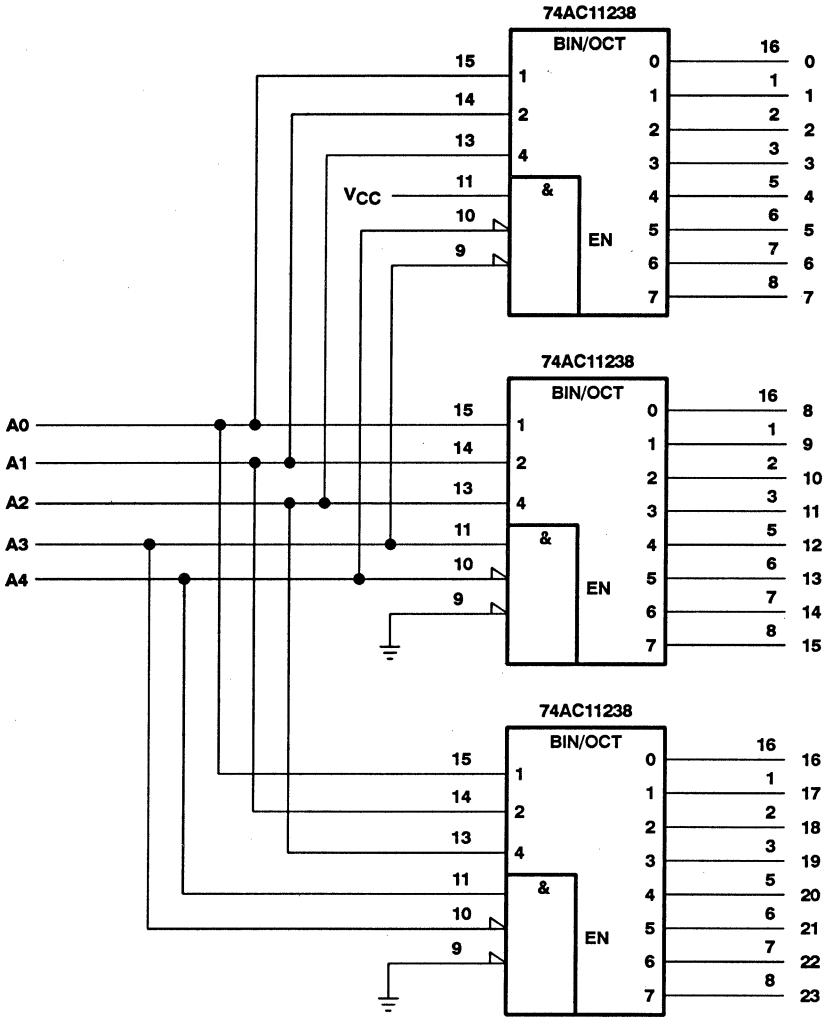


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

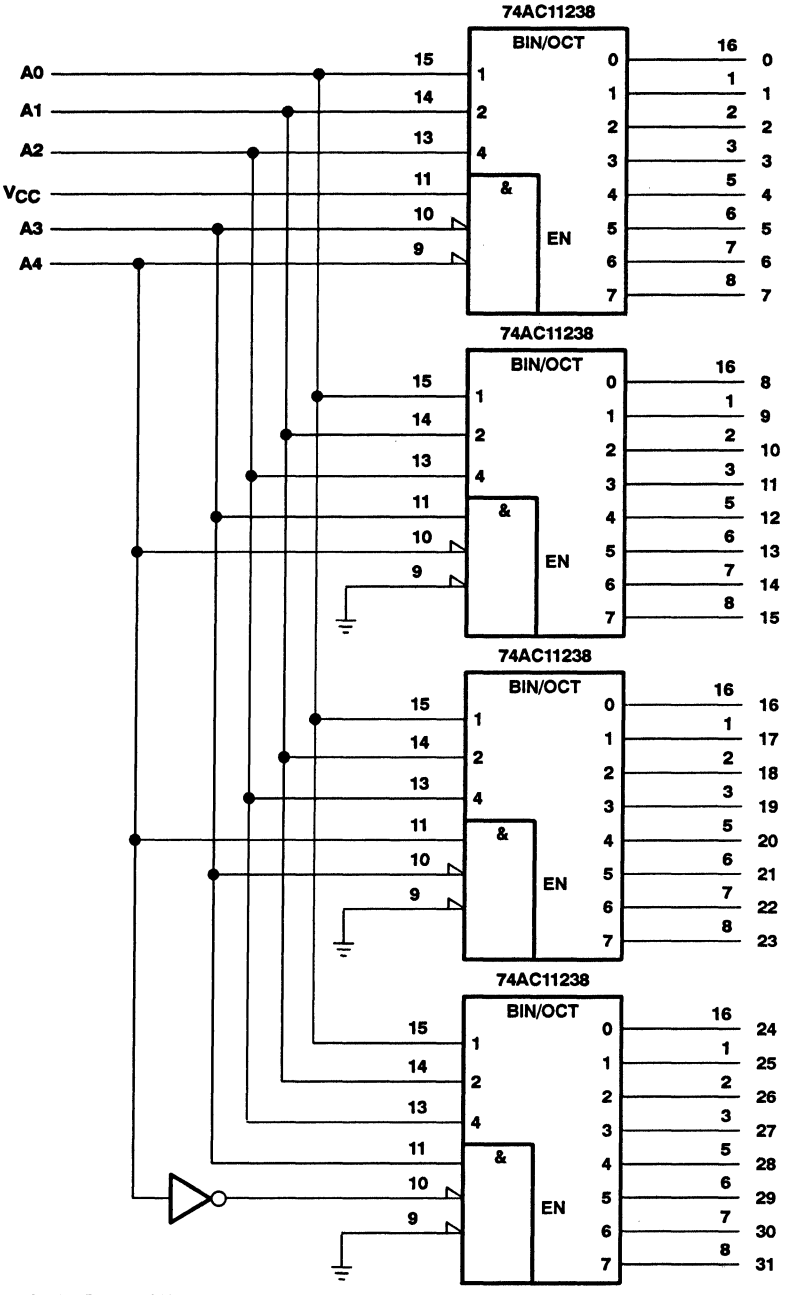
TYPICAL APPLICATION DATA



Pin numbers shown are for the D, J, and N packages.

Figure 2. 24-Bit Decoding Scheme

TYPICAL APPLICATION DATA



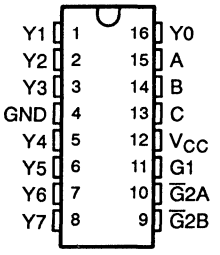
Pin numbers shown are for the D, J, and N packages.

Figure 3. 32-Bit Decoding Scheme

D3185, NOVEMBER 1988 – REVISED APRIL 1993

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Noninverting Version of 'ACT11138**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The 74ACT11238 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

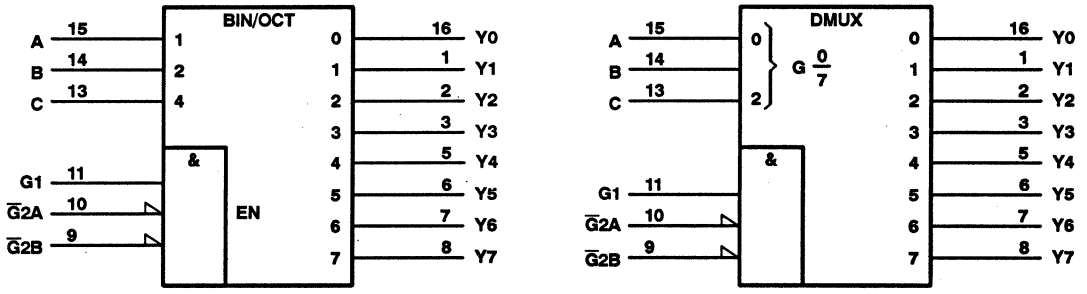
The 74ACT11238 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

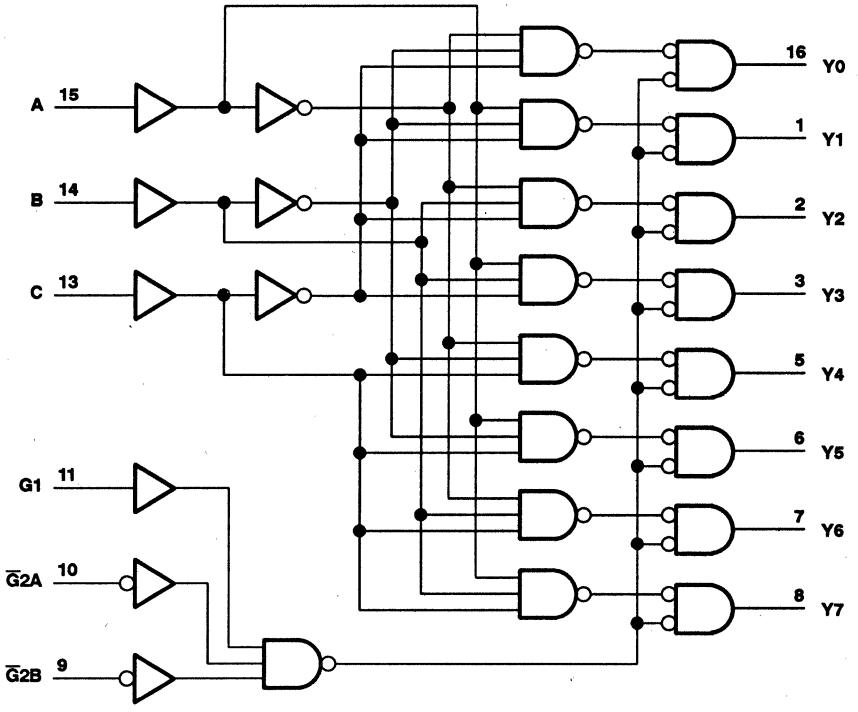
EPIC is a trademark of Texas Instruments Incorporated.

logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		NOM	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±0.1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	mA
ΔI_{CC}§	V_I = V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

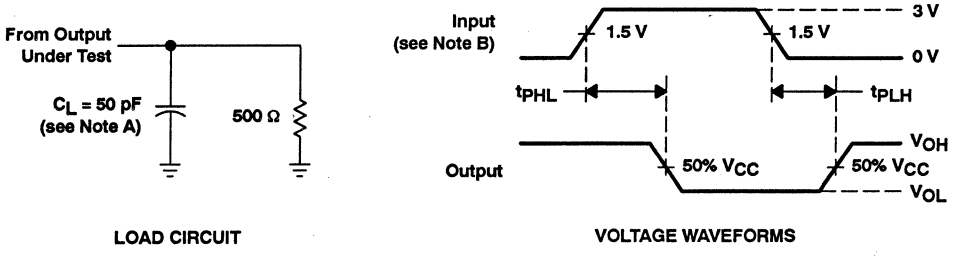
switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B or C	Y	1.5	5	8.6	1.5	9.6	ns
t_{PHL}			1.5	5.7	9.7	1.5	10.8	
t_{PLH}	G1	Y	1.5	6	8.4	1.5	9.4	ns
t_{PHL}			1.5	6.9	10.2	1.5	11.4	
t_{PLH}	$\overline{G}$2A, $\overline{G}$2B	Y	1.5	5.9	9	1.5	10.1	ns
t_{PHL}			1.5	7.8	10.7	1.5	12.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	57	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL APPLICATION DATA

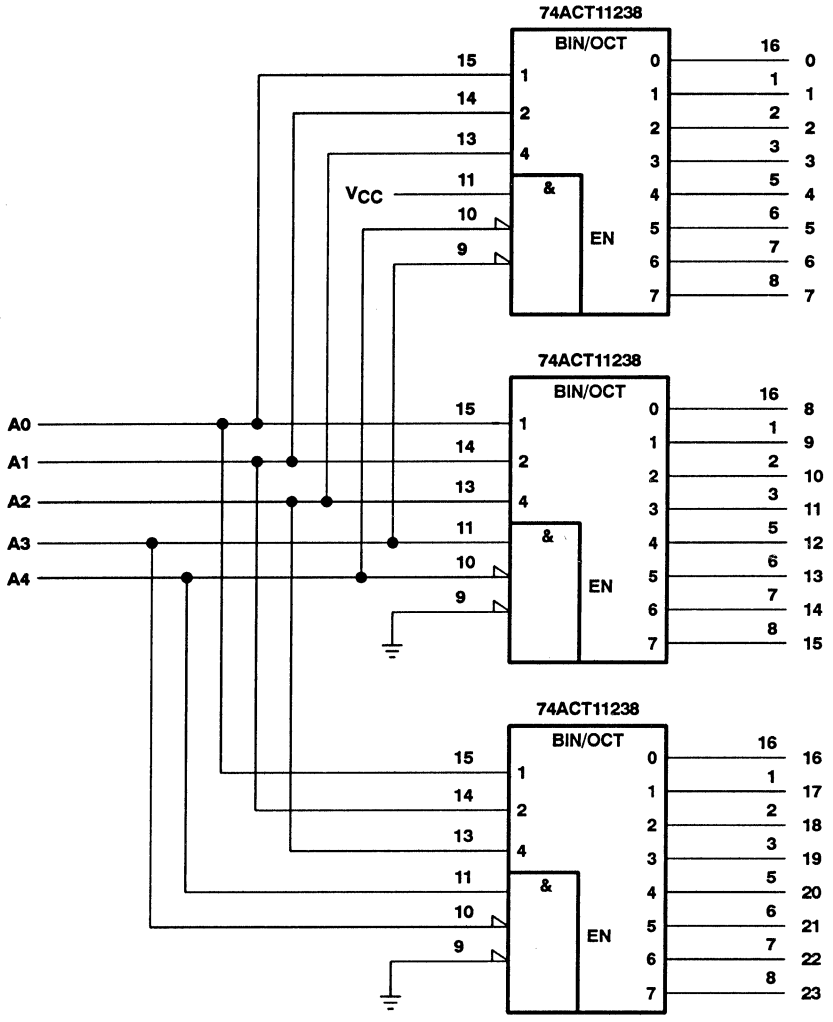


Figure 2. 24-Bit Decoding Scheme

TYPICAL APPLICATION DATA

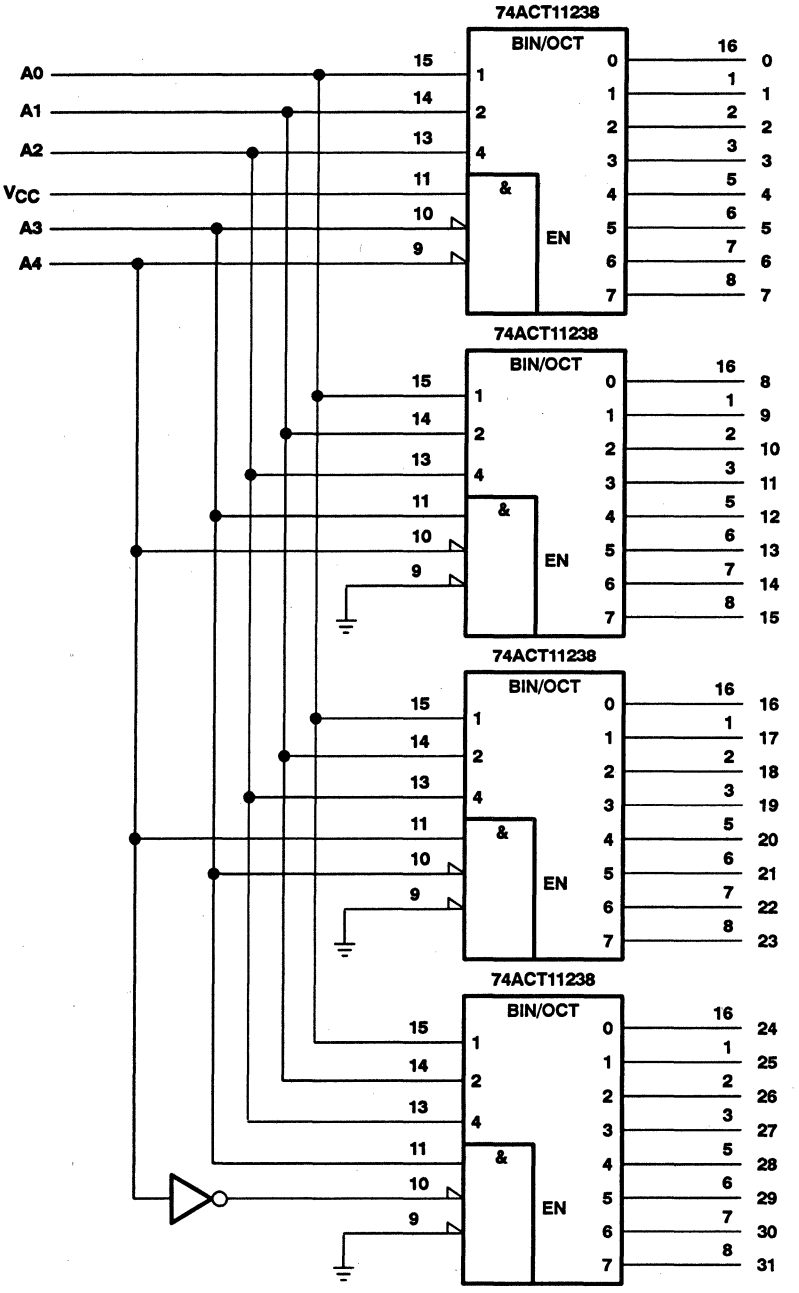


Figure 3. 32-Bit Decoding Scheme

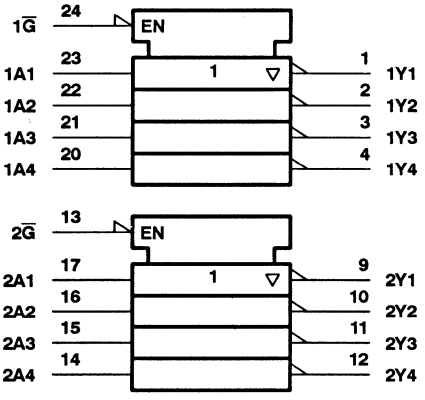
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These octal buffers/line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

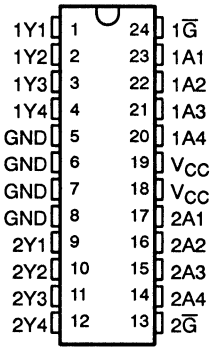
The 54AC11240 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11240 is characterized for operation from – 40°C to 85°C.

logic symbol†

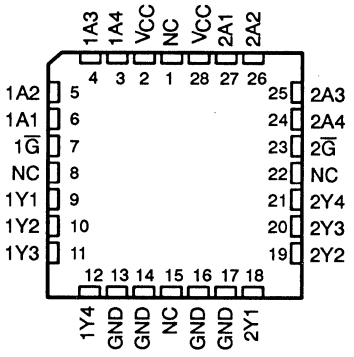


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

54AC11240 . . . JT PACKAGE
74AC11240 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54AC11240 . . . FK PACKAGE
(TOP VIEW)



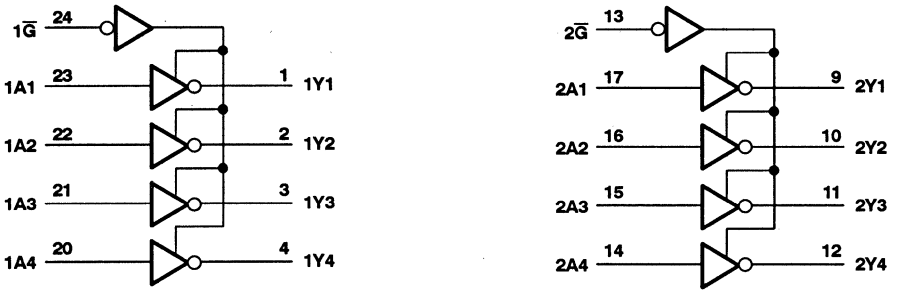
NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11240			74AC11240			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{G}$	0		5	0		5	ns/V
		Data	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11240		74AC11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_O	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11240		74AC11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	7.6	10.5	1.5	12.8	1.5	11.7	ns
t_{PHL}			1.5	6.3	8.6	1.5	10.2	1.5	9.5	
t_{PZH}	$\overline{G}$	Y	1.5	8.2	11.6	1.5	13.4	1.5	12.7	ns
t_{PZL}			1.5	7.6	10.8	1.5	13	1.5	12	
t_{PHZ}	$\overline{G}$	Y	1.5	5.5	7.5	1.5	8.1	1.5	7.8	ns
t_{PLZ}			1.5	6.7	9.4	1.5	10	1.5	9.8	

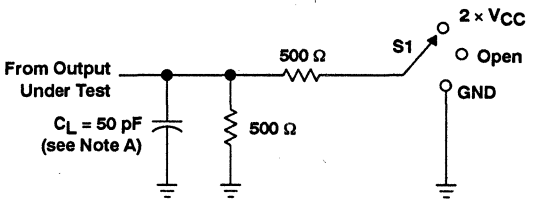
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11240		74AC11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5.4	7.5	1.5	9	1.5	8.4	ns
t_{PHL}			1.5	4.6	6.6	1.5	7.8	1.5	7.2	
t_{PZH}	$\overline{G}$	Y	1.5	5.7	8.2	1.5	9.9	1.5	9.2	ns
t_{PZL}			1.5	5.3	7.7	1.5	9.4	1.5	8.7	
t_{PHZ}	$\overline{G}$	Y	1.5	4.7	6.3	1.5	6.9	1.5	6.6	ns
t_{PLZ}			1.5	5.2	7.3	1.5	8	1.5	7.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

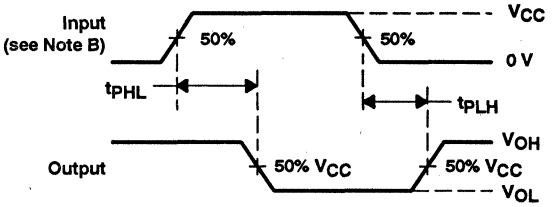
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

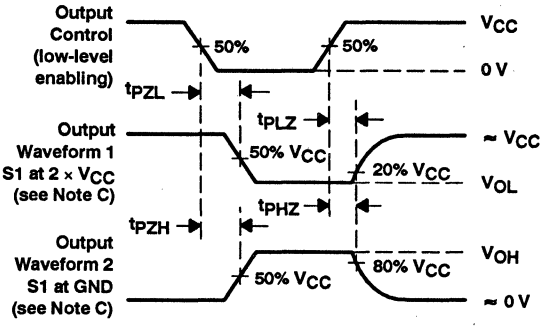


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

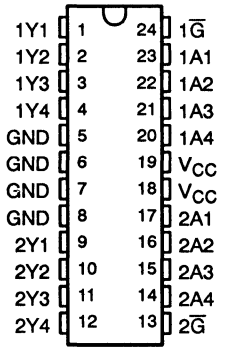
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

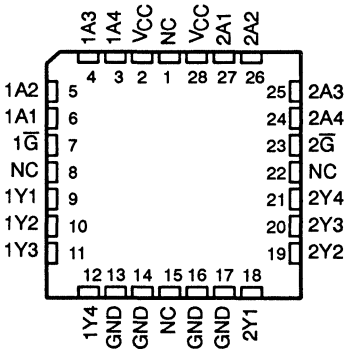
These octal buffers or line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide inverting outputs and symmetrical $\overline{G}$ (active-low output control) inputs. These devices feature high fan-out and improved fan-in.

The 54ACT11240 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11240 is characterized for operation from – 40°C to 85°C.

54ACT11240 . . . JT PACKAGE
74ACT11240 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11240 . . . FK PACKAGE
(TOP VIEW)



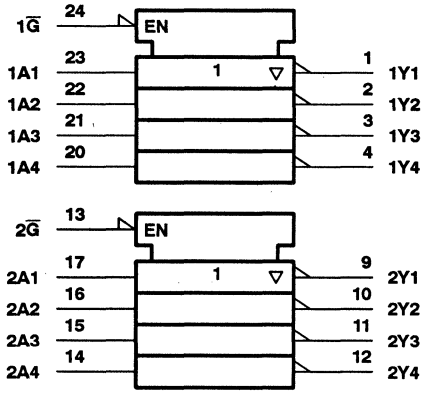
NC – No internal connection

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

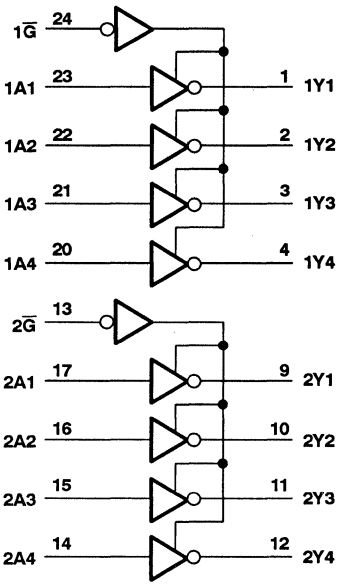
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_I = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

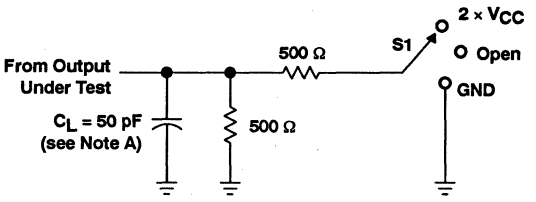
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11240		74ACT11240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6.5	9.9	1.5	11.1	1.5	10.6	ns
t_{PHL}			1.5	6	8	1.5	9.2	1.5	8.7	
t_{PZH}	$\overline{G}$	Y	1.5	7.5	11.7	1.5	13.1	1.5	12.5	ns
t_{PZL}			1.5	7.3	11.5	1.5	12.8	1.5	12.3	
t_{PHZ}	$\overline{G}$	Y	1.5	7.3	9.4	1.5	10.3	1.5	10	ns
t_{PLZ}			1.5	7.9	10.3	1.5	11.2	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

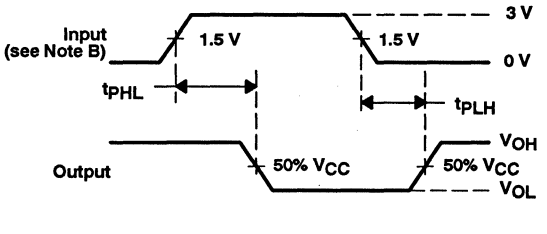
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

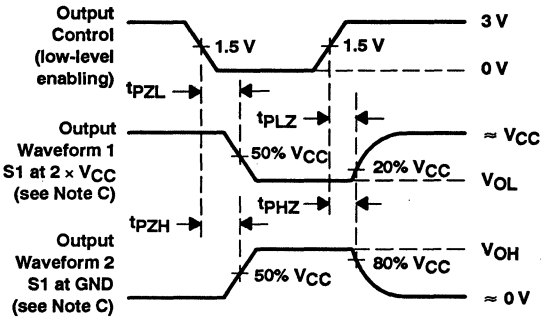


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



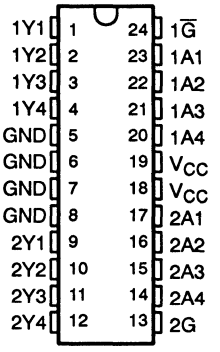
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

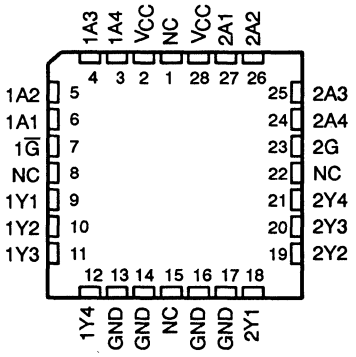
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11241 . . . JT PACKAGE
74AC11241 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54AC11241 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

This octal buffer or line driver is designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the AC11240 and AC11244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. This device features a high fan-out.

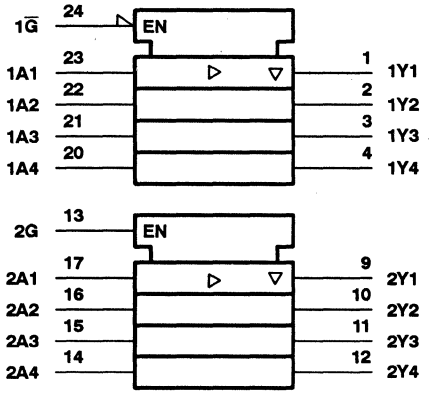
The 54AC11241 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11241 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

OUTPUT CONTROL $1\overline{G}$	DATA INPUT 1A	OUTPUT 1Y	OUTPUT CONTROL 2G	DATA INPUT 2A	OUTPUT 2Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

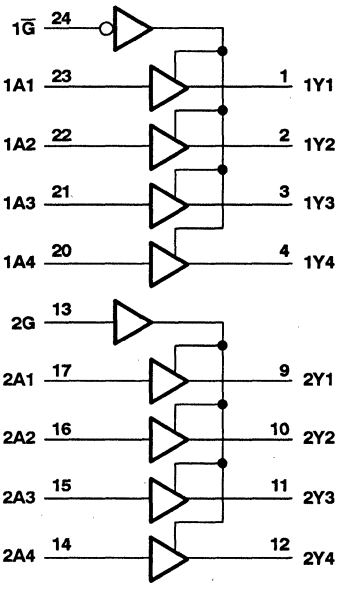
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11241			74AC11241			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			9.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		$\overline{G}$	0		5	0		5	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11241		74AC11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.7		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11241		74AC11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	7	10	1.5	12.2	1.5	11.4	ns
t_{PHL}			1.5	6.2	8.4	1.5	10.2	1.5	9.2	
t_{PZH}	$\overline{G}$ or G	Y	1.5	7.8	11.4	1.5	13.8	1.5	12.9	ns
t_{PZL}			1.5	7.7	10.6	1.5	12.6	1.5	11.7	
t_{PHZ}	$\overline{G}$ or G	Y	1.5	5.8	7.6	1.5	8.2	1.5	7.9	ns
t_{PLZ}			1.5	7.1	9.3	1.5	10.3	1.5	9.9	

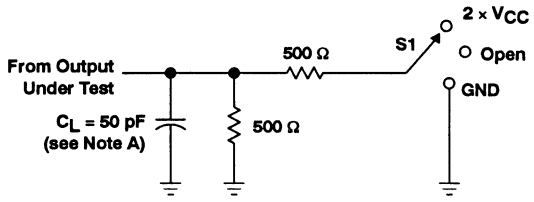
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11241		74AC11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4.9	7.1	1.5	8.5	1.5	8	ns
t_{PHL}			1.5	4.5	6.3	1.5	7.2	1.5	6.8	
t_{PZH}	$\overline{G}$ or G	Y	1.5	5.4	8	1.5	9.7	1.5	9	ns
t_{PZL}			1.5	5.3	7.6	1.5	9	1.5	8.4	
t_{PHZ}	$\overline{G}$ or G	Y	1.5	4.9	6.6	1.5	7.2	1.5	6.9	ns
t_{PLZ}			1.5	5.6	7.5	1.5	8.3	1.5	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

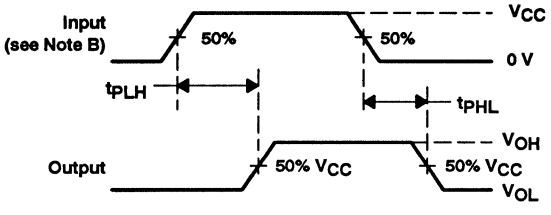
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	26	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

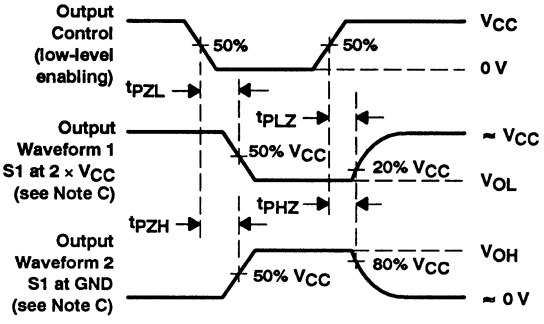


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



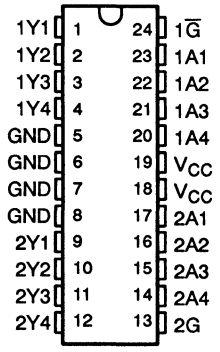
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

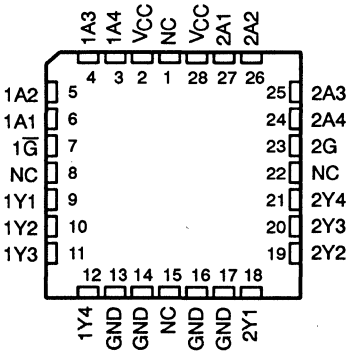
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11241 . . . JT PACKAGE
74ACT11241 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11241 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal buffers or line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ACT11240 and ACT11244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out.

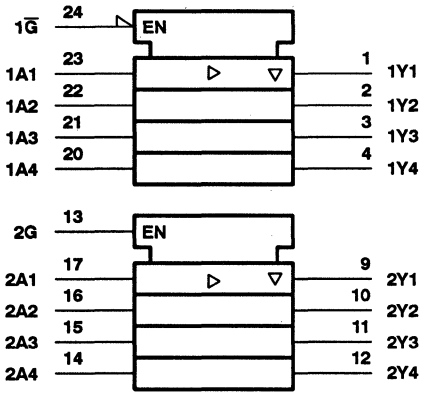
The 54ACT11241 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11241 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

OUTPUT CONTROL $1\overline{G}$	DATA INPUT 1A	OUTPUT 1Y	OUTPUT CONTROL 2G	DATA INPUT 2A	OUTPUT 2Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

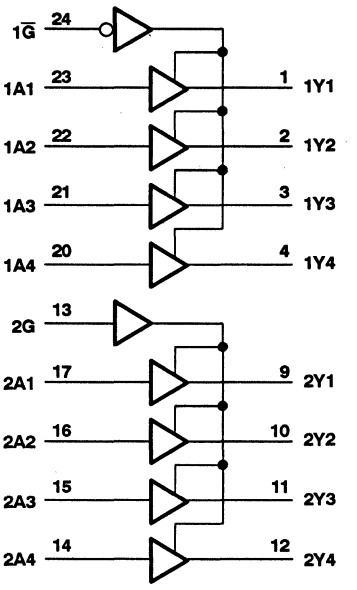
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at the se or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11241		74ACT11241		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

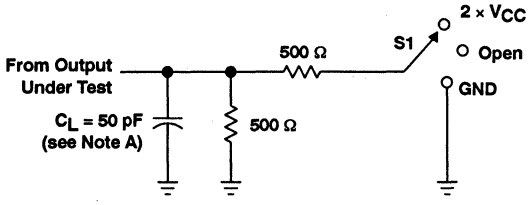
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6.6	9	1.5	10.7	1.5	10	ns
t_{PHL}			1.5	6.3	8.5	1.5	9.5	1.5	9.1	
t_{PZH}	G or $\overline{G}$	Y	1.5	7.5	11.3	1.5	13	1.5	12.3	
t_{PZL}			1.5	7.4	10.5	1.5	11.9	1.5	11.3	
t_{PHZ}	G or $\overline{G}$	Y	1.5	7.6	10.6	1.5	11.4	1.5	11	
t_{PLZ}			1.5	8.2	11.2	1.5	12	1.5	11.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

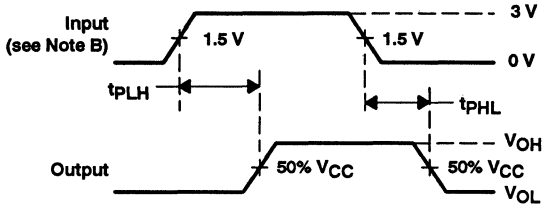
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
	Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

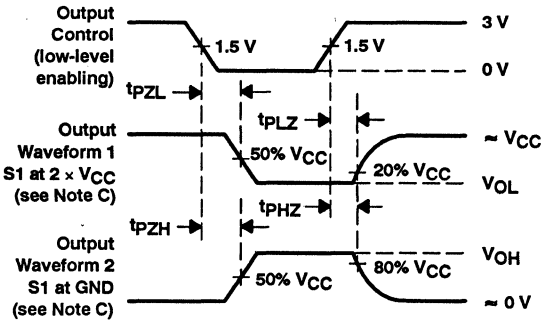


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



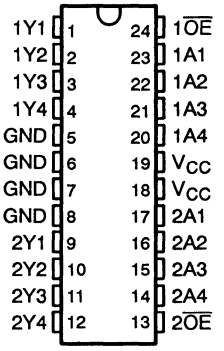
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

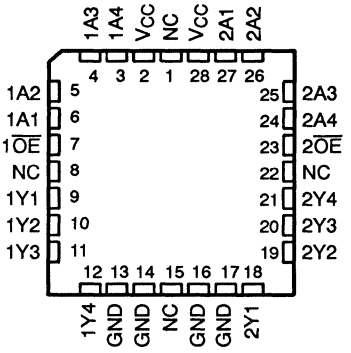
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC™* (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11244 . . . JT PACKAGE
74AC11244 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



54AC11244 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AC11244 is an octal buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as two 4-bit buffers or one 8-bit buffer. This device provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

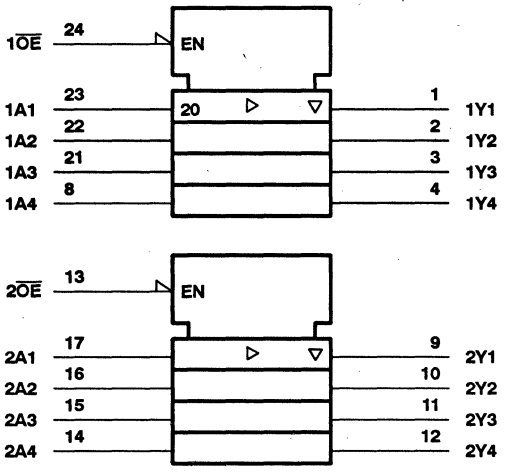
The 54AC11244 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

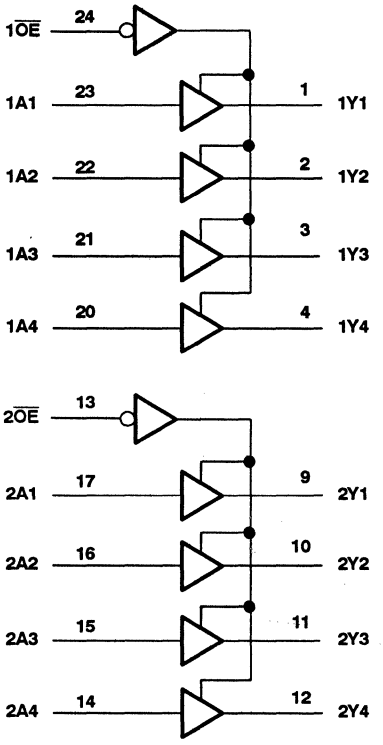
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol‡



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			54AC11244			74AC11244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = –4 mA	3 V	2.58			2.4		2.48		
	I_{OL} = –24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = –50 mA†	5.5 V				3.85				
	I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	7.1	9.3	1.5	10.8	1.5	10.2	ns
t_{PHL}			1.5	6.3	8.6	1.5	10.5	1.5	9.5	
t_{PZH}	$\overline{OE}$	Y	1.5	8	10.7	1.5	12.9	1.5	11.8	ns
t_{PZL}			1.5	7.9	10.6	1.5	12.9	1.5	11.9	
t_{PHZ}	$\overline{OE}$	Y	1.5	5.9	7.9	1.5	8.7	1.5	8.3	ns
t_{PLZ}			1.5	7.2	9.4	1.5	10.4	1.5	9.9	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

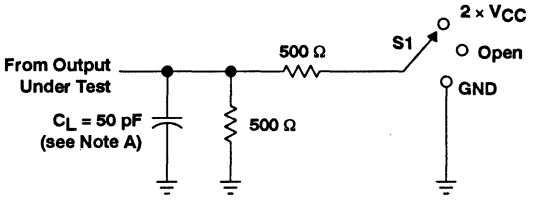
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4.9	6.7	1.5	7.7	1.5	7.3	ns
t_{PHL}			1.5	4.5	6.4	1.5	7.4	1.5	6.9	
t_{PZH}	$\overline{OE}$	Y	1.5	5.4	7.7	1.5	9.3	1.5	8.5	ns
t_{PZL}			1.5	5.4	7.6	1.5	9.1	1.5	8.5	
t_{PHZ}	$\overline{OE}$	Y	1.5	5.2	7	1.5	7.6	1.5	7.3	ns
t_{PLZ}			1.5	5.8	7.8	1.5	8.6	1.5	8.2	

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

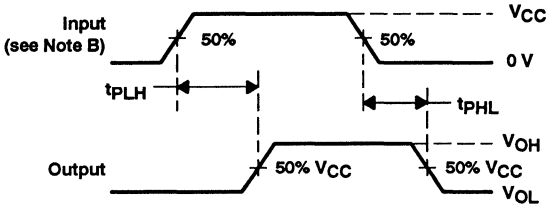
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

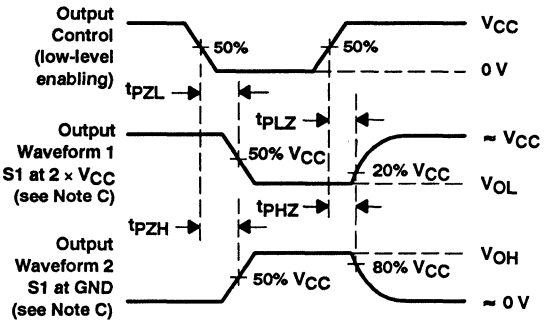


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



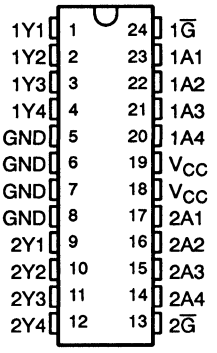
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

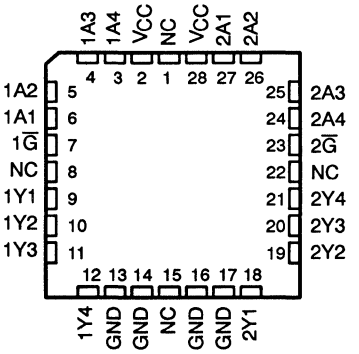
Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11244 . . . JT PACKAGE
74ACT11244 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



54ACT11244 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal buffers or line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ACT11240 and 'ACT11241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

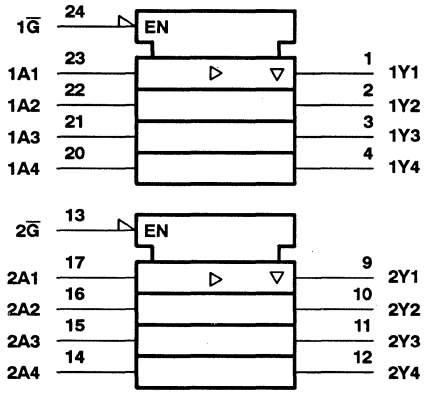
The 54ACT11244 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11244 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

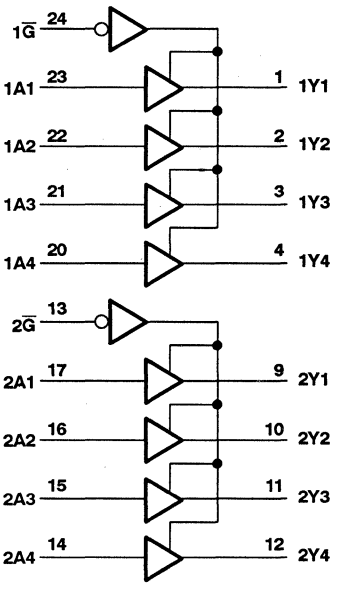
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11244		74ACT11244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

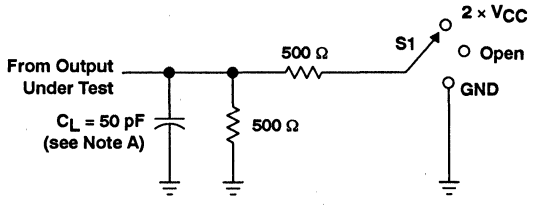
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11244		74ACT11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6	8.9	1.5	10.6	1.5	9.9	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.7	1.5	9.2	
t_{PZH}	$\overline{G}$	Y	1.5	6.6	11.3	1.5	13.4	1.5	12.5	ns
t_{PZL}			1.5	6.7	10.5	1.5	12.2	1.5	11.4	
t_{PHZ}	$\overline{G}$	Y	1.5	7.4	9.8	1.5	10.8	1.5	10.4	ns
t_{PLZ}			1.5	7.8	10.6	1.5	11.6	1.5	11.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

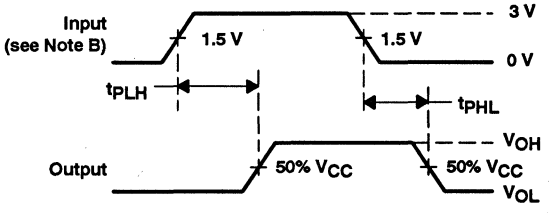
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	27	pF
	Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

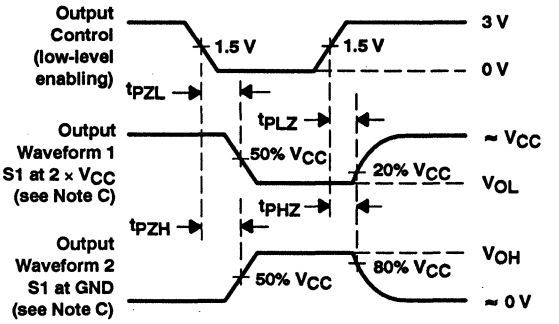


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
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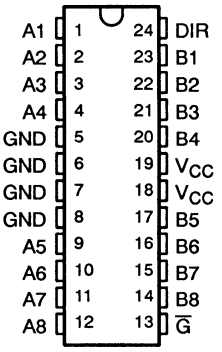
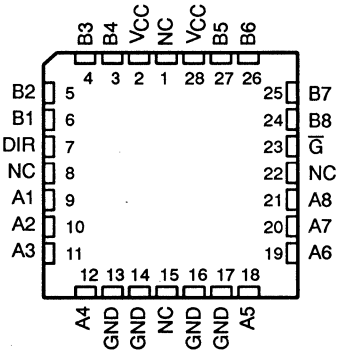
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11245 . . . JT PACKAGE
74AC11244 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



54AC11245 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

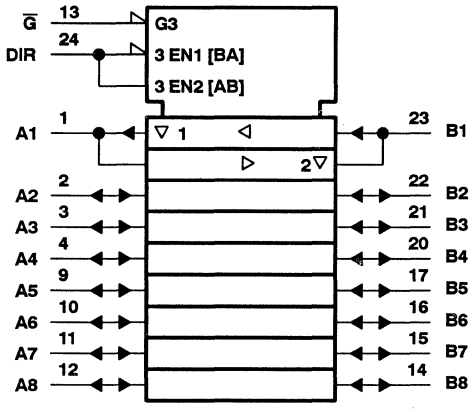
The 54AC11245 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11245 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

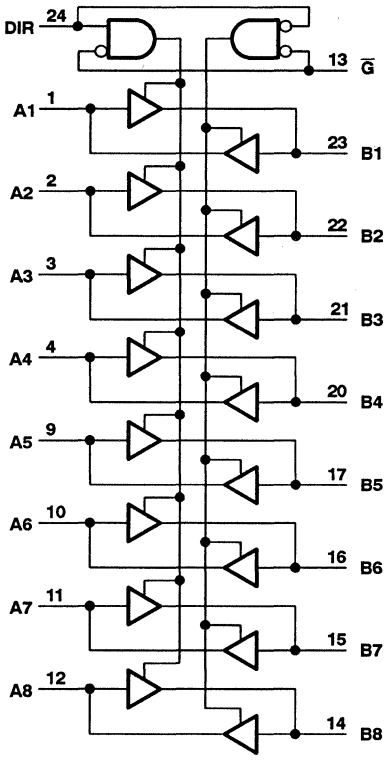
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11245			74AC11245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11245		74AC11245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	µA
	$\overline{G}$ or DIR					±0.1		±1		±1	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
C_i		V_I = V_{CC} or GND	5 V		4						pF
C_{io}		V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11245		74AC11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.5	11.2	1.5	13.3	1.5	12.5	ns
t_{PHL}			1.5	5.7	8.5	1.5	10.3	1.5	9.7	
t_{PZH}	$\overline{G}$	B or A	1.5	8.6	14.2	1.5	17.1	1.5	15.9	ns
t_{PZL}			1.5	8.2	11.5	1.5	13.7	1.5	12.7	
t_{PHZ}	$\overline{G}$	B or A	1.5	7.7	10.5	1.5	11.9	1.5	11.3	ns
t_{PLZ}			1.5	8.5	12	1.5	13.8	1.5	13	

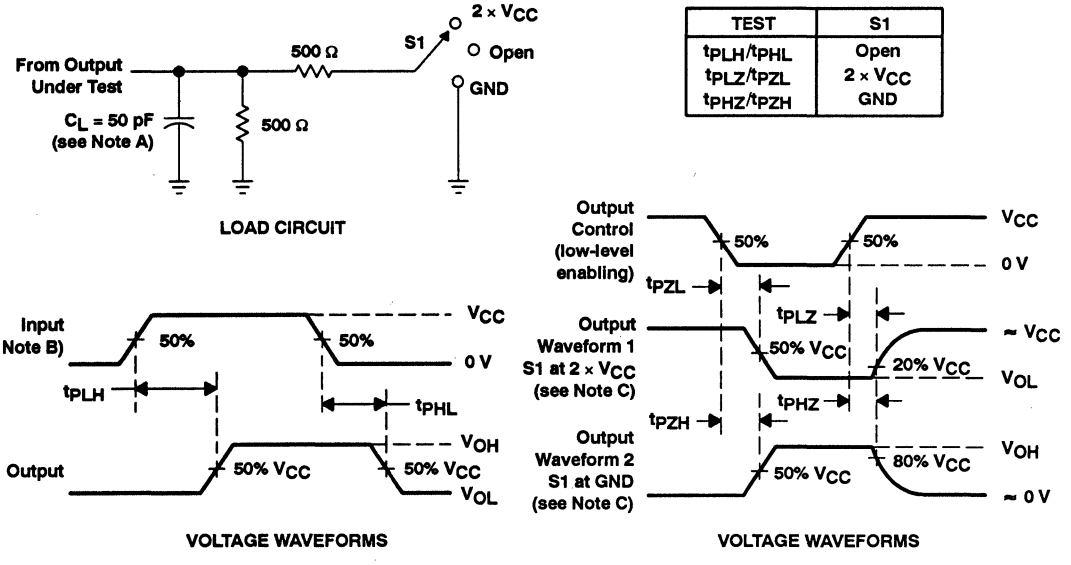
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11245		74AC11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	4.8	8.5	1.5	10.2	1.5	9.5	ns
t_{PHL}			1.5	4.1	6.3	1.5	7.4	1.5	6.9	
t_{PZH}	$\overline{G}$	B or A	1.5	6.2	10.2	1.5	12.4	1.5	11.4	ns
t_{PZL}			1.5	5.9	8.6	1.5	10.3	1.5	9.5	
t_{PHZ}	$\overline{G}$	B or A	1.5	6.4	8.8	1.5	10	1.5	9.5	ns
t_{PLZ}			1.5	7	9.6	1.5	11	1.5	10.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	64	pF
		Outputs disabled		16	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

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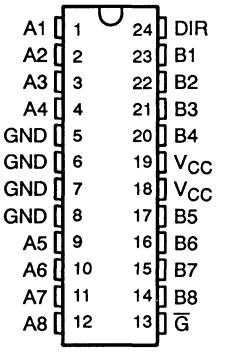
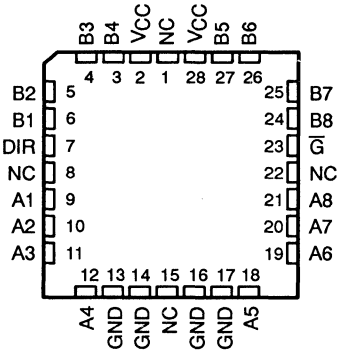
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Plastic Thin Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11245 . . . JT PACKAGE
74ACT11245 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



54ACT11245 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus tranceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disabled the device so that the buses are affectively isolated.

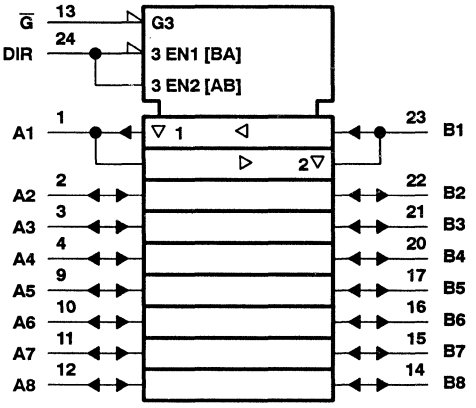
The 54ACT11245 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11245 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OUTPUT
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

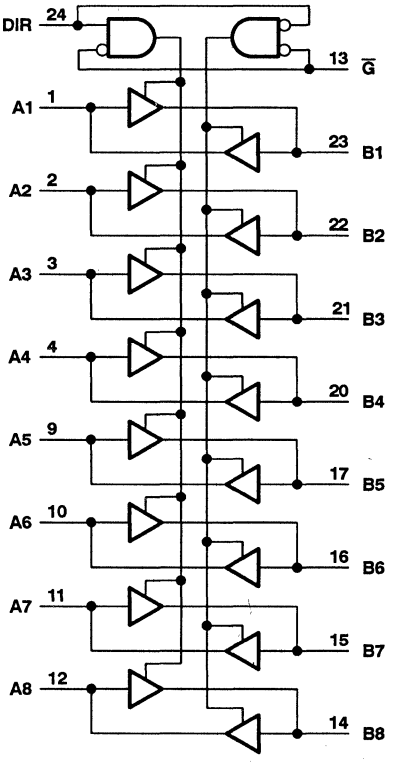
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11245		74ACT11245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11245		74ACT11245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		±5	μA
I_I	$\overline{G}$ or DIR	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i		$V_I = V_{CC}$ or GND	5 V		4						pF
C_o		$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

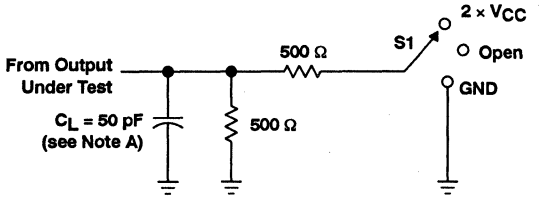
switching characteristics over recomended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.2	9.2	1.5	10.6	1.5	10	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.6	1.5	9.1	
t_{PZH}	$\overline{G}$	A or B	1.5	8.1	12	1.5	14.1	1.5	13.2	ns
t_{PZL}			1.5	8.2	11.7	1.5	13.7	1.5	12.9	
t_{PHZ}	$\overline{G}$	A or B	1.5	9.3	11.8	1.5	13.6	1.5	12.9	ns
t_{PLZ}			1.5	9.8	12.9	1.5	14.6	1.5	13.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

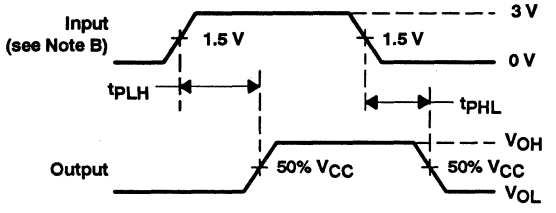
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		19	

PARAMETER MEASUREMENT INFORMATION

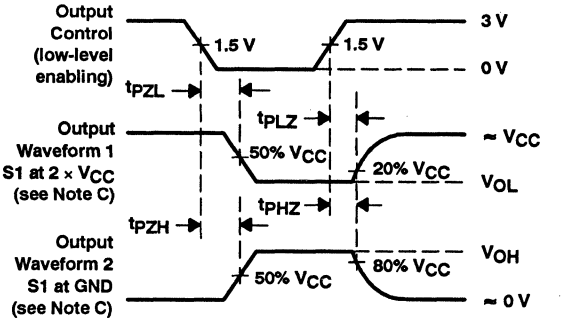


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



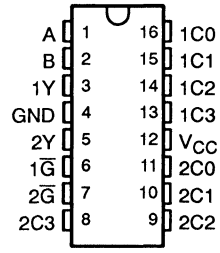
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

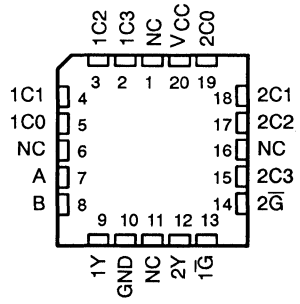
Figure 1. Load Circuit and Voltage Waveforms

- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11253 . . . J PACKAGE
74AC11253 . . . D OR N PACKAGE
(TOP VIEW)



54AC11253 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

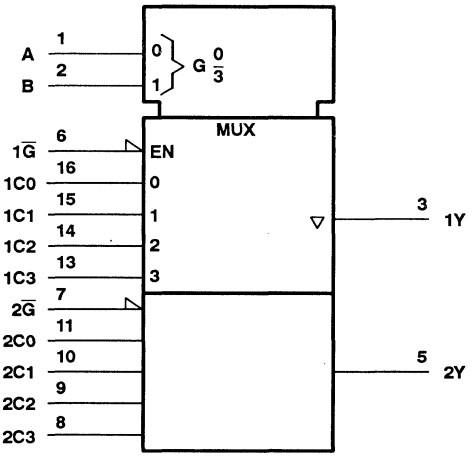
The 54AC11253 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11253 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

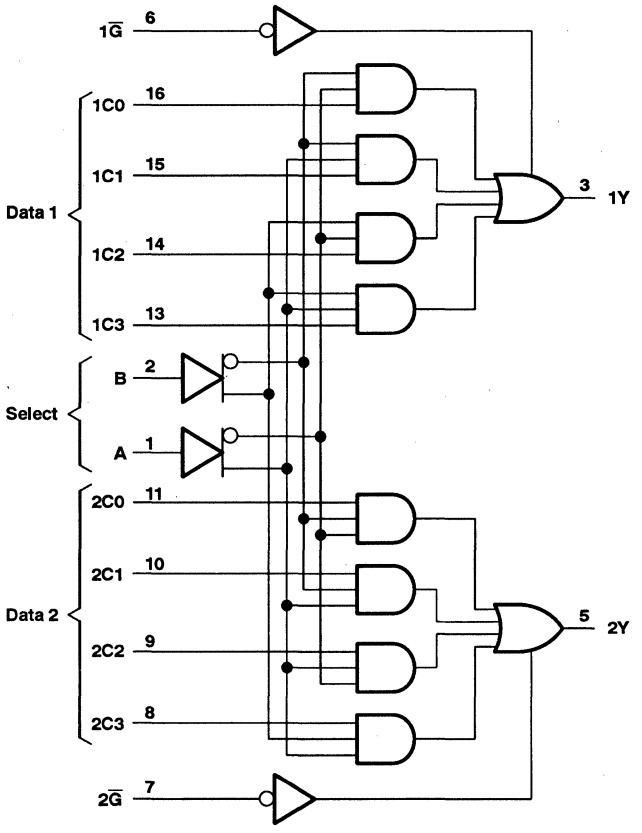
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

			54AC11253			74AC11253			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11253		74AC11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF
C_o	V_O = V_{CC} or GND	5 V		8						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11253		74AC11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	7.1	9.7	1.5	11.7	1.5	11	ns
t_{PHL}			1.5	7.5	10.1	1.5	12.1	1.5	11.4	
t_{PLH}	Data (Any C)	Y	1.5	6.8	8.3	1.5	9.9	1.5	9.3	ns
t_{PHL}			1.5	7	8.8	1.5	10.3	1.5	9.6	
t_{PZH}	$\overline{G}$	Y	1.5	4.8	6.2	1.5	7.2	1.5	6.8	ns
t_{PZL}			1.5	5.8	7.4	1.5	8.7	1.5	8.2	
t_{PHZ}	$\overline{G}$	Y	1.5	5	6.3	1.5	7	1.5	6.7	ns
t_{PLZ}			1.5	5.2	6.5	1.5	7.2	1.5	6.9	

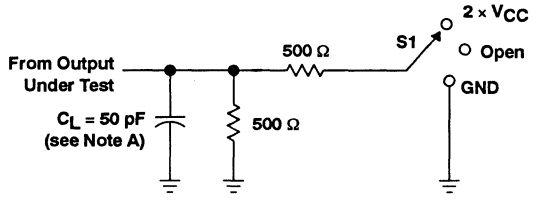
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11253		74AC11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	4.9	7	1.5	8.3	1.5	7.9	ns
t_{PHL}			1.5	5.2	7.3	1.5	8.7	1.5	8.2	
t_{PLH}	Data (Any C)	Y	1.5	4.5	5.9	1.5	7.1	1.5	6.6	ns
t_{PHL}			1.5	4.8	6.3	1.5	7.3	1.5	6.9	
t_{PZH}	$\overline{G}$	Y	1.5	3.4	4.6	1.5	6.4	1.5	5.1	ns
t_{PZL}			1.5	4	5.3	1.5	6.1	1.5	5.8	
t_{PHZ}	$\overline{G}$	Y	1.5	4.7	6	1.5	6.6	1.5	6.3	ns
t_{PLZ}			1.5	4.6	5.9	1.5	6.4	1.5	6.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

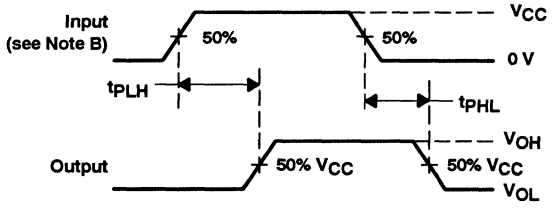
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	Outputs enabled	C_L = 50 pF, f = 1 MHz	31	pF
		Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

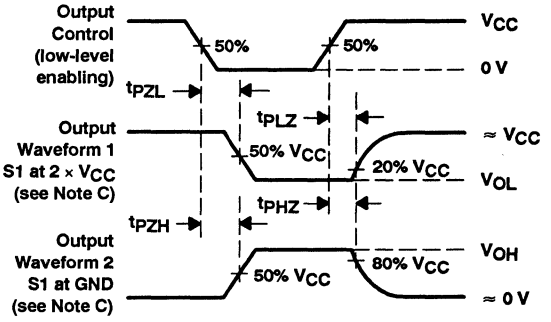


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Version of 'ACT11153**
- **Permits Multiplexing From N Lines to One Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

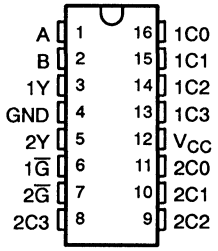
The 54ACT11253 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11253 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

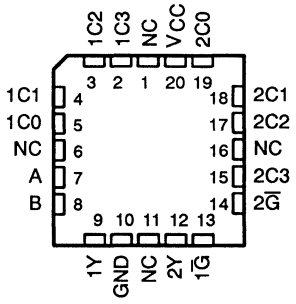
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

54ACT11253 . . . J PACKAGE
74ACT11253 . . . D OR N PACKAGE
(TOP VIEW)

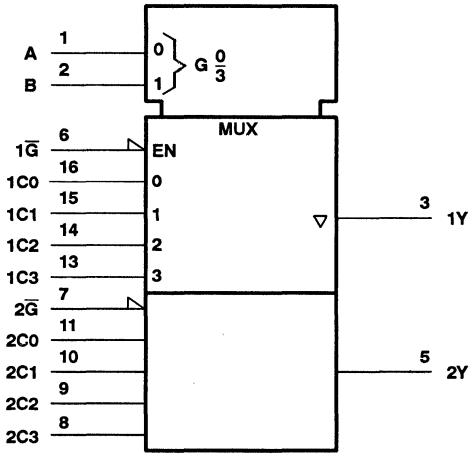


54ACT11253 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

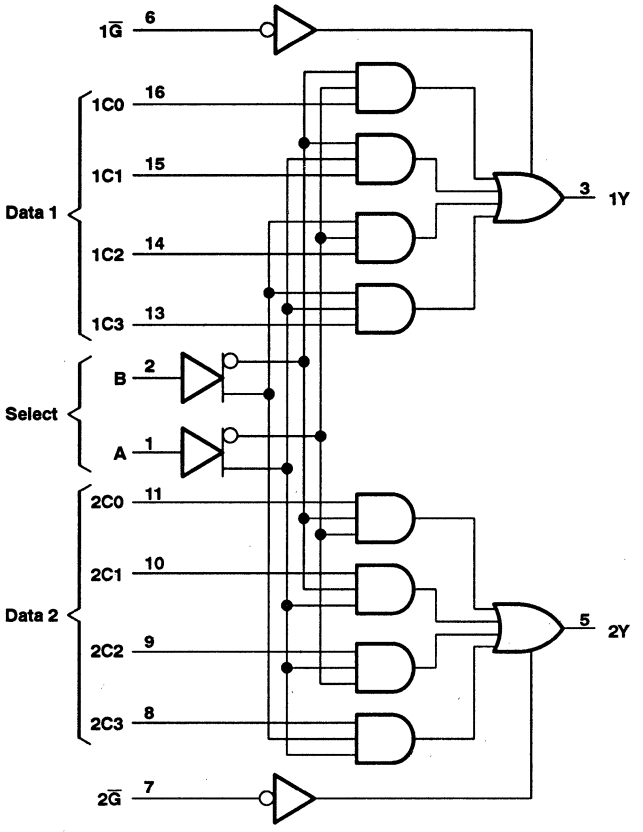
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

recommended operating conditions

		54ACT11253		74ACT11253		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11253		74ACT11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		8						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

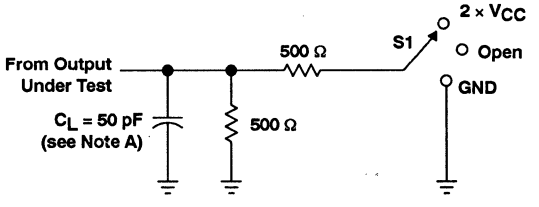
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11253		74ACT11253		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1.5	6.8	9.8	1.5	11.8	1.5	11	ns
t_{PHL}			1.5	9.1	12.6	1.5	15.5	1.5	14.3	
t_{PLH}	Data (Any C)	Y	1.5	5.7	7.4	1.5	8.9	1.5	8.3	ns
t_{PHL}			1.5	7.2	10.5	1.5	12.5	1.5	11.7	
t_{PZH}	$\overline{G}$	Y	1.5	5	7.6	1.5	9	1.5	8.5	ns
t_{PZL}			1.5	4.8	7.3	1.5	8.6	1.5	8.1	
t_{PHZ}	$\overline{G}$	Y	1.5	6.4	8.6	1.5	9.5	1.5	9.2	ns
t_{PLZ}			1.5	5.9	7.4	1.5	8.1	1.5	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

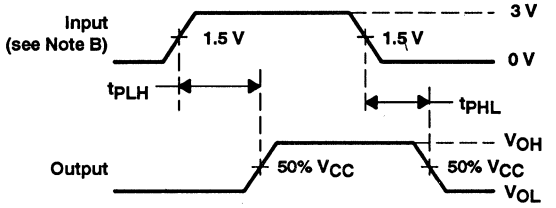
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		18	

PARAMETER MEASUREMENT INFORMATION

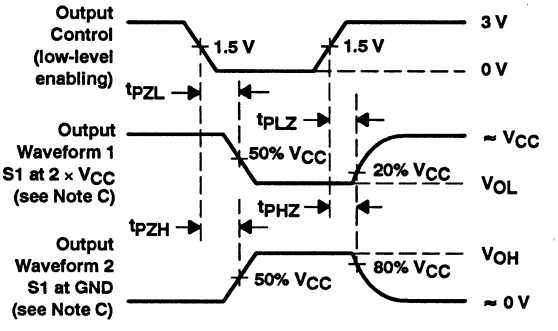


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

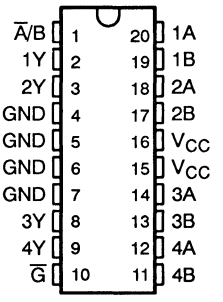
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3259, MARCH 1989 – REVISED APRIL 1993

- **3-State Outputs Interface Directly With System Bus**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Provides Bus Interface From Multiple Sources In High-Performance Systems**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This device is designed to multiplex signals from 4-bit data sources to four output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high logic level.

The 74AC11257 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

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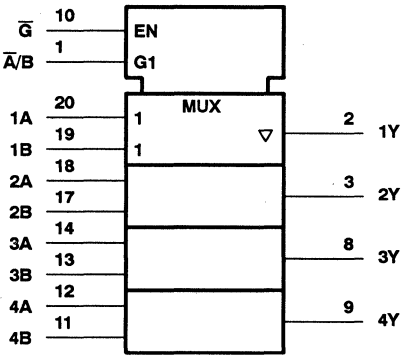
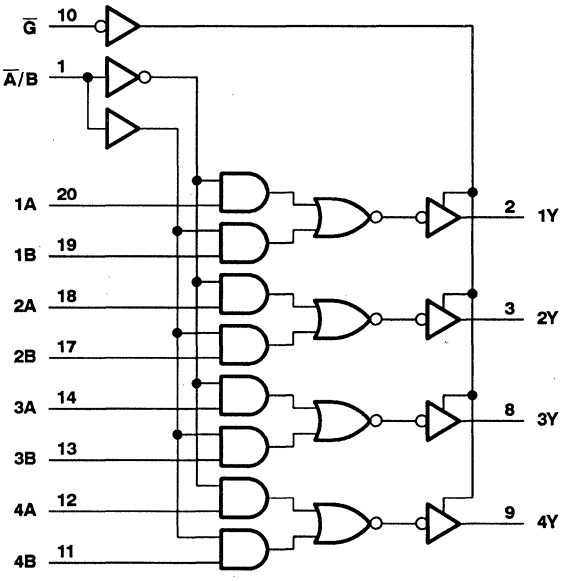
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF
C_o	V_O = V_{CC} or GND	5.5 V		8				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	5.6	8.1	1.5	8.9	ns
t_{PHL}			1.5	6.2	9	1.5	10.1	
t_{PLH}	$\overline{A}$/B	Any Y	1.5	6.1	9.2	1.5	10.2	ns
t_{PHL}			1.5	6.6	10	1.5	11.2	
t_{PZH}	$\overline{G}$	Any Y	1.5	5.6	8.2	1.5	9.1	ns
t_{PZL}			1.5	7.5	10.4	1.5	11.8	
t_{PHZ}	$\overline{G}$	Any Y	1.5	5.6	7.6	1.5	8.3	ns
t_{PLZ}			1.5	6.2	8.8	1.5	9.6	

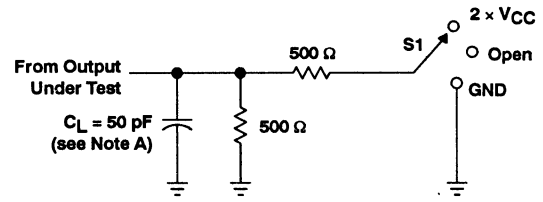
switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	3.6	5.8	1.5	6.4	ns
t_{PHL}			1.5	4.1	6.5	1.5	7.2	
t_{PLH}	$\overline{A}$/B	Any Y	1.5	4	6.5	1.5	7.2	ns
t_{PHL}			1.5	4.4	7.1	1.5	7.9	
t_{PZH}	$\overline{G}$	Any Y	1.5	3.8	5.9	1.5	6.5	ns
t_{PZL}			1.5	5	7.6	1.5	8.6	
t_{PHZ}	$\overline{G}$	Any Y	1.5	4.5	6.4	1.5	7.6	ns
t_{PLZ}			1.5	4.8	6.9	1.5	7.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

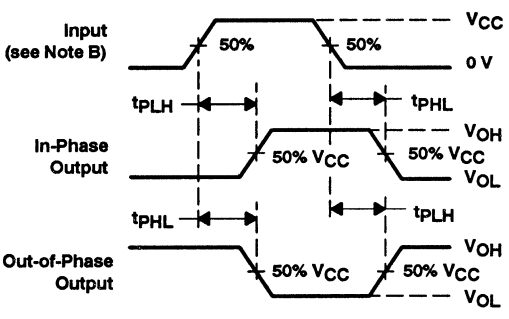
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	37	pF
	Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

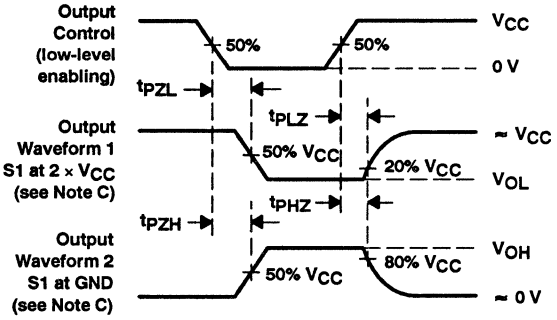


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



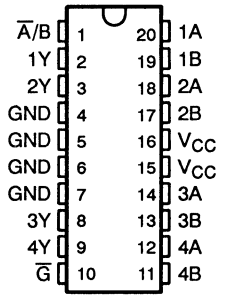
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

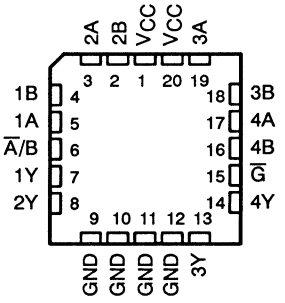
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Interface Directly With System Bus**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Provides Bus Interface From Multiple Sources In High-Performance Systems**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11257 . . . J PACKAGE
74ACT11257 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11257 . . . FK PACKAGE
(TOP VIEW)



description

The ACT11257 is designed to multiplex signals from 4-bit data sources to four output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high logic level.

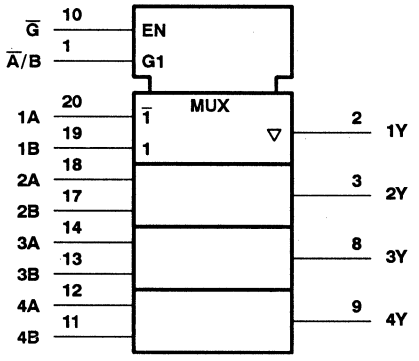
The 54ACT11257 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11257 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

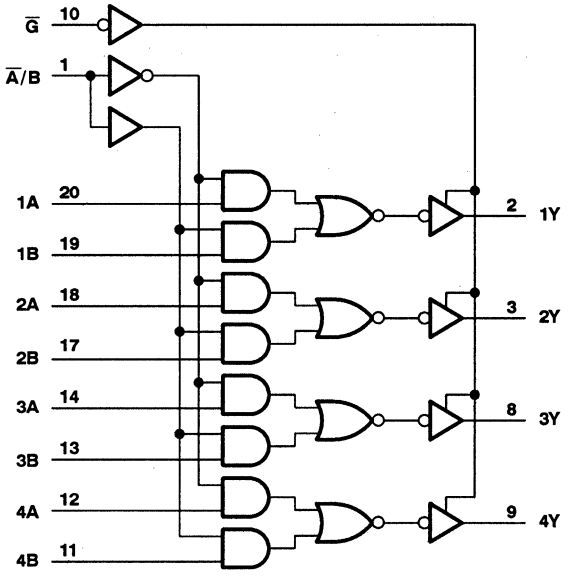
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11257		74ACT11257		UNIT
		MIN	MAX	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11257		74ACT11257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		8						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

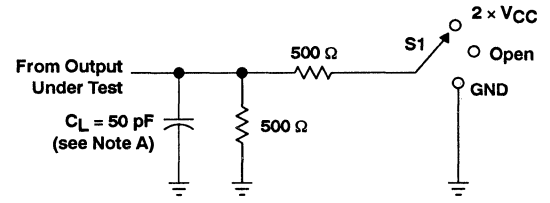
switching characteristics over recomended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11257		74ACT11257		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	4.4	6.4	1.5	7.4	1.5	6.9	ns
t_{PHL}			1.5	5	8	1.5	9.3	1.5	8.7	
t_{PLH}	$\overline{A}$/B	Any Y	1.5	4.7	7.6	1.5	8.7	1.5	8.2	ns
t_{PHL}			1.5	5.7	8.5	1.5	10.1	1.5	9.4	
t_{PZH}	$\overline{G}$	Any Y	1.5	4.2	6.9	1.5	7.7	1.5	7.3	ns
t_{PZL}			1.5	5.5	8.7	1.5	10.3	1.5	9.6	
t_{PHZ}	$\overline{G}$	Any Y	1.5	5.7	7.6	1.5	8.9	1.5	8.4	ns
t_{PLZ}			1.5	6	7.9	1.5	9	1.5	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

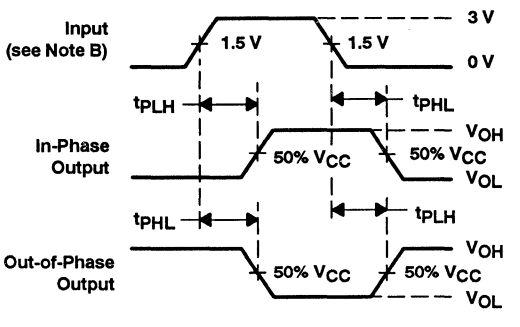
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
	Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

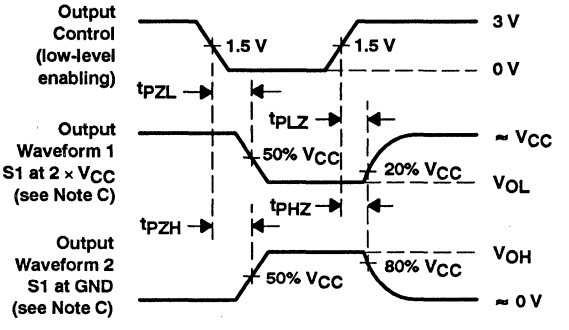


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



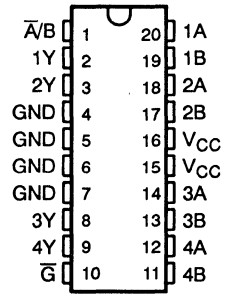
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Interface Directly With System Bus**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high logic level.

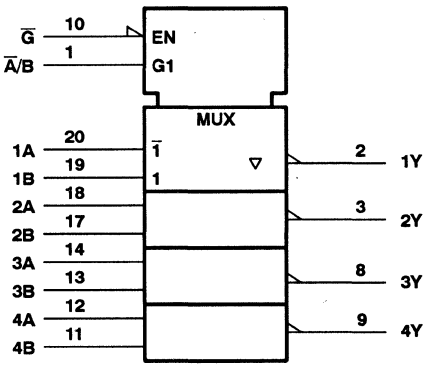
The 74ACT11258 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

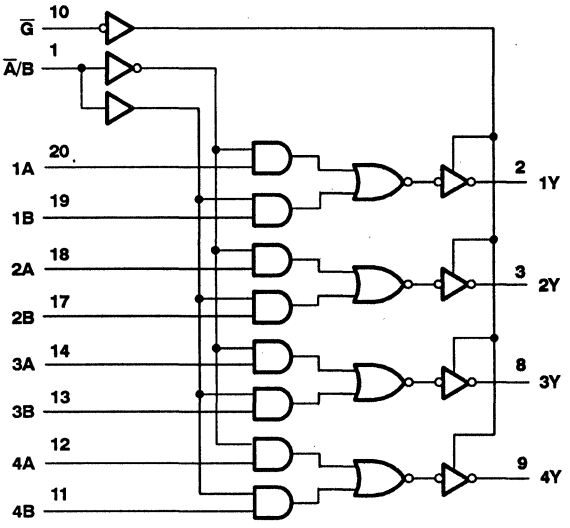
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = –24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5				pF
C_o	$V_O = V_{CC}$ or GND	5 V		8				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

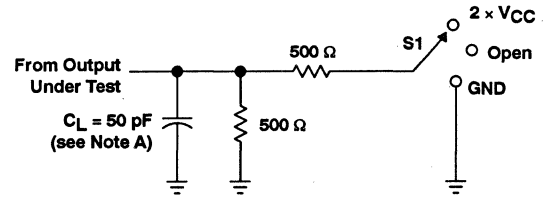
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Any Y	1.5	5.4	7.7	1.5	8.5	ns
t_{PHL}			1.5	5.7	7.7	1.5	8.7	
t_{PLH}	$\overline{A}$/B	Any Y	1.5	5.7	8	1.5	8.8	ns
t_{PHL}			1.5	6.7	9.4	1.5	10.4	
t_{PZH}	$\overline{G}$	Any Y	1.5	5.7	8.1	1.5	8.8	ns
t_{PZL}			1.5	6.4	8.8	1.5	9.8	
t_{PHZ}	$\overline{G}$	Any Y	1.5	6.1	7.5	1.5	7.7	ns
t_{PLZ}			1.5	6.3	8.3	1.5	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

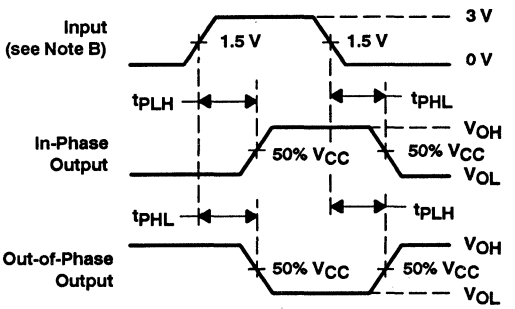
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	35	pF
	Outputs disabled		15	

PARAMETER MEASUREMENT INFORMATION

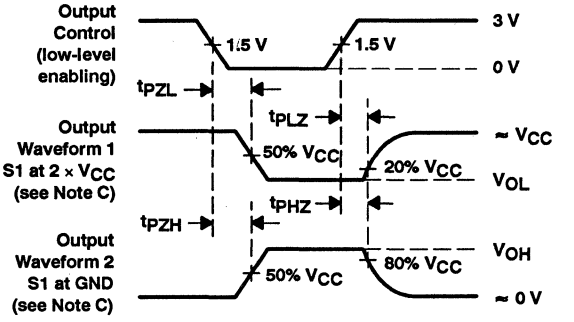


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



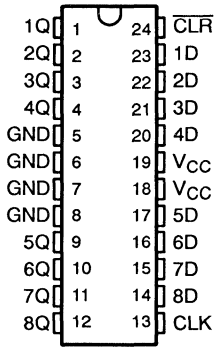
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Flow-Through Architecture to Optimize PCB Layout**
- **Multiple Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These positive-edge-triggered flip-flops implement D-type flip-flop logic with a direct clear input.

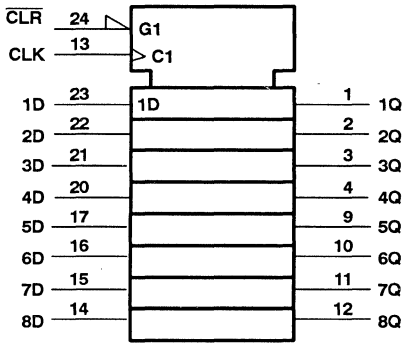
Data at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 74AC11273 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

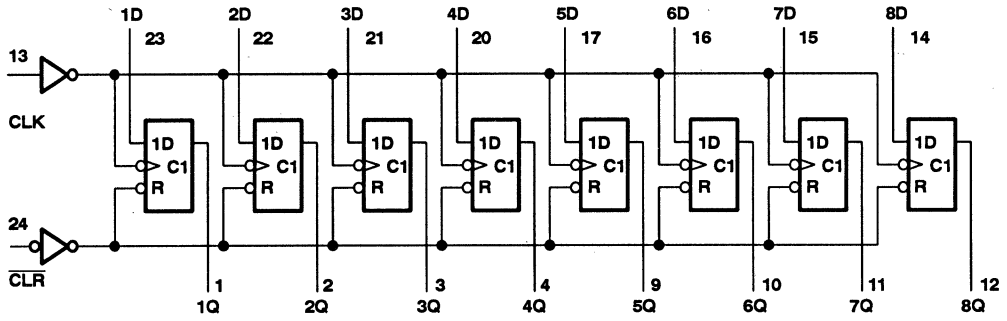
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 50 mA†	5.5 V						
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 50 mA†	5.5 V						
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	55	0	55	MHz
t_w	Pulse duration	$\overline{CLR}$ low	6		6		ns
		CLK high or low	9.1		9.1		
t_{su}	Setup time before CLK↑	Data	7.5		7.5		ns
		$\overline{CLR}$ inactive	6		6		
t_h	Hold time, data after CLK↑		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	80	0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	6.3		6.3		
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{CLR}$ inactive	4.5		4.5		
t_h	Hold time, data after CLK↑		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			55			55		MHz
t_{PHL}	$\overline{CLR}$	Any Q	5.2	14.3	16.5	5.2	18.4	ns
t_{PLH}	CLK	Any Q	4.2	12.1	14.3	4.2	16.5	ns
t_{PHL}			5.5	14.5	16.7	5.5	18.6	

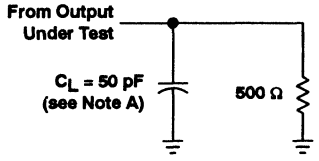
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			80			80		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4.3	9.2	10.9	4.3	12.3	ns
t_{PLH}	CLK	Any Q	3.5	7.7	9.3	3.5	10.7	ns
t_{PHL}			4.5	9.3	11	4.5	12.4	

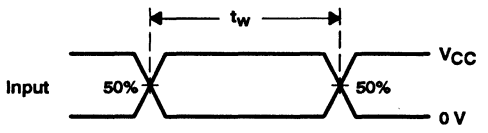
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	80	pF

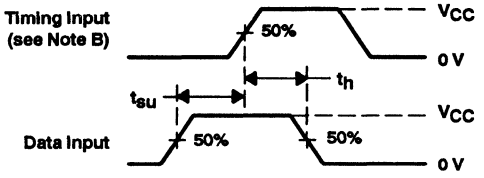
PARAMETER MEASUREMENT INFORMATION



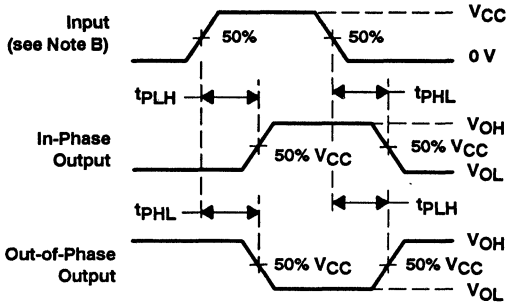
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



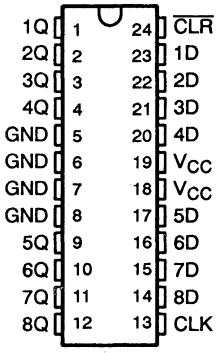
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Multiple Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These positive-edge-triggered flip-flops implement D-type flip-flop logic with a direct clear input.

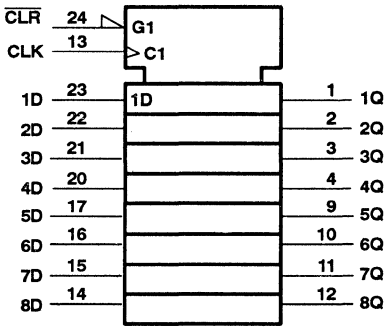
Data at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 74ACT11273 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

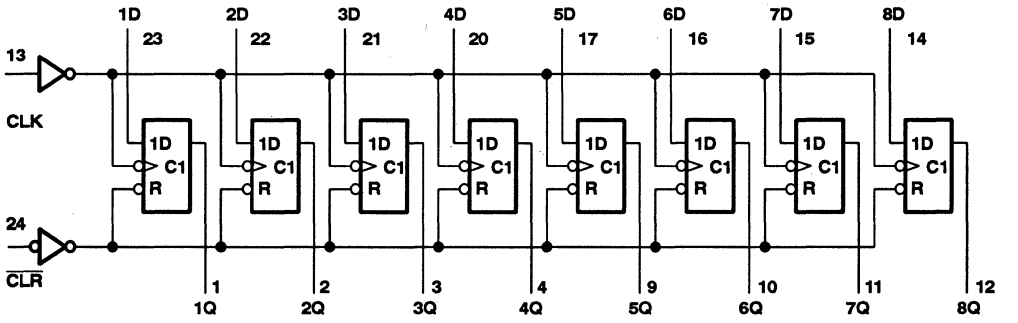
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 200 mA
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_O = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	85	0	85	MHz
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	5.9		5.9		
t_{su}	Setup time before CLK↑	Data high	4		4		ns
		Data low	5		5		
		$\overline{CLR}$ inactive	4		4		
t_h	Hold time after CLK↑		1		1		ns

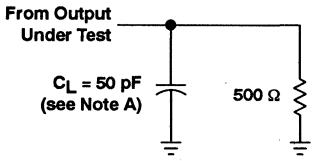
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			85			85		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4.4	9.5	12	4.4	13.3	ns
t_{PLH}	CLK	Any Q	5.4	9.4	11.4	5.4	13.1	ns
t_{PHL}			6	10.3	12.5	6	14.1	

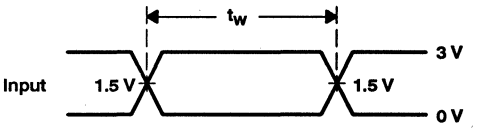
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	73	pF

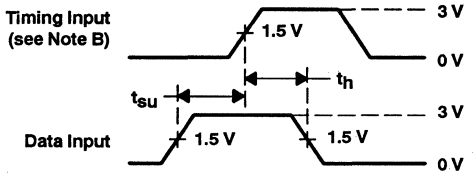
PARAMETER MEASUREMENT INFORMATION



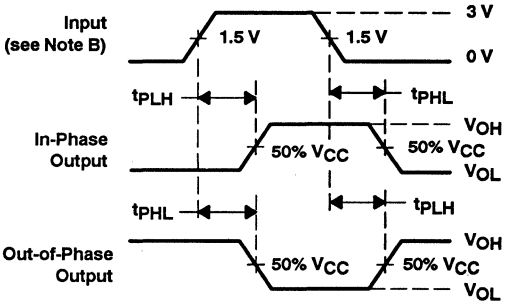
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

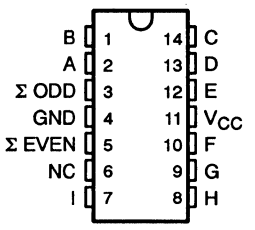
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS055A – D3201, APRIL 1989 – REVISED APRIL 1993

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

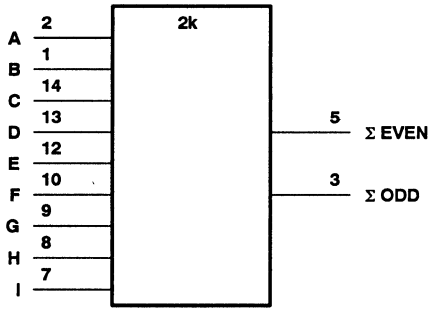
This universal, monolithic, nine-bit parity generator/checker features odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The 74AC11280 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

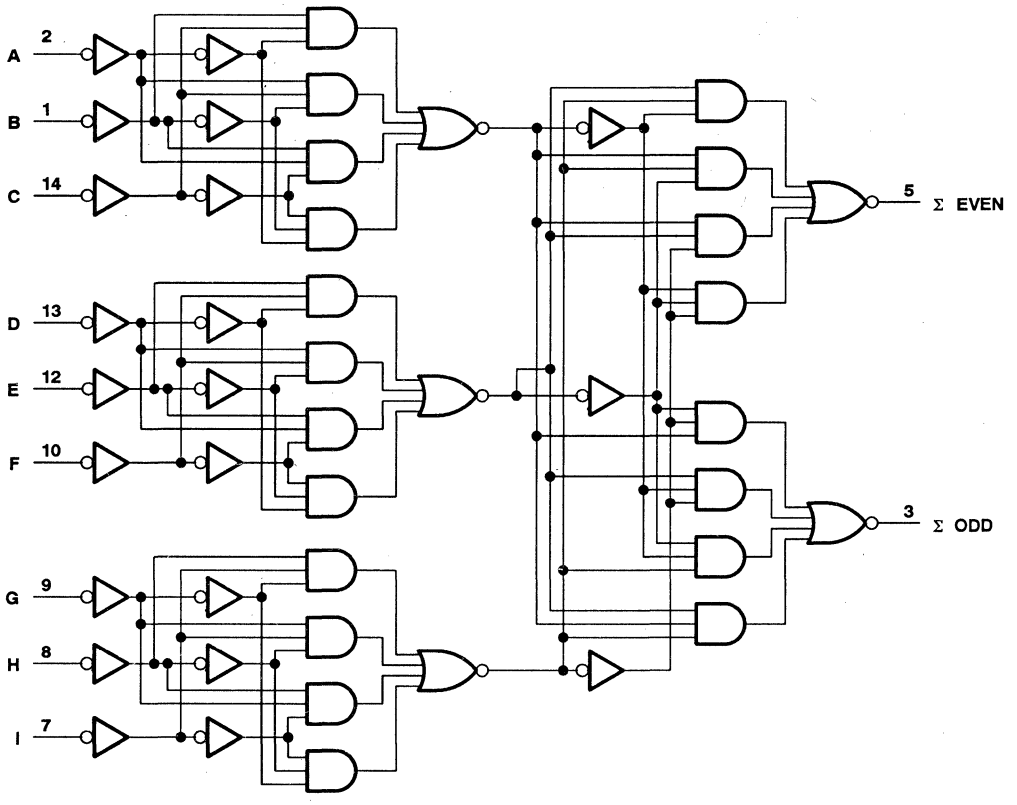
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	Any input	EVEN	1.5	9.8	13.5	1.5	14.9	ns
t_{PHL}			1.5	10.5	13.9	1.5	15.4	
t_{PLH}	Any input	ODD	1.5	9.9	13.8	1.5	15.1	ns
t_{PHL}			1.5	10.6	14.4	1.5	15.6	

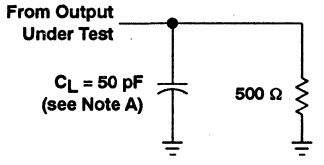
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	Any input	EVEN	1.5	5.9	9.1	1.5	10.1	ns
t_{PHL}			1.5	6.7	9.9	1.5	10.9	
t_{PLH}	Any input	ODD	1.5	6	9.3	1.5	10.3	ns
t_{PHL}			1.5	6.8	10.3	1.5	11.1	

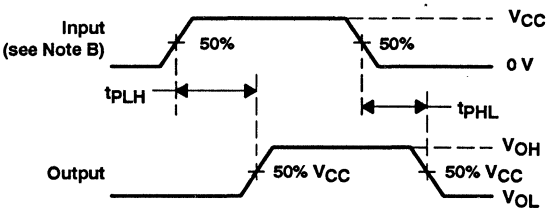
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	68	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

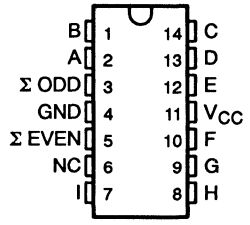
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

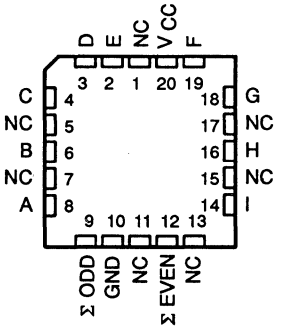
SCAS046A – D3148, AUGUST 1988 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11280 . . . J PACKAGE
74ACT11280 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11280 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

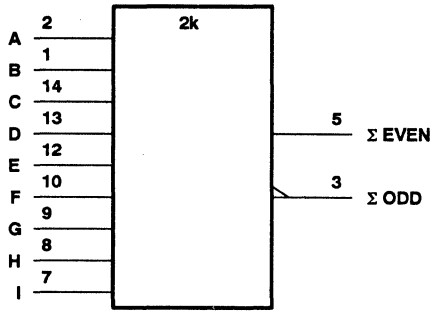
These universal, monolithic, 9-bit parity generators/checkers feature odd and even outputs to facilitate operation of either an odd or even parity application. The word-length capability is easily expanded by cascading.

The 54ACT11280 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11280 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

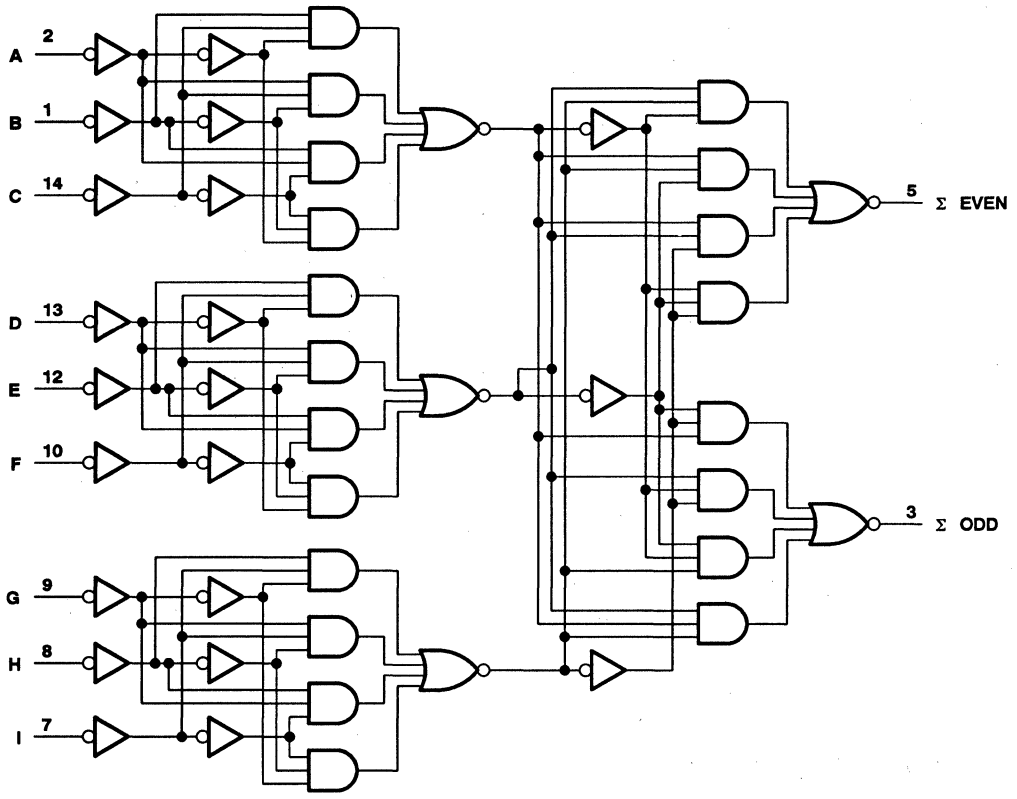
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	± 00 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11280		74ACT11280		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11280		74ACT11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.60			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output should be tested at a time and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

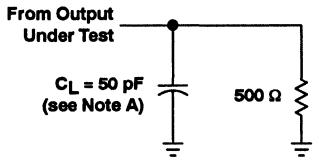
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11280		74ACT11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any input	Σ EVEN	1.5	7.3	10.8	1.5	13.1	1.5	12.2	ns
t_{PHL}			1.5	8.8	12.5	1.5	15.6	1.5	14.3	
t_{PLH}	Any input	Σ ODD	1.5	7.3	10.8	1.5	12.9	1.5	12.1	ns
t_{PHL}			1.5	8.6	12.4	1.5	15.7	1.5	14.3	

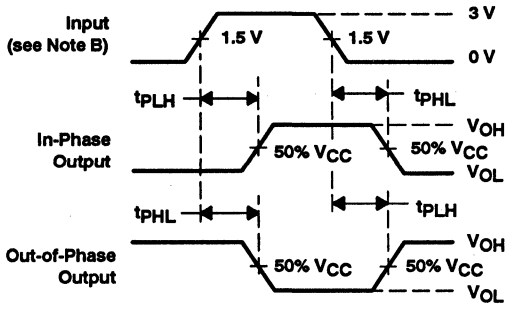
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	56	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



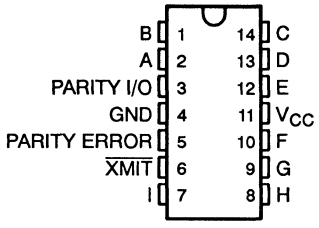
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Direct Bus Connection for Parity Generation or for Checking by Using the Parity I/O Port**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The 74AC11286 universal 9-bit parity generator/checker features a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When the $\overline{\text{XMIT}}$ is low, the parity tree is disabled and the PARITY ERROR output will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. The PARITY ERROR output will indicate a parity error when either an even number of inputs (A through I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power up or power down to prevent bus glitches.

The 74AC11286 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$ INPUT	PARITY I/O	PARITY ERROR OUTPUT
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

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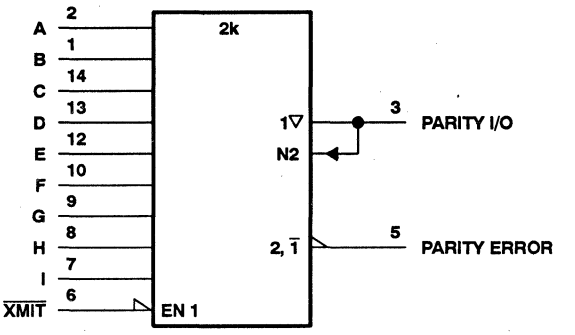
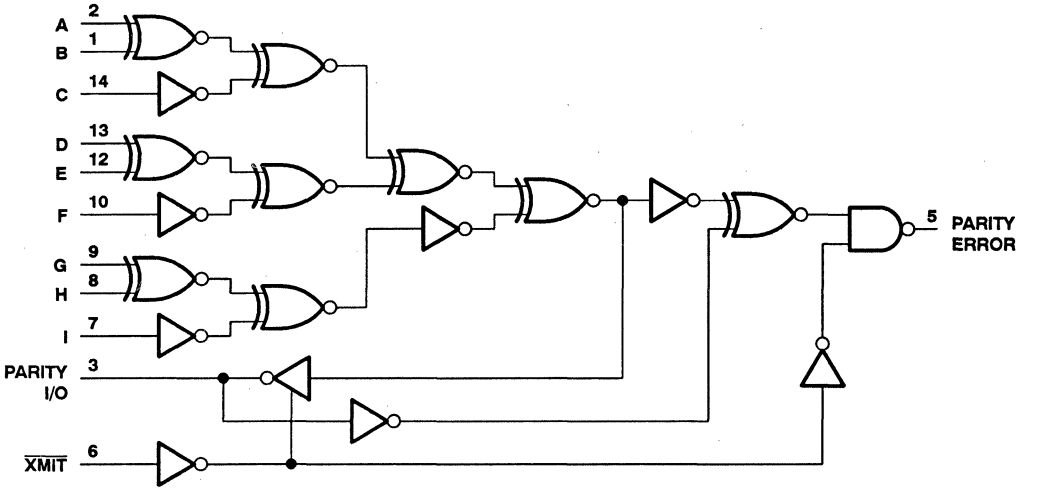
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3.5				pF
C_o	V_O = V_{CC} or GND	5 V		8.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	Any A thru I	PARITY I/O	2.6	10	11.7	2.6	13.1	ns
t_{PHL}			3.8	11.6	14.5	3.8	16.1	
t_{PLH}	Any A thru I	PARITY ERROR	3	8.5	13.1	3	14.7	ns
t_{PHL}			4	10.9	16	4	17.8	
t_{PLH}	PARITY I/O	PARITY ERROR	2.2	5.9	7.6	2.2	8.4	ns
t_{PHL}			3.4	7.9	10.2	3.4	11.1	
t_{PZH}	$\overline{XMIT}$	PARITY I/O	1.8	4.9	6.4	1.8	7	ns
t_{PZL}			3.5	9.7	12.8	3.5	13.6	
t_{PHZ}	$\overline{XMIT}$	PARITY I/O	3.2	5.4	6.6	3.2	7	ns
t_{PLZ}			3.2	5.4	6.7	3.2	7.2	

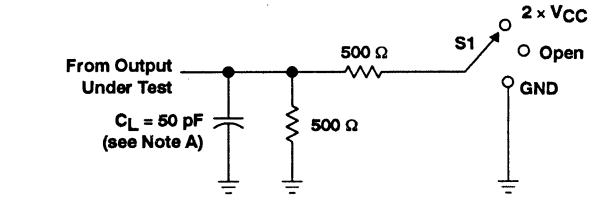
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	Any A thru I	PARITY I/O	2	5.5	8	2	9	ns
t_{PHL}			3.1	6.9	9.1	3.1	10.7	
t_{PLH}	Any A thru I	PARITY ERROR	2.5	5.2	8.9	2.5	10	ns
t_{PHL}			3.3	6.5	10.7	3.3	12	
t_{PLH}	PARITY I/O	PARITY ERROR	1.9	3.9	5.6	1.9	6.2	ns
t_{PHL}			2.9	5	7.2	2.9	7.9	
t_{PZH}	$\overline{XMIT}$	PARITY I/O	1.4	3.3	4.9	1.4	5.3	ns
t_{PZL}			3	5.4	8.3	3	8.9	
t_{PHZ}	$\overline{XMIT}$	PARITY I/O	3.1	4.8	6.1	3.1	6.5	ns
t_{PLZ}			3	4.6	6	3	6.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

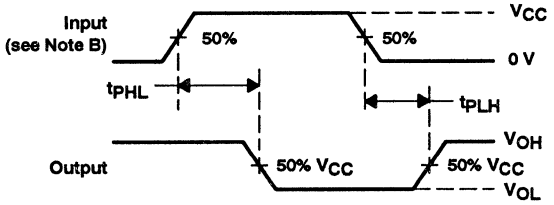
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	53	pF
		Outputs disabled		46	

PARAMETER MEASUREMENT INFORMATION

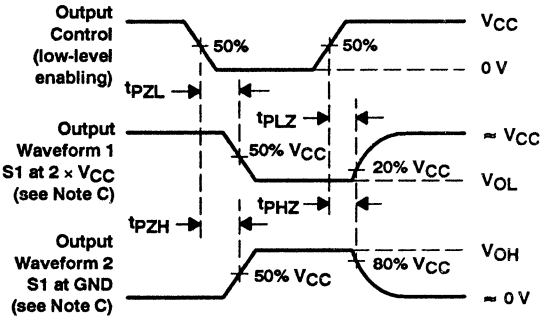


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



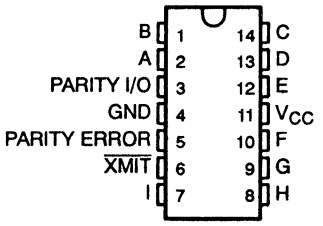
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The 74ACT11286 universal 9-bit parity generator/checker features a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When the $\overline{\text{XMIT}}$ is low, the parity tree is disabled and the PARITY ERROR output will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. The PARITY ERROR output will indicate a parity error when either an even number of inputs (A through I) are high and PARITY I/O is forced to a low logic level, or when an odd number of inputs are high and PARITY I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

The 74ACT11286 is characterized for operation from – 40°C to 85°C.

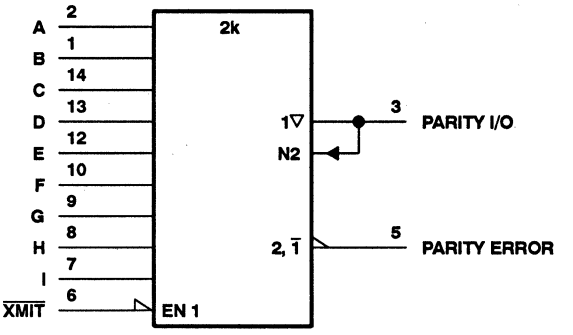
FUNCTION TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$ INPUT	PARITY I/O	PARITY ERROR OUTPUT
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h — high input level l — low input level
H — high output level L — low output level

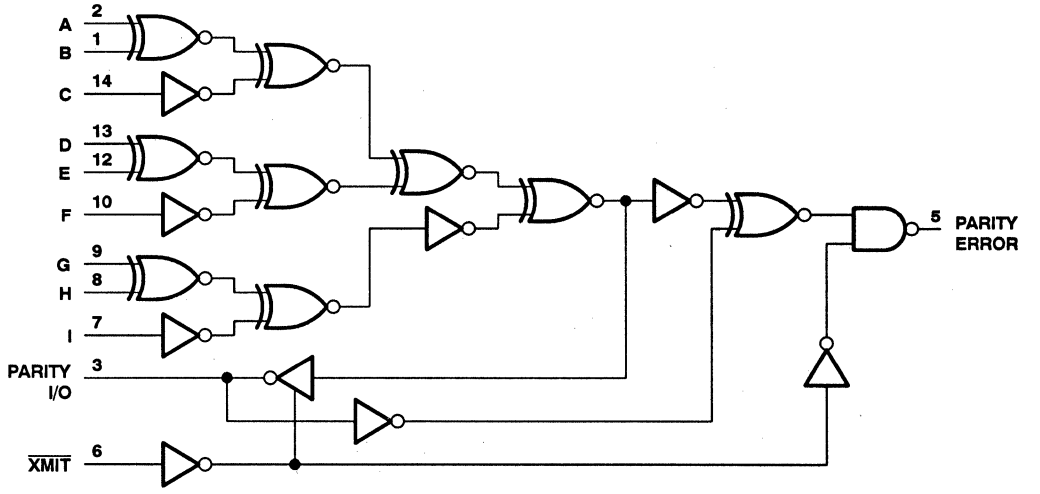
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_L = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	PARITY I/O	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_I	Except PARITY I/O	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i		$V_I = V_{CC}$ or GND	5 V		3.5				pF
C_o	PARITY I/O	$V_O = V_{CC}$ or GND	5 V		8				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

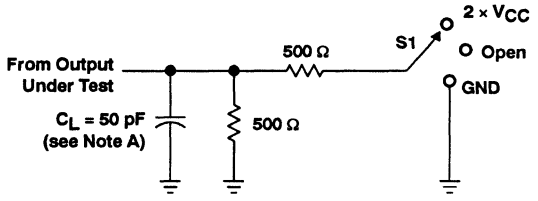
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	Any A thru I	PARITY I/O	2.7	6.1	9	2.7	10.4	ns
t_{PHL}			3.6	7.3	10.8	3.6	12	
t_{PLH}	Any A thru I	PARITY ERROR	3	6.9	9.7	3	11.3	ns
t_{PHL}			3.9	7.7	11.4	3.9	12.9	
t_{PLH}	PARITY I/O	PARITY ERROR	2.2	4.6	6.8	2.2	7.7	ns
t_{PHL}			3.1	5.6	8.3	3.1	9.1	
t_{PZH}	$\overline{XMIT}$	PARITY I/O	1.8	4.2	6.3	1.8	7.3	ns
t_{PZL}			3	6.3	9.4	3	11.4	
t_{PHZ}	$\overline{XMIT}$	PARITY I/O	4.7	6.5	7.9	4.7	8.5	ns
t_{PLZ}			4.1	6	7.3	4.1	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

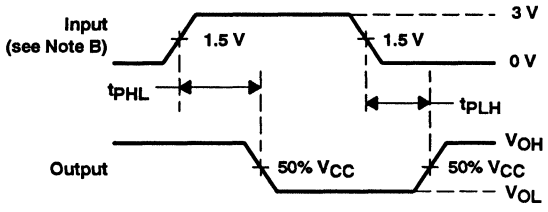
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	56	pF
		Outputs disabled		50	

PARAMETER MEASUREMENT INFORMATION

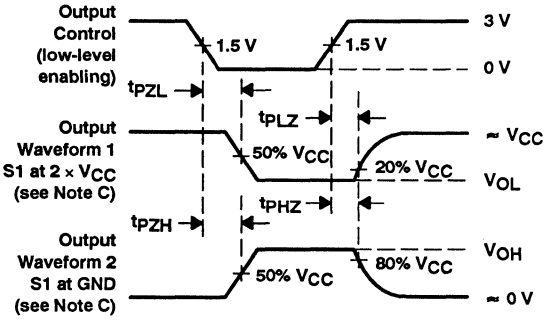


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



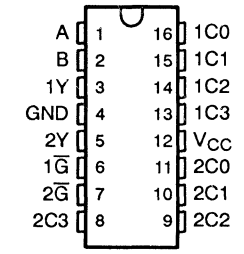
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

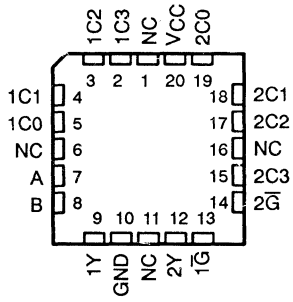
Figure 1. Load Circuit and Voltage Waveforms

- **Inverting Versions of 54ACT11253 and 74ACT11253**
- **Permits Multiplexing From N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11353 . . . J PACKAGE
74ACT11535 . . . D OR N PACKAGE
(TOP VIEW)



54ACT11353 . . . FK PACKAGE
(TOP VIEW)



description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

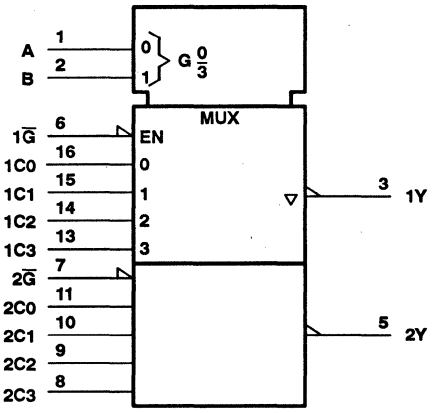
The 54ACT11353 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11353 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE $\overline{G}$	OUTPUT Y
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

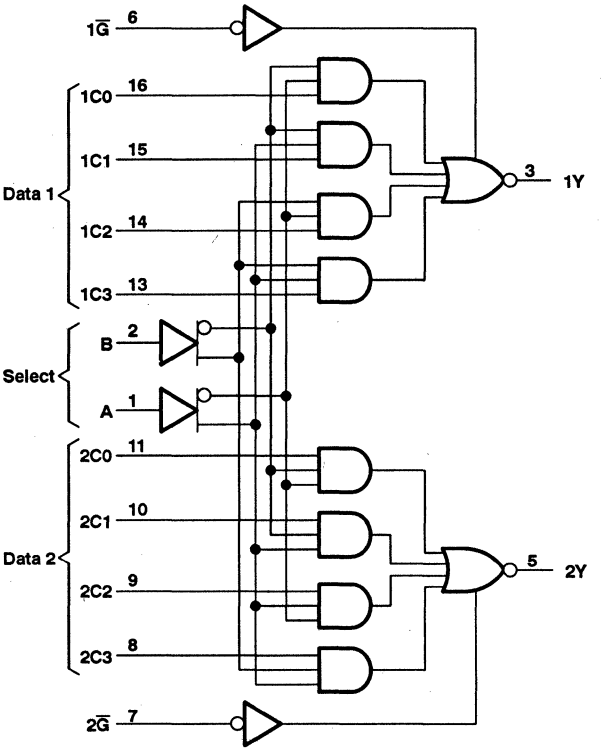
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11353		74ACT11353		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11353		74ACT11353		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		±5	µA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		8						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

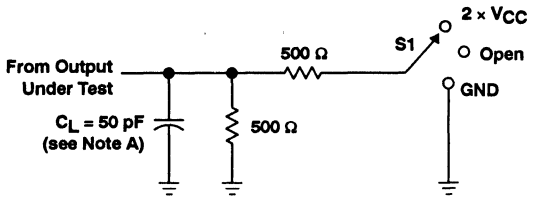
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11353		74ACT11353		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1.5	6.6	11.1	1.5	13.8	1.5	12.7	ns
t_{PHL}			1.5	5.9	8.3	1.5	10.1	1.5	9.4	
t_{PLH}	Data (Any C)	Any Y	1.5	6.3	9.8	1.5	12.3	1.5	11	ns
t_{PHL}			1.5	5.3	7.2	1.5	10.5	1.5	8	
t_{PZH}	$\overline{G}$	Any Y	1.5	4.3	6.8	1.5	7.9	1.5	7.4	ns
t_{PZL}			1.5	4.2	6.7	1.5	7.8	1.5	7.4	
t_{PHZ}	$\overline{G}$	Any Y	1.5	6.1	7.8	1.5	8.6	1.5	8.2	ns
t_{PLZ}			1.5	5.4	6.9	1.5	7.6	1.5	7.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

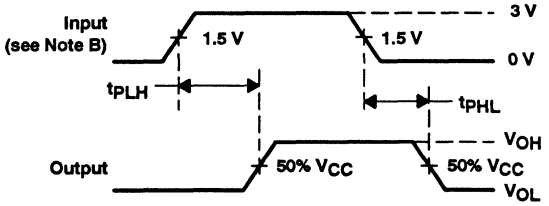
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	Outputs enabled	C_L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		19	

PARAMETER MEASUREMENT INFORMATION

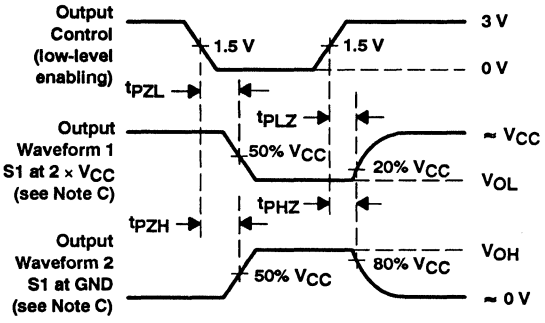


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



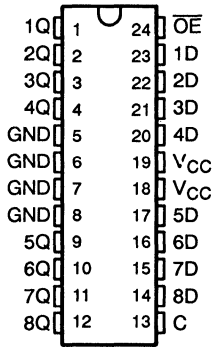
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

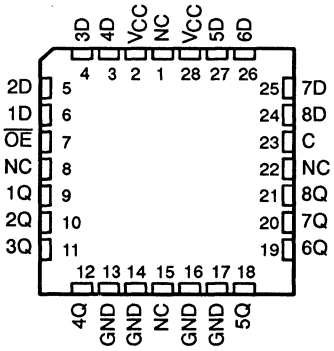
Figure 1. Load Circuit and Voltage Waveforms

- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11373 . . . JT PACKAGE
74AC11373 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54AC11373 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output enable $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

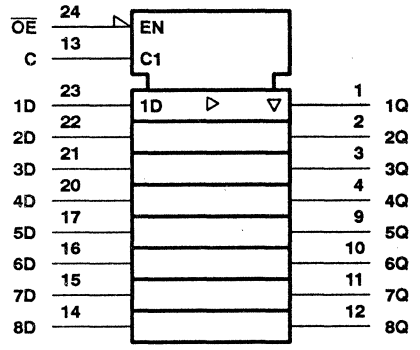
The 54AC11373 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11373 is characterized for operation from − 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

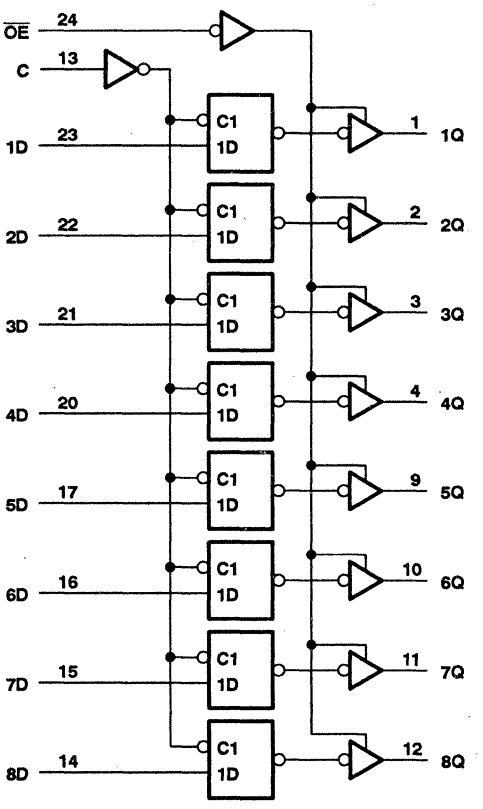
INPUTS			OUTPUT
$\overline{OE}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11373			74AC11373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OC}$	0		5	0		5	ns/V
		Data, C	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC11373		74AC11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	5.5		5.5		5.5		ns
t_{su}	Setup time, data before enable C↓	4		4		4		ns
t_h	Hold time, data after enable C↓	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC11373		74AC11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	4		4		4		ns
t_{su}	Setup time, data before enable C↓	3.5		3.5		3.5		ns
t_h	Hold time, data after enable C↓	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	9	13.1	1.5	15.7	1.5	14.8	ns
t_{PHL}			1.5	8	10.6	1.5	12.4	1.5	11.7	
t_{PLH}	C	Any Q	1.5	10	14.5	1.5	17.4	1.5	16.3	ns
t_{PHL}			1.5	9.5	12.8	1.5	15.2	1.5	14.2	
t_{PZH}	$\overline{OE}$	Any Q	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
t_{PZL}			1.5	8.5	11.6	1.5	14.1	1.5	13.1	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	9.5	12	1.5	13.1	1.5	12.7	ns
t_{PLZ}			1.5	7.5	10.2	1.5	11.3	1.5	10.8	

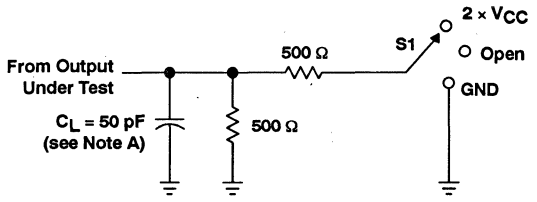
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11373		74AC11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	6	8.9	1.5	11.7	1.5	10.3	ns
t_{PHL}			1.5	5.5	7.6	1.5	9.1	1.5	8.4	
t_{PLH}	C	Any Q	1.5	6.5	10	1.5	12.1	1.5	11.3	ns
t_{PHL}			1.5	6.5	9.1	1.5	11	1.5	10.2	
t_{PZH}	$\overline{OE}$	Any Q	1.5	6.5	9.5	1.5	11.6	1.5	10.8	ns
t_{PZL}			1.5	6	8.6	1.5	10.9	1.5	9.7	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	8.5	10.6	1.5	11.5	1.5	11.1	ns
t_{PLZ}			1.5	6	8.2	1.5	9.1	1.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

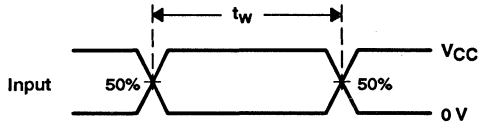
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		36	

PARAMETER MEASUREMENT INFORMATION

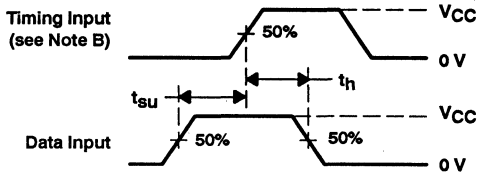


LOAD CIRCUIT

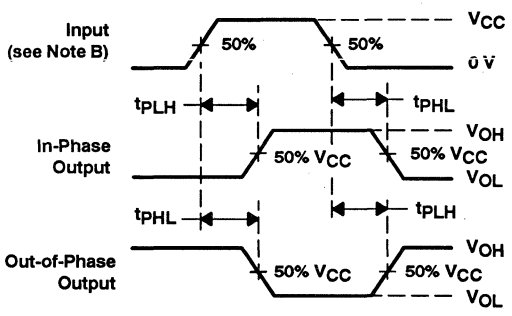
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



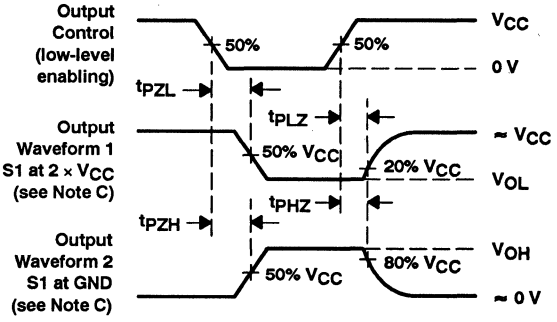
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



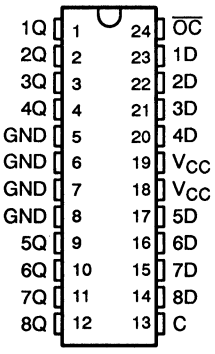
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

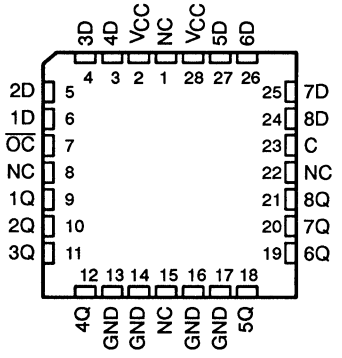
Figure 1. Load Circuit and Voltage Waveforms

- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11373 . . . JT PACKAGE
74ACT11373 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11373 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ACT11373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impendance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

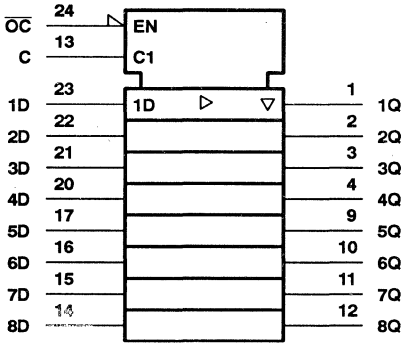
The 54ACT11373 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11373 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

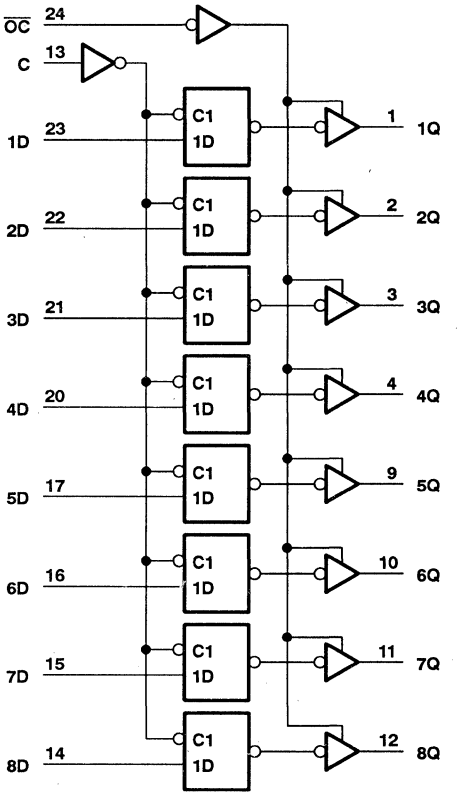
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 6 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 200 mA
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11373		74ACT11373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT11373		74ACT11373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, enable C high	5		6		5		ns
t_{su}	Setup time, data before enable C	3.5		3.5		3.5		ns
t_h	Hold time, data after enable C ↓	3.5		3.5		3.5		ns

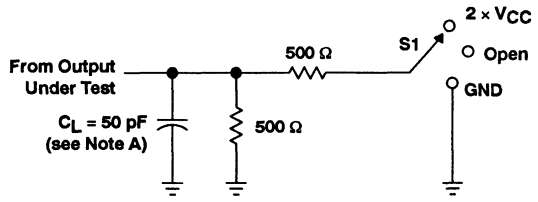
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11373		74ACT11373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	7.5	10.3	1.5	12.7	1.5	11.8	ns
t_{PHL}			1.5	6.5	9.3	1.5	10.6	1.5	10	
t_{PLH}	C	Any Q	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}			1.5	8.5	10.9	1.5	13	1.5	12.2	
t_{PZH}	$\overline{OC}$	Any Q	1.5	7	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}			1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	10	12.1	1.5	12.7	1.5	12.2	ns
t_{PLZ}			1.5	7.5	9.5	1.5	10.5	1.5	10.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

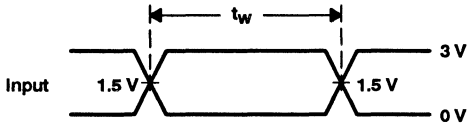
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	65	pF
		Outputs disabled		54	

PARAMETER MEASUREMENT INFORMATION

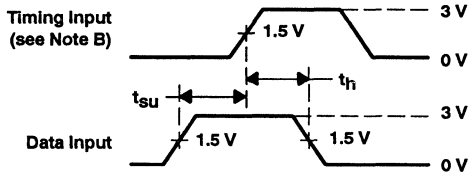


LOAD CIRCUIT

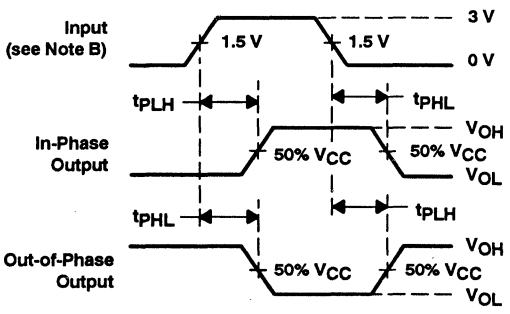
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



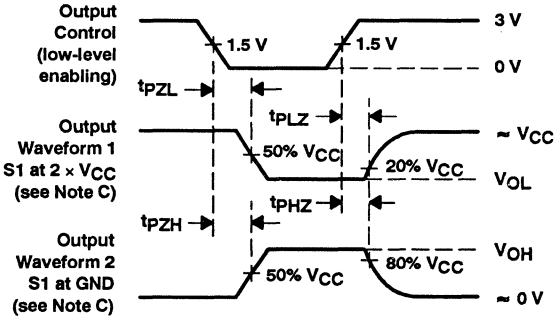
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



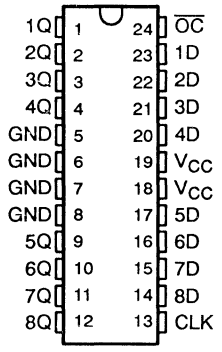
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

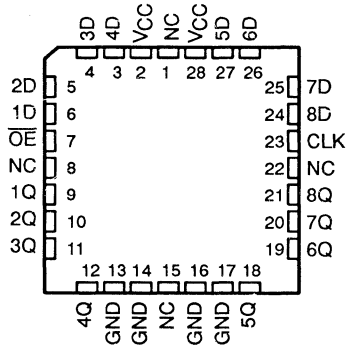
Figure 1. Load Circuit and Voltage Waveforms

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11374 . . . JT PACKAGE
74AC11374 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54AC11374 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ACT11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines signigicantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

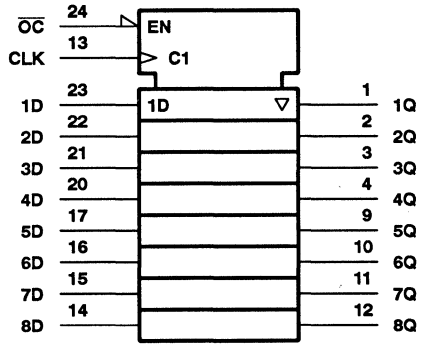
The 54AC11374 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11374 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

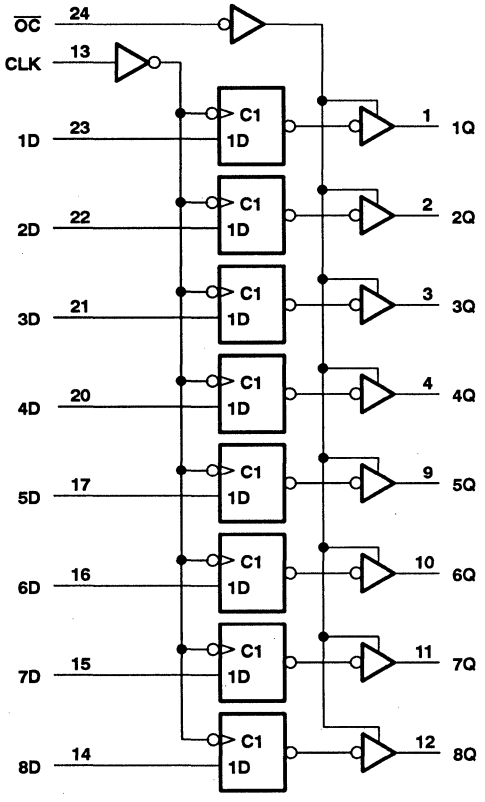
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
L	H	X	Q_O
L	↓	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11374			74AC11374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		$\overline{OC}$	0		5	0		5	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11374		74AC11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11374		74AC11374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	75	0	75	0	75	MHz
t_w	Pulse duration	CLK low or high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK↑		2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑		4.5		4.5		4.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54AC11374		74AC11374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	95	0	95	0	95	MHz
t_w	Pulse duration	CLK low or high	5		5		5		ns
t_{su}	Setup time, data before CLK↑		2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑		3.5		3.5		3.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11374		74AC11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75	90		75		75		MHz
t_{PLH}	CLK	Any Q	1.5	9.5	12.5	1.5	15.2	1.5	14.2	ns
t_{PHL}			1.5	9	12.6	1.5	14.9	1.5	14	
t_{PZH}	$\overline{OC}$	Any Q	1.5	8	10.9	1.5	13.3	1.5	12.3	ns
t_{PZL}			1.5	8	11.1	1.5	13.2	1.5	12.3	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	10	12.1	1.5	12.9	1.5	12.5	ns
t_{PLZ}			1.5	8	10.7	1.5	12.1	1.5	11.6	

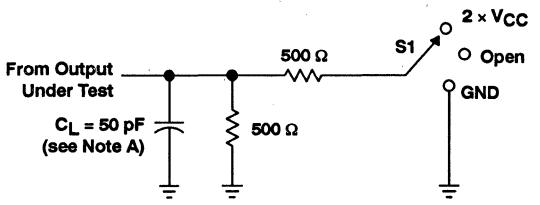
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11374		74AC11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			95	110		95		95		MHz
t_{PLH}	CLK	Any Q	1.5	6.5	9	1.5	10.9	1.5	10.2	ns
t_{PHL}			1.5	5.5	9.1	1.5	10.8	1.5	10.1	
t_{PZH}	$\overline{OC}$	Any Q	1.5	5.5	8	1.5	9.8	1.5	9.1	ns
t_{PZL}			1.5	5.5	8.4	1.5	10.2	1.5	9.4	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	9	11	1.5	11.4	1.5	11.2	ns
t_{PLZ}			1.5	6	8.6	1.5	9.6	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

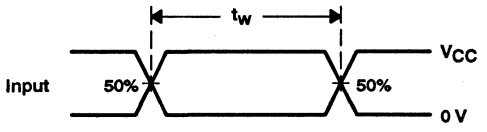
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	75	pF
		Outputs disabled		66	

PARAMETER MEASUREMENT INFORMATION

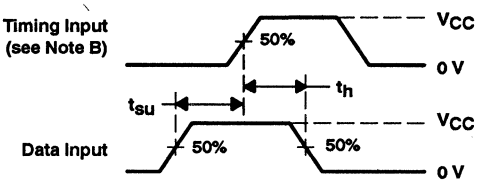


LOAD CIRCUIT

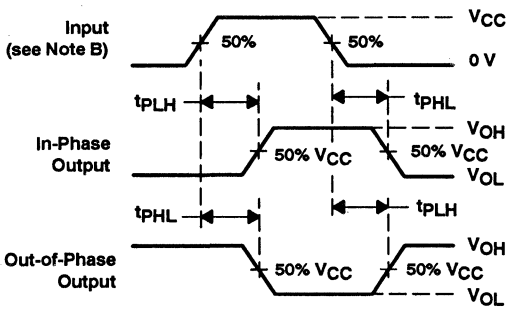
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



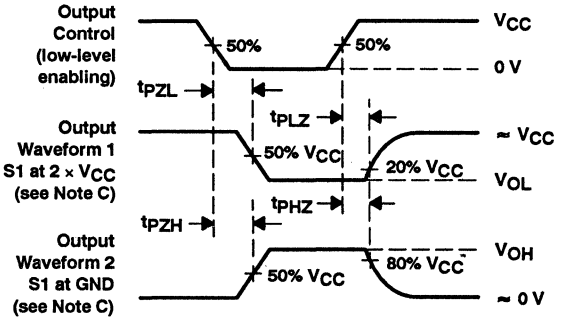
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



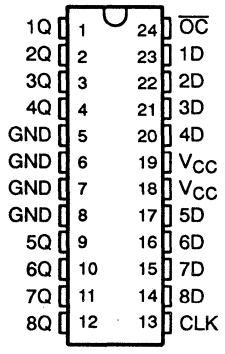
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

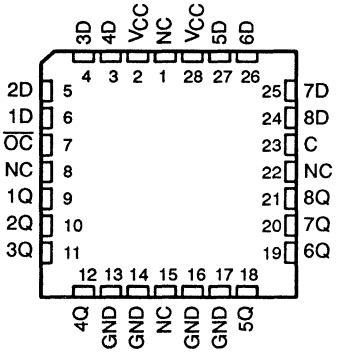
Figure 1. Load Circuit and Voltage Waveforms

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11374 . . . JT PACKAGE
74ACT11374 . . . DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11374 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ACT11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

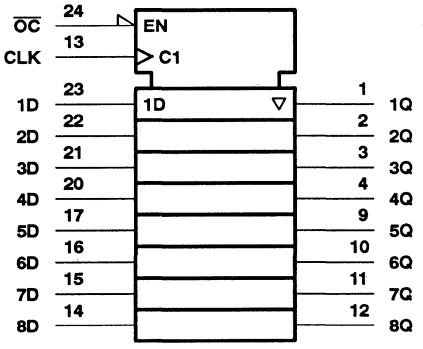
The 54ACT11374 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11374 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

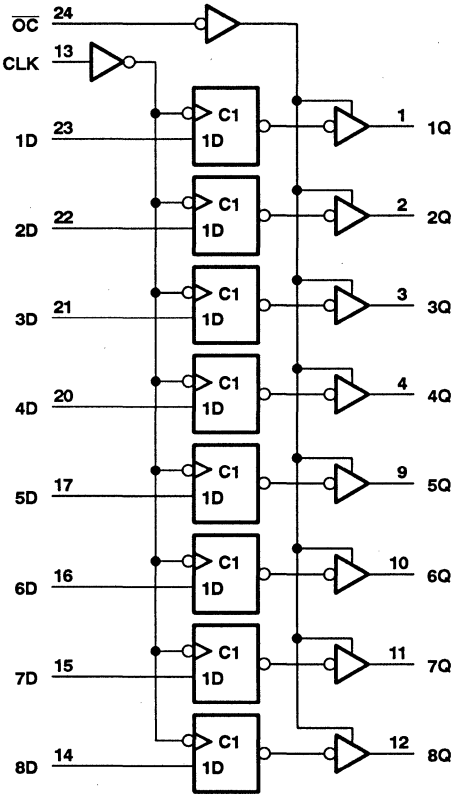
INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
L	H	X	Q_O
L	↓	X	Q_O
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11374		74ACT11374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns /V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltages and operating free-air temperature (unless otherwise notes) (see Figure 1)

		T_A = 25°C		54ACT11374		74ACT11374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	55	0	55	0	55	MHz
t_w	Pulse duration, CLK low or CLK high	9		9		9		ns
t_{su}	Setup time, data before CLK↑	3		3		3		ns
t_h	Hold time, data after CLK↑	5.5		5.5		5.5		ns

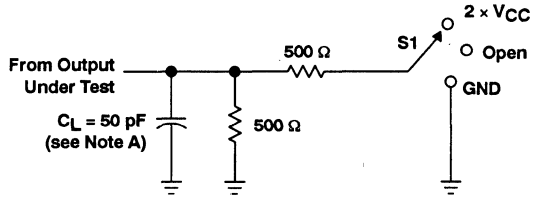
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11374		74ACT11374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55	70		55		55		MHz
t_{PLH}	CLK	Any Q	1.5	8.5	10.7	1.5	13.3	1.5	12.4	ns
t_{PHL}			1.5	8.5	11.3	1.5	13.9	1.5	13	
t_{PZH}	$\overline{OC}$	Any Q	1.5	7.5	11	1.5	13.2	1.5	12.3	ns
t_{PZL}			1.5	7.5	11	1.5	13.2	1.5	12.3	
t_{PHZ}	$\overline{OC}$	Any Q	1.5	11	12.7	1.5	13.6	1.5	13.2	ns
t_{PLZ}			1.5	8	10	1.5	11.3	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

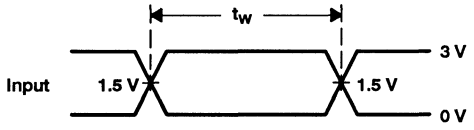
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	107	pF
		Outputs disabled		96	

PARAMETER MEASUREMENT INFORMATION

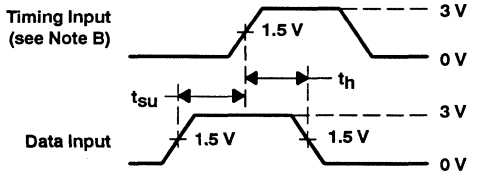


LOAD CIRCUIT

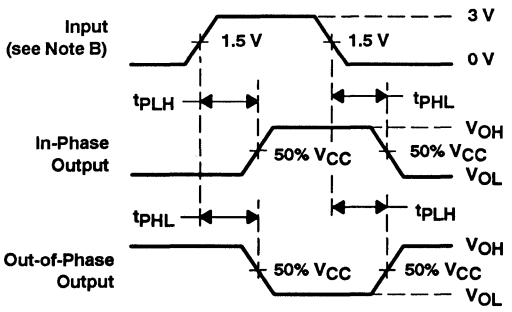
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



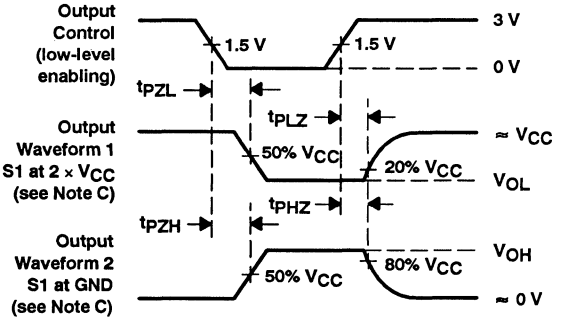
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



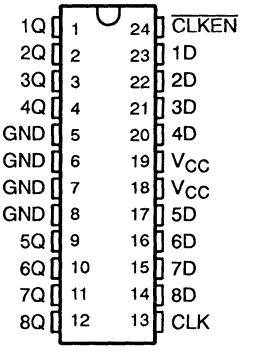
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Contains Eight D-Type Flip-Flops**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a clock enable input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{\text{CLKEN}}$ input.

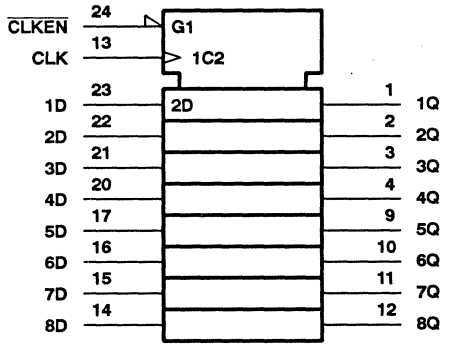
The 74AC11377 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

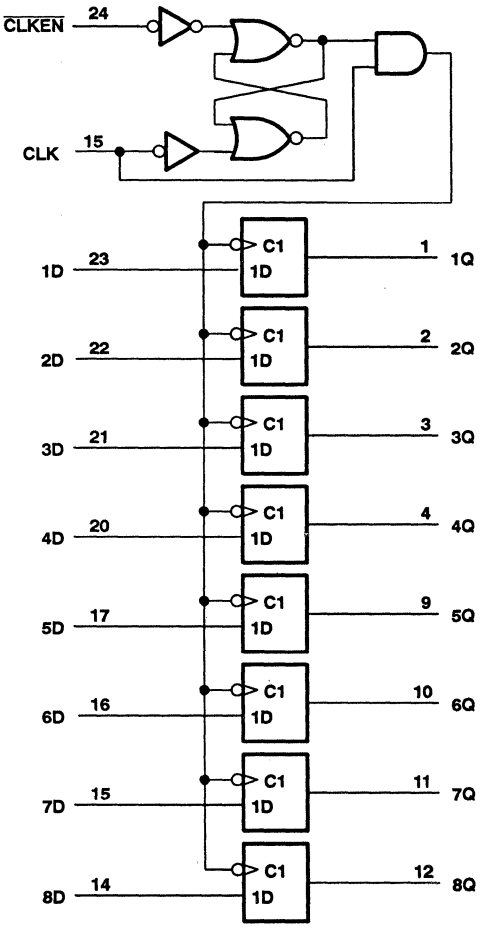
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 200 mA
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	60	0	60	MHz
t_w	Pulse duration	CLK high	5		5		ns
		CLK low	5		5		
t_{su}	Setup time before CLK↑	Data high	6		6		ns
		Data low	5		5		
		$\overline{CLKEN}$ high	9		9		
		$\overline{CLKEN}$ low	9		9		
t_h	Hold time after CLK↑	$\overline{CLKEN}$ inactive or active, data	0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high	5		5		ns
		CLK low	5		5		
t_{su}	Setup time before CLK↑	Data high or low	4		4		ns
		$\overline{CLKEN}$ high	6		6		
		$\overline{CLKEN}$ low	6		6		
t_h	Hold time after CLK↑	$\overline{CLKEN}$ inactive or active, data	0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			60			60		MHz
t_{PLH}	CLK	Any Q	4	9.8	15.7	4	17.9	ns
t_{PHL}			4.9	11.4	18	4.9	19.9	

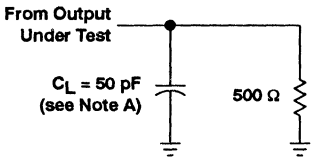
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100			100		MHz
t_{PLH}	CLK	Any Q	3.3	6.6	9.9	3.3	11.3	ns
t_{PHL}			4.1	7.8	11.5	4.1	12.9	

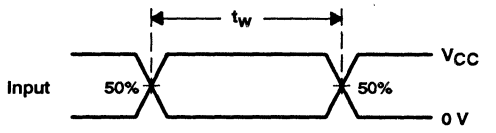
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	72	pF

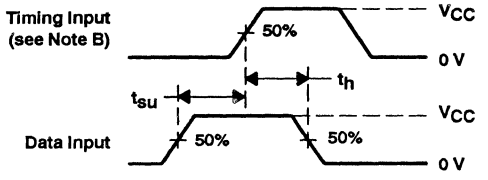
PARAMETER MEASUREMENT INFORMATION



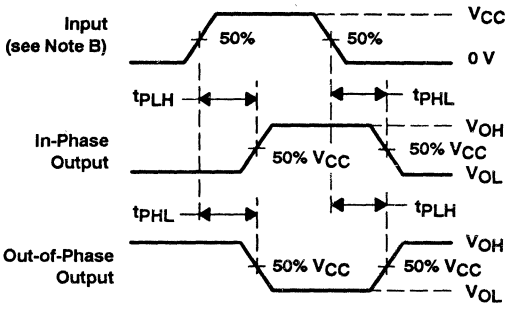
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



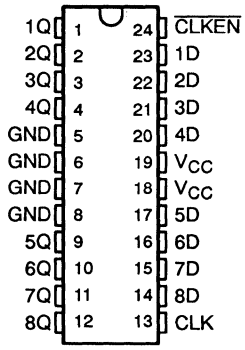
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Contains Eight D-Type Flip-Flops**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages and Standard Plastic 300-mil DIPs**

DB, DW OR NT PACKAGE
(TOP VIEW)



description

These circuits are positive-edge-triggered D-type flip-flops with a clock enable input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{\text{CLKEN}}$ input.

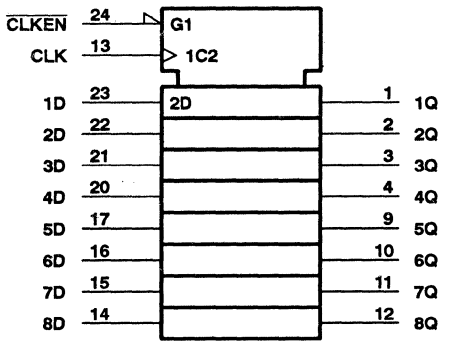
The 74ACT11377 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

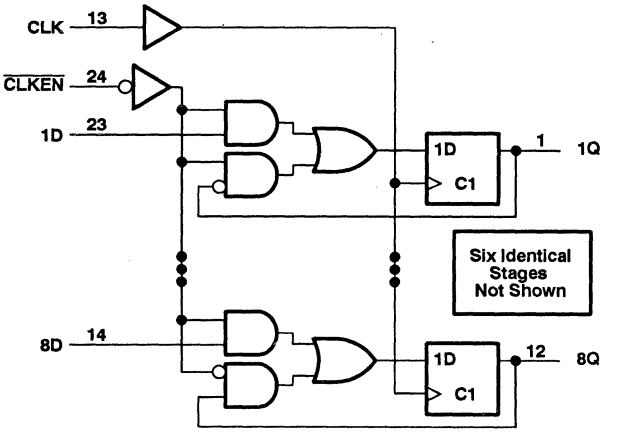
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = – 24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
V_{OL}	I_{OL} = 75 mA†		5.5 V					1.65	V
I_I	V_I = V_{CC} or GND		5.5 V			± 0.1		± 1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high	5		5		ns
		CLK low	5		5		
t_{su}	Setup time before CLK↑	Data	4		4		ns
		$\overline{CLKEN}$ high	4		4		
		$\overline{CLKEN}$ low	5		5		
t_h	Hold time after CLK↑	$\overline{CLKEN}$ high or low	0		0		ns
		Data high	1		1		
		Data low	0		0		

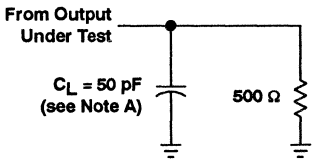
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100			100		MHz
t_{PLH}	CLK	Any Q	4.5	9.1	12.2	4.5	13.8	ns
t_{PHL}			4.8	9.6	12.7	4.8	14.2	

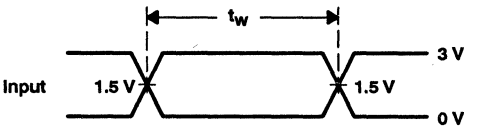
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	68	pF

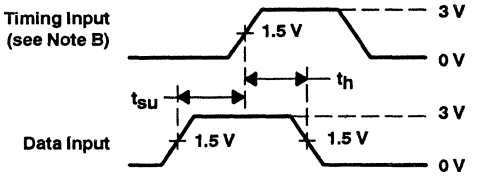
PARAMETER MEASUREMENT INFORMATION



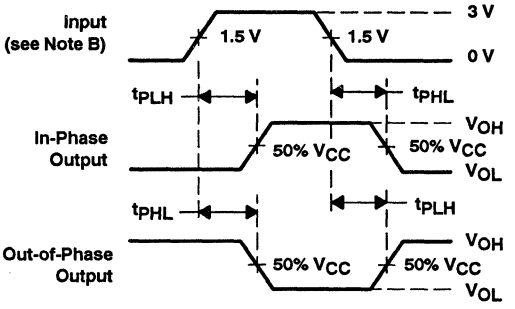
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



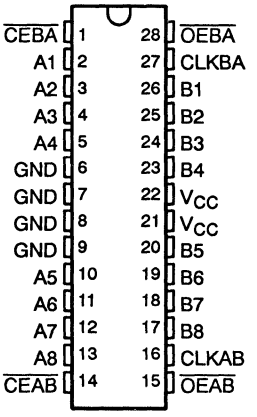
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

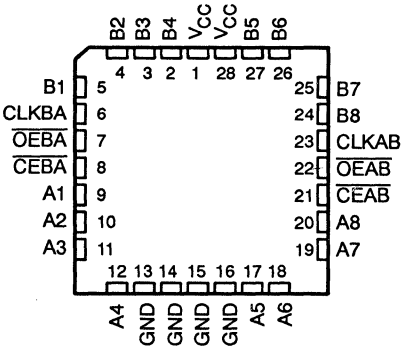
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

54ACT11470 . . . JT PACKAGE
74ACT11470 . . . DW PACKAGE
(TOP VIEW)



54AC11470 . . . FK PACKAGE
(TOP VIEW)



description

The 'ACT11470 is an 8-bit registered bus transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Separate clock (CLKAB or CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. If both $\overline{CEAB}$ and CLKAB are low, then the B port presents the level of the A port prior to the most recent low-to-high transition of CLKAB. Data flow from B to A is similar, but requires the use of $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$ inputs.

To avoid false clocking of the flip-flops, $\overline{CEAB}$ and $\overline{CEBA}$ should not be switched from low to high while CLK is low.

The 54ACT11470 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11470 is characterized for operation from −40°C to 85°C.

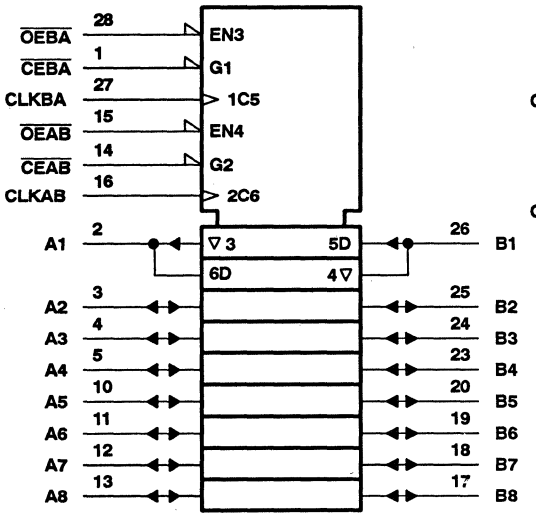
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H

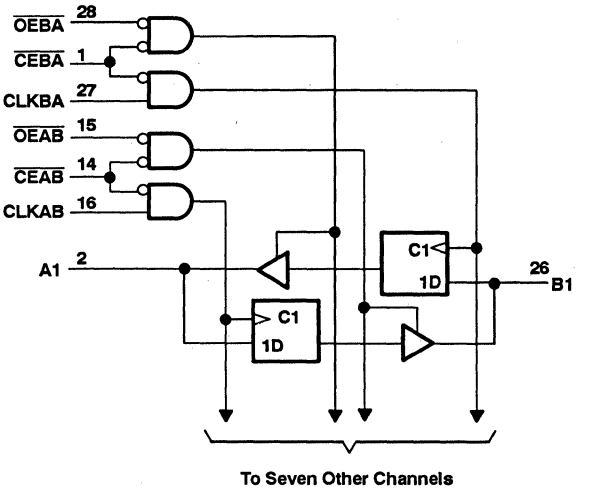
† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT11470			74ACT11470			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11470		74ACT11470		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = − 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = − 50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT11470		74ACT11470		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration	CLK high or low	5.5		5.5		5.5		ns
t_{su}	Setup time	Data before CLK↑	2				2		ns
		Data before $\overline{CEAB}$↑ or $\overline{CEBA}$↑	2				2		
t_h	Hold time	Data after CLK↑	3		3		3		ns
		Data after $\overline{CEAB}$↑ or $\overline{CEBA}$↑	3		3		3		

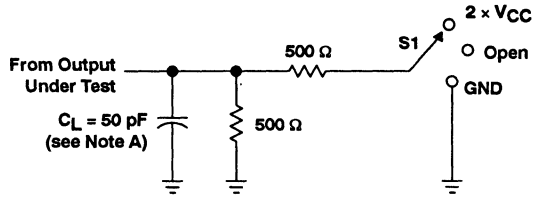
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11470		74ACT11470		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	CLKAB or CLKBA	A or B	3.4	7.3	9	3.4	10	3.4	10.1	ns
t_{PHL}			4.2	8.3	10.2	4.2	12	4.2	11.4	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	3	7	9.5	3	11.5	3	10.5	ns
t_{PZL}			4.3	8.6	11.4	4.3	15	4.3	13.7	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	4.5	7.9	9.6	4.5	11	4.5	10.5	ns
t_{PLZ}			5.1	7.7	9.5	5.1	10.7	5.1	10.2	
t_{PZH}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	3.4	7.3	10	3.4	12	3.4	11.1	ns
t_{PZL}			4.6	9	11.9	4.6	15.5	4.6	14.2	
t_{PHZ}	$\overline{CEAB}$ or $\overline{CEBA}$	B or A	4.8	7.9	9.9	4.8	11.4	4.8	10.9	ns
t_{PLZ}			5.1	7.9	9.8	5.1	11.2	5.1	10.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

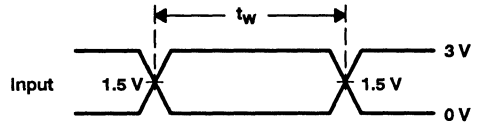
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		27	

PARAMETER MEASUREMENT INFORMATION

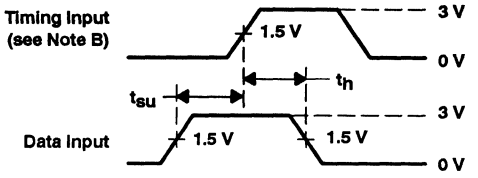


LOAD CIRCUIT

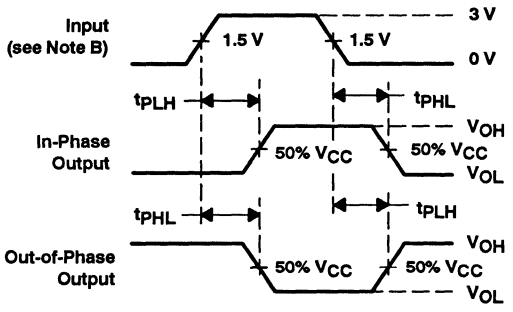
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



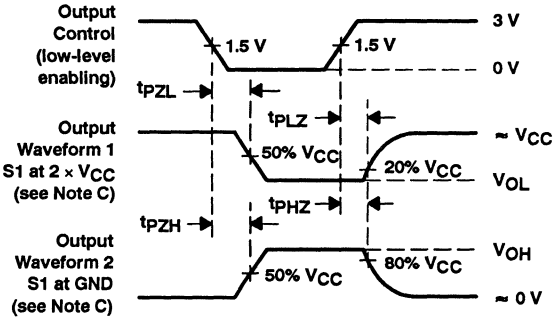
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

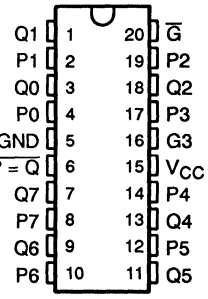
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

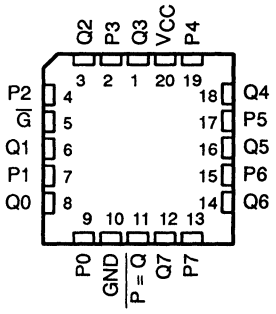
D2957, JULY 1987 – REVISED APRIL 1993

- **Compares Two 8-Bit Words**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **The Device Has the Equivalent of 20 kΩ Pullup Resistor on Q Inputs**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11520 . . . J PACKAGE
74AC11520 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11520 . . . FK PACKAGE
(TOP VIEW)



description

These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include 20-kΩ pullup termination resistors on the Q inputs for analog or switch data and a $\overline{P = Q}$ totem-pole output.

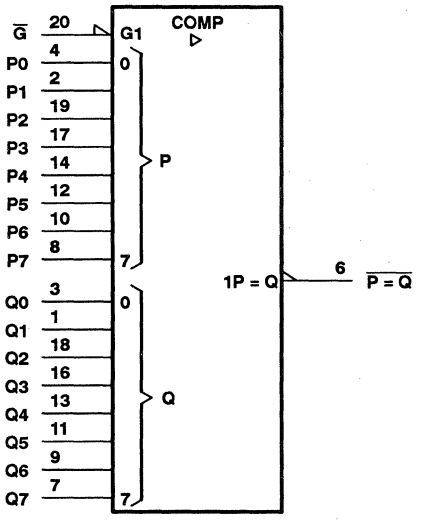
The 54AC11520 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11520 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

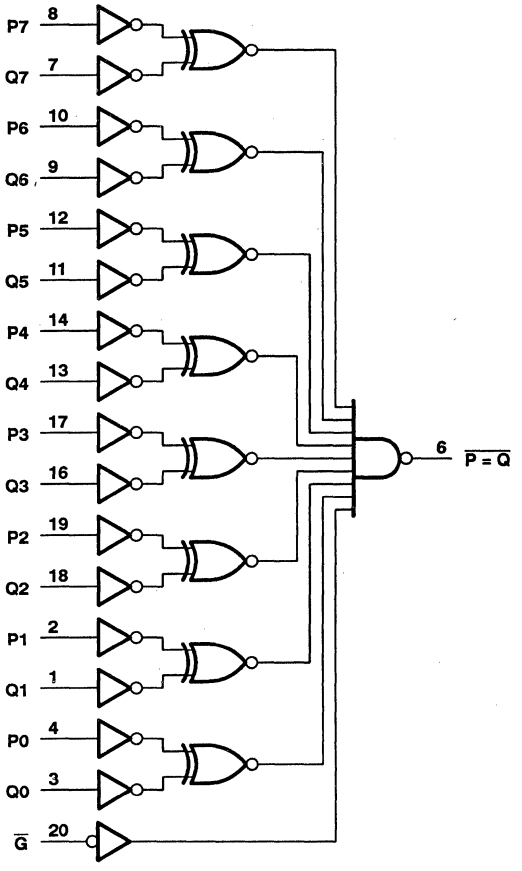
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



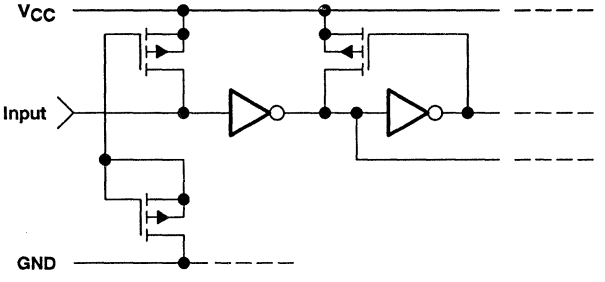
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, J, and N packages.

schematic of Q inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11520			74AC11520			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11520		74AC11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9	2.9		2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{IH}	$V_I = V_{CC}$, Q inputs only	5.5 V			10		10		10	μA
I_{IL}	V_I = GND, Q inputs only	5.5 V		– 0.3	– 0.6		– 1		– 1	mA
I_I	$V_I = V_{CC}$ or GND, P and $\overline{G}$ inputs only	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	Q inputs at GND Other inputs $V_I = V_{CC}$ or GND	5.5 V		2.3	4.8		8		8	mA
	Q inputs open Other inputs $V_I = V_{CC}$ or GND	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3.5						pF

† Not more than one output or input should be tested at a time and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11520		74AC11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	1.5	12	16.5	1.5	20.1	1.5	18.6	ns
t_{PHL}			1.5	10.4	14.4	1.5	17.6	1.5	16.3	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	1.5	6.9	9	1.5	10.8	1.5	10	ns
t_{PHL}			1.5	6.3	8.6	1.5	10.2	1.5	9.5	

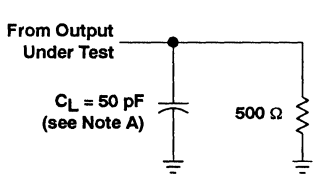
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11520		74AC11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	1.5	8.1	11.1	1.5	13.7	1.5	12.6	ns
t_{PHL}			1.5	7.1	10.1	1.5	12.3	1.5	11.3	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	1.5	4.9	6.6	1.5	8	1.5	7.4	ns
t_{PHL}			1.5	4.8	7.1	1.5	8.2	1.5	7.8	

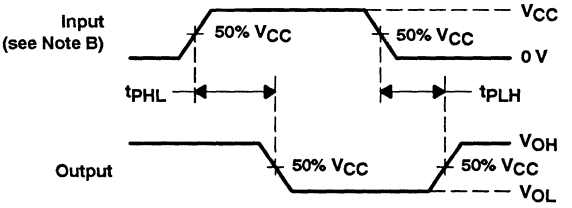
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

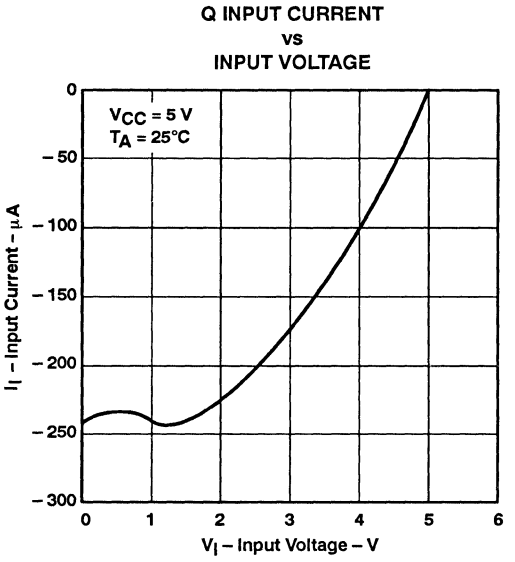
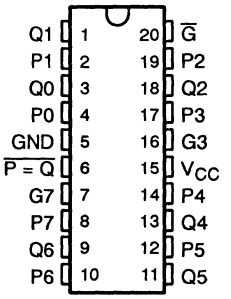


Figure 2

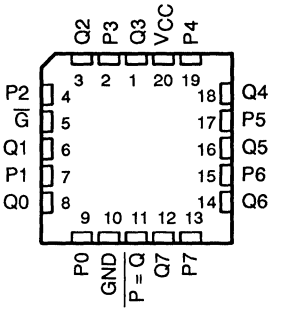
SCAS009B – D2957, JULY 1987 – REVISED APRIL 1993

- **Compares Two 8-Bit Words**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **The Device Has the Equivalent of 20-kΩ Pullup Resistors on Q Inputs**
- **Package Options Include Plastic Small- Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11520 . . . J PACKAGE
74ACT11520 . . . DW OR N PACKAGE
(TOP VIEW)



54ACT11520 . . . FK PACKAGE
(TOP VIEW)



description

These identity comparators perform comparisons on two 8-bit binary or BCD words. Features include 20-kΩ pullup termination resistors on the Q inputs for analog or switch data and a $\overline{P = Q}$ totem-pole output.

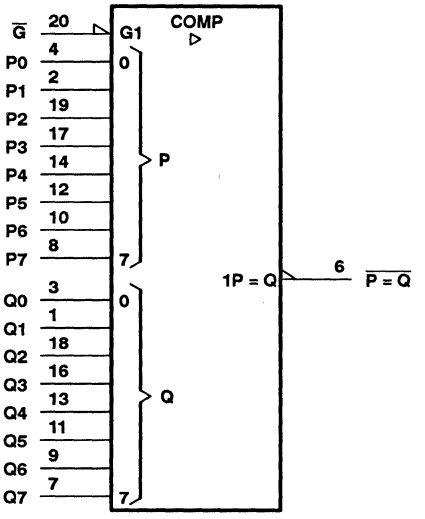
The 54ACT11520 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11520 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

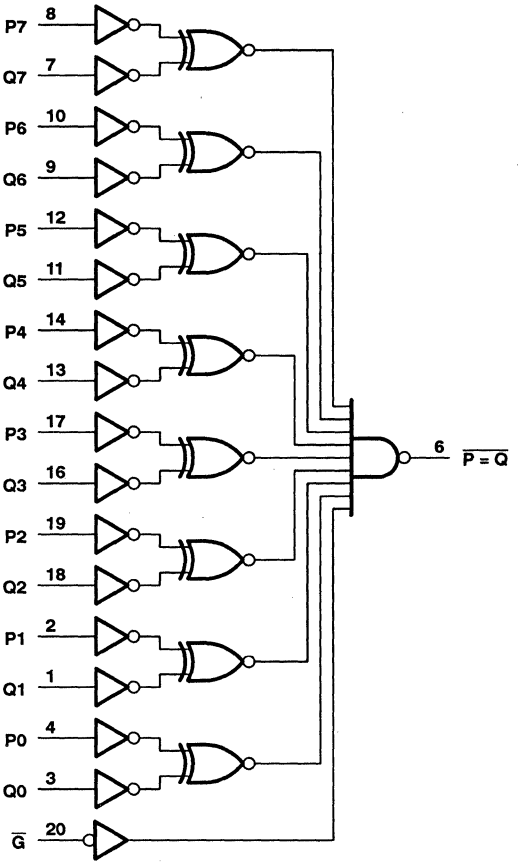
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



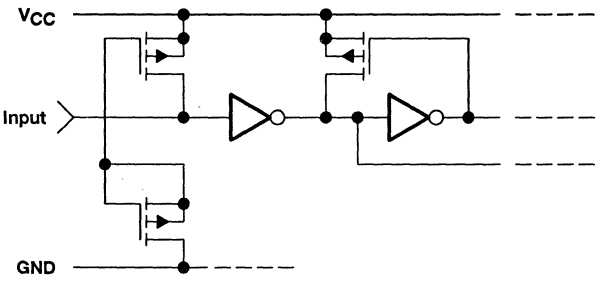
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, J, and N packages.

schematic of Q inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11520			74ACT11520			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−55		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{IH}	V_I = V_{CC}, Q inputs only	5.5 V			10		10		10	µA
I_{IL}	V_I = GND, Q inputs only	5.5 V		– 0.3	– 0.6		– 1		– 1	µA
I_I	V_I = V_{CC} or GND, P and $\overline{G}$ inputs only	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}	Q inputs at GND, Other inputs V_I = V_{CC} or GND	5.5 V		2.3	4.8		8		8	µA
	Q inputs at open, Other inputs V_I = V_{CC} or GND	5.5 V			8		160		80	µA
ΔI_{CC}‡	Q inputs open, One input at 3.4 V and other inputs at V_{CC} or GND, P and $\overline{G}$ inputs only	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

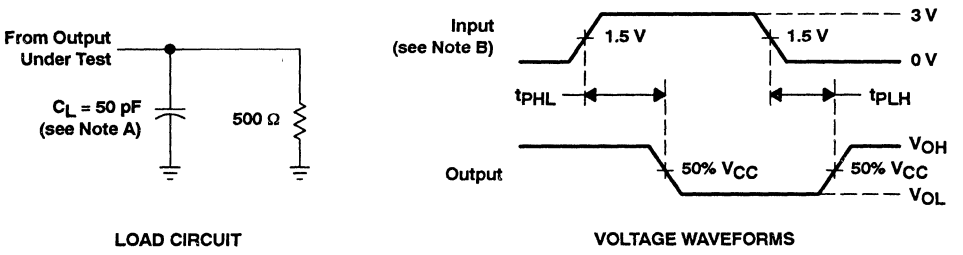
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11520		74ACT11520		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P = Q}$	1.5	8.6	12.7	1.5	15.4	1.5	14.3	ns
t_{PHL}			1.5	8	12.4	1.5	14.8	1.5	13.9	
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	1.5	6.4	8.5	1.5	10.2	1.5	9.5	ns
t_{PHL}			1.5	5.8	9	1.5	10.4	1.5	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

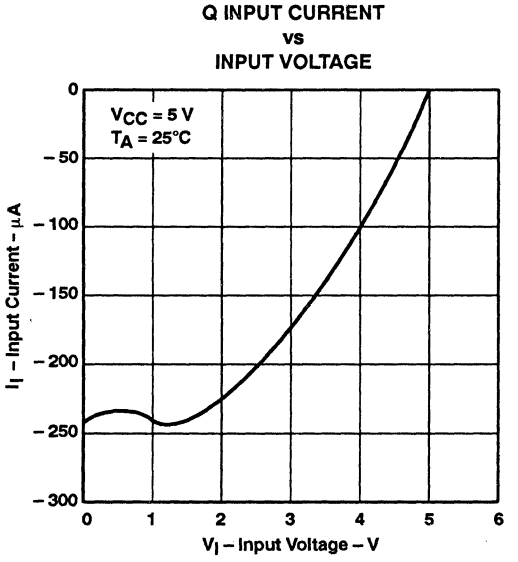
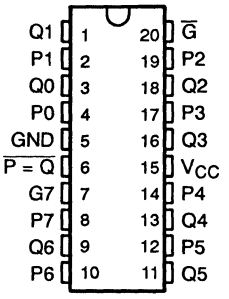


Figure 2

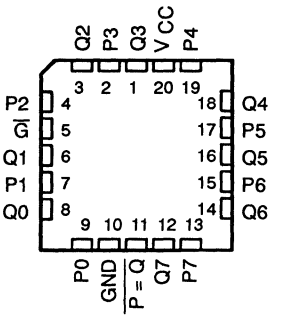
SCAS022A – D2957, JULY 1987 – REVISED APRIL 1993

- **Compares Two 8-Bit Words**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11521 . . . J PACKAGE
74AC11521 . . . DB, DW OR N PACKAGE
(TOP VIEW)



54AC11521 . . . FK PACKAGE
(TOP VIEW)



description

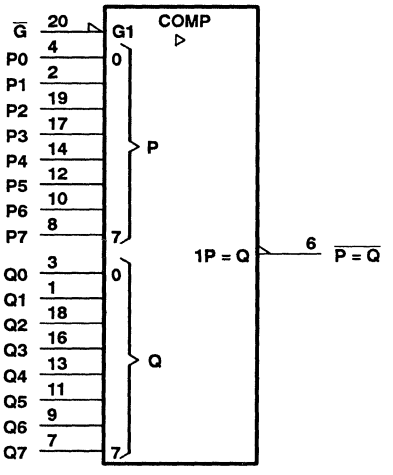
These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a $\overline{P = Q}$ totem-pole output.

The 54AC11521 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11521 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

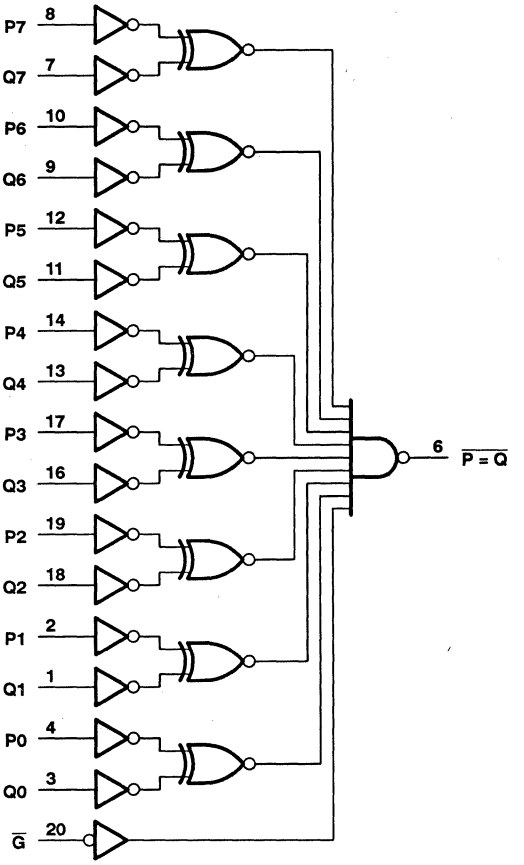
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins numbers shown are for the DW, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



Pin numbers shown are for the DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11521			74AC11521			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11521		74AC11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11521		74AC11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	1.5	12.5	16.6	1.5	20.4	1.5	19	ns
t_{PHL}			1.5	10.5	14.1	1.5	17.4	1.5	16.1	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	1.5	7.1	9.8	1.5	11.4	1.5	10.8	ns
t_{PHL}			1.5	6.4	8.8	1.5	10.8	1.5	10.1	

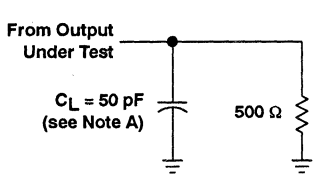
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11521		74AC11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	1.5	8.3	11.3	1.5	14	1.5	13	ns
t_{PHL}			1.5	7.2	10.1	1.5	12.2	1.5	11.4	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	1.5	5.1	7.1	1.5	8.4	1.5	7.9	ns
t_{PHL}			1.5	4.8	7.1	1.5	8.6	1.5	8.1	

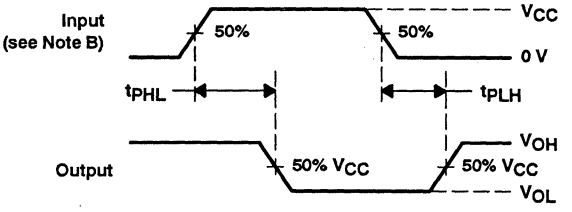
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	42	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



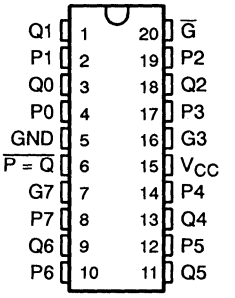
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

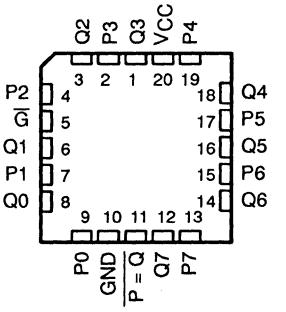
Figure 1. Load Circuit and Voltage Waveforms

- **Compares Two 8-Bit Words**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11521 . . . J PACKAGE
74ACT11521 . . . DB, DW OR N PACKAGE
(TOP VIEW)



54ACT11521 . . . FK PACKAGE
(TOP VIEW)



description

These identity comparators perform comparisons on two 8-bit binary or BCD words. Also included is a $\overline{P = Q}$ totem-pole output.

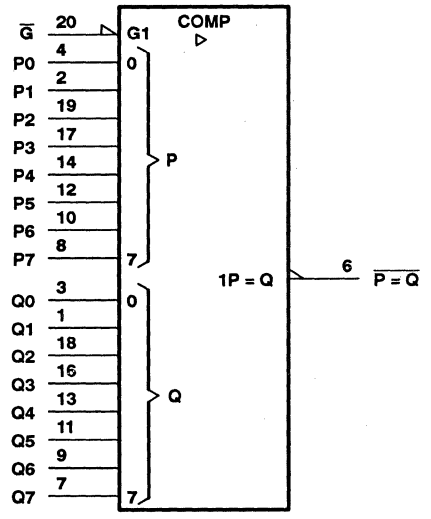
The 54ACT11521 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11521 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

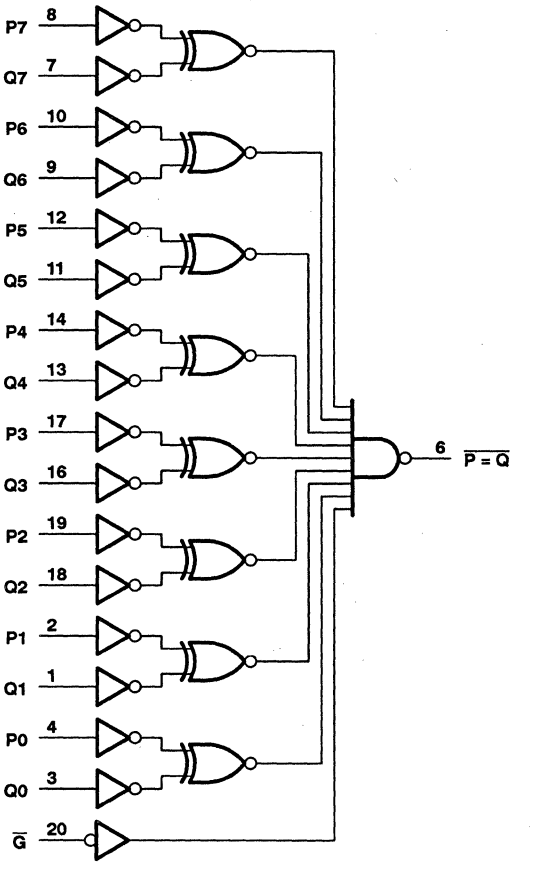
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 100 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11521			74ACT11521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

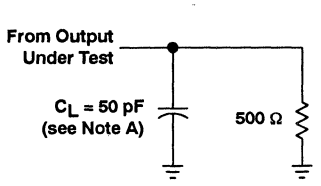
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11521		74ACT11521		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	P or Q	$\overline{P=Q}$	1.5	8.8	13	1.5	15.9	1.5	14.7	ns
t_{PHL}			1.5	8.2	12	1.5	14.6	1.5	13.6	
t_{PLH}	$\overline{G}$	$\overline{P=Q}$	1.5	6.7	9.3	1.5	11.2	1.5	10.5	ns
t_{PHL}			1.5	6.8	8.8	1.5	10.2	1.5	9.7	

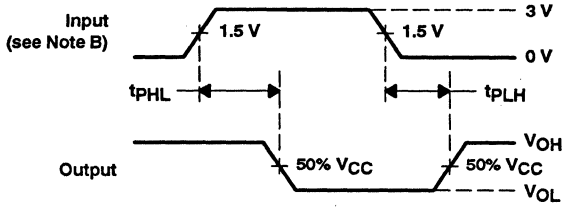
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



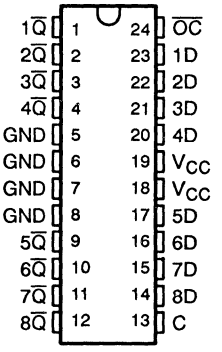
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

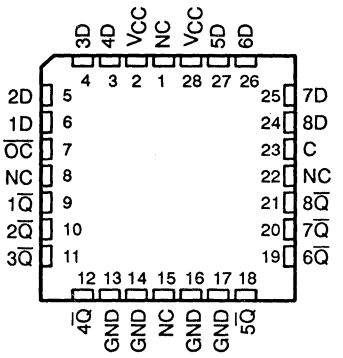
Figure 1. Load Circuit and Voltage Waveforms

- **8-Latches In a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11533 . . . JT PACKAGE
74AC11533 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11533 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'AC11533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the (D) inputs. When the output control $\overline{OC}$ is taken low, the $\overline{Q}$ outputs will be latched. The 'AC11533 is functionally equivalent to the 'AC11373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

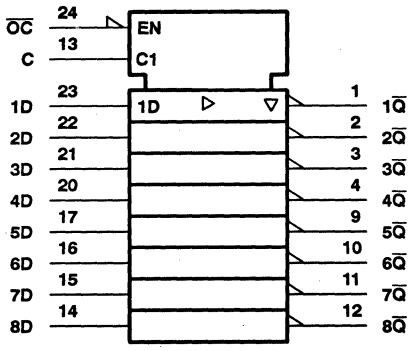
The 54AC11533 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11533 is characterized for operation from − 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each latch)

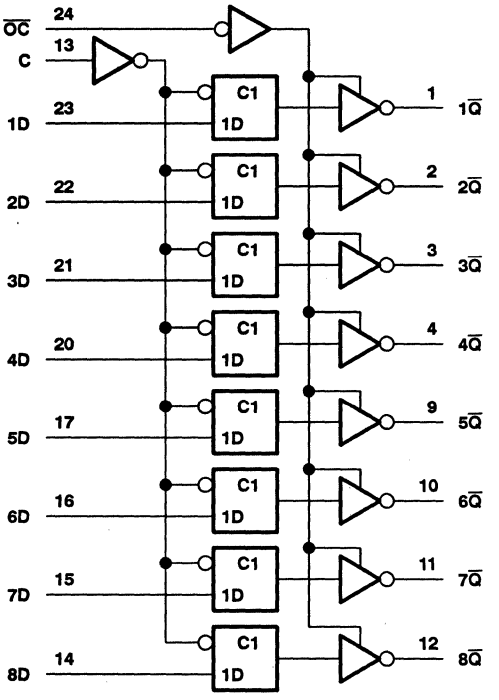
INPUTS			OUTPUT
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11533			74AC11533			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements (see Figure 1)

		V_{CC} RANGE	T_A = 25°C		54AC11533		74AC11533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	3.3 ± 0.3 V	5.5		5.5		5.5		ns
		5 ± 0.5 V	4		4		4		
t_{su}	Setup time, data before C	3.3 ± 0.3 V	4		4		4		ns
		5 ± 0.5 V	3.5		3.5		3.5		
t_h	Hold time, data after C↓	3.3 ± 0.3 V	2		2		2		ns
		5 ± 0.5 V	2		2		2		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	1.5	8.5	12.6	1.5	15.2	1.5	14.3	ns
t_{PHL}			1.5	7.5	10.1	1.5	12	1.5	11.3	
t_{PLH}	C	Any $\overline{Q}$	1.5	10	14.5	1.5	17.6	1.5	16.5	ns
t_{PHL}			1.5	9.5	12.8	1.5	15.2	1.5	14.3	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.5	9	13.1	1.5	15.7	1.5	14.7	ns
t_{PZL}			1.5	8.5	11.6	1.5	14.1	1.5	13.1	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.5	9.5	12	1.5	13.2	1.5	12.8	ns
t_{PLZ}			1.5	7.5	10.2	1.5	11.4	1.5	11	

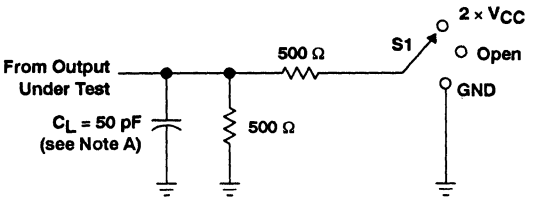
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11533		74AC11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	1.5	5.5	8.4	1.5	10.6	1.5	9.8	ns
t_{PHL}			1.5	5	7.1	1.5	8.6	1.5	8	
t_{PLH}	C	Any $\overline{Q}$	1.5	6.5	10	1.5	12.1	1.5	11.3	ns
t_{PHL}			1.5	6.5	9.1	1.5	11	1.5	10.3	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.5	6.5	9.5	1.5	11.7	1.5	10.8	ns
t_{PZL}			1.5	6	8.6	1.5	10.9	1.5	9.7	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.5	8.5	10.7	1.5	11.7	1.5	11.4	ns
t_{PLZ}			1.5	6	8.2	1.5	9.3	1.5	8.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

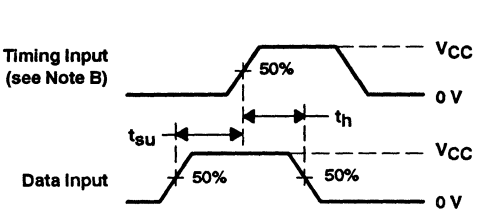
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		44	

PARAMETER MEASUREMENT INFORMATION

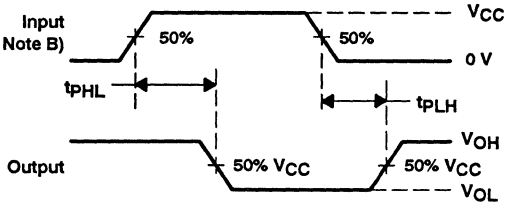


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

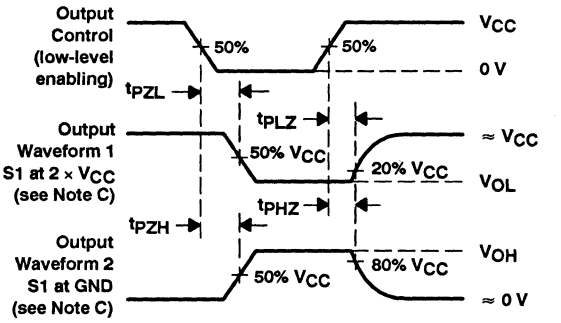
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Eight Latches in a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
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- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
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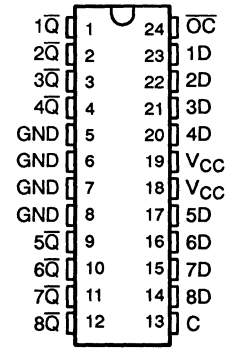
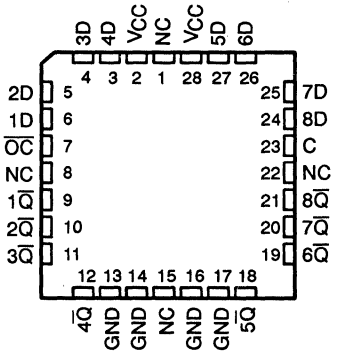
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11533 . . . JT PACKAGE
74ACT11533 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11533 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These eight latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'ACT11533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the (D) inputs. When the output control $\overline{OC}$ is taken low, the $\overline{Q}$ outputs will be latched. The 'ACT11533 is functionally equivalent to the 'ACT11373 except for having inverted outputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

The output control ($\overline{OC}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

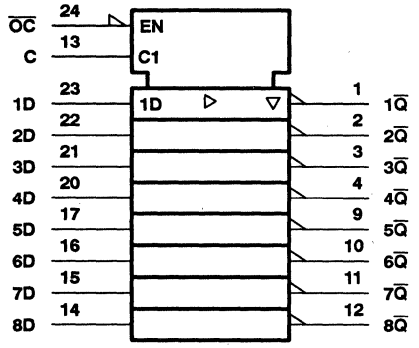
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

The 54ACT11533 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11533 is characterized for operation from − 40°C to 85°C.

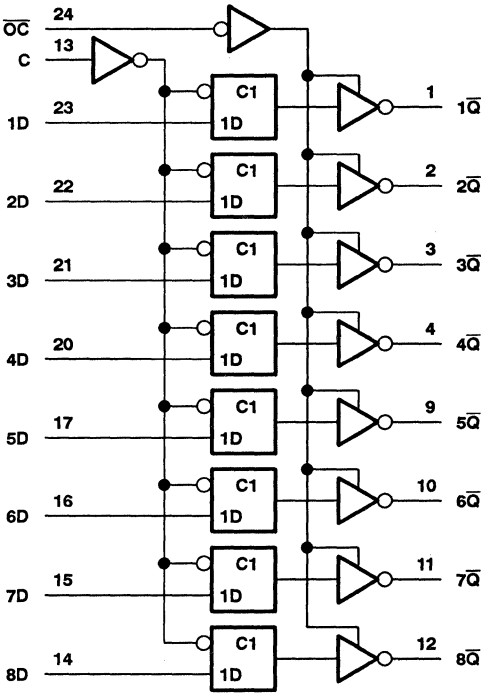
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT11533		74ACT11533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	5		5		5		ns
t_{su}	Setup time, data before C↓	3.5		3.5		3.5		ns
t_h	Hold time, data after C↓	3.5		3.5		3.5		ns

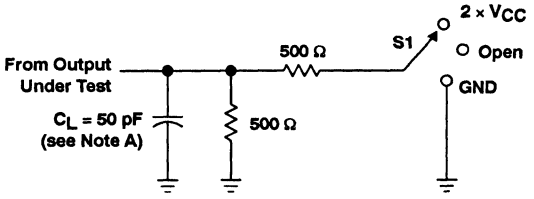
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11533		74ACT11533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$	1.5	7	10.1	1.5	11.9	1.5	11.3	ns
t_{PHL}			1.5	6.5	8.4	1.5	10.2	1.5	9.5	
t_{PLH}	C	Any $\overline{Q}$	1.5	8.5	11.3	1.5	14.1	1.5	13	ns
t_{PHL}			1.5	8.5	10.7	1.5	13.2	1.5	12.2	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.5	7.5	10.7	1.5	13.6	1.5	12.5	ns
t_{PZL}			1.5	7.5	10.9	1.5	12.9	1.5	12	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.5	10.5	12.1	1.5	13.1	1.5	12.8	ns
t_{PLZ}			1.5	7.5	9.5	1.5	10.7	1.5	10.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

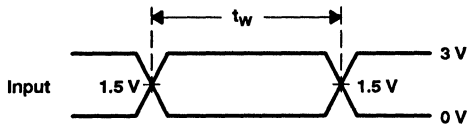
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	69	pF
		Outputs disabled		58	

PARAMETER MEASUREMENT INFORMATION

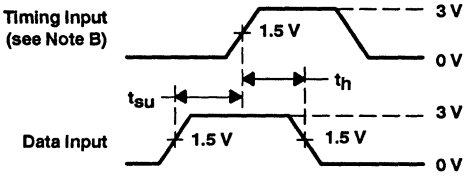


LOAD CIRCUIT

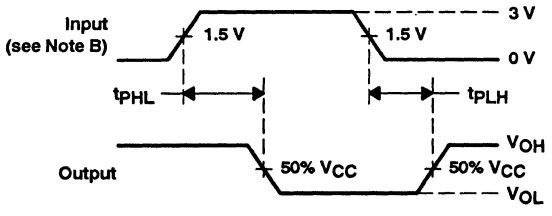
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



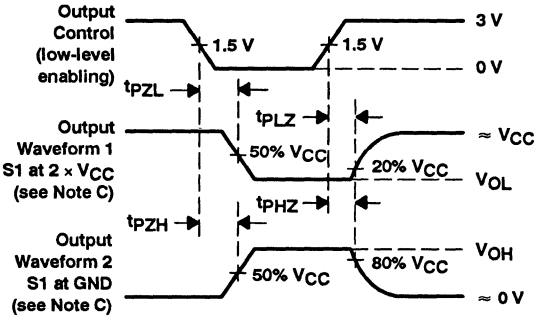
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



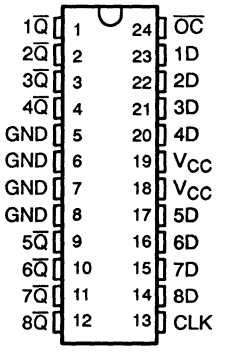
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

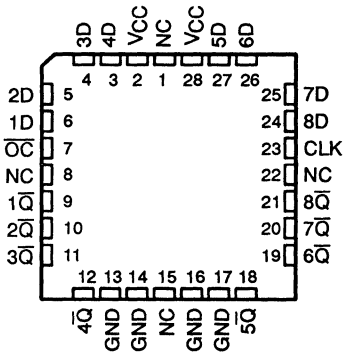
Figure 1. Load Circuit and Voltage Waveforms

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11534 . . . JT PACKAGE
74AC11534 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11534 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These eight flip-flops feature 3-state outputs designed for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'AC11534 are edge-triggered, D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs are set to the complement of the logic levels at the D inputs. The 'AC11534 is functionally equivalent to the 'AC11374 except for having inverted outputs.

An output-control input ($\overline{OC}$) is used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

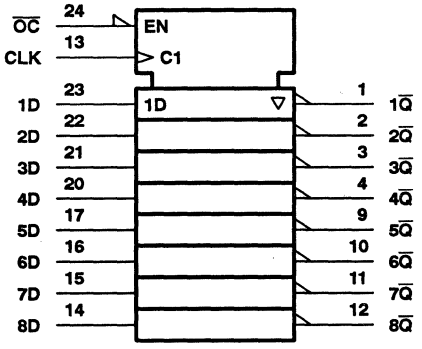
The 54AC11534 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11534 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

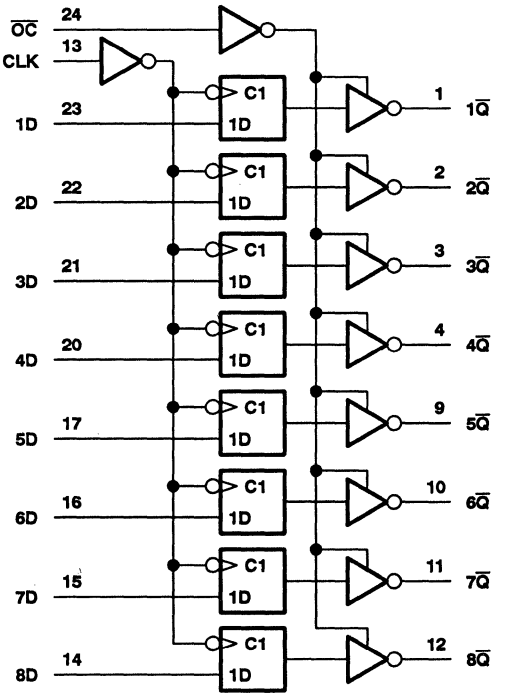
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11534			74AC11534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OC}$	0		5	0		5	ns/V
		D	0		10	0		10	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

		T_A = 25°C		54AC11534		74AC11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	50	0	50	0	50	MHz
t_w	Pulse duration, CLK low or CLK high	10		10		10		ns
t_{su}	Setup time, data before CLK ↑	3.5		3.5		3.5		ns
t_h	Hold time, data after CLK ↑	5.5		5.5		5.5		ns

timing requirements, V_{CC} = 5 V ± 0.5 V (see Figure 1)

		T_A = 25°C		54AC11534		74AC11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CLK low or CLK high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before CLK ↑	3.5		3.5		3.5		ns
t_h	Hold time, data after CLK ↑	4.5		4.5		4.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			50	75		50		50		MHz
t_{PLH}	CLK	$\overline{Q}$	1.5	11	15.3	1.5	19.1	1.5	17.6	ns
t_{PHL}			1.5	11	15.7	1.5	19	1.5	17.7	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	1.5	9	12.8	1.5	15.8	1.5	14.6	ns
t_{PZL}			1.5	9	12.6	1.5	15.6	1.5	14.3	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	1.5	10	12.6	1.5	13.8	1.5	13.3	ns
t_{PLZ}			1.5	8	13	1.5	14.2	1.5	13.8	

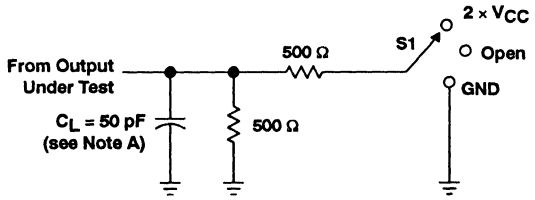
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11534		74AC11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75	100		75		75		MHz
t_{PLH}	CLK	$\overline{Q}$	1.5	7	10.3	1.5	12.7	1.5	11.7	ns
t_{PHL}			1.5	7	10.7	1.5	13.2	1.5	12.1	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	1.5	6	9.2	1.5	11.2	1.5	10.4	ns
t_{PZL}			1.5	6	9.2	1.5	11.3	1.5	10.4	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	1.5	9	11.1	1.5	11.9	1.5	11.6	ns
t_{PLZ}			1.5	6	8.8	1.5	9.6	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

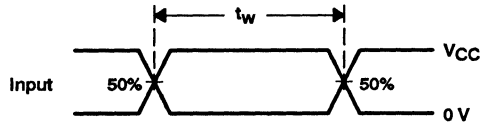
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	75	pF
		Outputs disabled		65	

PARAMETER MEASUREMENT INFORMATION

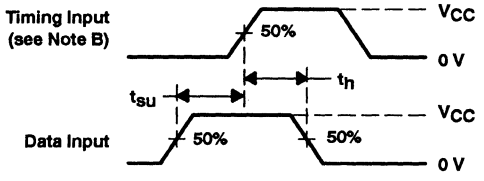


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

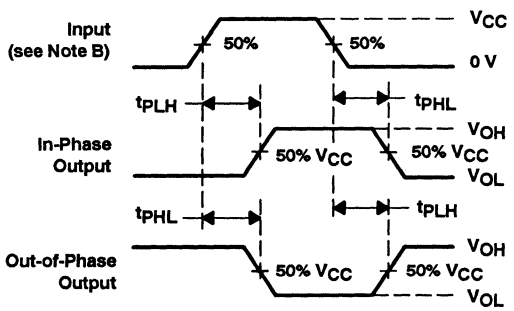
LOAD CIRCUIT



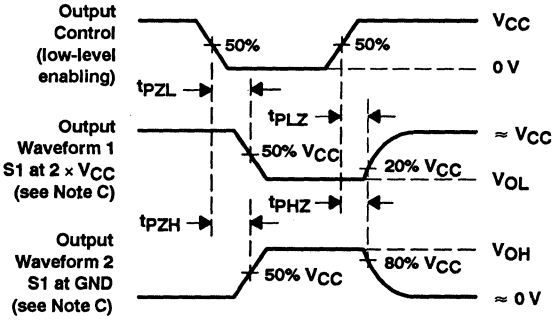
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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Figure 1. Load Circuit and Voltage Waveforms

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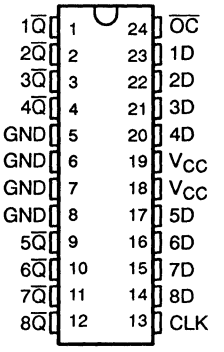
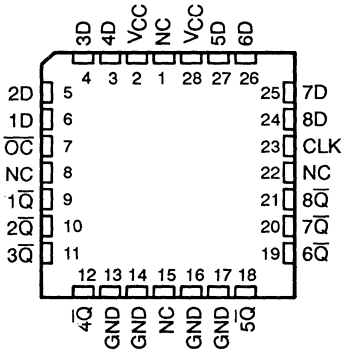
54ACT11534 . . . JT PACKAGE
74ACT11534 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11534 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These eight flip-flops feature 3-state outputs designed for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'ACT11534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs are set to the complement of the logic levels at the D inputs. The 'ACT11534 is functionally equivalent to the 'ACT11373 except for having inverted outputs.

An output-control input ($\overline{OC}$) is used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control ($\overline{OC}$) does not affect the internal operations of the flip-flops. Old data can be retained, or new data can be entered while the outputs are in the high-impedance state.

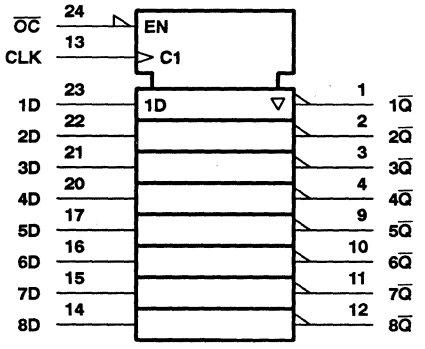
The 54ACT11534 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11534 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

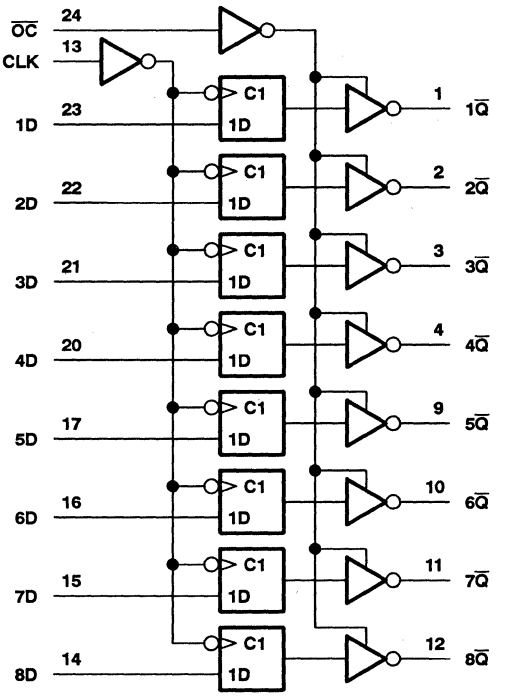
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11534		74ACT11534		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT11534		74ACT11534		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	55	0	55	0	55	MHz
t_w	Pulse duration, CLK low or CLK high	9		9		9		ns
t_{su}	Setup time, data before CLK ↑	3		3		3		ns
t_h	Hold time, data after CLK ↑	5.5		5.5		5.5		ns

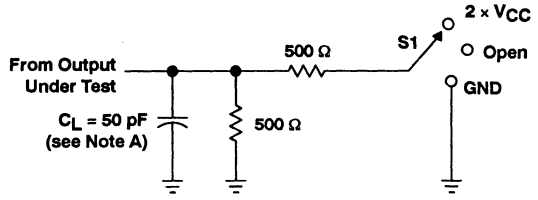
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11534		74ACT11534		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55	70		55		55		MHz
t_{PLH}	CLK	Any $\overline{Q}$	1.5	8.5	12.7	1.5	15.7	1.5	14.5	ns
t_{PHL}			1.5	8.5	13.3	1.5	16.3	1.5	15	
t_{PZH}	$\overline{OC}$	Any $\overline{Q}$	1.5	7.5	12	1.5	14.2	1.5	13.3	ns
t_{PZL}			1.5	7.5	12.2	1.5	14.5	1.5	13.5	
t_{PHZ}	$\overline{OC}$	Any $\overline{Q}$	1.5	11	12.9	1.5	13.9	1.5	13.5	ns
t_{PLZ}			1.5	8	11.2	1.5	12.5	1.5	12	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

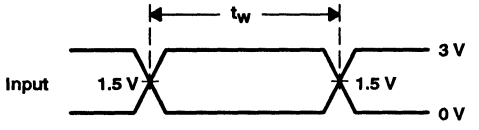
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	92	pF
		Outputs disabled		82	

PARAMETER MEASUREMENT INFORMATION

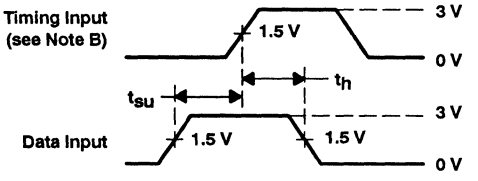


LOAD CIRCUIT

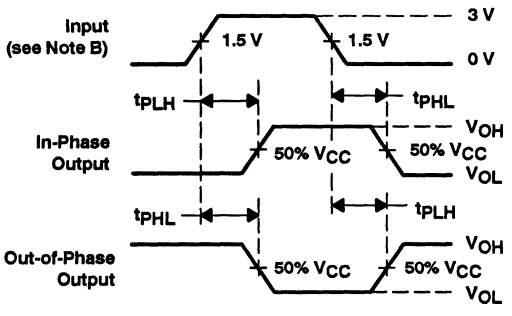
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



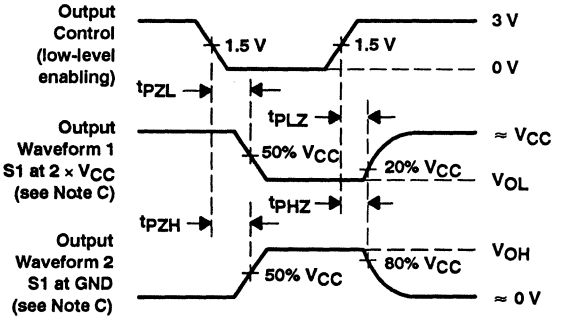
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



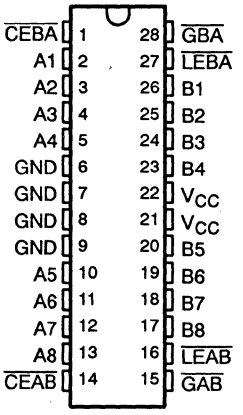
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This 8-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B-to-A is similar, but requires the use of $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The 74ACT11543 is characterized for operation from – 40°C to 85°C.

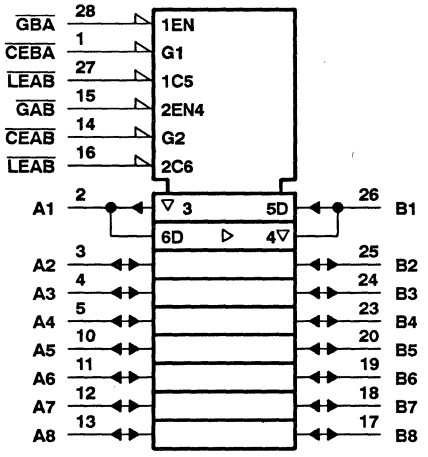
FUNCTION TABLE

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H		Storing	
X		H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡ Data present before low-to-high transition of $\overline{LEAB}$.

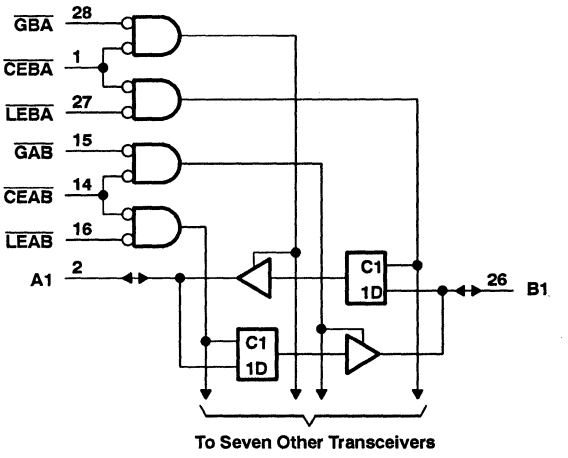
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 µA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		4		4		ns
t_{su}	Setup time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑	2.5		2.5		ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑	3		3		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑	2		2		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑	1.5		1.5		

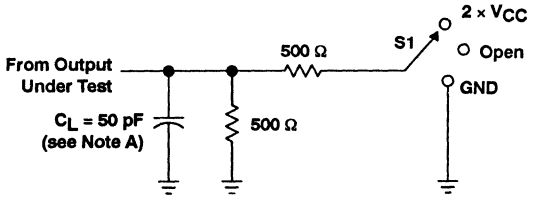
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.5	6.2	9.1	3.5	10.2	ns
t_{PHL}			3.2	6.5	10.8	3.2	12.1	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3	6.1	10.1	3	11.2	ns
t_{PHL}			3.7	7.2	11.7	3.7	13.2	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.5	6.7	11.1	3.5	12.2	ns
t_{PZL}			3.2	8.4	13.4	3.2	16	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.8	7.3	10.1	4.8	11	ns
t_{PLZ}			5.1	7.5	10.3	5.1	11.1	
t_{PZH}	$\overline{GBA}$ or $\overline{GAB}$	A or B	3.3	6.4	10.5	3.3	11.5	ns
t_{PZL}			3	8	12.8	3	15.3	
t_{PHZ}	$\overline{GBA}$ or $\overline{GAB}$	A or B	4.6	6.9	9.6	4.6	10.4	ns
t_{PLZ}			5	7.1	9.8	5	10.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

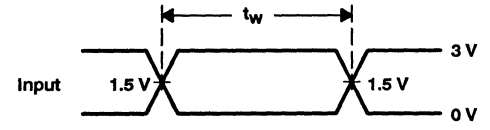
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	47	pF
		Outputs disabled			13	

PARAMETER MEASUREMENT INFORMATION

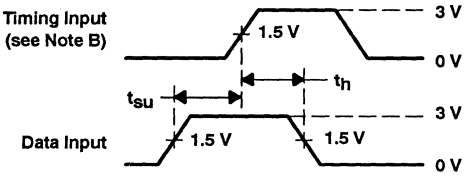


LOAD CIRCUIT

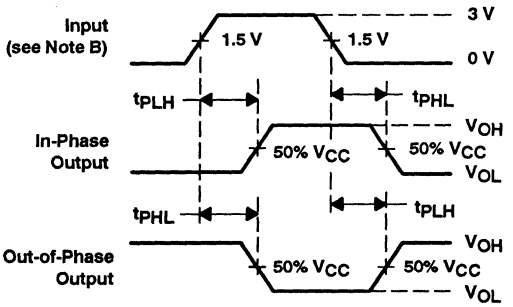
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



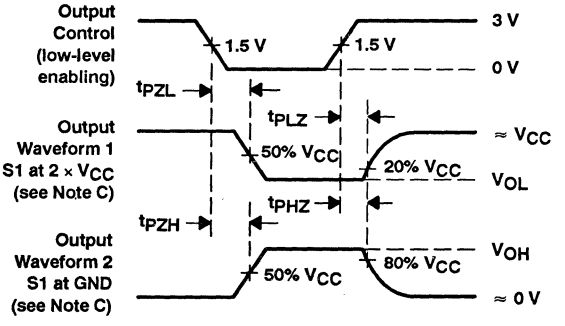
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

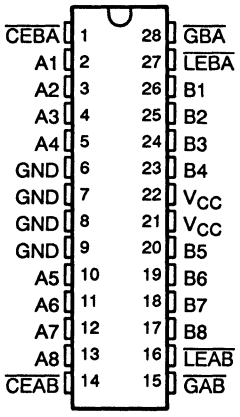
Figure 1. Load Circuit and Voltage Waveforms

74ACT11544
OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS133 – D3609, JULY 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **3-State Inverted Outputs**
- **Back-to-Back Registers for Storage**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This 8-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow. The 74ACT11544 inverts data in both directions.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B-to-A is similar, but requires the use of $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The 74ACT11544 is characterized for operation from −40°C to 85°C.

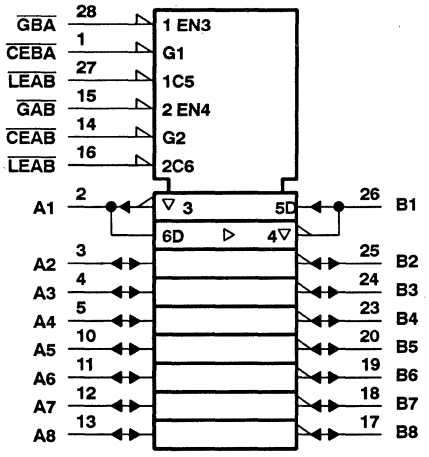
FUNCTION TABLE

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H		Storing	
X		H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡ Data present before low-to-high transition of $\overline{LEAB}$.

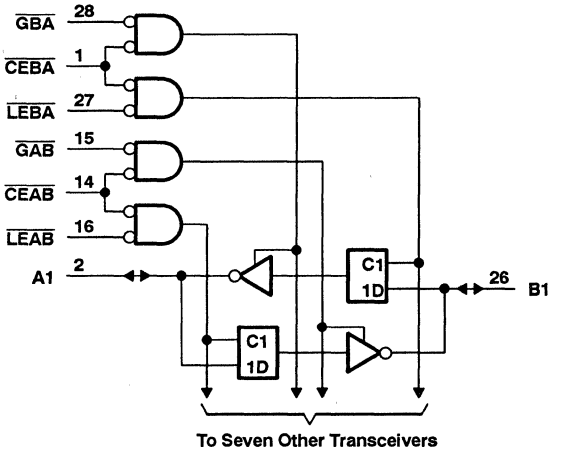
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 µA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_o	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		4		4		ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}$↑	2.5		2.5		ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$↑	3		3		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑	2		2		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑	1.5		1.5		

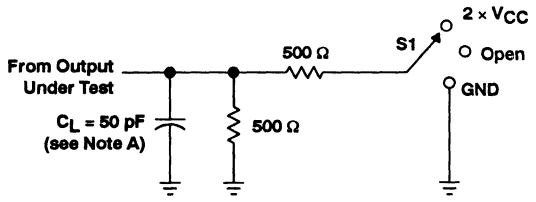
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.4	5.7	8.2	2.4	8.9	ns
t_{PHL}			4.1	7.3	9.3	4.1	10.3	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	2.6	6	8.7	2.6	9.5	ns
t_{PHL}			3.4	7.1	10.1	3.4	11	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.3	6.7	9.5	3.3	10.4	ns
t_{PZL}			3.6	8.2	11.2	3.6	13	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.8	7.6	9.7	4.8	10.4	ns
t_{PLZ}			4.7	7.6	9.5	4.7	10.2	
t_{PZH}	$\overline{GBA}$ or $\overline{GAB}$	A or B	3	6.4	9	3	9.9	ns
t_{PZL}			3.5	7.8	10.8	3.5	12.5	
t_{PHZ}	$\overline{GBA}$ or $\overline{GAB}$	A or B	4.6	7.3	9.3	4.6	9.9	ns
t_{PLZ}			4.6	7.2	9.2	4.6	9.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

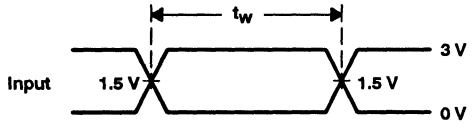
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

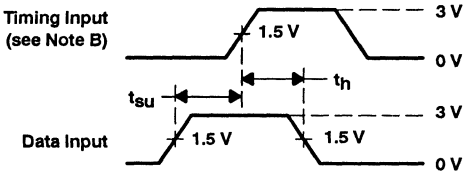


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

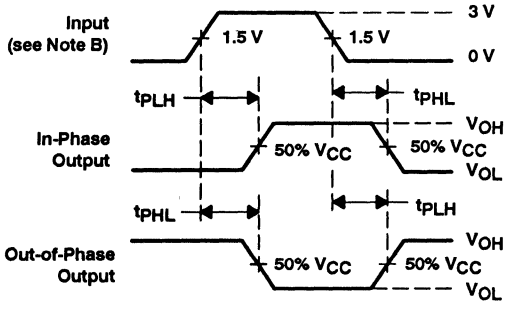
LOAD CIRCUIT



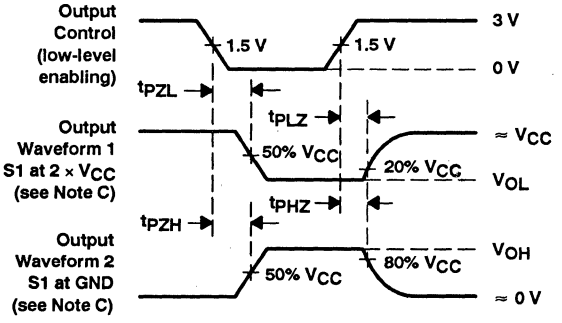
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



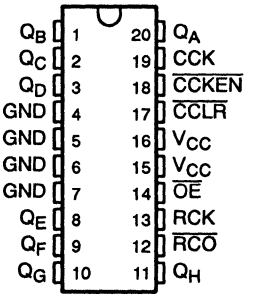
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Parallel Registered Outputs**
- **Internal Counters Have Direct Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

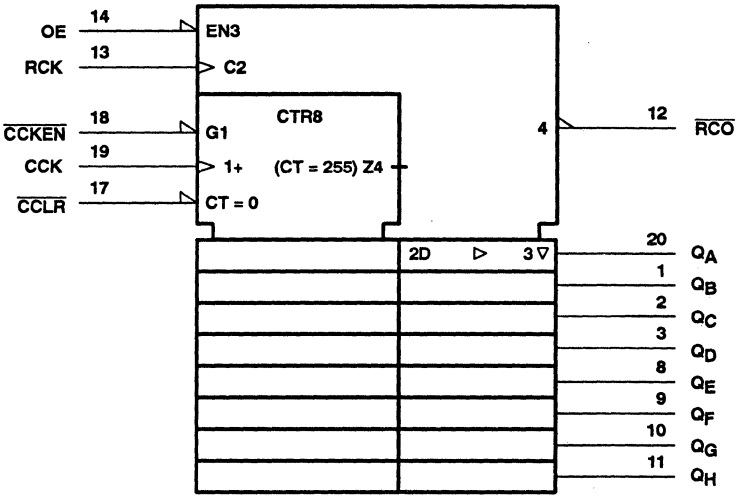
The 74AC11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear ($\overline{CCLR}$) input and a count-enable ($\overline{CCKEN}$) input. For cascading, a ripple-carry ($\overline{RCO}$) output is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74AC11590 is characterized for operation from −40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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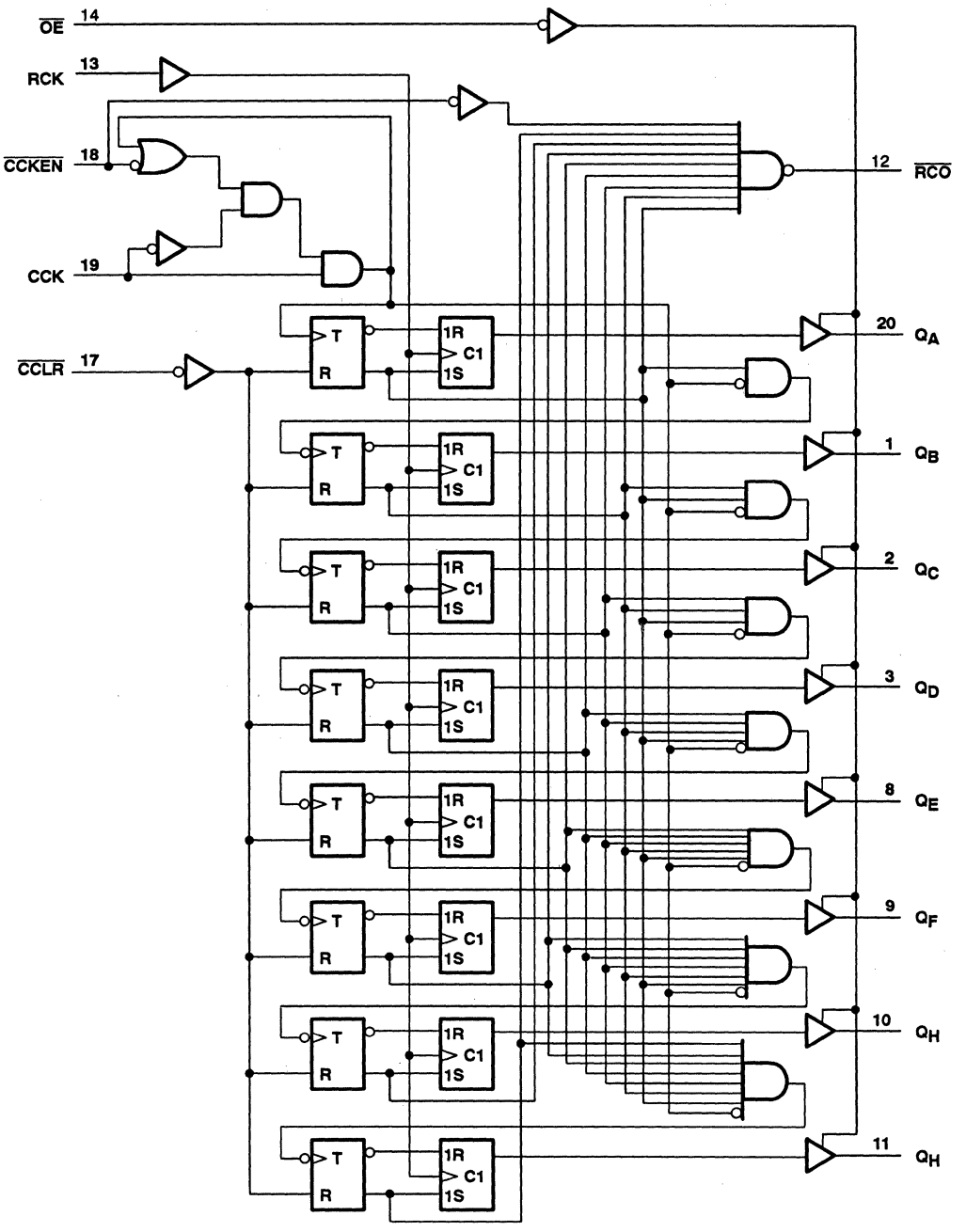
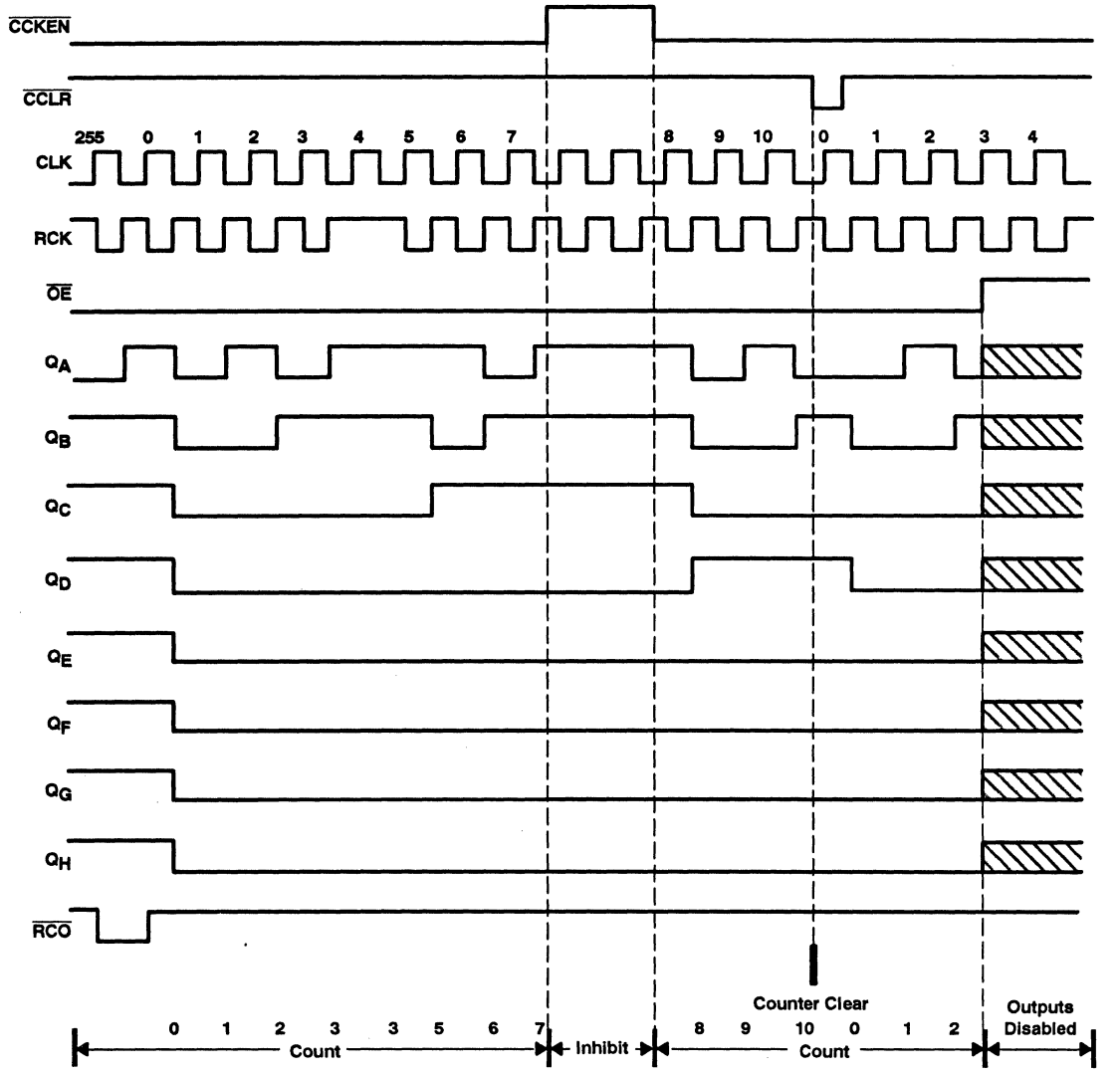
logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		3				pF
C_o	$V_O = V_{CC}$ or GND	5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK		0	50	0	50	MHz
t_w	Pulse duration	CCK or RCK high or low	10		10		ns
		$\overline{CCLR}$ low	7.4		7.4		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	5.2		5.2		ns
		$\overline{CCLR}$ high before CCK↑	3.4		3.4		
		CCK↑ before RCK↑‡	8.1		8.1		
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	0		0		ns

‡ This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK		0	80	0	80	MHz
t_w	Pulse duration	CCK or RCK high or low	6.3		6.3		ns
		$\overline{CCLR}$ low	4.9		4.9		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	3.7		3.7		ns
		$\overline{CCLR}$ high before CCK↑	1.6		1.6		
		CCK↑ before RCK↑†	5.5		5.5		
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	0.5		0.5		ns

† This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		50			50		MHz
t_{PLH}	CCK	$\overline{RCO}$	7	13.5	15.9	7	18.3	ns
t_{PHL}			9	16.9	19.5	9	22.1	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	6.2	12.4	14.8	6.2	17.1	ns
t_{PLH}	RCK	Q	7.3	13.7	16.2	7.3	18.7	ns
t_{PHL}			7	13.6	15.9	7	17.9	
t_{PZH}	$\overline{OE}$	Q	7.8	15.5	18.5	7.8	21.1	ns
t_{PZL}			8.5	18.2	21.4	8.5	24.5	
t_{PHZ}	$\overline{OE}$	Q	6.3	10	11.9	6.3	13.2	ns
t_{PLZ}			6.8	10.8	12.8	6.8	14.1	
t_{PLH}	$\overline{CCKEN}$	$\overline{RCO}$	6	11.7	14	6	16.2	ns
t_{PHL}			6	11.6	13.7	6	15.4	

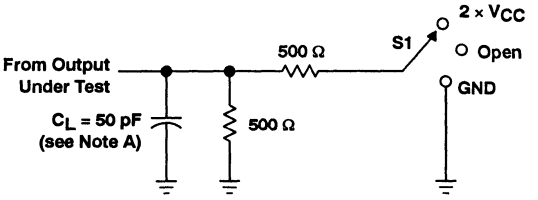
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80			80		MHz
t_{PLH}	CCK	RCO	3.6	7.8	10.2	3.6	11.7	ns
t_{PHL}			4.7	9.8	12.7	4.7	14.4	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	3.2	7.2	9.5	3.2	10.9	ns
t_{PLH}	RCK	Q	3.7	8	10.4	3.7	12	ns
t_{PHL}			3.6	8.2	10.7	3.6	12.1	
t_{PZH}	OE	Q	3.8	8.9	11.9	3.8	13.6	ns
t_{PZL}			3.7	9.5	12.6	3.7	14.3	
t_{PHZ}	OE	Q	4.5	7.5	9.4	4.5	10.5	ns
t_{PLZ}			5.4	8.7	10.8	5.4	12	
t_{PLH}	$\overline{CCKEN}$	$\overline{RCO}$	3	6.9	9	3	10.4	ns
t_{PHL}			2.9	7	9.2	2.9	10.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

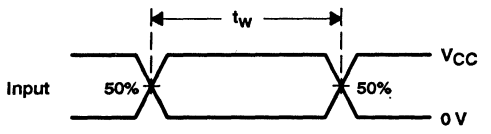
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		43	

PARAMETER MEASUREMENT INFORMATION

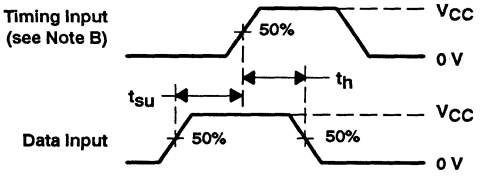


LOAD CIRCUIT

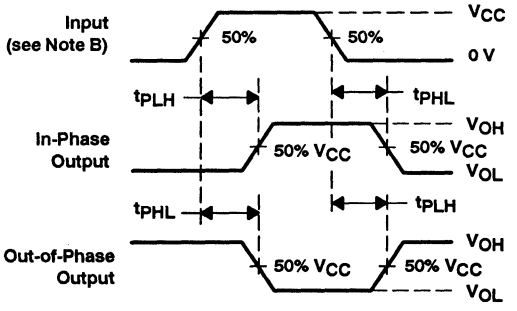
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



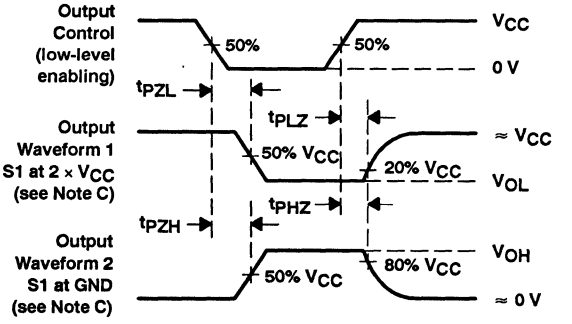
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



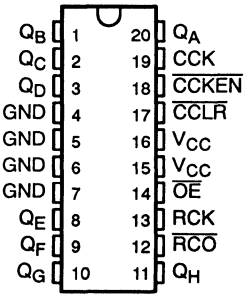
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Parallel Registered Outputs**
- **Internal Counters Have Direct Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear ($\overline{CCLR}$) input and a count-enable ($\overline{CCKEN}$) input. For cascading, a ripple-carry ($\overline{RCO}$) output is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

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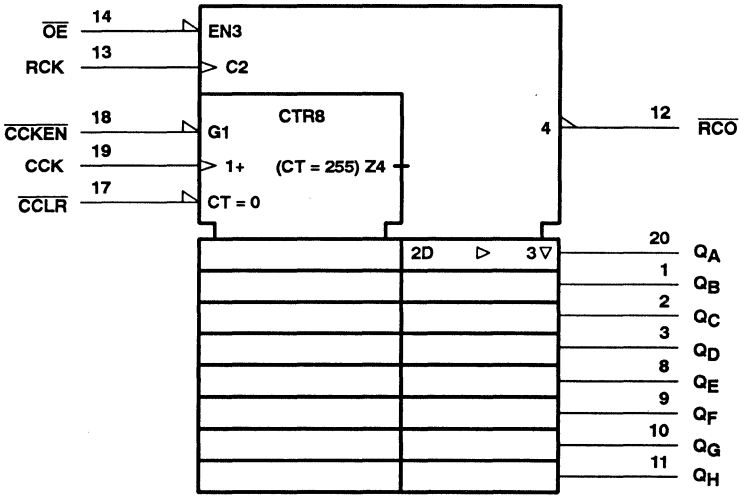
The 74ACT11590 is characterized for operation from −40°C to 85°C.

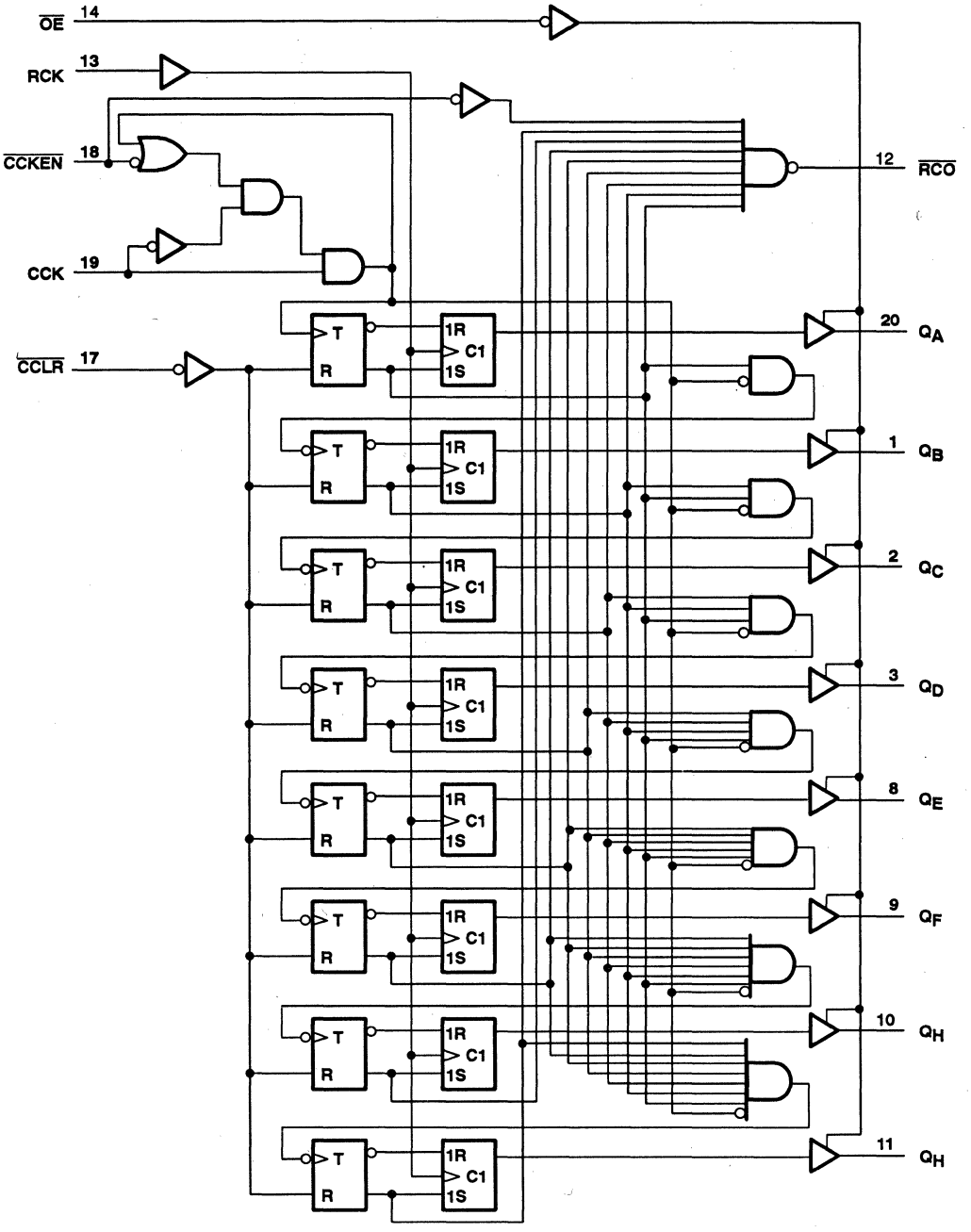
logic symbol†



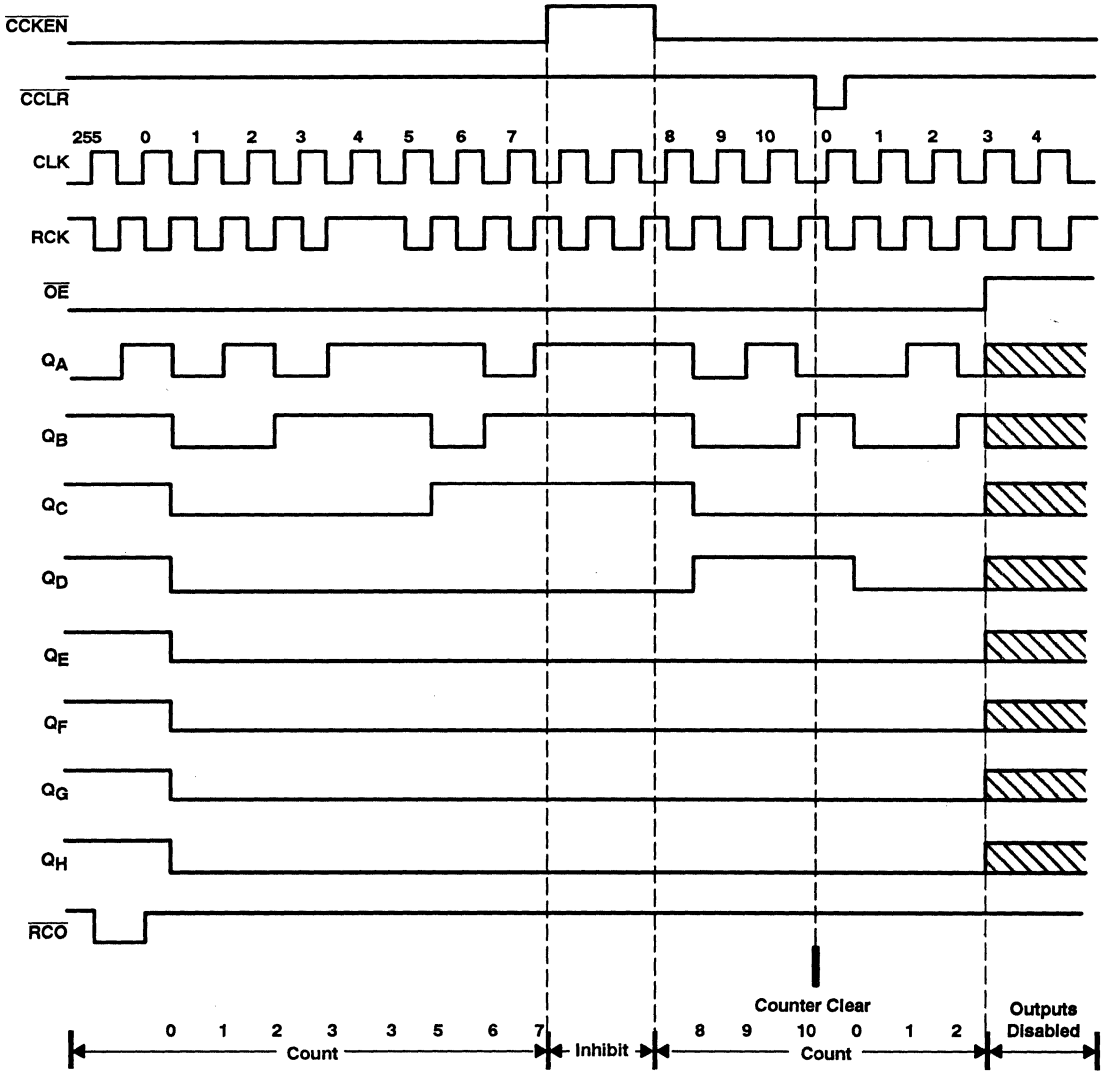
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3				pF
C_o	$V_O = V_{CC}$ or GND		5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK		0	80	0	80	MHz
t_w	Pulse duration	CCK or RCK high or low	6.3		6.3		ns
		$\overline{CCLR}$ low	8.4		8.4		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	5.1		5.1		ns
		$\overline{CCLR}$ high before CCK↑	1.6		1.6		
		CCK↑ before RCK↑§	5.5		5.5		
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	0.6		0.6		ns

§ This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

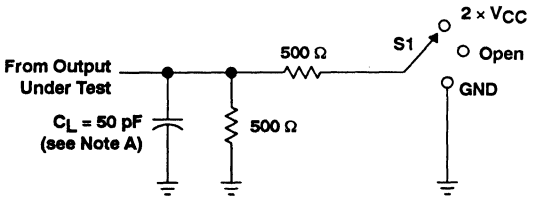
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80			80		MHz
t_{PLH}	CCK	$\overline{RCO}$	4.5	8	11	4.5	13	ns
t_{PHL}			5.1	9	13.8	5.1	16.4	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	3.5	7	11	3.5	13.1	ns
t_{PLH}	RCK	Q	4.6	8	11.1	4.6	13	ns
t_{PHL}			3.9	7.6	11.8	3.9	13.9	
t_{PZH}	$\overline{OE}$	Q	4	8.3	13.2	4	15.6	ns
t_{PZL}			3.8	8.2	13.9	3.8	16.2	
t_{PHZ}	$\overline{OE}$	Q	5.3	8	10.3	5.3	11.5	ns
t_{PLZ}			6.1	9.1	11.5	6.1	13	
t_{PLH}	$\overline{CCKEN}$	$\overline{RCO}$	3.8	6.8	9.7	3.8	11.2	ns
t_{PHL}			2.8	7.6	11	2.8	12.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

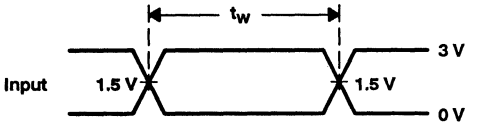
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		42	

PARAMETER MEASUREMENT INFORMATION

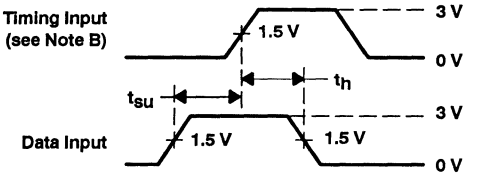


LOAD CIRCUIT

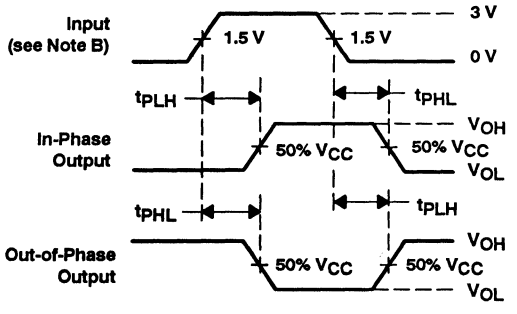
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



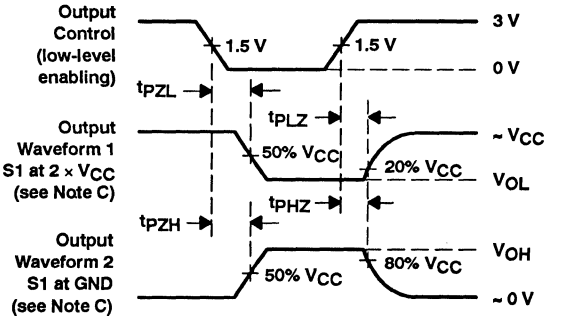
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

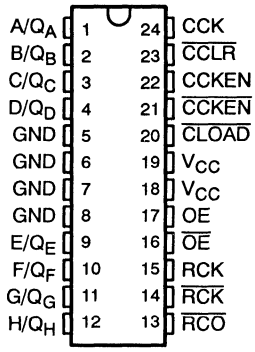
Figure 1. Load Circuit and Voltage Waveforms

74AC11593
8-BIT BINARY COUNTER WITH 3-STATE I/O INPUT REGISTERS

SCAS202 – MARCH 1992 – REVISED APRIL 1993

- **Parallel 3-State I/O: Register Inputs/ Counter Outputs**
- **Counter Has Direct Overriding Load and Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74AC11953 consists of a parallel input, an 8-bit storage register feeding an 8-bit counter, and a 3-state I/O which provides parallel count outputs. Both the register and the counter have individual positive-edge triggered clocks.

The function tables show the operation of the counter clock-enable (CCKEN, $\overline{\text{CCKEN}}$) and output-enable (OE, $\overline{\text{OE}}$) inputs. A register clock-enable ($\overline{\text{RCK}}$) input is also provided.

The counter ($\overline{\text{RCO}}$) input has direct load and clear functions. A low-going $\overline{\text{RCO}}$ pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{\text{RCO}}$ of each stage to CCK of the following stage.

The 74AC11593 is characterized for operation from – 40°C to 85°C.

Function Tables

COUNTER CLOCK ENABLE

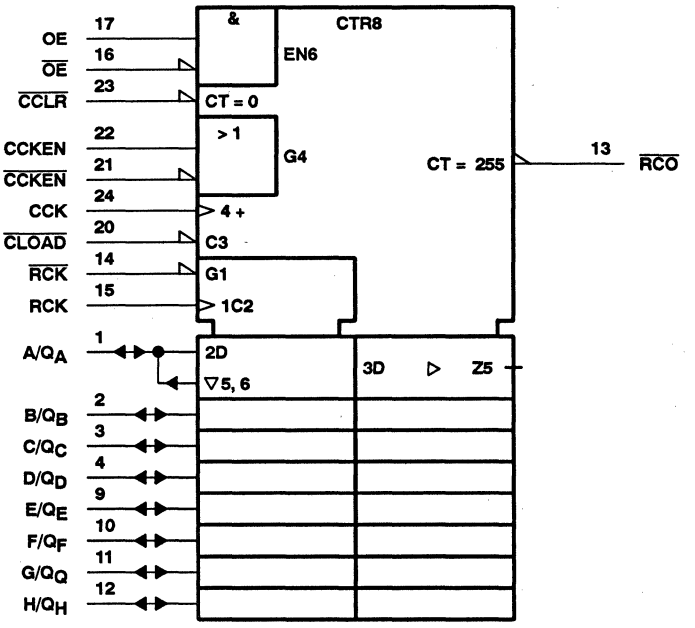
INPUTS		OUTPUTS
CCKEN	$\overline{\text{CCKEN}}$	A/Q_A THRU H/Q_H
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

OUTPUT ENABLE

INPUTS		OUTPUTS
OE	$\overline{\text{OE}}$	A/Q_A THRU H/Q_H
L	L	Input mode
L	H	Input mode
H	L	Output mode
H	H	Input mode

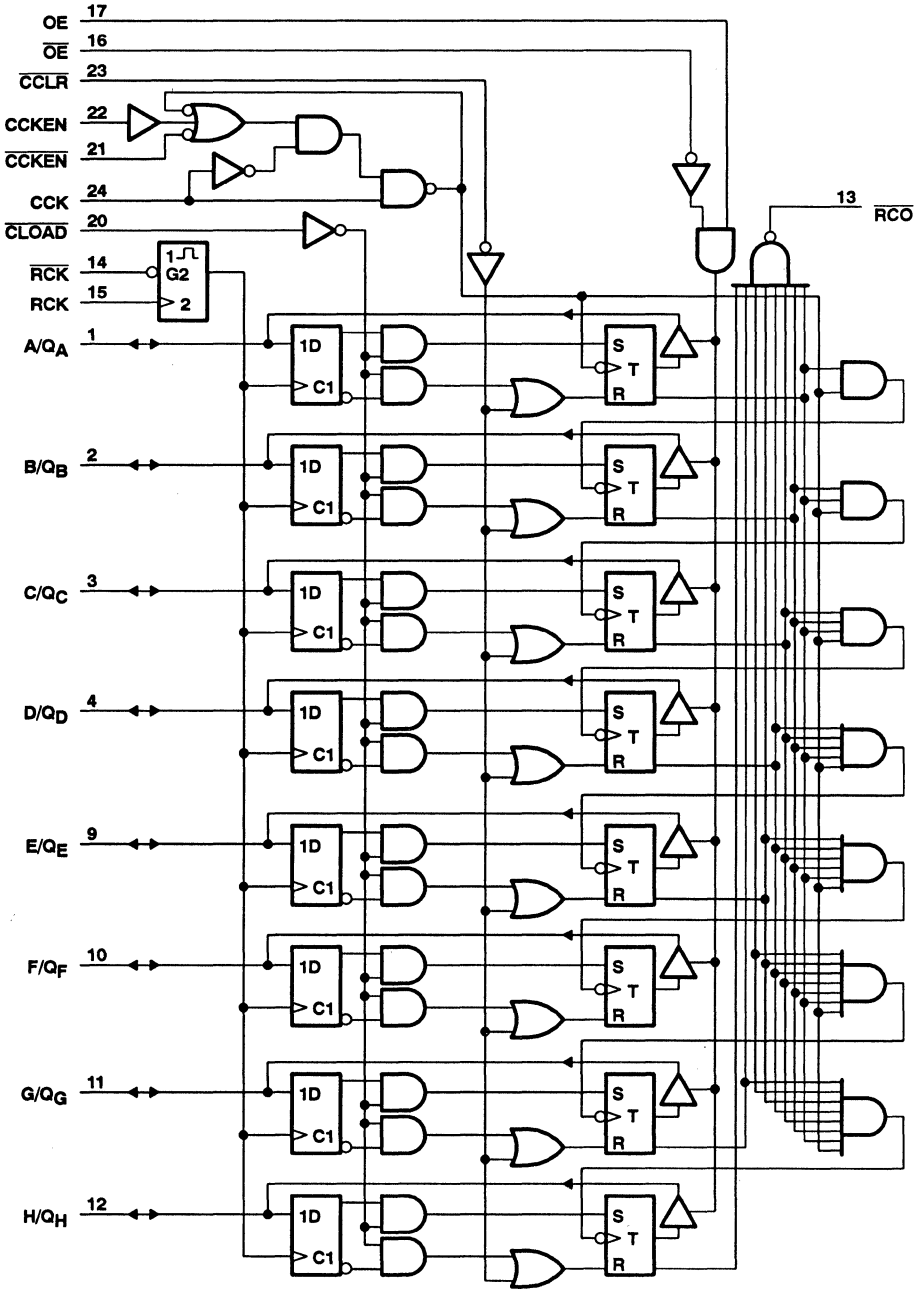
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

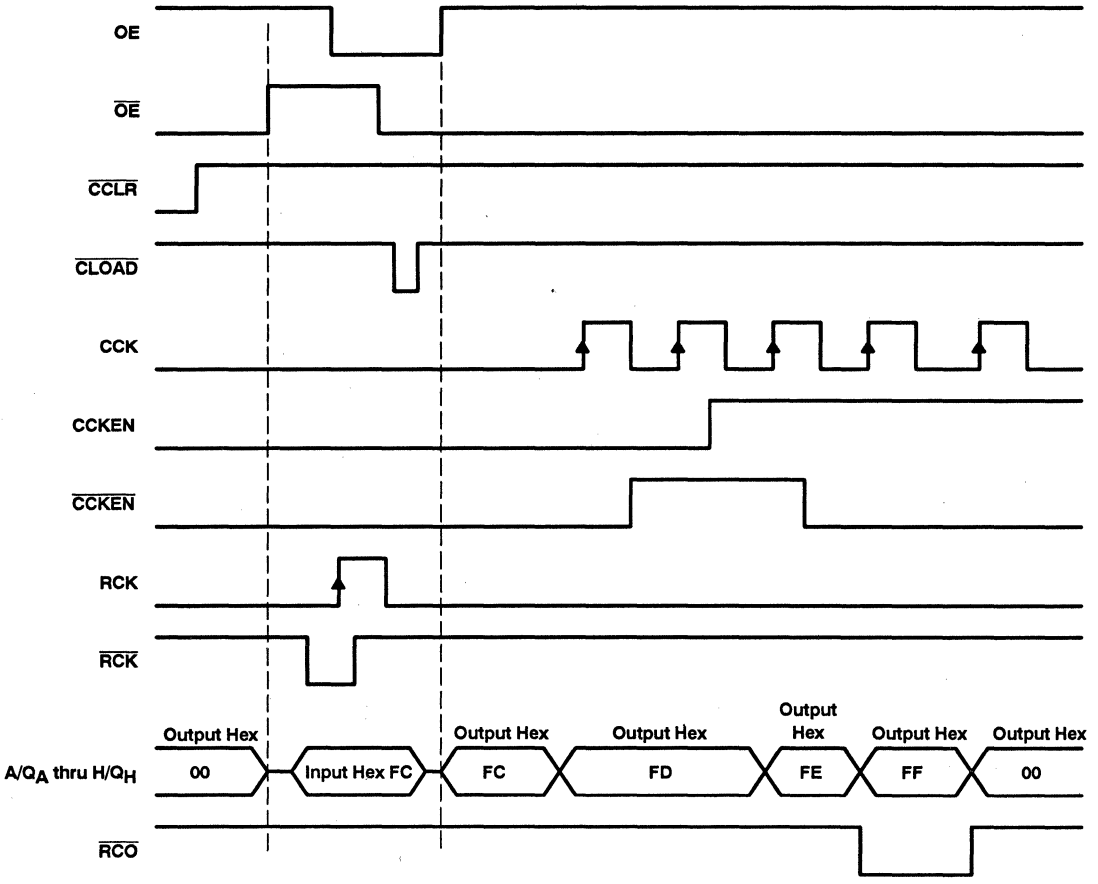


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 225 mA
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			– 4	mA
		V_{CC} = 4.5 V			– 24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		– 40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK			40		40	MHz
t_w	Pulse duration	CCK high or low	6		6		ns
		RCK high or low	6		6		
		$\overline{RCK}$ high or low	4.5		4.5		
		$\overline{CCLR}$ low	7.5		7.5		
		$\overline{CLOAD}$ low	6.1		6.1		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	5.2		5.2		ns
		CCKEN high before CCK↑	6.4		6.4		
		$\overline{CCLR}$ high before CCK↑	1.7		1.7		
		$\overline{CLOAD}$ high before CCK↑	8.2		8.2		
		RCK↑ before $\overline{CLOAD}$↑†	11.1		11.1		
		Data A thru H before RCK↑	2.3		2.3		
t_h	Hold time	Data A thru H after RCK↑	0.5		0.5		ns
		All others	0.2		0.2		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK			70		70	MHz
t_w	Pulse duration	CCK high or low	5		5		ns
		RCK high or low	5		5		
		$\overline{RCK}$ high or low	4.5		4.5		
		$\overline{CCLR}$ low	5		5		
		$\overline{CLOAD}$ low	4.7		4.7		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	3.1		3.1		ns
		CCKEN high before CCK↑	4.3		4.3		
		$\overline{CCLR}$ high before CCK↑	1.1		1.1		
		$\overline{CLOAD}$ high before CCK↑	5.4		5.4		
		RCK↑ before $\overline{CLOAD}$↑†	7.8		7.8		
		Data A thru H before RCK↑	2		2		
t_h	Hold time	Data A thru H after RCK↑	1.1		1.1		ns
		All others	0.8		0.8		

† This time insures the data saved by RCK↑ will also be loaded into the counter.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			40			40		MHz
t_{PLH}	CCK	Q	6.8	14.4	19.3	6.8	22.4	ns
t_{PHL}			6.4	14.1	18.8	6.4	21.1	
t_{PLH}	$\overline{CLOAD}$	Q	6.7	17.3	23.6	6.7	27.1	ns
t_{PHL}			3.9	18.9	29.1	3.9	32.3	
t_{PHL}	$\overline{CCLR}$	Q	5.4	13	17.6	5.4	19.8	ns
t_{PZH}	OE	Q	7.3	15.7	20.8	7.3	24.1	ns
t_{PZL}			8	17.7	23.2	8	26.7	
t_{PZH}	$\overline{OE}$	Q	6.9	15.2	20.2	6.9	23.3	ns
t_{PZL}			7.8	17.3	22.7	7.8	26.1	
t_{PHZ}	OE	Q	6.4	10.3	13.8	6.4	15.2	ns
t_{PLZ}			6.6	10.8	14.1	6.6	16.1	
t_{PHZ}	$\overline{OE}$	Q	5.7	9.6	12.8	5.7	14.1	ns
t_{PLZ}			5.9	10.2	13.4	5.9	15.2	
t_{PLH}	CCK	$\overline{RCO}$	5.3	12	16	5.3	18.6	ns
t_{PHL}			7.1	15.4	20.3	7.1	23.1	
t_{PLH}	$\overline{CLOAD}$	$\overline{RCO}$	5.9	12.4	16.5	5.9	18.8	ns
t_{PHL}			10.1	19.6	25.5	10.1	29.4	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	5.6	12.3	16.6	5.6	19.2	ns
t_{PLH}	RCK	$\overline{RCO}$	8.6	17.3	22.2	8.6	25.8	ns
t_{PHL}			10.3	20.3	26.2	10.3	30.3	

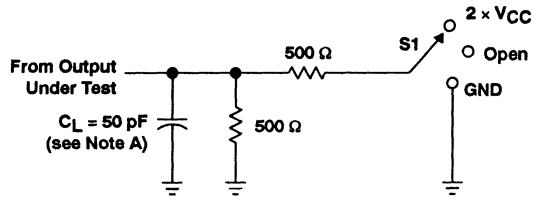
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CCK	Q	4.1	8.7	12.4	4.1	14.3	ns
t_{PHL}			4.2	8.9	12.6	4.2	14.2	
t_{PLH}	$\overline{CLOAD}$	Q	3.7	10	15.3	3.7	17.4	ns
t_{PHL}			3.4	11.4	18.3	3.4	20.6	
t_{PHL}	$\overline{CCLR}$	Q	3.3	7.9	11.8	3.3	13.4	ns
t_{PZH}	OE	Q	4.1	9.1	13.2	4.1	15.3	ns
t_{PZL}			4.1	9.4	13.8	4.1	16	
t_{PZH}	$\overline{OE}$	Q	3.8	8.7	13	3.8	15	ns
t_{PZL}			3.9	9.1	13.4	3.9	15.4	
t_{PHZ}	OE	Q	4.2	7.6	10.6	4.2	11.6	ns
t_{PLZ}			5.3	8.8	11.8	5.3	13.1	
t_{PHZ}	$\overline{OE}$	Q	4.4	7.3	10.1	4.4	11	ns
t_{PLZ}			5.2	8.5	11.6	5.2	13	
t_{PLH}	CCK	$\overline{RCO}$	3.5	7.6	11.2	3.5	12.8	ns
t_{PHL}			4.1	9.2	13.4	4.1	15.4	
t_{PLH}	$\overline{CLOAD}$	$\overline{RCO}$	3.5	7.8	11.2	3.5	12.8	ns
t_{PHL}			5.6	11.7	16.6	5.6	19	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	3.6	8	11.6	3.6	13.4	ns
t_{PLH}	RCK	$\overline{RCO}$	5	10.3	14.4	5	16.7	ns
t_{PHL}			5.5	11.7	16.6	5.5	19.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

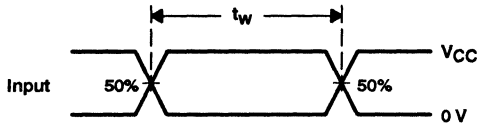
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz	66	pF
		Outputs disabled			15	

PARAMETER MEASUREMENT INFORMATION

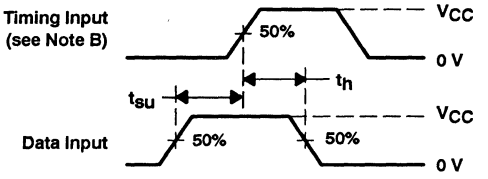


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

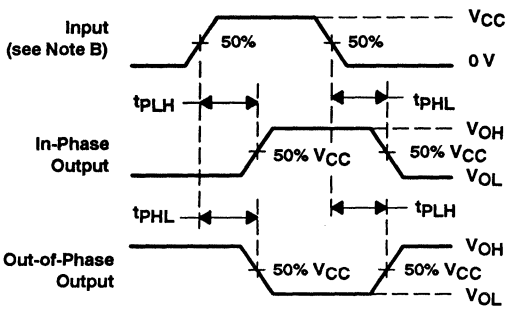
LOAD CIRCUIT



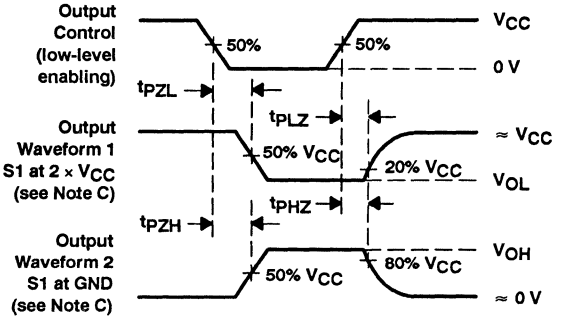
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



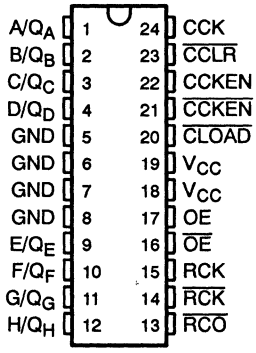
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Parallel Register Inputs/Binary Counter/3-State Outputs**
- **Counter Has Direct Overriding Load and Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74ACT11593 contains eight multiplexed parallel I/Os with 3-state output capability and an 8-bit storage register that feeds an 8-bit binary counter. Both the register and the counter have individual positive-edge triggered clocks.

The function tables show the operation of the counter clock-enable (CCKEN, $\overline{\text{CCKEN}}$) and output-enable (OE, $\overline{\text{OE}}$) inputs.

The counter input has direct load and clear functions. A low-going $\overline{\text{RCO}}$ pulse is obtained when the counter reaches the hex word FF.

Expansion is easily accomplished for two stages by connecting $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage. Cascading for larger count chains is accomplished by connecting $\overline{\text{RCO}}$ of each stage to CCK of the following stage.

The 74ACT11593 is characterized for operation from −40°C to 85°C.

Function Tables

COUNTER CLOCK ENABLE

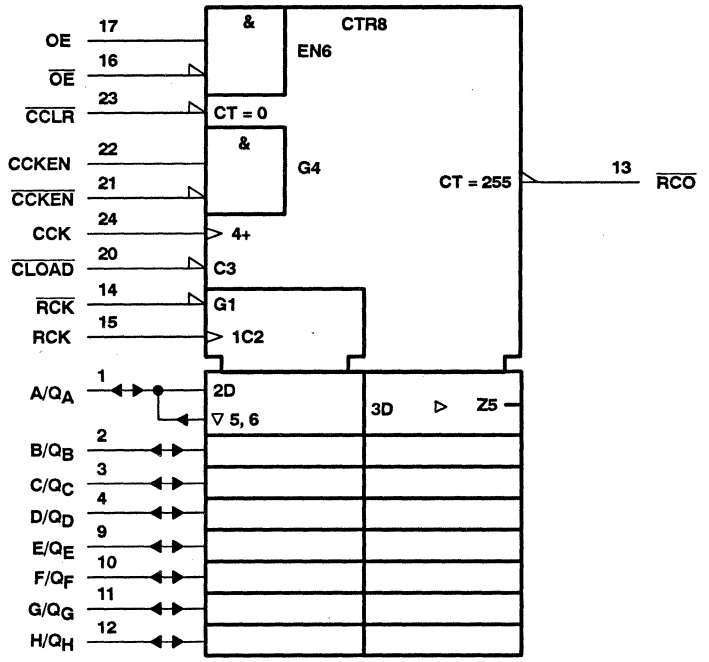
INPUTS		OUTPUTS
CCKEN	$\overline{\text{CCKEN}}$	A/Q_A THRU H/Q_H
L	L	Disable
L	H	Disable
H	L	Enable
H	H	Disable

OUTPUT ENABLE

INPUTS		OUTPUTS
OE	$\overline{\text{OE}}$	A/Q_A THRU H/Q_H
L	L	Input mode
L	H	Input mode
H	L	Output mode
H	H	Input mode

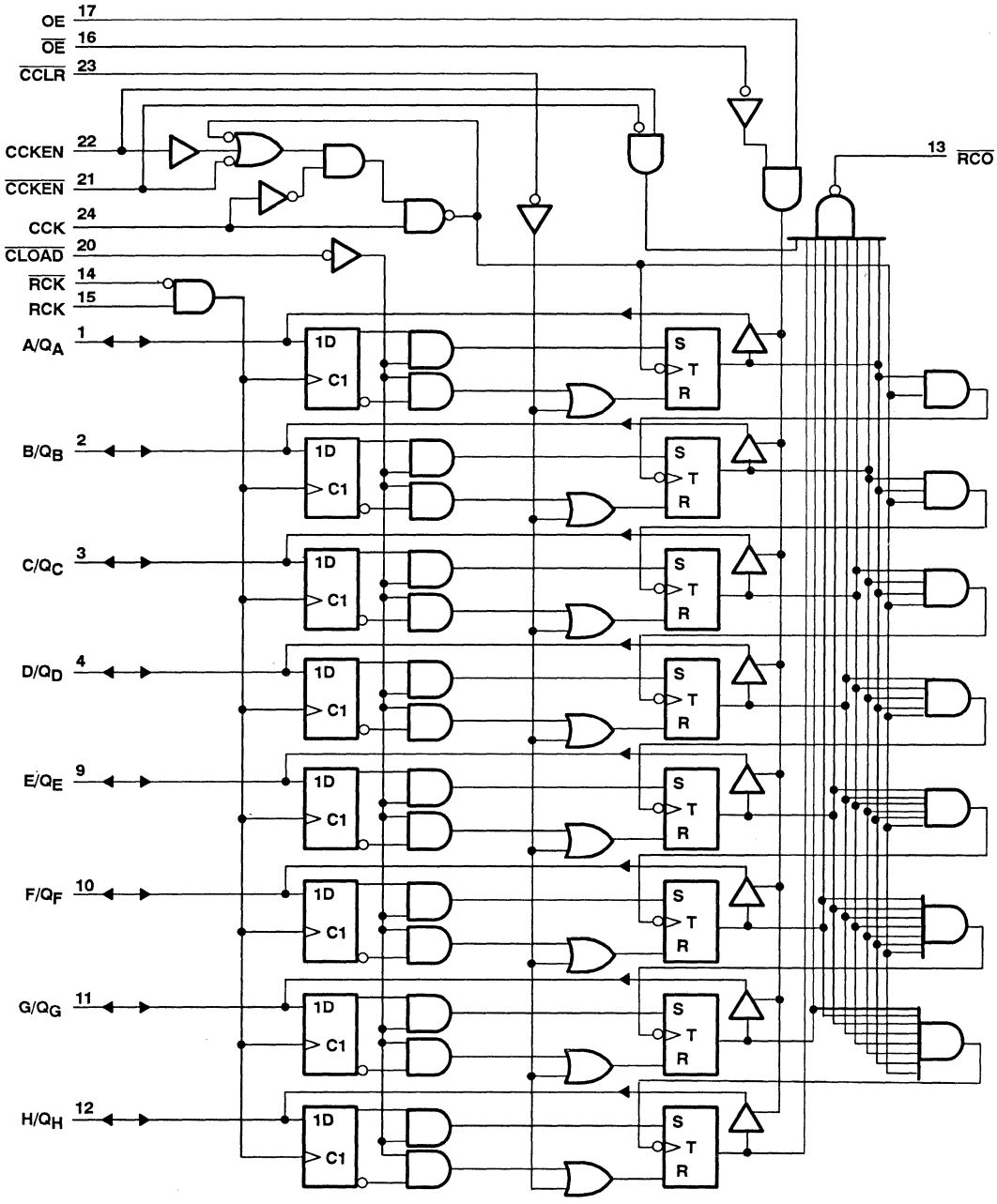
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

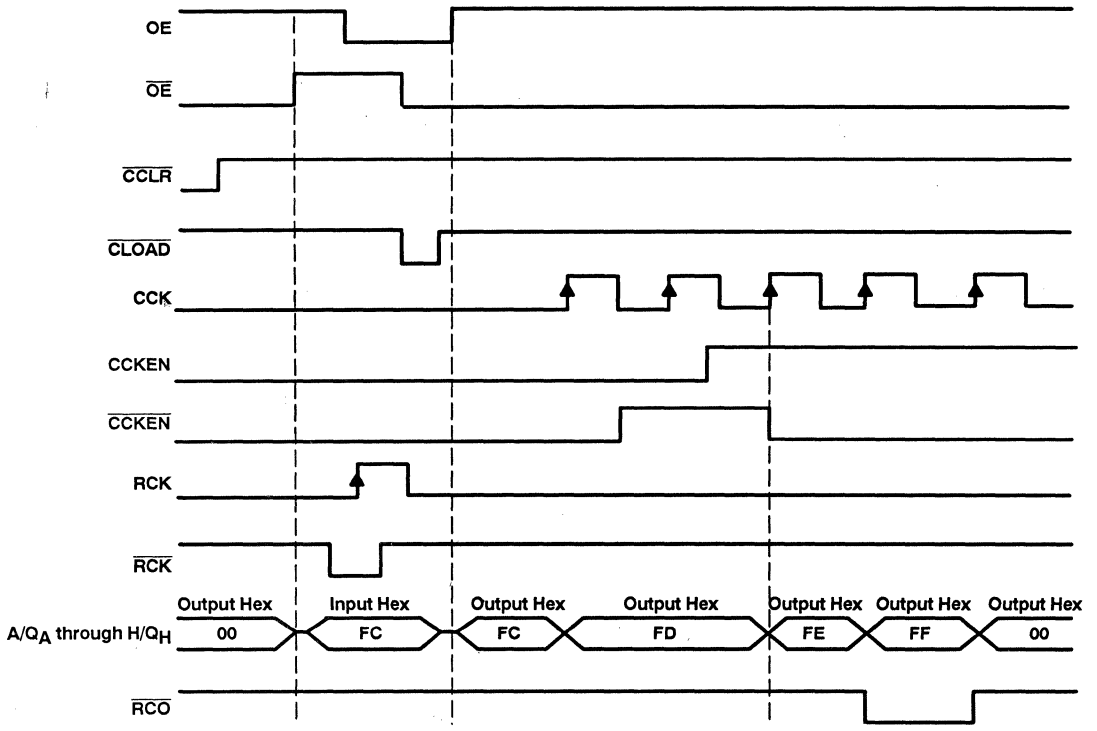


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		3.5				pF
C_{io}	V_O = V_{CC} or GND		5 V		12.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency, CCK or RCK			52		52	MHz
t_w	Pulse duration	CCK high or low	9.6		9.6		ns
		RCK high or low	5.8		5.8		
		$\overline{CCLR}$ low	7.6		7.6		
		$\overline{CLOAD}$ low	6.2		6.2		
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	3.6		3.6		ns
		CCKEN high before CCK↑	4		4		
		$\overline{CCLR}$ high before CCK↑	1.2		1.2		
		$\overline{CLOAD}$ high before CCK↑	5.1		5.1		
		RCK↑ before $\overline{CLOAD}$↑†	7.4		7.4		
		Data A thru H before RCK↑	2.4		2.4		
t_h	Hold time	Data A thru H after RCK↑	1.2		1.2		ns
		All others	0.8		0.8		

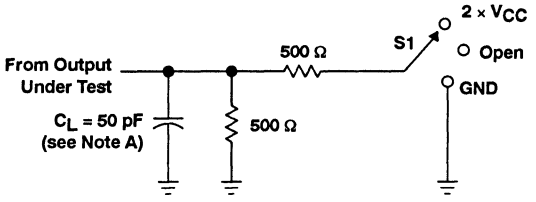
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			52			52		MHz
t_{PLH}	CCK	Q	5.6	10.2	13.3	5.6	15.1	ns
t_{PHL}			5.8	10.3	13.3	5.8	15	
t_{PLH}	$\overline{CLOAD}$	Q	5.5	12	16.9	5.5	19.1	ns
t_{PHL}			5.8	13.5	19.4	5.8	21.7	
t_{PHL}	$\overline{CCLR}$	Q	5	10.4	14.3	5	16	ns
t_{PZH}	OE	Q	5.9	10.9	14.3	5.9	16.3	ns
t_{PZL}			5.9	11.1	14.8	5.9	16.9	
t_{PZH}	$\overline{OE}$	Q	4.9	10.4	14.4	4.9	16.5	ns
t_{PZL}			5.1	10.7	15	5.1	17	
t_{PHZ}	OE	Q	5.3	9	11.8	5.3	12.9	ns
t_{PLZ}			6.2	10.2	13.1	6.2	14.4	
t_{PHZ}	$\overline{OE}$	Q	5.6	8.6	10.7	5.6	11.6	ns
t_{PLZ}			6.4	9.9	12	6.4	13.3	
t_{PLH}	CCK	$\overline{RCO}$	4.9	9.2	12.1	4.9	13.7	ns
t_{PHL}			5.8	10.9	14.3	5.8	16.3	
t_{PLH}	$\overline{CLOAD}$	$\overline{RCO}$	4.6	9.6	13.3	4.6	15	ns
t_{PHL}			7.1	13.6	18.5	7.1	21	
t_{PLH}	$\overline{CCLR}$	$\overline{RCO}$	5.1	10.3	14.5	5.1	16.2	ns
t_{PLH}	RCK	$\overline{RCO}$	6.7	12	15.6	6.7	17.7	ns
t_{PHL}			7.5	13.6	17.8	7.5	20.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

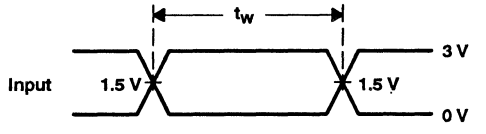
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	61	pF
		Outputs disabled		15	

PARAMETER MEASUREMENT INFORMATION

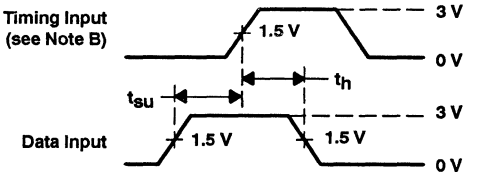


LOAD CIRCUIT

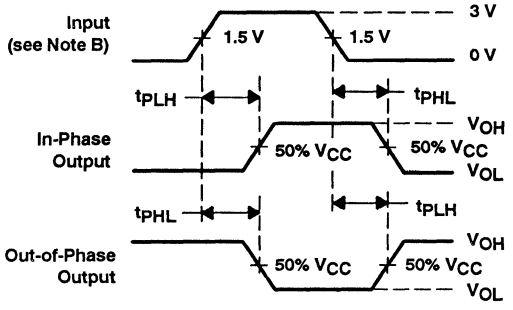
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



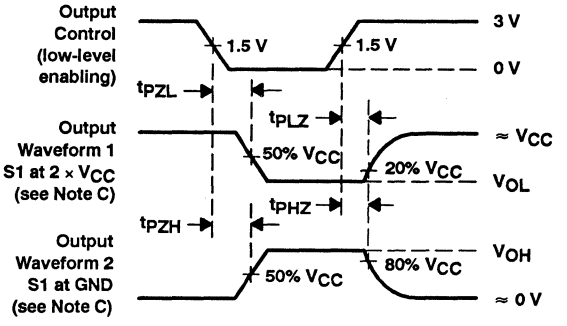
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



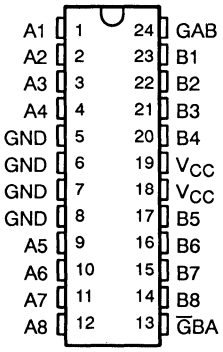
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Local Bus-Latch Capability**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74ACT11623 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 74ACT11623.

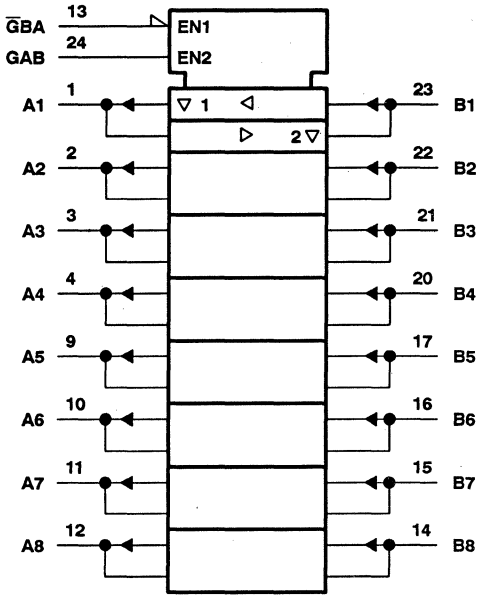
The 74ACT11623 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

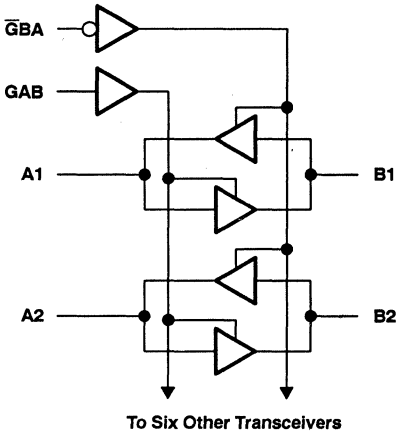
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	– 40	85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_I	$\overline{G}$BA or GAB	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	$\overline{G}$BA or GAB	V_I = V_{CC} or GND	5 V		4				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		20				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

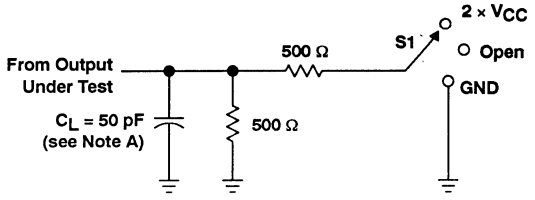
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.5	6	7.5	1.5	8.5	ns
t_{PHL}			1.5	5.5	7.2	1.5	7.9	
t_{PZH}	$\overline{G}$BA	A	1.5	6.9	8.6	1.5	9.7	ns
t_{PZL}			1.5	6.9	9	1.5	10	
t_{PHZ}	$\overline{G}$BA	A	1.5	8.1	10	1.5	10.9	ns
t_{PLZ}			1.5	8.5	10.5	1.5	11.5	
t_{PZH}	GAB	B	1.5	7.7	9.3	1.5	10.7	ns
t_{PZL}			1.5	7.7	9.7	1.5	10.9	
t_{PHZ}	GAB	B	1.5	7.1	8.8	1.5	9.5	ns
t_{PLZ}			1.5	7.3	9.2	1.5	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

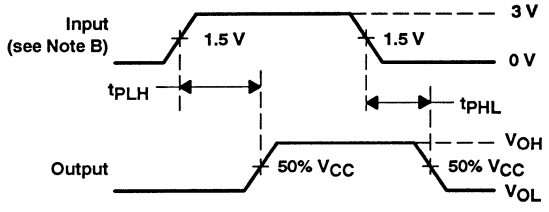
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	41	pF
		Outputs disabled			8	

PARAMETER MEASUREMENT INFORMATION

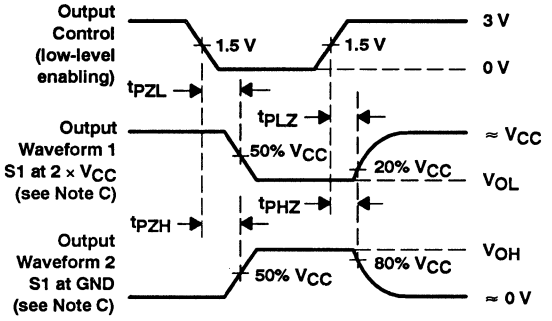


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



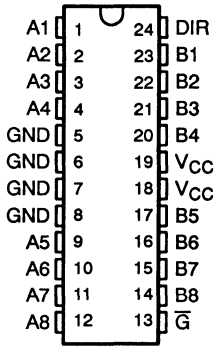
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

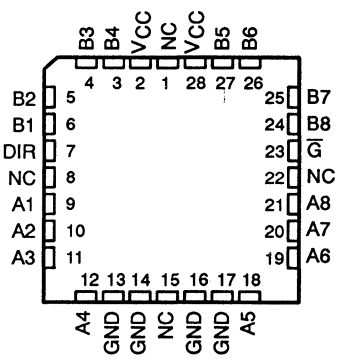
Figure 1. Load Circuit and Voltage Waveforms

- **Bidirectional Bus Transceivers in High-Density 24-Pin Packages**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54ACT11640 . . . JT PACKAGE
74ACT11640 . . . DW OR NT PACKAGE
(TOP VIEW)



54ACT11640 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input $\overline{G}$ is used to disable the device so the buses are effectively isolated.

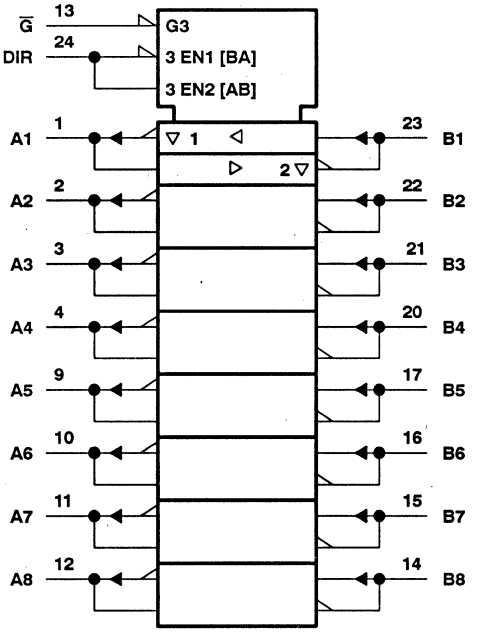
The 54ACT11640 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11640 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

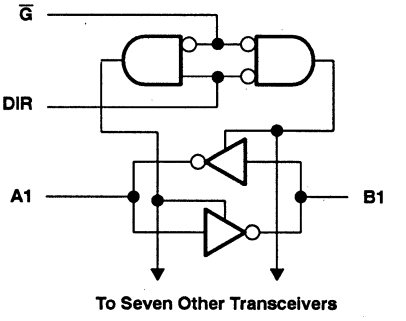
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11640			74ACT11640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11640		74ACT11640		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	$\overline{G}$ or DIR	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$\overline{G}$ or DIR	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

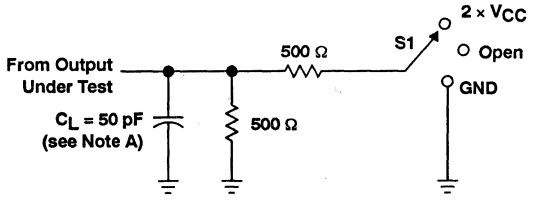
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11640		74ACT11640		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.3	9.6	1.5	11	1.5	10.5	ns
t_{PHL}			1.5	5.7	8.6	1.5	10	1.5	9.5	
t_{PZH}	$\overline{G}$	A or B	1.5	8.8	12.2	1.5	14.2	1.5	13.4	ns
t_{PZL}			1.5	8.4	12.3	1.5	14.5	1.5	13.6	
t_{PHZ}	$\overline{G}$	A or B	1.5	9.1	12.9	1.5	14.5	1.5	13.9	ns
t_{PLZ}			1.5	9.6	13.1	1.5	15	1.5	14.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

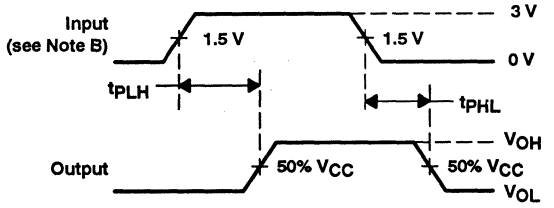
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

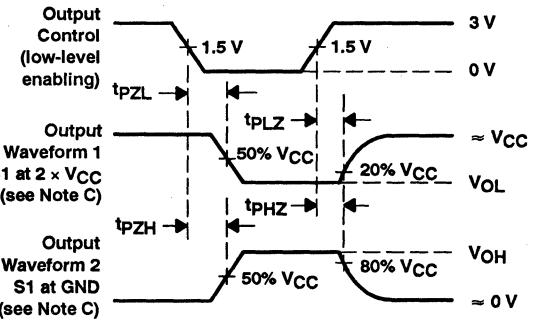


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



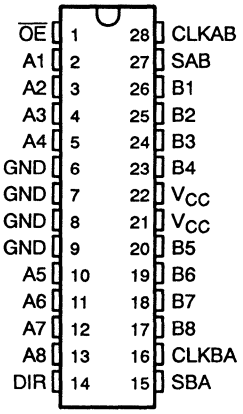
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74AC11646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11646.

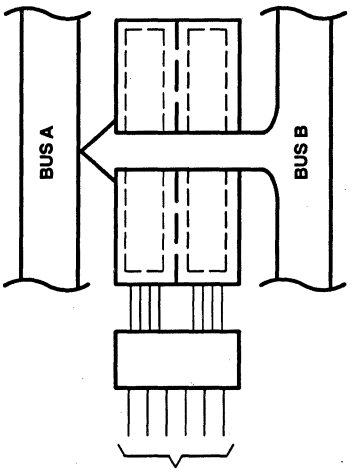
Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

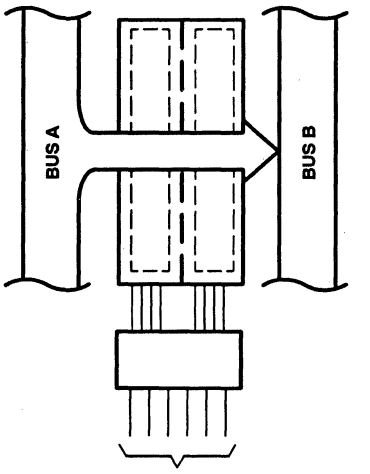
The 74AC11646 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



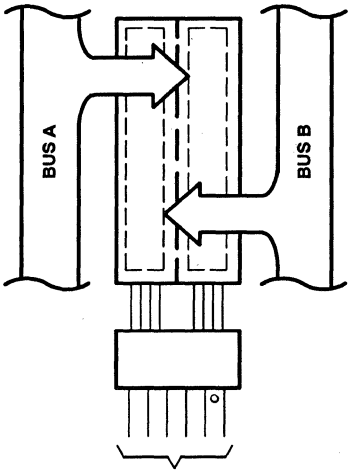
1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



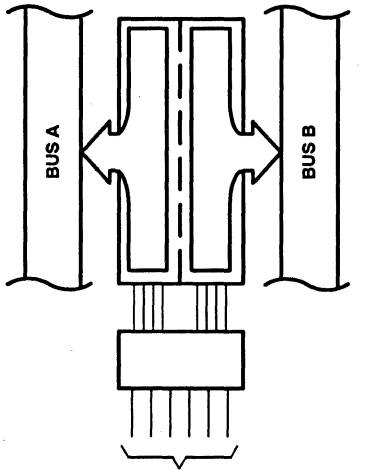
1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

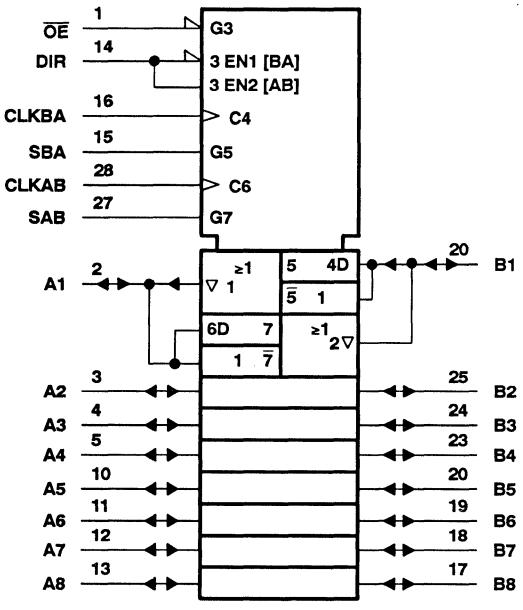
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

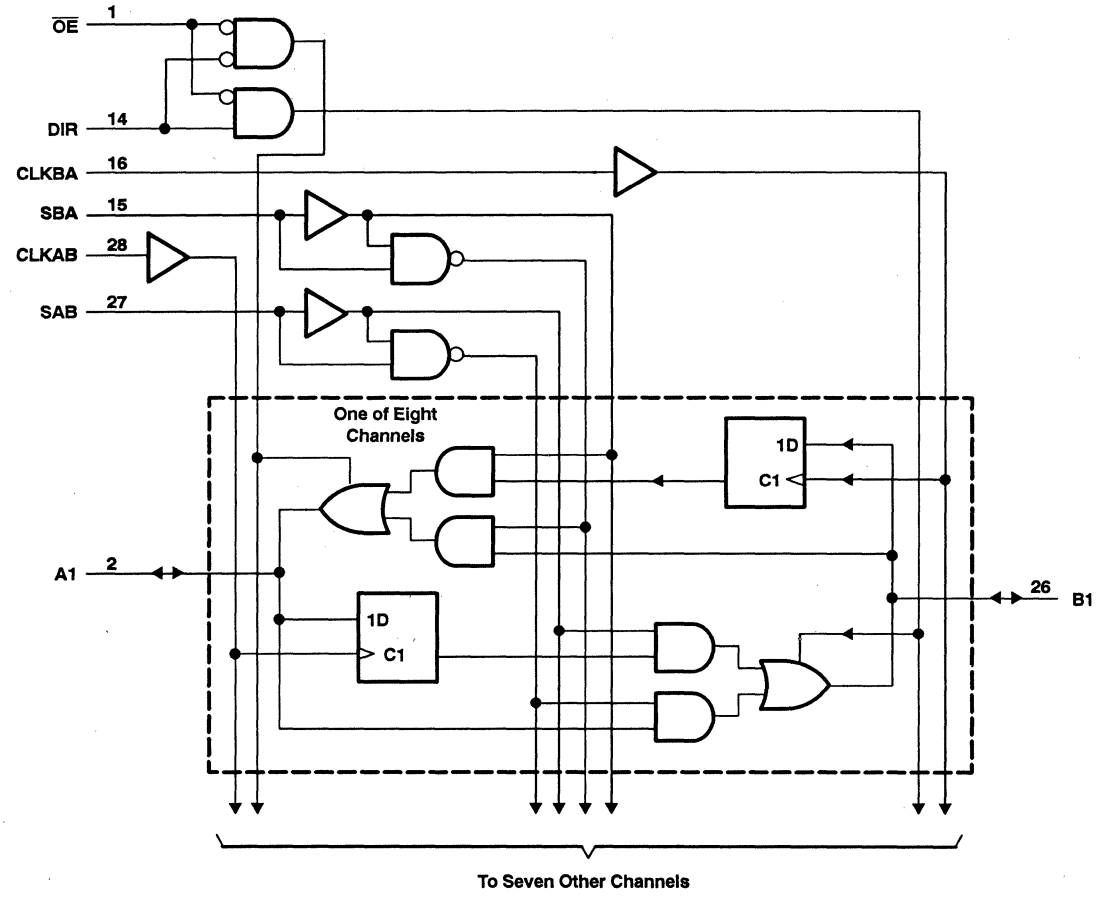
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control pins	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	65	0	65	MHz
t_w	Pulse duration, CLK high or low	7.7		7.7		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	6.5		6.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	100	0	100	MHz
t_w	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	4.5		4.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			65			65		MHz
t_{PLH}	A or B	B or A	1.5	9.1	12.1	1.5	13.8	ns
t_{PHL}			1.5	10.7	13.4	1.5	14.5	
t_{PZH}	$\overline{OE}$	A or B	1.5	13	16.4	1.5	18.7	ns
t_{PZL}			1.5	16.1	20.4	1.5	21.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	7.9	9.6	1.5	10.3	ns
t_{PLZ}			1.5	7.2	8.9	1.5	9.6	
t_{PLH}	CLKBA or CLKAB	A or B	1.5	11.8	15	1.5	17	ns
t_{PHL}			1.5	13.7	16.8	1.5	18.3	
t_{PLH}	SBA or SAB† (A or B high)	A or B	1.5	9.8	12.9	1.5	14.4	ns
t_{PHL}			1.5	12	14.5	1.5	15.8	
t_{PLH}	SBA or SAB† (A or B low)	A or B	1.5	10.7	13.8	1.5	15.4	ns
t_{PHL}			1.5	12.4	15	1.5	16.4	
t_{PZH}	DIR	A or B	1.5	13.7	17.1	1.5	19.4	ns
t_{PZL}			1.5	16.8	21	1.5	23.6	
t_{PHZ}	DIR	A or B	1.5	7.9	9.7	1.5	10.5	ns
t_{PLZ}			1.5	7.3	9.1	1.5	9.9	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

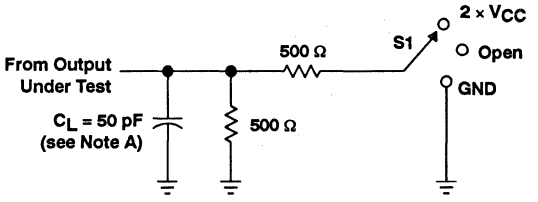
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100			100		MHz
t_{PLH}	A or B	B or A	1.5	5.5	7.9	1.5	8.8	ns
t_{PHL}			1.5	6.3	8.9	1.5	9.8	
t_{PZH}	$\overline{OE}$	A or B	1.5	7.8	10.7	1.5	12	ns
t_{PZL}			1.5	8.5	11.9	1.5	13.1	
t_{PHZ}	$\overline{OE}$	A or B	1.5	5.9	8.4	1.5	8.9	ns
t_{PLZ}			1.5	5.9	7.7	1.5	8.3	
t_{PLH}	CLKBA or CLKAB	A or B	1.5	7	9.7	1.5	11	ns
t_{PHL}			1.5	8.2	11	1.5	12.2	
t_{PLH}	SBA or SAB† (A or B high)	A or B	1.5	5.9	8.4	1.5	9.4	ns
t_{PHL}			1.5	7.2	9.8	1.5	10.7	
t_{PLH}	SBA or SAB† (A or B low)	A or B	1.5	6.3	8.9	1.5	9.9	ns
t_{PHL}			1.5	7.3	9.9	1.5	11	
t_{PZH}	DIR	A or B	1.5	8.4	11.2	1.5	12.6	ns
t_{PZL}			1.5	9.1	12.3	1.5	13.7	
t_{PHZ}	DIR	A or B	1.5	6.3	8.2	1.5	8.7	ns
t_{PLZ}			1.5	5.7	7.5	1.5	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

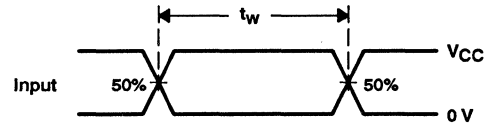
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		15	

PARAMETER MEASUREMENT INFORMATION

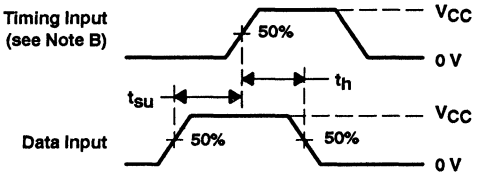


LOAD CIRCUIT

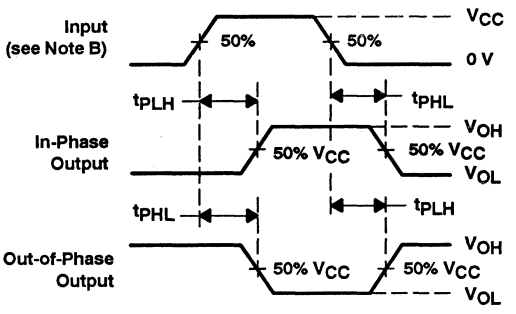
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



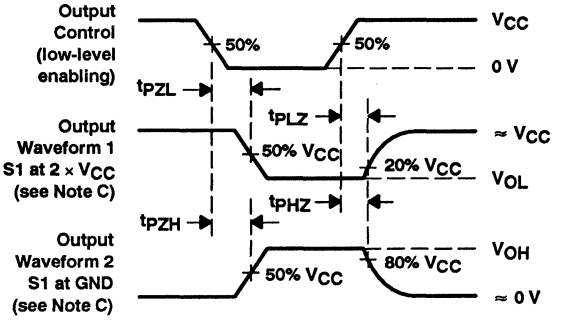
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



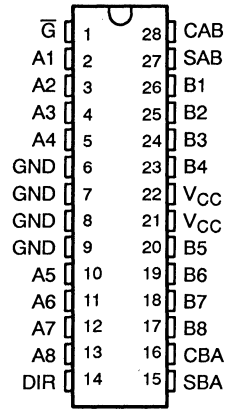
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

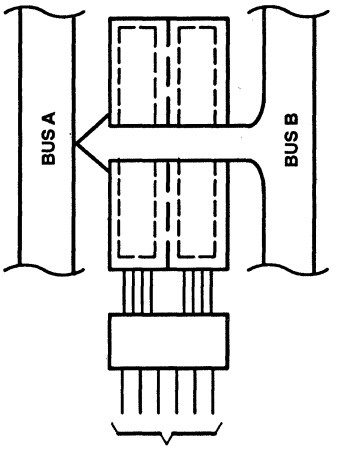
These devices consist of bus transceiver circuits, 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

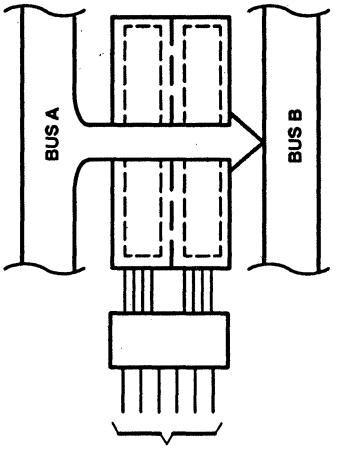
The 74ACT11646 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



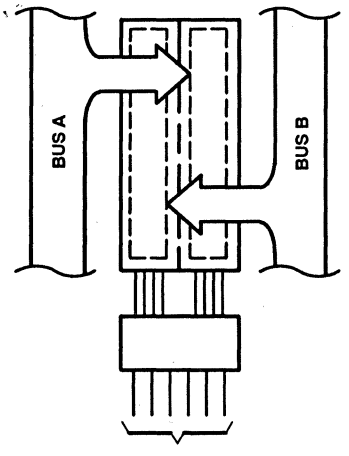
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



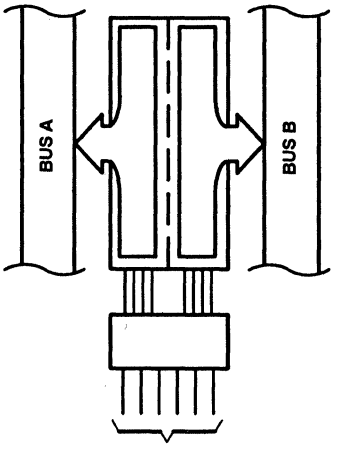
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

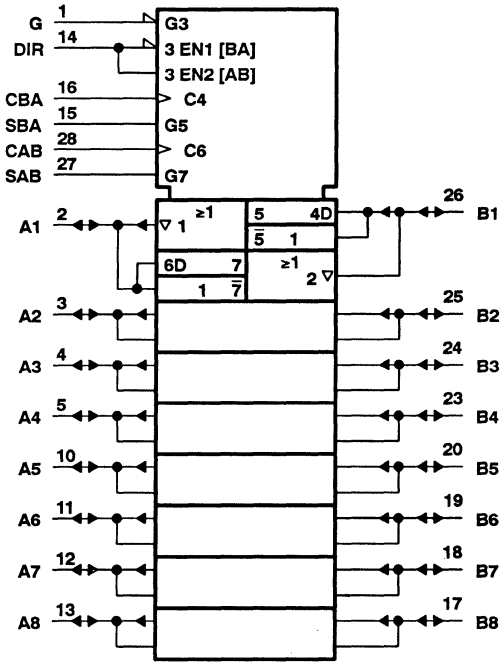
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

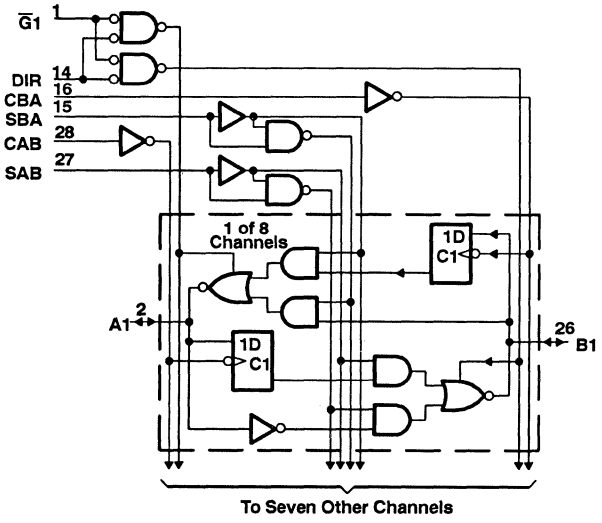
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA‡	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA‡	5.5 V					1.65	
I_{OZ}	A or B ports§	V_O = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_I	$\overline{G}$ or DIR	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}¶		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i		V_I = V_{CC} or GND	5 V		4.5				pF
C_o		V_O = V_{CC} or GND	5 V		12				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§ For I/O ports, the parameter I_{OZ} includes the leakage current.
¶ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	105	0	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8		4.8		ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑	4.5		4.5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2.5		2.5		ns

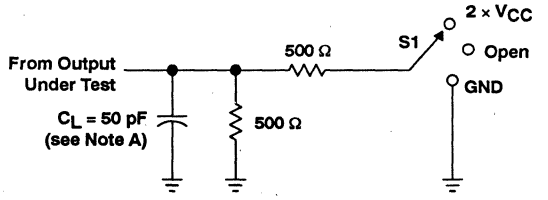
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			105			105		MHz
t_{PLH}	A or B	B or A	1.5	7.3	10.1	1.5	11.5	ns
t_{PHL}			1.5	7.2	11	1.5	12	
t_{PZH}	$\overline{G}$	A or B	1.5	7.7	12.8	1.5	14.4	ns
t_{PZL}			1.5	9.2	13.8	1.5	15.3	
t_{PHZ}	$\overline{G}$	A or B	1.5	8.6	10.7	1.5	11.6	ns
t_{PLZ}			1.5	7.8	9.7	1.5	10.6	
t_{PLH}	CBA or CAB	A or B	1.5	8.8	11.9	1.5	13.5	ns
t_{PHL}			1.5	10	13.4	1.5	14.9	
t_{PZH}	DIR	A or B	1.5	10.2	13.7	1.5	15.3	ns
t_{PZL}			1.5	10.9	14.8	1.5	16.5	
t_{PHZ}	DIR	A or B	1.5	7.9	10.5	1.5	11.3	ns
t_{PLZ}			1.5	7.3	9.5	1.5	10.3	
t_{PLH}	SBA or SAB (A or B high)	A or B	1.5	6.7	10.3	1.5	11.5	ns
t_{PHL}			1.5	9.1	12.1	1.5	13.5	
t_{PLH}	SBA or SAB (A or B low)	A or B	1.5	8	10.9	1.5	12.4	ns
t_{PHL}			1.5	8.1	11.9	1.5	13.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

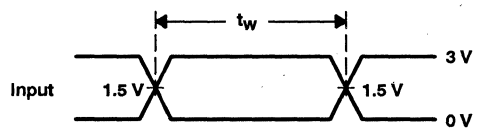
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	63	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

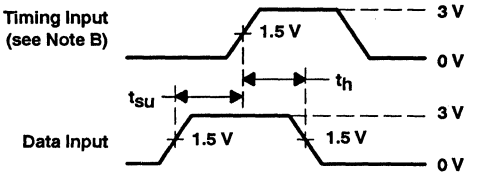


LOAD CIRCUIT

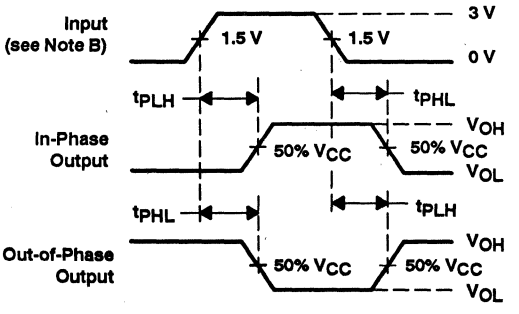
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



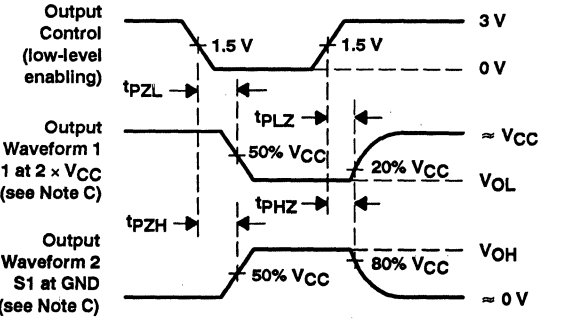
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
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C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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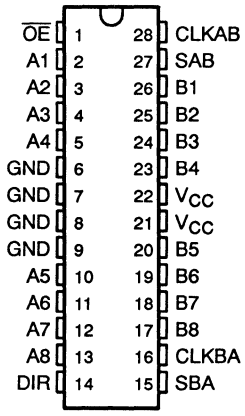
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74AC11648 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11648.

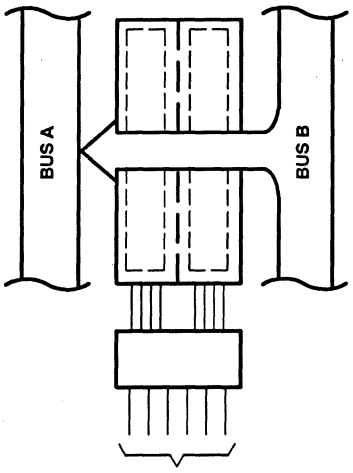
Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

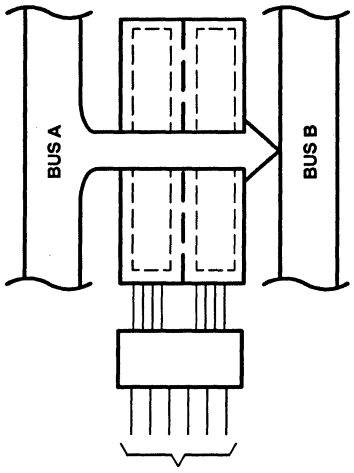
The 74AC11648 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



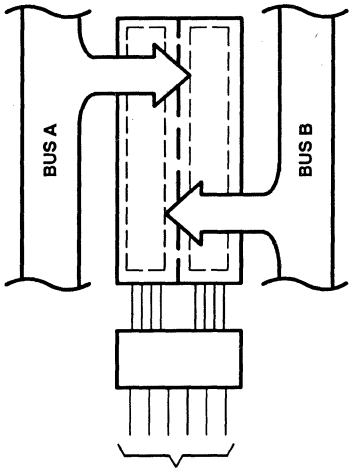
1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



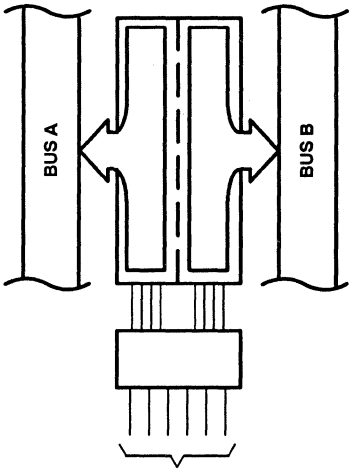
1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



1	14	28	16	27	15
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

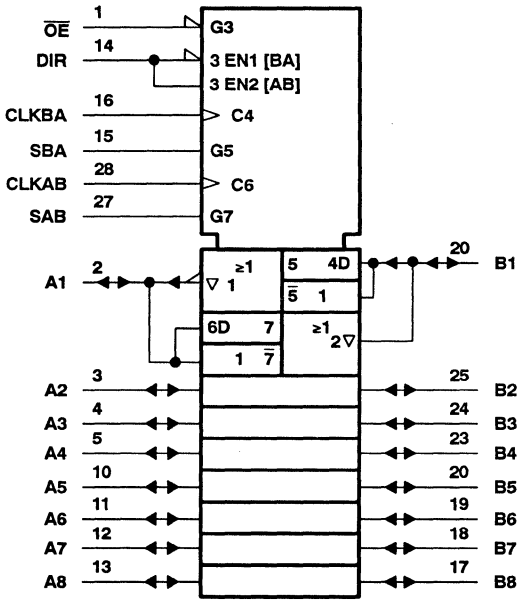
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

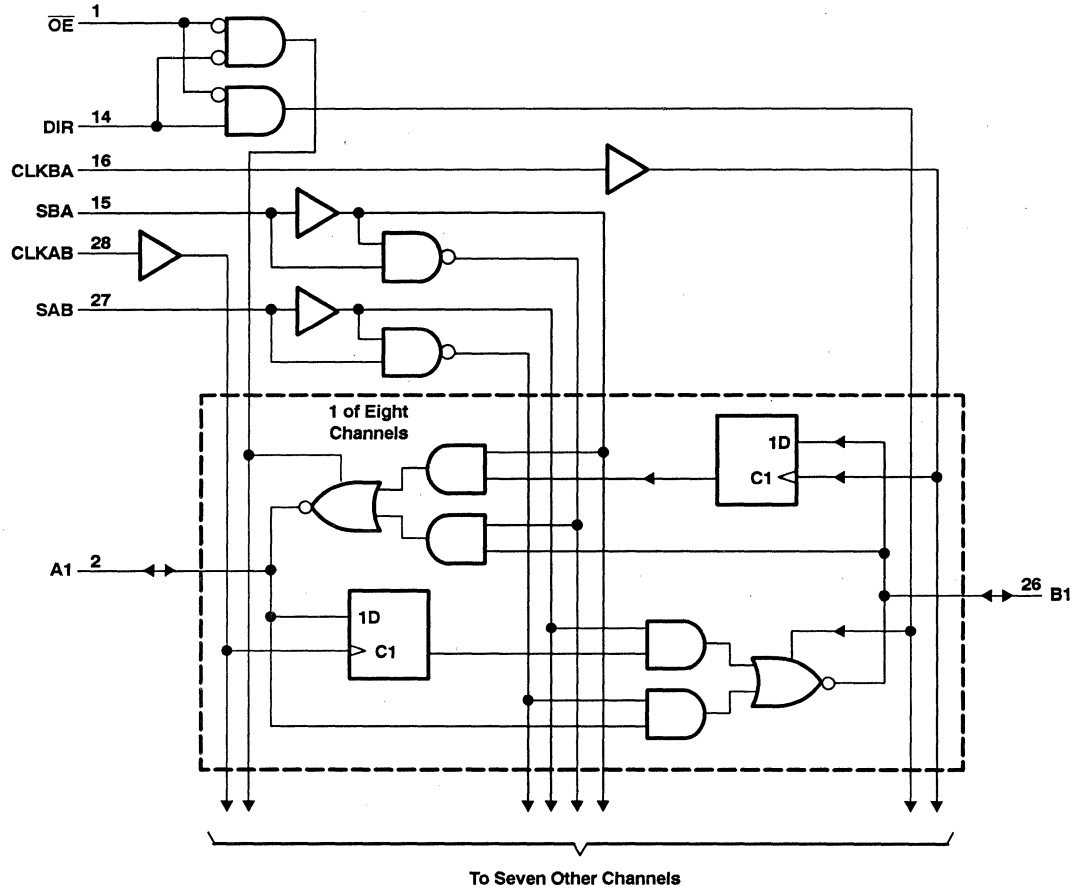
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	40	0	40	MHz
t_w	Pulse duration, CLK high or low	12.5		12.5		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	6.5		6.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	90	0	90	MHz
t_w	Pulse duration, CLK high or low	5.6		5.6		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	4.5		4.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			40			40		MHz
t_{PLH}	A or B	B or A	3	8.7	12.6	3	14.3	ns
t_{PHL}			3.8	9.3	14.4	3.8	15.9	
t_{PZH}	$\overline{OE}$	A or B	5	11.1	17.2	5	19.4	ns
t_{PZL}			5.2	12.8	20.5	5.2	23	
t_{PHZ}	$\overline{OE}$	A or B	4.1	7.2	9.9	4.1	10.6	ns
t_{PLZ}			3.7	6.5	9.1	3.7	9.7	
t_{PLH}	CLKBA or CLKAB	A or B	4.3	10.1	15.6	4.3	17.6	ns
t_{PHL}			5.2	11.5	17.6	5.2	19.4	
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.7	9.1	14.1	3.7	15.8	ns
t_{PHL}			4.5	10.3	15.9	4.5	17.4	
t_{PLH}	SBA or SAB† (A or B low)	A or B	3.2	8.6	13.6	3.2	15.3	ns
t_{PHL}			4.6	10.3	15.6	4.6	17.1	
t_{PZH}	DIR	A or B	4.9	11.6	18.2	4.9	20.6	ns
t_{PZL}			5.2	14.2	21.6	5.2	24.3	
t_{PHZ}	DIR	A or B	3.8	7.1	10.1	3.8	10.9	ns

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

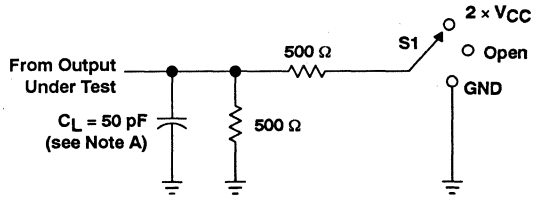
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			90			90		MHz
t_{PLH}	A or B	B or A	2.6	5.6	8.3	2.6	9.5	ns
t_{PHL}			3.2	6.4	9.4	3.2	10.6	
t_{PZH}	$\overline{OE}$	A or B	4.2	7.8	11.3	4.2	12.8	ns
t_{PZL}			4.1	8.1	12	4.1	13.6	
t_{PHZ}	$\overline{OE}$	A or B	3.8	6.3	8.6	3.8	9.2	ns
t_{PLZ}			3.5	5.7	7.8	3.5	8.4	
t_{PLH}	CLKBA or CLKAB	A or B	3.6	6.9	10	3.6	11.4	ns
t_{PHL}			4.3	8	11.4	4.3	12.8	
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.1	6.2	9.2	3.1	10.4	ns
t_{PHL}			3.8	7.6	10.4	3.8	11.6	
t_{PLH}	SBA or SAB† (A or B low)	A or B	2.8	6.1	8.9	2.8	10.1	ns
t_{PHL}			3.8	7.3	10.4	3.8	11.6	
t_{PZH}	DIR	A or B	4	8	11.9	4	13.4	ns
t_{PZL}			4.1	8.4	12.7	4.1	14.4	
t_{PHZ}	DIR	A or B	3.5	6.1	8.5	3.5	9.1	ns
t_{PLZ}			3.4	5.9	7.8	3.4	8.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

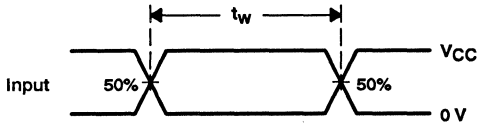
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	66	pF
		Outputs disabled		17	

PARAMETER MEASUREMENT INFORMATION

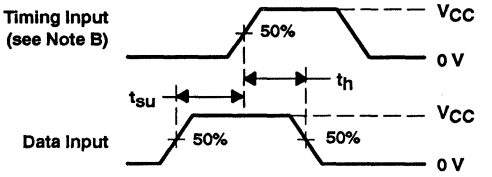


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

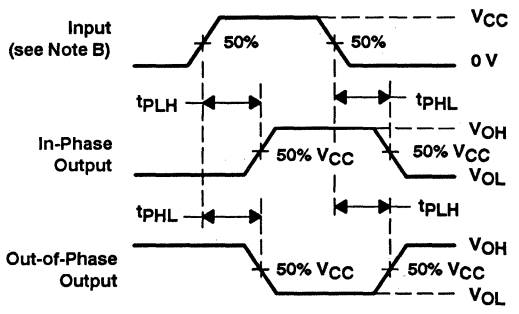
LOAD CIRCUIT



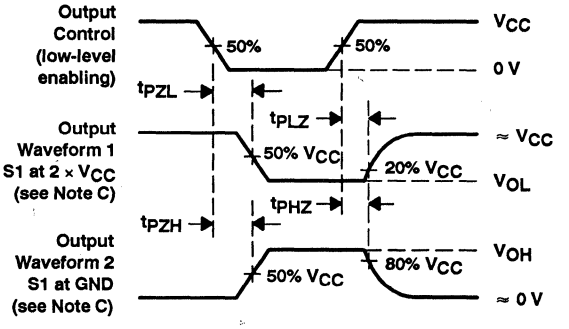
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



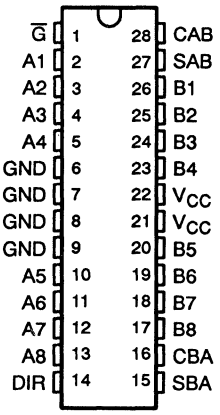
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11648 consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). Examples of the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers are shown in Figure 1.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a mulitplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT11648 is characterized for operation from – 40°C to 85°C.

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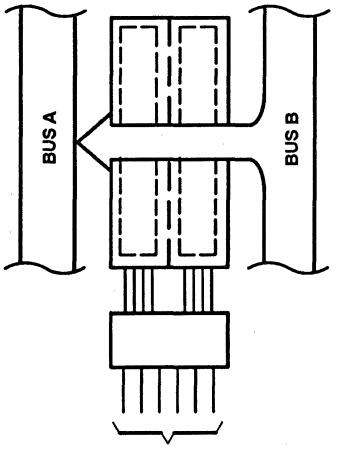
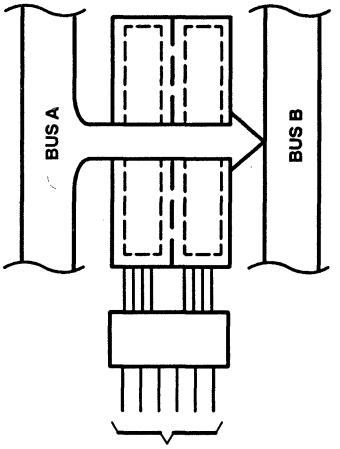


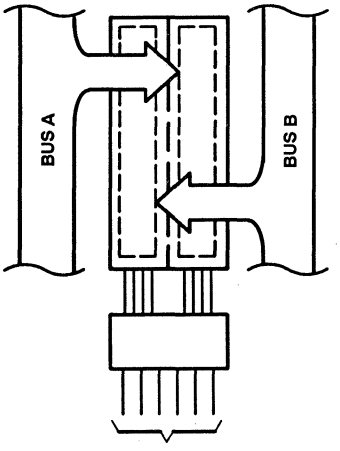
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



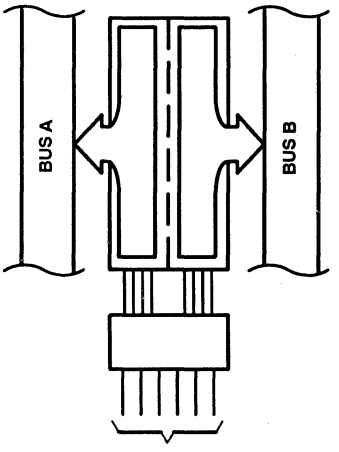
1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B, OR A AND B



1	14	28	16	27	15
$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

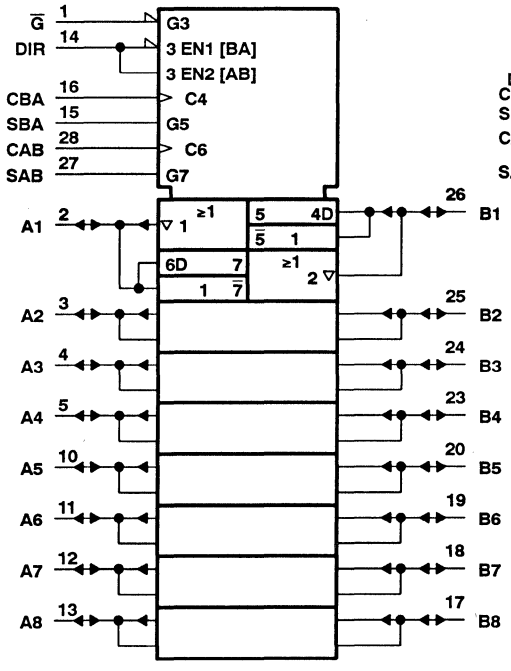
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus

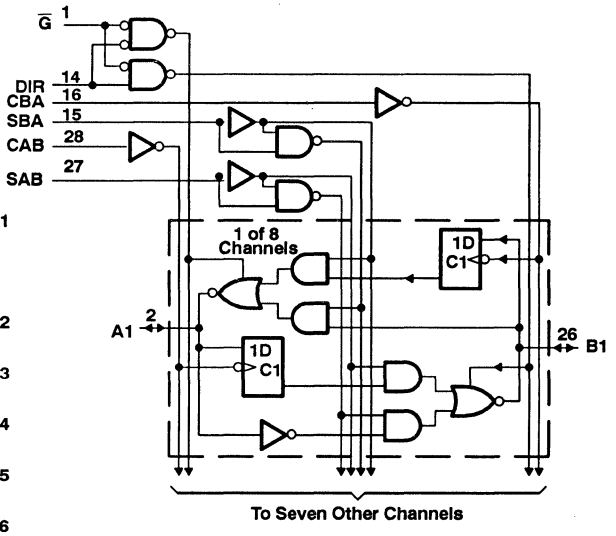
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control Inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	A or B ports‡	V_I = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control Inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_I = V_{CC} or GND	5 V		12				

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended range of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	90	0	75	MHz
t_w	Pulse duration, CAB or CBA high or low	6.7		6.7		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	5		5		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2		2		ns

switching characteristics over recommended ranges of supply voltage operating free-air temperature (unless otherwise noted) (see Figure 2)

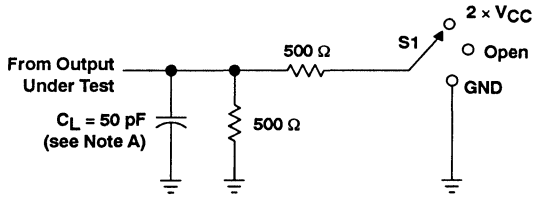
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75			75		MHz
t_{PLH}	A or B	B or A	2.4	6.5	9.5	2.4	10.7	ns
t_{PHL}			4.4	8.5	11.3	4.4	12.7	
t_{PZH}	$\overline{G}$	A or B	4.2	9.2	13	4.2	14.6	ns
t_{PZL}			4.3	9.8	13.9	4.3	15.6	
t_{PHZ}	$\overline{G}$	A or B	5.7	8.7	11.3	5.7	12.2	ns
t_{PLZ}			5.3	8.1	10.5	5.3	11.4	
t_{PLH}	CBA or CAB	A or B	5.2	9.4	12	5.2	13.7	ns
t_{PHL}			6	10.5	13.5	6	15.2	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4.7	8.6	11.3	4.7	12.9	ns
t_{PHL}			3.8	8.6	12	3.8	13.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	2.6	7.1	10.2	2.6	11.5	ns
t_{PHL}			5.4	9.7	12.6	5.4	14.1	
t_{PZH}	DIR	A or B	3.9	9.8	14.9	3.9	16.9	ns
t_{PZL}			3.9	10.8	15.1	3.9	17.2	
t_{PHZ}	DIR	A or B	4.5	8.2	10.6	4.5	11.5	ns
t_{PLZ}			3.9	7.3	9.6	3.9	11.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

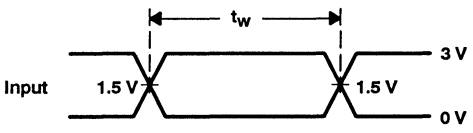
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceivers	Outputs enabled	C_L = 50 pF, f = 1 MHz	61	pF
		Outputs disabled		15	

PARAMETER MEASUREMENT INFORMATION

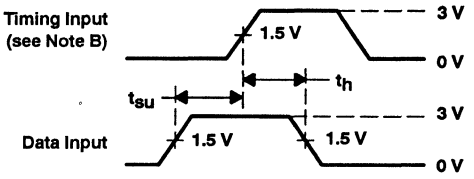


LOAD CIRCUIT

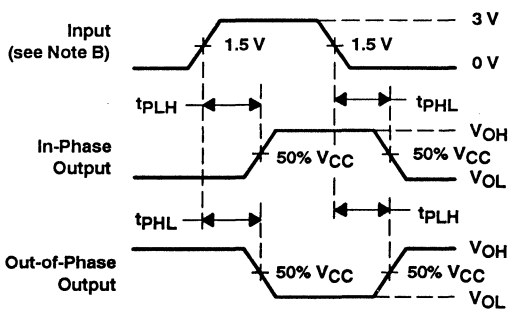
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



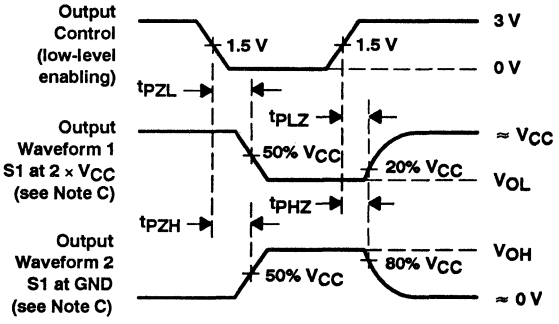
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



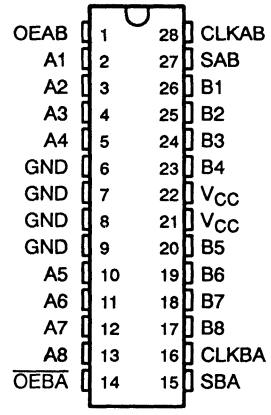
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Inverting Data Paths**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74AC11652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all the other data sources to the two sets of bus lines are at high impedance, each set will remain at its last state.

The 74AC11652 is characterized for operation from −40°C to 85°C.

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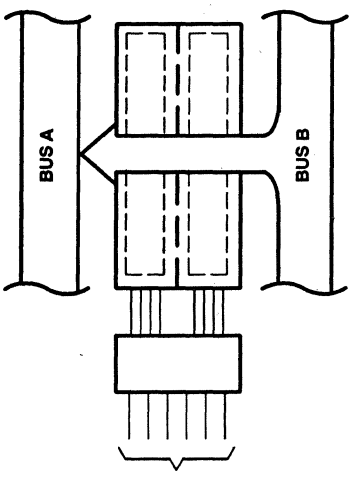
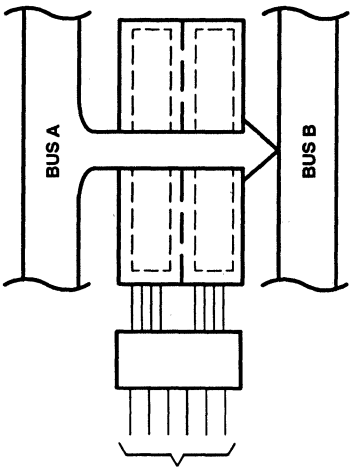


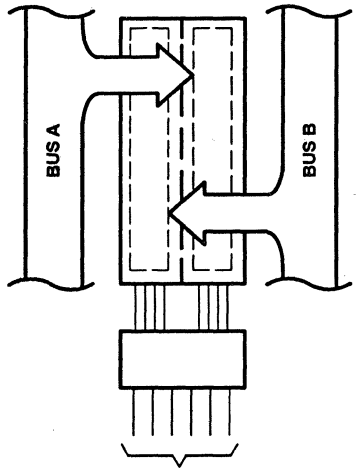
1	14	28	16	27	15
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



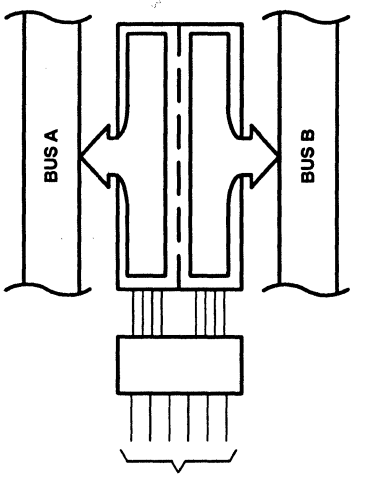
1	14	28	16	27	15
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



1	14	28	16	27	15
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



1	14	28	16	27	15
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

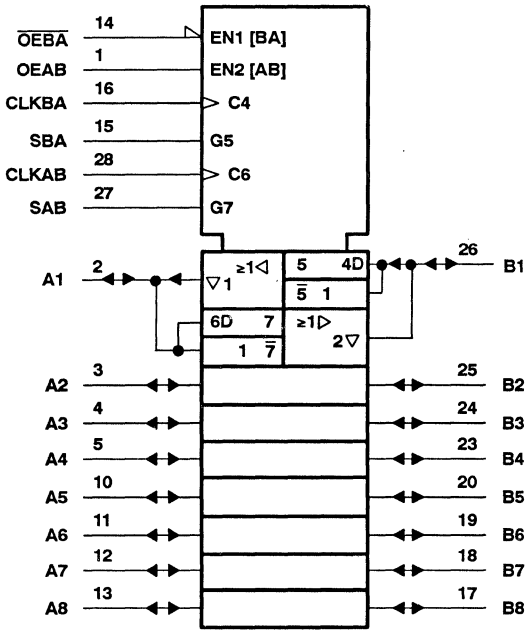
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

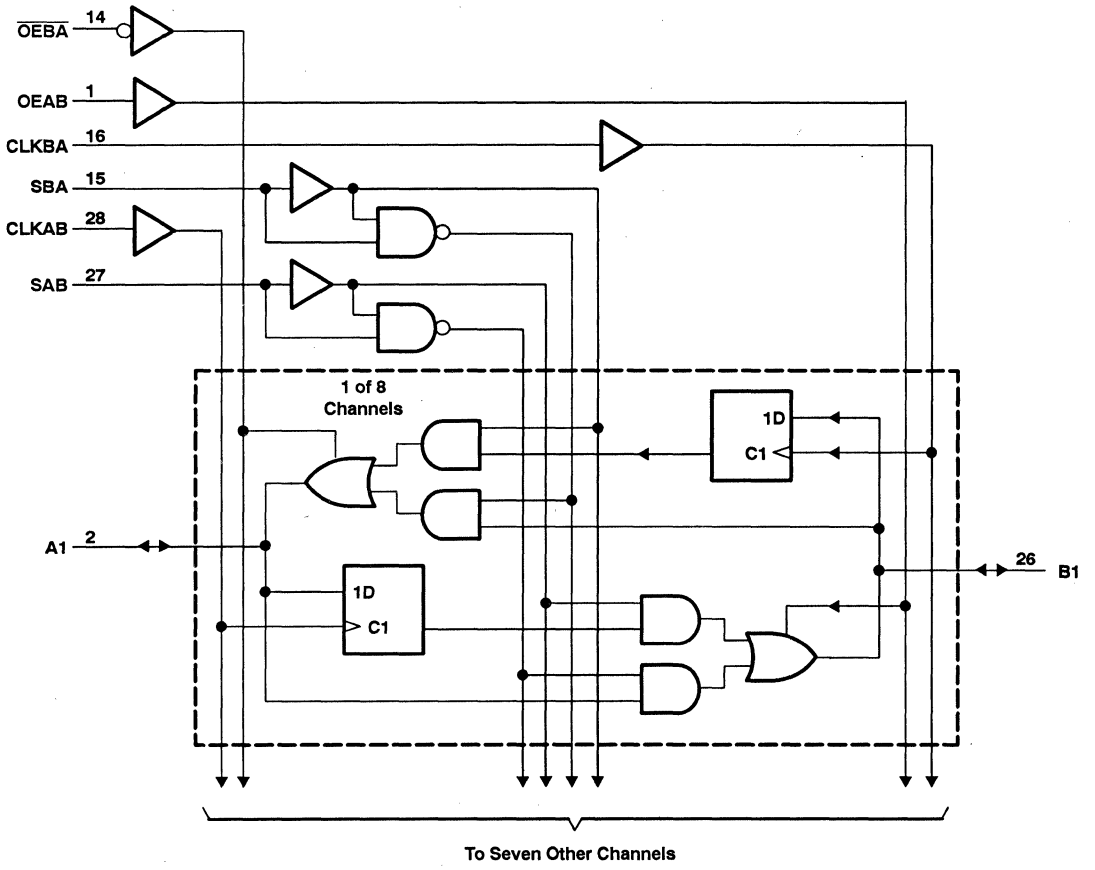
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins	0		5	ns/V
		Data	0		10	
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	65	0	65	MHz
t_w	Pulse duration, CLK high or low	7.7		7.7		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	6		6		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	105	0	105	MHz
t_w	Pulse duration, CLK high or low	4.8		4.8		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	4.5		4.5		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			65			65		MHz
t_{PLH}	A or B	B or A	2.9	8.5	11.1	2.9	12.9	ns
t_{PHL}			3.9	10.3	12.9	3.9	14.2	
t_{PLH}	CLKBA or CLKAB	A or B	4.3	11.2	14.3	4.3	16.2	ns
t_{PHL}			5.3	13.1	16.2	5.3	17.8	
t_{PLH}	SBA or SAB† (A or B high)	A or B	3.4	9.4	12	3.4	13.7	ns
t_{PHL}			4.7	11.5	14.3	4.7	15.6	
t_{PLH}	SBA or SAB† (A or B low)	A or B	3.9	10.5	13.3	3.9	14.9	ns
t_{PHL}			4.8	12.1	16.3	4.8	17.7	
t_{PZH}	$\overline{OEBA}$	A	4.3	11.1	14.5	4.3	16.5	ns
t_{PZL}			5.2	14.4	19.8	5.2	22	
t_{PHZ}	$\overline{OEBA}$	A	3.7	6.4	8.1	3.7	8.5	ns
t_{PLZ}			3.5	6	7.8	3.5	8.2	
t_{PZH}	OEAB	B	4.7	11.6	15	4.7	16.9	ns
t_{PZL}			5.6	14.8	19.9	5.6	21.9	
t_{PHZ}	OEAB	B	4	6.6	8.2	4	8.6	ns
t_{PLZ}			3.5	6.1	7.7	3.5	8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

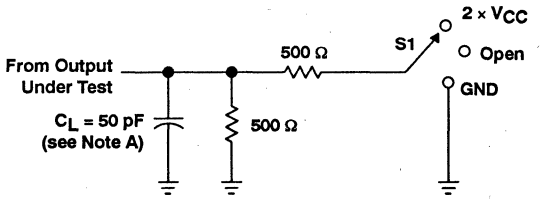
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			105			105		MHz
t_{PLH}	A or B	B or A	2.4	5.2	7.6	2.4	8.6	ns
t_{PHL}			3.1	6	8.7	3.1	9.6	
t_{PLH}	CLKBA or CLKAB	A or B	3.6	6.7	9.5	3.6	10.7	ns
t_{PHL}			4.4	7.8	10.8	4.4	12	
t_{PLH}	SBA or SAB† (A or B high)	A or B	2.9	5.6	8.1	2.9	9.1	ns
t_{PHL}			3.8	6.9	9.6	3.8	10.7	
t_{PLH}	SBA or SAB† (A or B low)	A or B	3.3	6.2	8.8	3.3	9.9	ns
t_{PHL}			4	7.1	9.9	4	10.9	
t_{PZH}	$\overline{OEBA}$	A	3.3	6.6	9.6	3.3	10.9	ns
t_{PZL}			4.2	7.4	10.9	4.2	12.2	
t_{PHZ}	$\overline{OEBA}$	A	3.6	5.5	7.2	3.6	7.6	ns
t_{PLZ}			3.3	5	6.7	3.3	7.1	
t_{PZH}	OEAB	B	4.1	7.2	10.1	4.1	11.3	ns
t_{PZL}			4.6	7.9	11.1	4.6	12.3	
t_{PHZ}	OEAB	B	3.9	5.6	7.3	3.9	7.6	ns
t_{PLZ}			3.4	5.2	6.8	3.4	7.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

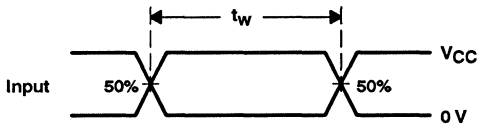
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	60	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

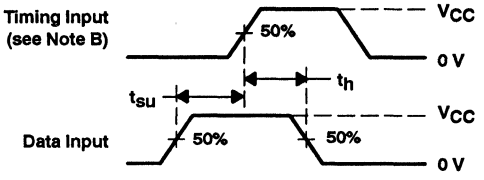


LOAD CIRCUIT

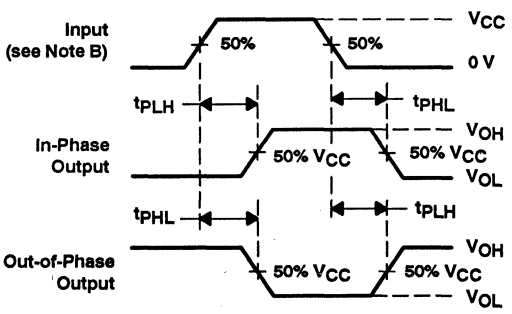
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



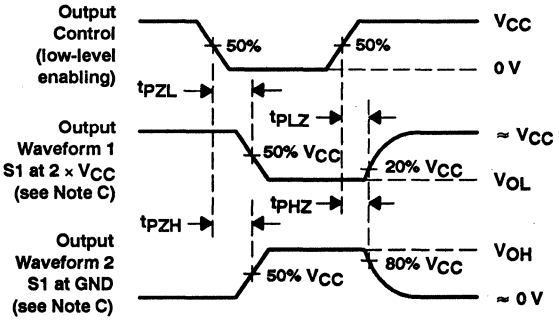
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



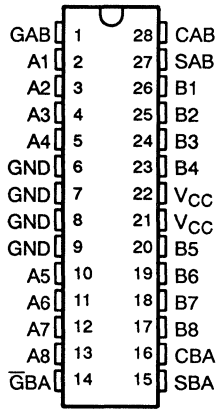
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

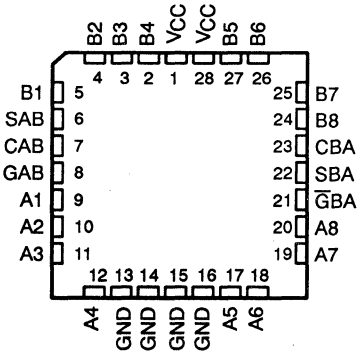
Figure 2. Load Circuit and Voltage Waveforms

- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic DIPs**

54ACT11652 . . . JT PACKAGE
74ACT11652 . . . DW PACKAGE
(TOP VIEW)



54ACT11652 . . . FK PACKAGE
(TOP VIEW)



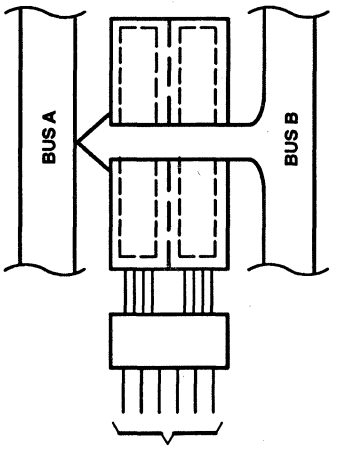
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}$BA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}$BA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

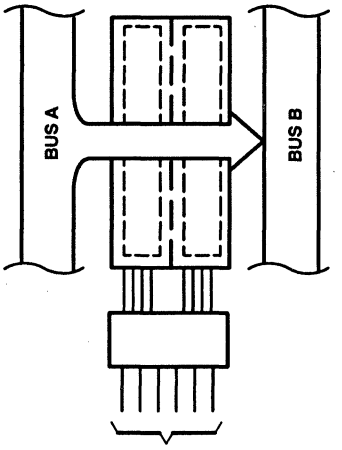
The 54ACT11652 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11652 is characterized for operation from – 40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.



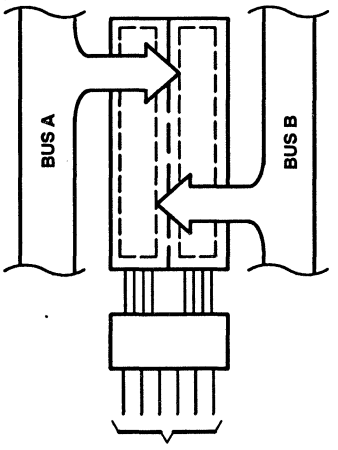
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



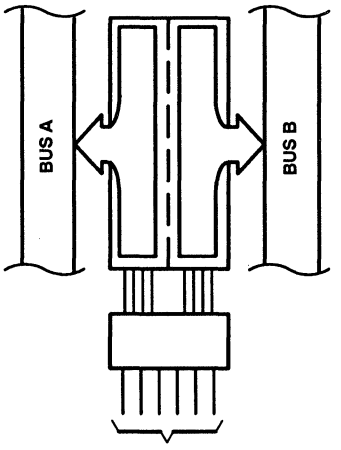
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	H or L	H or L	X	H

TRANSFER STORED DATA TO A AND/OR B

Figure 1. Bus Transfer Diagram

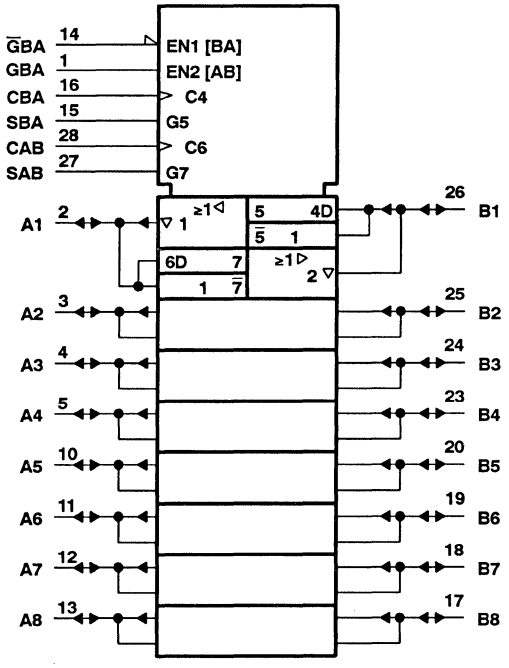
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified†	Input	Hold A, Store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

† The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

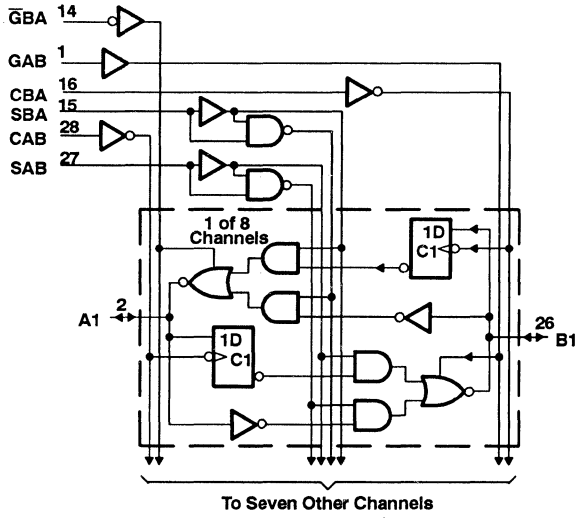
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... − 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 200 mA
Storage temperature range ..... − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11652		74ACT11652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage		V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11652		74ACT11652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	GAB or $\overline{GBA}$	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	GAB or $\overline{GBA}$	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	A or B ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER		T_A = 25°C		54ACT11652		74ACT11652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	105	0		0	105	MHz
t_w	Pulse duration, CAB or CBA high or low	4.8				4.8		ns
t_{su}	Setup time, A before CLK↑ or B before CBA↑	4				4		ns
t_h	Hold time, A after CAB↑ or B after CBA↑	2.5				2.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

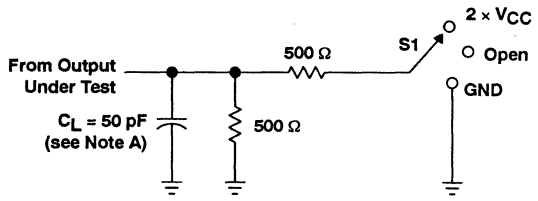
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11652		74ACT11652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			105			105		105		MHz
t_{PLH}	A or B	B or A	3.8	7	9.9	3.8	11.9	3.8	11.1	ns
t_{PHL}			3.4	6.7	10.7	3.4	12.2	3.4	11.6	
t_{PLH}	CBA or CAB	A or B	5.4	8.4	11.8	5.4	14.1	5.4	13.1	ns
t_{PHL}			6.1	9.4	13.1	6.1	15.3	6.1	14.4	
t_{PLH}	SBA or SAB† with A or B high	A or B	2.8	6.2	10.1	2.8		2.8	11	ns
t_{PHL}			5.5	8.7	12.1	5.5		5.5	13.3	
t_{PLH}	SBA or SAB† with A or B low	A or B	4.9	7.8	11			4.9	12.2	ns
t_{PHL}			3.9	7.5	11.6	3.9	13.3	3.9	12.6	
t_{PZH}	$\overline{G}BA$	A	3.3	7.2	11.4	3.3	13.5	3.3	12.6	ns
t_{PZL}			4.1	7.8	12.6		14.7	4.1	13.8	
t_{PHZ}	$\overline{G}BA$	A	5.2	7.2	9.3		10.4	5.2	9.9	ns
t_{PLZ}			4.8	6.7	8.6	4.8	9.7	4.8	9.3	
t_{PZH}	GAB	B	5.1	9.1	13.4	5.1	16.7	5.1	15.2	ns
t_{PZL}			5.8	9.7	14.2	5.8	17.6	5.8	16.1	
t_{PHZ}	GAB	B	3.4	6.8	9.7	3.4	10.8	3.4	10.3	ns
t_{PLZ}			3.1	6	8.8	3.1	9.7	3.1	9.3	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

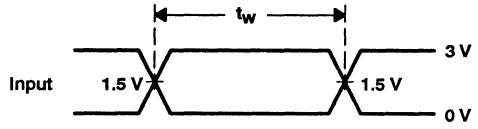
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

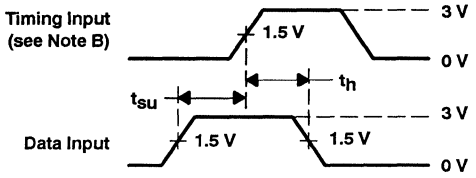


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

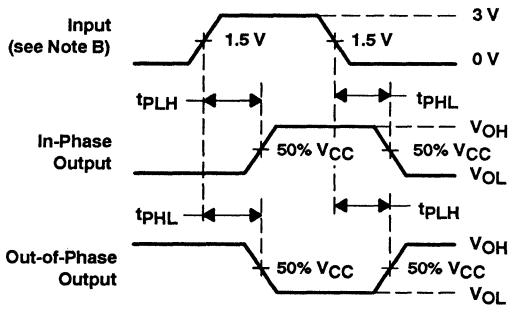
LOAD CIRCUIT



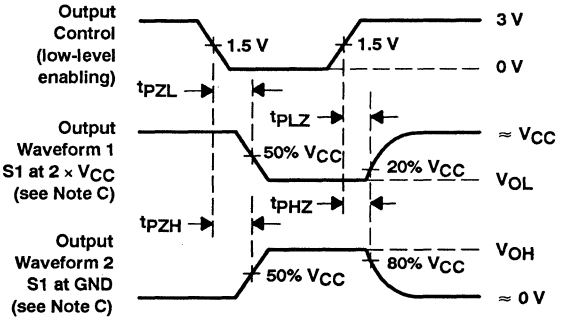
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



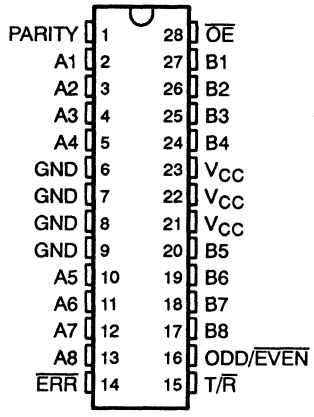
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11657 contains eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker and is intended for bus-oriented applications.

The transmit/receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceivers. When T/$\overline{R}$ is high, data flows from the A port to the B port (transmit mode); when T/$\overline{R}$ is low, data flows from the B port to the A port (receive mode). When the output-enable ($\overline{OE}$) input is high, both the A and B ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the ODD/$\overline{EVEN}$ input. PARITY carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the A bus is polled to determine the number of high bits, PARITY is set to the logic level that maintains the parity sense selected by the level at the ODD/$\overline{EVEN}$ input. For example, if ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the A bus, then PARITY is set to the logic high level so that an even number of the nine total bits (eight A-bus bits plus parity bit) are high.

In the receive mode, after the B bus is polled to determine the number of high bits, the $\overline{ERR}$ output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if ODD/$\overline{EVEN}$ is high (odd parity selected), PARITY is high, and there are three high bits on the B bus, then $\overline{ERR}$ is low, indicating a parity error.

The 74ACT11657 is characterized for operation from −40°C to 85°C.

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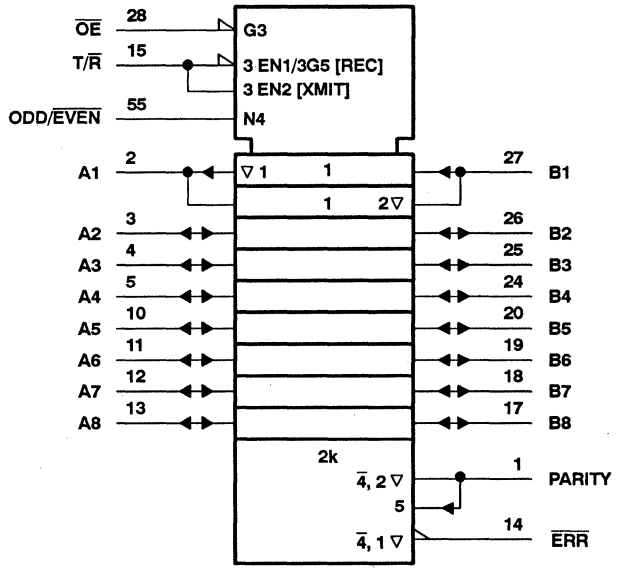
FUNCTION TABLE

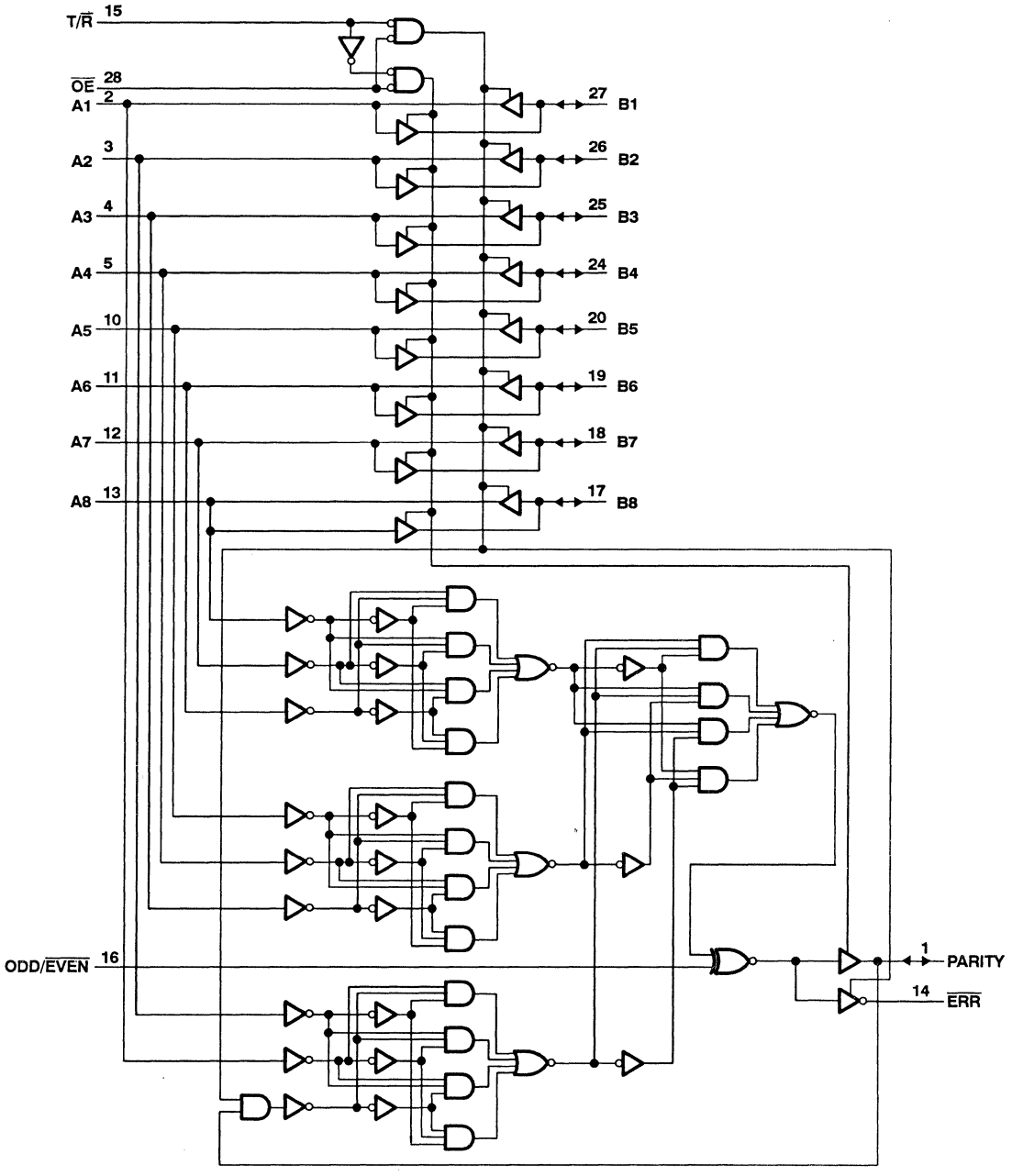
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	A or B ports	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	Control Inputs	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	PARITY/$\overline{ERR}$	V_O = V_{CC} or GND	5 V		10				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

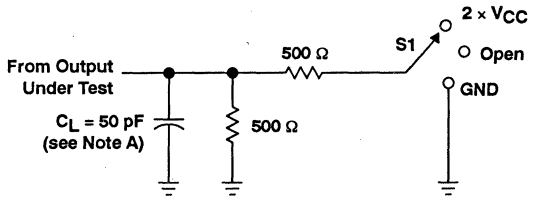
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.9	6.7	8.4	2.9	9.4	ns
t_{PHL}			2.2	7	8.4	2.2	9.4	
t_{PLH}	A	PARITY	3.4	10.4	12.7	3.4	14.4	ns
t_{PHL}			3.9	10.9	13.2	3.9	15	
t_{PLH}	ODD/$\overline{EVEN}$	PARITY, $\overline{ERR}$	2.5	7.9	9.4	2.5	10.7	ns
t_{PHL}			3	8.5	10	3	11.3	
t_{PLH}	B	$\overline{ERR}$	4.6	18.1	20.6	4.6	23.6	ns
t_{PHL}			4.9	18.5	21.8	4.9	24.6	
t_{PLH}	PARITY	$\overline{ERR}$	4	10.9	12.8	4	14.6	ns
t_{PHL}			3.9	11	12.9	3.9	14.7	
t_{PZH}	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	2.6	9.1	10.8	2.6	12.1	ns
t_{PZL}			3.1	10.6	12.3	3.1	13.8	
t_{PHZ}	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	4.5	9.1	10.8	4.5	12.1	ns
t_{PLZ}			4.5	8.7	10.5	4.5	11.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

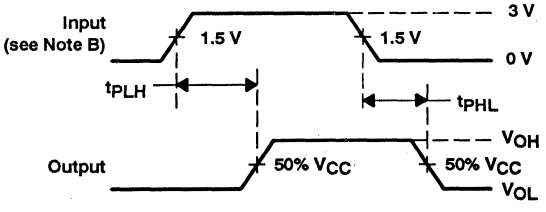
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	95	pF
		Outputs disabled		21	

PARAMETER MEASUREMENT INFORMATION

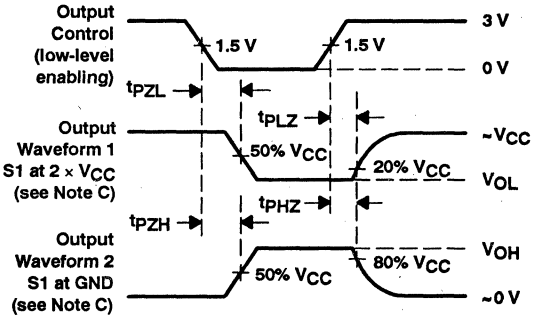


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

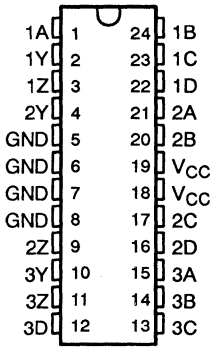
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

AUGUST 1992 – REVISED APRIL 1993

- **Suitable for Use in Applications Such as:**
  - **Differential Line Drivers**
  - **Complementary Input Circuits for Decoders and Code Converters**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

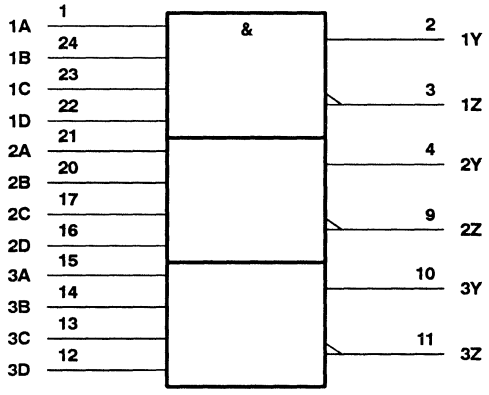
The 74AC11800 is a triple 4-input AND/NAND gate. Elimination of decode spikes in symmetrical decoder and code-converter applications makes the device useful for applications such as a decoder or differential line driver.

The 74AC11800 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
L	X	X	X	L	H
X	L	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
H	H	H	H	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each section (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			4		40	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B, C, or D	Y or Z	2.5	5.8	9.8	2.5	10.7	ns
t_{PHL}			2.7	6.2	10.9	2.7	12	

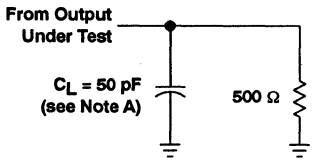
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B, C, or D	Y or Z	2.2	4.6	7.2	2.2	7.7	ns
t_{PHL}			2.3	4.8	7.7	2.3	8.4	

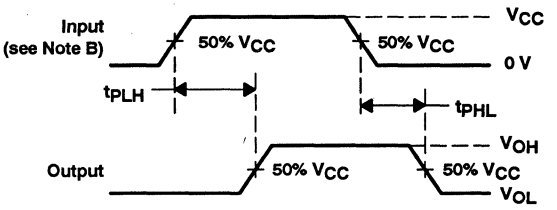
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	63	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

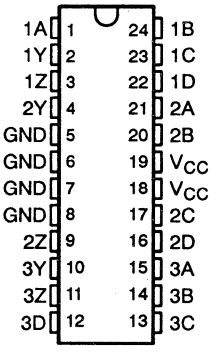
NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS153A – D3594, JULY 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

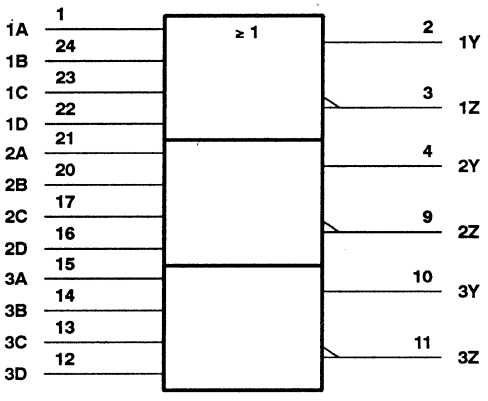
The 74ACT11802 contains three independent 4-input OR/NOR gates. They perform the Boolean functions in positive logic $Y = A + B + C + D$ and $Z = \overline{A + B + C + D}$.

The 74ACT11802 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 4-input gate)

INPUTS				OUTPUTS	
A	B	C	D	Y	Z
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each section (positive logic)

EPIC is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±150 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

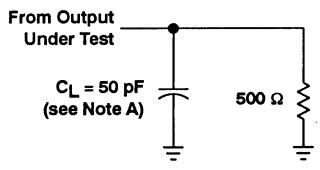
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A, B, C, or D	Y	1.3	6.1	8.4	1.3	9.5	ns
t_{PHL}			1.3	4.8	7.4	1.3	8.1	
t_{PLH}	A, B, C, or D	Z	1.3	4.6	7.5	1.3	8.3	ns
t_{PHL}			1	4.6	7.3	1	8.1	

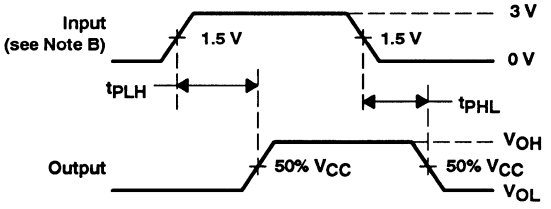
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF, f = 1 MHz	59	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



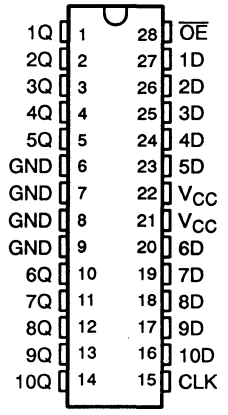
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

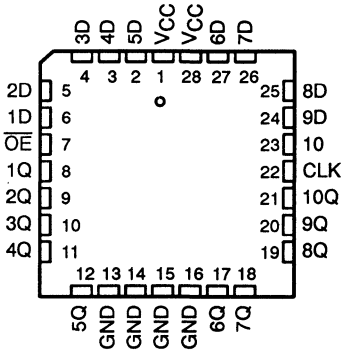
Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

54ACT11821 . . . JT PACKAGE
74ACT11821 . . . DW PACKAGE
(TOP VIEW)



54ACT11821 . . . FK PACKAGE
(TOP VIEW)



description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

On the positive transition of the clock the Q outputs will follow the D inputs.

A buffered output enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output enable ($\overline{OE}$)does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

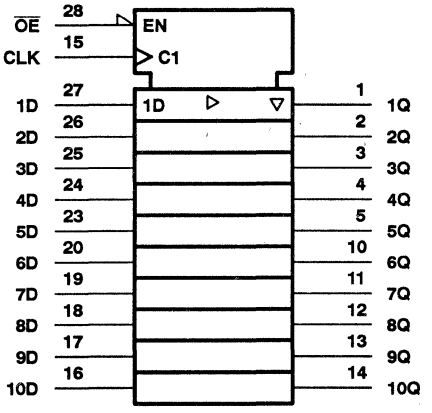
The 54ACT11821 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT11821 is characterized for operation form –40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each flip-flop)

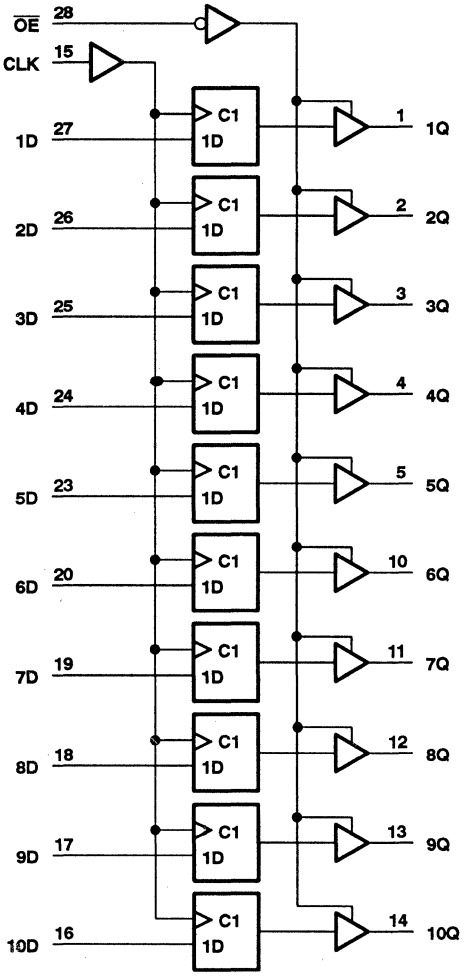
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	X_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±250 mA
Storage temperature range ..... −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT11821			74ACT11821			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10			10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11821		74ACT11821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT11821		74ACT11821		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low	4		4		4		ns
t_{su}	Setup time, data before CLK↑	2.5		2.5		2.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

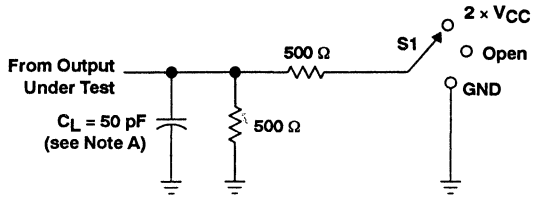
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11821		74ACT11821		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125			125		125		MHz
t_{PLH}	CLK	Any Q	4.7	7.6	10.4	4.7	12.6	4.7	11.7	ns
t_{PHL}			5	8.1	11	5	12.9	5	12.1	
t_{PZH}	$\overline{OE}$	Any Q	3.1	6.1	9.1	3.1	10.8	3.1	10	ns
t_{PZL}			4.1	7.6	11	4.1	13.2	4.1	12.3	
t_{PHZ}	$\overline{OE}$	Any Q	4.8	7.2	9.2	4.8	10.6	4.8	10.1	ns
t_{PLZ}			4.8	6.8	8.6	4.8	9.8	4.8	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

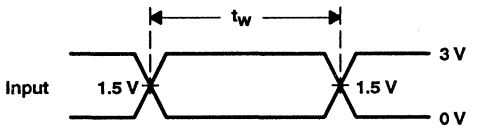
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF,	f = 1 MHz	45	pF
		Outputs disabled			31	

PARAMETER MEASUREMENT INFORMATION

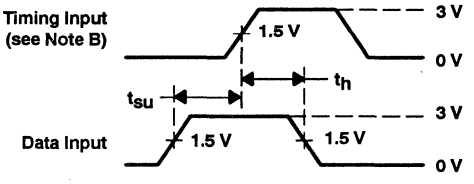


LOAD CIRCUIT

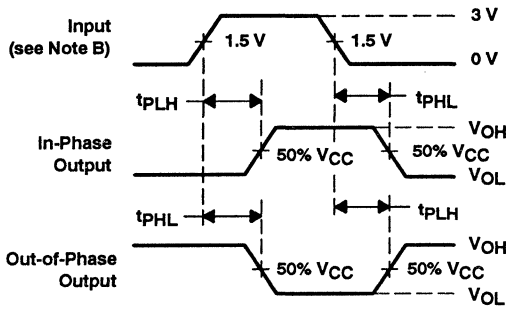
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



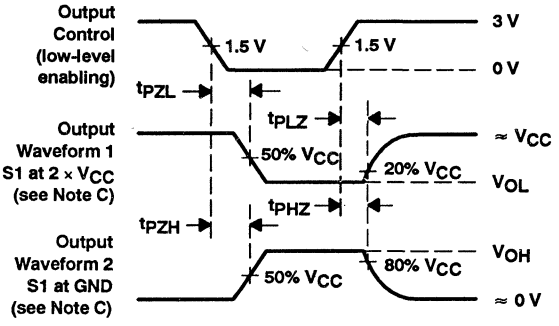
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



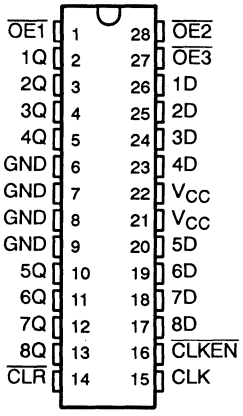
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This device contains eight flip-flops that feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. The 74ACT11825 has noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT11825 is characterized for operation from −40°C to 85°C.

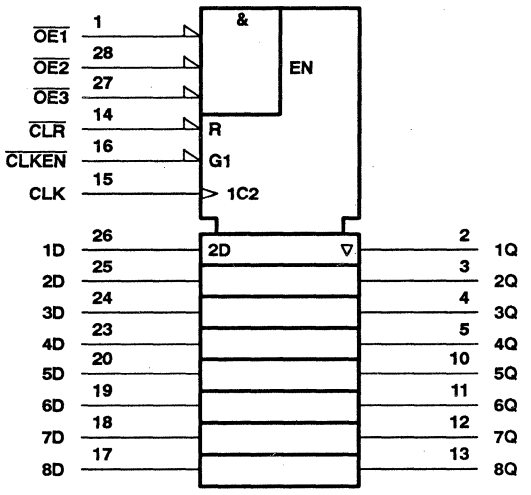
FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$†	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

† $\overline{OE}$ = H if any of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are high.
$\overline{OE}$ = L if all of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are low.

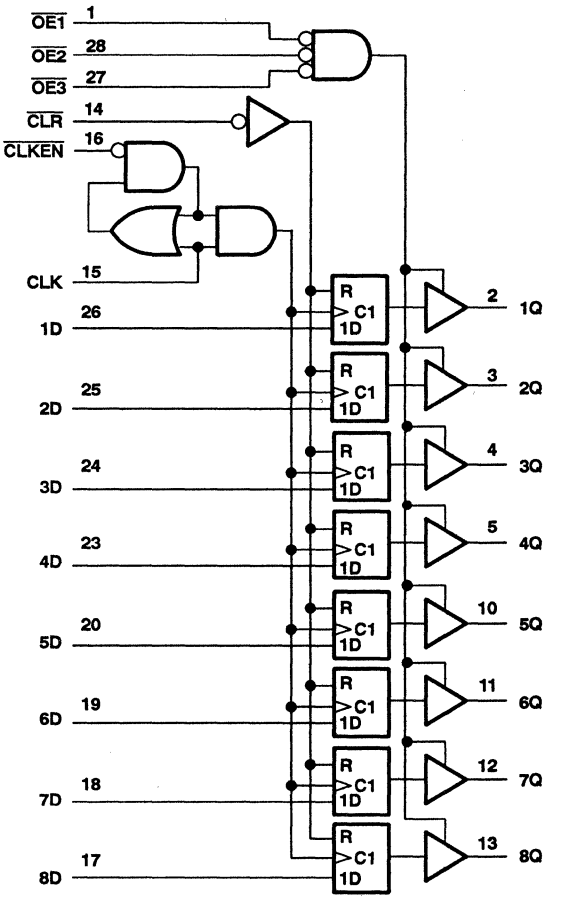
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND		5 V		4.5				pF
C_o	V_O = V_{CC} or GND		5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	122	0	122	MHz
t_w	Pulse duration	$\overline{CLR}$ low	4		4		ns
		CLK high or low	4.5		4.5		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	3		3		ns
		Data	3		3		
		$\overline{CLKEN}$ high or low	3		3		
t_h	Hold time after CLK↑	Data	1.5		1.5		ns
		$\overline{CLKEN}$ high or low	2		2		

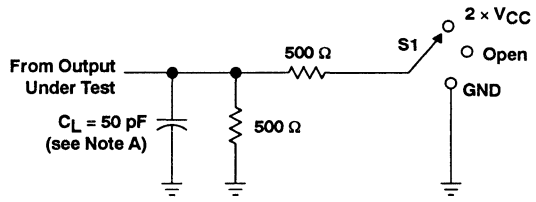
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			122			122		MHz
t_{PLH}	CLK	Q	4.6	7.7	10.2	4.6	11.6	ns
t_{PHL}			5.1	8.4	10.9	5.1	12.3	
t_{PHL}	$\overline{CLR}$	Q	4.5	8.5	11.9	4.5	13.2	ns
t_{PZH}	$\overline{OE}$	Q	3.3	6.4	9.2	3.3	10.4	ns
t_{PZL}			4.2	7.9	11.5	4.2	13	
t_{PHZ}	$\overline{OE}$	Q	6.1	8.5	10.7	6.1	12	ns
t_{PLZ}			5.5	7.9	10	5.5	11.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

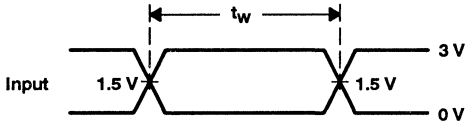
PARAMETER			TEST CONDITIONS			TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 1 MHz		47	pF
		Outputs disabled				34	

PARAMETER MEASUREMENT INFORMATION

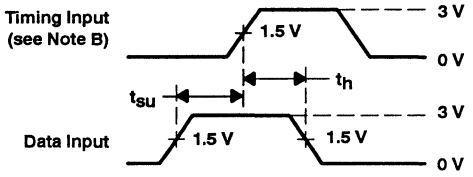


LOAD CIRCUIT

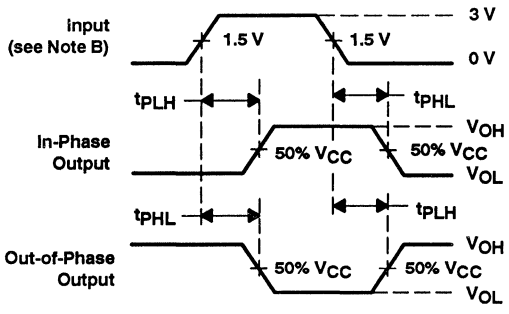
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



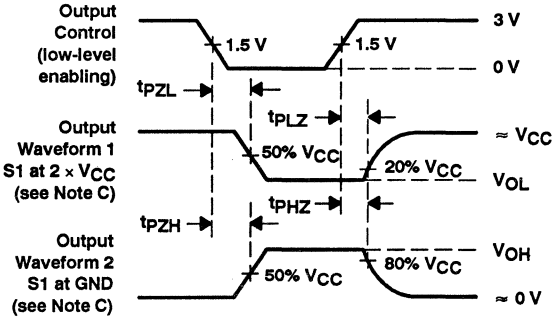
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

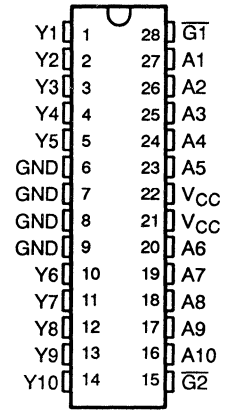
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3379, NOVEMBER 1989 – REVISED APRIL 1993

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This device contains ten buffers/bus drivers that provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ is high, all ten outputs are in the high-impedance state.

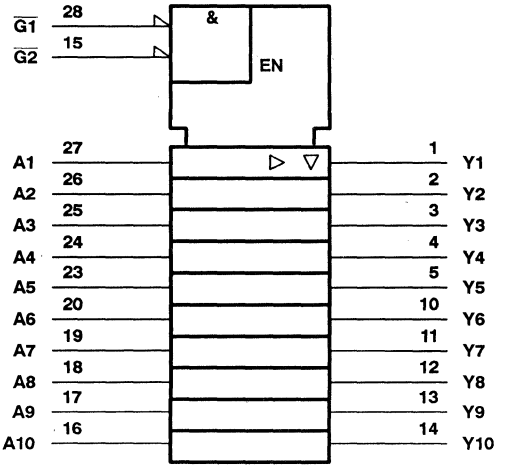
The 74AC11827 provides true data.

The 74AC11827 is characterized for operation from −40°C to 85°C.

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

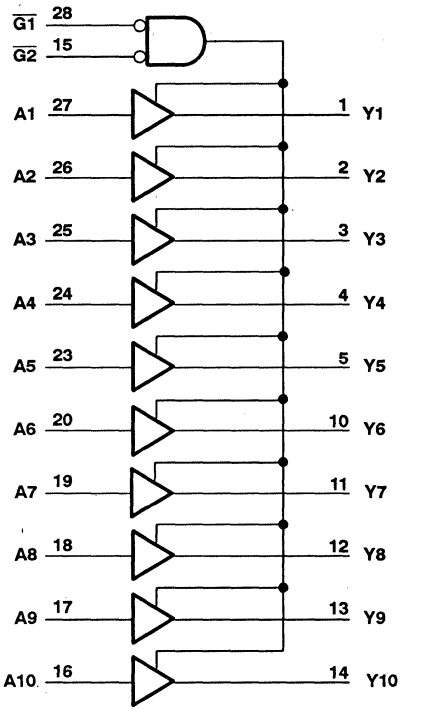
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±250 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_I = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	4.8	8.4	10.8	4.8	12.4	ns
t_{PHL}			6.8	10.4	12.6	6.8	13.4	
t_{PZH}	$\overline{G1}$ or $\overline{G2}$	Y	6.3	10.2	12.7	6.3	14.5	ns
t_{PZL}			10	16	19.2	10	21.7	
t_{PHZ}	$\overline{G1}$ or $\overline{G2}$	Y	5.9	8.5	10.4	5.9	11.1	ns
t_{PLZ}			5.4	8	10	5.4	10.5	

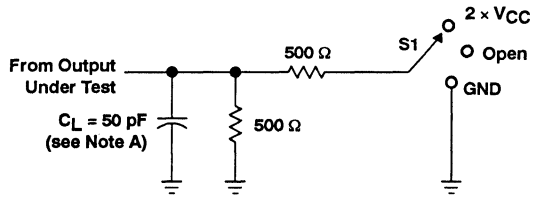
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	2.1	5.3	7.5	2.1	8.7	ns
t_{PHL}			2.9	6.2	8.4	2.9	9.7	
t_{PZH}	$\overline{G1}$ or $\overline{G2}$	Y	3.1	5.9	8.2	3.1	9.7	ns
t_{PZL}			4.1	7.7	10.6	4.1	13	
t_{PHZ}	$\overline{G1}$ or $\overline{G2}$	Y	3.9	6.6	8.4	3.9	9.1	ns
t_{PLZ}			4	6.3	7.9	4	8.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

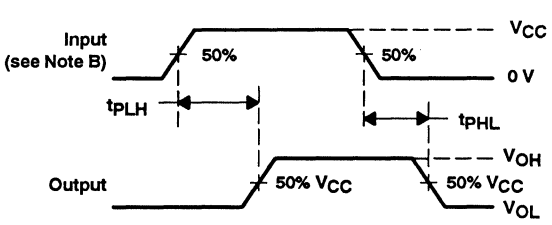
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	35	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

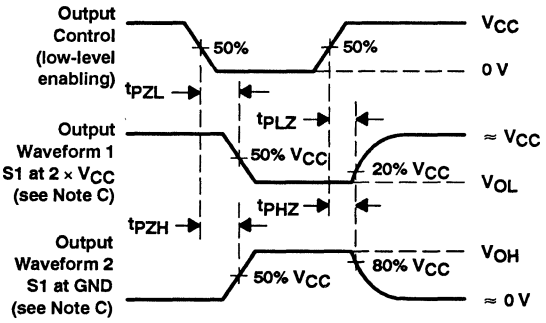


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture to Optimize PCB Layout**
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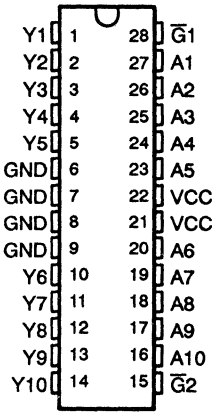
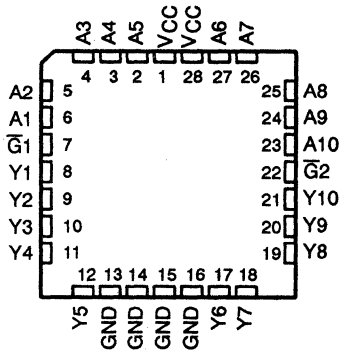
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Ceramic 300-mil DIPs**

54ACT11827 . . . JT PACKAGE
74ACT11827 . . . DW PACKAGE
(TOP VIEW)



54ACT11827 . . . FK PACKAGE
(TOP VIEW)



description

These 10-bit buffers/bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all ten outputs are in the high-impedance state.

The 'ACT11827 provides inverted data.

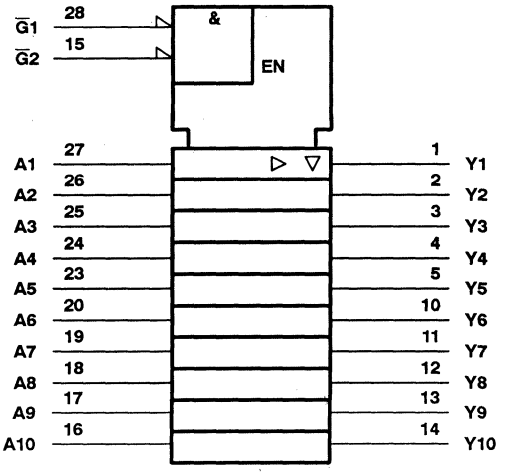
The 54ACT11827 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11827 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

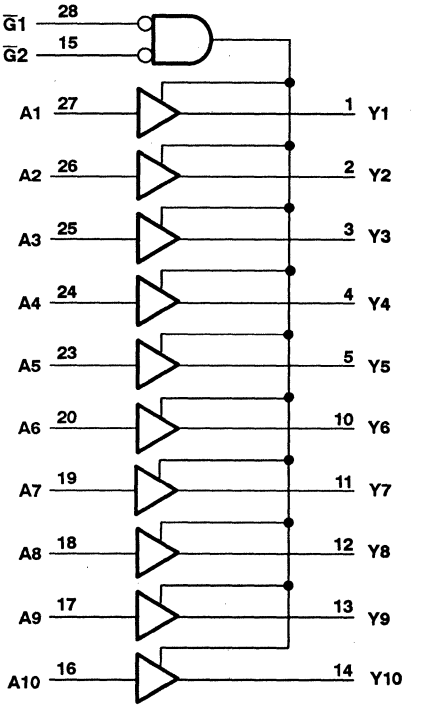
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 250 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11827		74ACT11827		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11827		74ACT11827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_O = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

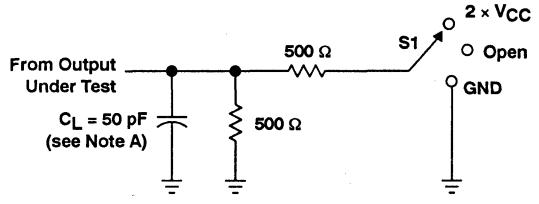
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11827		74ACT11827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.8	6.3	8	3.8	9.9	3.8	9.2	ns
t_{PHL}			2.7	6.9	9.5	2.7	11.9	2.7	11.2	
t_{PZH}	$\overline{G}$	Y	2.6	6.4	9.2	2.6	12.2	2.6	11.3	ns
t_{PZL}			3.2	8	11.2	3.2	15.1	3.2	14	
t_{PHZ}	$\overline{G}$	Y	6.1	8.8	11.1	6.1	12.9	6.1	12	ns
t_{PLZ}			5.8	8.3	10.6	5.8	12.4	5.8	11.6	

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

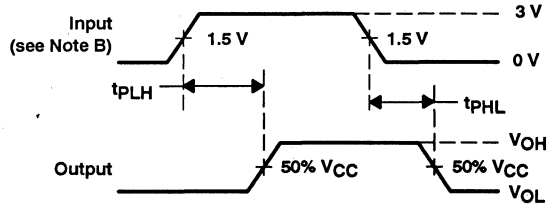
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	35	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

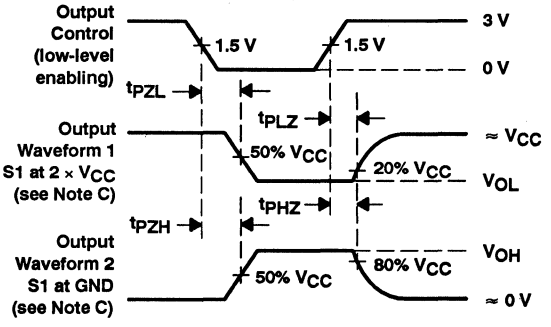


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

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description

These 10-bit buffers/bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all ten outputs are in the high-impedance state.

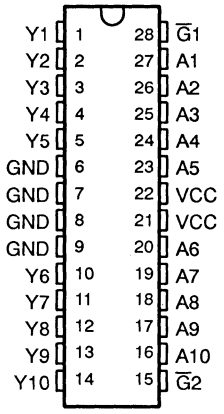
The 'ACT11828 provides inverted data.

The 54ACT11828 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT11828 is characterized for operation from – 40°C to 85°C.

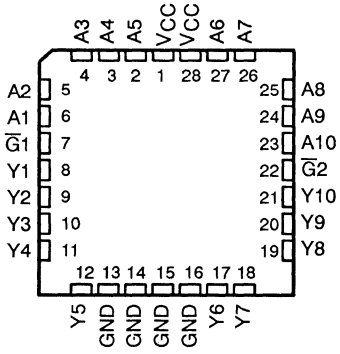
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	H	L
L	L	L	H
X	H	X	Z
H	X	X	Z

54ACT11828 . . . JT PACKAGE
74ACT11828 . . . DW PACKAGE
(TOP VIEW)

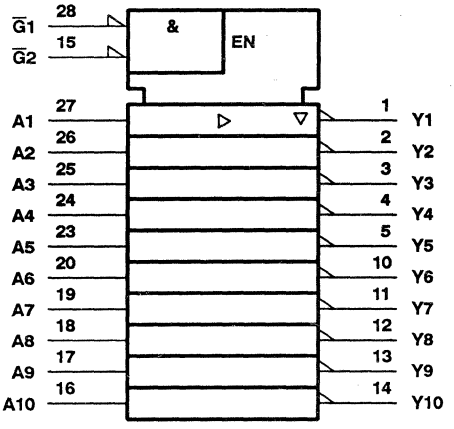


54ACT11828 . . . FK PACKAGE
(TOP VIEW)



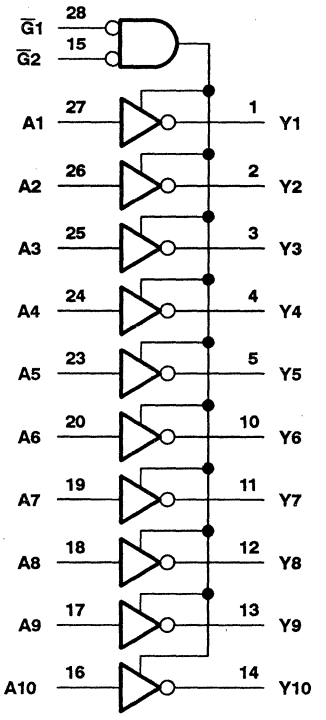
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 250 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT11828		74ACT11828		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11828		74ACT11828		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_I = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

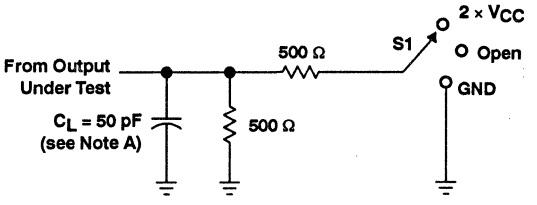
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11828		74ACT11828		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.9	5.6	8.3	1.9	10.9	1.9	10.2	ns
t_{PHL}			5.2	8	10.3	5.2	12.4	5.2	11.7	
t_{PZH}	$\overline{G}1$ or $\overline{G}2$	Y	2.9	7	9.9	2.9	13	2.9	12.1	ns
t_{PZL}			3.4	8.3	11.4	3.4	15.8	3.4	14.7	
t_{PHZ}	$\overline{G}1$ or $\overline{G}2$	Y	6	9	11.3	6	12.9	6	12.3	ns
t_{PLZ}			5.9	8.5	10.9	5.9	12.3	5.9	11.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

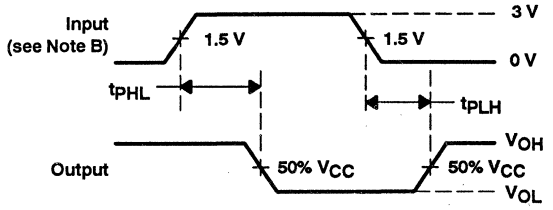
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	37	pF
		Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

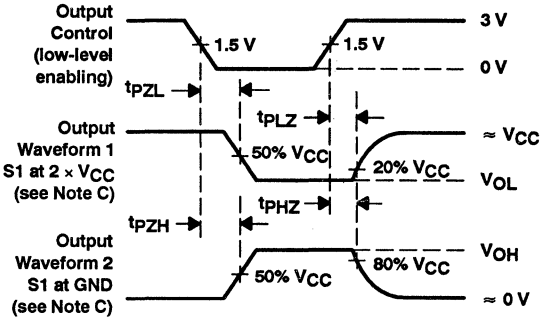


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



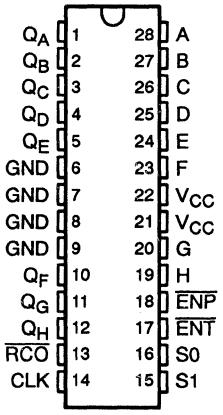
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **Asynchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11867 is a synchronous presettable binary counter featuring an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

The counters are fully programmable; that is, the outputs may each be preset to either logic level. The load-mode circuitry allows parallel loading of the cascaded counters. As loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock rising edge.

The carry look-ahead circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. This is done with two count-enable inputs and a carry output. Both count-enable ($\overline{ENP}$ and $\overline{ENT}$) inputs must be low to count. The direction of the count is determined by the levels of the select (S0 and S1) inputs (see the function table). Input $\overline{ENT}$ is fed forward to enable the ripple-carry ($\overline{RCO}$) output. $\overline{RCO}$ then produces a low-level pulse while the count is zero (all outputs low) when counting down or 255 during counting up (all outputs high). This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ and $\overline{ENT}$ are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Whenever $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ either goes high or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

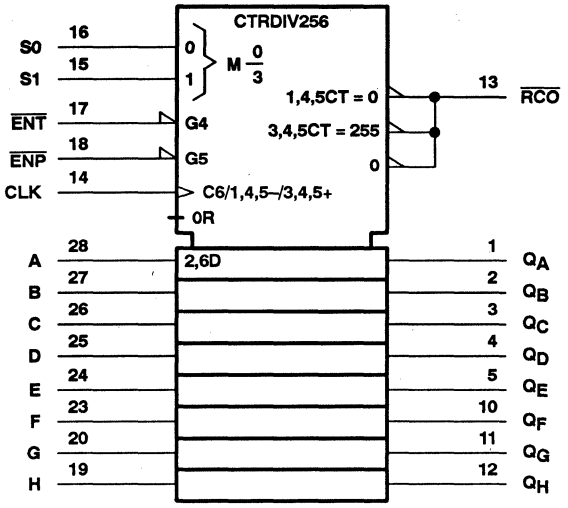
The 74ACT11867 is characterized for operation from −40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated.

MODE FUNCTION TABLE

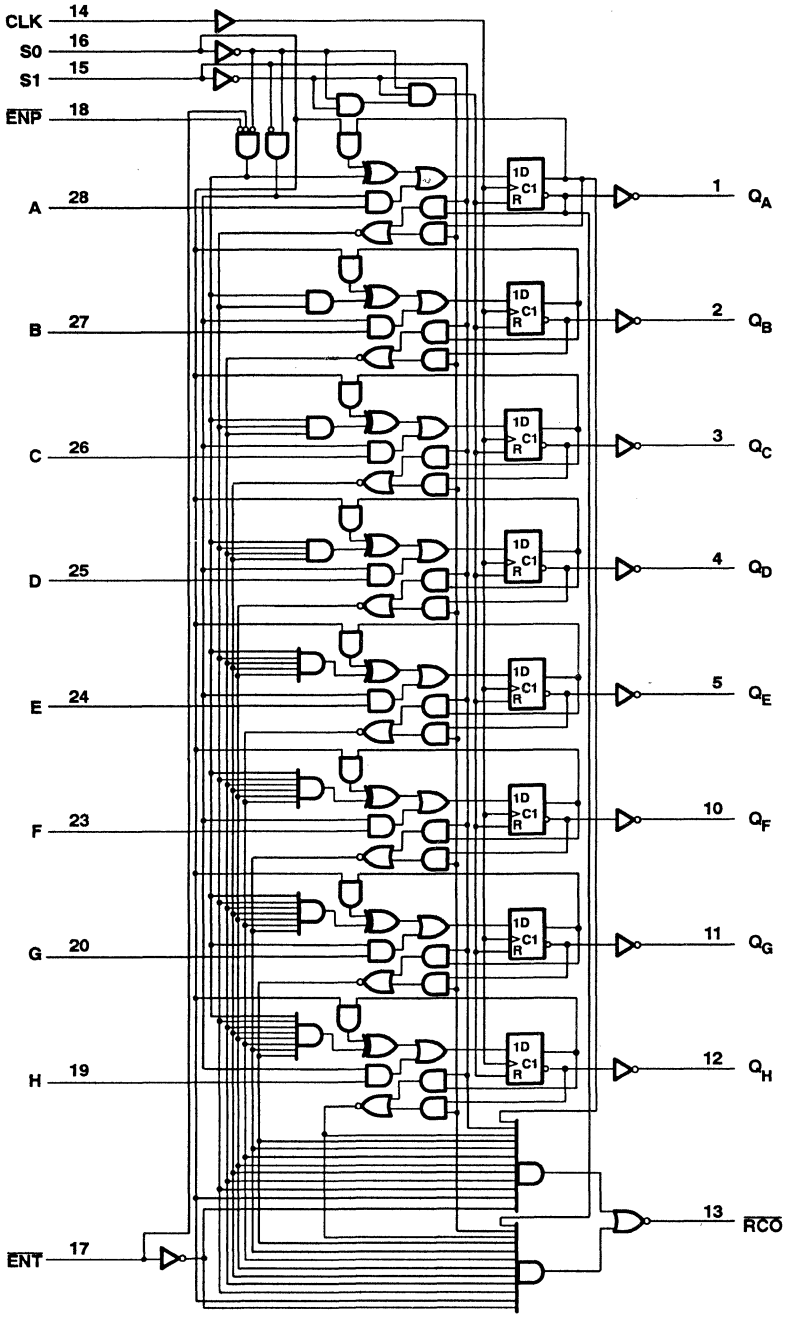
S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

logic symbol†

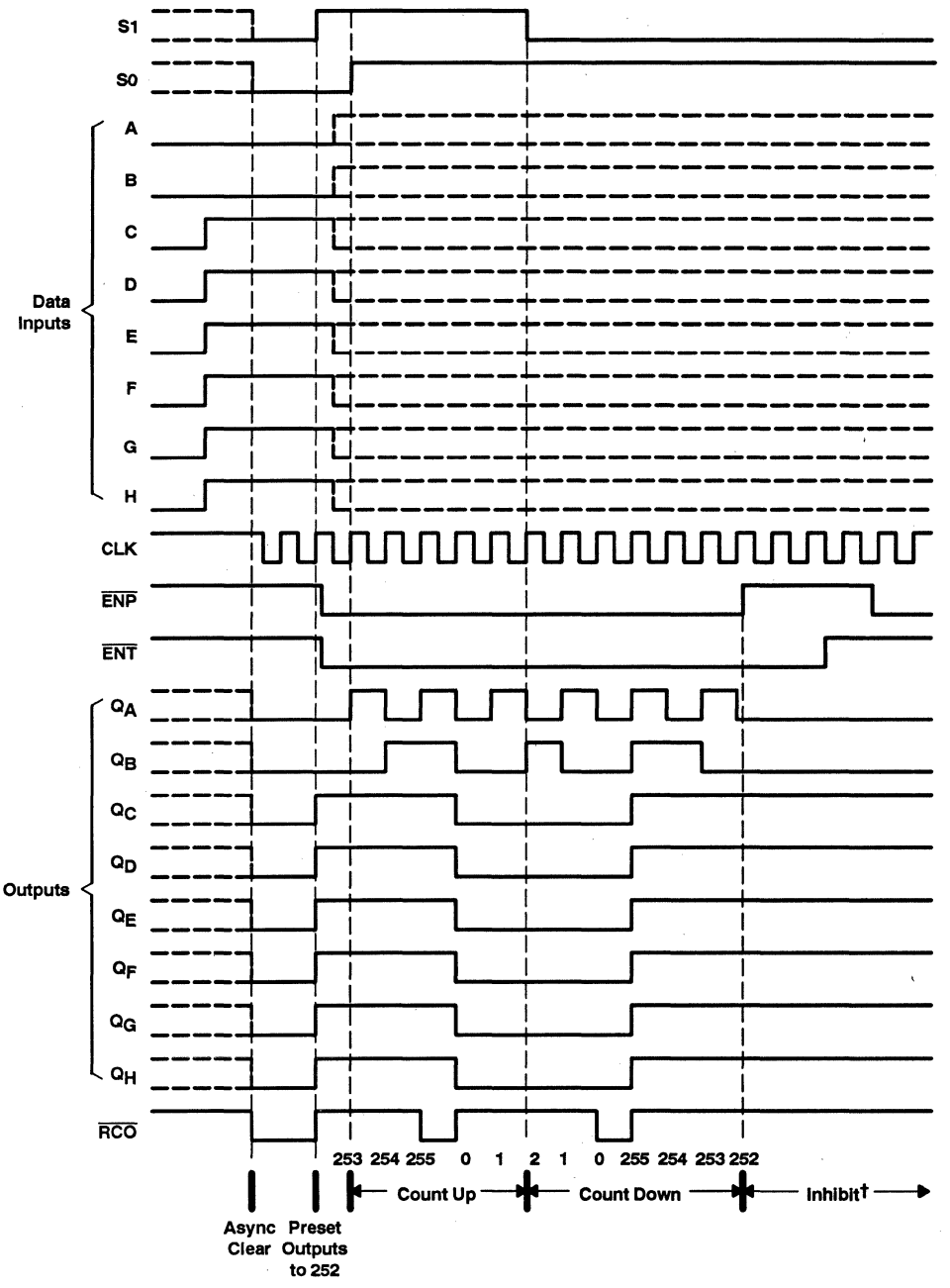


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



output sequence



† $\overline{ENT}$ and $\overline{ENP}$ must both be low for counting to occur.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	70	0	70	MHz
t_w	Pulse duration	S0 and S1 low	12		12		ns
		CLK	6.5		6.5		
t_{su}†	Setup time before CLK↑	Data	8		8		ns
		$\overline{ENP}$, $\overline{ENT}$	4		4		
		S0, S1 (load)	11		11		
		S0, S1 (count down)	11		11		
		S0, S1 (count up)	11		11		
t_h	Hold time after CLK↑	Data	1		1		ns
t_{skew}	Skew time between S0 and S1 to avoid inadvertent clear‡	S0 and S1 low		0		0	ns

† This setup time is required to ensure stable data.
‡ This is the maximum time for which S0 and S1 may be low simultaneously when the device transitions between the load (S1 = H, S0 = L) and count-down (S1 = L, S0 = H) modes.

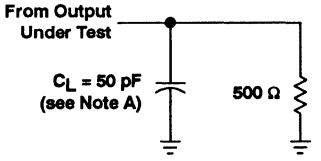
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CLK	$\overline{RCO}$	6	9.9	12.7	6	14.6	ns
t_{PHL}			6.4	10.9	14.2	6.4	16.3	
t_{PLH}	CLK	Q	5	8.9	11.9	5	13.6	ns
t_{PHL}			4.9	9	12.2	4.9	14	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	3.9	6.8	9.1	3.9	10.5	ns
t_{PHL}			3.1	7	10.2	3.1	11.5	
t_{PHL}	Clear (S0, S1 low)	Q	6.3	11.9	16.6	6.3	19.1	ns
t_{PLH}	S0, S1 (count up/down)	$\overline{RCO}$	5.5	10.4	15.6	5.5	17.8	ns
t_{PHL}	S0, S1 (count up/down)	$\overline{RCO}$	5.6	10.1	14.8	5.6	17.2	ns
t_{PHL}	Clear (S0, S1 low)	$\overline{RCO}$	6.2	11.3	15.6	6.2	17.8	ns

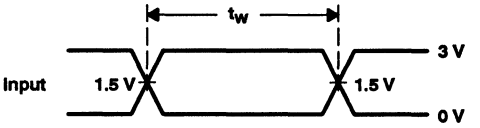
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	62	pF

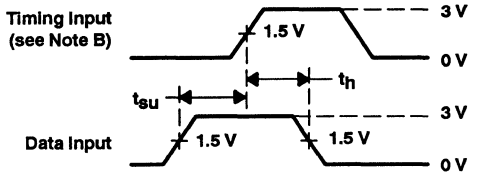
PARAMETER MEASUREMENT INFORMATION



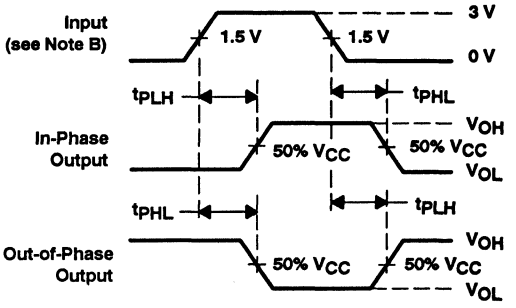
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



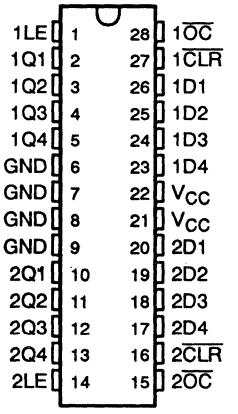
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

This dual 4-bit transparent D-type latch features 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

When the latch-enable (1LE or 2LE) input is high, the Q outputs will follow the data (D) inputs in true form, according to the function table. When LE is taken low, the outputs will be latched. When the clear ($1\overline{CLR}$ or $2\overline{CLR}$) input goes low, the Q outputs go low independently of LE. The outputs are in a high-impedance state when the output-control ($1\overline{OC}$ or $2\overline{OC}$) input is at a high logic level.

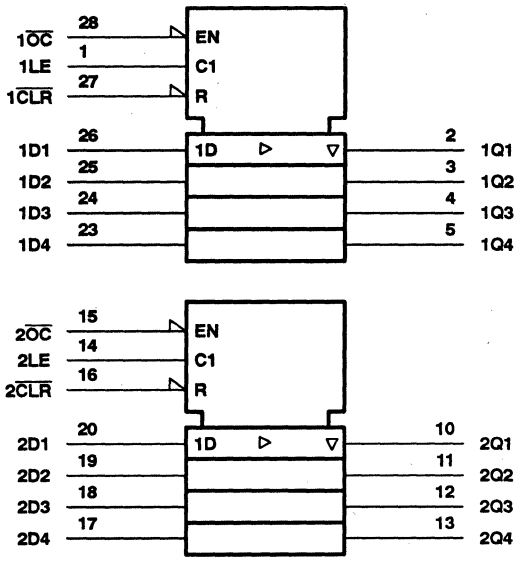
The 74AC11873 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 4-bit latch)

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	LE	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

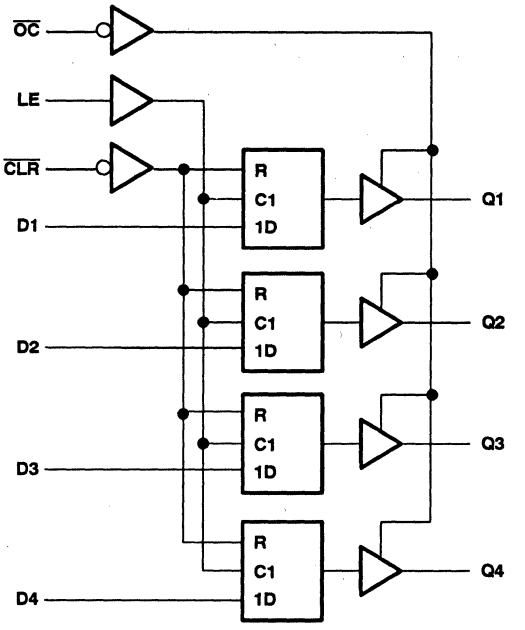
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each quad latch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_O = V_{CC} or GND	5 V		13.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		LE high	5		5		
t_{su}	Setup time, data before LE↓	High	3		3		ns
		Low	4		4		
t_h	Hold time, data after LE↓	High	1		1		ns
		Low	1		1		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		LE high	5		5		
t_{su}	Setup time, data before LE↓	High	2		2		ns
		Low	3		3		
t_h	Hold time, data after LE↓	High	1		1		ns
		Low	1		1		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	2.8	8.8	11.2	2.8	13	ns
t_{PHL}			2.8	9	11.2	2.8	12.7	
t_{PLH}	LE	Q	3	9.4	11.8	3	13.6	ns
t_{PHL}			2.9	9.4	11.7	2.9	13.2	
t_{PHL}	$\overline{CLR}$	Q	2.3	8.2	10.3	2.3	11.5	ns
t_{PZH}	$\overline{OC}$	Q	1.8	6.4	8.4	1.8	9.7	ns
t_{PZL}			2.7	9.9	12.5	2.7	14.4	
t_{PHZ}	$\overline{OC}$	Q	3.8	6.8	8.4	3.8	9	ns
t_{PLZ}			3.5	6.8	8.5	3.5	9.1	

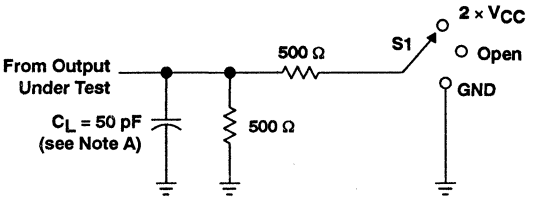
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	2.2	5.5	7.3	2.2	8.4	ns
t_{PHL}			2.1	5.5	7.2	2.1	8.2	
t_{PLH}	LE	Q	2.4	5.9	7.8	2.4	8.9	ns
t_{PHL}			2.2	5.8	7.6	2.2	8.7	
t_{PHL}	$\overline{CLR}$	Q	1.7	5.1	6.8	1.7	7.6	ns
t_{PZH}	$\overline{OC}$	Q	1.2	4.1	5.6	1.2	6.4	ns
t_{PZL}			1.9	5.5	7.3	1.9	8.5	
t_{PHZ}	$\overline{OC}$	Q	3.5	5.9	7.4	3.5	7.9	ns
t_{PLZ}			3.3	5.5	7	3.3	7.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

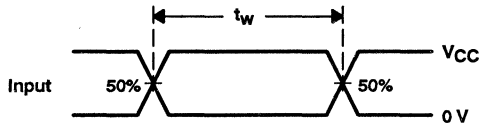
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

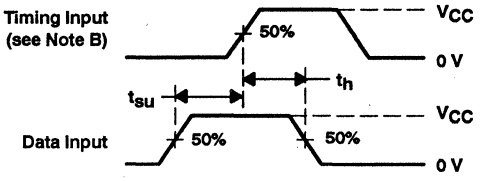


LOAD CIRCUIT

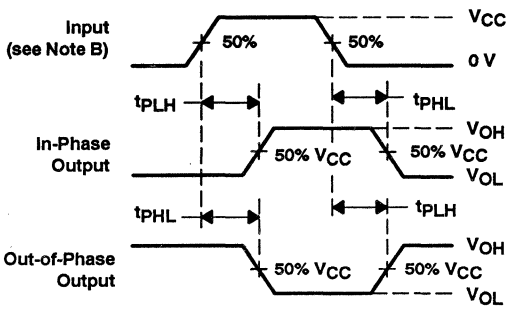
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



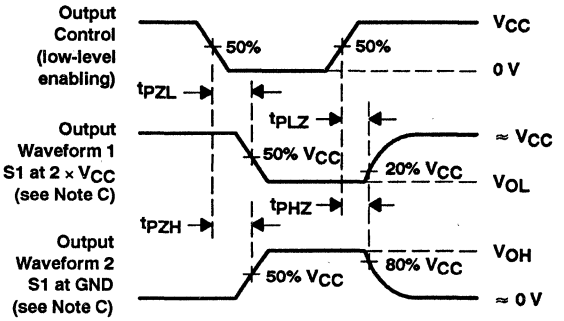
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



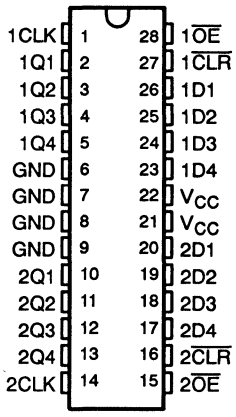
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Inputs Are TTL-Voltage Compatible**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Asynchronous Clear**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DW PACKAGE
(TOP VIEW)



description

The 74ACT11874 contains dual 4-bit registers featuring 3-state outputs designed specifically for bus driving. This makes this device particularly suitable for implementing buffer registers, I/O ports, and working registers.

The D-type edge-triggered flip-flops enter data on the low-to-high transition of the clock. The 74ACT11874 has $\overline{CLR}$ inputs and noninverting outputs. Taking $\overline{CLR}$ low causes the four Q outputs to go low independently of the clock.

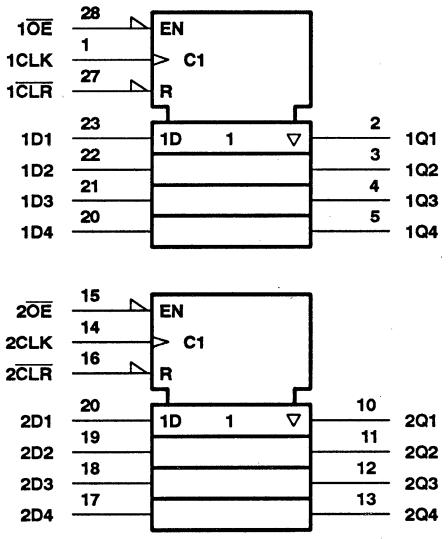
The 74ACT11874 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

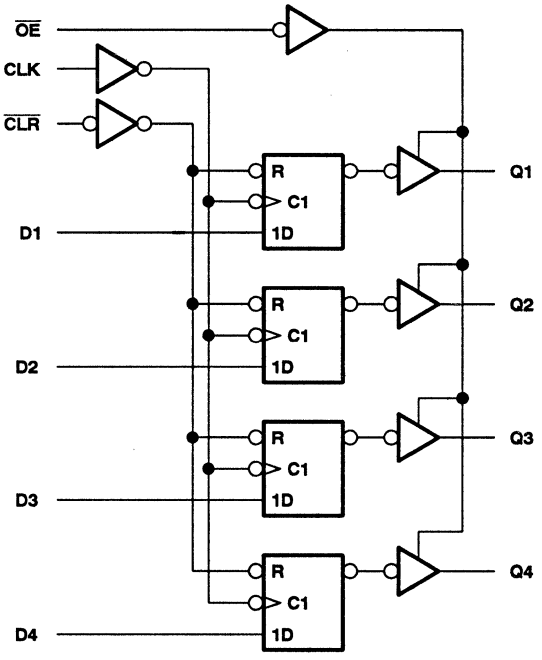
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each 4-bits) (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±200 mA
Storage temperature range ..... −55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{clock}	Clock frequency		0		125	0	125	MHz
t_w	Pulse duration	$\overline{CLR}$ low		2		4		ns
		CLK high or low		2		4		
t_{su}	Setup time before CLK↑	Data		1		5		ns
		$\overline{CLR}$ low		2		2		
t_h	Hold time after CLK↑	Data		2		1		ns

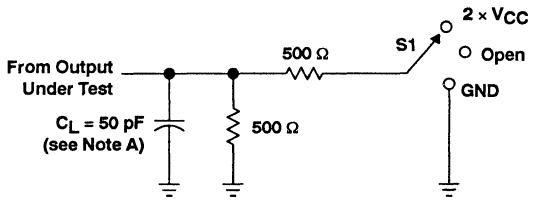
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			125			125		MHz
t_{PLH}	CLK	Any Q		7.5		3.7	9.4	ns
t_{PHL}				8.1		4.1	10.6	
t_{PHL}	$\overline{CLR}$	Any Q		8.8		3.5	11.8	ns
t_{PZH}	$\overline{OE}$	Any Q		6.4		1.6	7.4	ns
t_{PZL}				8.6		2.4	9.5	
t_{PHZ}	$\overline{OE}$	Any Q		6.9		5.4	9.4	ns
t_{PLZ}				6.8		4.9	9.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

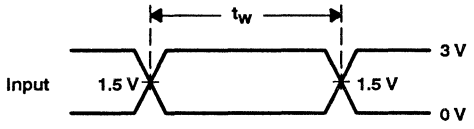
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	76	pF
		Outputs disabled		64	

PARAMETER MEASUREMENT INFORMATION

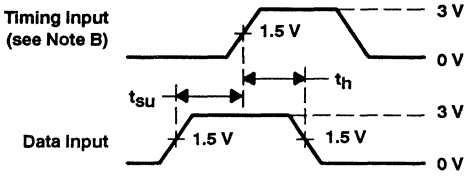


LOAD CIRCUIT

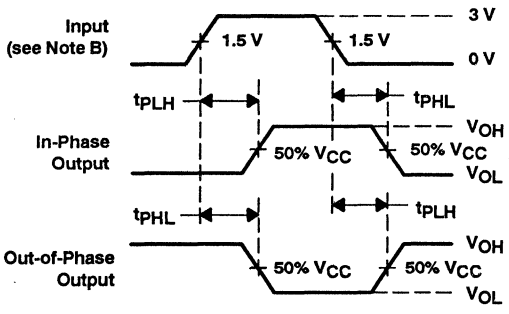
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



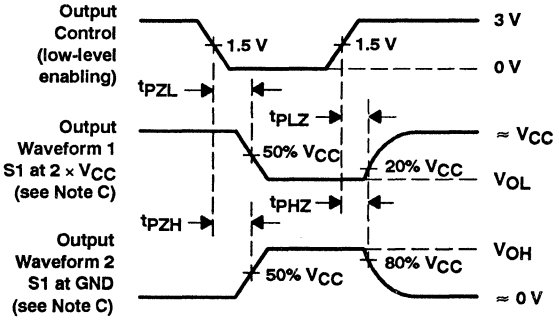
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

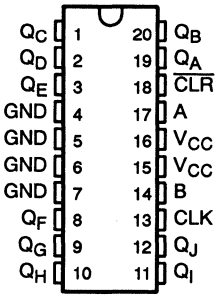
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3644, OCTOBER 1990 – REVISED APRIL 1993

- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Fully Synchronous Data Transfers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74AC11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74AC11898 is characterized for operation from −40°C to 85°C.

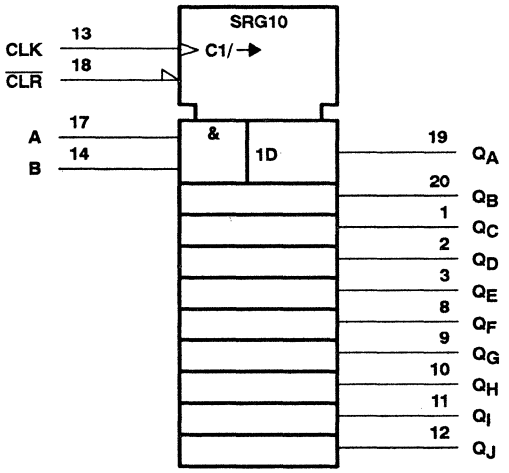
FUNCTION TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	...	Q_J
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{J0}
H	↑	H	H	H	Q_{An}		Q_{In}
H	↑	L	X	L	Q_{An}		Q_{In}
H	↑	X	L	L	Q_{An}		Q_{In}

H = high level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{J0} = the level of Q_A, Q_B, Q_J respectively, before the indicated steady-state input conditions were established.
Q_n, Q_{in} = the level or Q_A or Q_J before the most recent ↑ transition of the clock; indicates a one-bit shift.

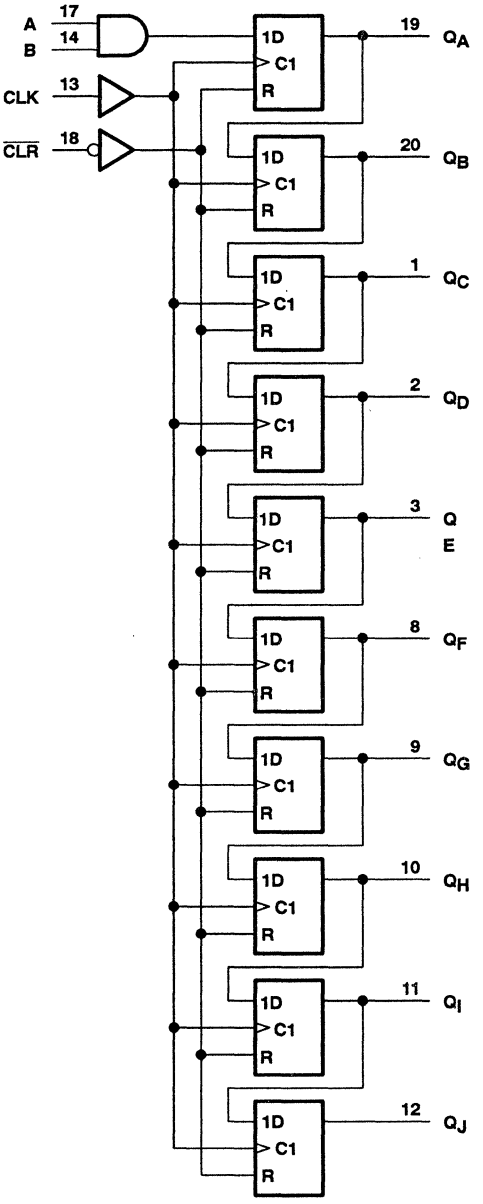
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±250 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	40	0	40	ns
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		CLK high or low	12.5		12.5		
t_{su}	Setup time before CLK↑	Data	14		14		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time, data after CLK↑		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	60	0	60	ns
t_w	Pulse duration	$\overline{CLR}$ low	4.5		4.5		ns
		CLK high or low	8.3		8.3		
t_{su}	Setup time before CLK↑	Data	8.5		8.5		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time, data after CLK↑		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			40	60		40		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4.1	9.4	11.7	4.1	13	ns
t_{PLH}	CLK	Any Q	3.3	8.2	10.7	3.3	11.9	ns
t_{PHL}			3.9	8.9	10.8	3.9	12.2	

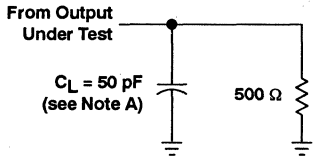
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			60	90		60		MHz
t_{PHL}	$\overline{CLR}$	Any Q	3.8	6.7	9.1	3.8	10.3	ns
t_{PLH}	CLK	Any Q	2.7	5.5	7.9	2.7	8.1	ns
t_{PHL}			3.1	6.3	8.6	3.1	10	

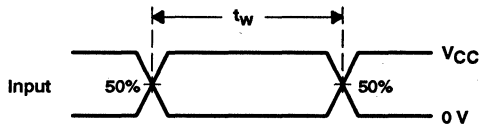
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	122	pF

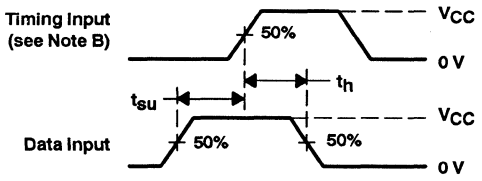
PARAMETER MEASUREMENT INFORMATION



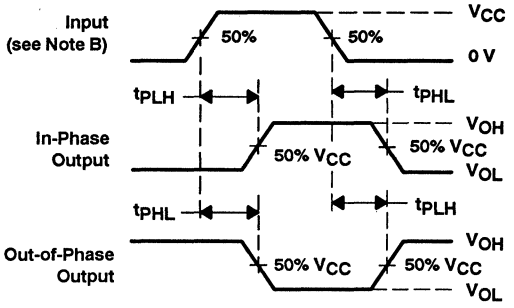
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

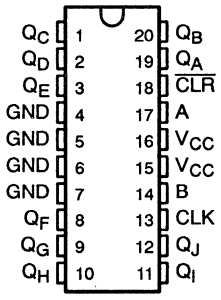
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

D3644, OCTOBER 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **AND-Gated (Enable/Disable) Serial Inputs**
- **Fully Buffered Clock and Serial Inputs**
- **Direct Clear**
- **Fully Synchronous Data Transfers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

The 74ACT11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74ACT11898 is characterized for operation from −40°C to 85°C.

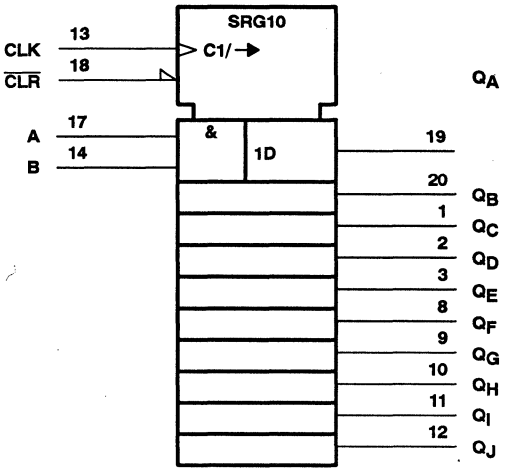
FUNCTION TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	...	Q_J
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{J0}
H	↑	H	H	H	Q_{AN}		Q_{IN}
H	↑	L	X	L	Q_{AN}		Q_{IN}
H	↑	X	L	L	Q_{AN}		Q_{IN}

H = high level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{J0} = the level of Q_A, Q_B, Q_J respectively, before the indicated steady-state inputconditions were established.
Q_n, Q_{in} = the level or Q_A or Q_J before the most recent ↑ transition of the clock; indicates aone-bit shift.t

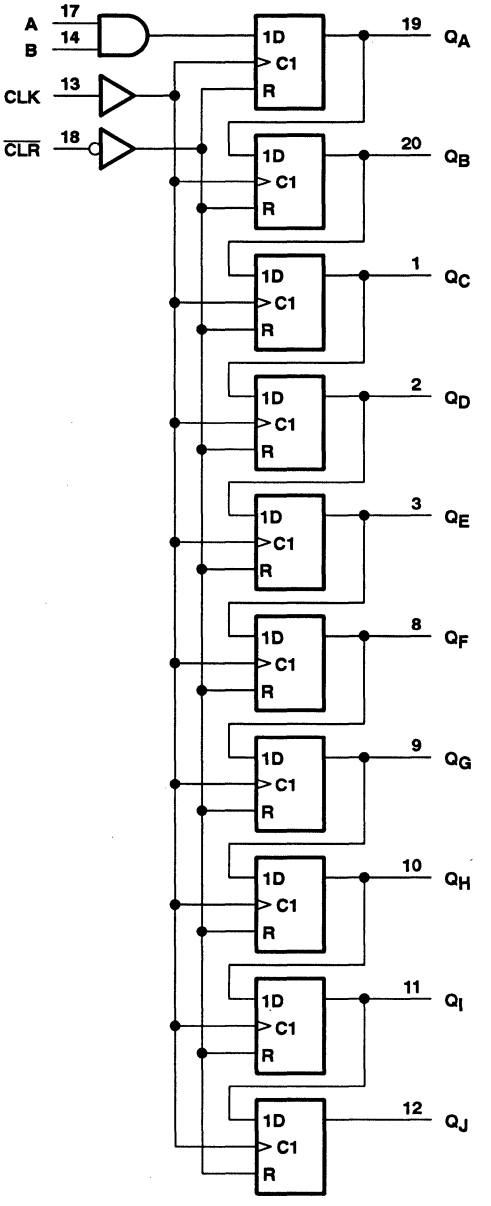
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±250 mA
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	−40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA‡	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA‡	5.5 V					1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	40	0	40	ns
t_w	Pulse duration	$\overline{CLR}$ low	4.5		4.5		ns
		CLK high or low	12.5		12.5		
t_{su}	Setup time before CLK↑	Data	10		10		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time, data after CLK↑		0		0		ns

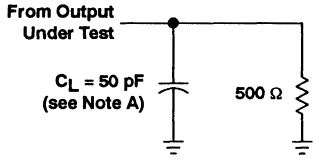
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			20	65		40		MHz
t_{PHL}	$\overline{CLR}$	Any Q	4.6	6.7	11.1	3.8	12.1	ns
t_{PLH}	CLK	Any Q	4.1	5.5	8.8	2.7	9.7	ns
t_{PHL}			4.4	6.3	9.4	3.1	10.6	

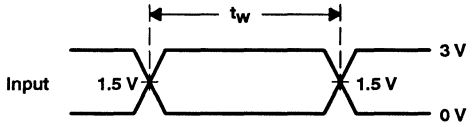
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	117	pF

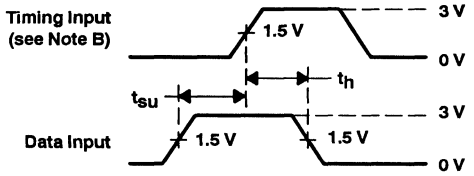
PARAMETER MEASUREMENT INFORMATION



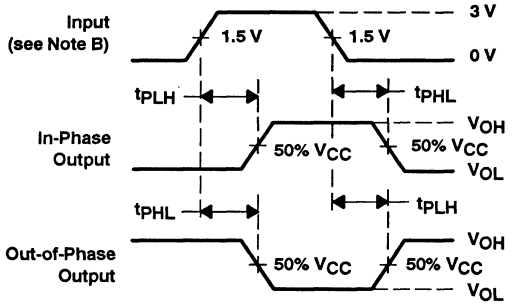
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

ACL Widebus™

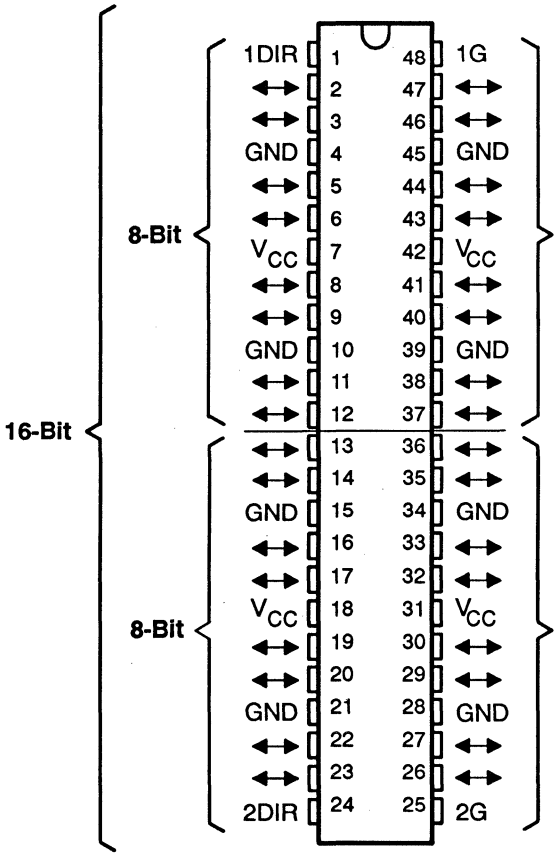
Features

- Low CMOS Power (ACL)
- 24-mA Output Drive Capability (ACL)
- OEC™ Outputs (ACL)
- Distributed V_{CC}/GND (ACL/ABT)

Features

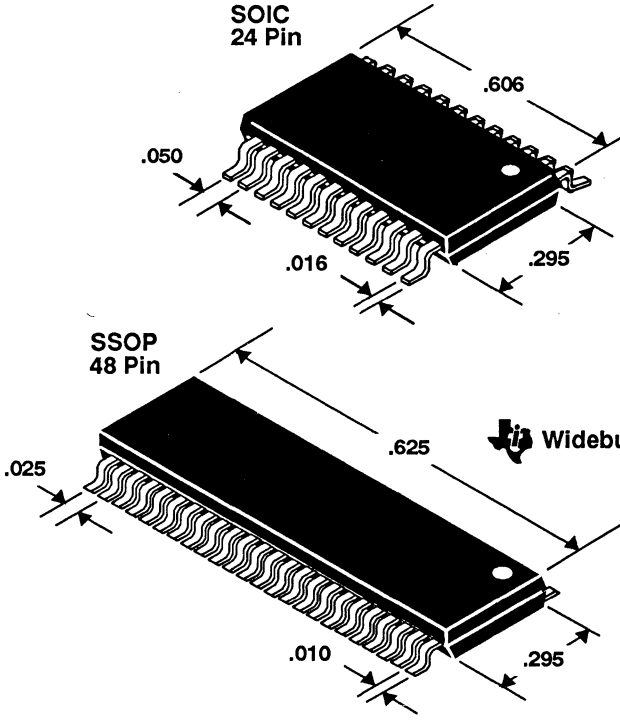
- Saves Board Space
- Advanced Performance
- Minimizes System Power
- 50-Ω Transmission Line Drive Capacity
- Reduced Simultaneous Switching Noise

Distributed Pinout of 'ACT16245



- Flow-Through Architecture
- Word Width Control Capability
- Distributed V_{CC} and GND
- 1 GND per 2 Outputs
- Minimal Mutual Coupling

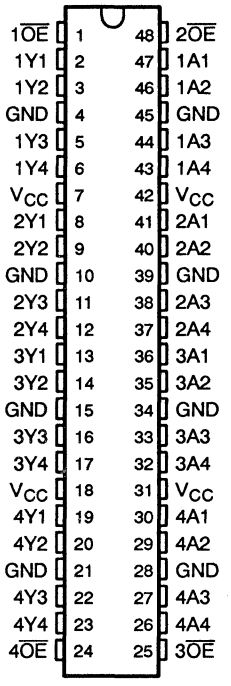
Package Size Comparison



Widebus is a trademark of Texas Instruments Incorporated.

- **Member of the Texas Instruments *Widebus*™ Family**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**

DL PACKAGE
(TOP VIEW)



description

The 74AC16240 is a 16-bit buffer and line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

The 74AC16240 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

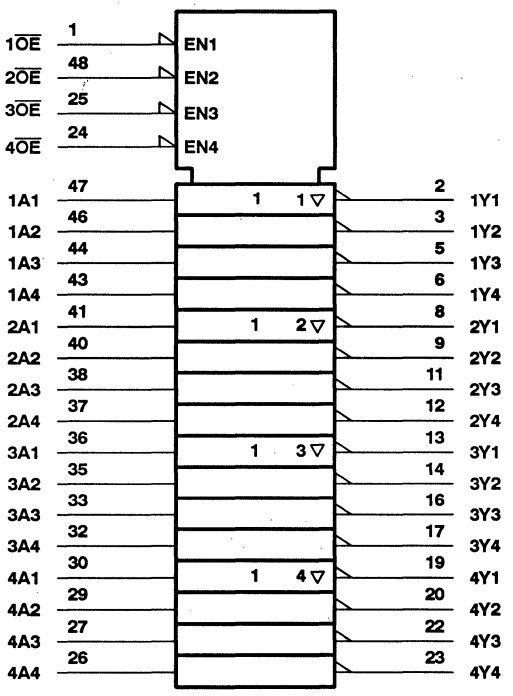
The 74AC16240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

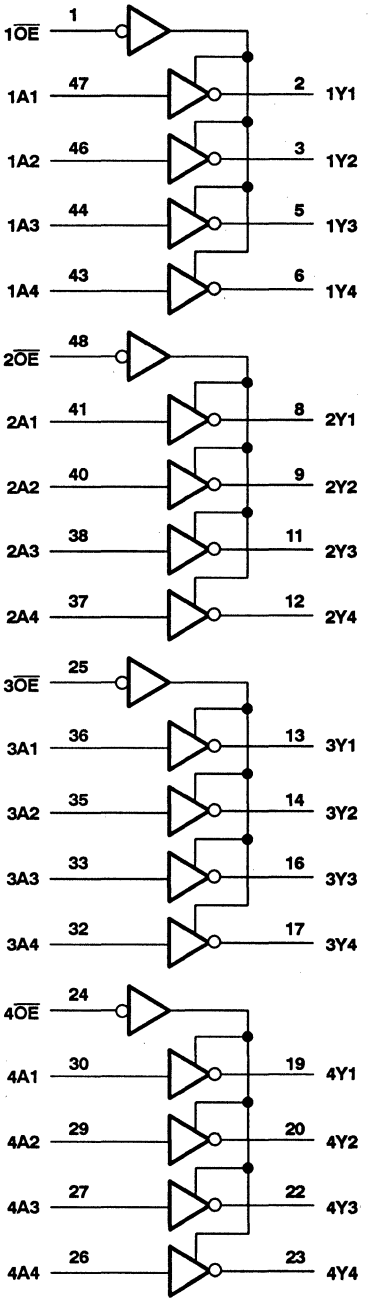
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.8	5.4	7.5	1.8	8.3	ns
t_{PHL}			2.5	7	9.3	2.5	10.2	
t_{PZH}	$\overline{OE}$	Y	2.1	6.1	8.5	2.1	9.5	ns
t_{PZL}			2.9	8.4	11.3	2.9	12.6	
t_{PHZ}	$\overline{OE}$	Y	4.3	6.2	8.3	4.3	8.7	ns
t_{PLZ}			3.6	6	7.8	3.6	8.4	

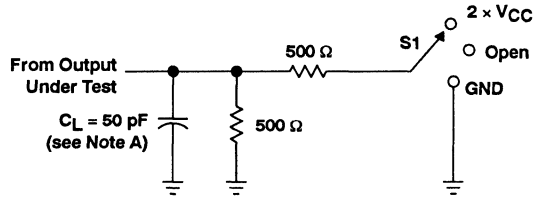
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.3	3.3	5.3	1.3	5.8	ns
t_{PHL}			1.9	4.3	6.5	1.9	7.1	
t_{PZH}	$\overline{OE}$	Y	1.6	3.8	5.9	1.6	6.6	ns
t_{PZL}			3.2	4.7	7.2	3.2	8.1	
t_{PHZ}	$\overline{OE}$	Y	4.2	6	7.7	4.2	8.1	ns
t_{PLZ}			3.4	5.1	6.9	3.4	7.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

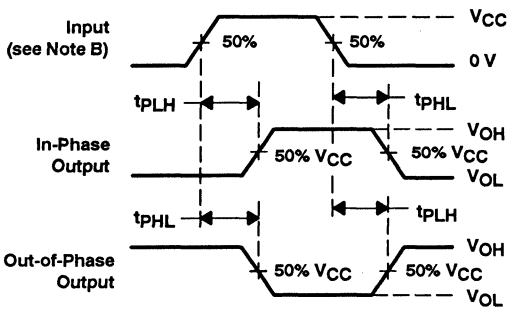
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		6	

PARAMETER MEASUREMENT INFORMATION

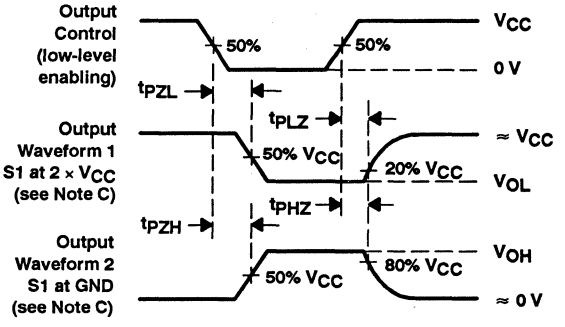


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



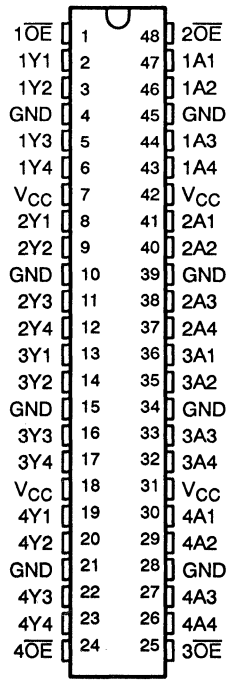
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16240 . . . WD PACKAGE
74ACT16240 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16240 is a 16-bit buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The 74ACT16240 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

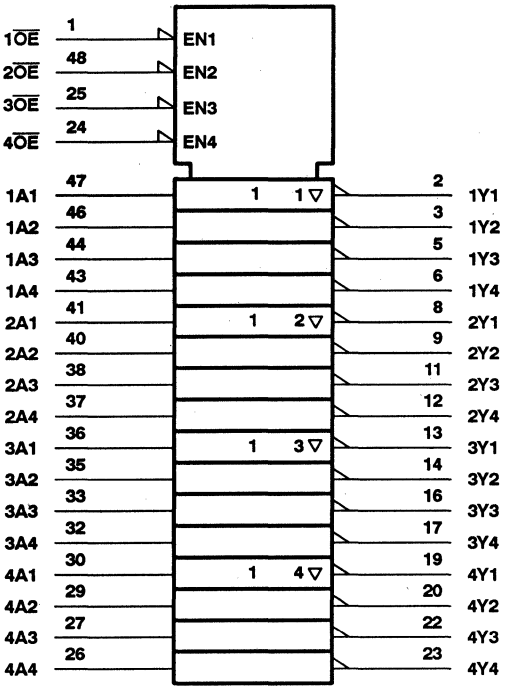
The 54ACT16240 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each section)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

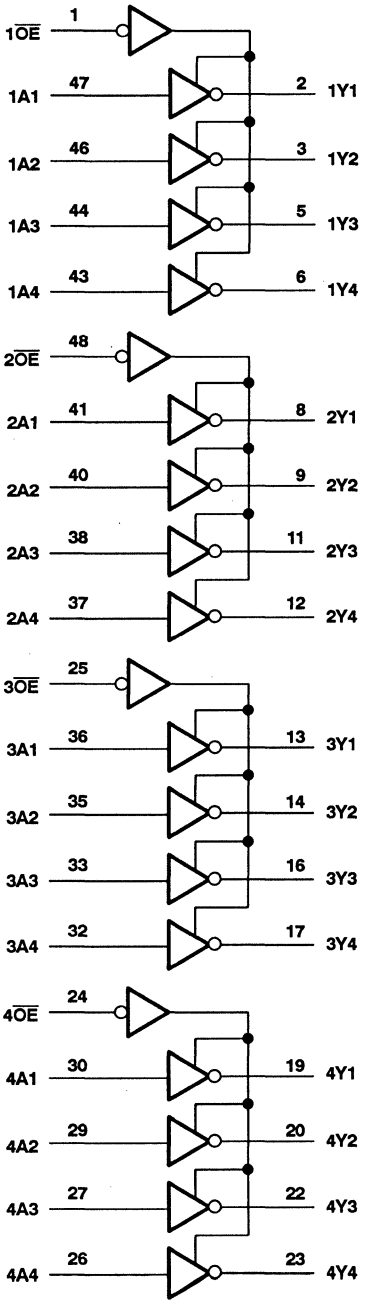
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16240			74ACT16240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16240		74ACT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at VCC or GND	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5.5 V		4.5						pF
C_o	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

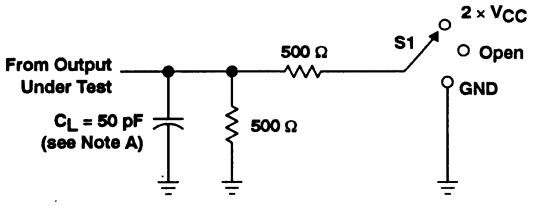
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16240		74ACT16240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.3	5	7.7	2	9.5	2.3	8.5	ns
t_{PHL}			4.1	6.7	9.2	3	11.5	4.1	10.2	
t_{PZH}	$\overline{OE}$	Y	2.6	5.6	8.5	2	10.1	2.6	9.4	ns
t_{PZL}			3.3	6.7	10.2	2.5	12.2	3.3	11.4	
t_{PHZ}	$\overline{OE}$	Y	5.9	8.3	11	4.5	12.7	5.9	12	ns
t_{PLZ}			5.1	7.4	9.9	4	12	5.1	10.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

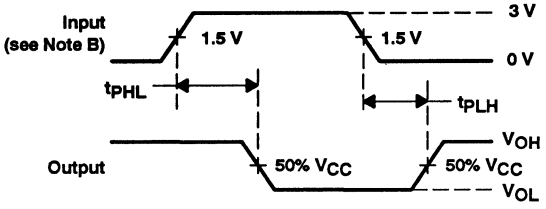
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per driver	Outputs enabled	C_L = 50 pF, f = 1 MHz	38	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

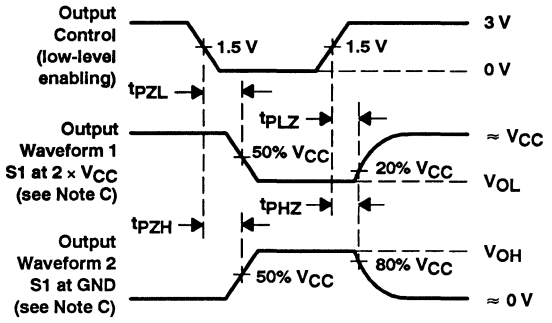


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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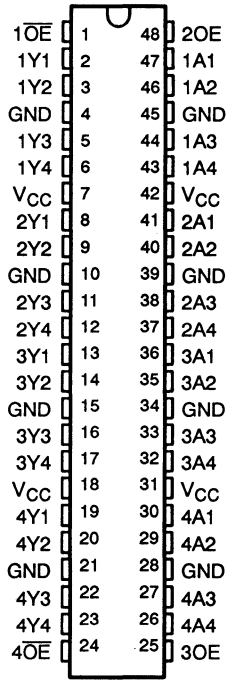
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16241 is a 16-bit buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-enable (OE and $\overline{OE}$) inputs.

The 74ACT16241 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16241 is characterized for operation from −40°C to 85°C.

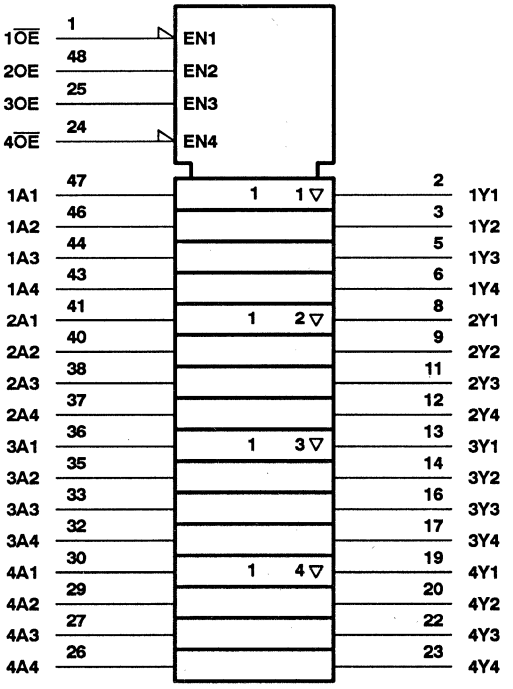
FUNCTION TABLES

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

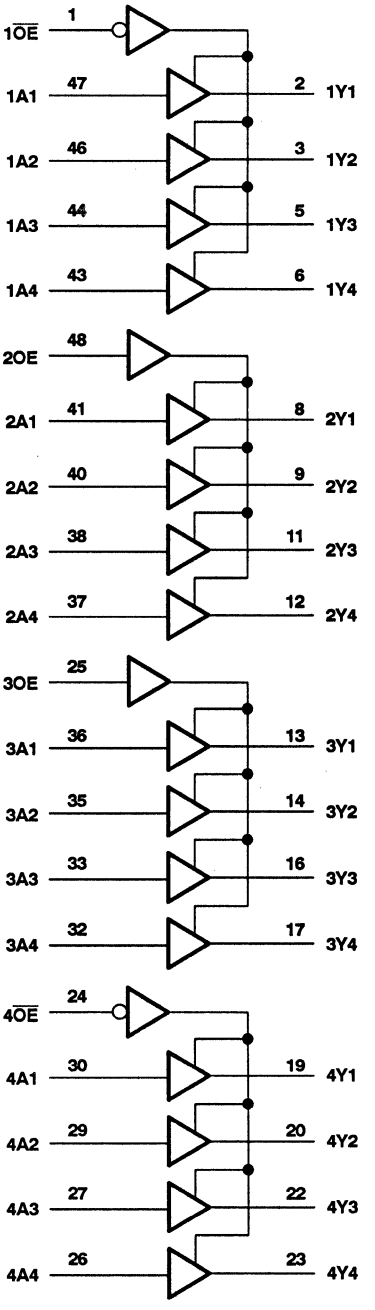
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_O = V_{CC} or GND	5 V		13				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

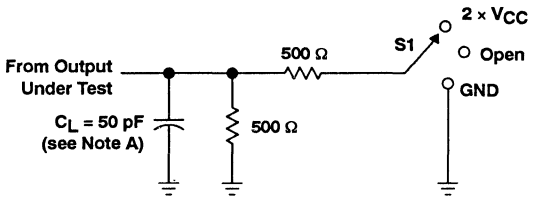
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	3.3	6.5	8.4	3.3	9.5	ns
t_{PHL}			2.3	6.3	8.2	2.3	9.1	
t_{PZH}	$\overline{OE}$ or OE	Y	2.3	6.5	8.3	2.3	9.4	ns
t_{PZL}			2.9	7.3	9.3	2.9	10.5	
t_{PHZ}	$\overline{OE}$ or OE	Y	4.3	8.9	10.6	4.3	11.6	ns
t_{PLZ}			4	8.1	9.8	4	10.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

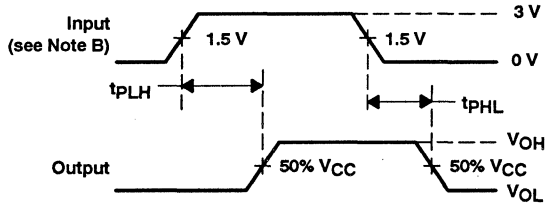
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

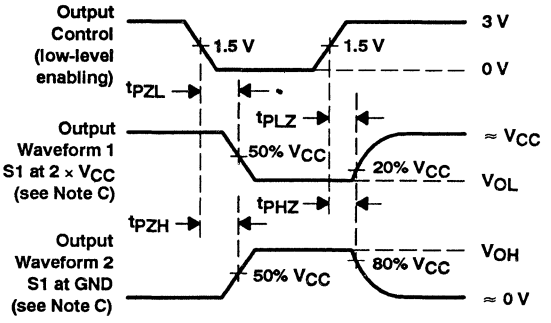


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



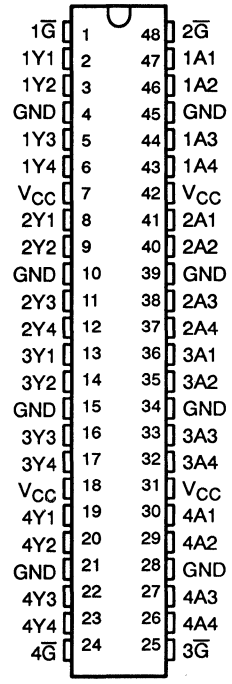
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Shrink and Plastic Thin Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**

DGG OR DL PACKAGE
(TOP VIEW)



description

The 74AC16244 is a 16-bit buffer/line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{G}$ (active-low) output-enable inputs.

The 74AC16244 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

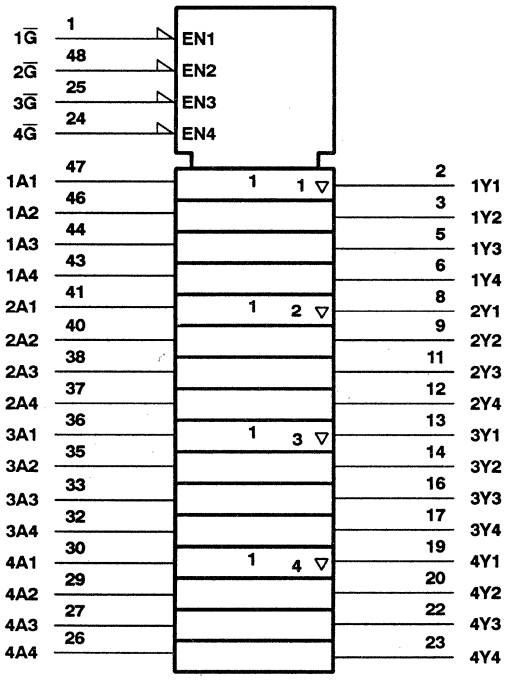
The 74AC16244 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

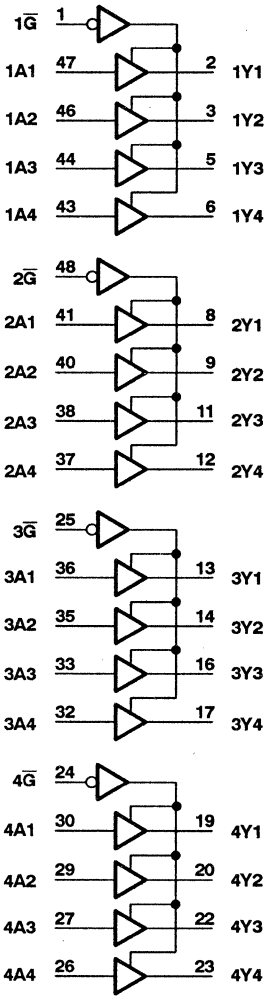
Widebus and EPIC are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 400 mA
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = −50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_I = V_{CC} or GND	5 V		12				

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	2	7.1	9.4	2	10.8	ns
t_{PHL}			2.4	8.3	10.7	2.4	11.8	
t_{PZH}	$\overline{G}$	Y	2.2	7.5	10	2.2	11.5	ns
t_{PZL}			2.9	10.4	13	2.9	14.6	
t_{PHZ}	$\overline{G}$	Y	4.1	6.8	8.4	4.1	9.1	ns
t_{PLZ}			3.7	6.5	8.1	3.7	8.8	

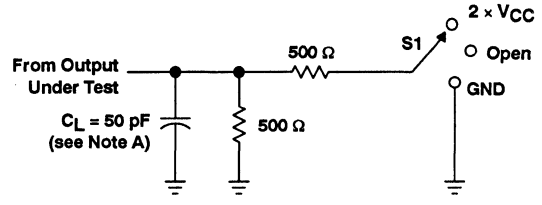
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.6	4.6	6.3	1.6	7.1	ns
t_{PHL}			2	5.3	7	2	7.9	
t_{PZH}	$\overline{G}$	Y	1.7	4.8	6.7	1.7	7.5	ns
t_{PZL}			2.2	6.1	8.1	2.2	9	
t_{PHZ}	$\overline{G}$	Y	4	6.4	7.8	4	8.4	ns
t_{PLZ}			3.5	5.5	7.2	3.5	7.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

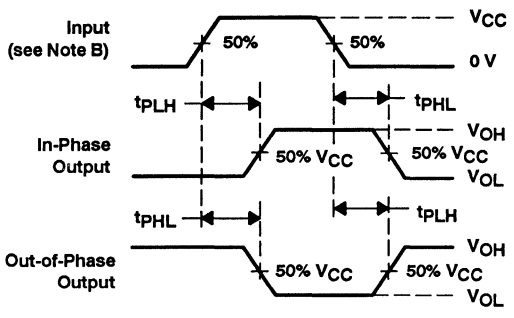
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		7	

PARAMETER MEASUREMENT INFORMATION

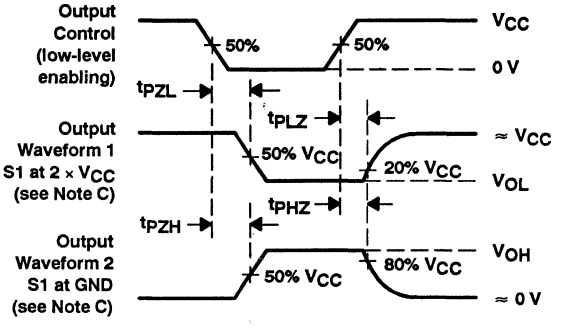


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



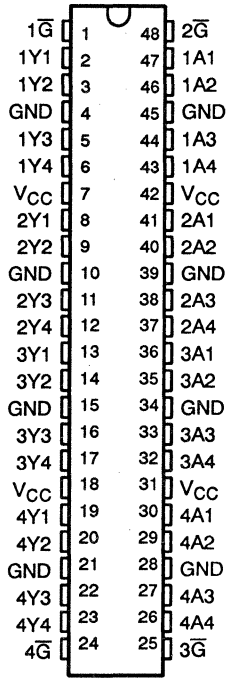
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Shrink and Plastic Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16244 . . . WD PACKAGE
74ACT16244 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ACT16244 is a 16-bit buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical $\overline{G}$ (active-low) output-enable inputs.

The 'ACT16244 is packaged in the TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

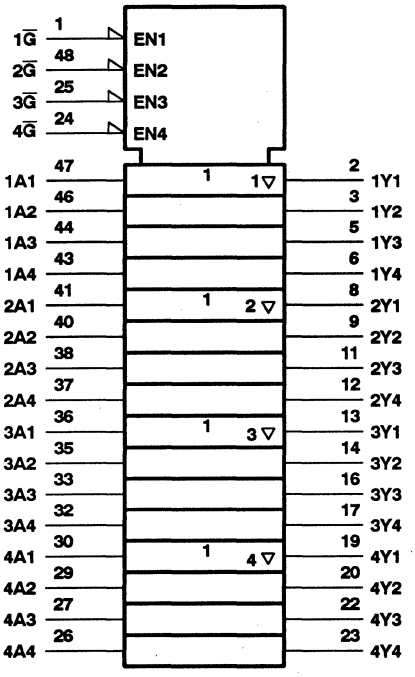
The 54ACT16244 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT16244 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

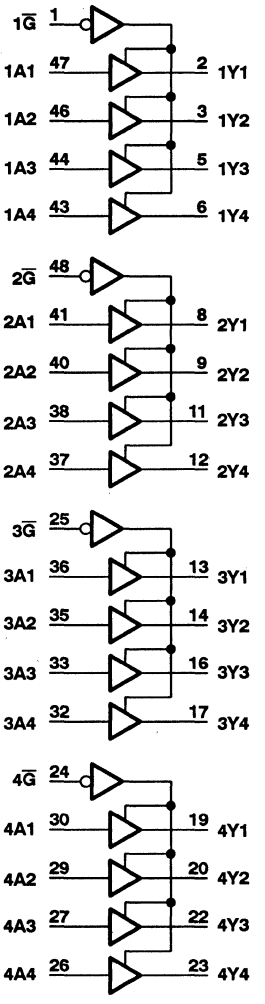
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16244		74ACT16244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16244		74ACT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		13.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

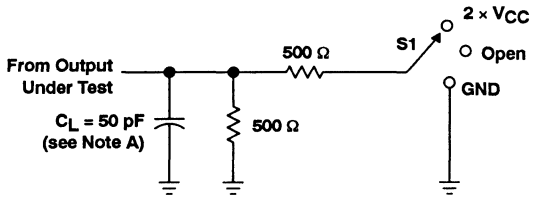
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16244		74ACT16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4	6.5	8.5	4	10.3	4	9.4	ns
t_{PHL}			3.4	6.3	8.7	3.4	10.1	3.4	9.5	
t_{PZH}	$\overline{G}$	Y	3	5.8	8.1	3	9.5	3	8.9	ns
t_{PZL}			3.7	6.7	9.3	3.7	11	3.7	10.3	
t_{PHZ}	$\overline{G}$	Y	5.4	8.1	10.3	5.4	12	5.4	11.3	ns
t_{PLZ}			5	7.5	9.5	5	10.9	5	10.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

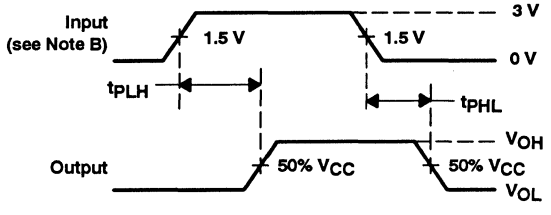
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

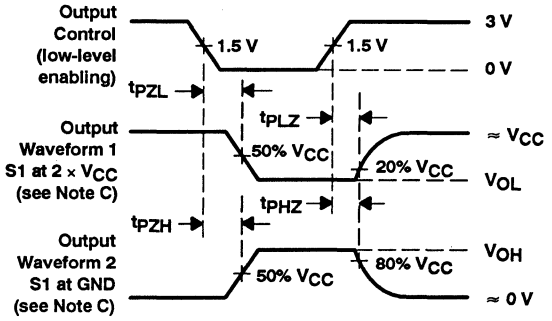


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
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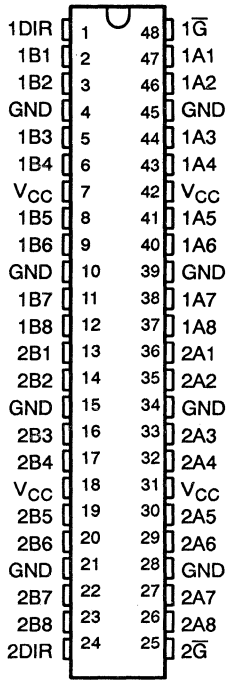
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Shrink and Plastic Thin Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**

DGG OR DL PACKAGE
(TOP VIEW)



description

The 74AC16245 is a 16-bit bus transceiver organized as a dual-octal noninverting 3-state transceiver and is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the devices so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16245 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to bus
H	X	Isolation

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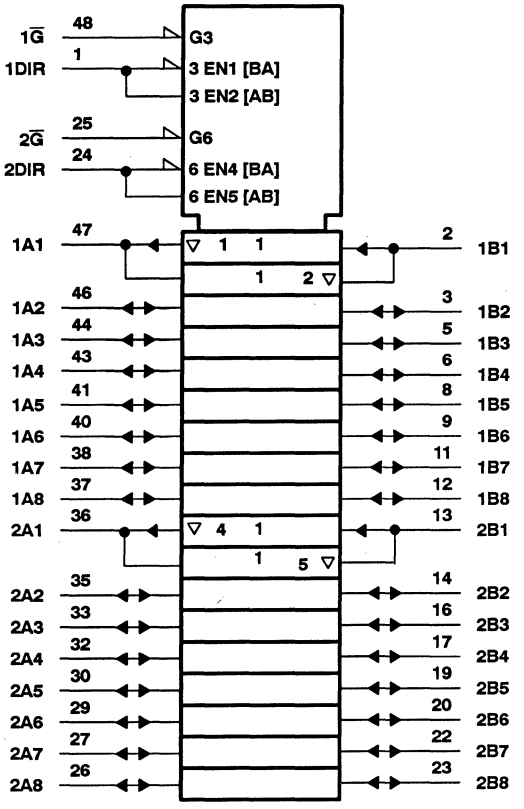
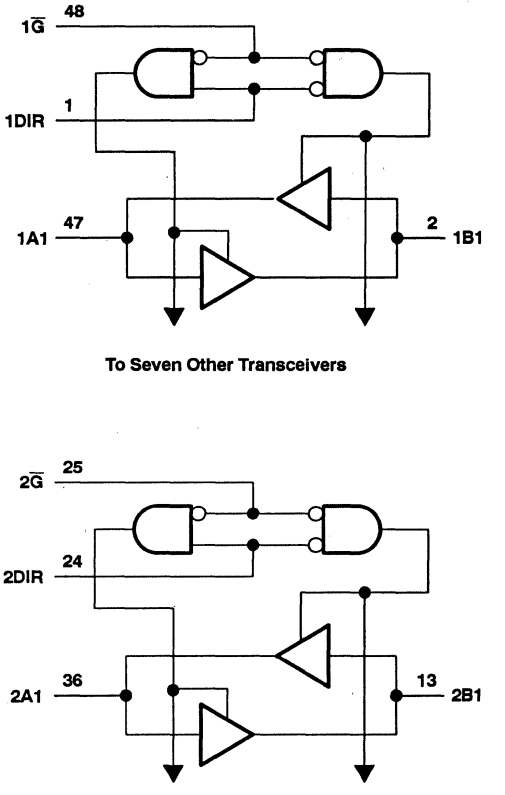
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 400 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_I = V_{CC} or GND	5 V		16				

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.5	7.6	10.4	2.5	11.9	ns
t_{PHL}			3.1	9	12.3	3.1	13.5	
t_{PZH}	$\overline{G}$	A or B	2.8	8.6	11.8	2.8	13.2	ns
t_{PZL}			3.9	12	16.2	3.9	18	
t_{PHZ}	$\overline{G}$	A or B	5.3	8.4	10.4	5.3	11.2	ns
t_{PLZ}			4.4	7.7	9.7	4.4	10.3	

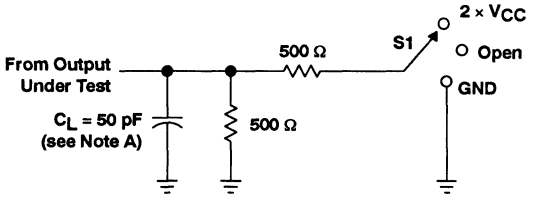
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2	4.6	6.9	2	7.9	ns
t_{PHL}			2.5	5.2	7.9	2.5	8.9	
t_{PZH}	$\overline{G}$	A or B	2.3	4.9	7.5	2.3	8.6	ns
t_{PZL}			3	6.2	9.5	3	10.7	
t_{PHZ}	$\overline{G}$	A or B	5	7.2	9.1	5	9.8	ns
t_{PLZ}			4.2	6.2	8.1	4.2	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

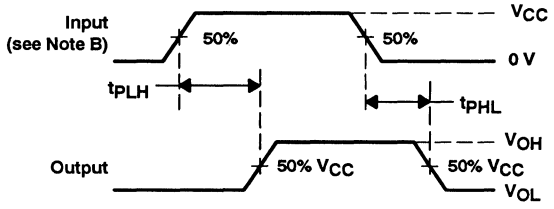
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		8	

PARAMETER MEASUREMENT INFORMATION

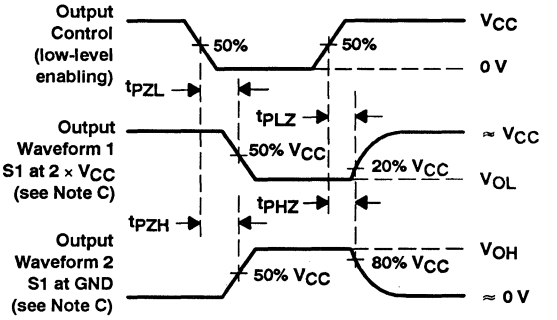


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

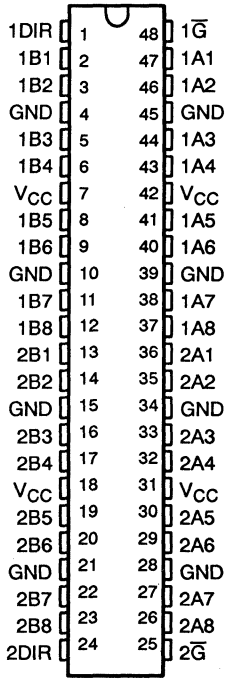
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS097 – D3402, DECEMBER 1989 – REVISED APRIL 1993

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged In Shrink Small-Outline 300-mil Package and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Distributed V_{CC} and GND Configuration to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Shrink and Plastic Thin Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16245 . . . WD PACKAGE
74ACT16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ACT16245 is a 16-bit bus transceiver organized as a dual-octal noninverting 3-state transceiver and is designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the devices so that the buses are effectively isolated.

The 54ACT16245 is characterized over the full military temperature range of – 55°C to 125°C. The 74ACT16245 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A Bus
L	H	A data to B Bus
H	X	Isolation

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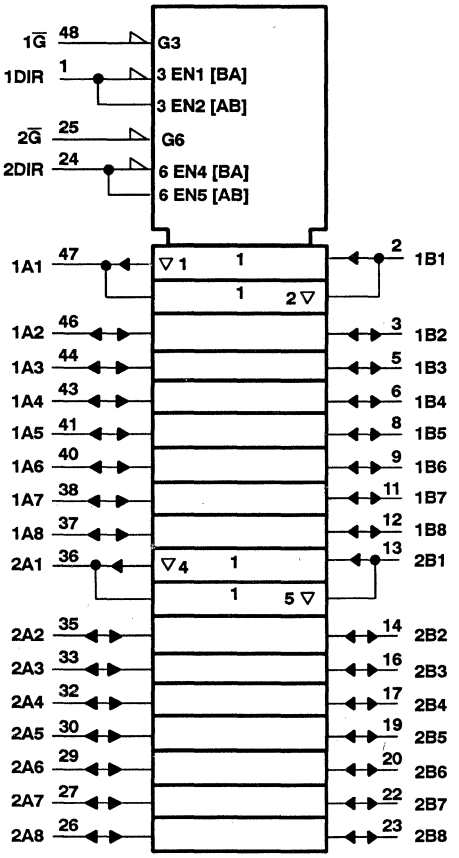
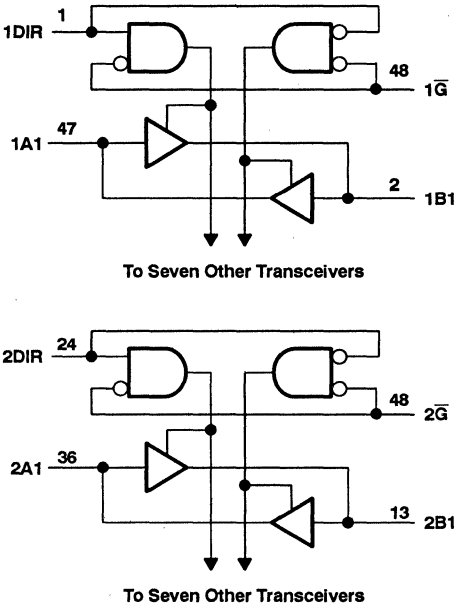
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . . ± 400 mA
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16245		74ACT16245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	– 40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16245		74ACT16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.94		3.8		
			5.5 V	4.94			4.94		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

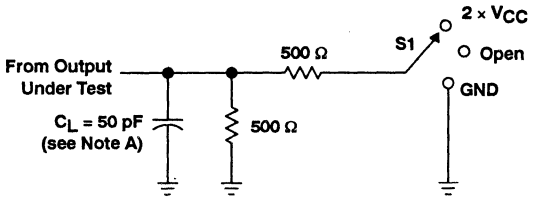
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	nA or nB	nB or nA	3.2	6.9	9.3	3.2	11.5	3.2	10.5	ns
t_{PHL}			2.6	6.4	9.2	2.6	11.1	2.6	10.2	
t_{PZH}	$n\overline{G}$	nB or nA	2.7	6.4	9.1	2.7	10.9	2.7	10	ns
t_{PZL}			3.4	7.4	10.5	3.4	12.6	3.4	11.6	
t_{PHZ}	$\overline{G}$	nB or nA	5.8	9.2	11.6	5.8	13.4	5.8	12.6	ns
t_{PLZ}			5.5	8.5	10.8	5.5	12.7	5.5	11.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

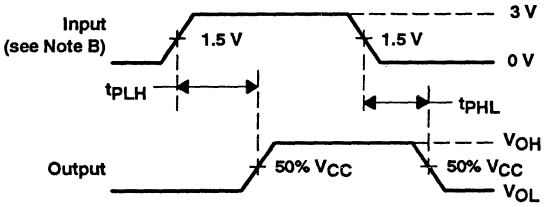
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

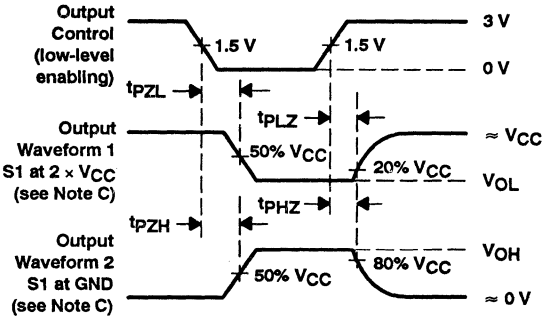


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



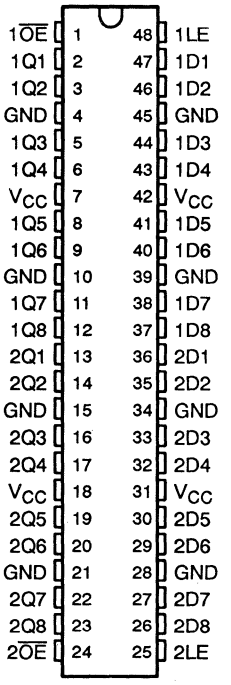
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**
- **3-State True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74AC16373 is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output enable ($\overline{OE}$) does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16373 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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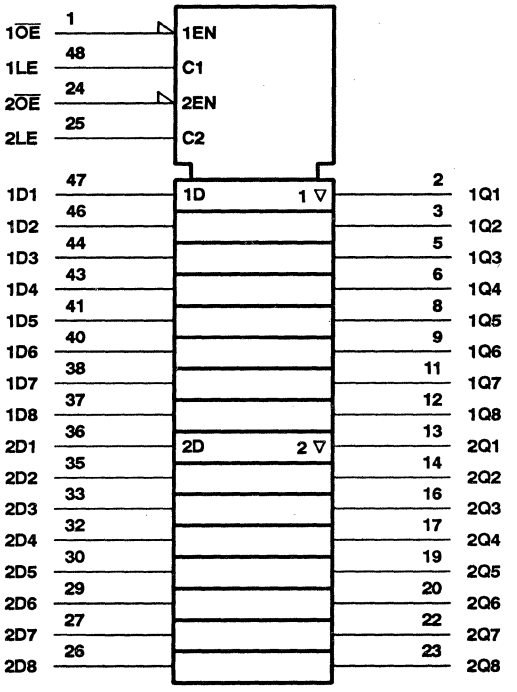
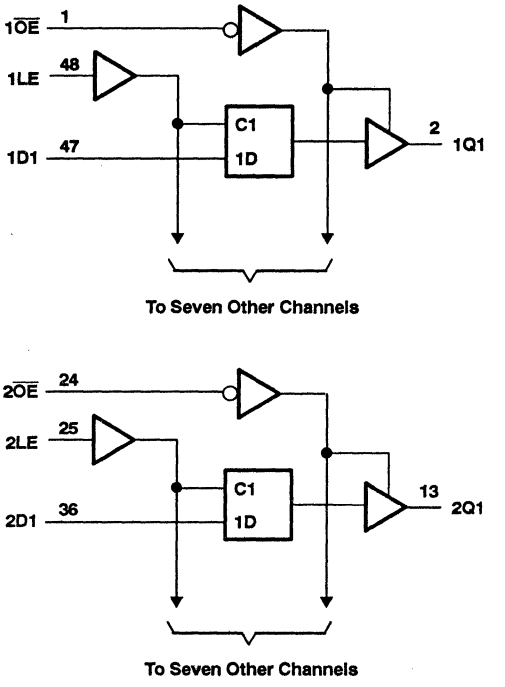
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OL} = –24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	5		5		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		ns
t_h	Hold time, data after LE↓	3		3		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	4		4		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		ns
t_h	Hold time, data after LE↓	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	3.7	10.6	13.4	3.7	15.1	ns
t_{PHL}			4.3	11.3	14	4.3	14.8	
t_{PLH}	LE	Q	4.6	12.9	15.8	4.6	18.6	ns
t_{PHL}			4.5	12.1	14.6	4.5	16.4	
t_{PZH}	$\overline{OE}$	Q	4.2	11.8	14.8	4.2	17.5	ns
t_{PZL}			5.4	16.3	19.8	5.4	22.3	
t_{PHZ}	$\overline{OE}$	Q	4.2	7.9	9.5	4.2	10.2	ns
t_{PLZ}			3.8	7.1	8.9	3.8	9.8	

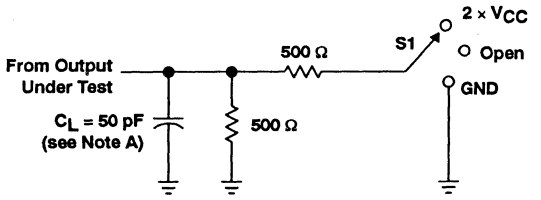
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	3.1	6.7	8.5	3.1	9.7	ns
t_{PHL}			3.5	7.3	9.1	3.5	10.1	
t_{PLH}	LE	Q	3.8	8.2	10.2	3.8	11.9	ns
t_{PHL}			3.6	7.8	9.7	3.6	10.9	
t_{PZH}	$\overline{OE}$	Q	3.5	7.4	9.4	3.5	10.8	ns
t_{PZL}			4.3	9.1	11.3	4.3	12.8	
t_{PHZ}	$\overline{OE}$	Q	3.9	6.6	8	3.9	8.8	ns
t_{PLZ}			3.7	5.9	7.4	3.7	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

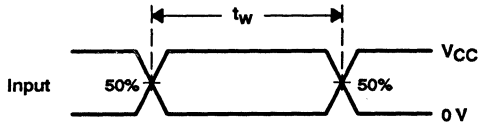
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		5	

PARAMETER MEASUREMENT INFORMATION

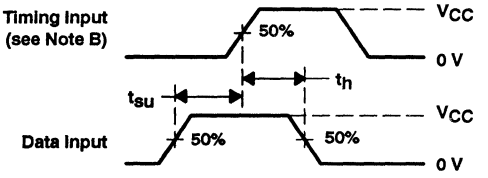


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

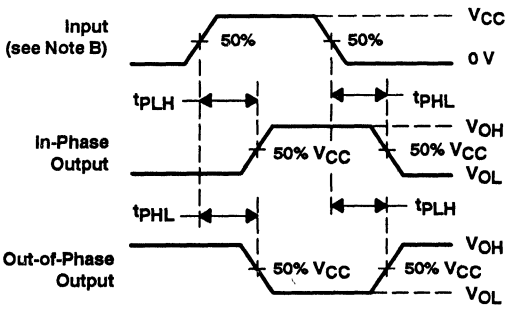
LOAD CIRCUIT



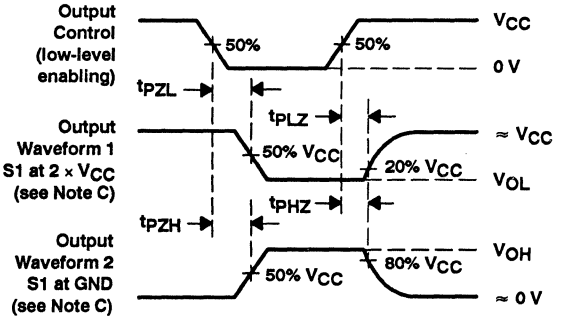
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



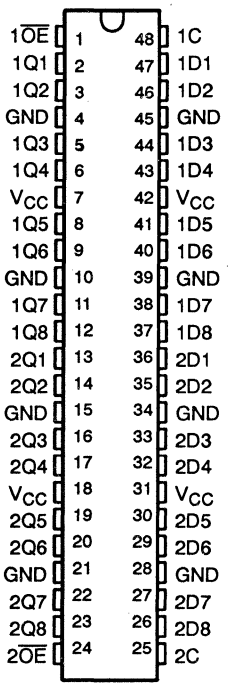
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16373 . . . WD PACKAGE
74ACT16373 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16373 is a 16-bit D-type transparent latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches will follow the D inputs if enable C is taken high. When C is taken low, the Q outputs will be latched at the levels set up at the D inputs.

A buffered output-enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output enable $\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16373 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

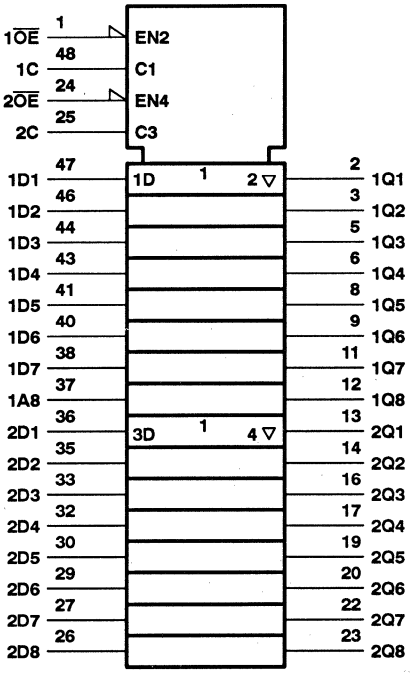
The 54ACT16373 is characterized over the full military temperature range of – 55°C to 125°C. The 74ACT16373 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

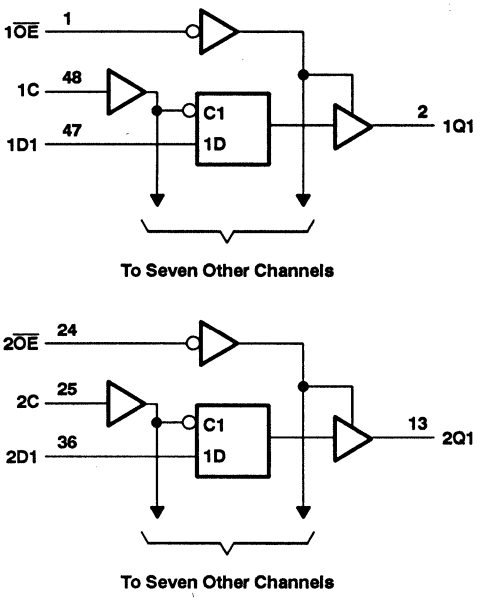
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 400 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 3)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTES: 2. Unused or floating inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_I = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54ACT16373		74ACT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, C high	4		4		1		ns
t_{su}	Setup time, data before C↓	1		1		1		ns
t_h	Hold time, data after C↓	5		5		5		ns

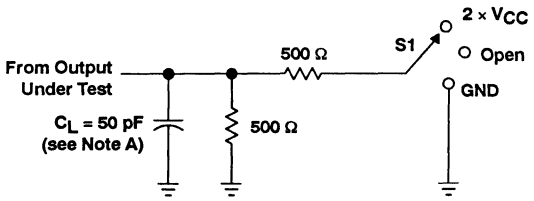
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16373		74ACT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.8	7.9	9.4	3.8	11.8	3.8	11.1	ns
t_{PHL}			3.1	8.2	9.7	3.1	13	3.1	12.3	
t_{PLH}	C	Q	4.6	9.3	10.8	4.6	13.7	4.6	12.8	ns
t_{PHL}			4.5	9.1	10.5	4.5	13	4.5	12.2	
t_{PZH}	$\overline{OE}$	Q	3.1	8	9.5	3.1	13	3.1	12.1	ns
t_{PZL}			3.8	9.4	11.1	3.8	15.1	3.8	14.2	
t_{PHZ}	$\overline{OE}$	Q	5.3	8.6	9.9	5.3	11	5.3	10.7	ns
t_{PLZ}			4.3	7.4	8.7	4.3	9.8	4.3	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

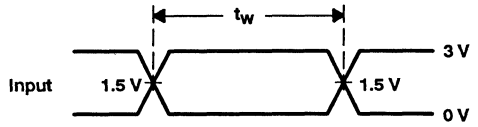
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
		Outputs disabled		4.5	

PARAMETER MEASUREMENT INFORMATION

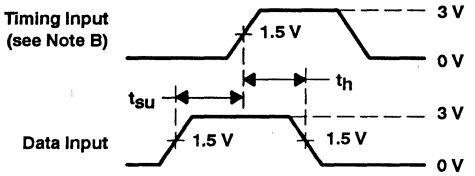


LOAD CIRCUIT

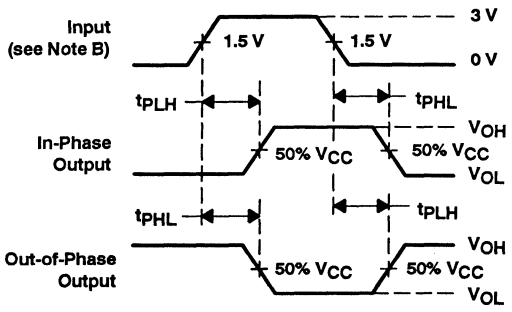
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



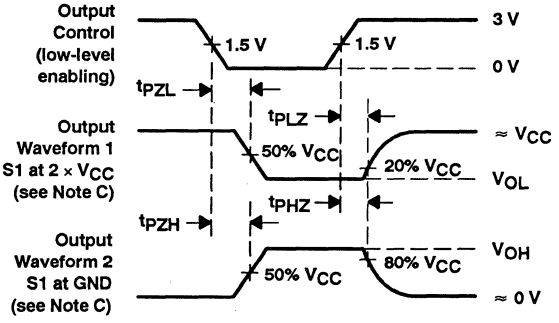
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **3-State True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
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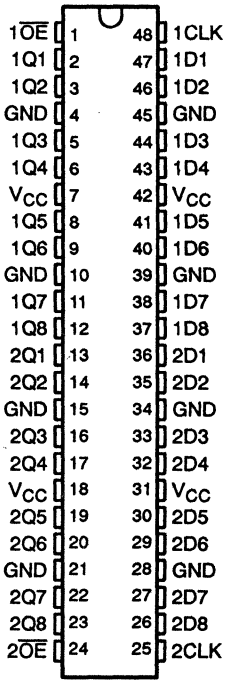
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74AC16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 74AC16374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output enable ($\overline{OE}$) does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

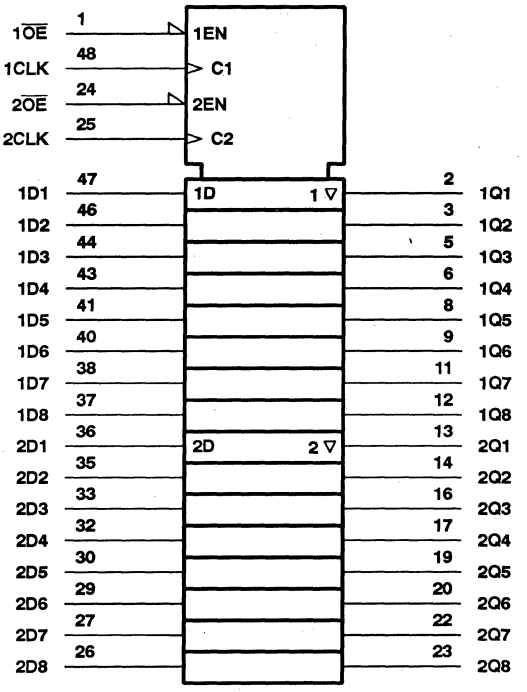
The 74AC16374 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

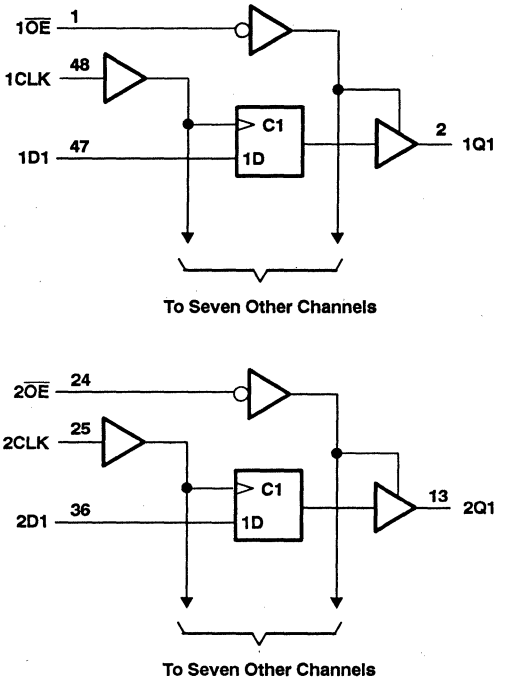
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	X	X	Q_0
L	↓	X	Q_0
H	X	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	TA = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA		3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
	I_{OH} = −4 mA		3 V	2.58			2.48		
	I_{OL} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA		3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
	I_{OL} = 12 mA		3 V			0.36		0.44	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND		5 V		3				pF
C_o	V_O = V_{CC} or GND		5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	60	0	60	MHz
t_w	Pulse duration	CLK high or low	8.3		8.3		ns
t_{su}	Setup time, data before CLK↑		7.5		7.5		ns
t_h	Hold time, data after CLK↑		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK↑		5		5		ns
t_h	Hold time, data after CLK↑		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			60			60		MHz
t_{PLH}	CLK	Q	4.9	12.2	15	4.9	17	ns
t_{PHL}			4.8	11.9	14.3	4.8	15.7	
t_{PZH}	$\overline{OE}$	Q	4.3	11.9	14.7	4.3	16.8	ns
t_{PZL}			5.3	15.5	18.7	5.3	21.2	
t_{PHZ}	$\overline{OE}$	Q	4	7.3	9	4	9.8	ns
t_{PLZ}			3.8	7.1	8.8	3.8	9.4	

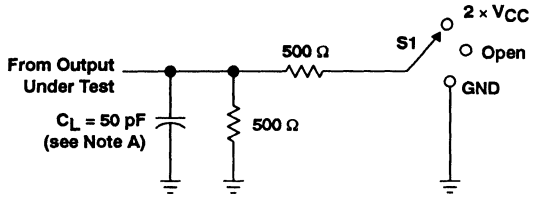
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100			100		MHz
t_{PLH}	CLK	Q	3.8	7.6	9.5	3.8	10.8	ns
t_{PHL}			3.8	7.6	9.5	3.8	10.6	
t_{PZH}	$\overline{OE}$	Q	3.2	7.2	9	3.2	10.2	ns
t_{PZL}			3.8	8.7	10.7	3.8	12.1	
t_{PHZ}	$\overline{OE}$	Q	3.7	6	7.5	3.7	8.2	ns
t_{PLZ}			3.5	5.8	7.3	3.5	7.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

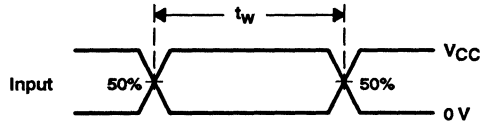
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	49	pF
		Outputs disabled		32	

PARAMETER MEASUREMENT INFORMATION

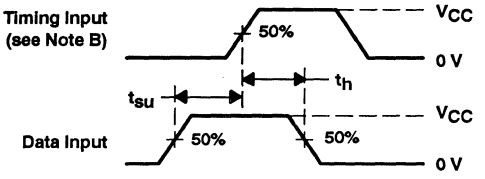


LOAD CIRCUIT

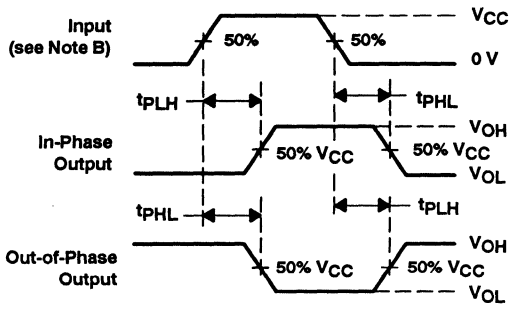
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



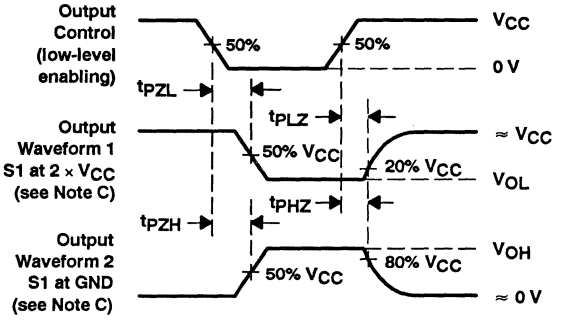
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



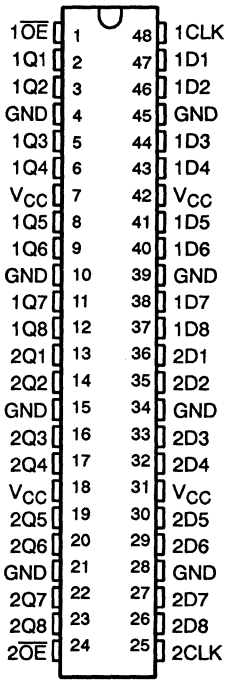
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package and 380-mil Fine-Pitch Ceramic Flat Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Bus-Driving True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16374 . . . WD PACKAGE
74ACT16374 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16374 is a 16-bit edge-triggered D-type flip-flop with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of CLK, the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

An output-enable input $\overline{OE}$ can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components. The output-enable $\overline{OE}$ does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16374 is packaged in TI's shrink small-outline package (SSOP), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit board area.

The 54ACT16374 is characterized over the full military temperature range of −55°C to 125°C. The 74ACT16374 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each section)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	K
L	L	X	Q_0
H	X	X	Z

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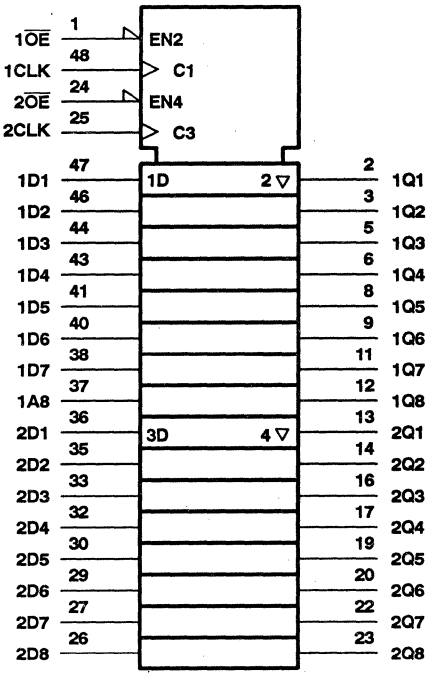
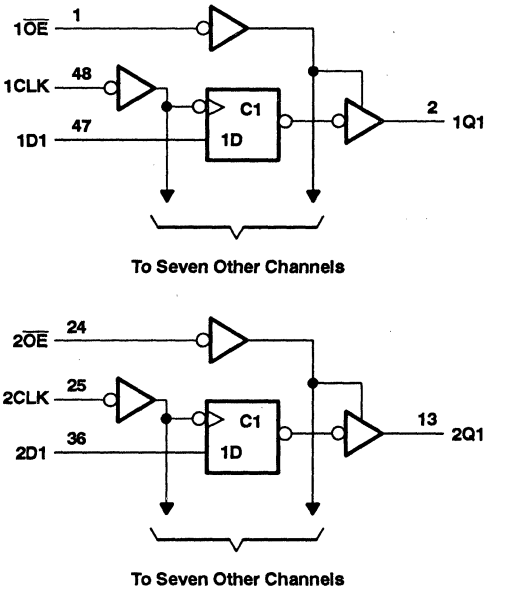
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT16374			74ACT16374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_o	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C		54ACT16374		74ACT16374		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	65	0	65	0	65	MHz
t_w	Pulse duration	CLK low	7.5		7.5		7.5		ns
		CLK high	4.5		4.5		4.5		
t_{su}	Setup time, data before C↑		6.5		6.5		6.5		ns
t_h	Hold time, data after C↑		1		1		1		ns

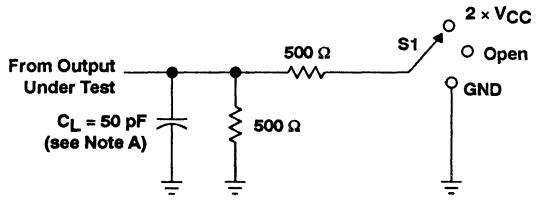
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16374		74ACT16374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	CLK	Q	5.1	8.8	10.9	5.1	13.2	5.1	12.4	ns
t_{PHL}			5.3	8.8	10.9	5.3	13.1	5.3	12.2	
t_{PZH}	$\overline{OE}$	Q	3.7	8.4	10.5	3.7	12.7	3.7	11.9	ns
t_{PZL}			4.4	9.7	11.9	4.4	14.3	4.4	13.4	
t_{PHZ}	$\overline{OE}$	Q	5.4	7.9	9.8	5.4	10.9	5.4	10.4	ns
t_{PLZ}			4.9	7.2	9.1	4.9	10.2	4.9	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

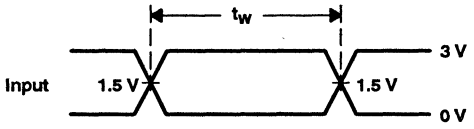
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		38	

PARAMETER MEASUREMENT INFORMATION

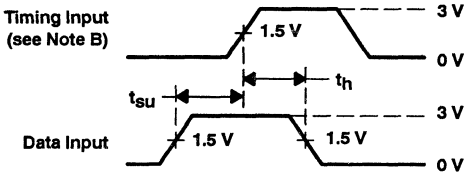


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

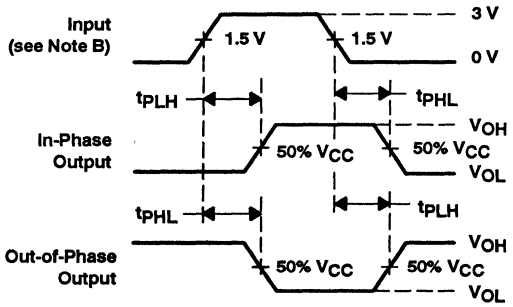
LOAD CIRCUIT



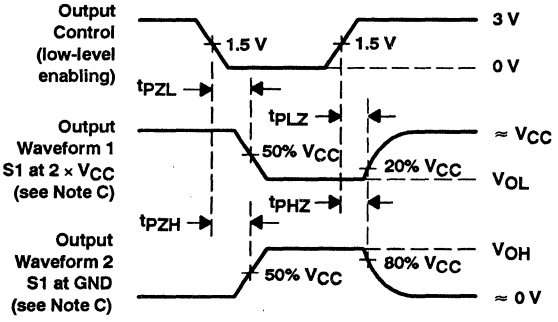
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
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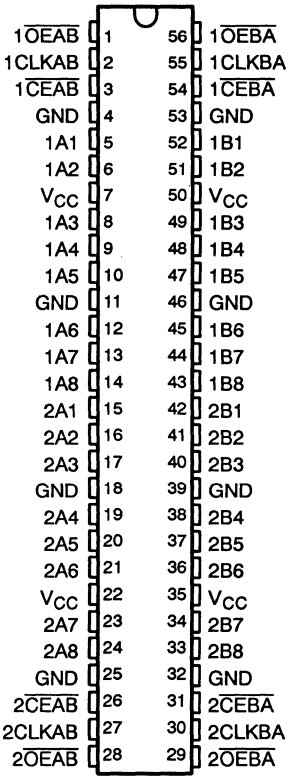
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16470 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate clock (CLKAB or CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. If both $\overline{CEAB}$ and CLKAB are low, then B port will have the level of A port prior to the most recent low-to-high transition of CLKAB. Data flow from B to A is similar, but requires the use of $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$ inputs.

To avoid false clocking of the flip-flops, $\overline{CE}$ should not be switched from high to low while CLK is high.

The 74ACT16470 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16470 is characterized for operation from −40°C to 85°C.

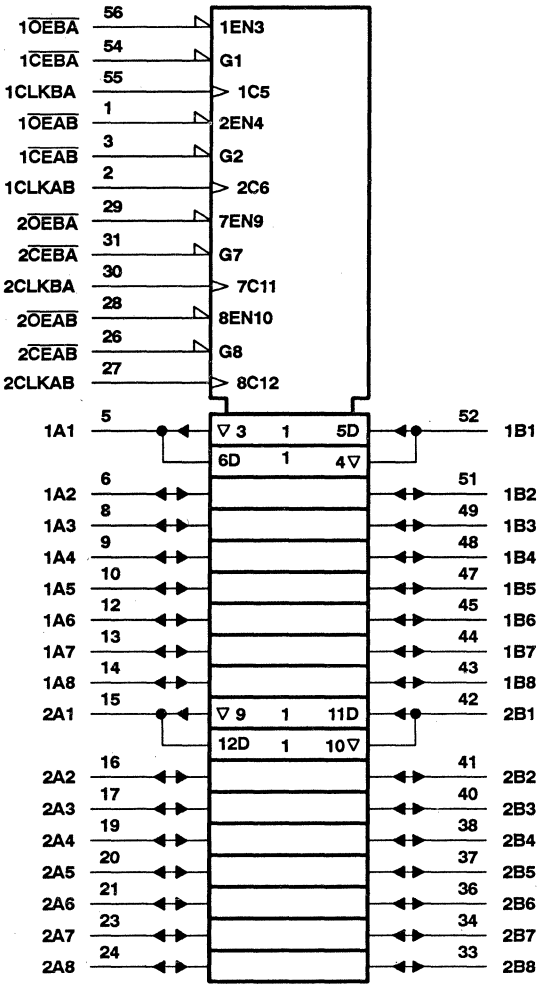
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

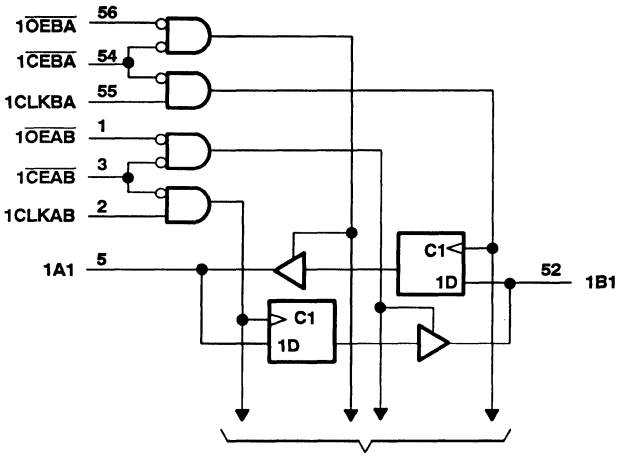
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

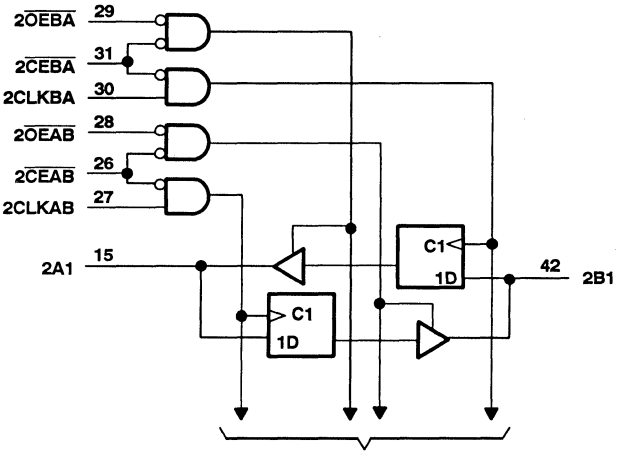
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		11.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	55	0	55	MHz
t_w	Pulse duration	CLK high	4		4		ns
		CLK low	8.5		8.5		
t_{su}	Setup time	Data before CLK↑	6		6		ns
t_h	Hold time	Data after CLK↑	1		1		ns

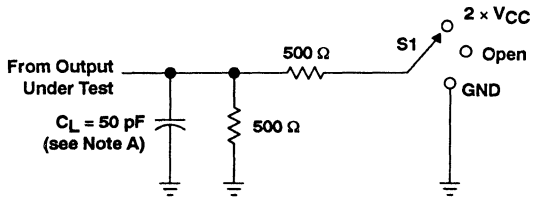
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see NO TAG)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			55			55		MHz
t_{PLH}	CLK	A or B	3.9	8.3	10.3	3.9	11.8	ns
t_{PHL}			3.8	8.4	10.3	3.8	11.7	
t_{PZH}	$\overline{OE}$	A or B	3.2	8.3	10.5	3.2	11.9	ns
t_{PZL}			3.6	9.5	11.8	3.6	13.4	
t_{PHZ}	$\overline{OE}$	A or B	4.6	7.4	9.3	4.6	9.9	ns
t_{PLZ}			4.6	7	8.8	4.6	9.5	
t_{PZH}	$\overline{CE}$	A or B	3.5	8.8	10.9	3.5	12.5	ns
t_{PZL}			4.2	10.1	12.4	4.2	14.3	
t_{PHZ}	$\overline{CE}$	A or B	5.2	8.3	10.3	5.2	11.2	ns
t_{PLZ}			5.2	7.9	10	5.2	10.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

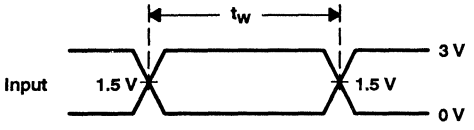
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		39	

PARAMETER MEASUREMENT INFORMATION

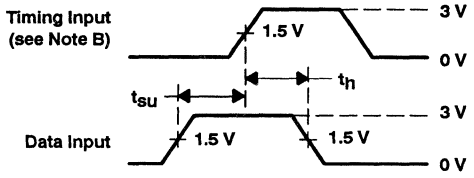


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

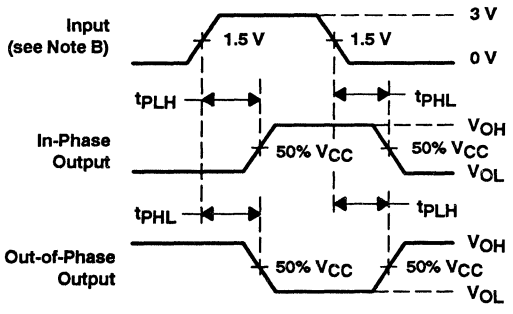
LOAD CIRCUIT



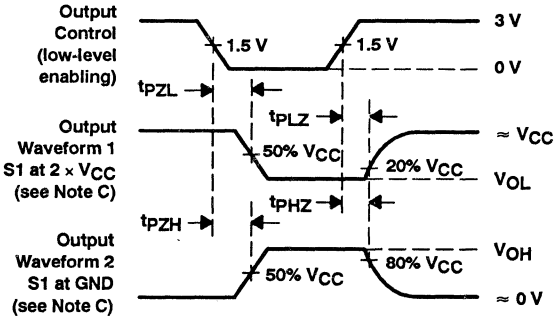
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



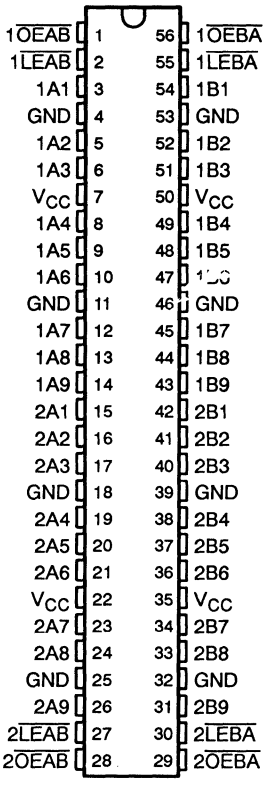
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74AC16472 is an 18-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. It can be used as two 9-bit transceivers or one 18-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

When $\overline{OEAB}$ and $\overline{LEAB}$ are both low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{OEAB}$ low, the B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires the use of the $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

The 74AC16472 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16472 is characterized for operation from −40°C to 85°C.

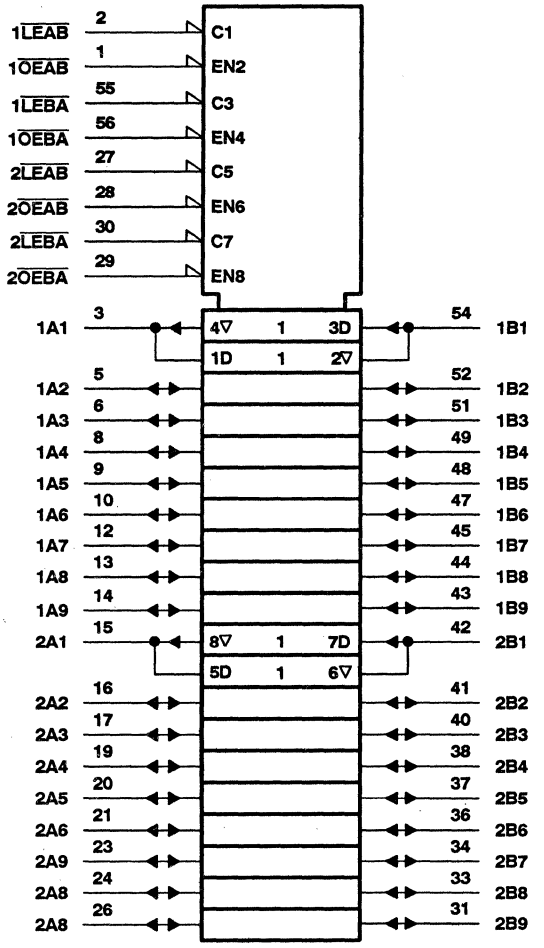
FUNCTION TABLE†

INPUTS			OUTPUT
$\overline{LEAB}$	$\overline{OEAB}$	A	B
X	H	X	Z
H	L	X	B_0‡
L	L	H	H
L	L	L	L

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{LEBA}$ and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

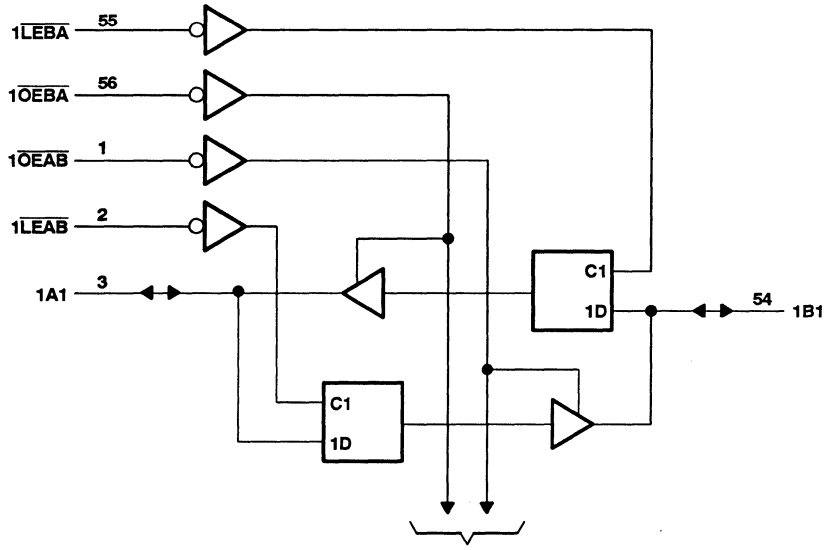
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

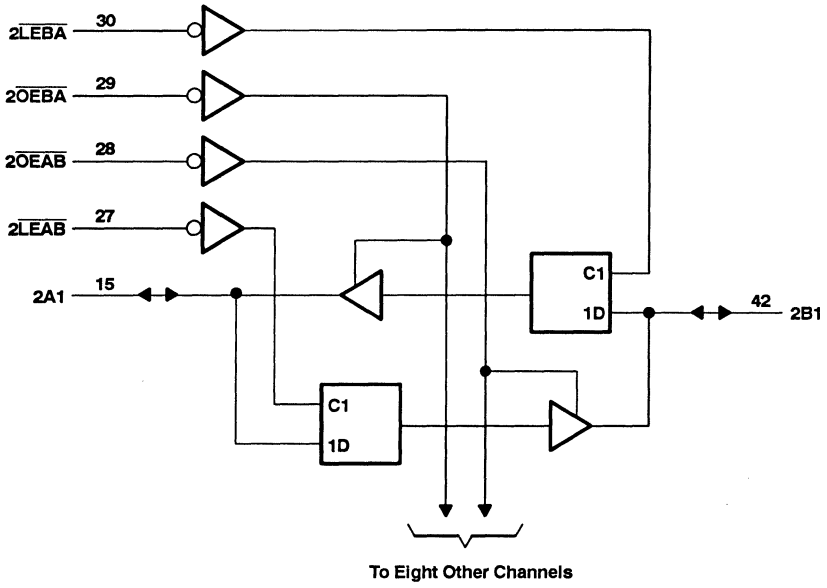
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.48		
		I_{OL} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		3				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		11.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	4		4		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	0.5		0.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	3.5		3.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	4		4		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	0.5		0.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.5	8	12.5	3.5	14.2	ns
t_{PHL}			3.9	8.4	12.8	3.9	13.9	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	4.8	10.3	15.6	4.8	17.9	ns
t_{PHL}			4.7	9.7	14.7	4.7	16.3	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.9	8.9	14	3.9	15.9	ns
t_{PZL}			5	11.2	17.6	5	19.7	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.4	7	9.4	4.4	10	ns
t_{PLZ}			4	6.4	8.7	4	9.4	

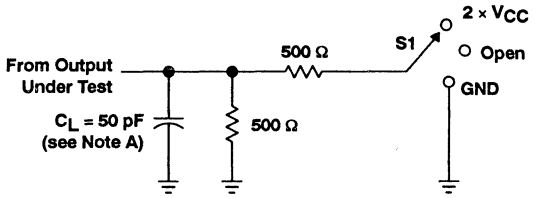
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.9	5.6	8.4	2.9	9.5	ns
t_{PHL}			3.1	6	8.7	3.1	9.6	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	7.3	10.3	3.9	11.7	ns
t_{PHL}			3.7	6.9	9.7	3.7	10.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.1	6.2	8.9	3.1	10.2	ns
t_{PZL}			3.9	7.3	10.4	3.9	11.6	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.3	6.2	8.1	4.3	8.6	ns
t_{PLZ}			3.8	5.7	7.4	3.8	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

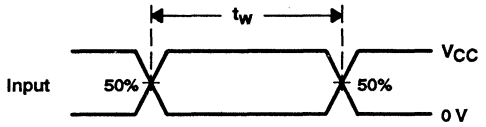
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
		Outputs disabled		6	

PARAMETER MEASUREMENT INFORMATION

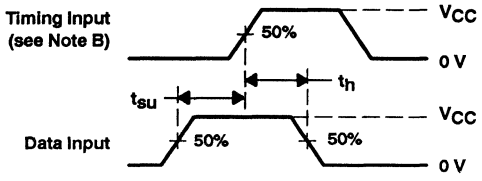


LOAD CIRCUIT

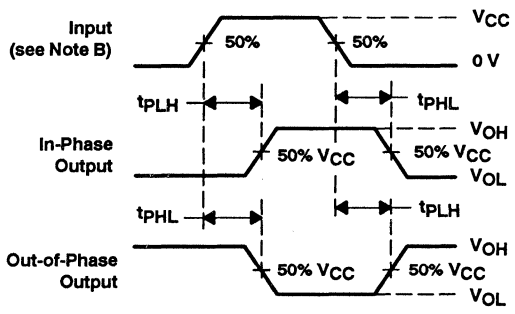
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



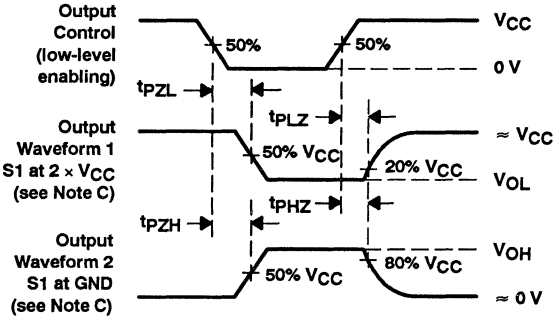
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



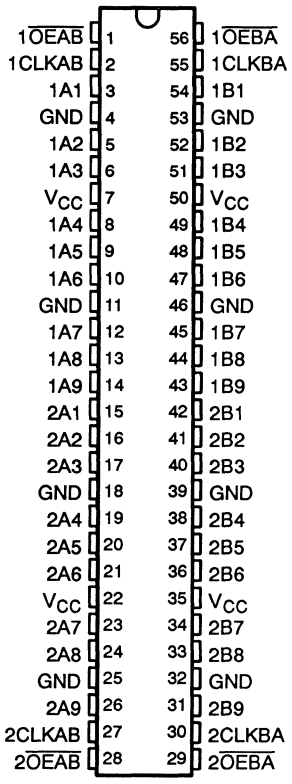
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16474 is a noninverting 18-bit registered bus transceiver composed of two 9-bit sections with separate control signals. For either 9-bit transceiver section, data flow in the A-to-B mode is controlled by output-enable ($1\overline{OEAB}$ or $2\overline{OEAB}$) and clock (1CLKAB or 2CLKAB) inputs. When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is low, the corresponding outputs are active (high or low) and take on either the current data on low-to-high transition of 1CLKAB (or 2CLKAB) or the previously stored data if 1CLKAB (or 2CLKAB) is low.

When $1\overline{OEAB}$ (or $2\overline{OEAB}$) is high, the corresponding outputs are in the high-impedance state. $1\overline{OEAB}$ (or $2\overline{OEAB}$) does not affect the operation on the internal registers. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Data flow from B to A is similar, but uses $1\overline{OEBA}$ (and/or $2\overline{OEBA}$) and 1CLKBA (and/or 2CLKBA).

The 74ACT16474 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16474 is characterized for operation from −40°C to 85°C.

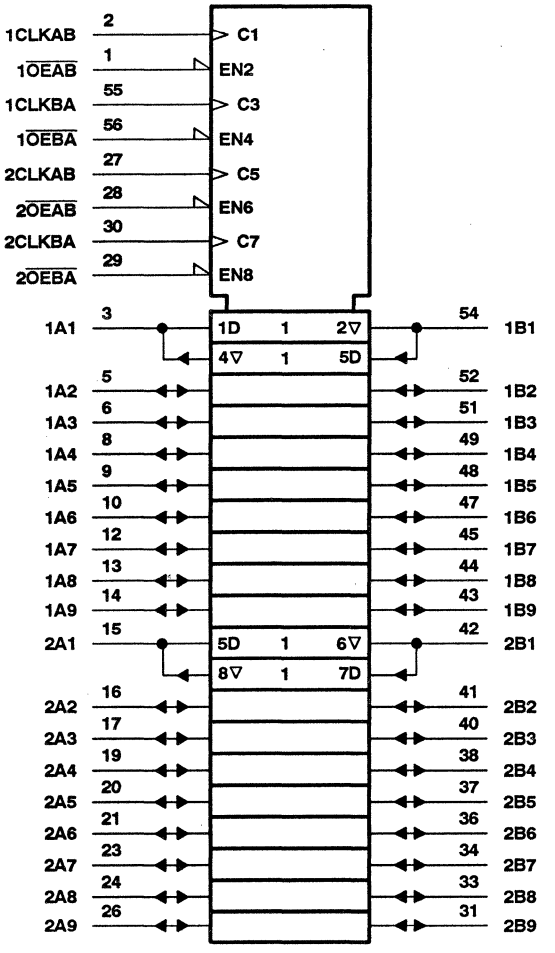
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE†

INPUTS			OUTPUT
CLKAB	$\overline{OEAB}$	A	B
X	H	X	Z
L	L	X	B_0‡
↑	L	H	H
↑	L	L	L

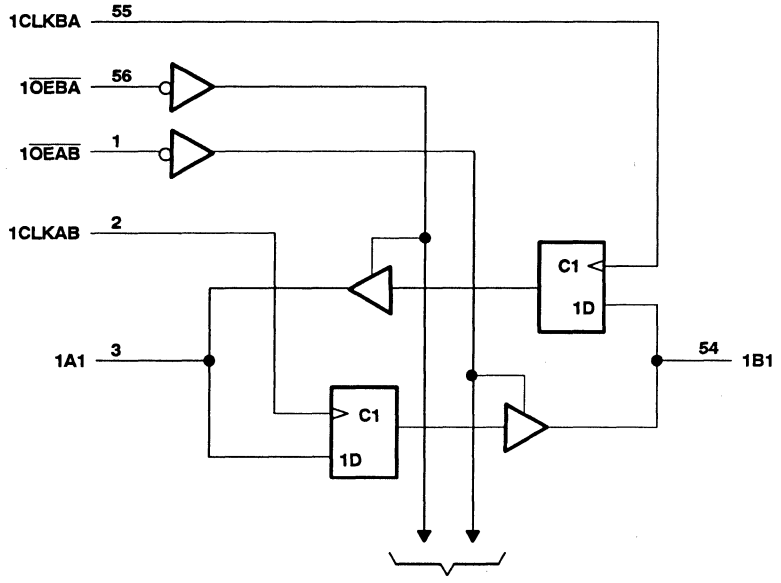
† A-to-B data flow is shown: B-to-A flow is similar but uses CLKBA, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

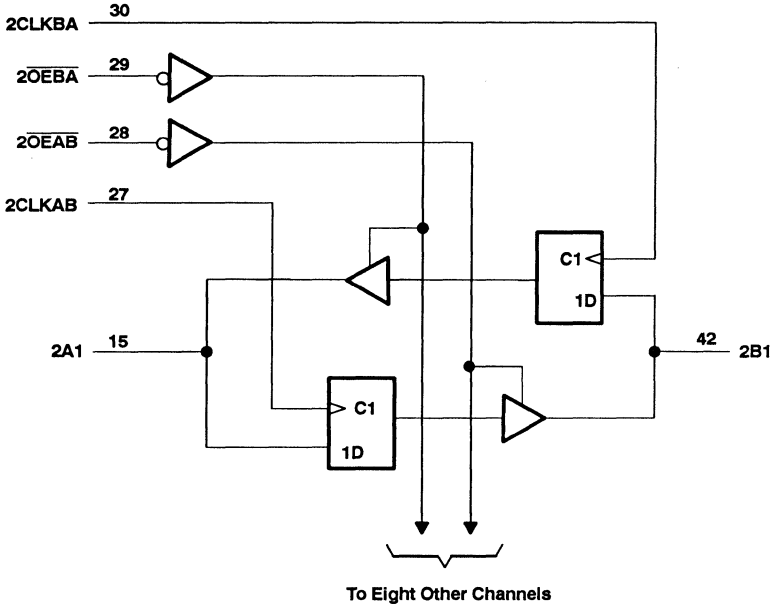
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		11.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	75	0	75	MHz
t_w	Pulse duration	CLK high	4		4		ns
		CLK low	6.6		6.6		
t_{su}	Setup time	Data before CLK↑	5.5		5.5		ns
t_h	Hold time	Data after CLK↑	1		1		ns

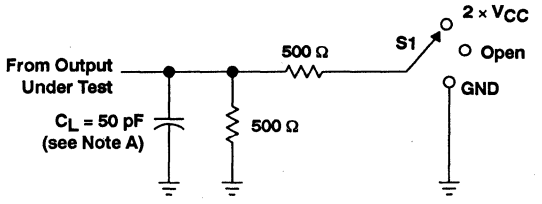
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75			75		MHz
t_{PLH}	CLK	A or B	4	8	10.2	4	11.5	ns
t_{PHL}			4.2	8	10.2	4.2	11.4	
t_{PZH}	$\overline{OE}$	A or B	3	7.8	10.3	3	11.7	ns
t_{PZL}			3.7	9.2	11.6	3.7	13.1	
t_{PHZ}	$\overline{OE}$	A or B	4.8	7.1	8.8	4.8	9.5	ns
t_{PLZ}			4.4	6.6	8.4	4.4	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

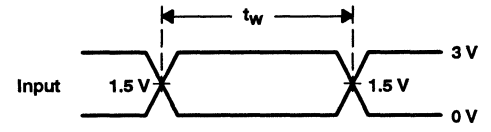
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	61	pF
		Outputs disabled		37	

PARAMETER MEASUREMENT INFORMATION

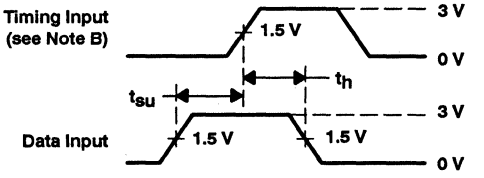


LOAD CIRCUIT

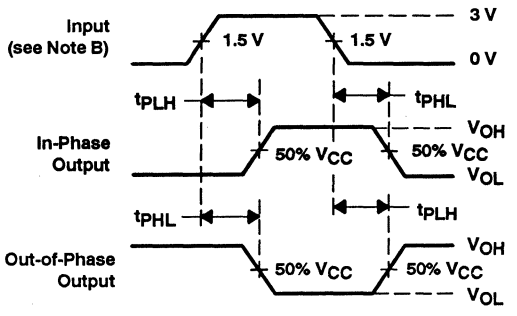
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



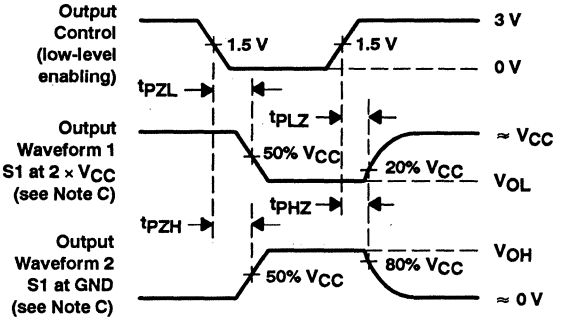
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
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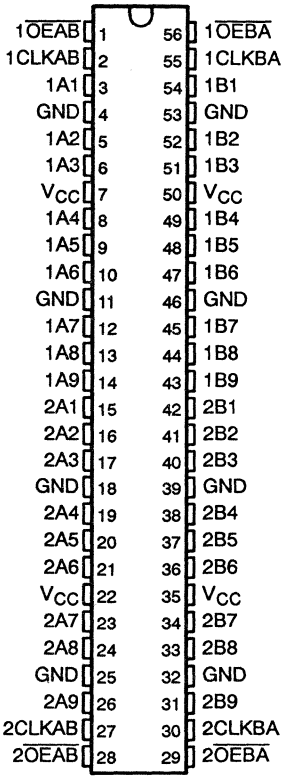
- **3-State Inverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16475 is an 18-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 9-bit transceivers or one 18-bit transceiver. Separate clock (CLKAB and CLKBA) and output-enable ($\overline{OEAB}$ or $\overline{OEAB}$) inputs are provided for each register to permit independent control in either direction of data flow.

Data at the A inputs meeting the setup time requirements is transferred to the B outputs on the positive-going edge of CLKAB. With $\overline{OEAB}$ low, the 3-state B outputs are enabled and reflect the inverted A data. Data flow from B to A is similar but requires the use of the CLKAB and $\overline{OEBA}$ inputs.

The 74ACT16475 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16475 is characterized for operation from −40°C to 85°C.

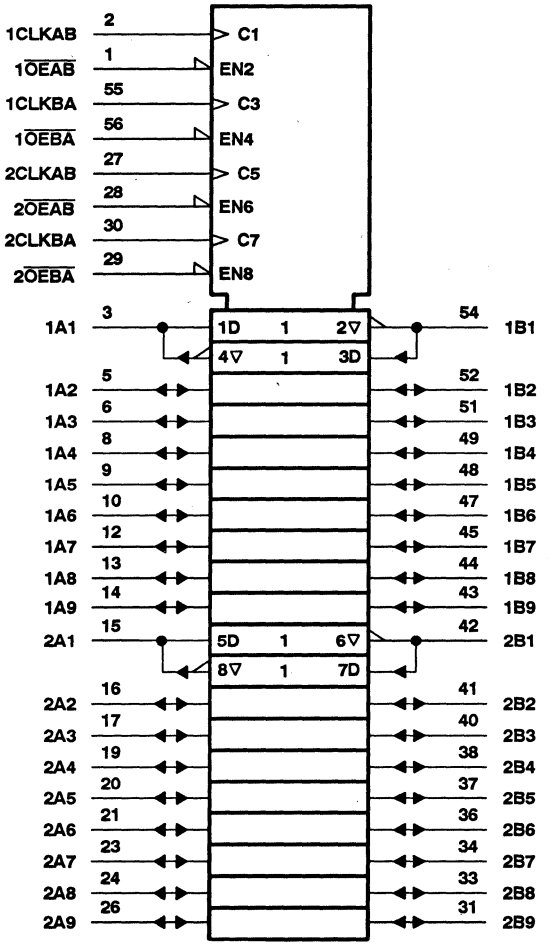
FUNCTION TABLE†

INPUTS			OUTPUT
$\overline{OEAB}$	CLKAB	A	B
H	X	X	Z
L	L	X	B_0‡
L	↑	L	H
L	↑	H	L

† A-to-B data flow is shown: B-to-A flow is similar but uses CLKBA and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

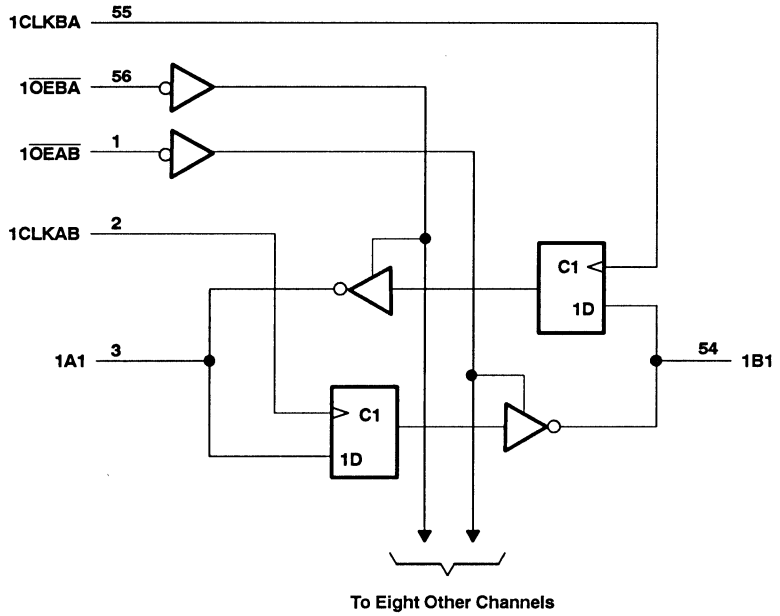
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

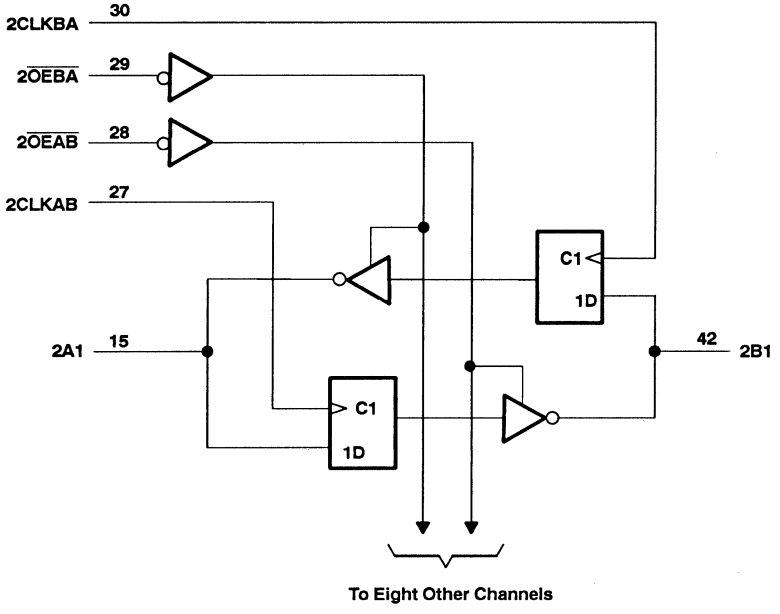
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	75	0	75	MHz
t_w	Pulse duration	CLK high or low	6.5		6.5		ns
t_{su}	Setup time	Data before CLK↑	5.5		5.5		ns
t_h	Hold time	Data after CLK↑	1.5		1.5		ns

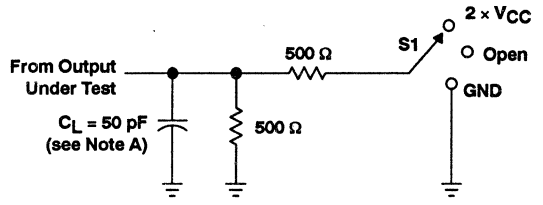
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75			75		MHz
t_{PLH}	CLKAB or CLKBA	B or A	3.8	7.9	11.1	3.8	12.5	ns
t_{PHL}			4.2	8.1	11.4	4.2	12.6	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.8	7.3	11.4	2.8	12.8	ns
t_{PZL}			3.4	7.4	13.1	3.4	14.8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	5.2	6.5	9.8	5.2	10.5	ns
t_{PLZ}			4.5	6.6	9.1	4.5	9.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

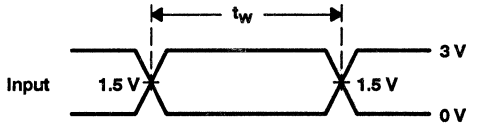
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	27	pF
		Outputs disabled			9	

PARAMETER MEASUREMENT INFORMATION

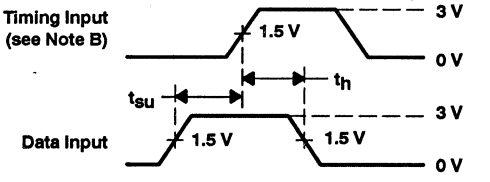


LOAD CIRCUIT

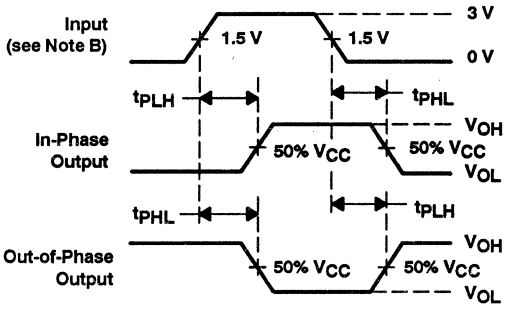
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



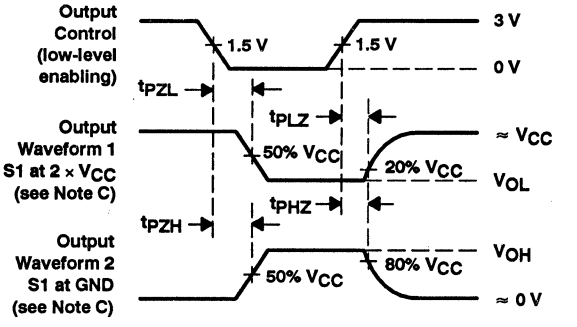
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



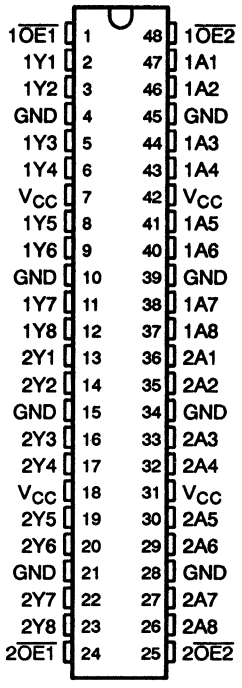
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths**
- **Provide Inverted Data**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/bus driver provides a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The 74ACT16540 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

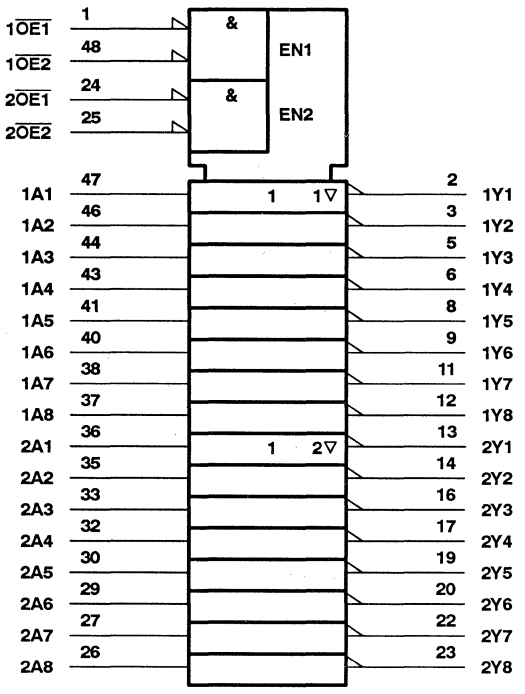
The 74ACT16540 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

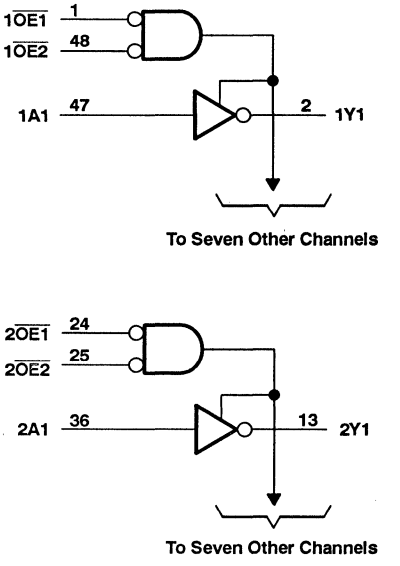
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		13				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

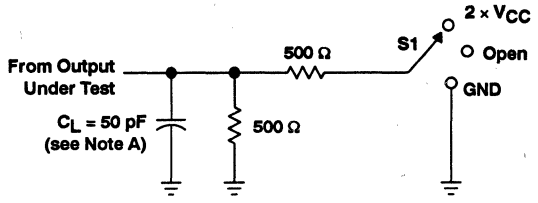
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	2.1	5.1	6.8	2.1	7.5	ns
t_{PHL}			3.9	6.8	8.5	3.9	9.5	
t_{PZH}	$\overline{OE}$	Y	2.7	6.2	8	2.7	8.9	ns
t_{PZL}			3.6	7.5	9.5	3.6	10.5	
t_{PHZ}	$\overline{OE}$	Y	5.4	9.2	10.9	5.4	11.9	ns
t_{PLZ}			5.4	8.6	10.3	5.4	11.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

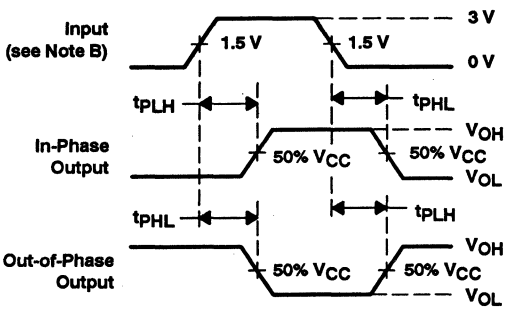
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		8.5	

PARAMETER MEASUREMENT INFORMATION

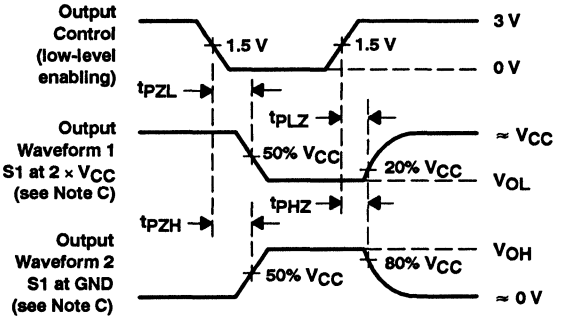


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



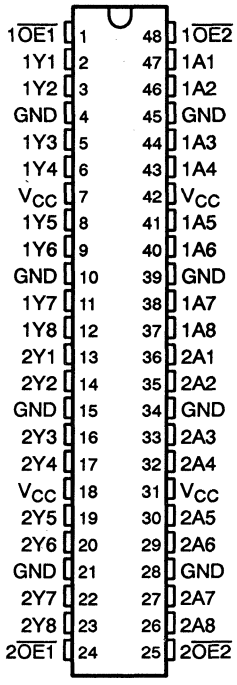
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL- or CMOS-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16541 is a noninverting 16-bit buffer composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

The 74ACT16541 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

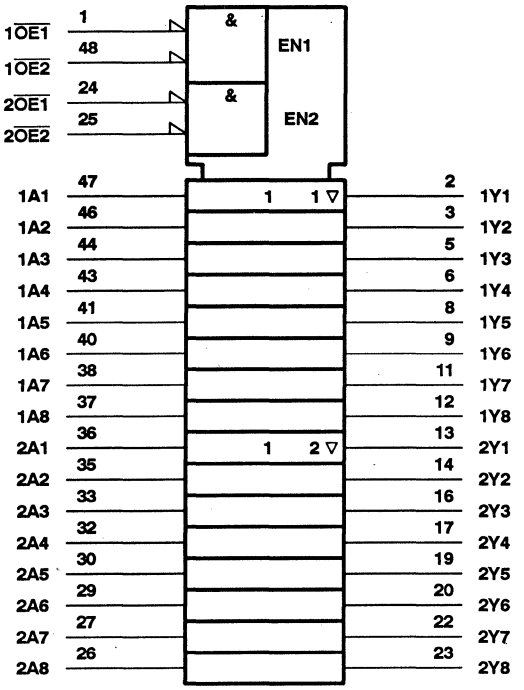
The 74ACT16541 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

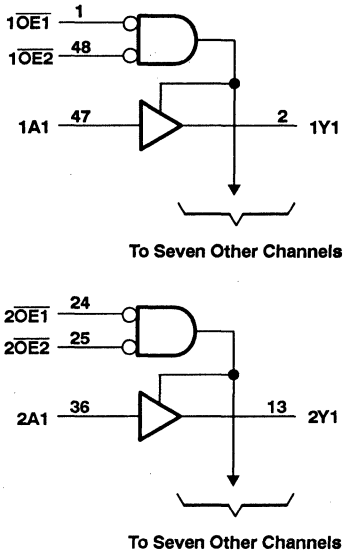
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum package power dissipation at T_A = 55°C (in still air)	0.85 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5.5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		13				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

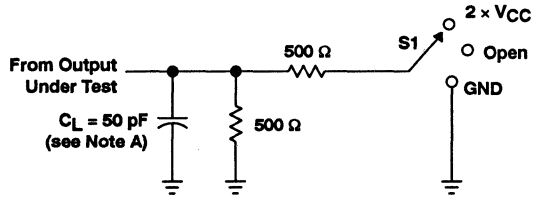
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	3.1	5.9	7.9	3.1	9	ns
t_{PHL}			2.7	6.3	8.3	2.7	9.2	
t_{PZH}	$\overline{OE}$	Y	2.8	6.5	8.9	2.8	9.7	ns
t_{PZL}			3.5	7.5	9.9	3.5	11	
t_{PHZ}	$\overline{OE}$	Y	4.5	8.5	10.3	4.5	11.3	ns
t_{PLZ}			4.9	8	9.9	4.9	10.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

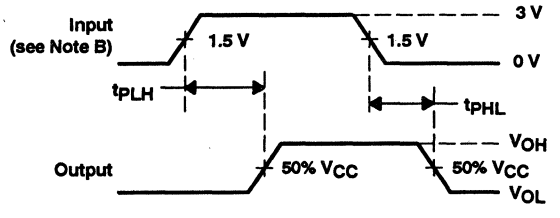
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF, f = 1 MHz	40	pF
		Outputs disabled		9.5	

PARAMETER MEASUREMENT INFORMATION

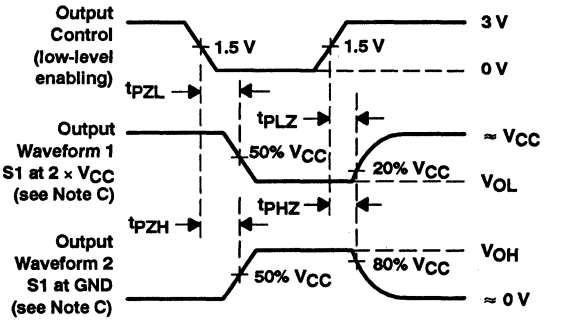


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



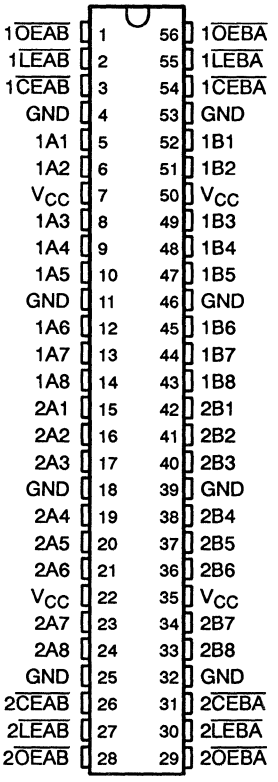
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74AC16543 is a 16-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition at $\overline{LEAB}$ puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The 74AC16543 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16543 is characterized for operation from −40°C to 85°C.

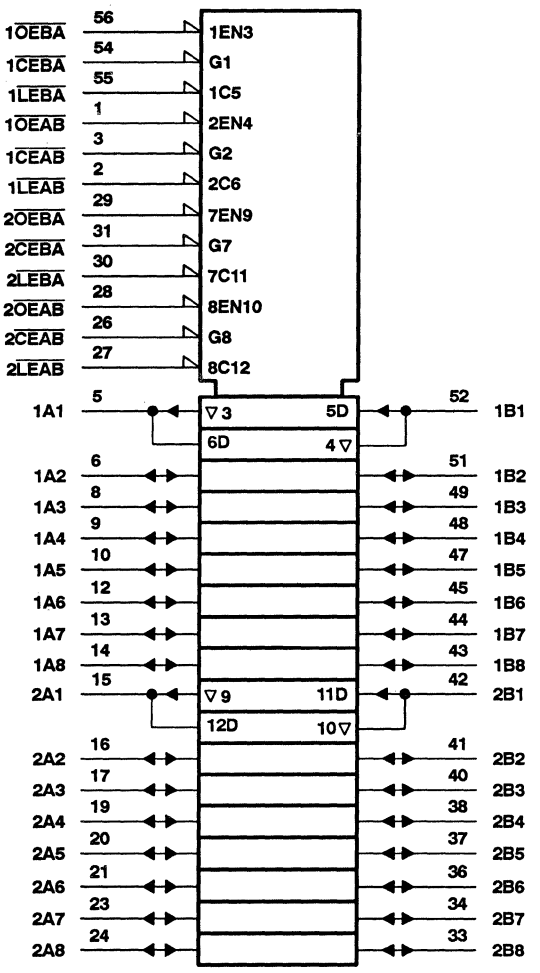
FUNCTION TABLE†
(each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

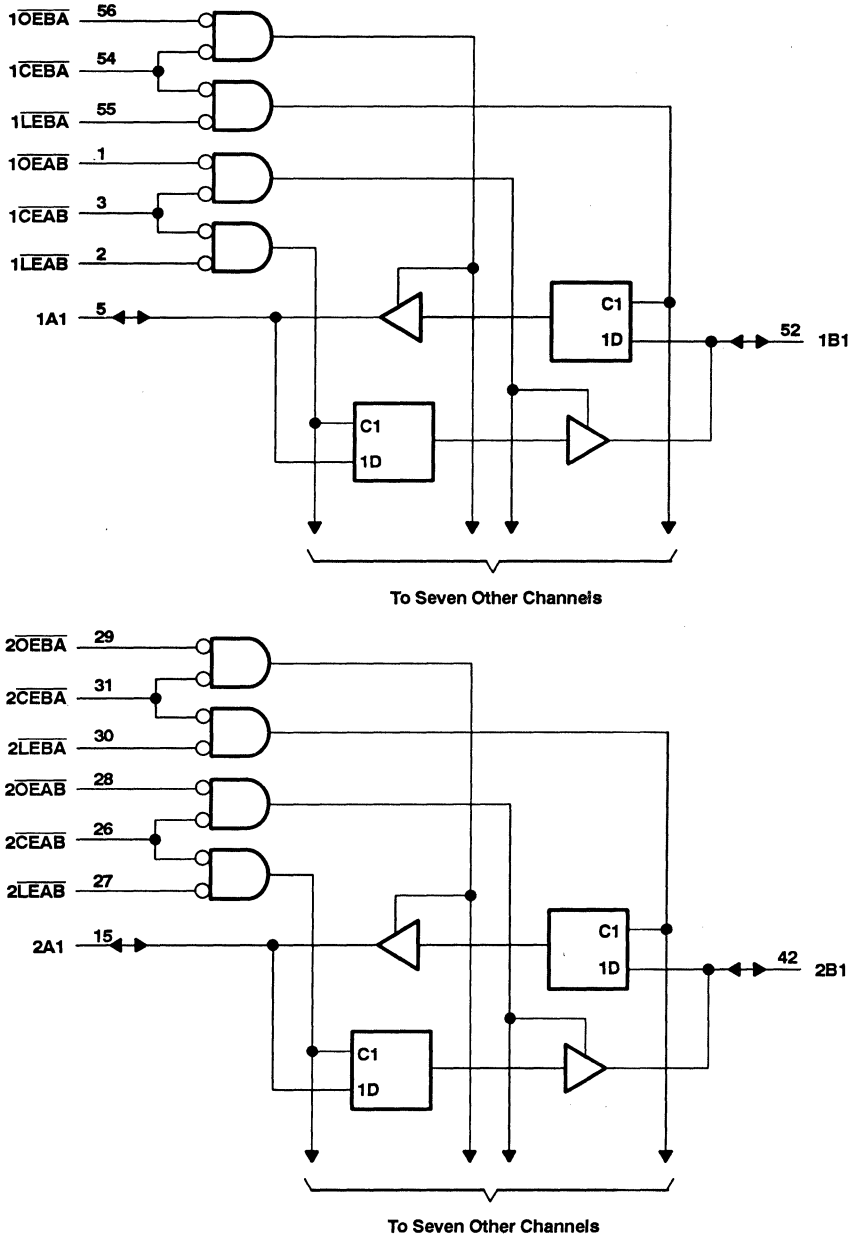
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		
		I_{OL} = –24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		11.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	5		5		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	1		1		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	3.5		3.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	4		4		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	1		1		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	3		3		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.2	8.6	12.5	3.2	13.9	ns
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	4.6	11.8	16	4.6	18	ns
t_{PHL}			4.6	11.3	15.4	4.6	16.8	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.7	10	14	3.7	15.8	ns
t_{PZL}			4.6	12.7	17.7	4.6	19.8	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.7	7.8	10.1	4.7	10.8	ns
t_{PLZ}			4.3	7.3	9.7	4.3	10.4	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.5	9.7	13.9	3.5	15.7	ns
t_{PZL}			4.5	12.5	17.6	4.5	19.7	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.8	7.5	9.6	4.8	10.2	ns
t_{PLZ}			4.1	6.8	9.2	4.1	9.8	

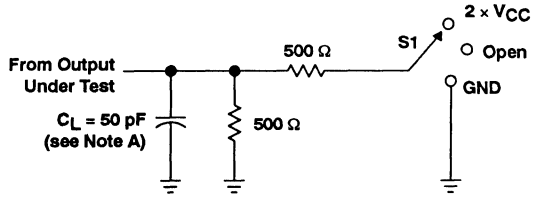
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.7	5.2	7.8	2.7	8.8	ns
t_{PHL}			2.9	5.5	8.3	2.9	9.2	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	7	10.2	3.9	11.5	ns
t_{PHL}			3.7	6.7	9.9	3.7	10.9	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3	5.8	8.7	3	9.8	ns
t_{PZL}			3.6	6.7	10.3	3.6	11.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.2	6.5	8.7	4.2	9.3	ns
t_{PLZ}			4	5.9	8.2	4	8.8	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.9	5.6	8.5	2.9	9.6	ns
t_{PZL}			3.5	6.6	10.2	3.5	11.3	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.2	6.3	8.4	4.2	8.9	ns
t_{PLZ}			3.7	5.6	7.9	3.7	8.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

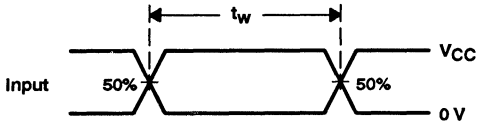
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	53	pF
		Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

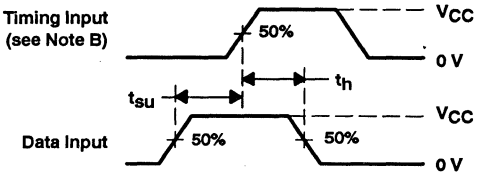


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

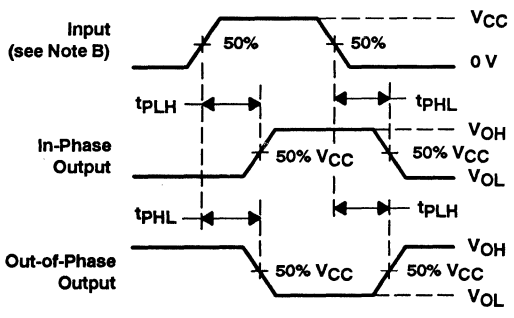
LOAD CIRCUIT



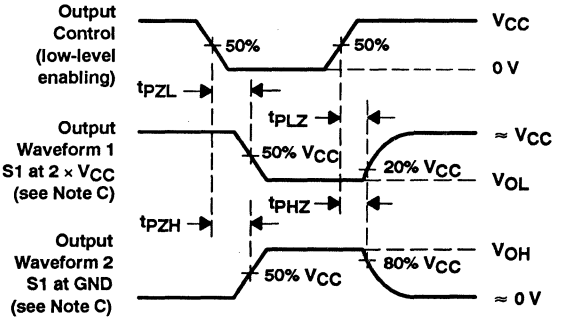
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



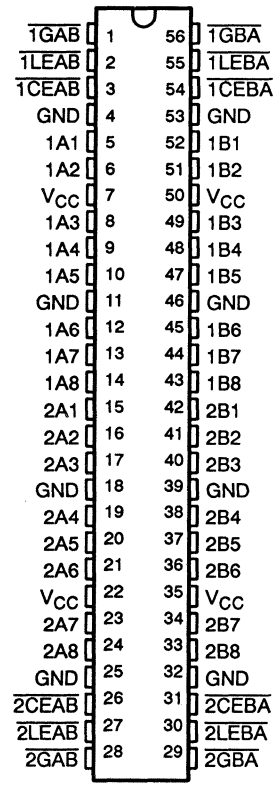
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16543 is a 16-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. The 74ACT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high-transition at $\overline{LEAB}$ puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The 74ACT16543 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 74ACT16543 is characterized for operation from – 40°C to 85°C.

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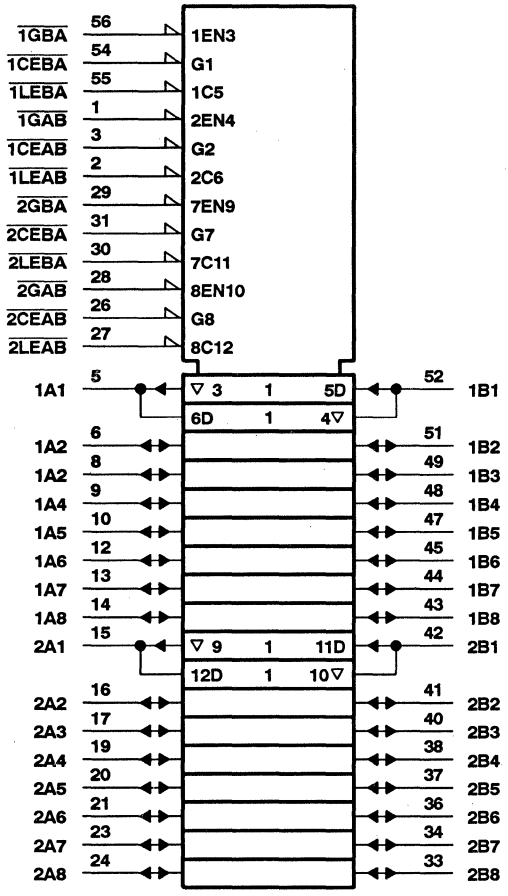
FUNCTION TABLE
(each octal register)

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H	X	Storing	
X	X	H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

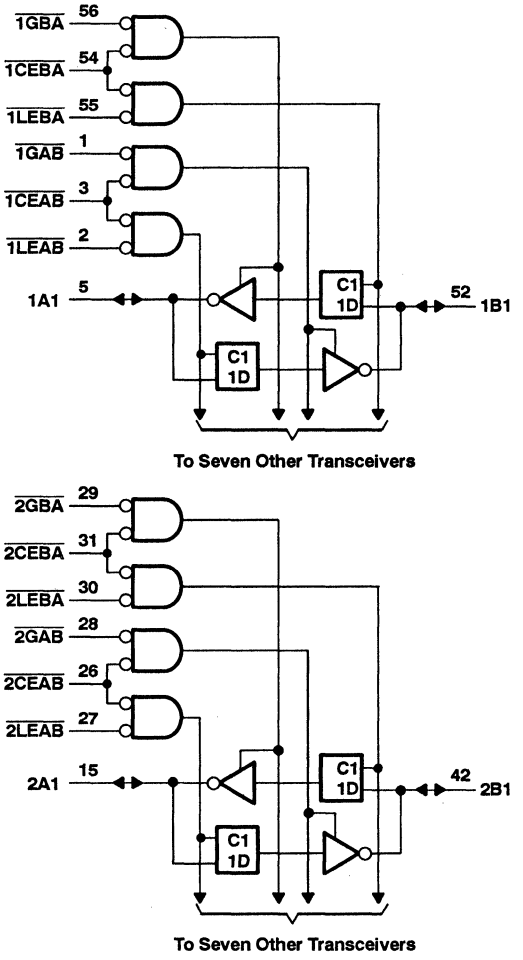
† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ are used.
‡ Data present before low-to-high transition of $\overline{LEAB}$ occurring while $\overline{CEAB}$ is low.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 2)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = – 75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			± 0.1		± 1	μA
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			± 0.5		± 5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	7.5		7.5		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$↑	2.5		2.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$↑	4		4		ns

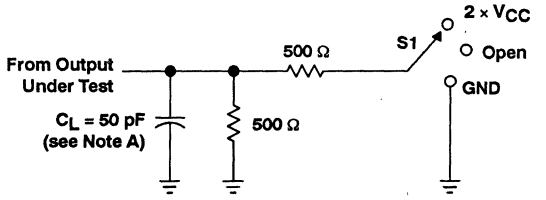
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.5	6.9	9.5	3.5	10.5	ns
t_{PHL}			3.1	7.3	10.7	3.1	11.6	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	8.6	12.3	3.9	13.8	ns
t_{PHL}			3.9	8.7	12.2	3.9	13.5	
t_{PZH}	$\overline{GBA}$ or $\overline{GAB}$	A or B	2.6	7.1	10.3	2.6	11.4	ns
t_{PZL}			3.5	8.3	11.9	3.5	13.2	
t_{PHZ}	$\overline{GBA}$ or $\overline{GAB}$	A or B	4.1	8.2	10.5	4.1	11.1	ns
t_{PLZ}			5	7.3	9.3	5	9.6	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.1	7.3	10.7	3.1	11.7	ns
t_{PZL}			3.9	8.5	12.2	3.9	13.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.6	8.5	11	4.6	11.6	ns
t_{PLZ}			5.2	7.4	9.7	5.2	10.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

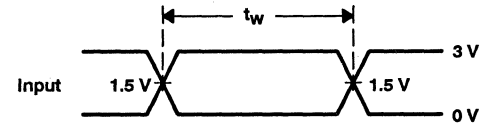
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	45	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

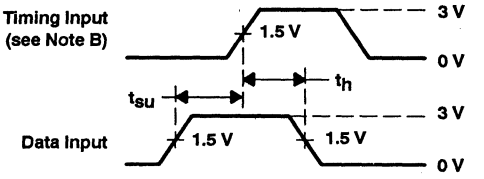


LOAD CIRCUIT

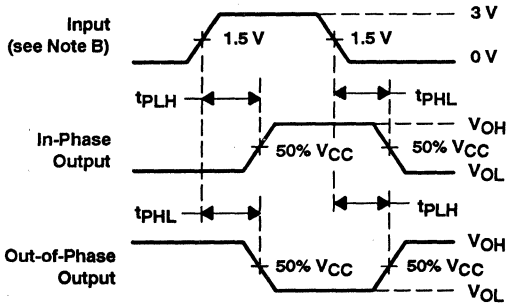
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



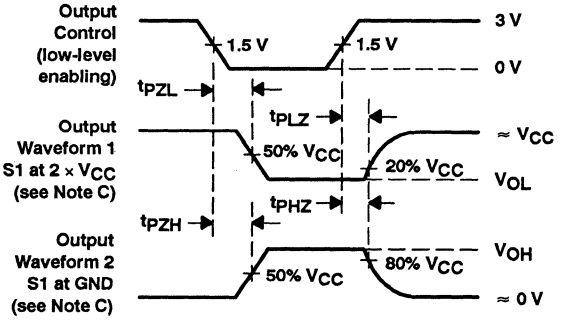
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- **Packaged in Plastic 300-Mil Shrink Small-Outline Package Using 25-Mil Center-to-Center Pin Spacings**
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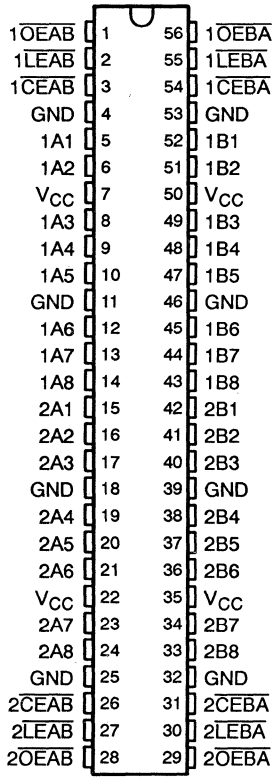
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PPACKAGE
(TOP VIEW)



description

The 74ACT16544 is a 16-bit registered transceiver that contains two sets of D-type latches for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data to B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition at $\overline{LEAB}$ puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The 74ACT16544 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16544 is characterized for operation from −40°C to 85°C.

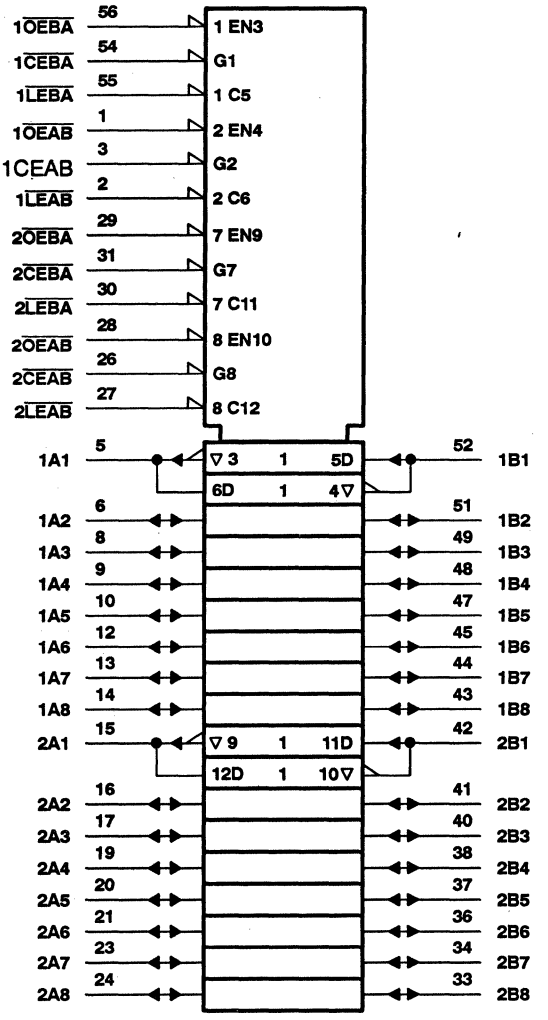
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	H
L	L	L	H	L

† A-to-B data flow is shown: B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

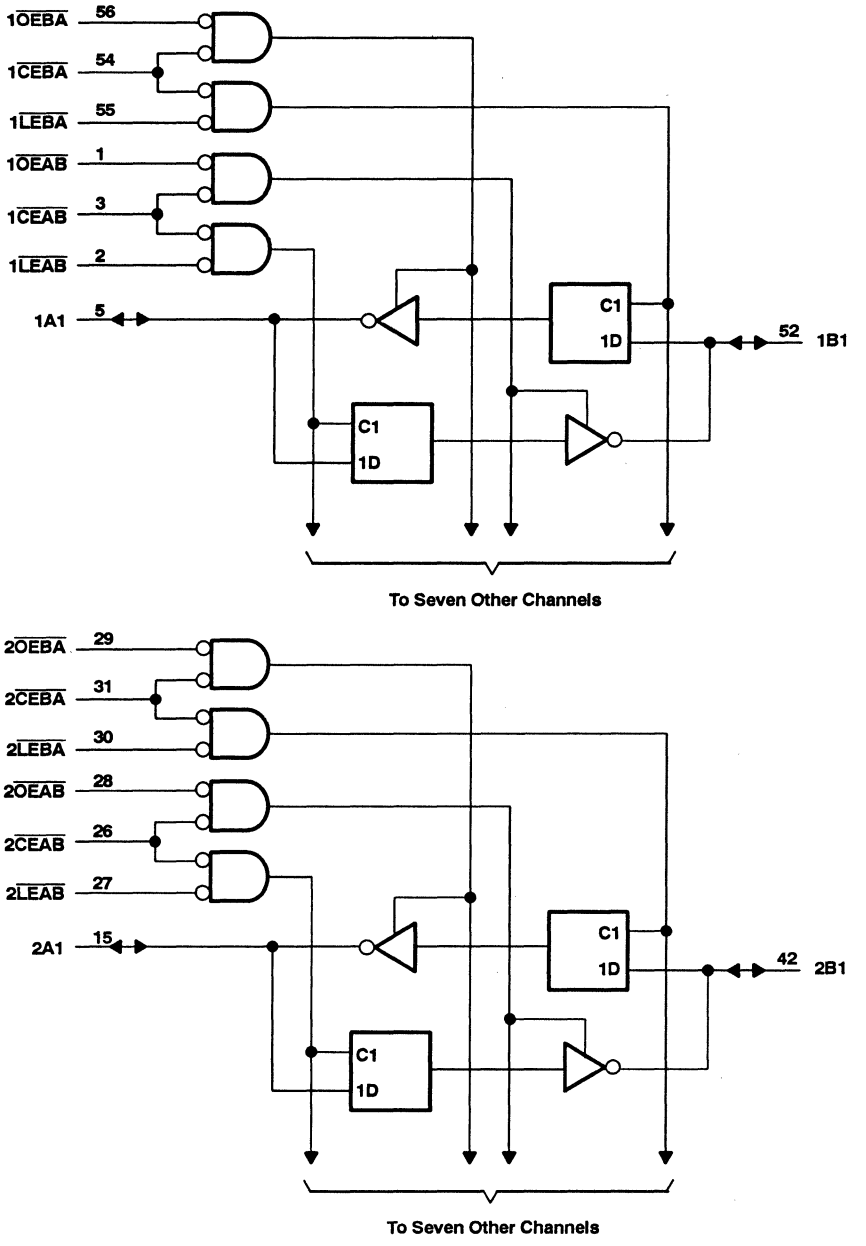
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input voltage range, V_O (see Note 1) ..... −0.5 to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (NO TAG)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{LEAB}$ or $\overline{LEBA}$ low	5.5		5.5		ns
t_{su}	Setup time	Data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	1.5		1.5		ns
		Data before $\overline{CEAB}$ or $\overline{CEBA}$ ↑	1.5		1.5		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	3		3		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$ ↑	3		3		

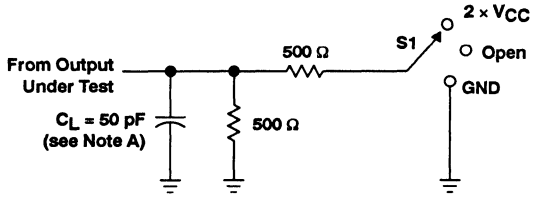
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see NO TAG)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.8	6.7	10	2.8	11.2	ns
t_{PHL}			4	7.5	10	4	11.2	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	2.7	9	13.3	2.7	14	ns
t_{PHL}			2.8	8.5	12.1	2.8	13.5	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.2	7.2	10.5	3.2	11.7	ns
t_{PZL}			3.8	8.2	12	3.8	13.6	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	5.8	8.2	10.3	5.8	11.1	ns
t_{PLZ}			5	7.4	9.4	5	10.2	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.8	6.9	10.2	2.8	11.4	ns
t_{PZL}			3.6	7.9	11.7	3.6	13.3	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	5.2	7.7	9.8	5.2	10.5	ns
t_{PLZ}			3.4	6.8	8.8	3.4	9.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

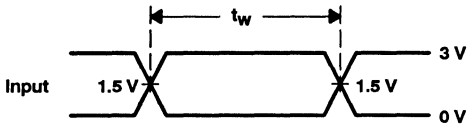
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	60	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

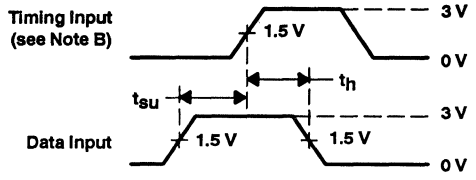


LOAD CIRCUIT

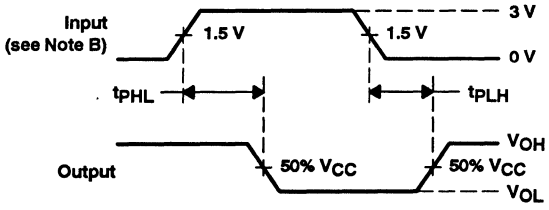
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



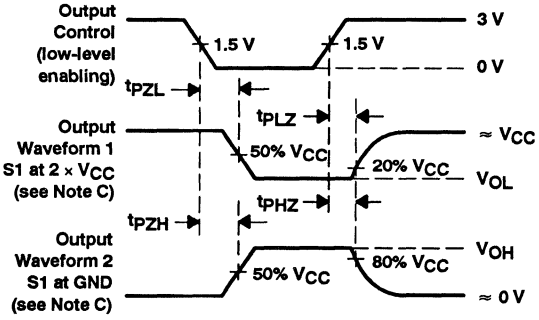
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



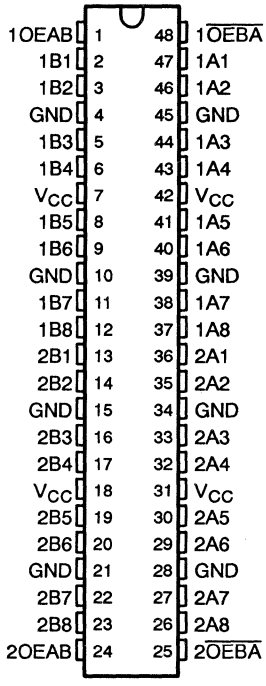
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**

DL PACKAGE
(TOP VIEW)



description

The 74AC16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the complementary output-enable (OEAB or $\overline{\text{OEBA}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the transceiver the capability to store data by simultaneous enabling of OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74AC16620 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16620 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus
H	L	Isolation
H	H	$\overline{A}$ data to B bus

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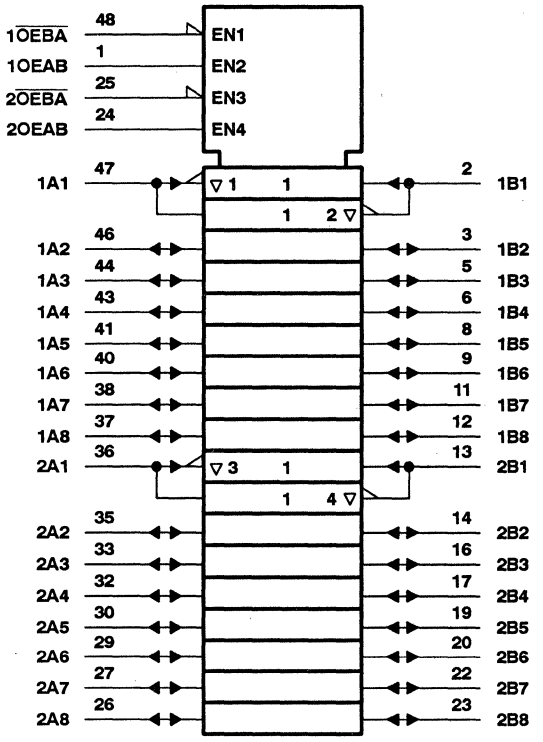
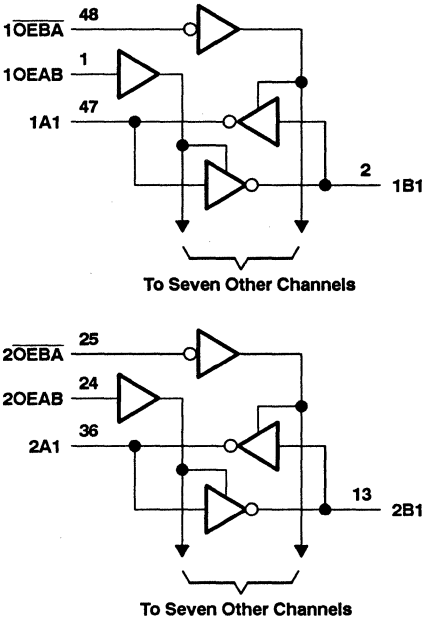
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.7	6.1	8.7	2.7	9.7	ns
t_{PHL}			3.9	7.9	10.6	3.9	11.7	
t_{PZH}	$\overline{OEBA}$	A	3.2	7.1	10	3.2	11.2	ns
t_{PZL}			4.5	11.1	13.5	4.5	15	
t_{PHZ}	$\overline{OEBA}$	A	5.3	7.4	9.5	5.3	10.2	ns
t_{PLZ}			4.6	7	9.2	4.6	9.8	
t_{PZH}	OEAB	B	3.1	6.7	9.5	3.1	10.7	ns
t_{PZL}			4.4	9.6	13	4.4	14.5	
t_{PHZ}	OEAB	B	5	7.1	9.3	5	9.8	ns
t_{PLZ}			4.4	6.8	8.9	4.4	9.4	

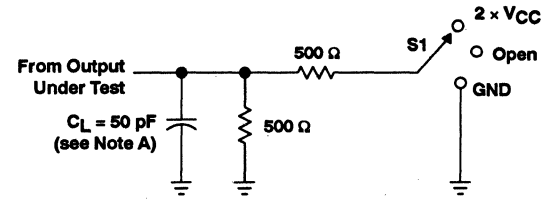
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.1	3.9	6.1	2.1	6.8	ns
t_{PHL}			3.1	4.9	7.3	3.1	8.2	
t_{PZH}	$\overline{OEBA}$	A	2.2	4.3	6.8	2.2	7.6	ns
t_{PZL}			3.3	5.5	8.4	3.3	9.4	
t_{PHZ}	$\overline{OEBA}$	A	4.9	6.6	8.6	4.9	9.2	ns
t_{PLZ}			4.1	5.8	7.8	4.1	8.3	
t_{PZH}	OEAB	B	2.2	4.2	6.5	2.2	7.3	ns
t_{PZL}			3.4	5.4	8.1	3.4	9.1	
t_{PHZ}	OEAB	B	4.6	6.4	8.5	4.6	9	ns
t_{PLZ}			4.1	5.6	7.6	4.1	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

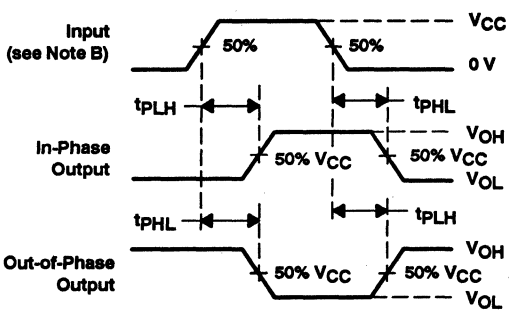
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	49	pF
		Outputs disabled		6	

PARAMETER MEASUREMENT INFORMATION

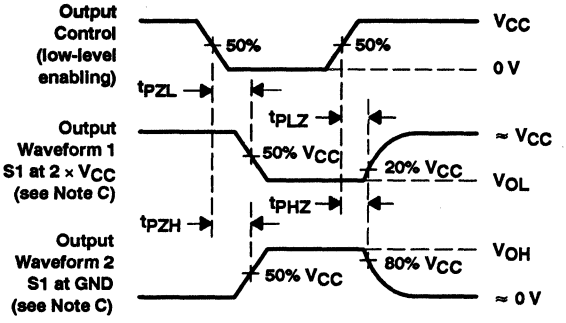


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



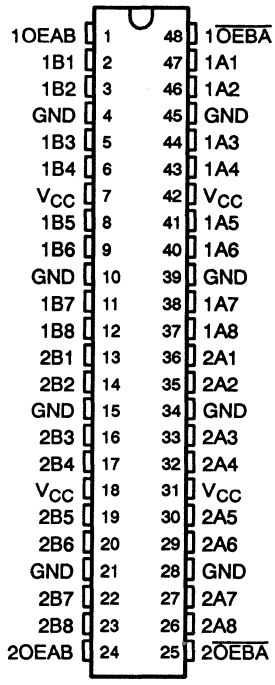
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Inverting Logic**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16620 is an inverting 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the output-enable (OEAB or $\overline{OEBA}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the transceiver the capability to store data by simultaneous enabling of OEAB and $\overline{OEBA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74ACT16620 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

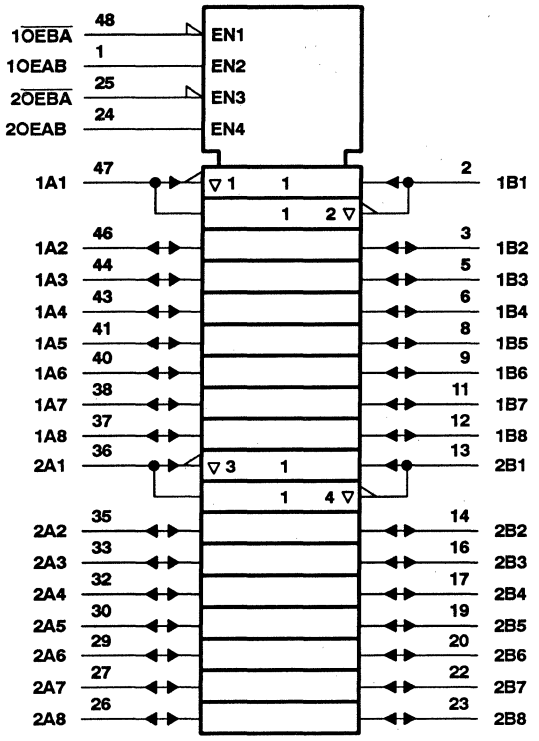
The 74ACT16620 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

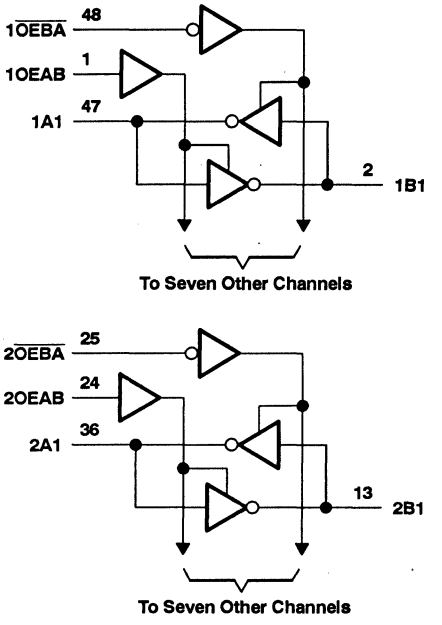
INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus
H	L	Isolation
H	H	$\overline{A}$ data to B bus

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum package power dissipation at T_A = 55°C (in still air)	0.85 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		15				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

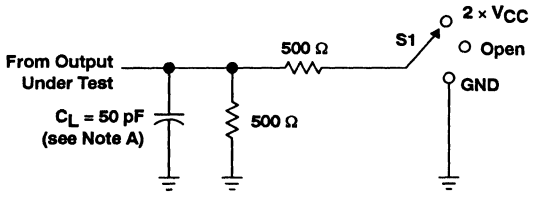
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2	5	7.7	2	8.5	ns
t_{PHL}			4	7	9.3	4	10.5	
t_{PZH}	$\overline{OEBA}$	A	2.2	5.5	8.3	2.2	9.1	ns
t_{PZL}			2.8	6.4	10	2.8	10.9	
t_{PHZ}	$\overline{OEBA}$	A	6	8.8	11	6	11.9	ns
t_{PLZ}			5.1	7.9	10	5.1	10.6	
t_{PZH}	OEAB	B	3.6	6.2	7.9	3.6	8.9	ns
t_{PZL}			4.4	7.1	9.4	4.4	10.5	
t_{PHZ}	OEAB	B	5	7.8	10.1	5	10.8	ns
t_{PLZ}			4.1	6.7	9.1	4.1	9.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

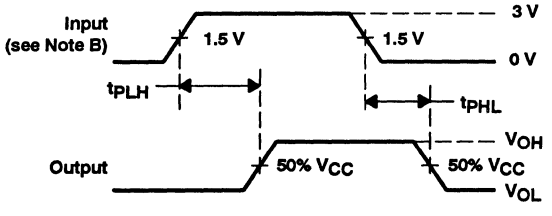
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	57	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

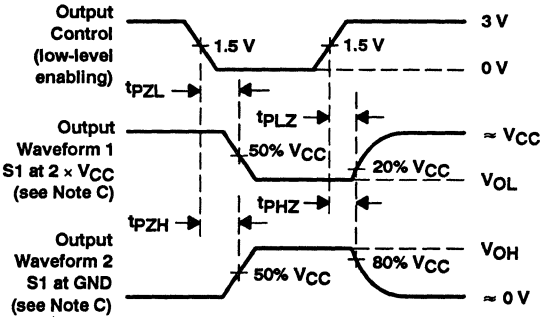


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



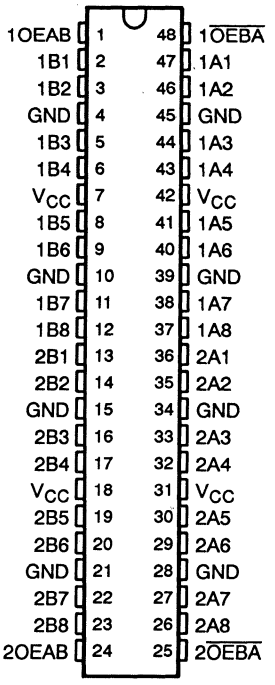
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74AC16623 is a 16-bit transceiver designed for asynchronous communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the output-enable ($\overline{OEBA}$ and OEAB) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines will remain at their last states.

The 74AC16623 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16623 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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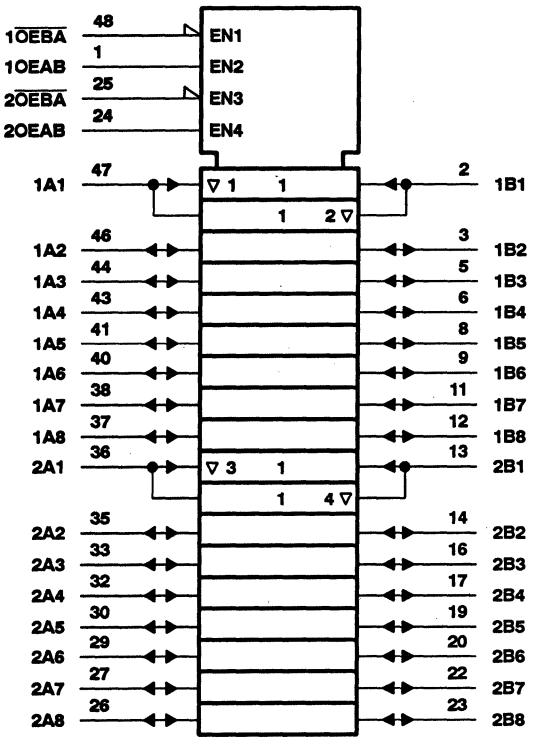
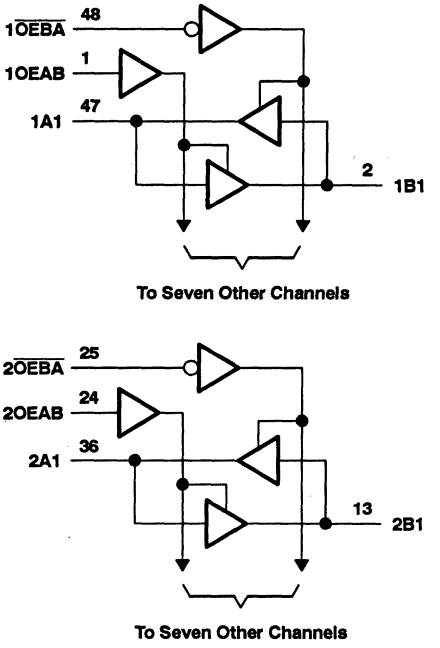
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum power package dissipation at T_A = 55°C (in still air)	0.85 W
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TA = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OL} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.7	8.1	10	2.7	11.2	ns
t_{PHL}			3.1	9.3	11.4	3.1	12.5	
t_{PZH}	$\overline{OEBA}$	A	2.7	8.3	10.3	2.7	11.5	ns
t_{PZL}			3.5	11.8	14.2	3.5	15.6	
t_{PHZ}	$\overline{OEBA}$	A	4.8	7.7	9.3	4.8	9.9	ns
t_{PLZ}			4.1	7.5	9.2	4.1	9.8	
t_{PZH}	OEAB	B	2.8	8.1	9.9	2.8	11.1	ns
t_{PZL}			3.8	10.7	14.1	3.8	15.1	
t_{PHZ}	OEAB	B	4.7	7.5	9.1	4.7	9.5	ns
t_{PLZ}			4.3	7.3	8.9	4.3	9.3	

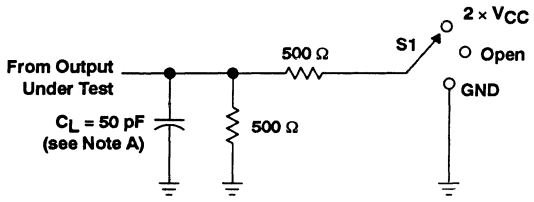
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.3	5.1	6.9	2.3	7.7	ns
t_{PHL}			2.6	6	7.8	2.6	8.6	
t_{PZH}	$\overline{OEBA}$	A	2.1	5.3	6.8	2.1	7.6	ns
t_{PZL}			2.8	6.9	8.5	2.8	9.4	
t_{PHZ}	$\overline{OEBA}$	A	4.7	6.9	8.4	4.7	8.9	ns
t_{PLZ}			4	6.3	7.7	4	8.2	
t_{PZH}	OEAB	B	2.3	5.2	6.7	2.3	7.5	ns
t_{PZL}			3	6.7	8.4	3	9.3	
t_{PHZ}	OEAB	B	4.5	6.9	8.4	4.5	8.9	ns
t_{PLZ}			4	6.2	7.6	4	7.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

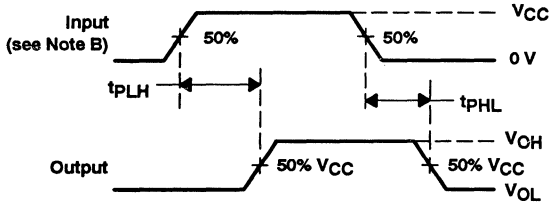
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	47	pF
		Outputs disabled		8	

PARAMETER MEASUREMENT INFORMATION

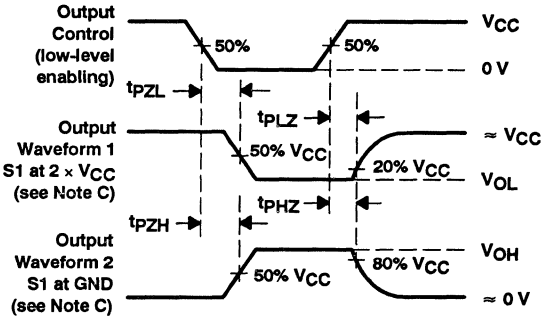


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



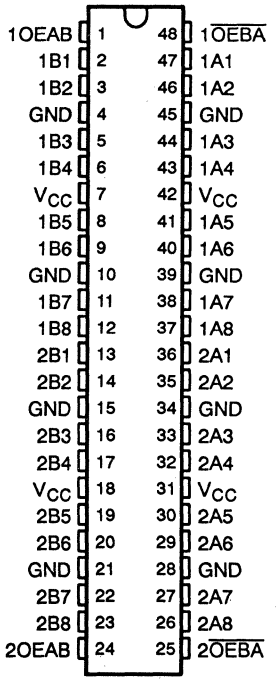
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16623 is a 16-bit transceiver designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the enable inputs ($\overline{OEBA}$ and OEAB) The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the bus transceiver the capability to store data by simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. When both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74ACT16623 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16623 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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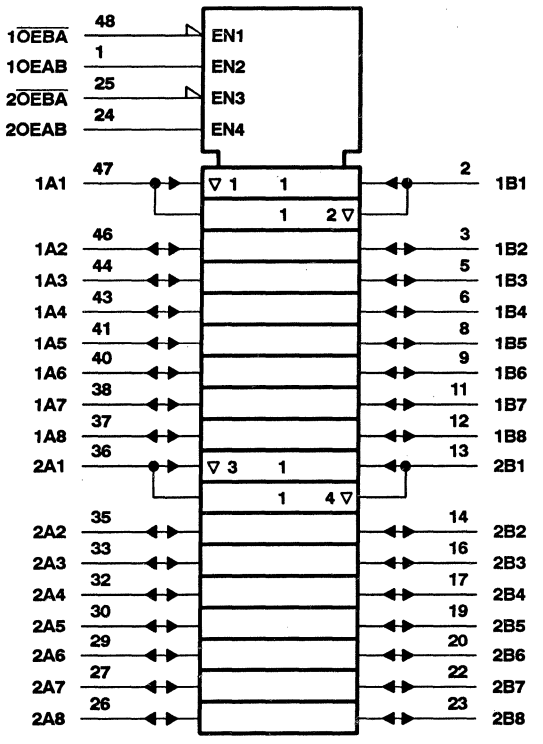
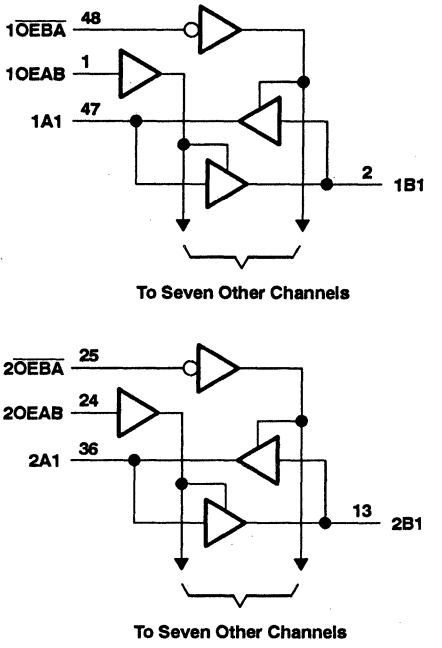
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTES: 2. Unused or floating inputs should be connected to V_{CC} through a pullup resistor of approximately 5 kΩ or greater.
3. All V_{CC} and GND pins must be connected to the proper supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TA = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −50 mA†	5.5 V						
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 50 mA†	5.5 V						
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

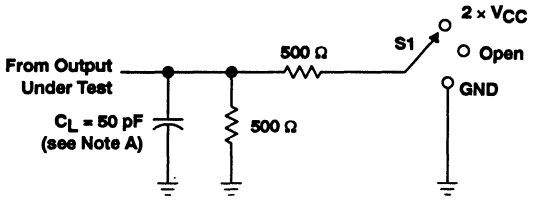
switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	4.2	7.3	9.5	4.2	10.4	ns
t_{PHL}			3.1	7.3	9.5	3.1	10.3	
t_{PZH}	$\overline{OEBA}$	A	2.7	6.8	8.8	2.7	9.5	ns
t_{PZL}			3.5	8.2	10.2	3.5	11.1	
t_{PHZ}	$\overline{OEBA}$	A	6	9.6	11.3	6	12	ns
t_{PLZ}			5.3	8.6	10.3	5.3	10.7	
t_{PZH}	OEAB	B	4.1	6.9	8.7	4.1	9.3	ns
t_{PZL}			5.1	7.9	9.7	5.1	10.6	
t_{PHZ}	OEAB	B	5.1	8.2	10.2	5.1	10.4	ns
t_{PLZ}			4.4	7.4	9.3	4.4	9.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

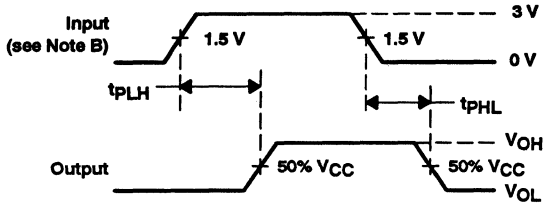
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	56	pF
		Outputs disabled		11	

PARAMETER MEASUREMENT INFORMATION

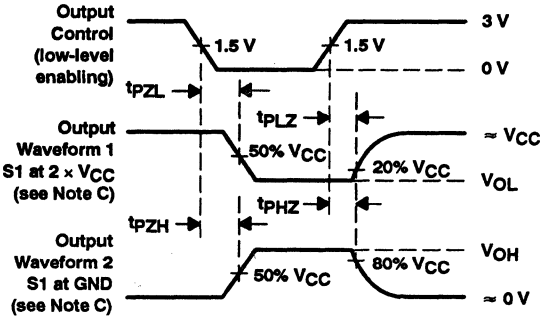


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



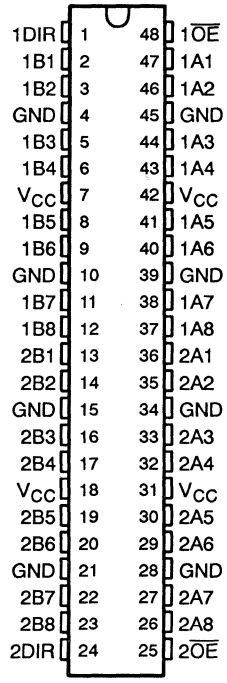
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**

DL PACKAGE
(TOP VIEW)



description

The 74AC16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable (1$\overline{OE}$ and 2$\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

The 74AC16640 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

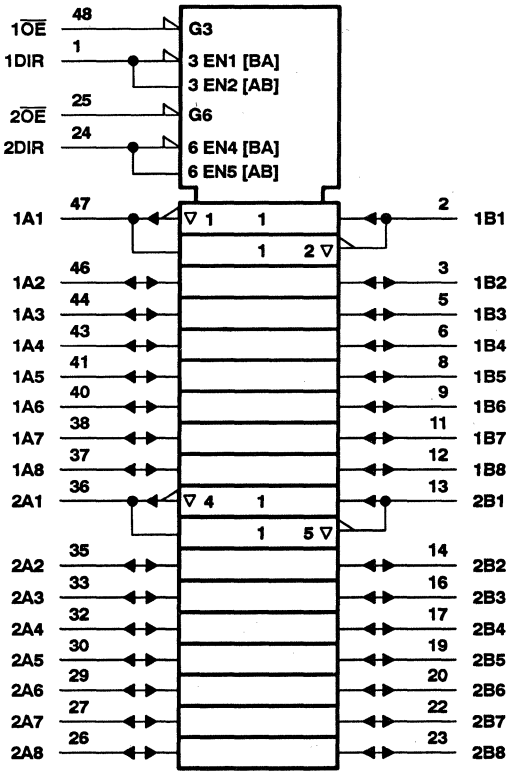
The 74AC16640 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

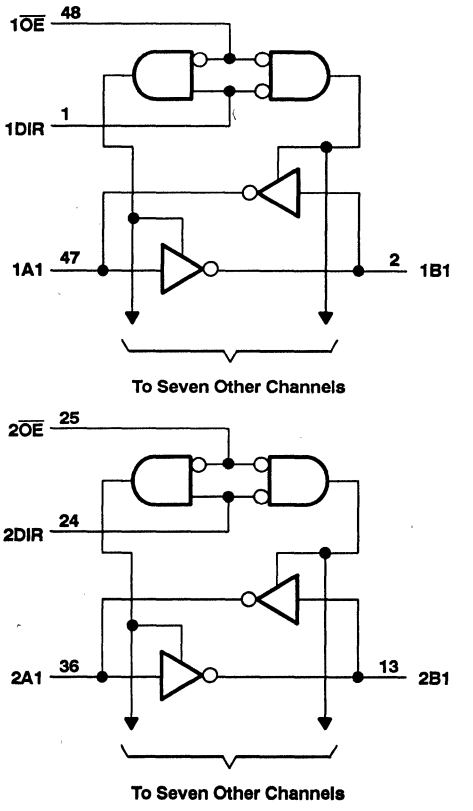
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I_{OH} = −4 mA	3 V	2.58			2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.2	6.9	9.1	2.2	10	ns
t_{PHL}			3	8.5	11	3	11.9	
t_{PZH}	$\overline{OE}$	A or B	3	8.2	11	3	12.3	ns
t_{PZL}			3.9	10.9	14	3.9	15.5	
t_{PHZ}	$\overline{OE}$	A or B	5.1	8.3	10.6	5.1	11.2	ns
t_{PLZ}			4.3	7.8	10.1	4.3	10.6	

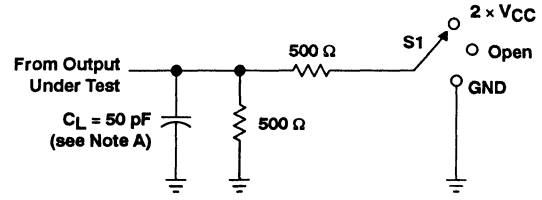
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.8	4.7		1.8	7.3	ns
t_{PHL}			2.6	5.7		2.6	8.6	
t_{PZH}	$\overline{OE}$	A or B	2.4	5.6		2.4	8	ns
t_{PZL}			3	6.6		3	9.9	
t_{PHZ}	$\overline{OE}$	A or B	5	7.5		5	9.9	ns
t_{PLZ}			4.1	6.5		4.1	9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

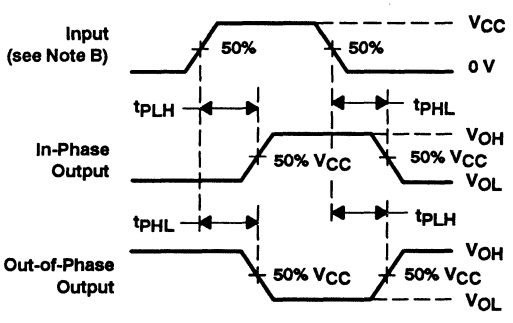
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		8	

PARAMETER MEASUREMENT INFORMATION

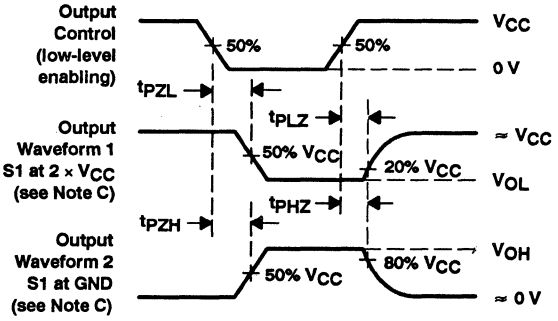


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



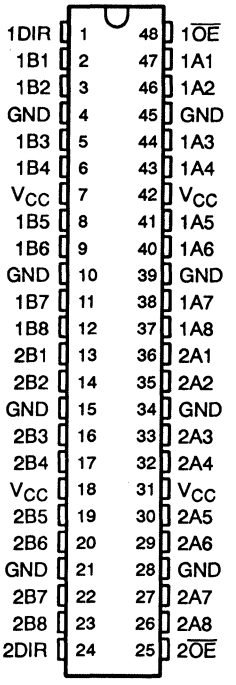
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16640 is an inverting 16-bit transceiver designed for asynchronous communication between data buses.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (1DIR and 2DIR) inputs. The output-enable (1$\overline{OE}$ and 2$\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

The 74ACT16640 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

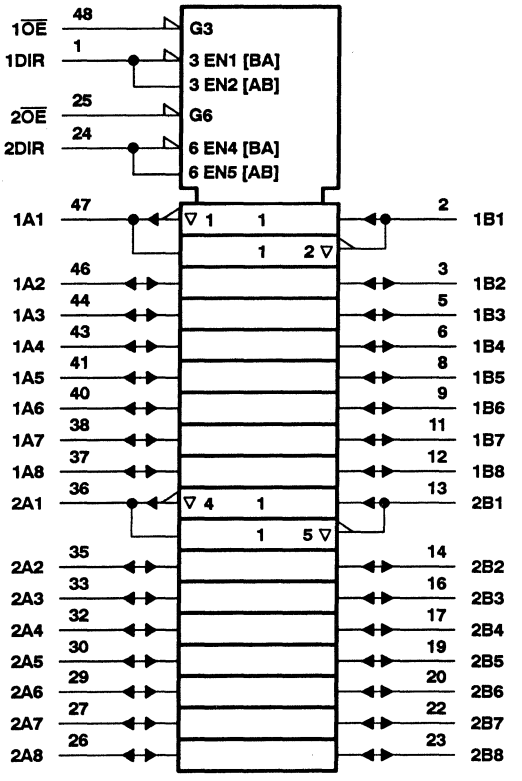
The 74ACT16640 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

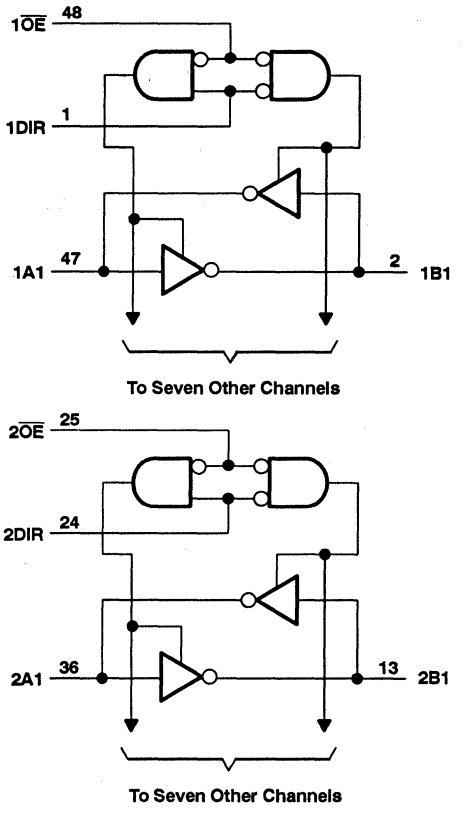
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

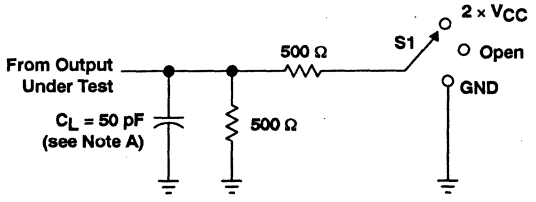
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see NO TAG)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	2.2	6	8.3	2.2	9.1	ns
t_{PHL}			4.1	7.6	9.3	4.1	10.5	
t_{PZH}	$\overline{OE}$	A or B	2.7	6.9	8.9	2.7	9.8	ns
t_{PZL}			3.5	8.2	10.4	3.5	11.5	
t_{PHZ}	$\overline{OE}$	A or B	6.1	9.4	11.4	6.1	12.5	ns
t_{PLZ}			5.5	8.7	10.3	5.5	11	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

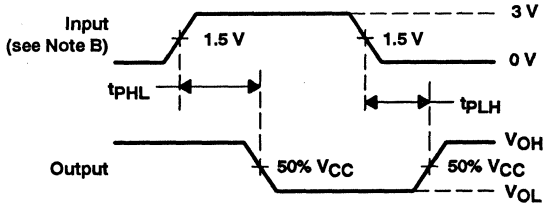
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

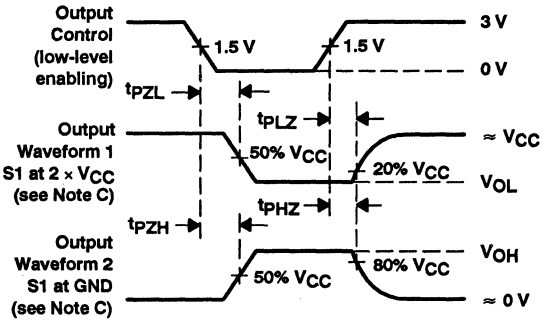


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
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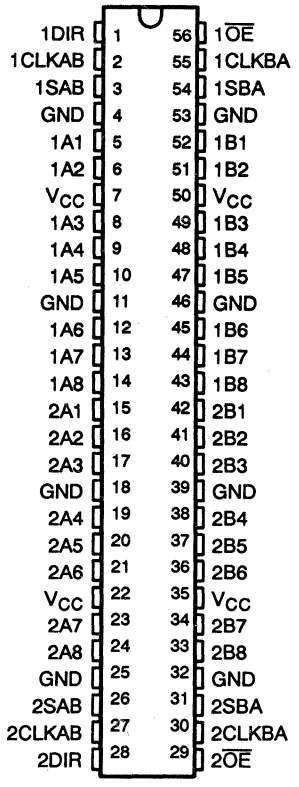
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16646 . . . WD PACKAGE
74ACT16646 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16646 is a 16-bit bus transceiver, which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CLKAB or CLKBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receives data when $\overline{OE}$ is active (low). In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74AC16646 is packaged in the TI shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

The 54AC16646 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16646 is characterized for operation from −40°C to 85°C.

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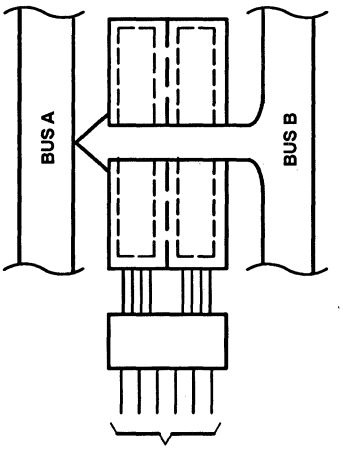
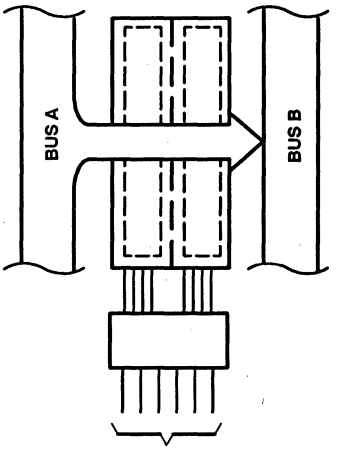


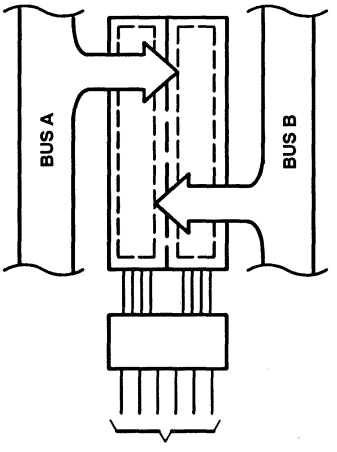
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



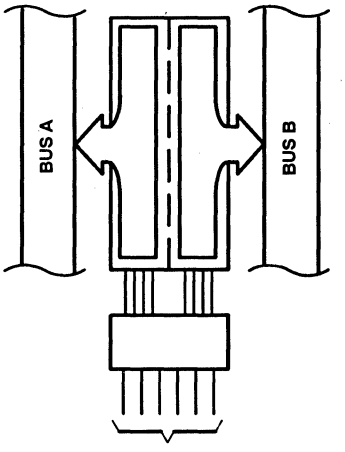
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM A, B OR A AND B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A OR B

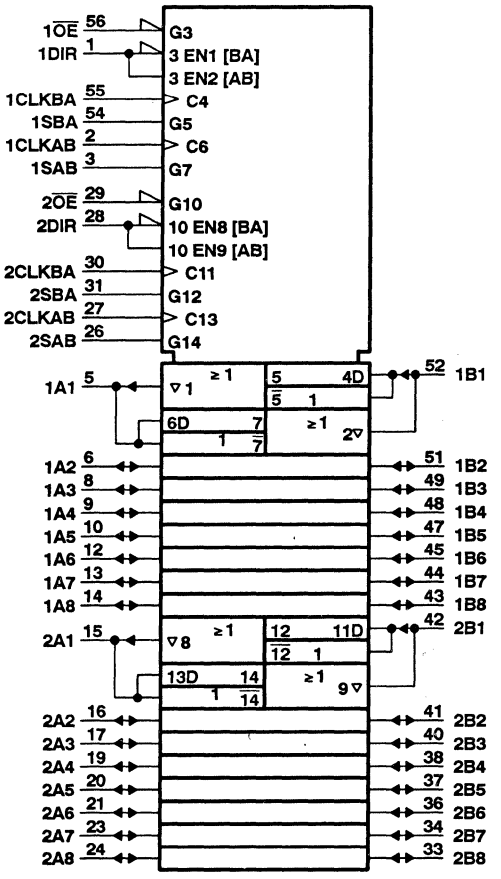
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

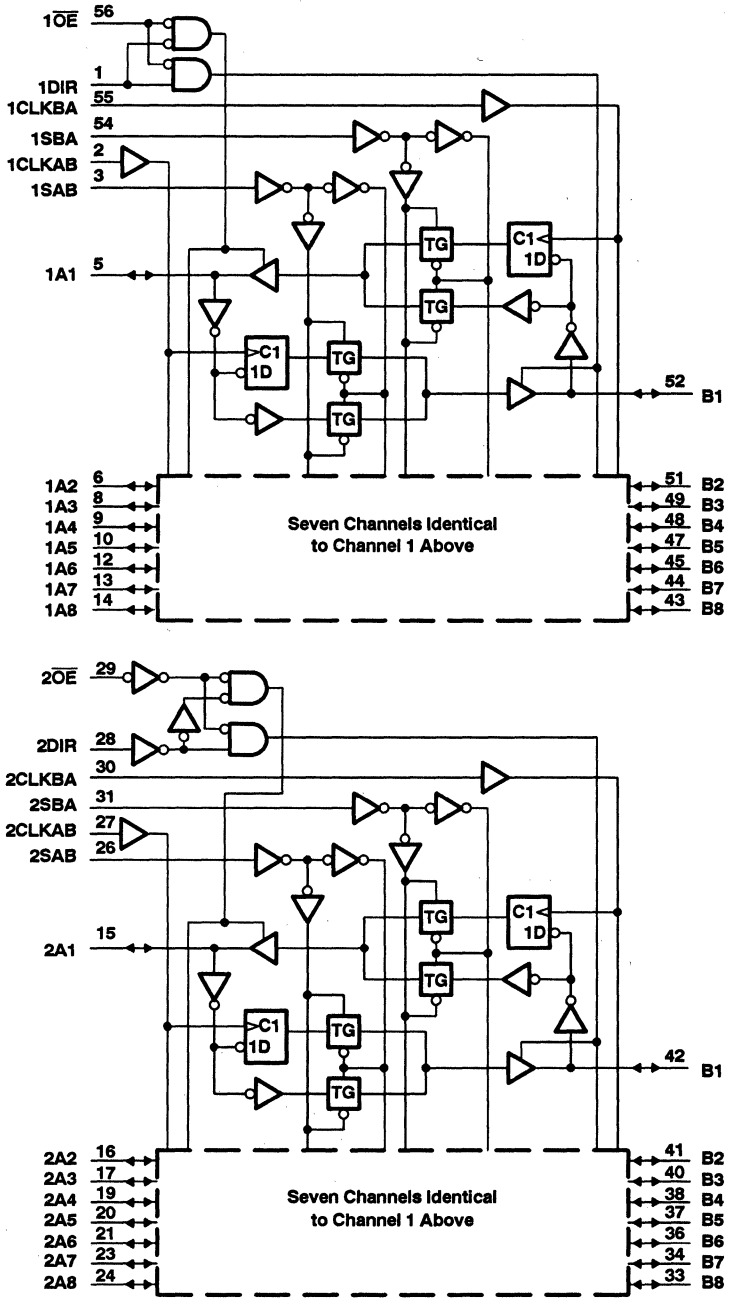
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC16646			74AC16646			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage				V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4			–4	mA
		V_{CC} = 4.5 V			–24			–24	
		V_{CC} = 5.5 V			–24			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	V_I = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_o	V_I = V_{CC} or GND	5 V		16						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16646		74AC16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	65	0	65	0	65	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	7				7		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	6.5				6.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16646		74AC16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	75	0	75	0	75	MHz
t_w	Pulse duration, CLKAB or CLkBA high or low	6.5				6.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	5				5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			65			65		65		MHz
t_{PLH}	A or B	B or A	3.4	9.3	13.2	3.4	15.7	3.4	14.8	ns
t_{PHL}			3.6	10	13.4	3.6	15.1	3.6	4.5	
t_{PZH}	$\overline{OE}$	A or B	3.8	10.5		3.8	17.6	3.8	16.4	ns
t_{PZL}			4.8	13.9		4.8	22.1	4.8	20.9	
t_{PHZ}	$\overline{OE}$	A or B	4.4	7.6		4.4	11	4.4	10.7	ns
t_{PLZ}			4	7		4	10.4	4	10.1	
t_{PLH}	CLKBA or CLKAB	A or B	4.7	12.1		4.7	19.9	4.7	18.7	ns
t_{PHL}			4.8	12.2		4.8	18.8	4.8	18	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4.7	12		4.7	19.9	4.7	18.5	ns
t_{PHL}			4.5	11.4		4.5	17.2	4.5	16.4	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4	10.5		4	17.3	4	16.3	ns
t_{PHL}			5.2	13.3		5.2	20.3	5.2	19.3	
t_{PZH}	DIR	A or B	3.6	10.3		3.6	17.9	3.6	16.8	ns
t_{PZL}			4.7	13.5		4.7	22.1	4.7	20.8	
t_{PHZ}	DIR	A or B	4.6	7.8		4.6	11.6	4.6	11.2	ns
t_{PLZ}			3.9	7		3.9	11	3.9	10.6	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

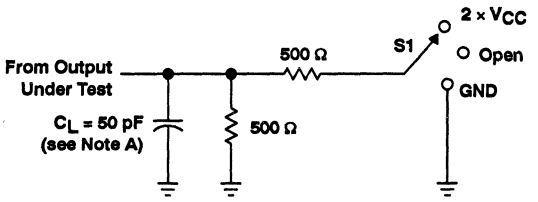
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16646		74AC16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			75			75		75		MHz
t_{PLH}	A or B	B or A	2.9	5.5	8.5	2.9	10.1	2.9	9.5	ns
t_{PHL}			2.9	5.7	8.9	2.9	10.1	2.9	9.7	
t_{PZH}	$\overline{OE}$	A or B	3.1	6.1	9.4	3.1	11.1	3.1	10.5	ns
t_{PZL}			4.1	7.3	11	4.1	12.9	4.1	12.2	
t_{PHZ}	$\overline{OE}$	A or B	4	6.1	8.4	4	9.1	4	8.9	ns
t_{PLZ}			3.8	5.7	8	3.8	8.9	3.8	8.6	
t_{PLH}	CLKBA or CLKAB	A or B	3.9	7	10.8	3.9	12.8	3.9	12.1	ns
t_{PHL}			3.9	7.1	10.8	3.9	12.5	3.9	11.9	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	4	7.4	11.1	4	13.4	4	12.5	ns
t_{PHL}			3.6	6.7	10.2	3.6	11.8	3.6	11.2	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	3.3	6.1	9.5	3.3	11.2	3.3	10.6	ns
t_{PHL}			4.3	8	11.7	4.3	13.9	4.3	13.1	
t_{PZH}	DIR	A or B	3	5.9	9.6	3	11.6	3	10.9	ns
t_{PZL}			3.6	7	11.1	3.6	12.9	3.6	12.2	
t_{PHZ}	DIR	A or B	4	6.2	8.8	4	9.6	3	9.4	ns
t_{PLZ}			3.7	5.7	8.2	3.7	9	3.7	8.8	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

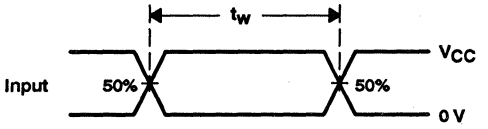
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	62	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

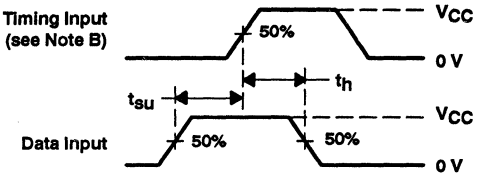


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



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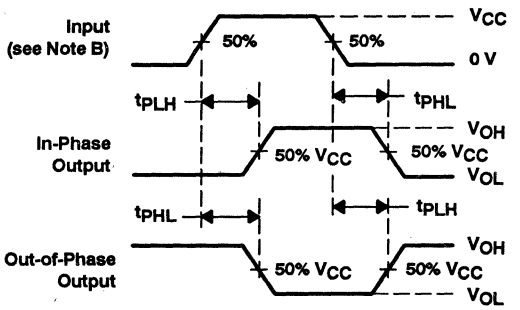
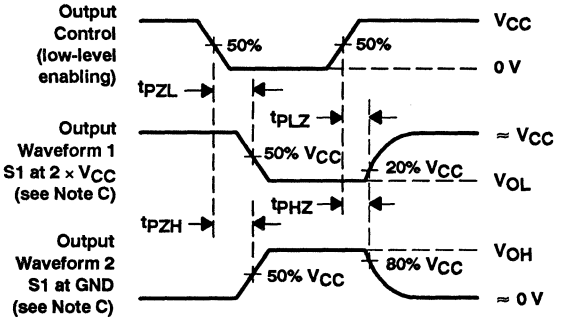


VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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- **Packaged in Shrink Small-Outline 300-mil Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
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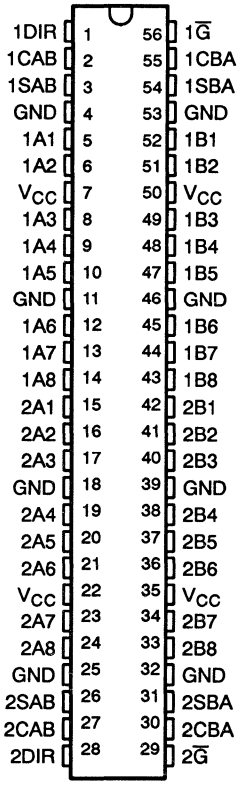
54ACT16646 . . . WD PACKAGE
74ACT16646 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16646 is a 16-bit bus transceiver which consists of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock input (CAB or CBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the bus transceivers and registers.

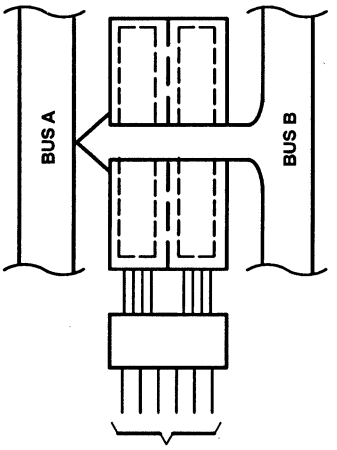
Output enable ($\overline{G}$) and direction (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus receives data when $\overline{G}$ is low. In the isolation mode ($\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT16646 is packaged in TI's shrink small-outline package (SSOP), which provides twice the functionality of standard small-outline packages in the same PCB area.

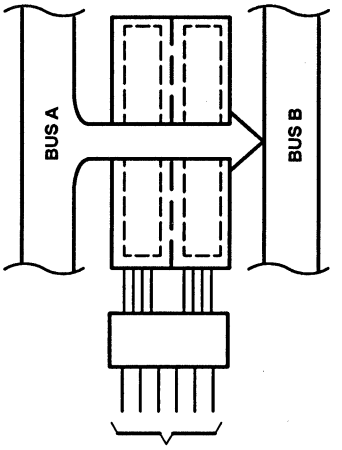
The 54ACT16646 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74ACT16646 is characterized for operation from – 40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.



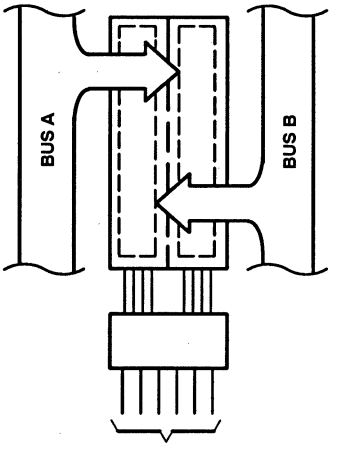
$\overline{G}$	$\overline{DIR}$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



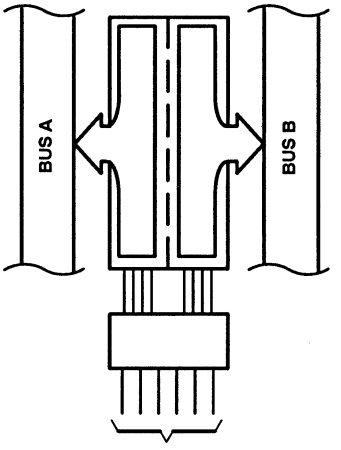
$\overline{G}$	$\overline{DIR}$	CAB	CBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



$\overline{G}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

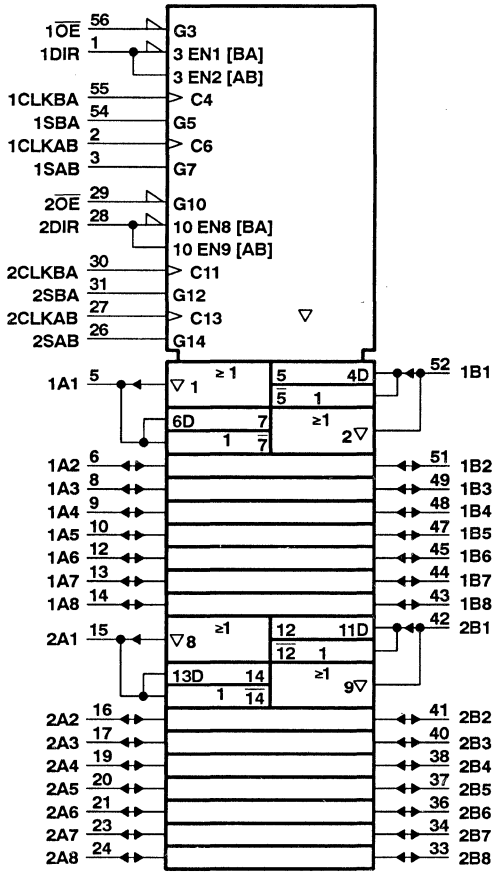
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus

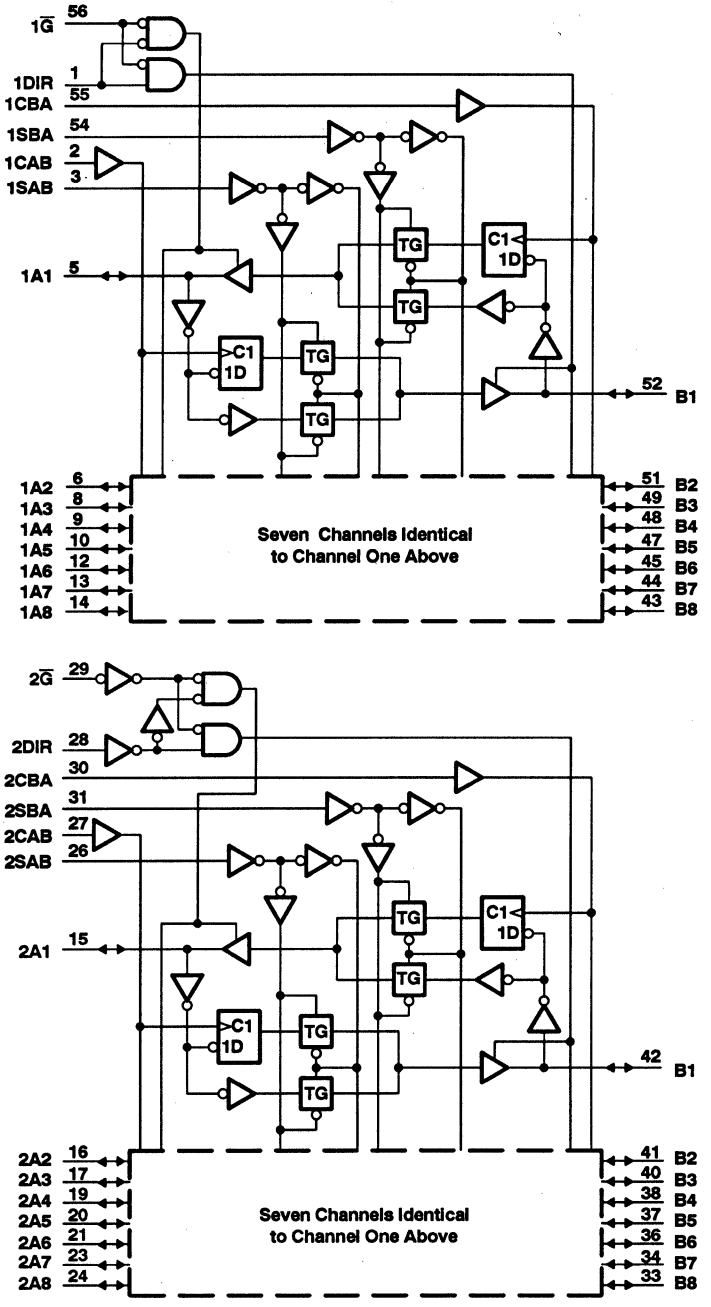
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND ..... ± 400 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		54ACT16646		74ACT16646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 2)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16646		74ACT16646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = – 50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

			T_A = 25°C		54ACT16646		74ACT16646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration, CAB or CBA high or low		5.5		5.5		5.5		ns
t_{su}	Setup time, A before CAB↑ or B before CBA↑	Data high	4		4		4		ns
		Data low	6		6		6		
t_h	Hold time, A before CAB↑ or B before CBA↑		1.5		1.5		1.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

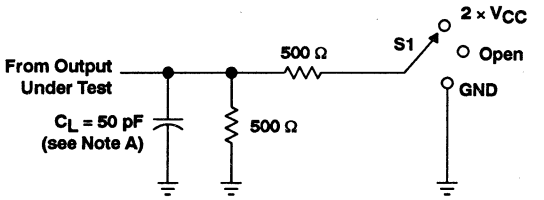
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16646		74ACT16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	3.9	7.5	9.4	3.9	11.5	3.9	10.6	ns
t_{PHL}			3.4	7.6	10.6	3.4	12.2	3.4	11.4	
t_{PZH}	$\overline{G}$	A or B	3.2	7.7	10.8	3.2	12.9	3.2	11.9	ns
t_{PZL}			4.2	9	12.2	4.2	14.6	4.2	13.5	
t_{PHZ}	$\overline{G}$	A or B	5.3	7.7	9.6	5.3	10.4	5.3	10.2	ns
t_{PLZL}			4.9	7.3	9.2	4.9	10.3	4.9	9.9	
t_{PLH}	CBA or CAB	A or B	4.9	8.9	11.1	4.9	13.1	4.9	12.2	ns
t_{PHL}			5.1	9	11	5.1	13.1	5.1	12.3	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	5.2	10.3	13.8	5.2	17.2	5.2	15.6	ns
t_{PHL}			4.9	8.2	10.6	4.9	12.5	4.9	11.7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	4.3	7.8	9.9	4.3	12.1	4.3	11.1	ns
t_{PHL}			5.9	11.2	14.9	5.9	18.2	5.9	16.7	
t_{PZH}	DIR	A or B	4.5	9.5	13.6	4.5	16.2	4.5	15.2	ns
t_{PZL}			4.3	9.2	11.8	4.3	14.2	4.3	13.1	
t_{PHZ}	DIR	A or B	4.5	7.9	10.2	4.5	11.2	4.5	10.8	ns
t_{PLZ}			4.4	7.5	9.8	4.4	10.8	4.4	10.4	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

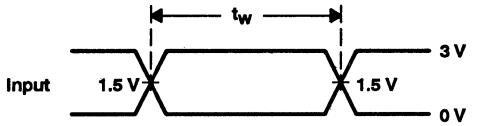
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	58	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

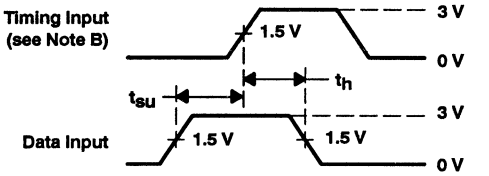


LOAD CIRCUIT

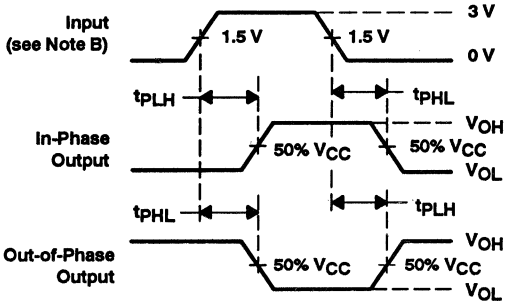
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



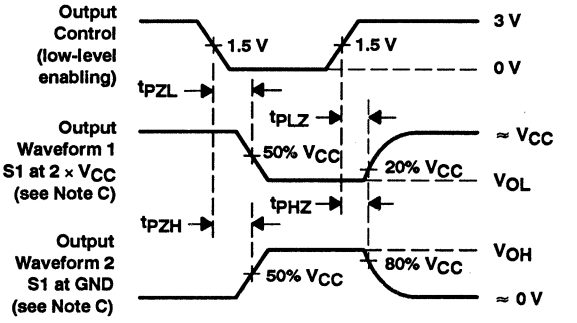
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



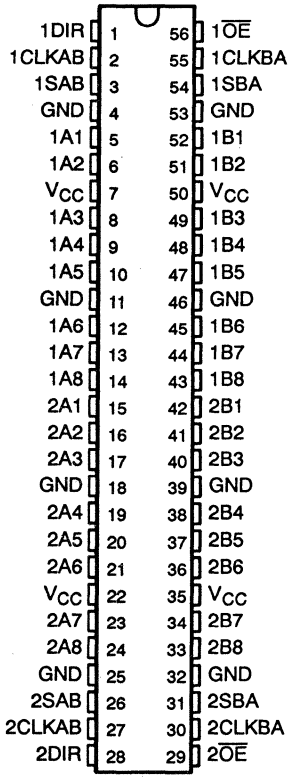
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged In Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Inverting Data Path**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16648 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CLKAB or CLKBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74ACT16648.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The 74ACT16648 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16648 is characterized for operation from −40°C to 85°C.

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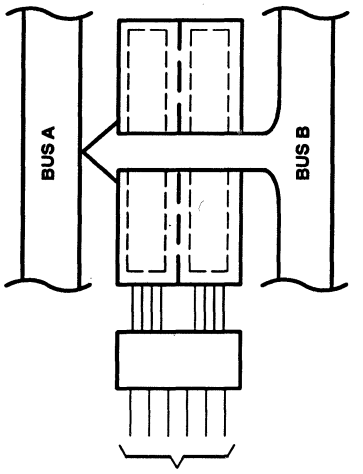
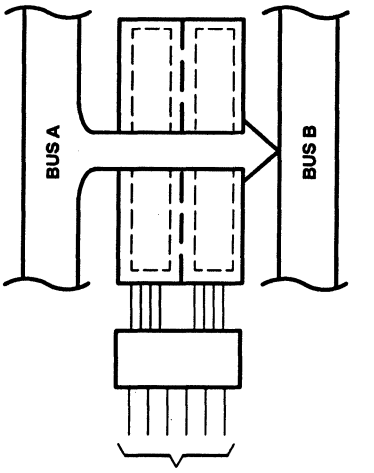


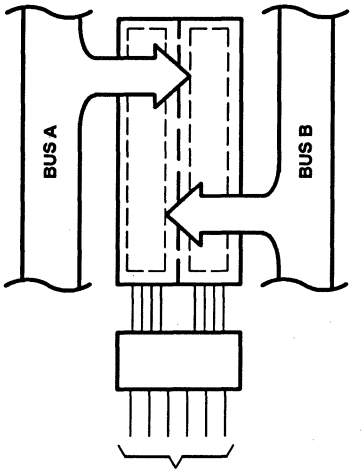
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



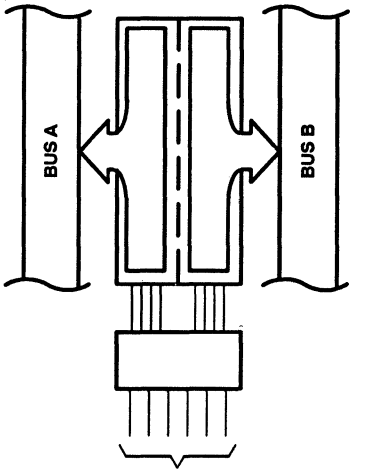
56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

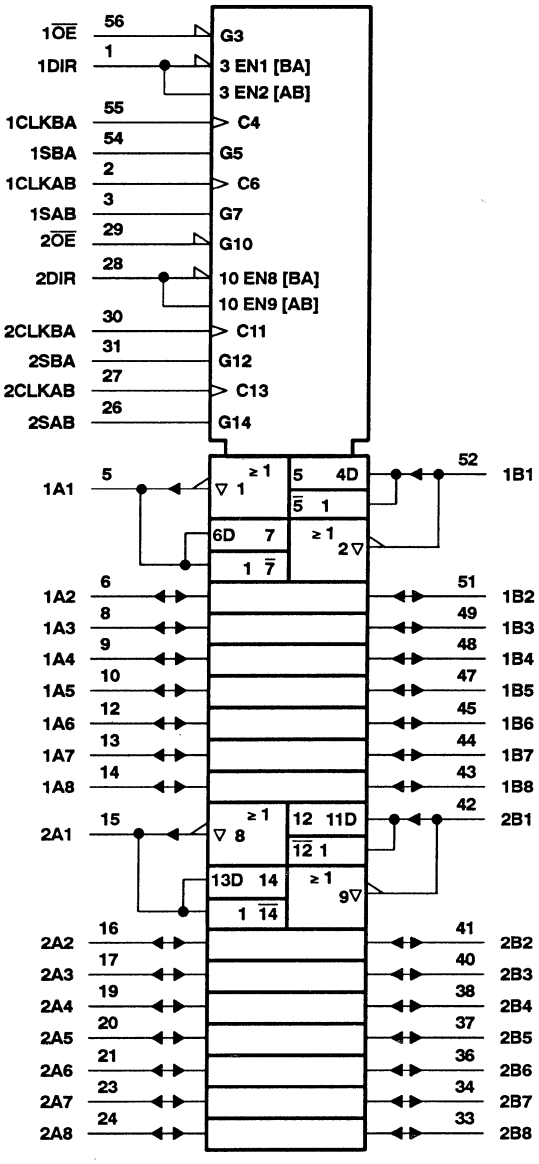


56 $\overline{OE}$	1 DIR	2 CLKAB	55 CLKBA	3 SAB	54 SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

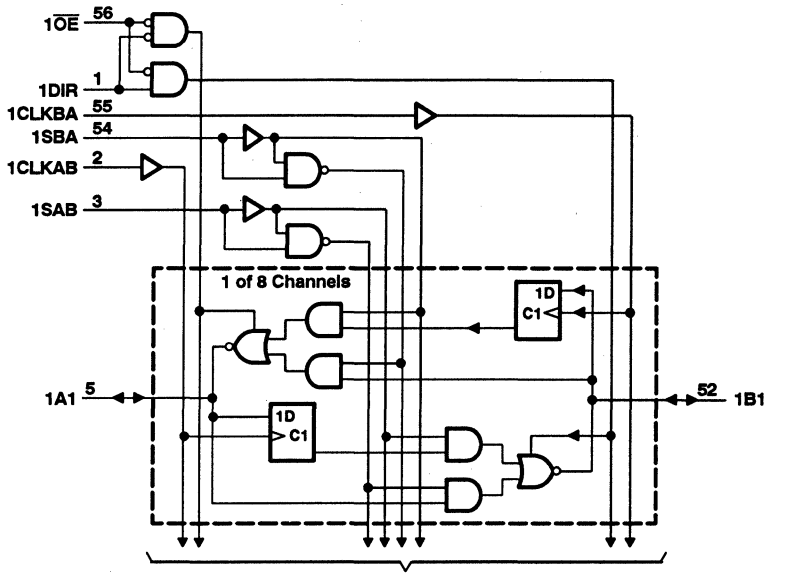
Figure 1. Bus-Management Functions

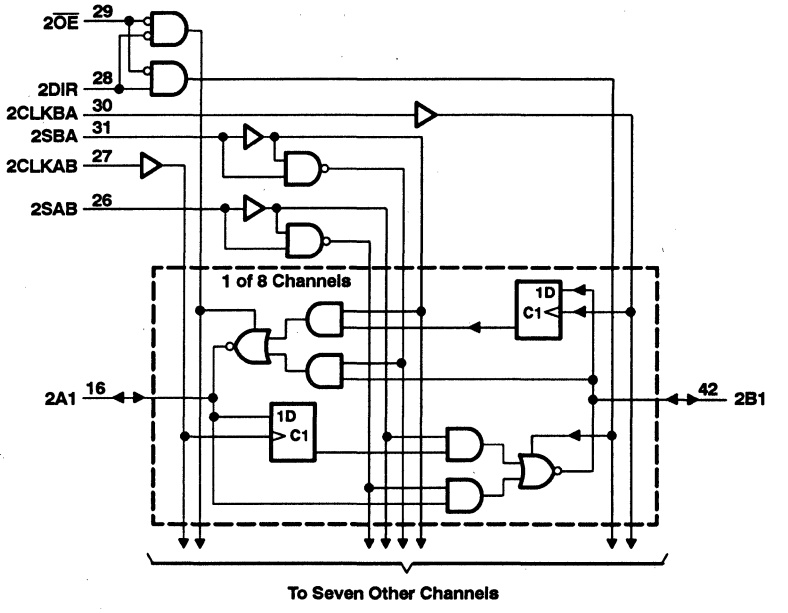
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





FUNCTION TABLE
(each 8-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data output functions may be enabled or disabled by a variety of level combinations at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	75	0	75	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	6.5		6.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

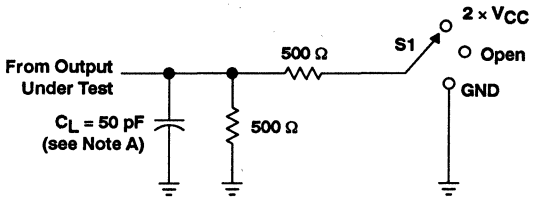
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75			75		MHz
t_{PLH}	A or B	B or A	2.4	7.2	9.8	2.4	11	ns
t_{PHL}			3.8	7.7	10.1	3.8	11.2	
t_{PZH}	$\overline{OE}$	A or B	2.9	7.9	10.7	2.9	12	ns
t_{PZL}			3.6	9.1	12.1	3.6	13.7	
t_{PHZ}			5.2	8.1	9.7	5.2	10.4	
t_{PLZ}			4.7	7.3	9.1	4.7	9.9	
t_{PLH}	CLKBA or CLKAB	A or B	4.4	8.5	11.3	4.4	12.7	ns
t_{PHL}			4.6	8.8	11.4	4.6	12.7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	3.8	7.5	10	3.8	11.3	ns
t_{PHL}			5.1	11.4	12.7	5.1	16.6	
t_{PLH}	SBA or SAB† (with A or B low)	A or B	4.5	10.6	13.9	4.5	15.8	ns
t_{PHL}			4.3	8.3	10.8	4.3	11.9	
t_{PZH}	DIR	A or B	2.8	7.8	10.7	2.8	11.9	ns
t_{PZL}			3.7	9.3	12.2	3.7	13.7	
t_{PHZ}			4.6	8.6	10.9	4.6	11.5	
t_{PLZ}			4	7.4	9.7	4	10.4	

† These parameters are measured with the internal output state of the storage registers opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

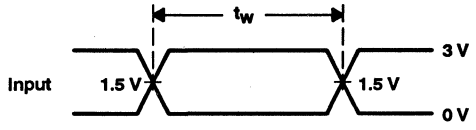
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	63	pF
		Outputs disabled			14	

PARAMETER MEASUREMENT INFORMATION

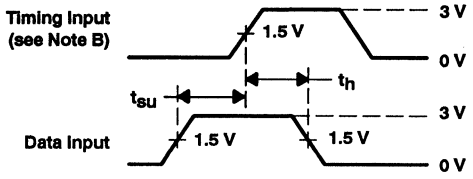


LOAD CIRCUIT

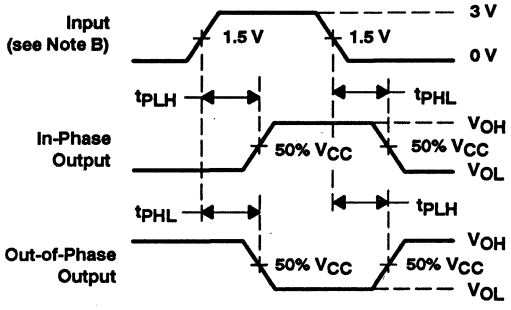
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



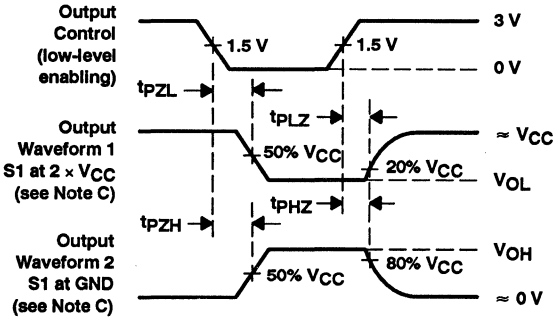
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



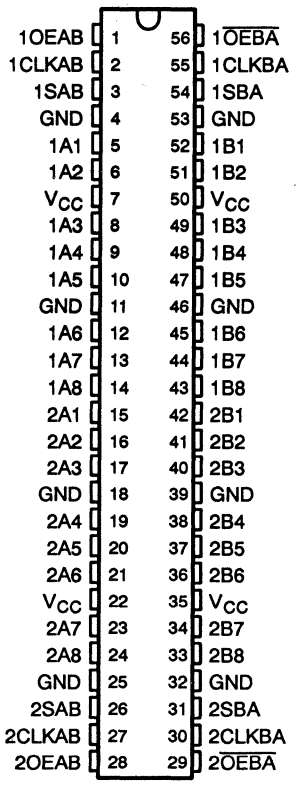
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged In Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Inverting Data Paths**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16651 . . . WD PACKAGE
74ACT16651 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16651 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ACT16651.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last state.

The 74ACT16651 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16651 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16651 is characterized fro operation from −40°C to 85°C.

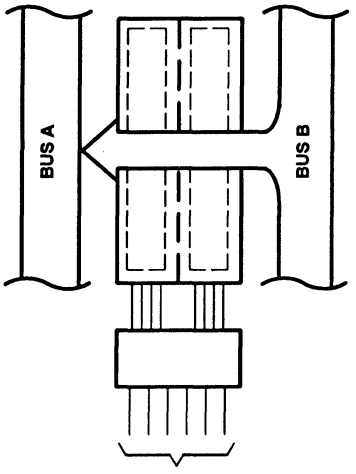
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	L	L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

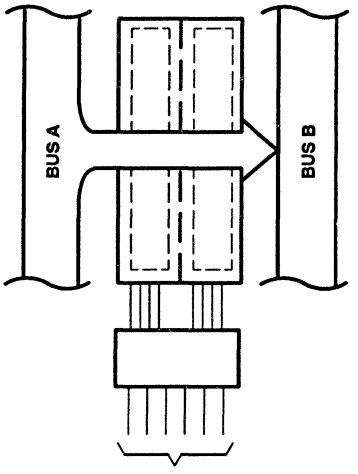
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



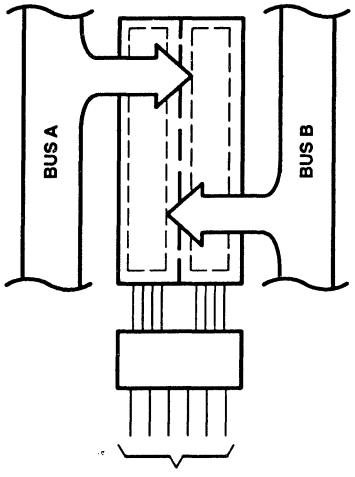
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO BUS A



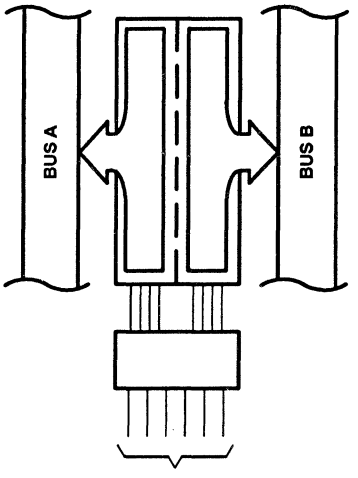
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A, B, OR A AND B

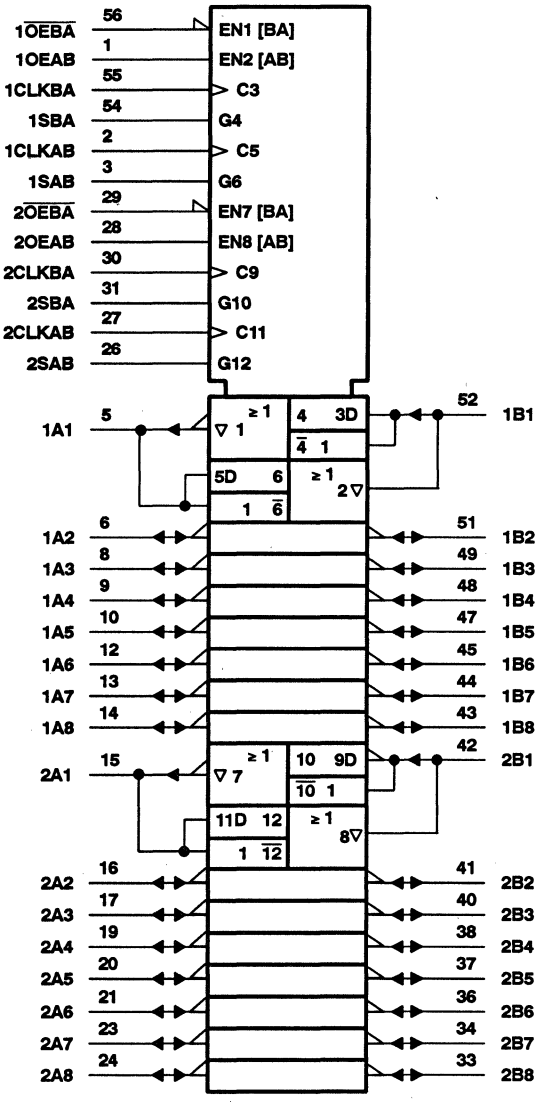


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA TO A AND/OR B

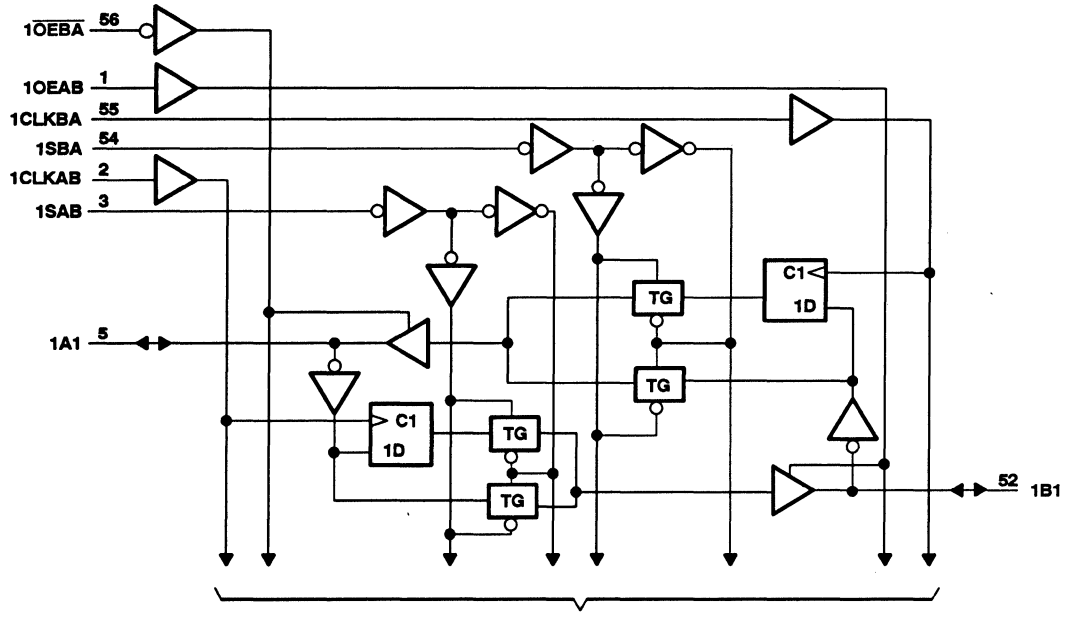
Figure 1. Bus-Management Functions

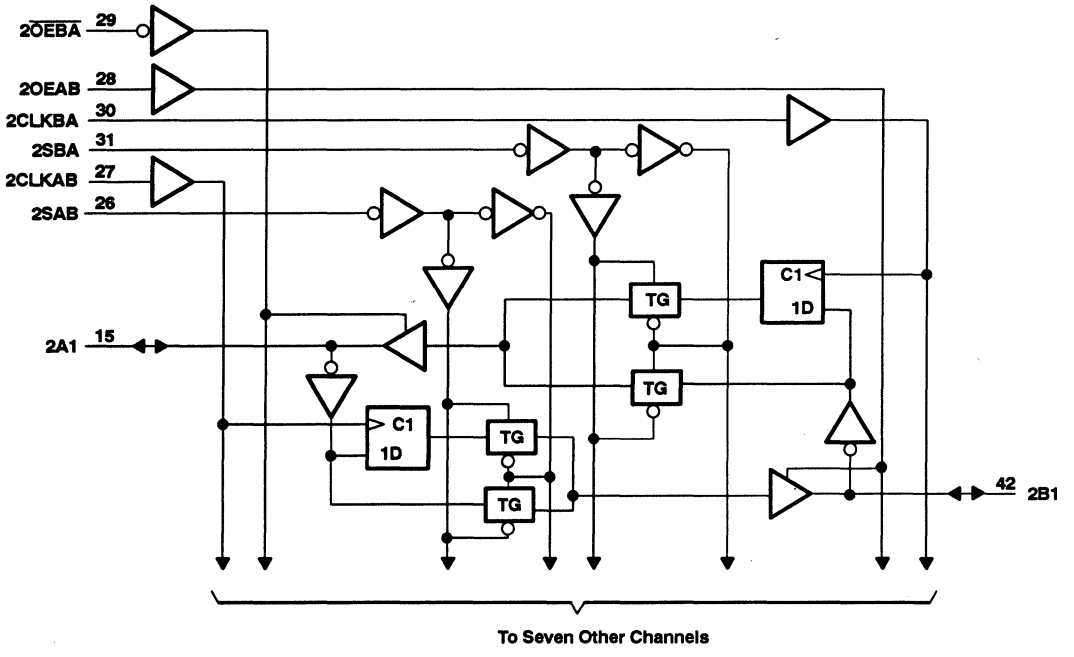
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16651			74ACT16651			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16651		74ACT16651		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54ACT16651		74ACT16651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	90	0	90	0	90	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	5.5		5.5		5.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	5.3		6.3		5.3		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		1		ns

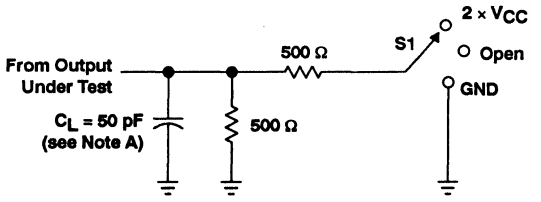
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16651		74ACT16651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	3	6.6	10	3	12.2	3	11.3	ns
t_{PHL}			4.6	8	10.6	4.6	12.7	4.6	11.9	
t_{PLH}	CLKBA or CLKAB	A or B	5.4	9.1	12	5.4	14.8	5.4	13.7	ns
t_{PHL}			5.4	9.1	12	5.4	14.6	5.4	13.6	
t_{PLH}	SBA or SAB (with A or B high)	A or B	4.6	7.9	10.5	4.6	13.1	4.6	12.1	ns
t_{PHL}			5.4	10.9	15.5	5.4	18.6	5.4	17.8	
t_{PLH}	SBA or SAB (with A or B low)	A or B	5	10.4	14.9	5	16.2	5	17.3	ns
t_{PHL}			4.9	8.6	11.9	4.9	13.7	4.9	12.7	
t_{PZH}	$\overline{OEBA}$	A	3.2	7.2	10.8	3.2	13.6	3.2	12.3	ns
t_{PZL}			3.8	8	12.2	3.8	15.3	3.8	13.9	
t_{PHZ}	$\overline{OEBA}$	A	5.1	7.8	9.8	5.1	11.3	5.1	10.6	ns
t_{PLZ}			4.9	7.7	9.9	4.9	11.4	4.9	10.8	
t_{PZH}	OEAB	B	4.9	8	10.5	4.9	12.9	4.9	11.9	ns
t_{PZL}			5.4	8.8	11.8	5.4	14.7	5.4	13.5	
t_{PHZ}	OEAB	B	4.3	7.5	10.7	4.3	12	4.3	11.4	ns
t_{PLZ}			4.5	7.6	10.8	4.5	12.3	4.5	11.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

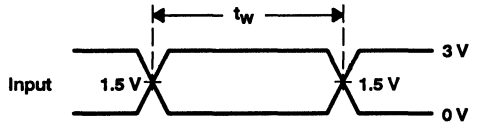
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	62	pF
		Outputs disabled			14	

PARAMETER MEASUREMENT INFORMATION

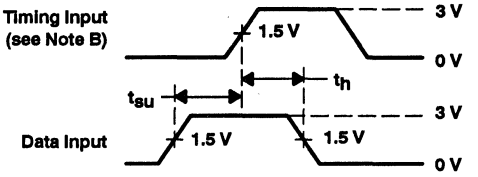


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

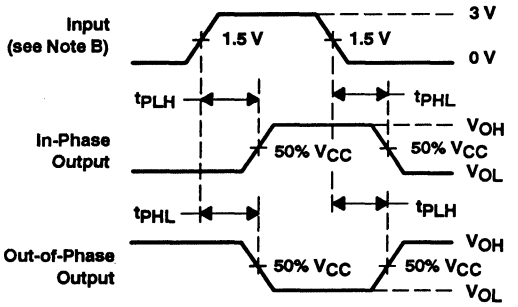
LOAD CIRCUIT



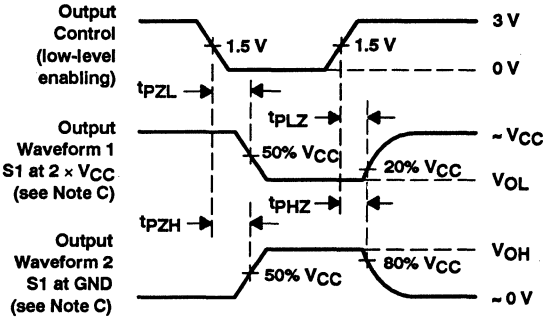
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



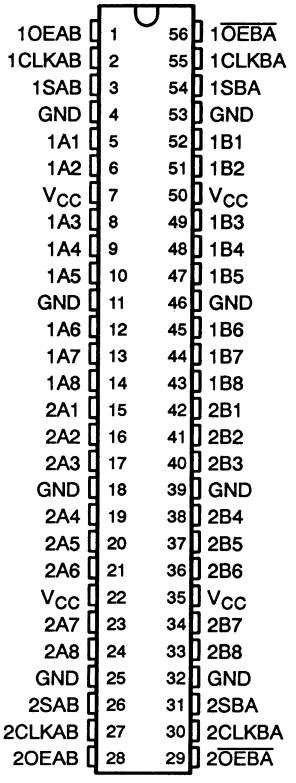
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54AC16652 . . . WD PACKAGE
74AC16652 . . . DL PACKAGE
(TOP VIEW)



description

The 'AC16652 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'AC16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last state.

The 74AC16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16652 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC16652 is characterized for operation from −40°C to 85°C.

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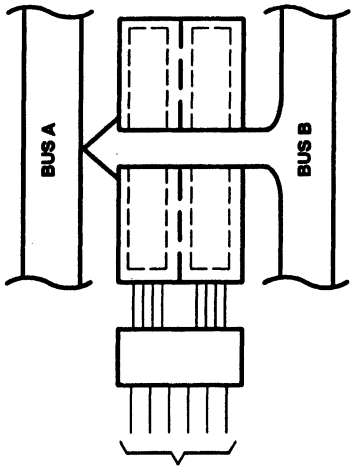
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

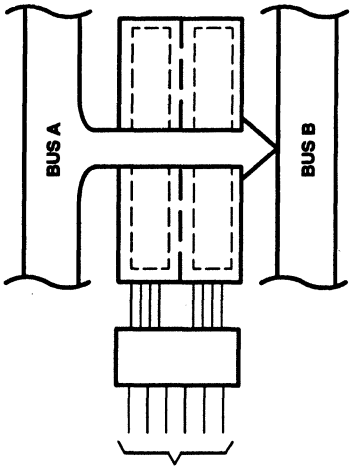
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



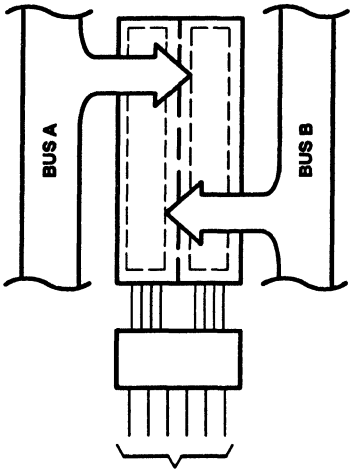
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



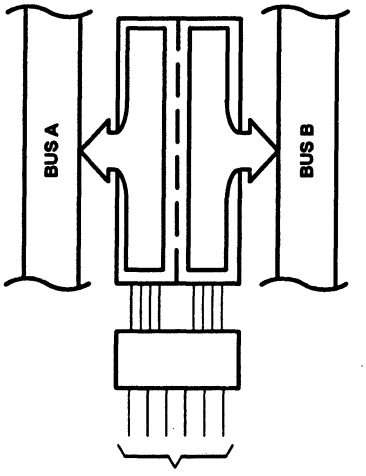
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

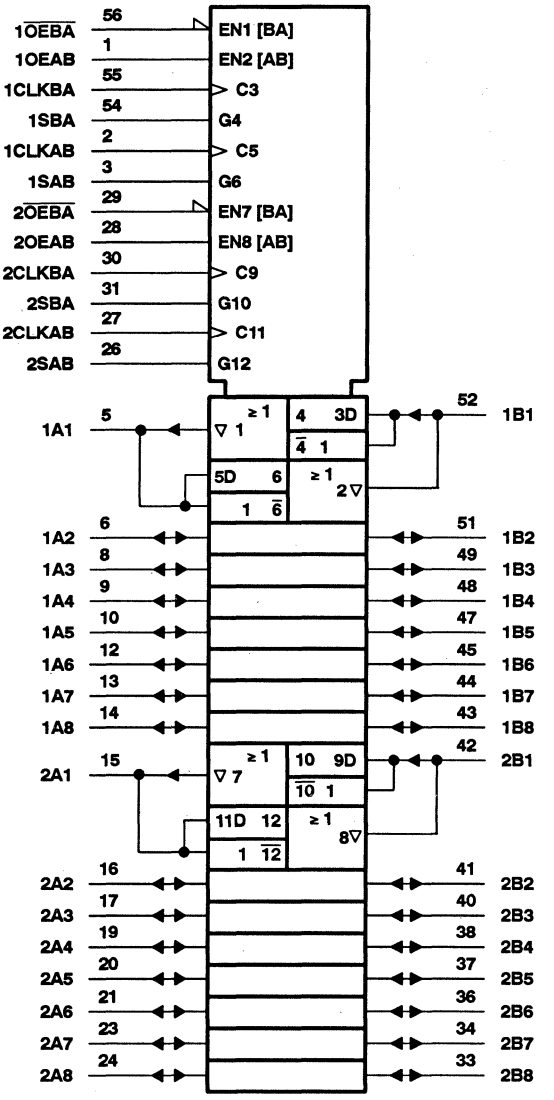


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

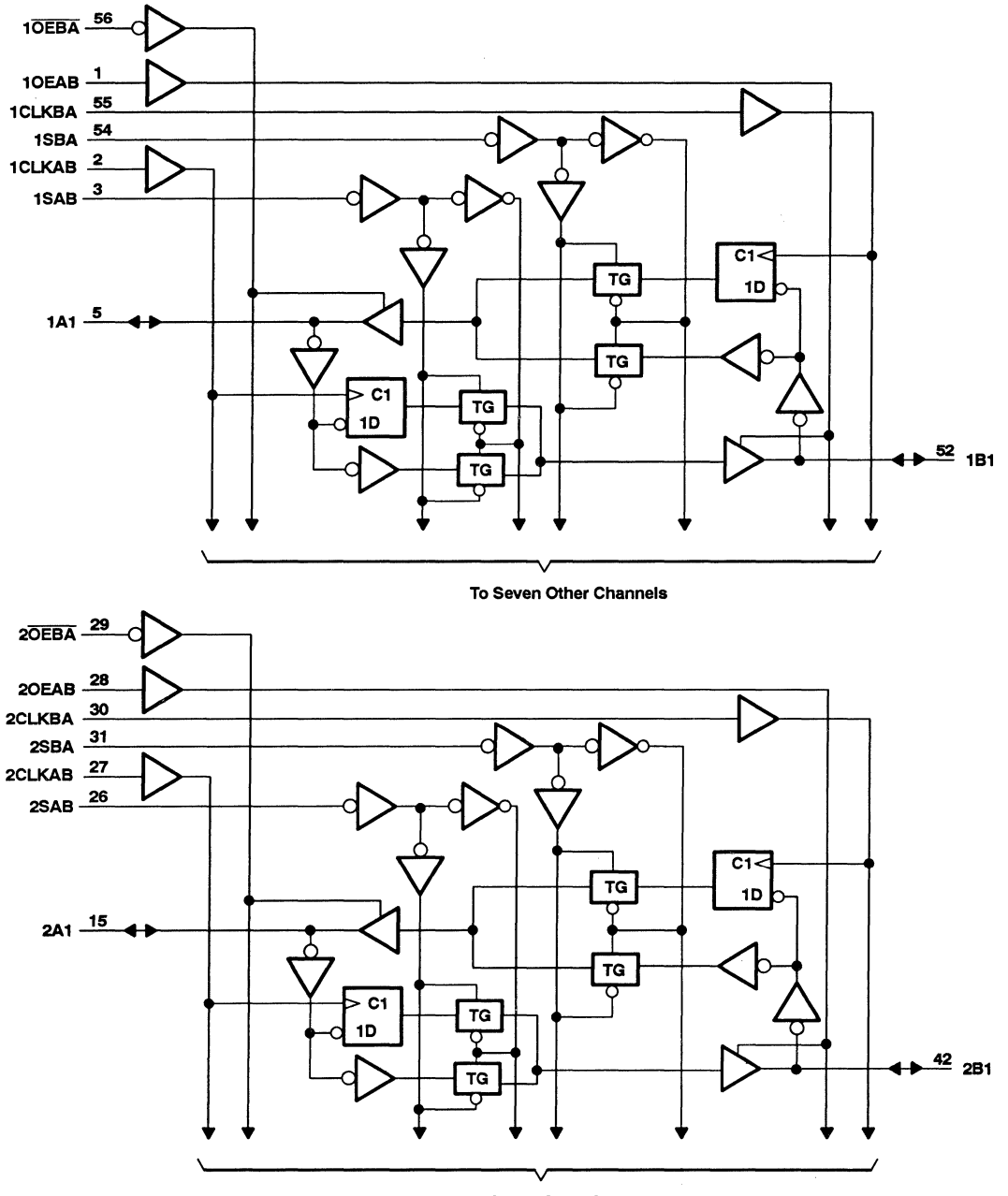
Figure 1. Bus-Management Functions

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			54AC16652			74AC16652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16652		74AC16652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16652		74AC16652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	55	0	55	0	55	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	9				9		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	7				7		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	0		0		0		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		54AC16652		74AC16652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	95	0	95	0	95	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	5				5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5				4.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	0		0		0		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16652		74AC16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			55			55		55		MHz
t_{PLH}	A or B	B or A	3.6	10.4	13.7	3.6	17.1	3.6	15.6	ns
t_{PHL}			4.1	10.9	14.3	4.1	16.3	4.1	15.4	
t_{PLH}	CLKBA or CLKAB	A or B	5.1	13.6	17.3	5.1	21.2	5.1	19.5	ns
t_{PHL}			5.4	13.5	17.2	5.4	19.9	5.4	18.8	
t_{PLH}	SBA or SAB (with A or B high)	A or B	5.8	15.0	18.7	5.8	23.3	5.8	21.4	ns
t_{PHL}			5.4	13.1	16.7	5.4	19.1	5.4	18.1	
t_{PLH}	SBA or SAB (with A or B low)	A or B	4.2	11.8	15.2	4.2	18.9	4.2	17.4	ns
t_{PHL}			5.9	14.4	18.3	5.9	21.7	5.9	20.3	
t_{PZH}	$\overline{OEBA}$	A	4.2	11.8	15.1	4.2	18.8	4.2	17.2	ns
t_{PZL}			6	16.2	20.6	6	25.3	6	23.5	
t_{PHZ}	$\overline{OEBA}$	A	4.6	8.1	10	4.6	10.9	4.6	10.6	ns
t_{PLZ}			4.4	7.6	9.6	4.4	10.6	4.4	10.3	
t_{PZH}	OEAB	B	4.1	11.5	14.6	4.1	18.1	4.1	16.6	ns
t_{PZL}			6	16.0	20	6	24.6	6	22.7	
t_{PHZ}	OEAB	B	4.3	7.2	9	4.3	9.7	4.3	9.5	ns
t_{PLZ}			3.9	6.7	8.6	3.9	9.2	3.9	9.1	

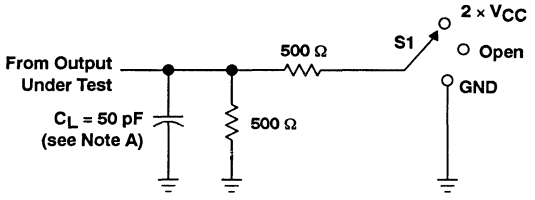
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16652		74AC16652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			95			95		95		MHz
t_{PLH}	A or B	B or A	2.7	6.1	8.8	2.7	10.7	2.7	9.9	ns
t_{PHL}			3	6.3	9.2	3	10.8	3	10.2	
t_{PLH}	CLKBA or CLKAB	A or B	3.9	7.8	10.9	3.9	13.3	3.9	12.2	ns
t_{PHL}			4.2	7.8	11.1	4.2	13.2	4.2	12.3	
t_{PLH}	SBA or SAB (with A or B high)	A or B	4.5	8.8	12.1	4.5	15	4.5	13.8	ns
t_{PHL}			4.1	7.7	11	4.1	12.9	4.1	12.1	
t_{PLH}	SBA or SAB (with A or B low)	A or B	3.1	6.7	9.7	3.1	11.9	3.1	11	ns
t_{PHL}			4.6	8.8	12.2	4.6	14.9	4.6	13.8	
t_{PZH}	$\overline{OEBA}$	A	3.1	6.7	9.5	3.1	11.6	3.1	10.7	ns
t_{PZL}			4.5	8.3	11.8	4.5	14.4	4.5	13.2	
t_{PHZ}	$\overline{OEBA}$	A	4.6	6.5	8.3	4.6	9	4.6	8.8	ns
t_{PLZ}			4.1	6.1	8.1	4.1	9.1	4.1	8.7	
t_{PZH}	OEAB	B	3.1	6.6	9.3	3.1	11.3	3.1	10.5	ns
t_{PZL}			4.6	8.2	11.6	4.6	14.1	4.6	13	
t_{PHZ}	OEAB	B	4.2	5.9	7.7	4.2	8.3	4.2	8	ns
t_{PLZ}			3.7	5.5	7.4	3.7	8.3	3.7	7.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

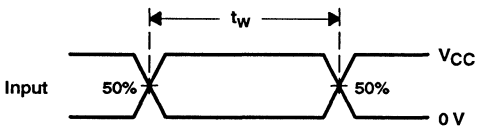
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	57	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

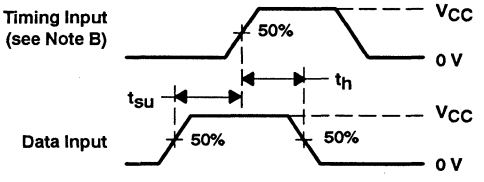


LOAD CIRCUIT

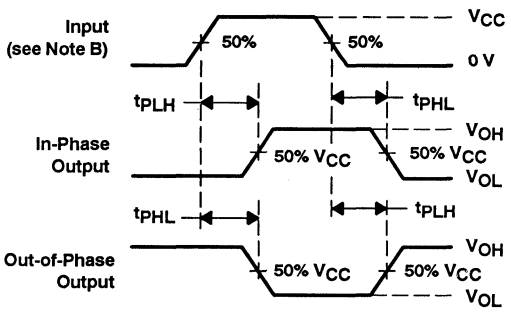
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



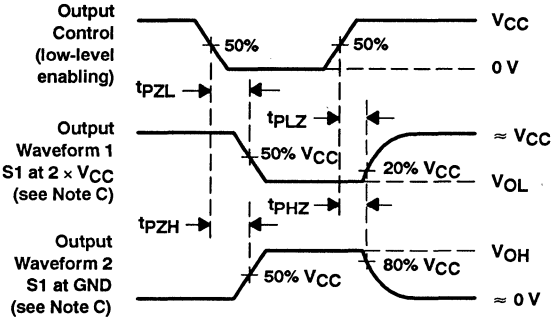
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers and Enables for A and B Buses**
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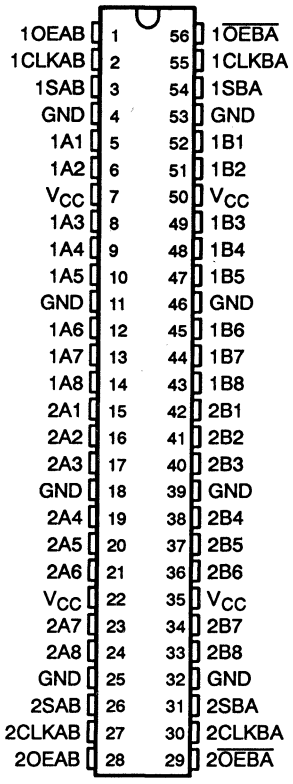
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16652 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74ACT16652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last state.

The 74ACT16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16652 is characterized for operation from −40°C to 85°C.

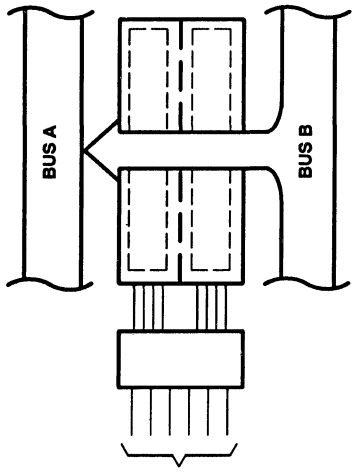
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

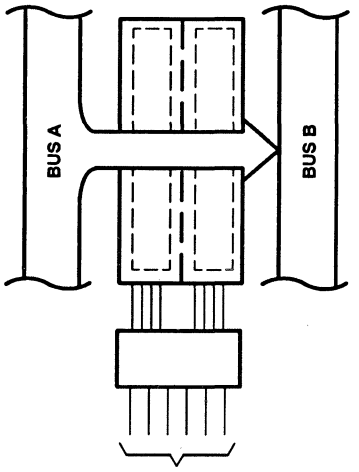
† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



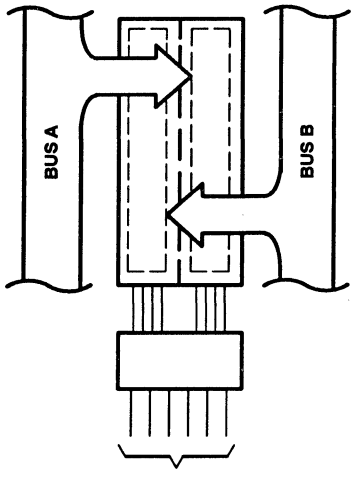
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



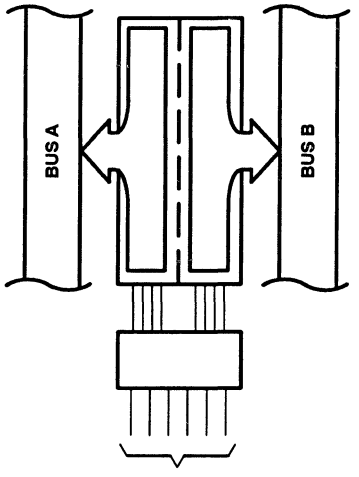
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

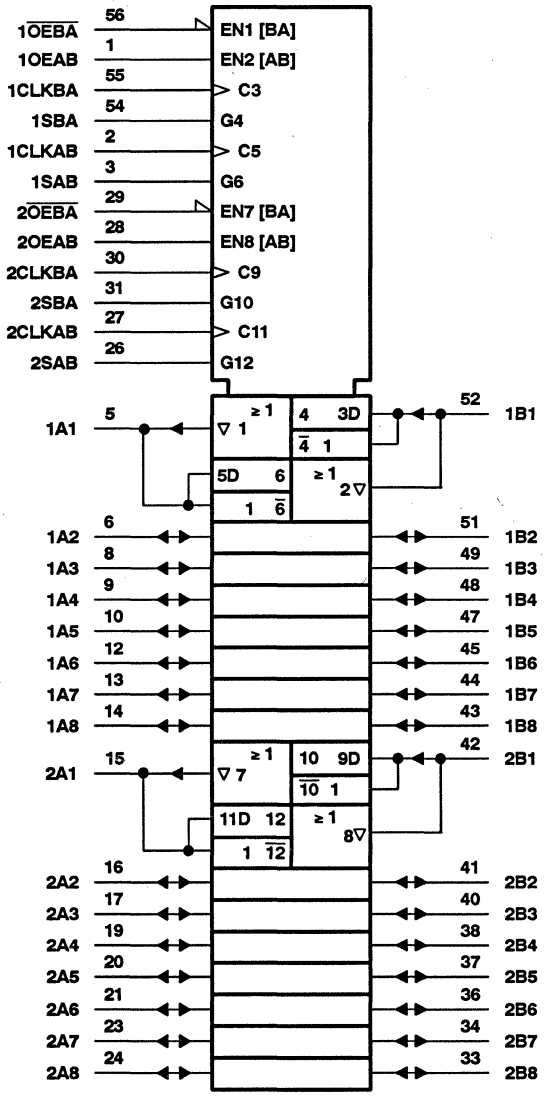


OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	L	L	H	H

TRANSFER STORED DATA
TO A AND/OR B

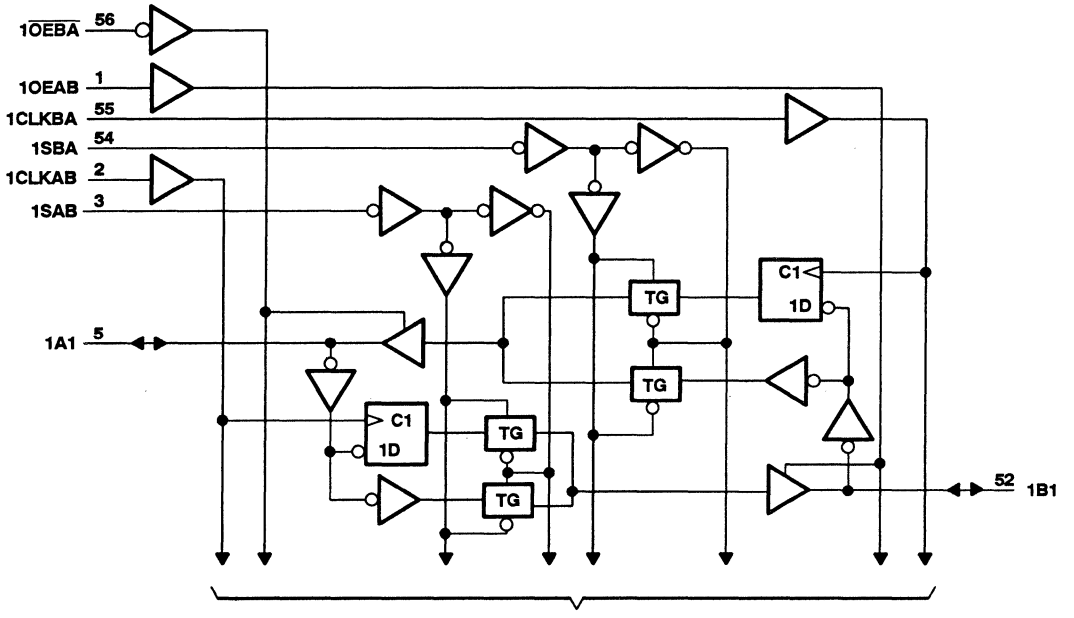
Figure 1. Bus-Management Functions

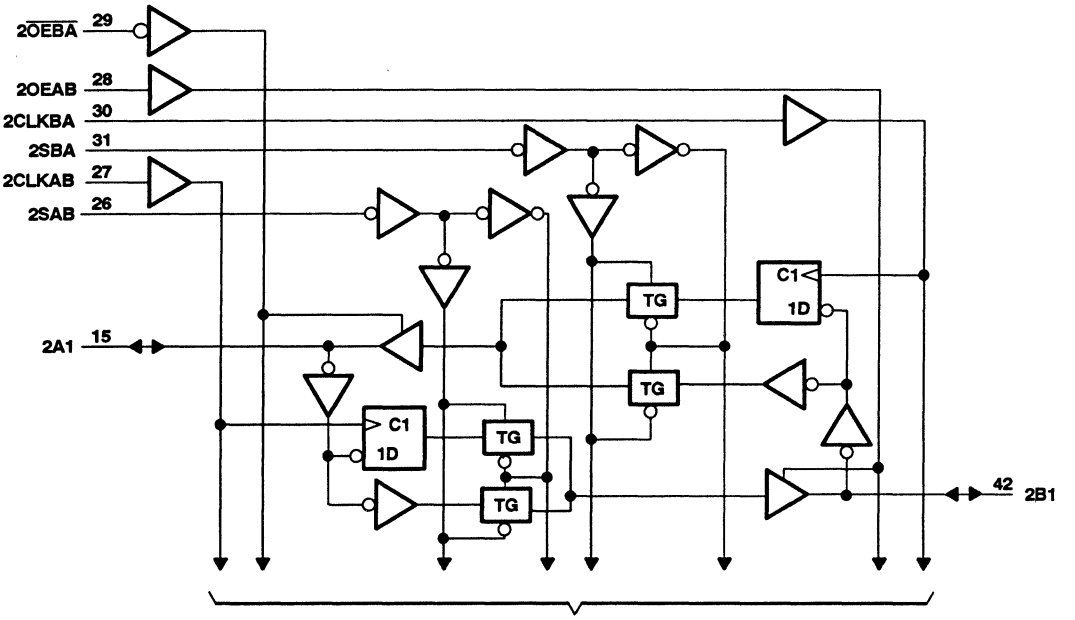
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	90	0	90	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low	5.5		5.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	4.5		4.5		ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	1		1		ns

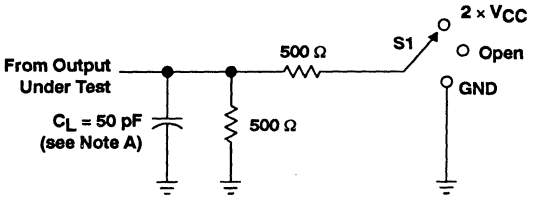
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			90			90		MHz
t_{PLH}	A or B	B or A	3.7	7.2	9.4	3.7	10.5	ns
t_{PHL}			3	8.1	10.5	3	11.6	
t_{PLH}	CBA or CAB	A or B	4.5	8.7	11.2	4.5	12.3	ns
t_{PHL}			4.9	8.9	11.3	4.9	12.3	
t_{PLH}	SBA or SAB (with A or B high)	A or B	4.9	10.4	14.1	4.9	16	ns
t_{PHL}			4.6	8.4	10.6	4.6	11.7	
t_{PLH}	SBA or SAB (with A or B low)	A or B	3.9	7.8	10	3.9	11.2	ns
t_{PHL}			5.6	12.3	14.9	5.6	16.9	
t_{PZH}	$\overline{OEBA}$	A	3	8.1	10.5	3	11.7	ns
t_{PZL}			3.9	9.4	12	3.9	13.4	
t_{PHZ}	$\overline{OEBA}$	A	5.3	7.4	8.9	5.3	9.5	ns
t_{PLZ}			4.8	6.8	8.6	4.8	9.2	
t_{PZH}	OEAB	B	4.1	7.7	9.8	4.1	10.8	ns
t_{PZL}			5	9	11	5	12.4	
t_{PHZ}	OEAB	B	4.4	8.1	10.1	4.4	10.5	ns
t_{PLZ}			4.3	7.7	9.7	4.3	9.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

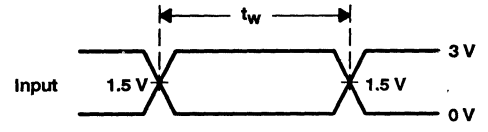
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	57	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

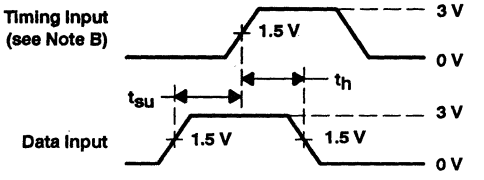


LOAD CIRCUIT

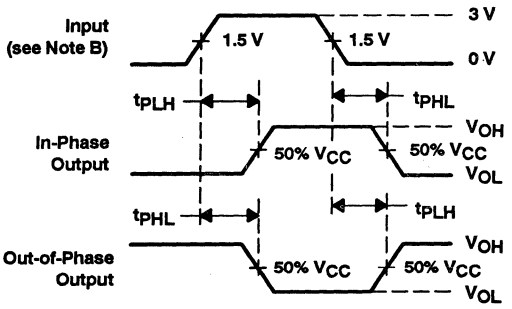
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



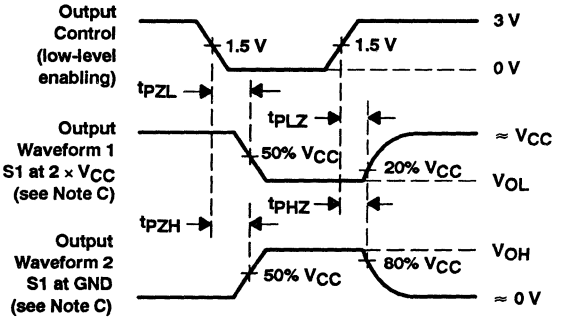
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



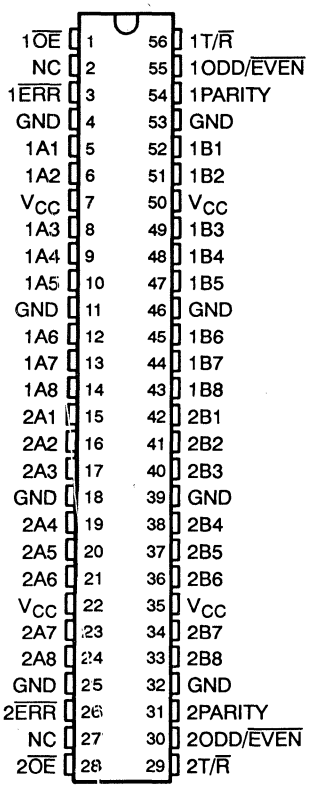
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged In Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16657 contains two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive (1T/$\overline{R}$ or 2T/$\overline{R}$) input determines the direction of data flow. When 1T/$\overline{R}$ (or 2T/$\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/$\overline{R}$ (or 2T/$\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable (1$\overline{OE}$ or 2$\overline{OE}$) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. For example, if 1ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1$\overline{ERR}$ (or 2$\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/$\overline{EVEN}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1$\overline{ERR}$ is low, indicating a parity error.

The 74ACT16657 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

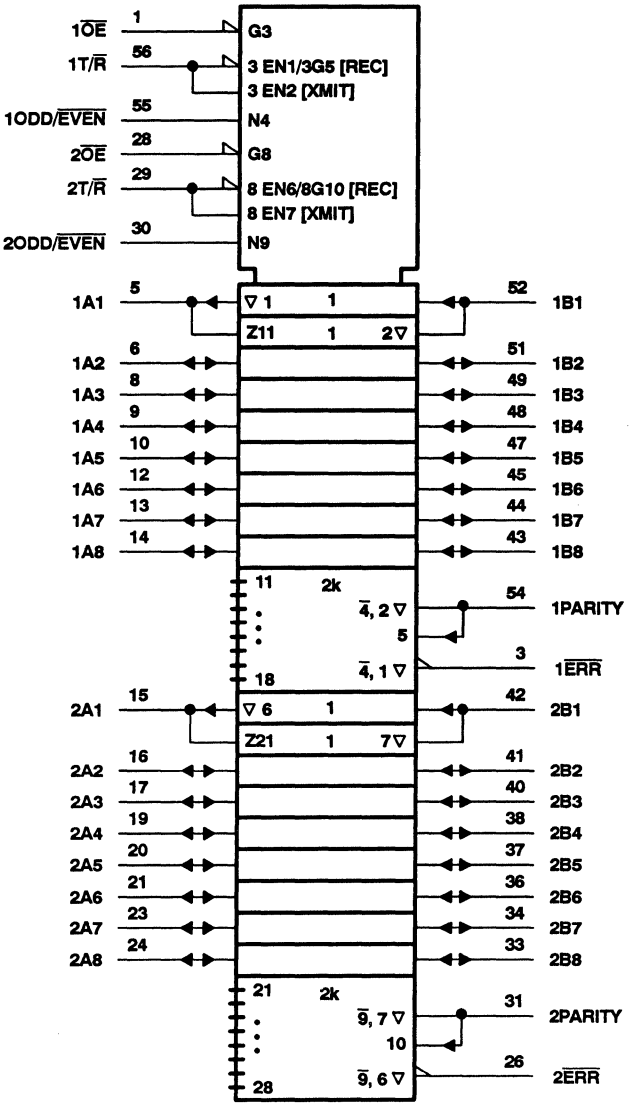
The 74ACT16657 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE

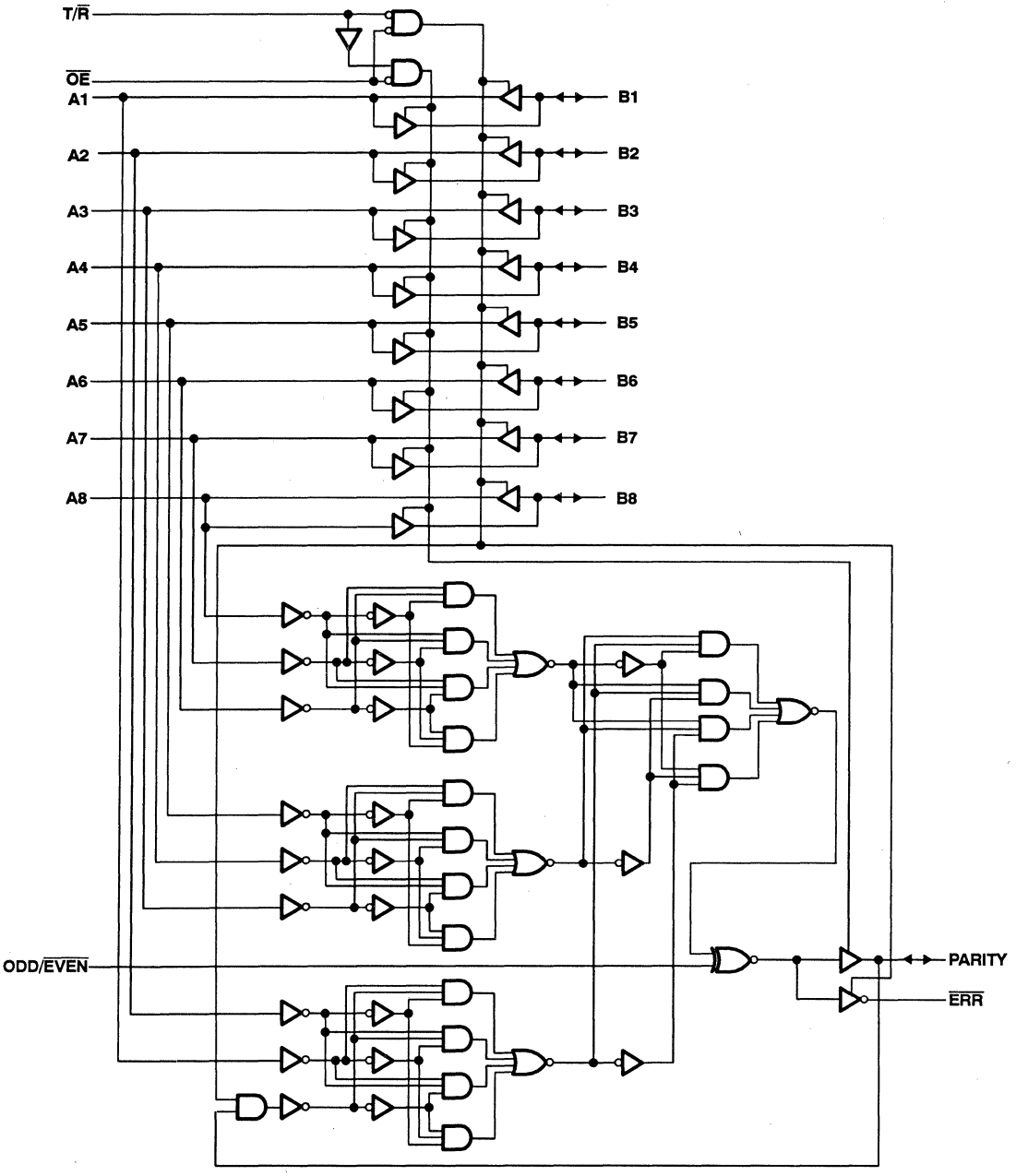
NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each transceiver (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = – 50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = – 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	A or B ports	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	Control Inputs	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	$\overline{ERR}$	V_O = V_{CC} or GND	5 V		11				pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

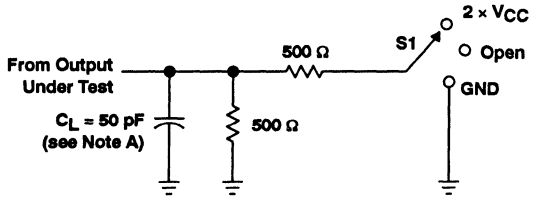
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	4.1	7.3	9.6	4.1	10.7	ns
t_{PHL}			3.2	6.8	9.8	3.2	10.6	
t_{PLH}	A	PARITY	4	8.6	12.9	4	14.3	ns
t_{PHL}			4.3	9	13.1	4.3	14.3	
t_{PLH}	ODD/$\overline{EVEN}$	PARITY, $\overline{ERR}$	3.7	8.3	12.3	3.7	13.7	ns
t_{PHL}			4.1	8.8	12.8	4.1	14.1	
t_{PLH}	B	$\overline{ERR}$	3.9	8.6	13	3.9	14.6	ns
t_{PHL}			4.3	9	13.3	4.3	14.7	
t_{PLH}	PARITY	$\overline{ERR}$	3.8	8.4	12.2	3.8	13.8	ns
t_{PHL}			4.1	8	12.8	4.1	14.2	
t_{PZH}	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	2.6	6.1	10.1	2.6	11.3	ns
t_{PZL}			3.2	7.2	11.7	3.2	13	
t_{PHZ}	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	5.9	8.6	10.5	5.9	11.2	ns
t_{PLZ}			5.3	8	9.8	5.3	10.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

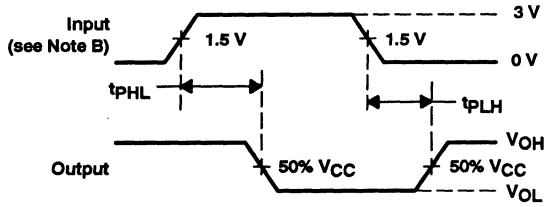
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	76	pF
		Outputs disabled		35	

PARAMETER MEASUREMENT INFORMATION

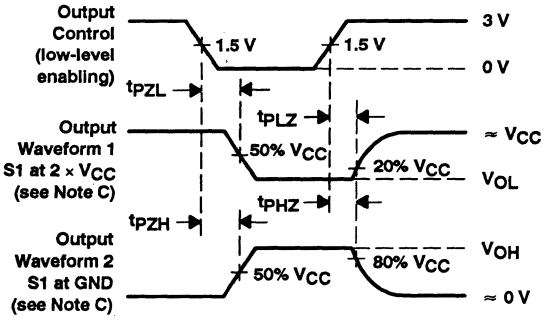


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



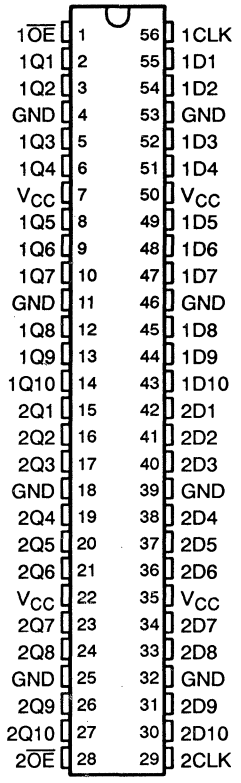
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes Printed-Circuit-Board (PCB) Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

DL PACKAGE
(TOP VIEW)



description

This 20-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

This device can be used as two 10-bit flip-flops or one 20-bit flip-flop.

On the positive transition of the clock, the Q outputs will follow the data (D) inputs. Each 10-bit flip-flop section has a buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input that can be used to place the ten outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16821 is packaged in theTI shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16821 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 10-bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

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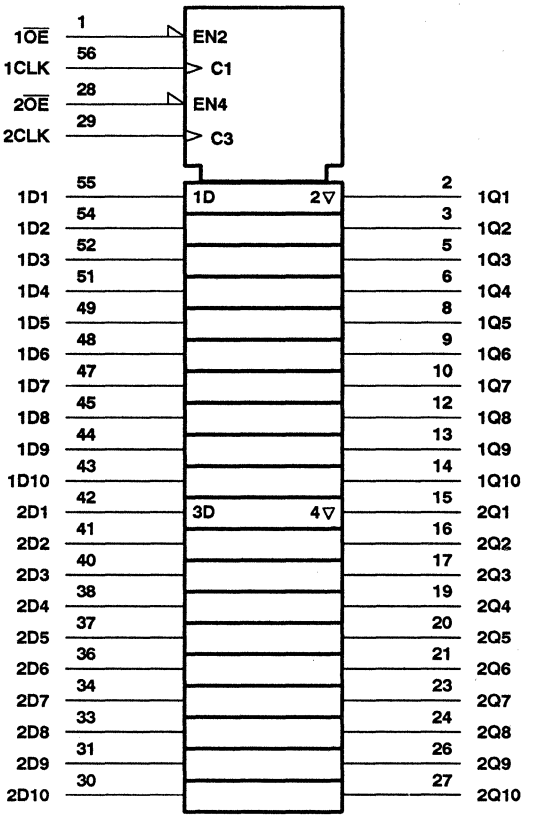
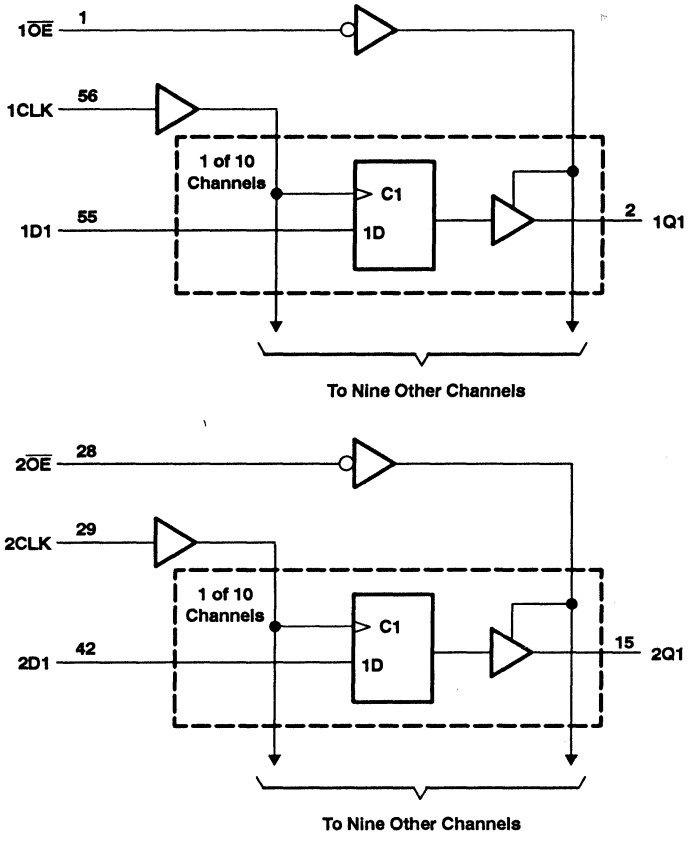
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±500 mA
Maximum package power dissipation at T_A = 55°C (in still air)	1 W
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	V_I = V_{CC} or GND	5 V		3				pF
C_o	V_O = V_{CC} or GND	5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	70	0	70	MHz
t_w	Pulse duration, CLK high or low	7		7		ns
t_{su}	Setup time, data before CLK↑	7.5		7.5		ns
t_h	Hold time, data after CLK↑	0.5		0.5		ns

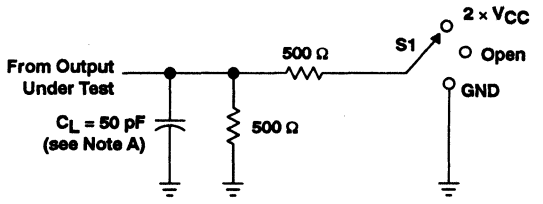
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			70			70		MHz
t_{PLH}	CLK	Any Q	4.5	8.8	12	4.5	13.4	ns
t_{PHL}			5.2	9.5	12.6	5.2	14	
t_{PZH}	$\overline{OE}$	Any Q	2.8	8.6	10.8	2.8	11.9	ns
t_{PZL}			4	9.7	13.3	4	14.7	
t_{PHZ}	$\overline{OE}$	Any Q	5.4	8.3	10	5.4	10.7	ns
t_{PLZ}			4.7	7.6	9.3	4.7	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

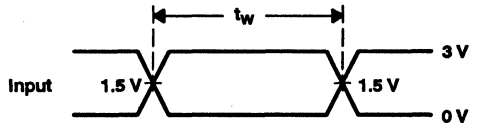
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		25	

PARAMETER MEASUREMENT INFORMATION

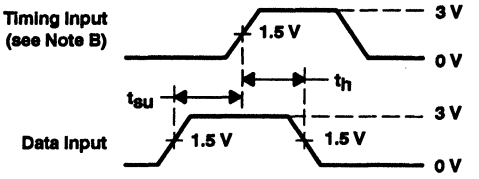


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND

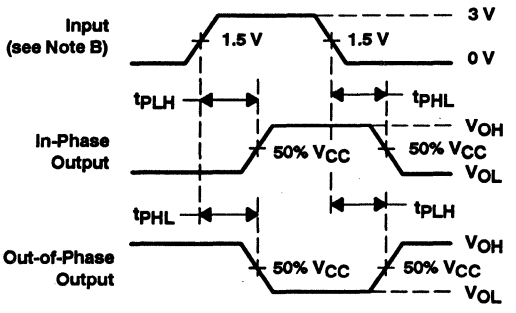
LOAD CIRCUIT



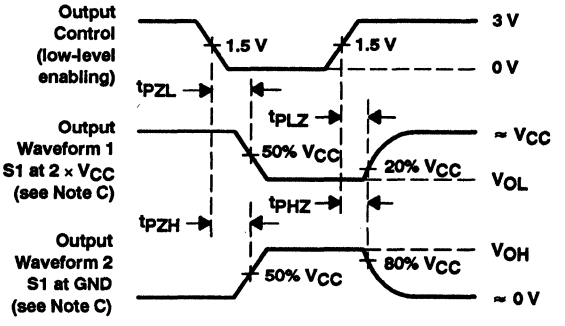
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



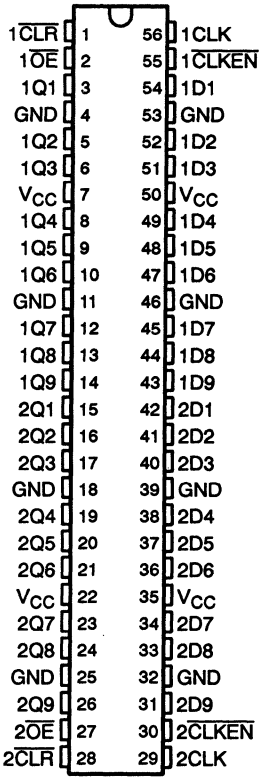
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages Using 25-mil Center-to-Center Pin Spacings**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

This 18-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

The 74AC16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16823 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74AC16823 is characterized for operation from −40°C to 85°C.

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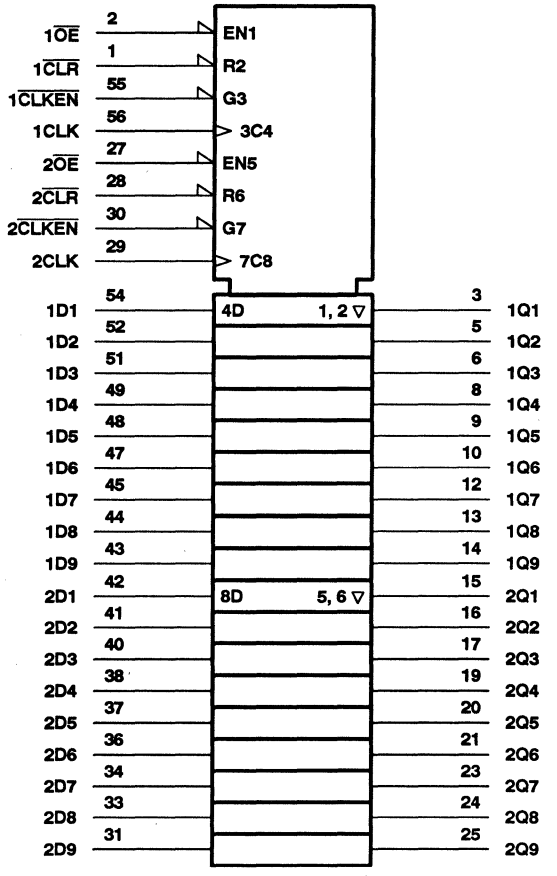
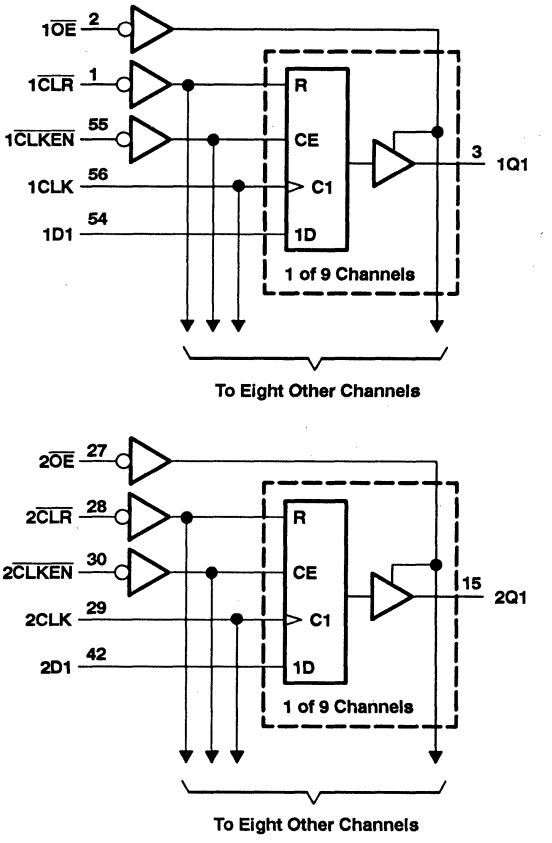
FUNCTION TABLE
(each 9-bit stage)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum power package dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		3				pF
C_o	V_O = V_{CC} or GND	5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	60	0	60	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		ns
		CLK high or low	8.4		8.4		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	0.5		0.5		ns
		Data	7.2		7.2		
		$\overline{CLKEN}$ low	5.8		5.8		
t_h	Hold time after CLK↑	Data	0		0		ns
		$\overline{CLKEN}$ high or low	1		1		

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	115	0	115	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		ns
		CLK high or low	4.4		4.4		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	0.6		0.6		ns
		Data	5		5		
		$\overline{CLKEN}$ low	4.2		4.2		
t_h	Hold time after CLK↑	Data	1.3		1.3		ns
		$\overline{CLKEN}$ high or low	1.4		1.4		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			60			60		MHz
t_{PLH}	CLK	Q	3.9	13.8	16.8	3.9	18.8	ns
t_{PHL}			4.7	14.5	17.3	4.7	18.9	
t_{PHL}	$\overline{CLR}$	Q	4	12.4	14.9	4	16.2	ns
t_{PZH}	$\overline{OE}$	Q	3	11.1	14	3	15.4	ns
t_{PZL}			4.3	15	18.7	4.3	20.8	
t_{PHZ}	$\overline{OE}$	Q	4.5	8.5	10.4	4.5	11.2	ns
t_{PLZ}			3.9	7.7	9.3	3.9	10.3	

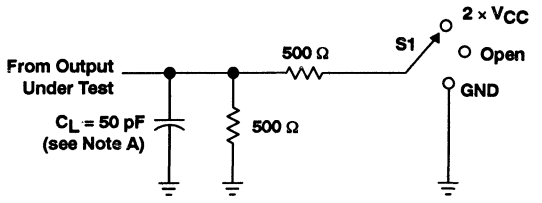
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			115			115		MHz
t_{PLH}	CLK	Q	3.1	7.8	10.6	3.1	12	ns
t_{PHL}			3.9	8.6	11.4	3.9	12.7	
t_{PHL}	$\overline{CLR}$	Q	3.2	7.4	9.9	3.2	11	ns
t_{PZH}	$\overline{OE}$	Q	2.2	6.1	8.6	2.2	9.7	ns
t_{PZL}			3	7.4	10.6	3	11.8	
t_{PHZ}	$\overline{OE}$	Q	4.2	6.8	8.7	4.2	9.3	ns
t_{PLZ}			3.7	6.2	7.8	3.7	8.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

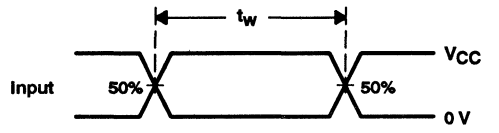
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	36	pF
		Outputs disabled		18	

PARAMETER MEASUREMENT INFORMATION

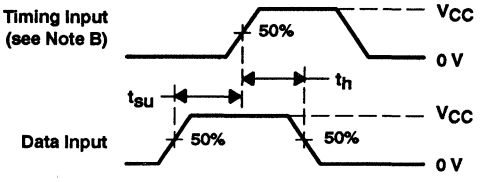


LOAD CIRCUIT

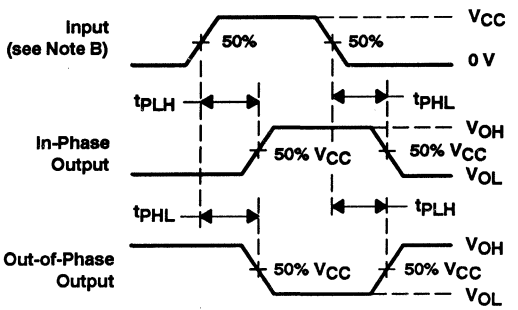
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × VCC
t_{PHZ}/t_{PZH}	GND



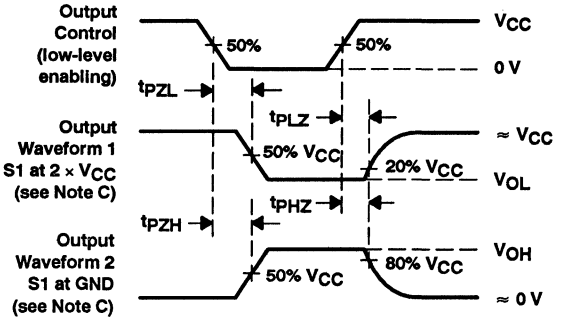
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



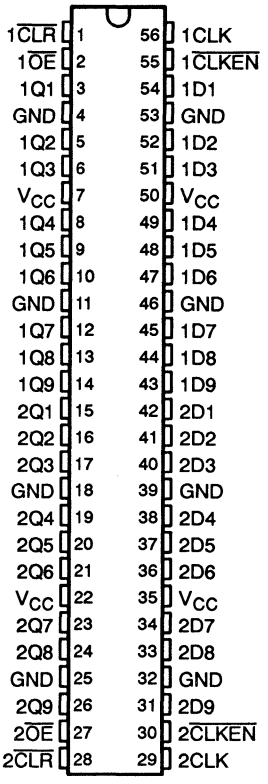
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes Printed-Circuit-Board (PCB) Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

DL PACKAGE
(TOP VIEW)



description

This 18-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, parity bus interfacing, and working registers.

The 74ACT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16823 is packaged in theTI shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

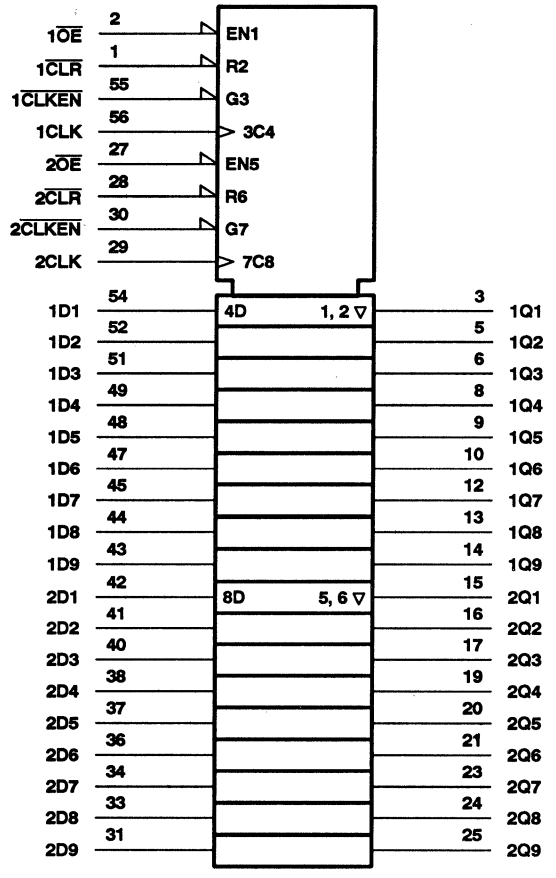
The 74ACT16823 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

FUNCTION TABLE
(each 9-bit stage)

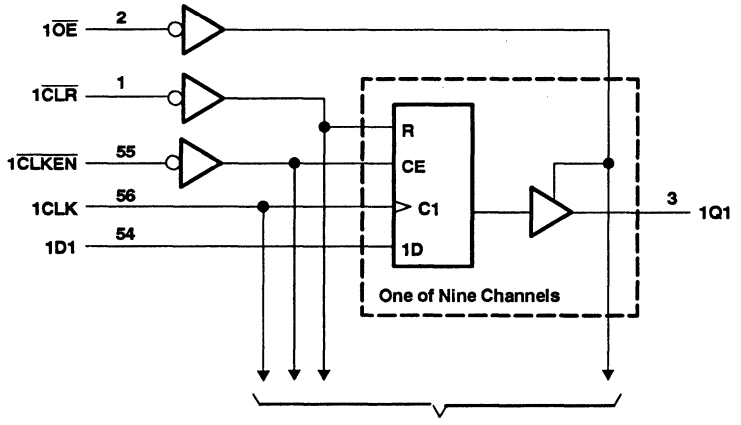
INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

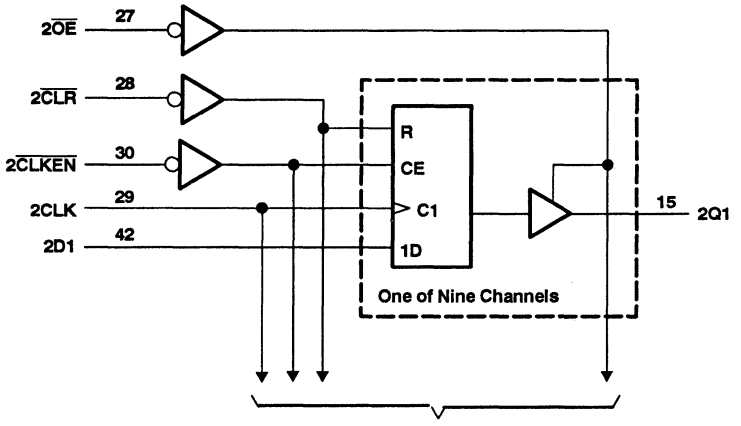
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3				pF
C_o	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	90	0	90	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		ns
		CLK high or low	5.5		5.5		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	0.5		0.5		ns
		Data	7		7		
		$\overline{CLKEN}$ low	3.5		3.5		
t_h	Hold time after CLK↑	Data	0.5		0.5		ns
		$\overline{CLKEN}$ high or low	2.5		2.5		

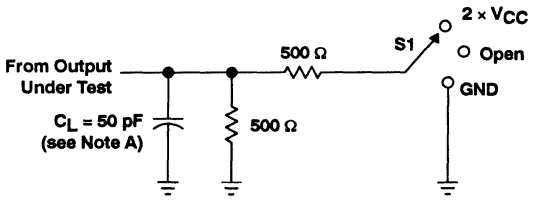
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			90			90		MHz
t_{PLH}	CLK	Q	4.2	7.5	10.6	4.2	12.1	ns
t_{PHL}			4.8	8.3	11.5	4.8	12.9	
t_{PHL}	$\overline{CLR}$	Q	3.4	7.3	11.2	3.4	12.5	ns
t_{PZH}	$\overline{OE}$	Q	2.4	5.9	9.5	2.4	10.7	ns
t_{PZL}			3.3	7.1	11.3	3.3	12.8	
t_{PHZ}	$\overline{OE}$	Q	5.5	7.6	9.7	5.5	10.3	ns
t_{PLZ}			4.6	6.7	8.8	4.6	9.4	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

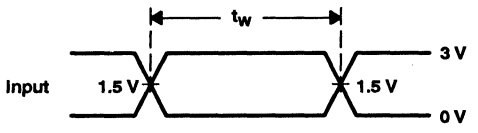
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		24	

PARAMETER MEASUREMENT INFORMATION

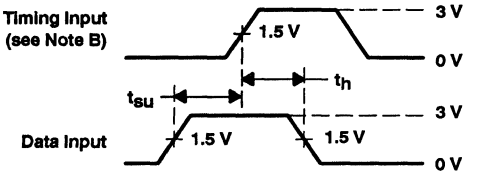


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

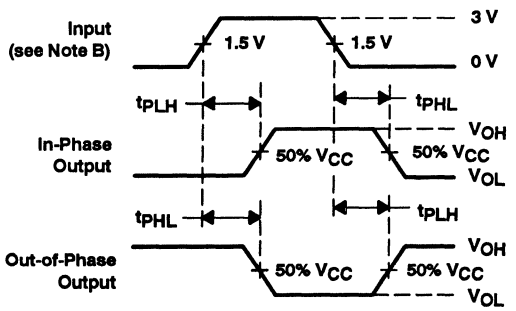
LOAD CIRCUIT



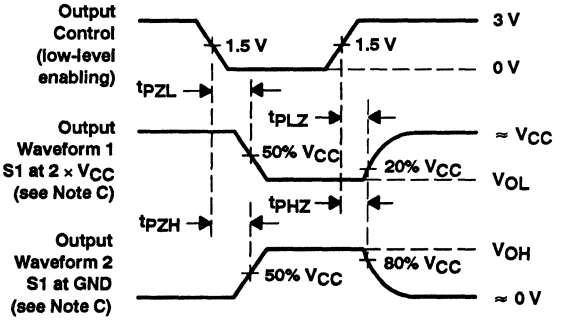
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



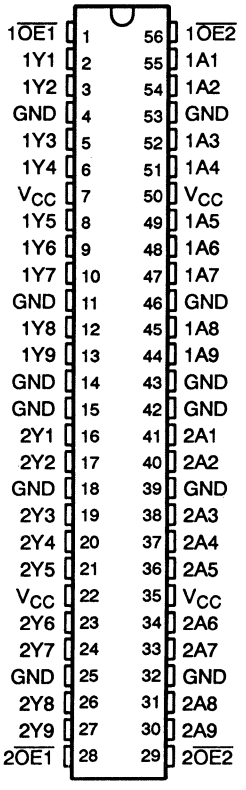
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged In Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes Printed-Circuit-Board (PCB) Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16825 is an 18-bit buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 74ACT16825 can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input NOR gate so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) inputs is high, all nine affected outputs are in the high-impedance state.

The 74ACT16825 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

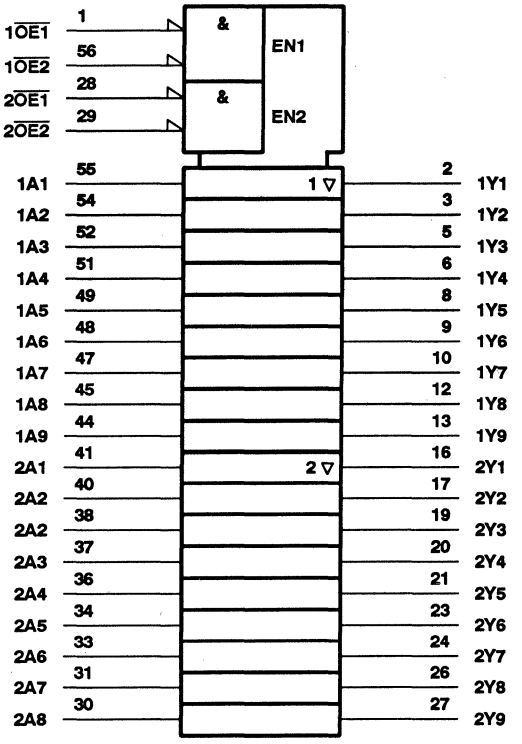
The 74ACT16825 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

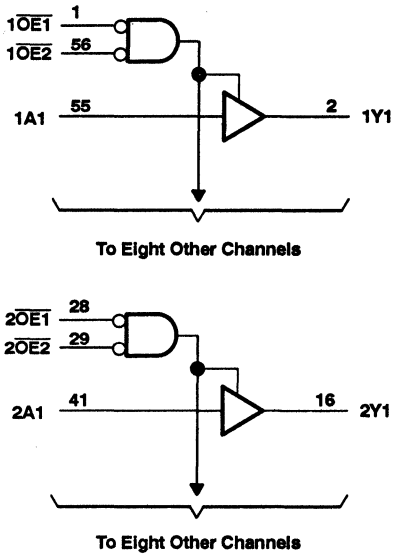
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF
C_o	$V_O = V_{CC}$ or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

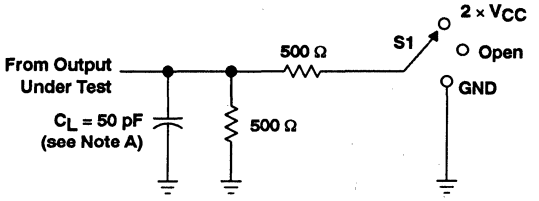
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	4.1	7.5	9.3	4.1	10.5	ns
t_{PHL}			3.1	7.5	9.6	3.1	10.3	
t_{PZH}	$\overline{OE}$	Y	3.3	7.9	9.9	3.3	11	ns
t_{PZL}			4.1	9.5	12.1	4.1	13.2	
t_{PHZ}	$\overline{OE}$	Y	5.7	9	10.8	5.7	11.5	ns
t_{PLZ}			5.5	8.5	10	5.5	10.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

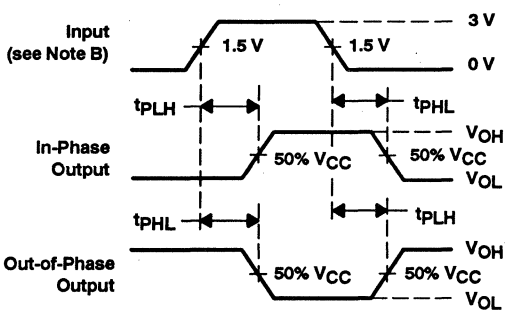
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	42	pF
		Outputs disabled		12	

PARAMETER MEASUREMENT INFORMATION

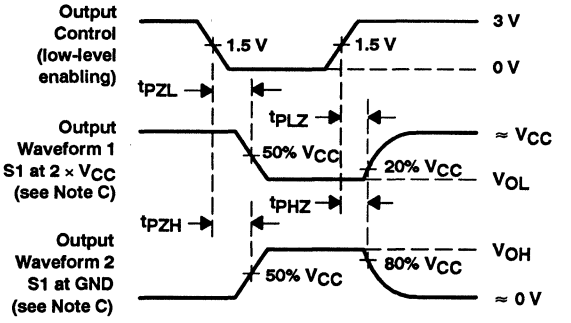


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



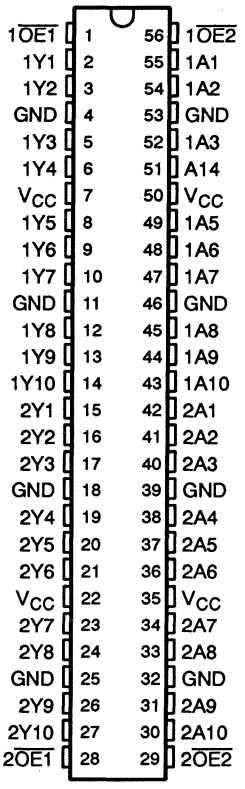
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL- or CMOS-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16827 is a noninverting 20-bit buffer composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The 74ACT16827 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16827 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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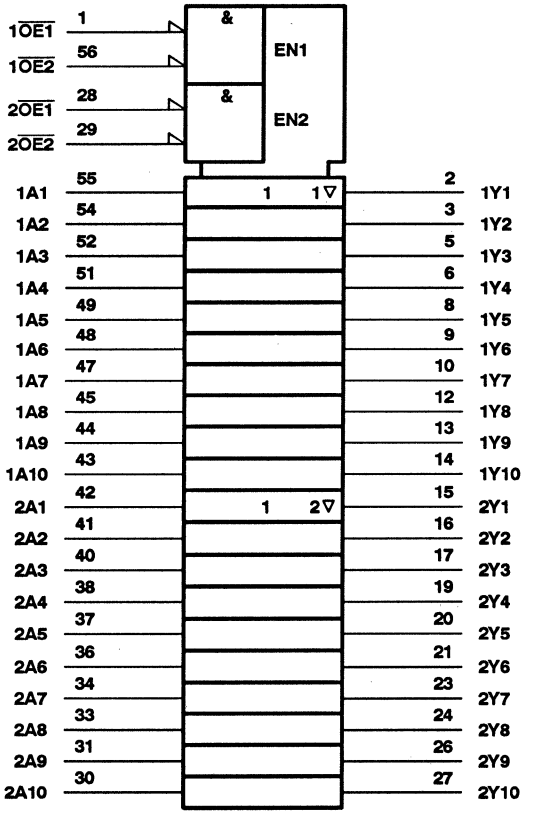
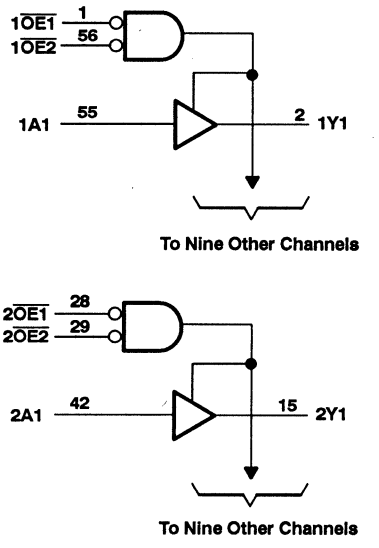
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_o	$V_O = V_{CC}$ or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

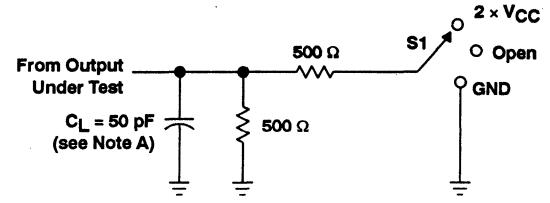
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	3.6	7.4	9.8	3.6	11	ns
t_{PHL}			2.8	7.4	9.8	2.8	10.8	
t_{PZH}	$\overline{OE}$	Y	3	7.9	10.4	3	11.7	ns
t_{PZL}			4	9.6	12.4	4	14	
t_{PHZ}	$\overline{OE}$	Y	5.8	9.1	11.3	5.8	12.4	ns
t_{PLZ}			5.3	8.5	10.5	5.3	11.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

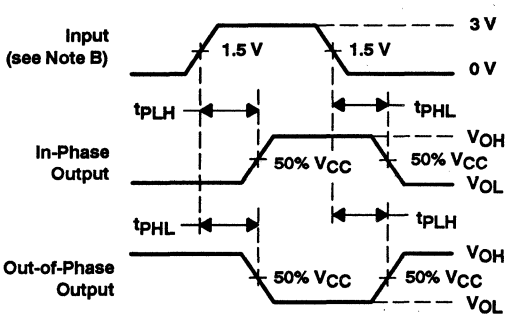
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

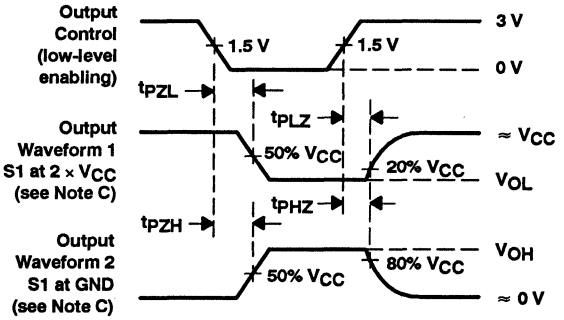


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

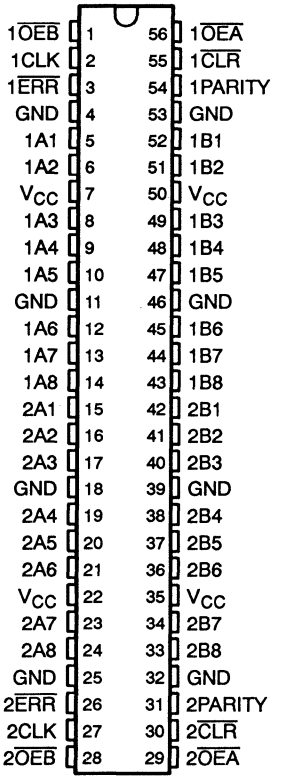
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS166 – D3546, JUNE 1990 – REVISED APRIL 1993

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16833 consists of two noninverting 8-bit to 9-bit parity bus transceivers and is designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error (1$\overline{\text{ERR}}$ or 2$\overline{\text{ERR}}$) output is configured as an open-collector output. The B-to-A parity error flag is clocked into 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) on the low-to-high transition of the clock (1CLK or 2CLK) input. 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) is cleared (set high) by taking the clear (1$\overline{\text{CLR}}$ or 2$\overline{\text{CLR}}$) input low.

The 74ACT16833 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The output-enable ($\overline{\text{OEA}}$ and $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 74ACT16833 is characterized for operation from −40°C to 85°C.

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FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	AI Σ OF H's	BI† Σ OF H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd					H	
		H	↑	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

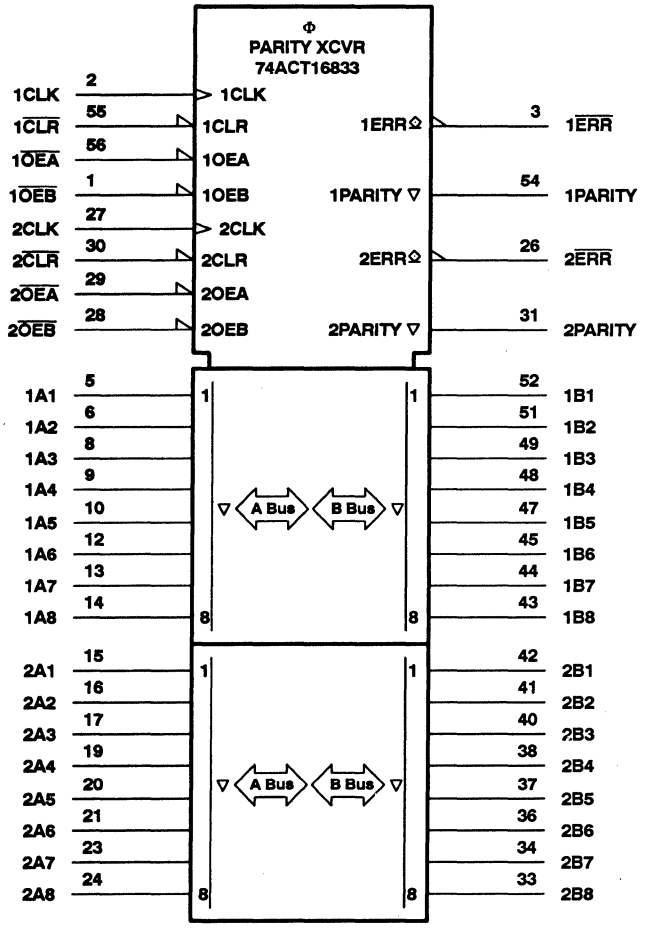
NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume the $\overline{ERR}$ output was previously high.

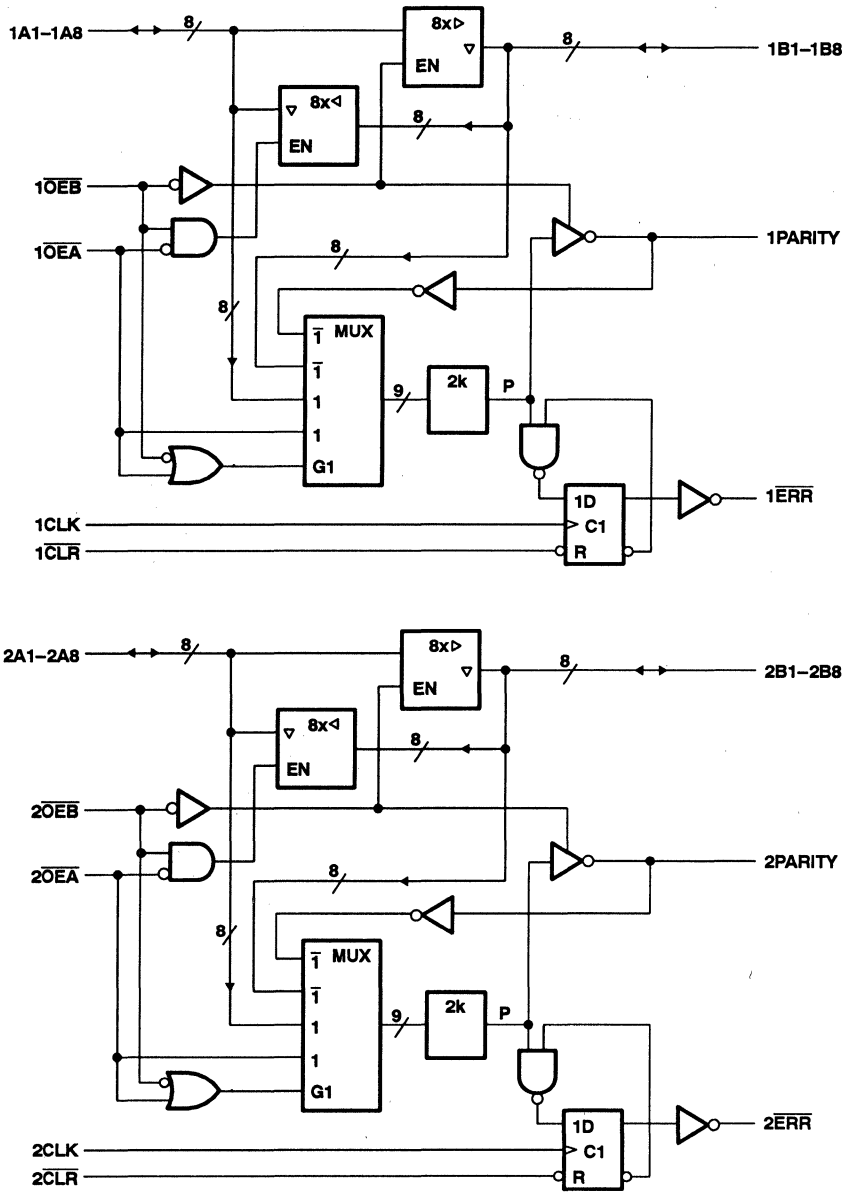
§ In this mode, the $\overline{ERR}$ output (when clocked) shows inverted parity of the A bus.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

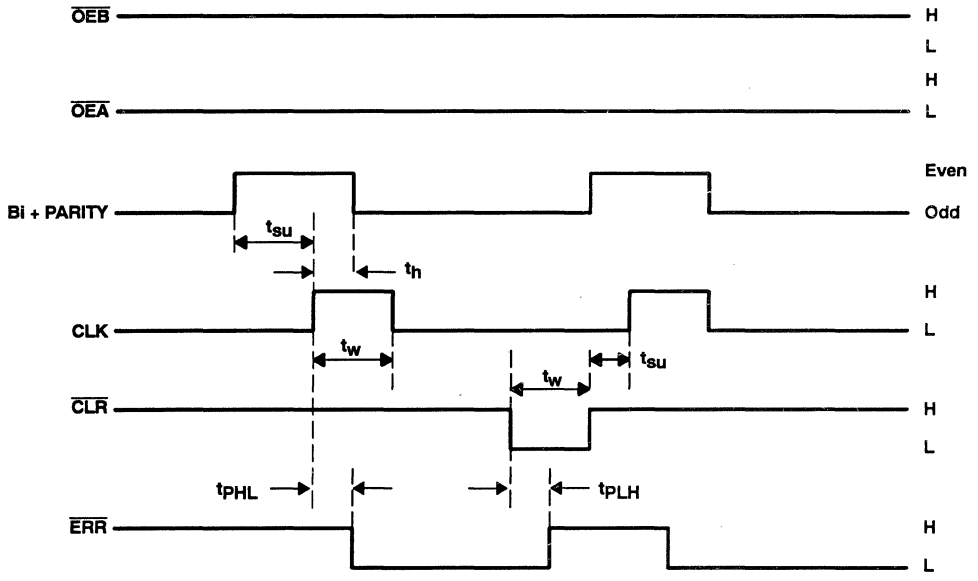


ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT P‡	$\overline{ERR}_{n-1}$†		
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point P.
‡ Location of point P is shown on local diagram.

timing waveforms, error flag



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
I_{OH}	$\overline{ERR}$	$V_O = V_{CC}$	5.5 V			0.5		5	μA
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	A or B ports	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	Control Inputs	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3.5				pF
C_{io}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5 V		11.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1 and timing waveforms)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	CLK high or low	4		4		ns
		$\overline{CLR}$ low	4		4		
t_{su}	Setup time before CLK↑	Bi + PARITY	7.5		7.5		ns
		$\overline{CLR}$ inactive	1.5		1.5		
t_h	Hold time, Bi + PARITY low after CLK↑		0		0		ns

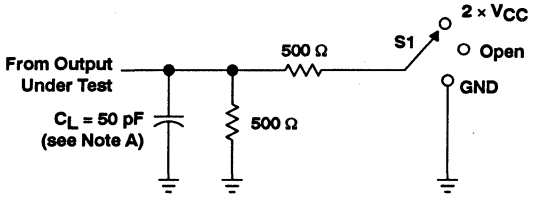
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1 and timing waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	4	7.2	9.2	4	10.4	ns
t_{PHL}			3.2	6.6	9.6	3.2	10.7	
t_{PLH}	A	PARITY	3.9	7.9	12	3.9	13.5	ns
t_{PHL}			4.2	8.3	12.4	4.2	13.8	
t_{PZH}	$\overline{OEB}$ or $\overline{OEA}$	A or B	3.1	6.7	10.1	3.1	11.2	ns
t_{PZL}			3.8	7.9	11.6	3.8	13	
t_{PHZ}	$\overline{OEB}$ or $\overline{OEA}$	A or B	5.5	7.8	10	5.5	10.8	ns
t_{PLZ}			5	7.1	9.3	5	10.1	
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	10.7	13.1	15.4	10.7	15.8	ns
t_{PHL}	CLK		4.6	7.8	10.3	4.6	11.6	
t_{PLH}	$\overline{OEA}$	PARITY	4	8	11.8	4	13.2	ns
t_{PHL}			4.3	8.5	12.3	4.3	13.6	
t_{PZH}	$\overline{OEB}$	PARITY	2.6	5.7	8.5	2.6	9.5	ns
t_{PZL}			3.4	6.8	9.8	3.4	10.7	
t_{PHZ}	$\overline{OEB}$	PARITY	5.6	7.9	9.5	5.6	10.2	ns
t_{PLZ}			5.1	7.2	9.1	5.1	9.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

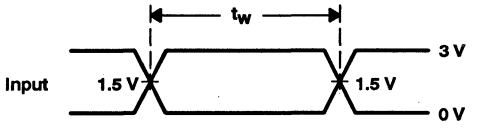
PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF, f = 1 MHz	64	pF
			B to A		72	
		Outputs disabled	A to B		6	
			B to A		10.5	

PARAMETER MEASUREMENT INFORMATION

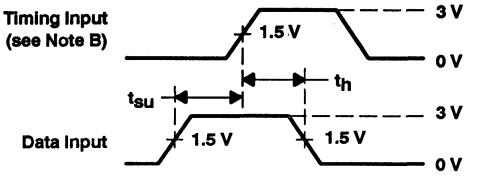


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

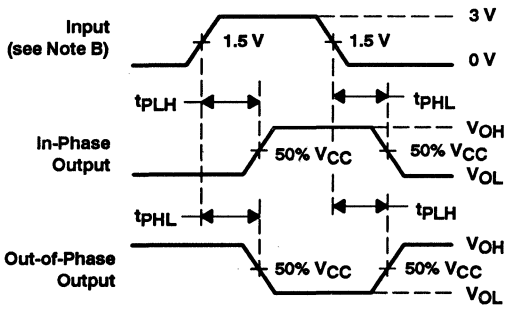
LOAD CIRCUIT



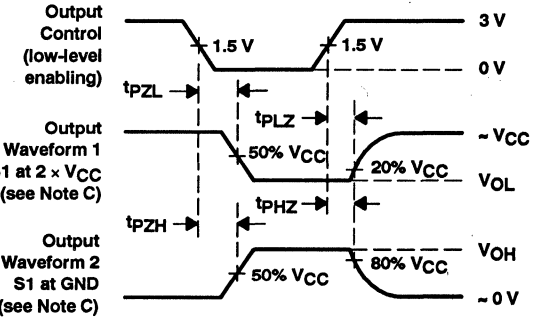
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



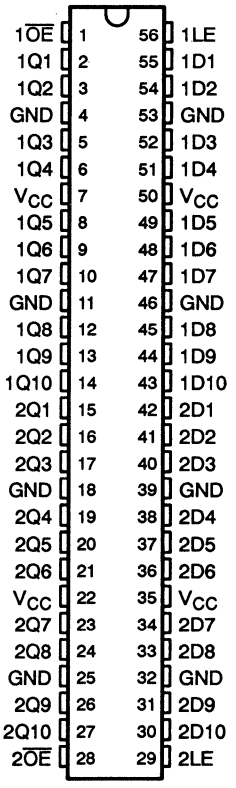
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Provide Extra Bus Driving/Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

This 20-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 74ACT16841 can be used as two 10-bit latches or one 20-bit latch. The twenty latches are transparent D-type. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT16841 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16841 is characterized for operation from −40°C to 85°C.

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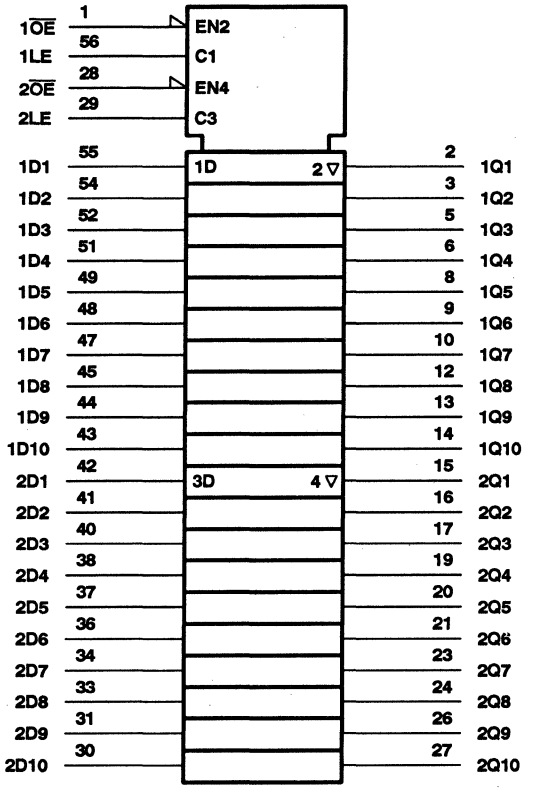
FUNCTION TABLE
(each 10-bit latch)

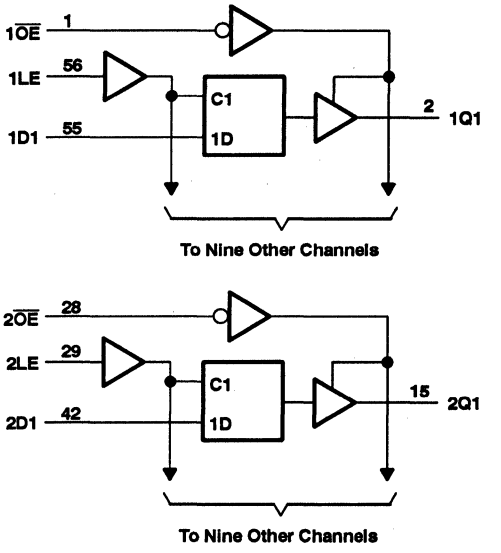
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3				pF
C_o	$V_O = V_{CC}$ or GND	5 V		11				pF

† No more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, LE high		4		4		ns
t_{su}	Setup time, data before LE↓		1.5		1.5		ns
t_h	Hold time, data after LE↓	High	3		3		ns
		Low	4.5		4.5		

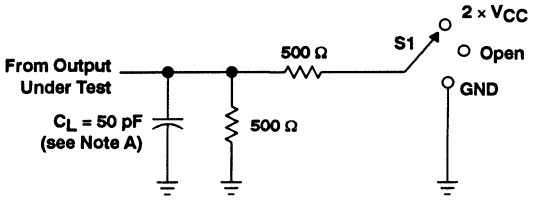
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	4	7.1	10.3	4	11.8	ns
t_{PHL}			3.2	6.9	11	3.2	12.2	
t_{PLH}	LE	Q	4.5	7.7	11.3	4.5	12.7	ns
t_{PHL}			4.3	7.8	11.4	4.3	12.7	
t_{PZH}	$\overline{OE}$	Q	3.1	6.4	10.1	3.1	11.3	ns
t_{PZL}			3.8	7.6	12.1	3.8	13.7	
t_{PHZ}	$\overline{OE}$	Q	4	7.3	9.5	4	10.2	ns
t_{PLZ}			4	6.8	8.9	4	9.6	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

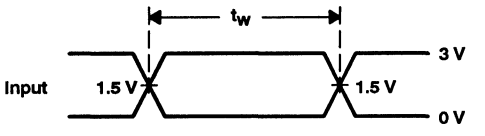
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 1 MHz	41	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

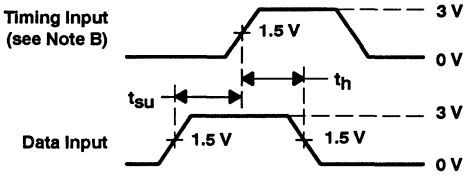


LOAD CIRCUIT

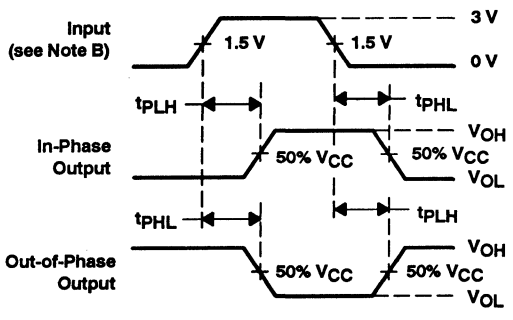
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



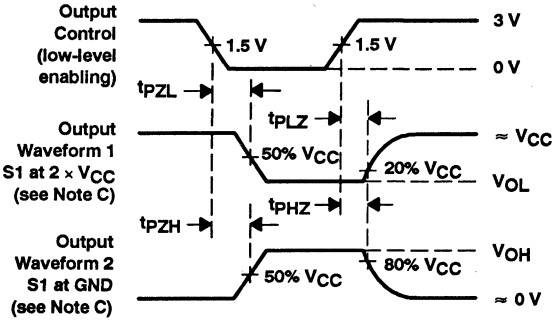
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



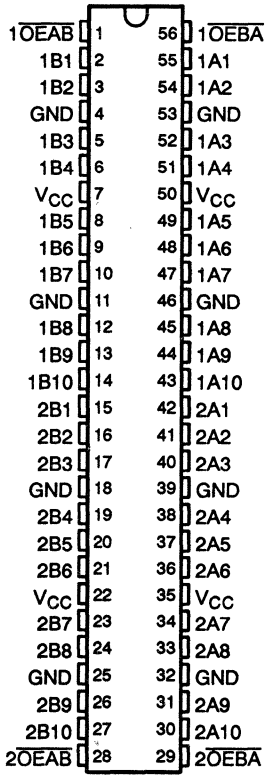
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16861 is a noninverting 20-bit transceiver designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 74ACT16861 can be used as two 10-bit transceivers or one 20-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The 74ACT16861 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

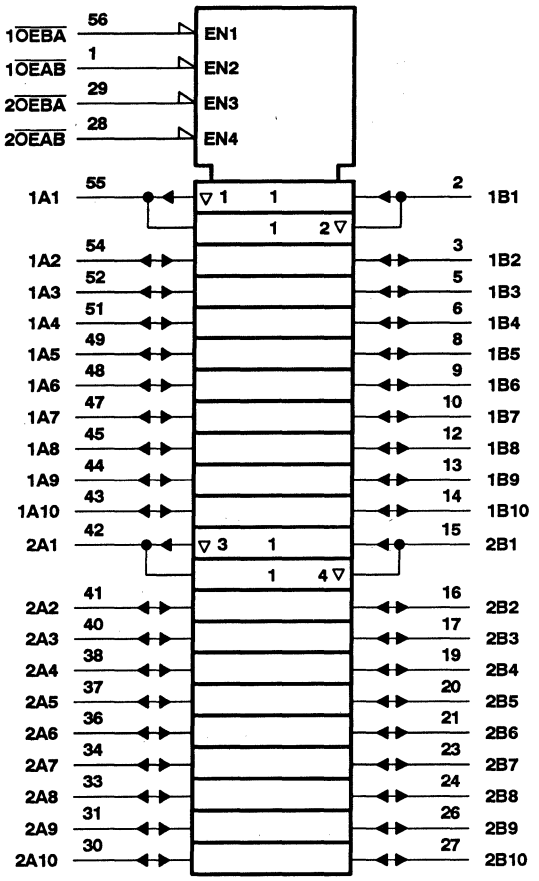
The 74ACT16861 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 10-bit section)

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	L	Latch A and B (A = B)
L	H	A to B
H	L	B to A
H	H	Isolation

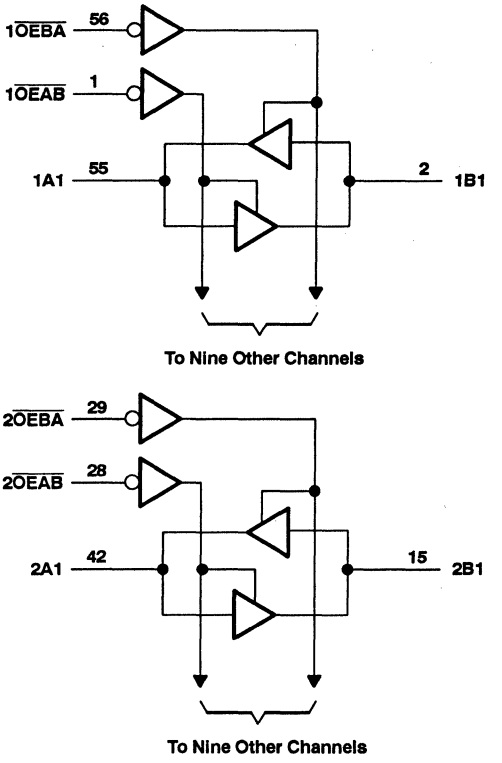
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±500 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = −24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		17				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

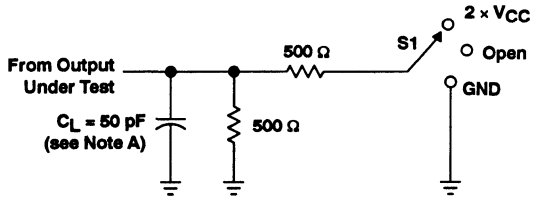
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.1	6.5	9.2	3.1	10.4	ns
t_{PHL}			2.9	7.5	10	2.9	11.1	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.4	6.6	9	2.4	10	ns
t_{PZL}			3.7	8.5	11.5	3.7	12.7	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.9	7.4	9.8	4.9	10.7	ns
t_{PLZ}			4.5	6.9	9.3	4.5	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

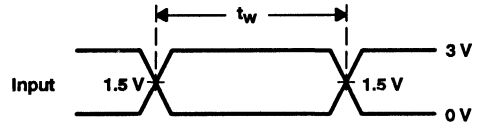
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	64	pF
		Outputs disabled		14	

PARAMETER MEASUREMENT INFORMATION

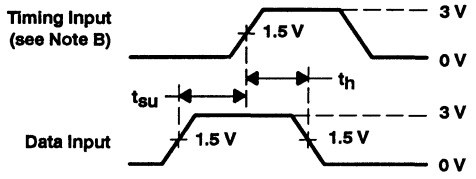


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

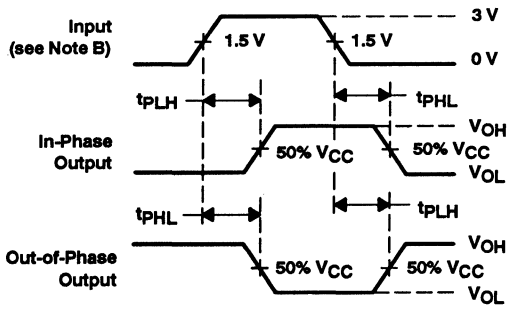
LOAD CIRCUIT



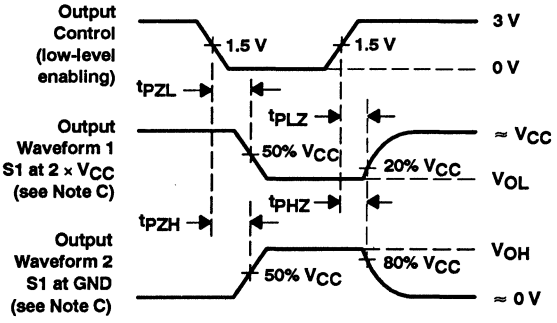
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



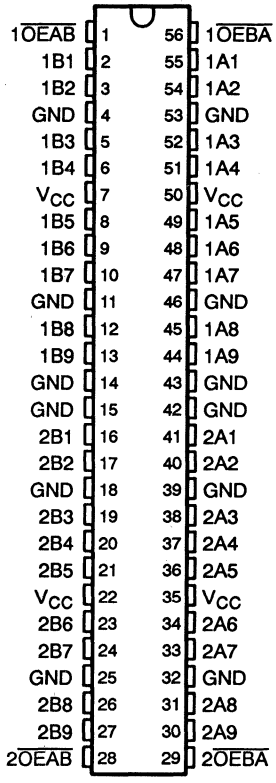
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

54ACT16863 . . . WD PACKAGE
74ACT16863 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16863 is an 18-bit noninverting transceiver designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 'ACT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs.

The 74ACT16863 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

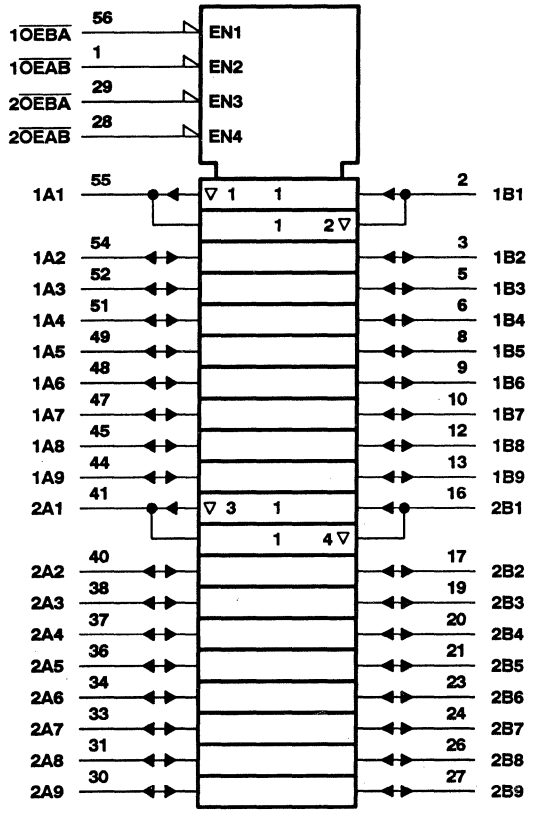
The 54ACT16863 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT16863 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

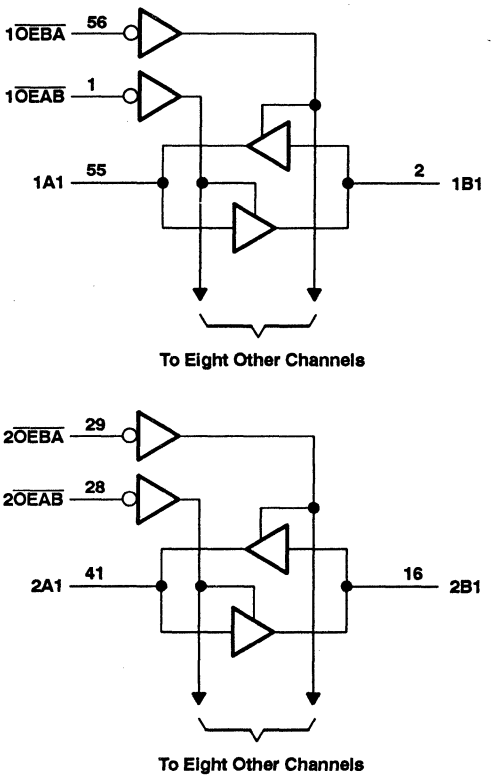
INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		54ACT16863			74ACT16863			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16863		74ACT16863		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}‡	A or B ports	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	V_I = V_{CC} or GND	5 V		4.5						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		17						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

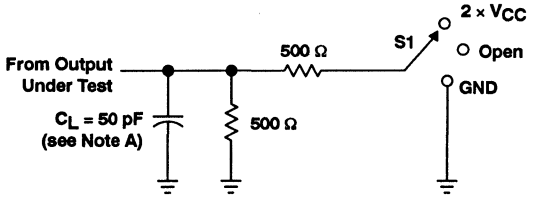
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16863		74ACT16863		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	4.1	7	9.9	4.1	12.1	4.1	11.1	ns
t_{PHL}			3.1	6.4	10.6	3.1	12.5	3.1	11.8	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3	5.9	9.6		11.5	3	10.6	ns
t_{PZL}			3.9	7.4	12.3	3.9	14.7	3.9	13.6	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	5.7	8.2	10.6	5.7	12.3	5.7	11.6	ns
t_{PLZ}			5.4	7.7	10	5.4	11.6	5.4	11	

PRODUCT PREVIEW

operating characteristics, V_{CC} = 5 V, T_A = 25°C

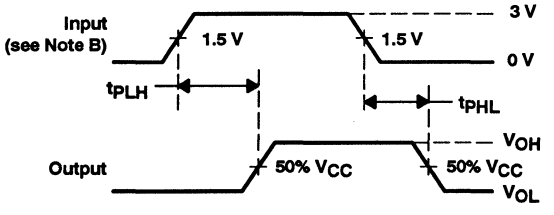
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	62	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

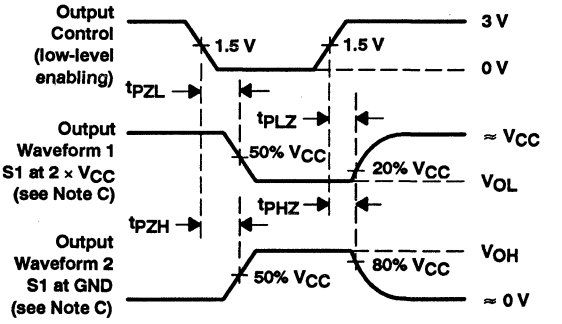


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
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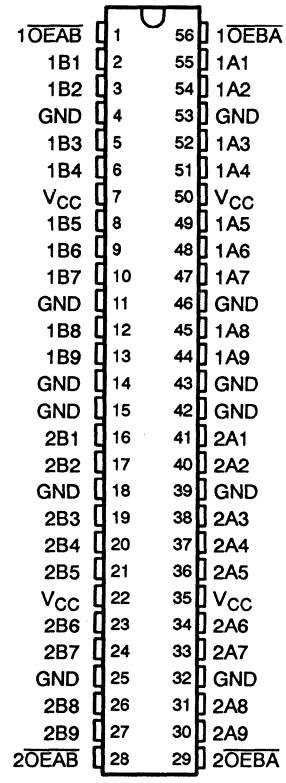
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 74ACT16864 is an 18-bit inverting transceiver designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

The 74ACT16864 can be used as two 9-bit transceivers or one 18-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs.

The 74ACT16864 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

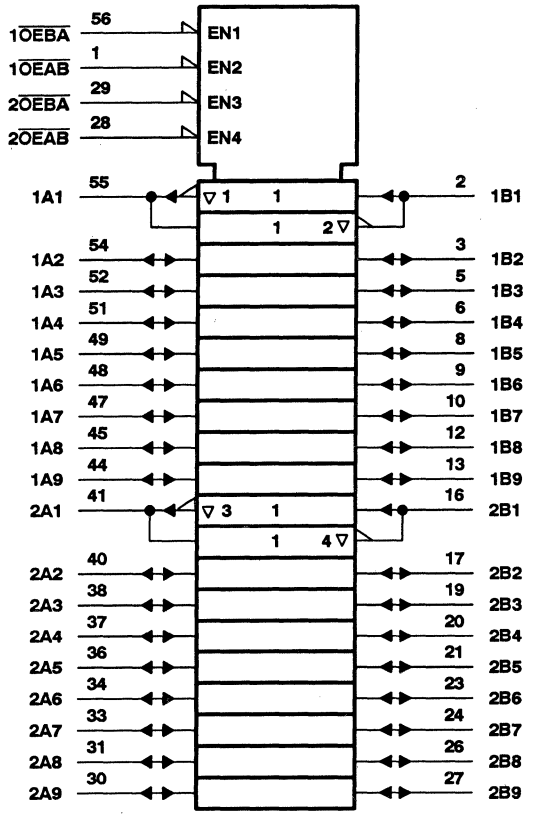
The 74ACT16864 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

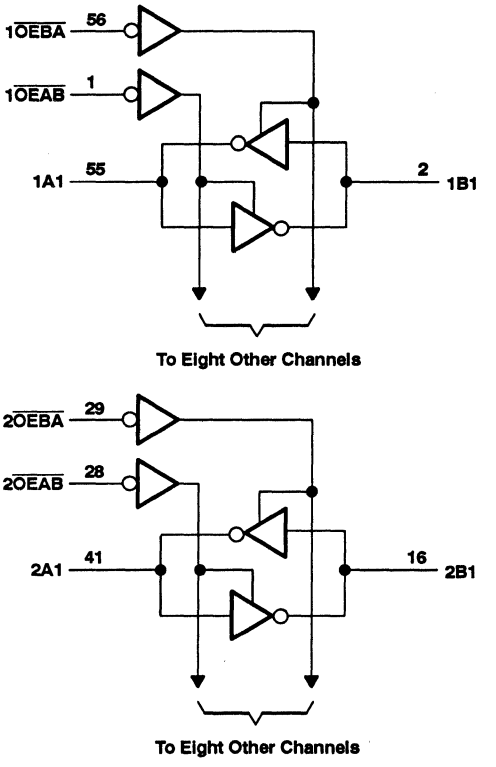
INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
H	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	H	Isolation

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		17				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

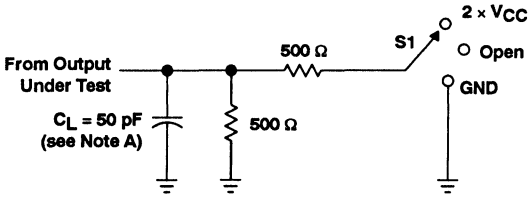
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.6	7	8.9	1.6	10.2	ns
t_{PHL}			3.7	8.1	10	3.7	11.3	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.2	8.2	10.1	2.2	11.1	ns
t_{PZL}			3.1	10.2	12.4	3.1	13.8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	5.1	8.6	10.1	5.1	10.8	ns
t_{PLZ}			5	8.3	9.7	5	10.3	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

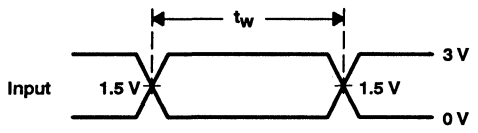
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	56	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

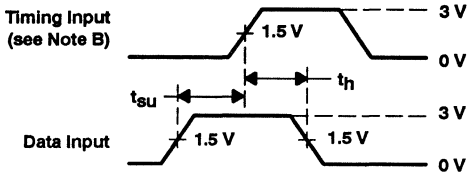


LOAD CIRCUIT

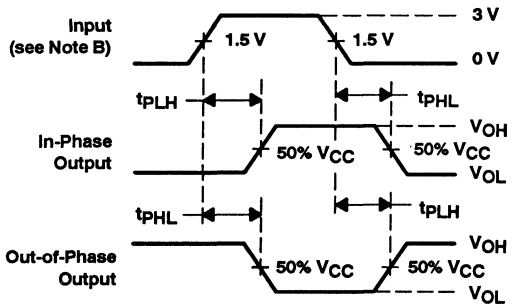
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



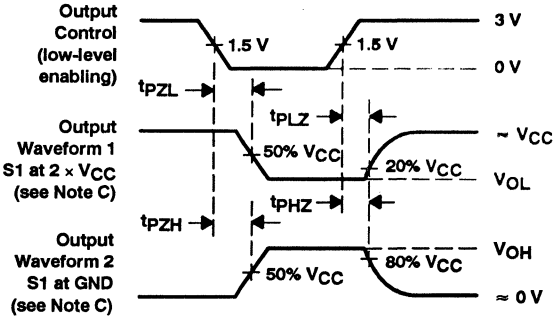
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



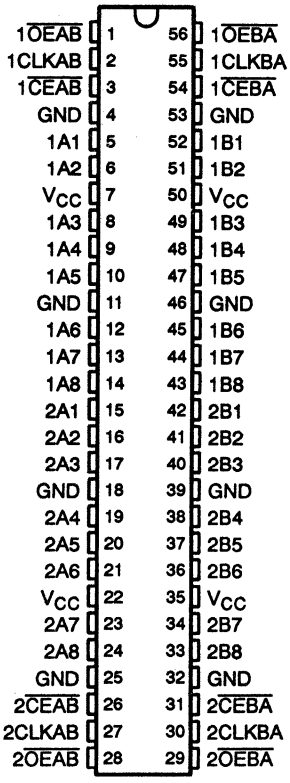
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- **Packaged in Plastic 300-mil Shrink Small-Outline Package Using 25-mil Center-to-Center Pin Spacings**
- **Inputs Are TTL-Voltage Compatible**
- **Noninverting Outputs**
- **Two 16-Bit, Back-to-Back Registers Store Data Flowing in Both Directions**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**

DL PACKAGE
(TOP VIEW)



description

The 'ACT16952 is a 16-bit registered transceiver that contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{CEAB}$ or $\overline{CEBA}$) input is low. Taking the output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) input low accesses the data on either port. To avoid false clocking of the flip-flops, $\overline{CEAB}$ (or $\overline{CEBA}$) should not be switched from low to high while CLKAB (or CLKBA) is low.

The 74ACT16952 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 74ACT16952 is characterized for operation from −40°C to 85°C.

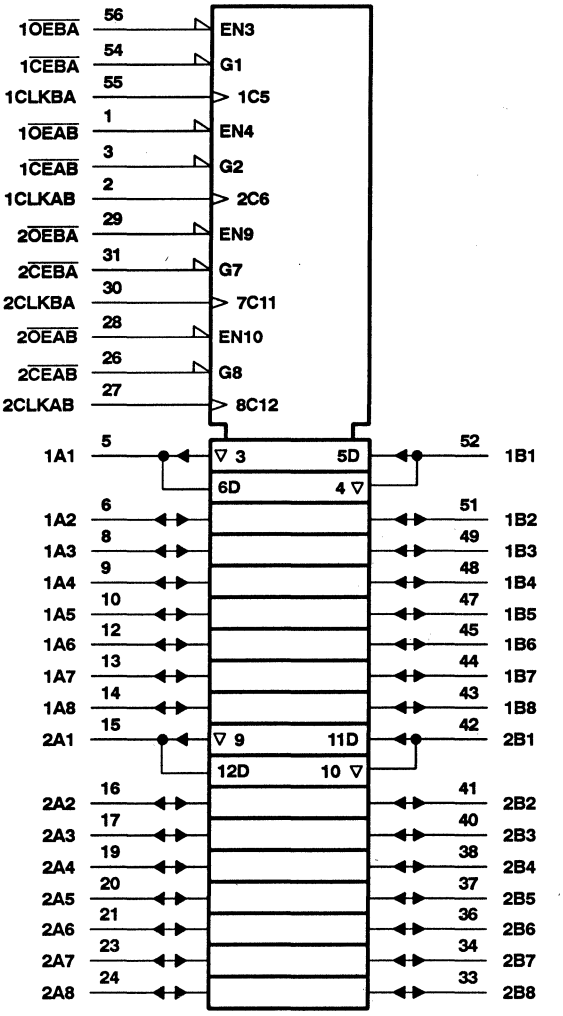
FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B_0‡
X	H	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

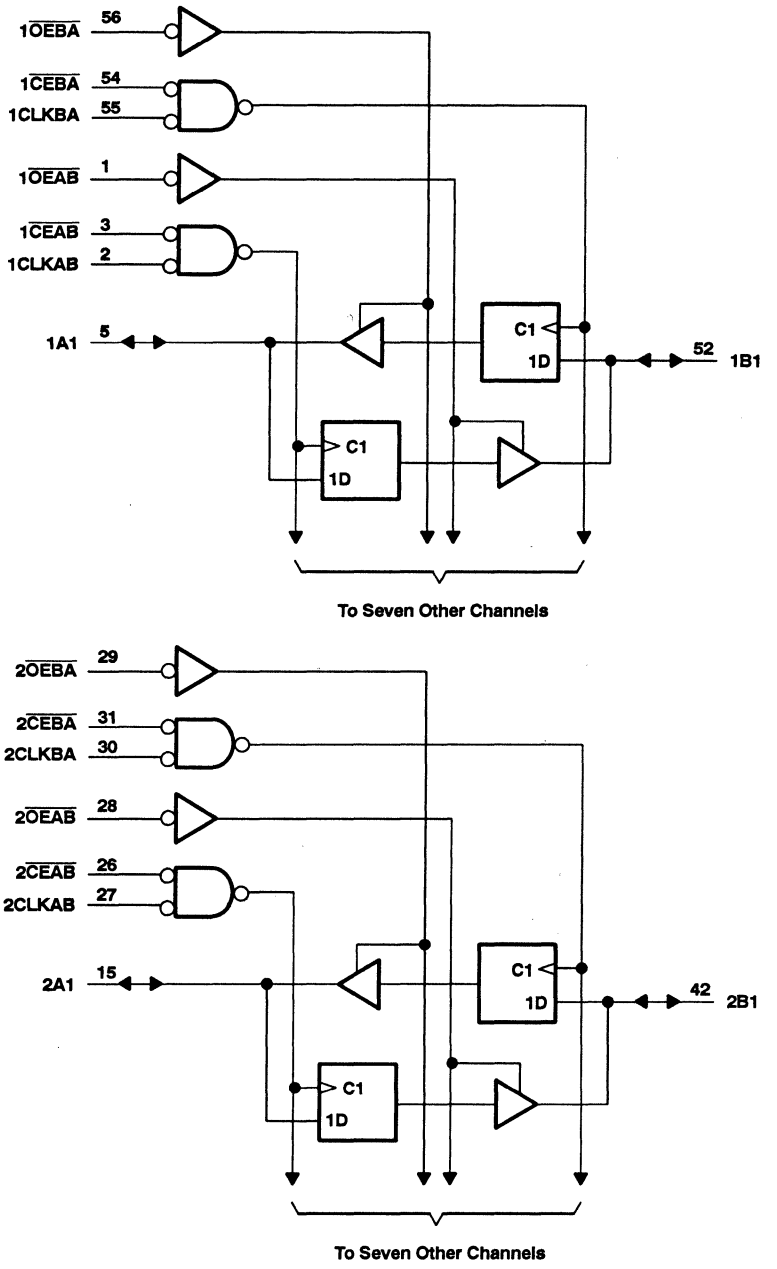
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = −50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = −24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I_{OH} = −50 mA†	5.5 V						
		I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
		I_{OL} = 50 mA†	5.5 V						
		I_{OL} = 75 mA†	5.5 V					1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 0.5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	75	0	75	MHz
t_w	Pulse duration, CLK high or low		6.7		6.7		ns
t_{su}	Setup time before CLK↑	Data	5		5		ns
		$\overline{CEAB}$ or $\overline{CEBA}$	6.5		6.5		
t_h	Hold time after CLK↑	Data	1		1		ns
		$\overline{CEAB}$ or $\overline{CEBA}$	0		0		

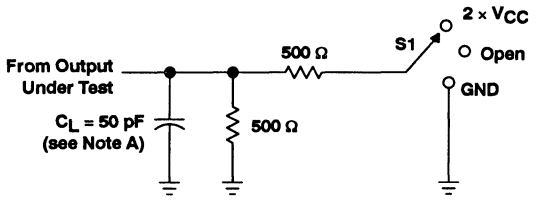
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75			75		MHz
t_{PLH}	CLK	A or B	4.7	8.5	10.7	4.7	11.8	ns
t_{PHL}			4.9	8.7	10.5	4.9	11.7	
t_{PLH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.7	8.5	10.7	4.7	11.8	ns
t_{PHL}			4.9	8.7	10.5	4.9	11.7	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.4	8.1	10.2	3.4	11.2	ns
t_{PZL}			4.2	9.6	11.8	4.2	13	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	5.2	7.5	8.9	5.2	9.4	ns
t_{PLZ}			4.5	6.7	8.2	4.5	8.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

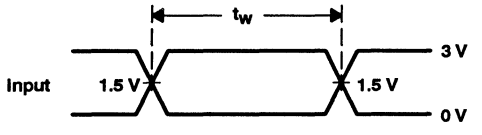
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	55	pF
		Outputs disabled		34	

PARAMETER MEASUREMENT INFORMATION

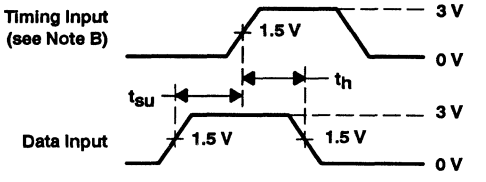


LOAD CIRCUIT

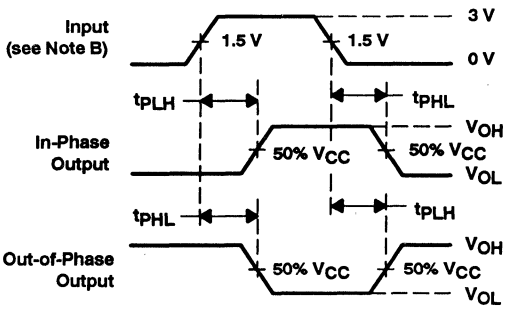
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



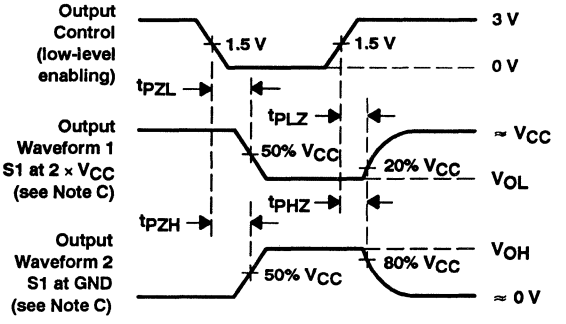
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

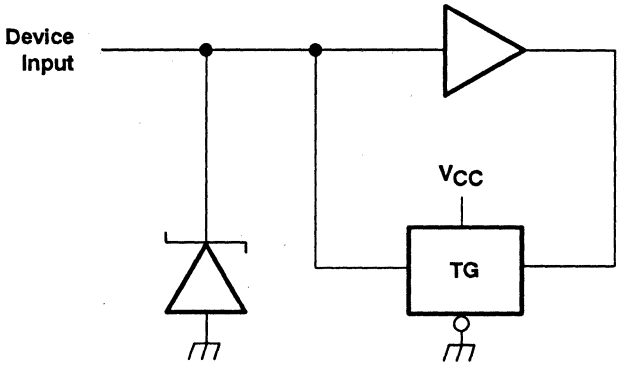
Figure 1. Load Circuit and Voltage Waveforms

ADVANCED TERMINATIONS

'ACT1071, 'ACT1073
BUS-HOLD DEVICES

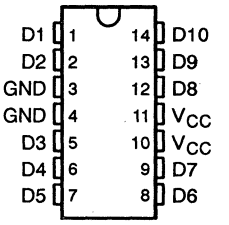
Features

- Holds Inputs at Valid Logic Level During 3-State Operation
- Effective Alternative to Pullup Resistors
- Maintains Last-Known State on Bus Line
- Does Not Load Down the Driving Output
- Schottky Diode Clamps to Ground
- Reduced Undershoot, Overshoot and Ringing
- SN741071DW 12-Bit Bus Holder With Clamp-to-Ground
- SN741073DW 16-Bit Bus Holder With Clamp-to-Ground



- **Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems**
- **Reduces Undershoot and Overshoot Caused By Line Reflections**
- **Repetitive Peak Forward Current . . . I_{FRM} = 100 mA**
- **Inputs Are TTL-Voltage Compatible**
- **Low Power Consumption (Like CMOS)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**

D PACKAGE
(TOP VIEW)



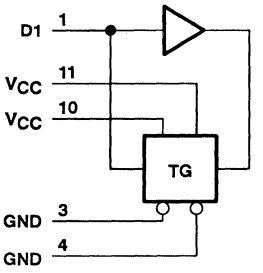
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1071 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1071 is characterized for operation from –40°C to 85°C.

logic diagram, one of ten channels (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Continuous input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Positive-peak input clamp current, I_{IK} (V_I > V_{CC}) (t_w < 1 µs, duty cycle < 20%) ..... 100 mA
Negative-peak input clamp current, I_{IK} (V_I < 0) (t_w < 1 µs, duty cycle < 20%) ..... −100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TA = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
I_{IL}	V_{CC} = 4.5 to 5.5 V,	V_I = 0.8 V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	V_{CC} = 4.5 to 5.5 V,	V_I = 2.5 V	−0.2	−0.5	−1.4	−0.15	−1.5	mA
V_{IKL}	I_{IN} = −18 mA				−1.5		−1.5	V
V_{IKH}	I_{IN} = 18 mA				V_{CC}+2		V_{CC}+2	V
I_{CC}‡	V_{CC} = 5.5 V,	Inputs open			4		40	µA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at V_{CC} or GND			0.9		1	mA
C_i	V_I = V_{CC} or GND			3				pF

† All typical values are at V_{CC} = 5 V.
‡ Inputs may be set high or low prior to the I_{CC} measurement.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

TYPICAL CHARACTERISTICS

FORWARD CURRENT
vs
INPUT VOLTAGE
(UPPER CLAMPING DIODE)

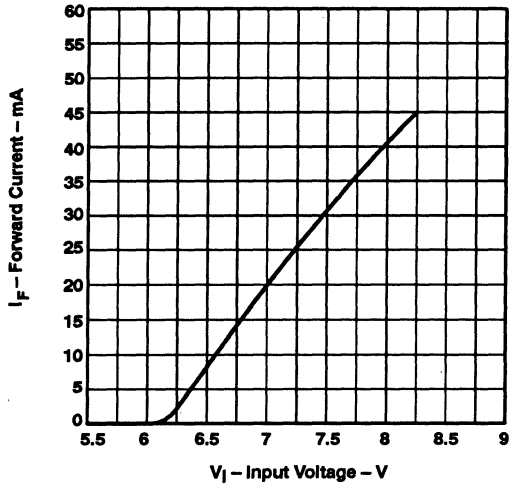


Figure 1

FORWARD CURRENT
vs
INPUT VOLTAGE
(LOWER CLAMPING DIODE)

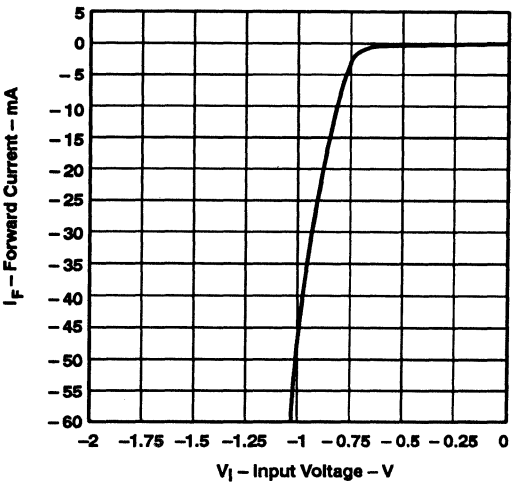


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE

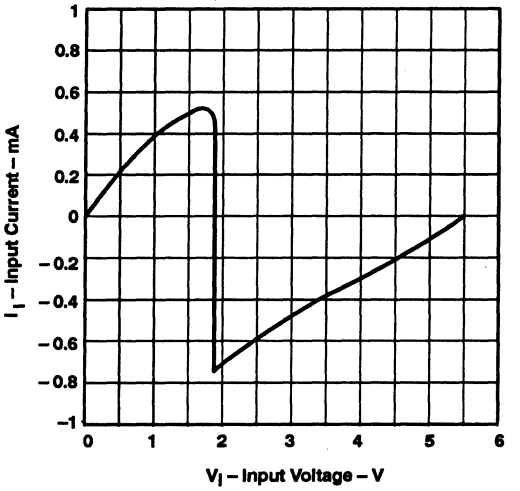


Figure 3

SUPPLY CURRENT
vs
INPUT VOLTAGE

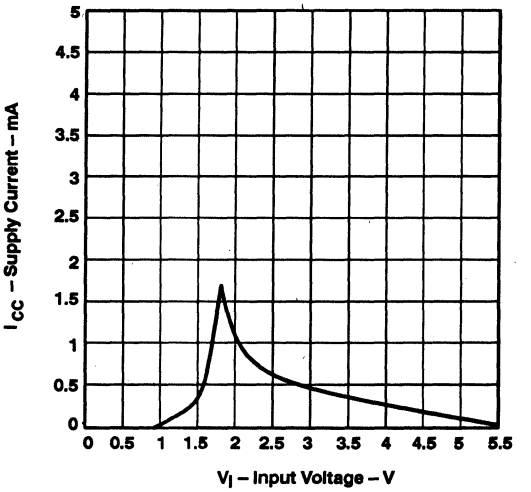


Figure 4

APPLICATION INFORMATION

The SN74ACT1071 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

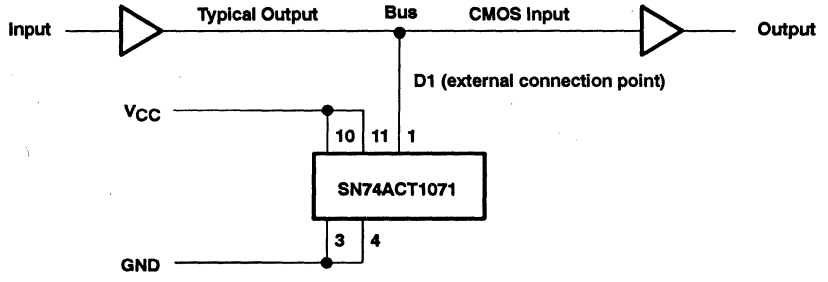
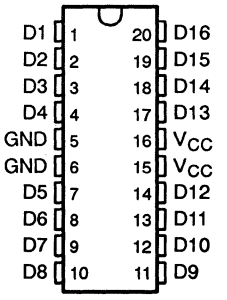


Figure 5. Bus-Hold Application

- **Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems**
- **Reduces Undershoot and Overshoot Caused By Line Reflections**
- **Repetitive Peak Forward Current . . . I_{FRM} = 100 mA**
- **Inputs Are TTL-Voltage Compatible**
- **Low Power Consumption (Like CMOS)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise**

DW PACKAGE
(TOP VIEW)



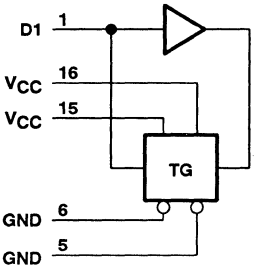
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1073 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1073 is characterized for operation from −40°C to 85°C.

logic diagram, one of sixteen channels (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Continuous input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Positive-peak input clamp current, I_{IK} (V_I > V_{CC}) (t_w < 1 μs, duty cycle < 20%) ..... 100 mA
Negative-peak input clamp current, I_{IK} (V_I < 0) (t_w < 1 μs, duty cycle < 20%) ..... −100 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TA = 25°C			MIN	MAX	UNIT
			MIN	TYP†	MAX			
I_{IL}	V_{CC} = 4.5 to 5.5 V,	V_I = 0.8 V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	V_{CC} = 4.5 to 5.5 V,	V_I = 2.5 V	−0.2	−0.5	−1.4	−0.15	−1.5	mA
V_{IKL}	I_{IN} = −18 mA				−1.5		−1.5	V
V_{IKH}	I_{IN} = 18 mA				V_{CC}+2		V_{CC}+2	V
I_{CC}‡	V_{CC} = 5.5 V,	Inputs open			4		40	μA
ΔI_{CC}§	One input at 3.4 V,	Other inputs at V_{CC} or GND			0.9		1	mA
C_i	V_I = V_{CC} or GND			3				pF

† All typical values are at V_{CC} = 5 V.
‡ Inputs may be set high or low prior to the I_{CC} measurement.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

TYPICAL CHARACTERISTICS

FORWARD CURRENT
vs
INPUT VOLTAGE
(UPPER CLAMPING DIODE)

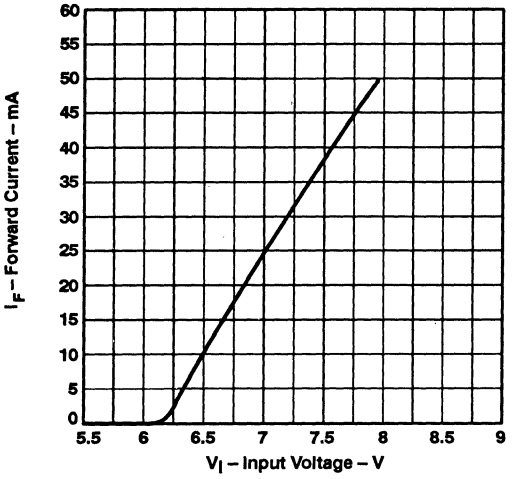


Figure 1

FORWARD CURRENT
vs
INPUT VOLTAGE
(LOWER CLAMPING DIODE)

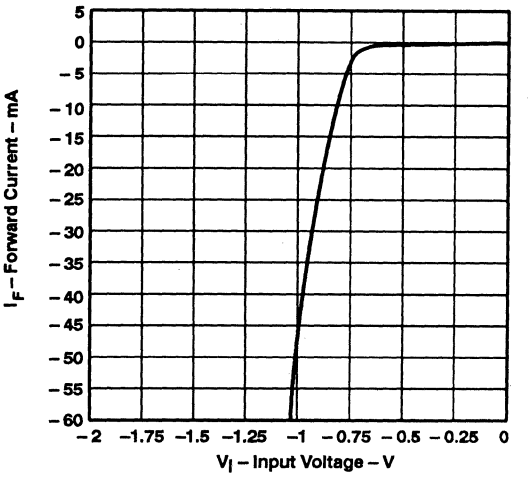


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE

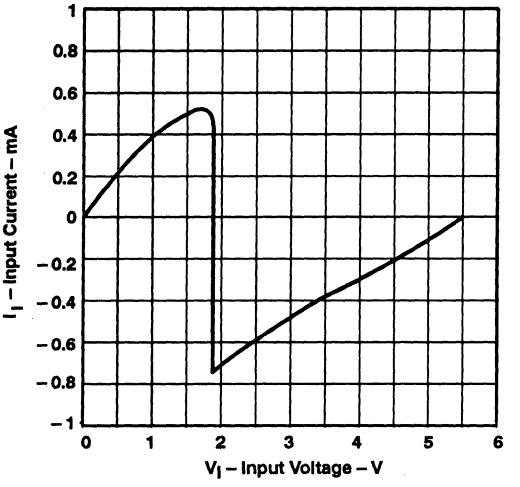


Figure 3

SUPPLY CURRENT
vs
INPUT VOLTAGE

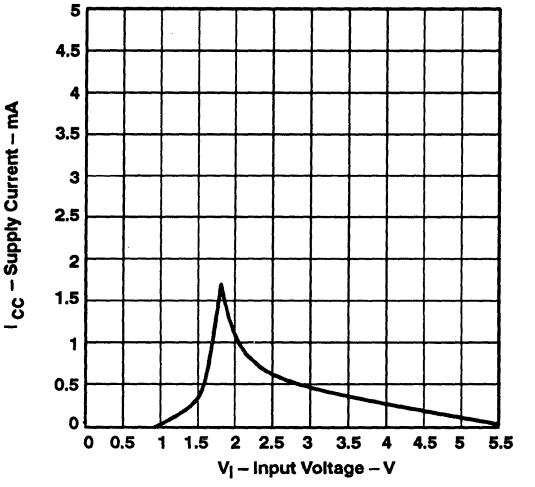


Figure 4

APPLICATION INFORMATION

The SN74ACT1073 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

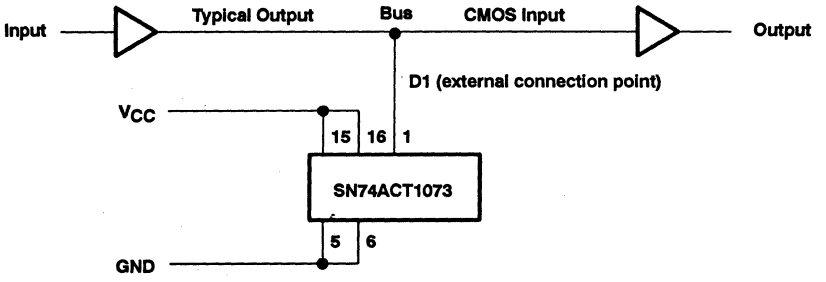


Figure 5. Bus-Hold Application

CROSSBAR SWITCH TECHNOLOGY (CBT)

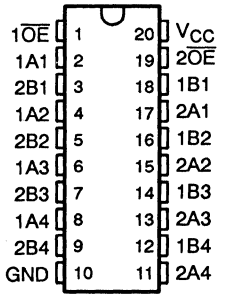
Features

- Simple FET Switches
- Very Low On-State Resistance r_{on} (4–6 Ω)
- Reduced Input Capacitance C_i (6–8 pF)
- Industry Standard Pinouts
- Widebus™ Functions
- Advanced Packaging Options (SSOP, TSSOP)
- Near-Zero Propagation Delay

NOVEMBER 1992 – REVISED APRIL 1993

- **Space-Saving Package Option: Shrink Small-Outline Package Features EIAJ 0.65-mm Lead Pitch**
- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Standard '244-Type Pinout**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3244 provides 8 bits of high-speed TTL-compatible bus switching in a standard '244 pinout. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device is organized as two 4-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

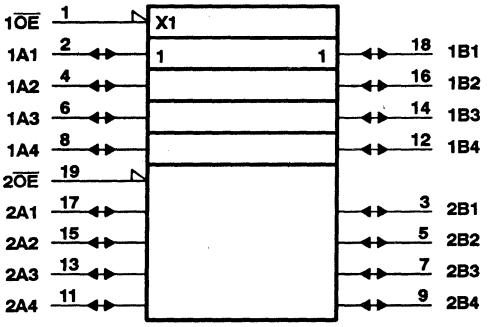
The SN74CBT3244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

$\overline{OE1}$	$\overline{OE2}$	B1–B4	B5–B8	FUNCTION
L	L	A1–A4	A5–A8	Connect
L	H	A1–A4	Z	Connect
H	L	Z	A5–A8	Connect
H	H	Z	Z	Disconnect

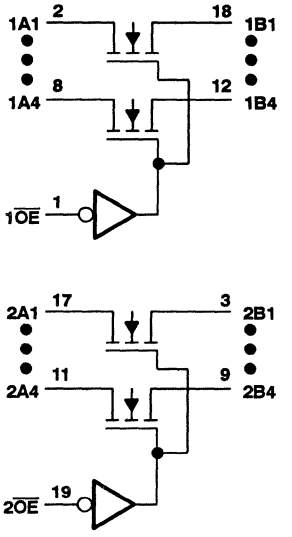
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.5 W
DW package ..... 0.85 W
NT package ..... 1.3 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

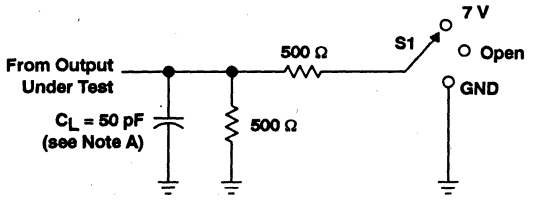
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}¶	A or B	B or A				0.25	ns
t_{PHL}¶						0.25	
t_{PZH}	$\overline{OE}$	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	$\overline{OE}$	Y			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

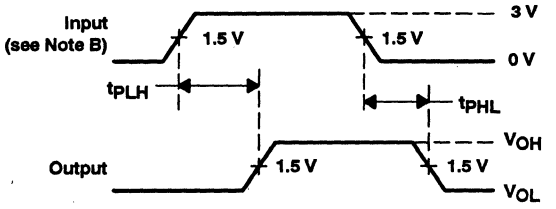
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

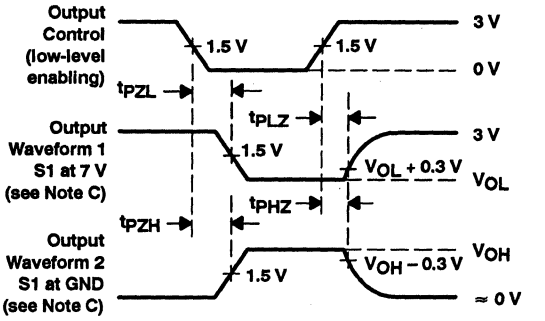


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

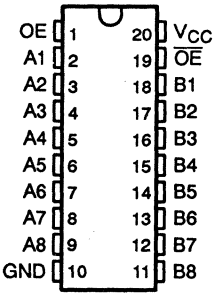
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

NOVEMBER 1992 – REVISED APRIL 1993

- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Standard '245-Type Pinout**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

NT, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3245 provides 8 bits of high-speed TTL-compatible bus switching in a standard '245 pinout. The low on-state resistance of the switch allows connections to be made while adding near-zero propagation delay.

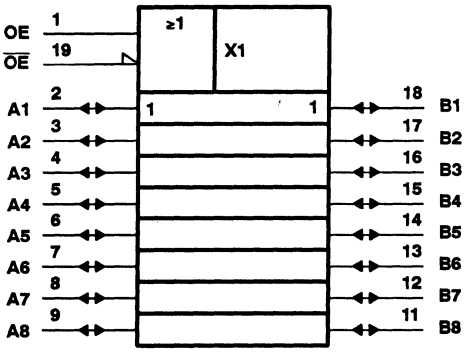
The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{OE}$) inputs. When $\overline{OE}$ is low or OE is high, the switch is on and port A is connected to port B. When $\overline{OE}$ is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

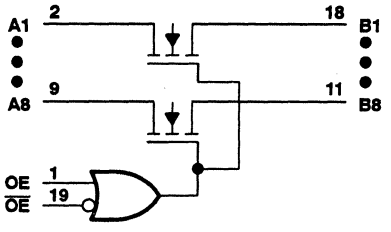
OE	$\overline{OE}$	B1–B8	FUNCTION
X	L	A1–A8	Connect
H	X	A1–A8	Connect
L	H	Z	Disconnect

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): PW package ..... 0.5 W
DW package ..... 0.85 W
NT package ..... 1.3 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

PRODUCT PREVIEW

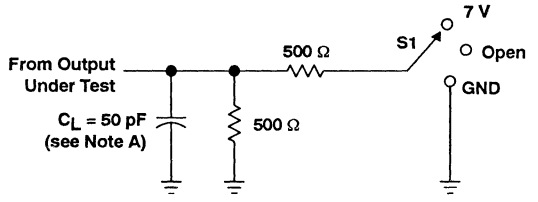
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PZH}	$\overline{OE}$ or OE	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	$\overline{OE}$ or OE	Y			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

† This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

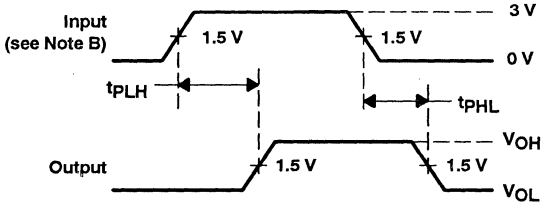
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

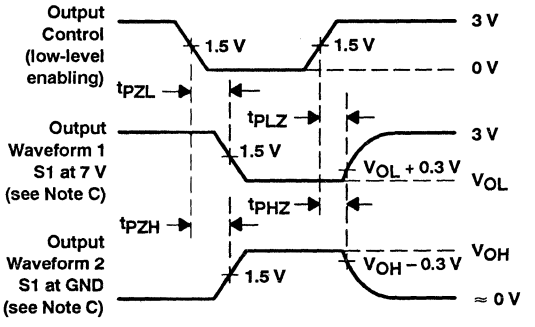


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

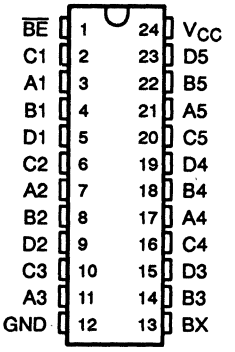
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

NOVEMBER 1992 – REVISED APRIL 1993

- **Space-Saving Package Option: Shrink Small-Outline Package Features EIAJ 0.65-mm Lead Pitch**
- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3383 provides 10 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides data exchanging of the AB and CD pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when $\overline{BE}$ is low.

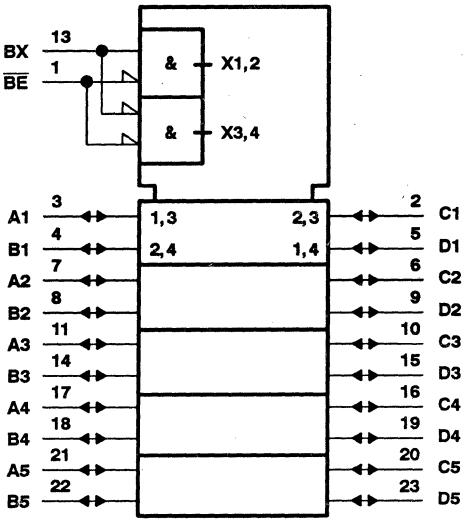
The SN74CBT3383 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3383 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

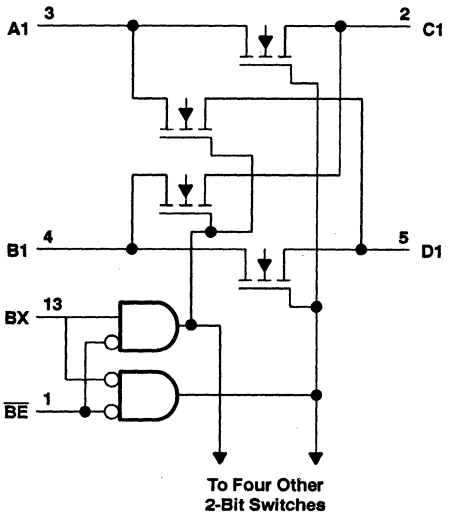
$\overline{BE}$	BX	A1–A5	B1–B5	FUNCTION
L	L	C1–C5	D1–D5	Connect
L	H	D1–D5	C1–C5	Exchange
H	X	Z	Z	Disconnect

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.5 W
DW package ..... 0.85 W
NT package ..... 1.3 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

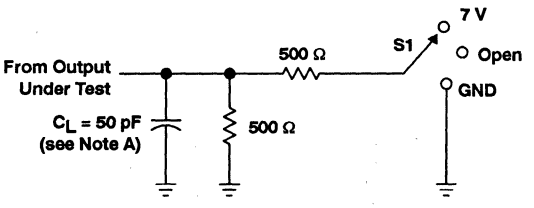
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}¶	A or B	B or A				0.25	ns
t_{PHL}¶						0.25	
t_{PLH}	BX	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	$\overline{BE}$	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	$\overline{BE}$	Y			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

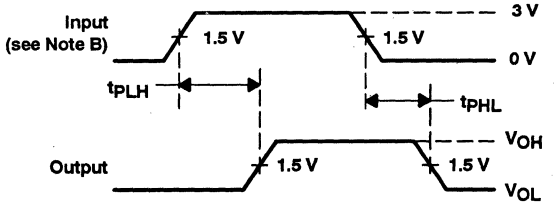
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

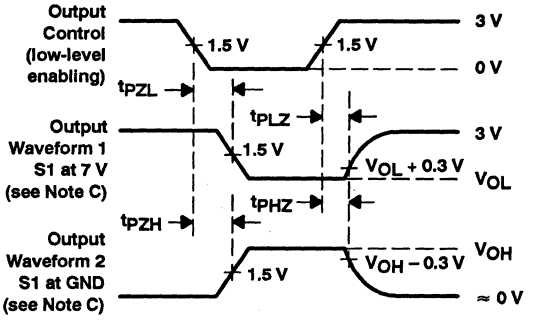


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

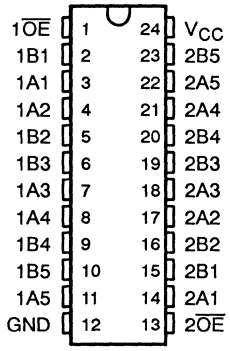
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

NOVEMBER 1992 – REVISED APRIL 1993

- **Space-Saving Package Option: Shrink Small-Outline Package Features EIAJ 0.65-mm Lead Pitch**
- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3384 provides 10 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device is organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

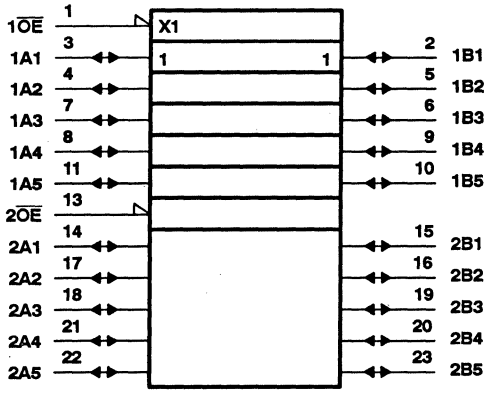
The SN74CBT3384 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

$\overline{OE1}$	$\overline{OE2}$	B1–B5	B6–B10	FUNCTION
L	L	A1–A5	A6–A10	Connect
L	H	A1–A5	Z	Connect
H	L	Z	A6–A10	Connect
H	H	Z	Z	Disconnect

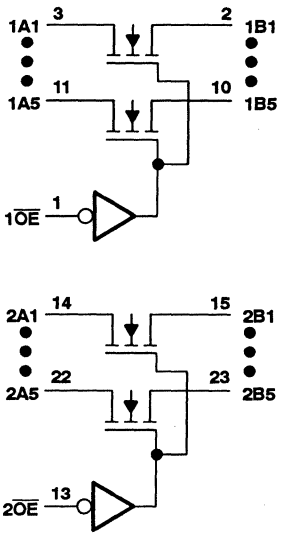
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package ..... 0.5 W
DW package ..... 0.85 W
NT package ..... 1.3 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

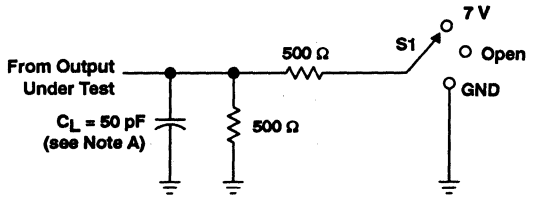
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}¶	A or B	B or A				0.25	ns
t_{PHL}¶						0.25	
t_{PZH}	$\overline{OE}$	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	$\overline{OE}$	Y			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

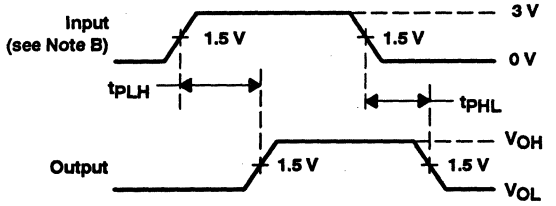
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

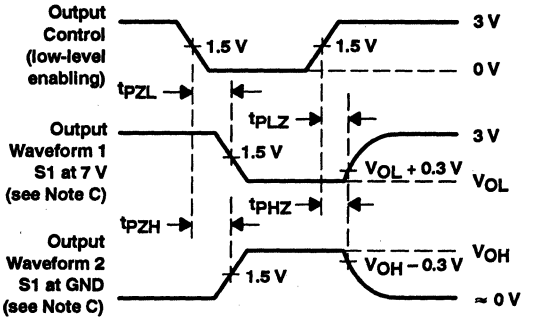


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

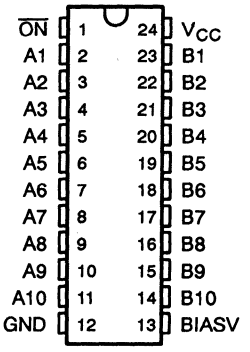
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Package Options Include Plastic DIP Packages and Small-Outline and Thin Shrink Small-Outline Packages**

DW, NT, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800 provides 10 bits of high-speed TTL-compatible bus switches. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

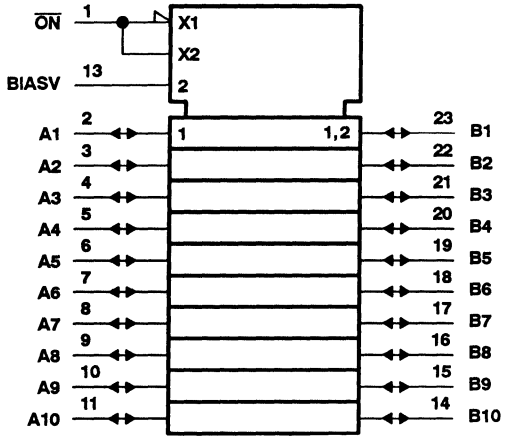
The SN74CBT6800 is organized as one 10-bit switch bank with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open and the B port is precharged to the BIASV voltage through the equivalent of a 10-kΩ resistor.

The SN74CBT6800 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

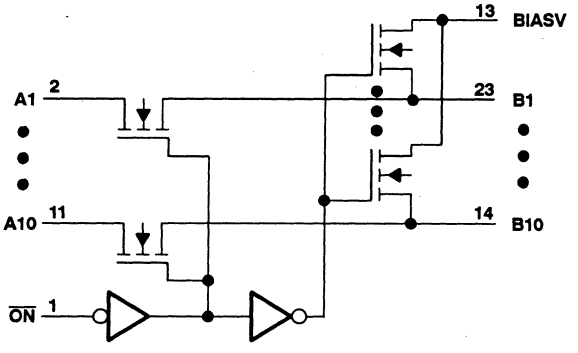
$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Bias voltage range, BIASV ..... −0.5 V to V_{CC} V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DW package ..... 0.85 W
NT package ..... 1.3 W
PW package ..... 0.5 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
BIASV	Supply voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O= 0	0.25			mA
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}§		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}¶		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O = 0	0.25			mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

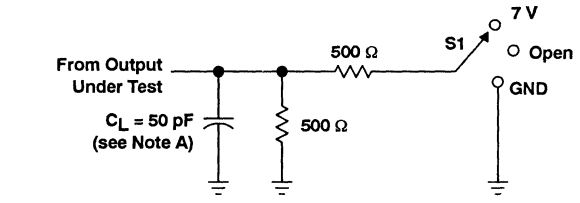
PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PZH}‡	$\overline{ON}$	A or B			1.5	7.5	ns
t_{PZL}§					1.5	7.5	
t_{PHZ}‡	$\overline{ON}$	A or B			1.5	6.5	ns
t_{PLZ}§					1.5	6.5	

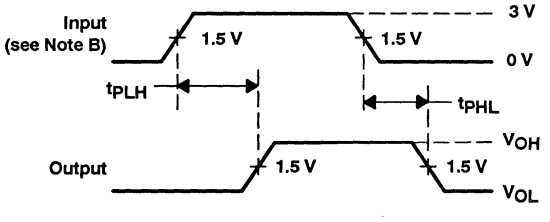
† This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.
‡ BIASV = GND
§ BIASV = 3 V

PARAMETER MEASUREMENT INFORMATION

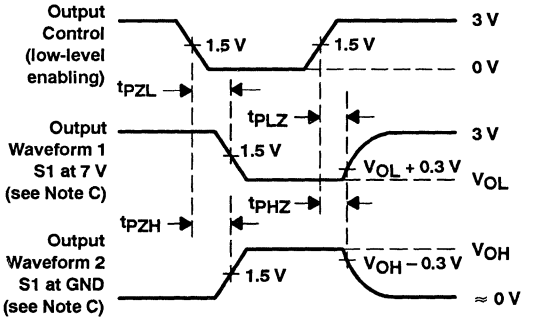


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

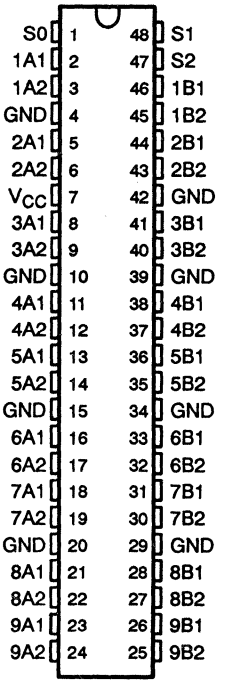
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

NOVEMBER 1992 – REVISED APRIL 1993

- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74CBT16209 provides 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device operates as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports using the data-select inputs (S0–S2).

The SN74CBT16209 is characterized for operation from −40°C to 85°C.

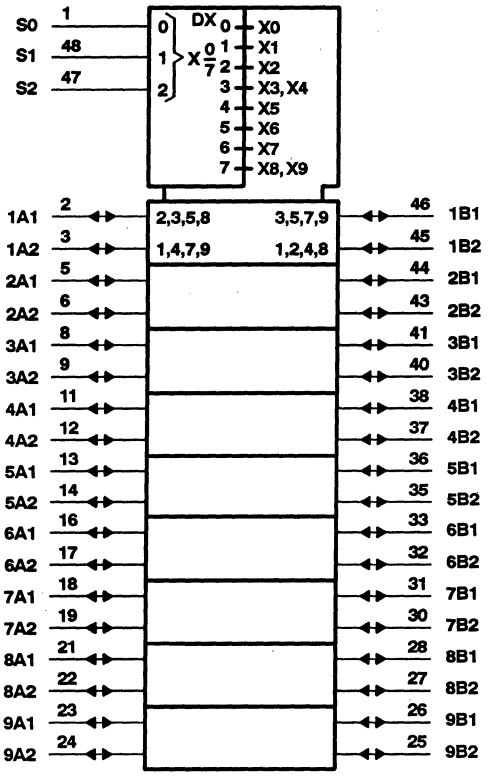
FUNCTION TABLE

FLOW CONTROL			OUTPUTS		FUNCTION
S0	S1	S2	A1	A2	
L	L	L	Z	Z	Disconnect
H	L	L	Z	B2	A2 to B2
L	H	L	B2	Z	A1 to B2
H	H	L	B1	B2	A1 to B1, A2 to B2
L	L	H	B1	Z	A1 to B1
H	L	H	Z	Z	Disconnect
L	H	H	Z	B1	A2 to B1
H	H	H	B2	B1	A1 to B2, A2 to B1

PRODUCT PREVIEW

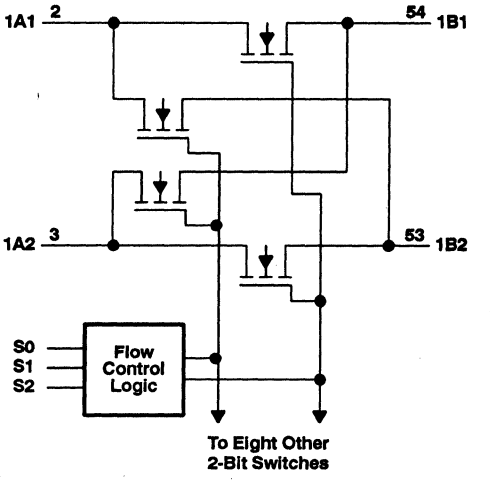
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.6 W
DL package ..... 0.85 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower of the voltages of the two (A or B) pins.

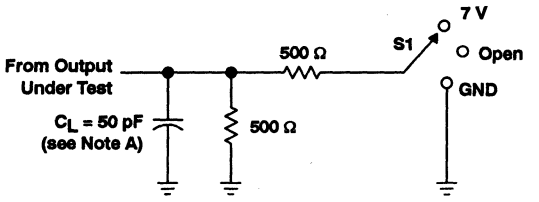
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}¶	A or B	B or A				0.25	ns
t_{PHL}¶						0.25	
t_{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	S0, S1, S2	A or B			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

¶ This parameter is characterized but not tested. This propagation delay is due to the RC delay of the on-state resistance of the switch and the load capacitance.

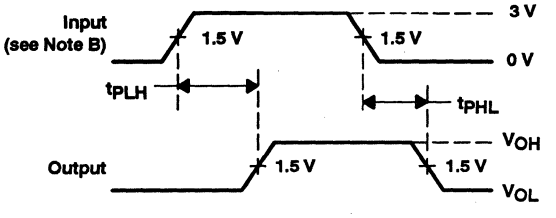
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

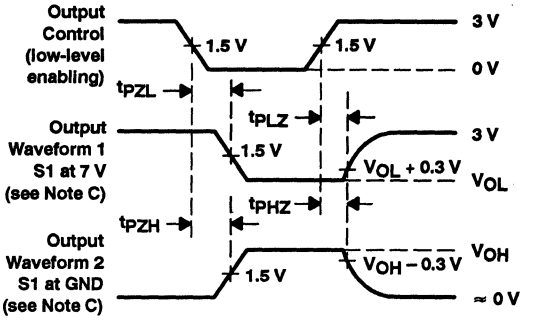


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

NOVEMBER 1992 – REVISED APRIL 1993

- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic 300-mil Shrink Small-Outline and Thin Shrink Small-Outline Packages**

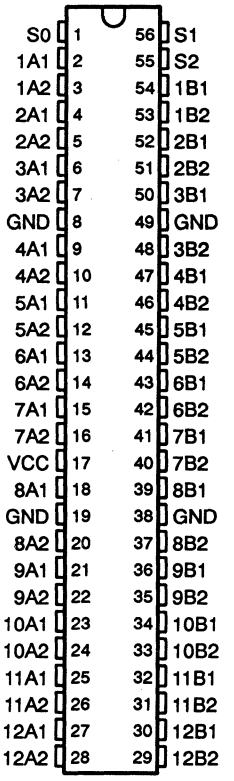
description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports, via the data-select pins (S0–S2).

The SN74CBT16212 is characterized for operation from −40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



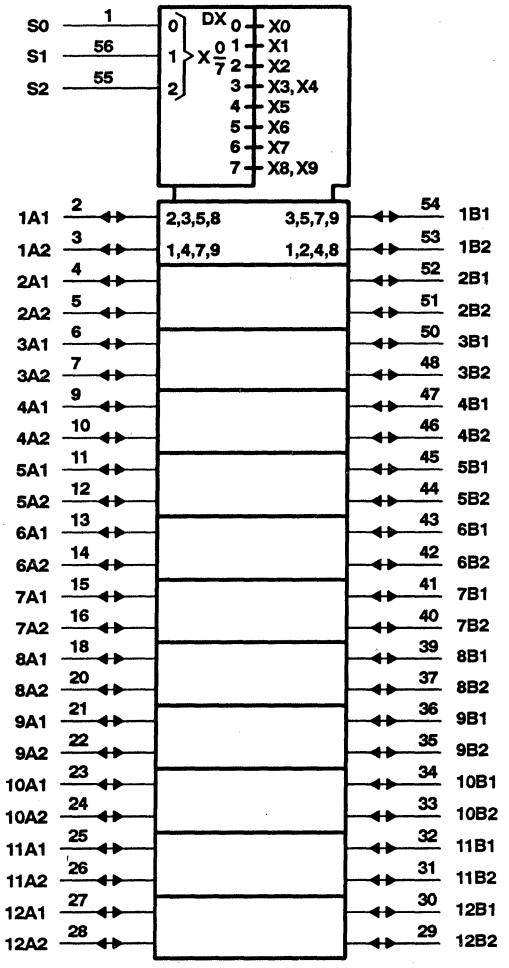
FUNCTION TABLE

FLOW CONTROL			OUTPUTS		FUNCTION
S0	S1	S2	A1	A2	
L	L	L	Z	Z	Disconnect
H	L	L	Z	B2	A2 to B2
L	H	L	B2	Z	A1 to B2
H	H	L	B1	B2	A1 to B1, A2 to B2
L	L	H	B1	Z	A1 to B1
H	L	H	Z	Z	Disconnect
L	H	H	Z	B1	A2 to B1
H	H	H	B2	B1	A1 to B2, A2 to B1

PRODUCT PREVIEW

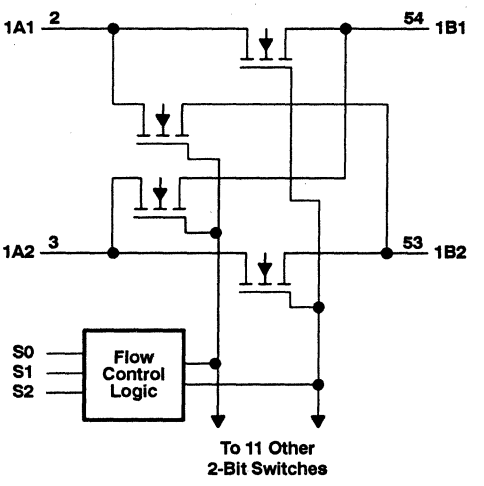
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Current into any pin, I_O ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 0.7 W
DL package ..... 1 W
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V	100			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			0.2	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{o(ON)}$		V_O = 3 V or 0,	Switch on			8		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA			6	Ω
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance (r_{on}) is determined by the lower between the A or B pins.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = −40°C TO 85°C		T_A = 0°C TO 70°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}†	A or B	B or A				0.25	ns
t_{PHL}†						0.25	
t_{PLH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PHL}					1.5	7.5	
t_{PZH}	S0, S1, S2	A or B			1.5	7.5	ns
t_{PZL}					1.5	7.5	
t_{PHZ}	S0, S1, S2	A or B			1.5	6.5	ns
t_{PLZ}					1.5	6.5	

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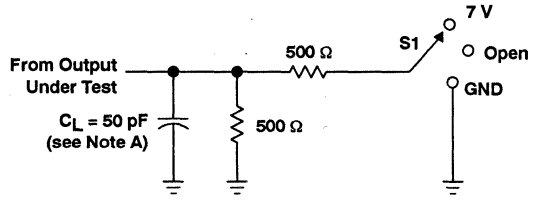
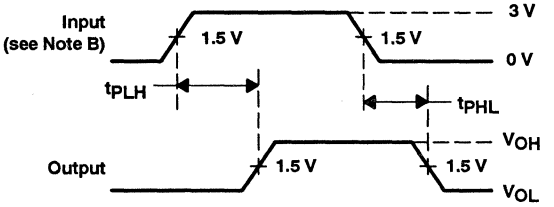
PARAMETER MEASUREMENT INFORMATION

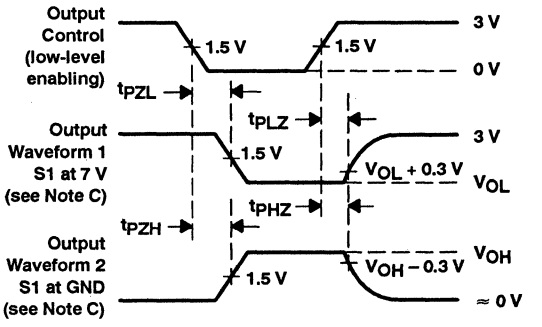


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

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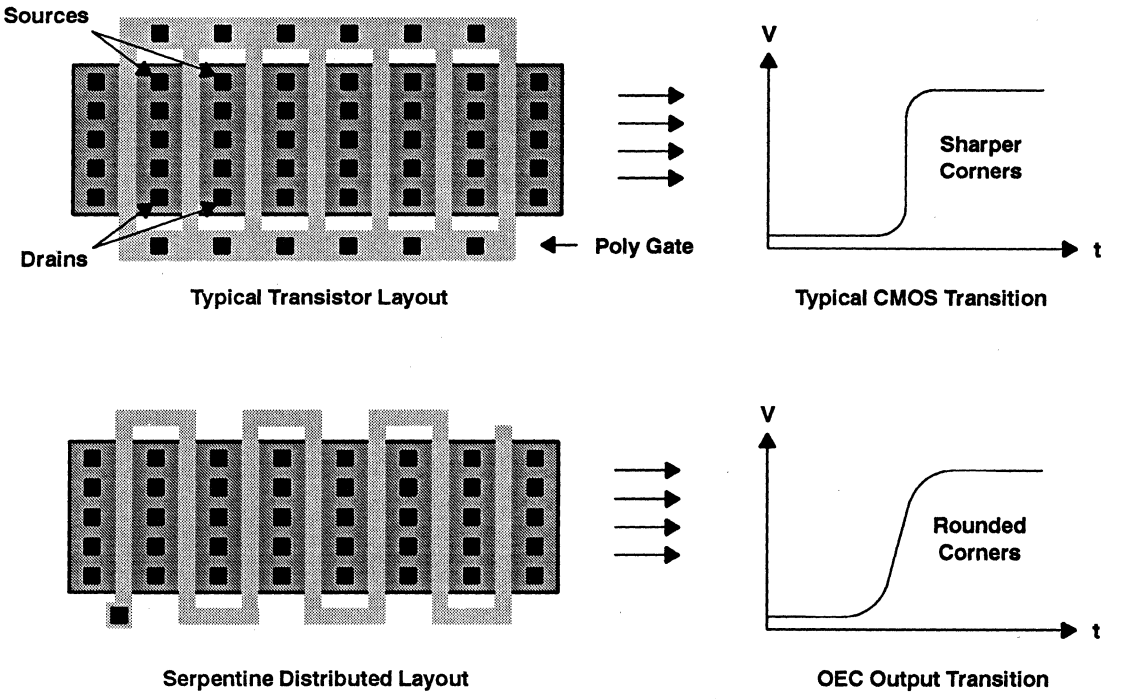
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

Contents

OUTPUT EDGE CONTROL (OEC)™



Typical Transistor Layout

Typical CMOS Transition

Serpentine Distributed Layout

OEC Output Transition

Mixing It Up With 3.3 Volts

Ken Ristow
Steve Perna
Advanced System Logic – Semiconductor Group
Texas Instruments Incorporated

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Printed in the U.S.A.

Introduction

The evolution to 3.3-V supply is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M versions will be developed for operation from a supply voltage of 3.3 +/– 0.3 V. For 16M-DRAM products, there is no such rule-of-thumb as certain vendors expect to operate from 3.3 V, while others offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most versions of the 16M will operate at 3.3 V or lower (with some down to 2.7 V).

Typical 1M-DRAM geometries are on the order of 1.2 μm, and it is not a problem to apply a 5-V power supply to these type of products. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection which over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide, causing internal shorts. Therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V also reduces the power consumed by the device, increasing system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship, a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor towards 3.3-V operation.

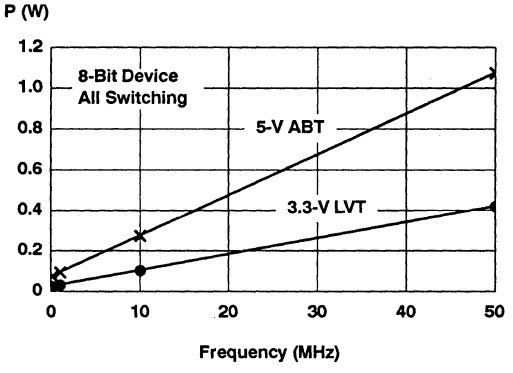

Figure 2. 3-V to 5-V Power vs Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards favor high performance over low power but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the neverending attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebook and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power such as lap-top computers, automotive and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower build-up of heat due to lower power consumption and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low voltage products is one of increased battery lifetime.

Of all the end equipment groups which can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as, point-of-sale terminals which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an onboard transmitter. The goal for these systems is to have a battery life of 8 to 10 hours, roughly the equivalent of one work day or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied, however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged but the spread actually runs from about 3.3 V up to 3.9 V. For now, the unregulated battery market demands low-voltage products which are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be reduced to 2.7 V since this is where devices slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V, with volume requirements not beginning until the 1994–1995 time frame. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies less than 3.3 V has been an issue since 1984 when, through various JEDEC committees, two standards were adopted. Standard 8.0 was intended to address both regulated (3 V to 3.6 V) and unregulated (2 V to 3.6 V) battery applications. Standard 8.1 was intended to address higher performance applications operating from a regulated power supply which could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially, Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage, battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the more critical one being reviewed. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems, as well as, containing a provision for battery-operated systems. Until this point, however, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC}. This limits input voltages to $V_{CC}+0.5$ V and limits direct connection to a 5-V system.

Mixed Mode Operation

This dilemma of device compatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a pressing industry concern. Mixed mode operation allows for direct communication between the two systems. Devices which support this mode must be designed for maximum input voltages of 5.5-V without any long term reliability issues. Another concern is that the output drive must be capable of driving a standard TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS system.

Figure 2 compares the standard TTL interface levels with two of the emerging low voltage standards. Low voltage CMOS (LVCMOS) is a pure CMOS specification which specifies low current rail-to-rail output drive, along with input voltage level, V_{IH} and V_{IL}, which are ratios of V_{CC}. Low-voltage TTL (LVTTL) utilizes the standard TTL input levels of 0.8 and 2 V, as well as specifying a higher output drive than (LVCMOS). To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet ensure requirements of all specifications.

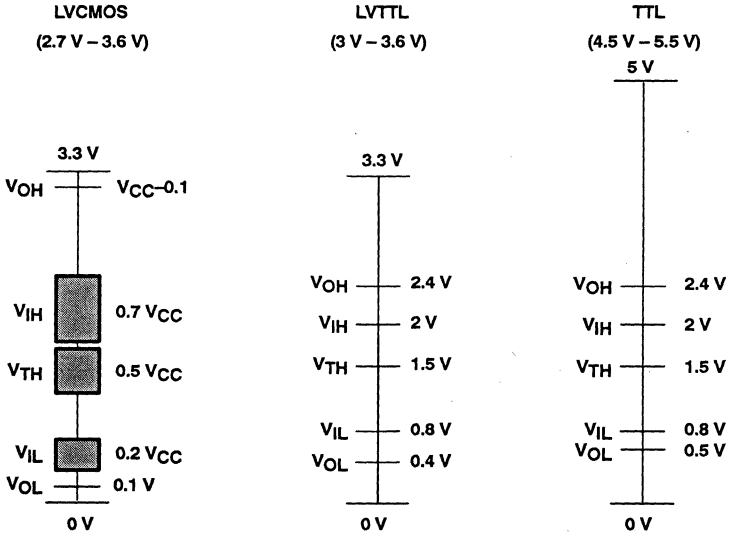

Figure 3. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic parts capable of mixed mode operation. The LVT series of parts rely on a state of the art sub-micron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7- to 3.6-V supply voltage

I/O structures which support live insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CC(L)}$ = 15 mA
$I_{CC(H)}$ = 250 µA
$I_{CC(Z)}$ = 250 µA

Propagation delays of:
t_{pd} < 4.6 ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48- and 56-pin SSOP for LVT
Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (Figure 4), providing the dc drive needed for existing 5-V backplanes, thus, allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

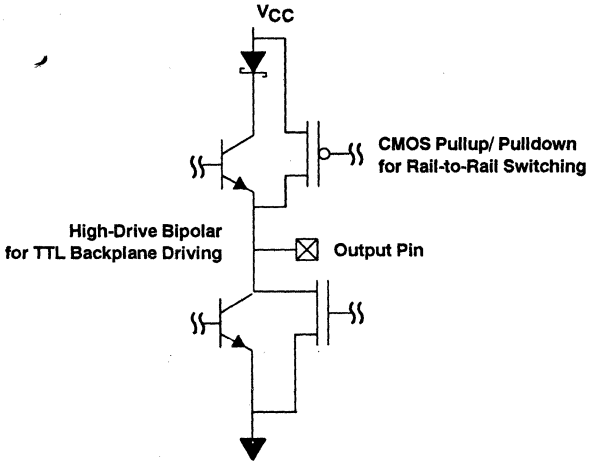

Figure 4. Simplified LVT Output Structure

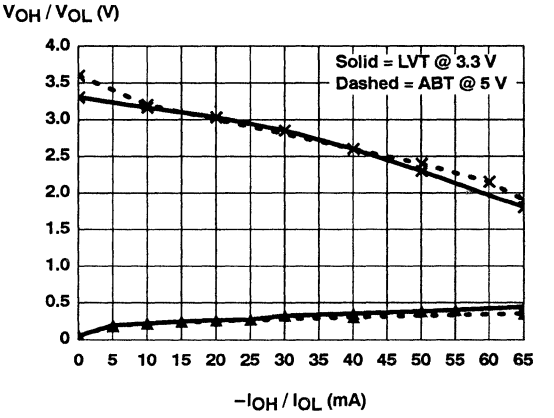

Figure 5. ABT vs LVT Output Drive Comparison

Not only can LVT devices operate as 3-V-to-5-V-level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This permits the devices to be used under partial system power-down applications or those which require live insertion.

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, +/–100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately +/–500 μA, to toggle the state of the input. This current is trivial when compared to the amount of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections, by providing for mixed-signal operation. The devices support live insertion or partial power applications, while providing for low input leakage currents. The outputs are capable of driving today's 5-V backplanes, with a considerable reduction in the device's power consumption, as well as, being packaged in state-of-the-art fine pitch surface-mount packages.

Texas Instruments Crossbar Switches (CBT)

Ramzi Ammar
General Purpose Logic – Semiconductor Group
Texas Instruments Incorporated

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What Are Texas Instruments Crossbar Switches (CBT)?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an N-channel MOS transistor driven by a CMOS gate. When enabled, the N-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈ 1 V less than the gate potential regardless of the level at the input pin. This is one of the N-channel transistor characteristics (see Figures 1 and 2). Note the ≈ 1 V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

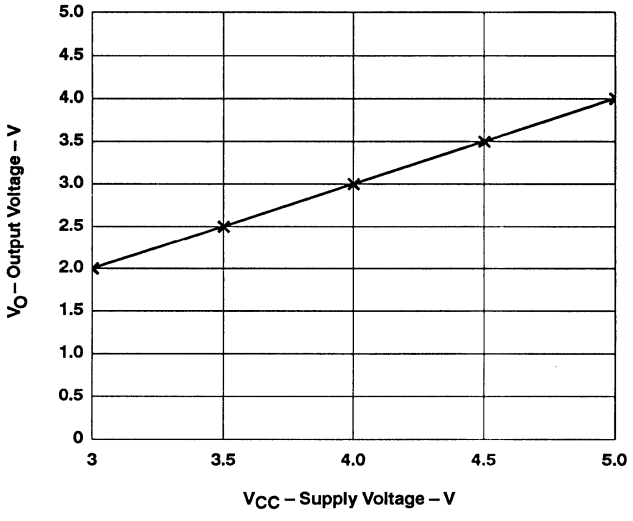


Figure 1. Output Voltage vs Supply Voltage

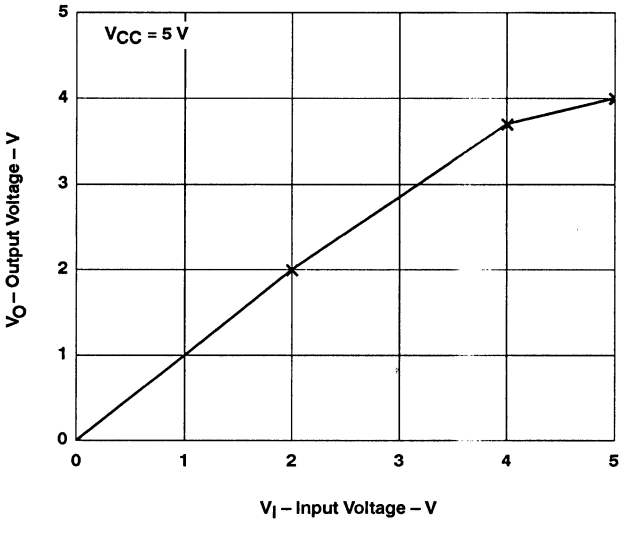


Figure 2. Output Voltage vs Input Voltage

The on-state resistance r_{on} increases gradually with V_I until V_I approaches $V_{CC} - 1$ V, where r_{on} rapidly increases clamping V_O at $V_{CC} - 1$ V (see Figure 3). Also, by the nature of the N-channel transistor design, the input and output pins are fully isolated when the transistor is off. Leakage and capacitance is to ground and not between input and output which minimizes feedthrough when the transistor is off.

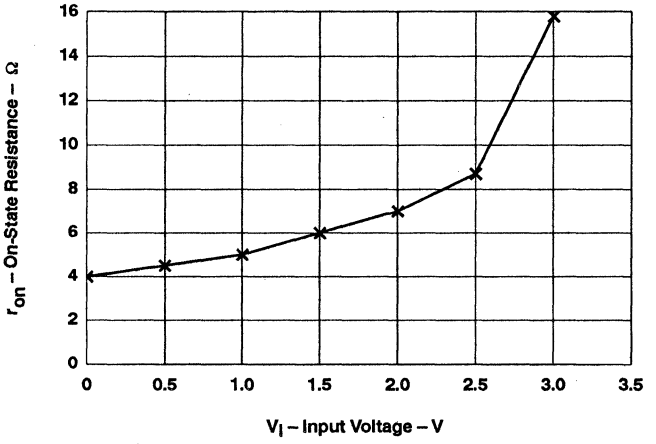
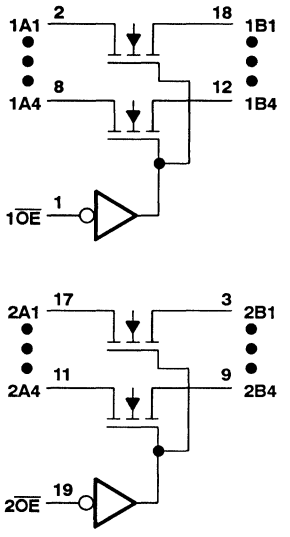


Figure 3. On-State Resistance vs Input Voltage

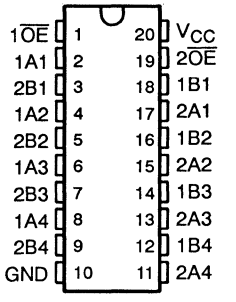
What Does Texas Instruments Offer in the CBT Family?

The following CBT switches offered by Texas Instruments are shown in this application report. This helps designers understand and identify areas where these devices are useful. The following CBT switches that will be offered by Texas Instruments are shown in this application report. This helps designers understand and identify areas where these devices are useful.

SN74CBT3244 – 8-Bit Crossbar Switch



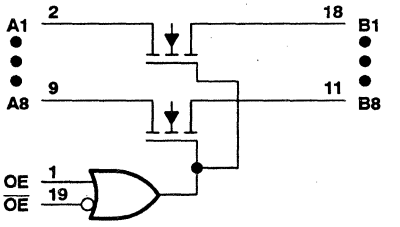
DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



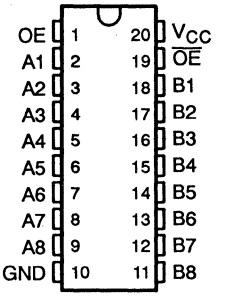
FUNCTION TABLE

1OE	2OE	B1–B4	B5–B8	FUNCTION
L	L	A1–A4	A5–A8	Connect
L	H	A1–A4	Z	Connect
H	L	Z	A5–A8	Connect
H	H	Z	Z	Disconnect

SN74CBT3245 – 8-Bit Crossbar Switch



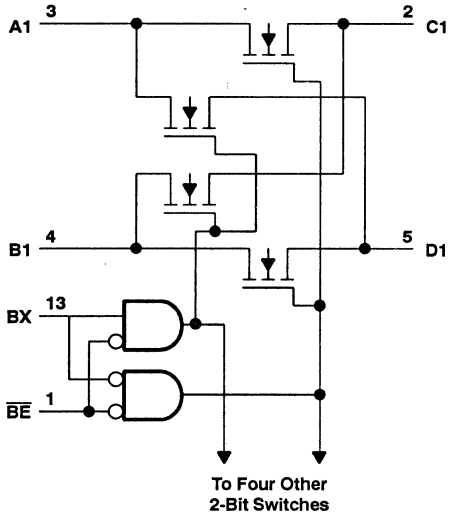
NT, DW, OR PW PACKAGE
(TOP VIEW)



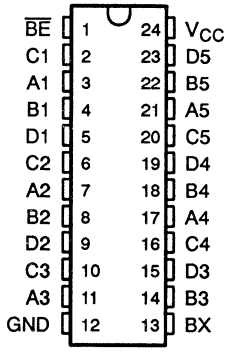
FUNCTION TABLE

OE	$\overline{OE}$	B1–B8	FUNCTION
X	L	A1–A8	Connect
H	X	A1–A8	Connect
L	H	Z	Disconnect

SN74CBT3383 – 10-Bit Bus-Exchange Switch



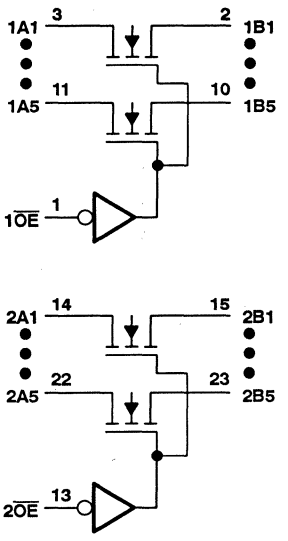
DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



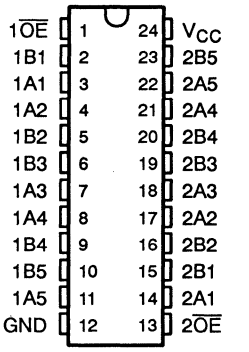
FUNCTION TABLE

$\overline{BE}$	BX	A1–A5	B1–B5	FUNCTION
L	L	C1–C5	D1–D5	Connect
L	H	D1–D5	C1–C5	Exchange
H	X	Z	Z	Disconnect

SN74CBT3384 – 10-Bit Crossbar Switch



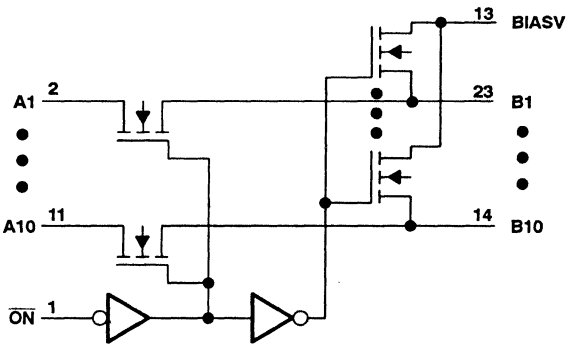
DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



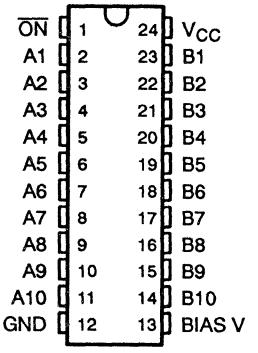
FUNCTION TABLE

1$\overline{OE}$	2$\overline{OE}$	B1–B5	B6–B10	FUNCTION
L	L	A1–A5	A6–A10	Connect
L	H	A1–A5	Z	Connect
H	L	Z	A6–A10	Connect
H	H	Z	Z	Disconnect

SN74CBT6800 – 10-Bit Crossbar Switch With Precharged Outputs for Live Insertion



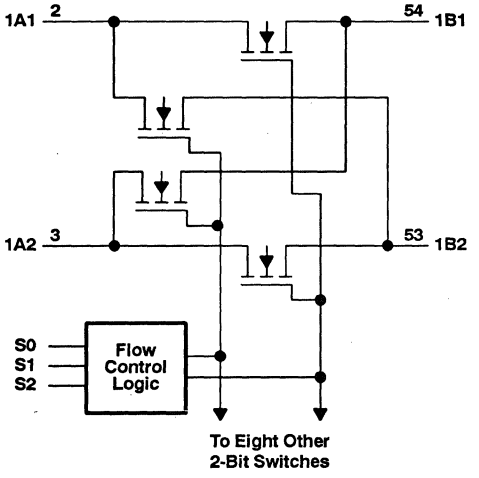
DW, NT, OR PW PACKAGE
(TOP VIEW)



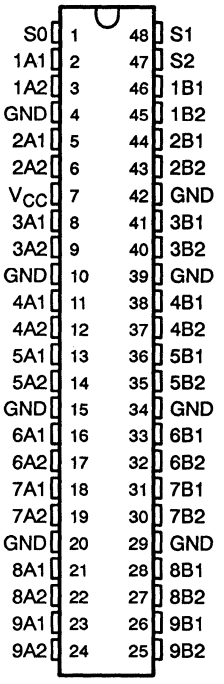
FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIAS V	Precharge

SN74CBT16209 – 18-Bit Bus-Exchange Switch



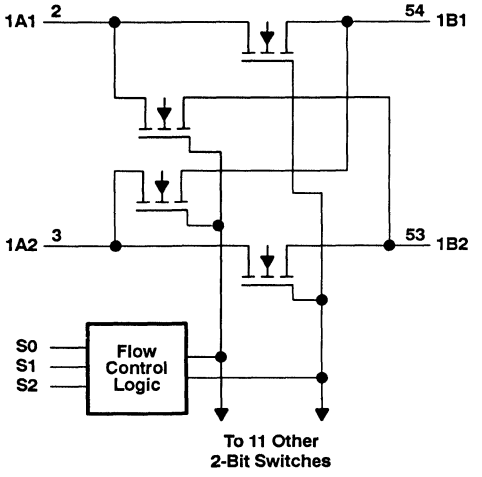
DGG OR DL PACKAGE
(TOP VIEW)



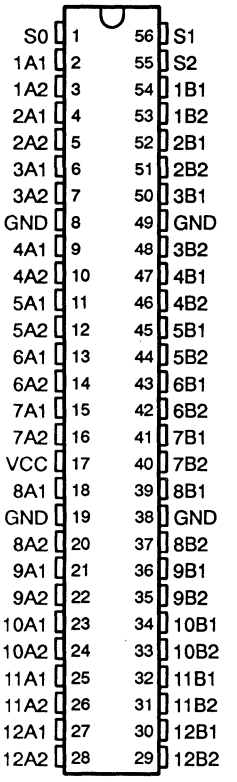
FUNCTION TABLE

FLOW CONTROL			OUTPUTS		FUNCTION
S0	S1	S2	A1	A2	
L	L	L	Z	Z	Disconnect
H	L	L	Z	B2	A2 to B2
L	H	L	B2	Z	A1 to B2
H	H	L	B1	B2	A1 to B1, A2 to B2
L	L	H	B1	Z	A1 to B1
H	L	H	Z	Z	Disconnect
L	H	H	Z	B1	A2 to B1
H	H	H	B2	B1	A1 to B2, A2 to B1

SN74CBT16212 – 24-Bit Bus-Exchange Switch



DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

FLOW CONTROL			OUTPUT		FUNCTION
S0	S1	S2	A1	A2	
L	L	L	Z	Z	Disconnect
H	L	L	Z	B2	A2 to B2
L	H	L	B2	Z	A1 to B2
H	H	L	B1	B2	A1 to B1, A2 to B2
L	L	H	B1	Z	A1 to B1
H	L	H	Z	Z	Disconnect
L	H	H	Z	B1	A2 to B1
H	H	H	B2	B1	A1 to B2, A2 to B1

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices can also provide bidirectional 5-V to 3-V translation with no added propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes the gate to drop to 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

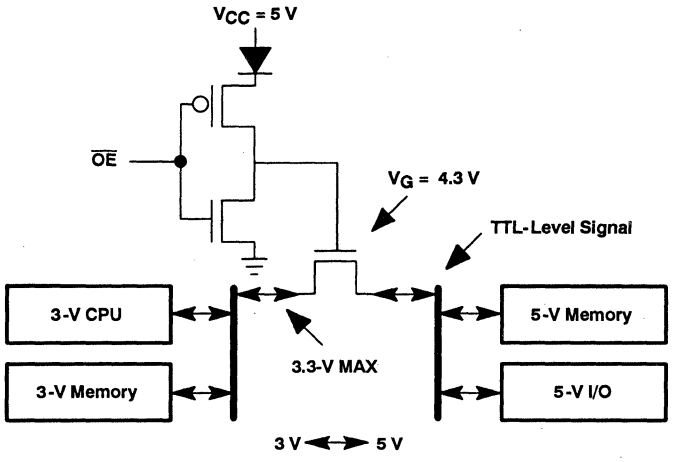


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems where signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices can also replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on resistance and without the reliability problem that relays provide.

Bus Switches Convert TTL Logic to Hot-Card Insertion Capability

This application is used mostly in systems that require hot-card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and can not be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., that do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first followed by the signal pins then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance can not be achieved using CMOS logic since it contains P-channel transistors that provide an inherent diode between the I/O pins and V_{CC} that is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground leaving the bus disturbed.

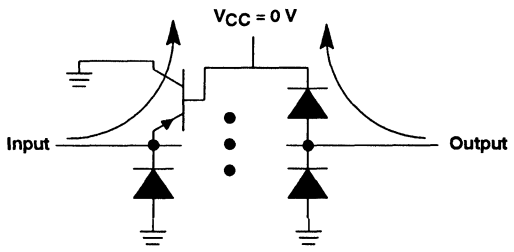


Figure 5. ACL Direction of Current Flow When V_{CC} = 0 V

Another issue to consider is that, when V_{CC} is ramping but still below the device operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error will not occur.

There are two solutions to this problem. One is to use Texas Instruments BCT or ABT families, since both guarantee the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down .

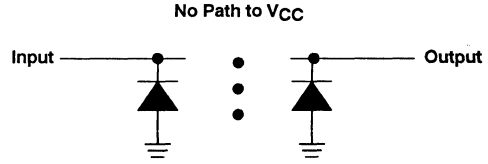


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments crossbar technology (CBT) family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot-card insertion. It has a built-in channel pullup tied to a bias voltage (BIAS V) that is provided to ensure power up such that the buses are not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

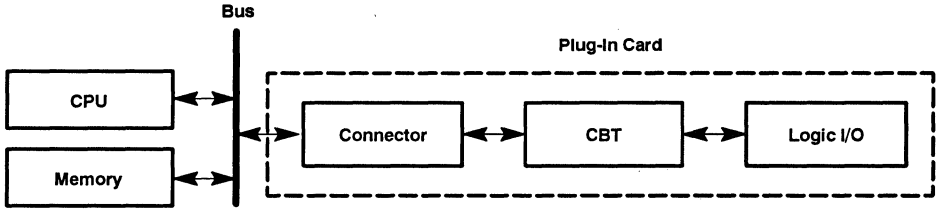
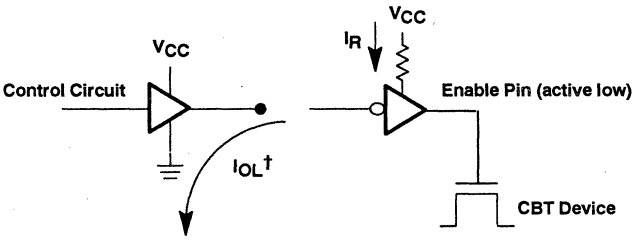


Figure 7. Hot-Card Insertion Application



† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple N-channel transistors, they are capable of providing several important bus functions, such as hot-card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

Example: SN 74ACT16245 DGG R

Prefix

Blank	=	(Standard product)
SN	=	Standard prefix
SNJ	=	JEDEC Publication 101, Class B
JANB	=	MIL-M-38510 Qualified

Unique Circuit Description

Must contain nine or ten characters
(from individual data sheet)

Package

Must contain one to three letters:

D	=	plastic small-outline package
DB	=	plastic shrink small-outline package
DGG	=	plastic thin shrink small-outline package
DL	=	plastic shrink small-outline package
DW	=	plastic wide-body small-outline package
FK	=	ceramic chip carrier package
J, JT	=	ceramic dual-in-line package
N, NT	=	plastic dual-in-line package
PW	=	plastic small-outline package
WD	=	ceramic flatpack package

Tape and Reel Packaging

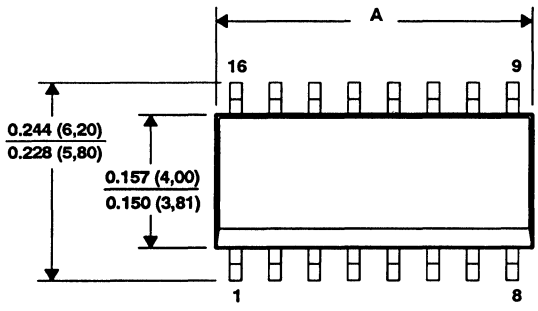
Must be designated by the letters R or LE and valid for surface-mount packages only.
All orders for tape and reel must be for whole reels.
Use R for D, DL, DW, and DGG packages.
Use LE for DB and PW packages.

JULY 1993

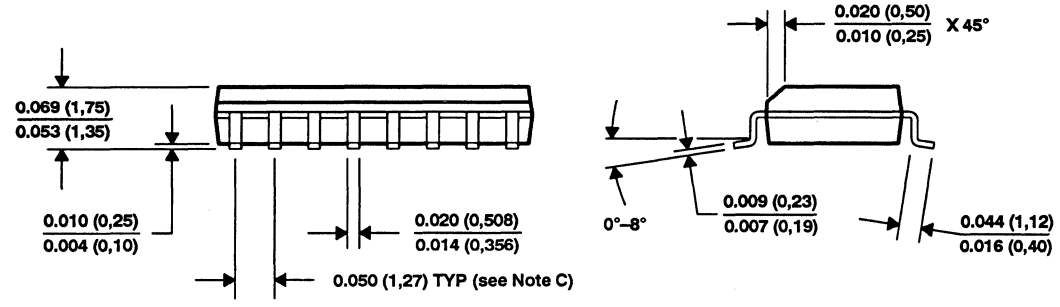
D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16-PIN SHOWN



DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)



4040047/A–07/93

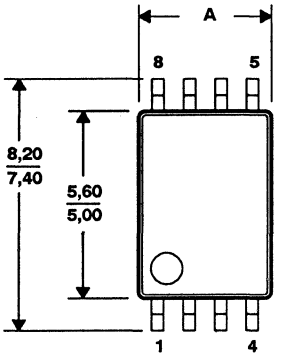
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).
F. Maximum deviation from coplanarity is 0.004 (0,10).

JULY 1993

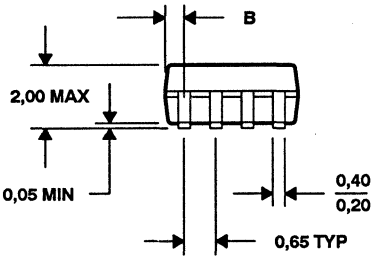
DB/R-PDSO-G**

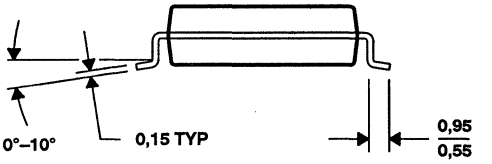
PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70	0,60



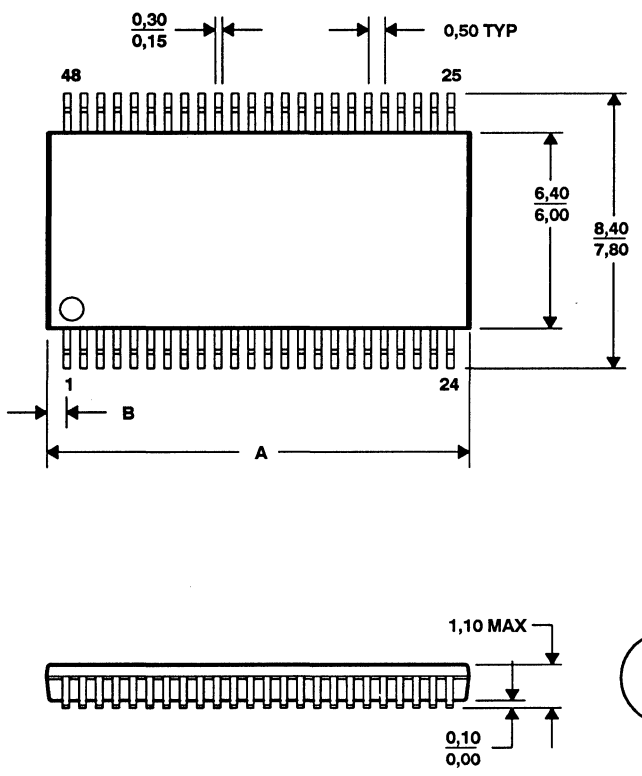


4040065/A–07/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

JULY 1993

DGG/R-PDSO-G** **300-MIL THIN SHRINK SMALL-OUTLINE PACKAGE**



DIM \ PINS**	48	56
A MAX	12,80	14,30
A MIN	12,40	13,90
B MAX	0,65	0,40

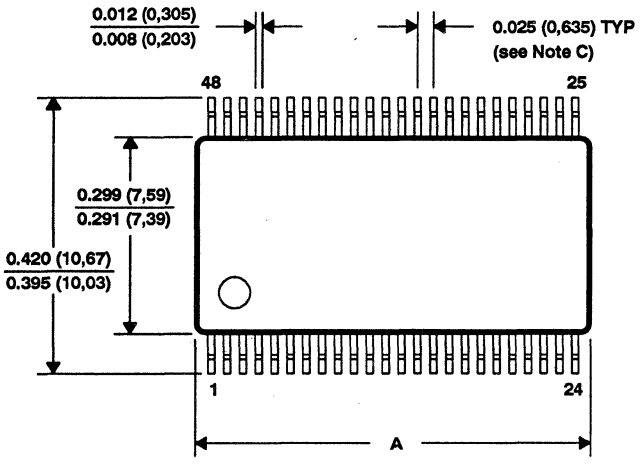
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

JUNE 1993

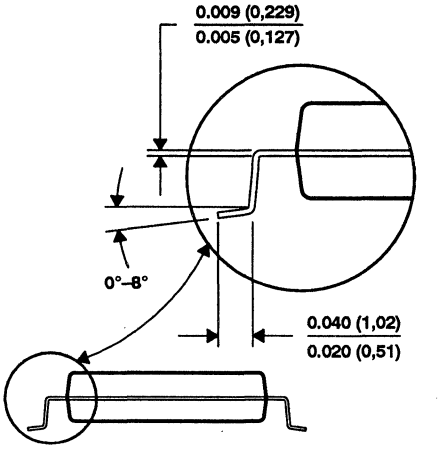
DL/R-PDSO-G**

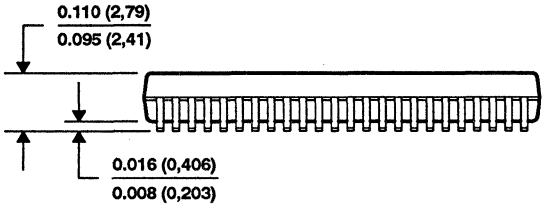
PLASTIC SHRINK SMALL-OUTLINE PACKAGE

48-PIN SHOWN



DIM \ PINS**	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)





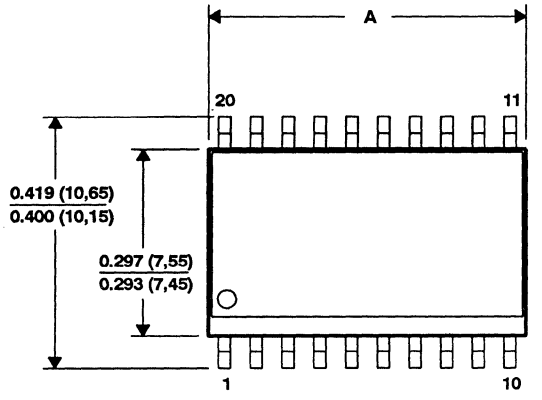
4040048/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash , protrusion or gate burr.
E. Mold flash or protrusion or gate burr shall not exceed 0.015 (0,381).
F. Lead tips coplanar within 0.004 (0,102).
G. Lead length measured from lead top to point 0.010 (0,254) above seating plane.

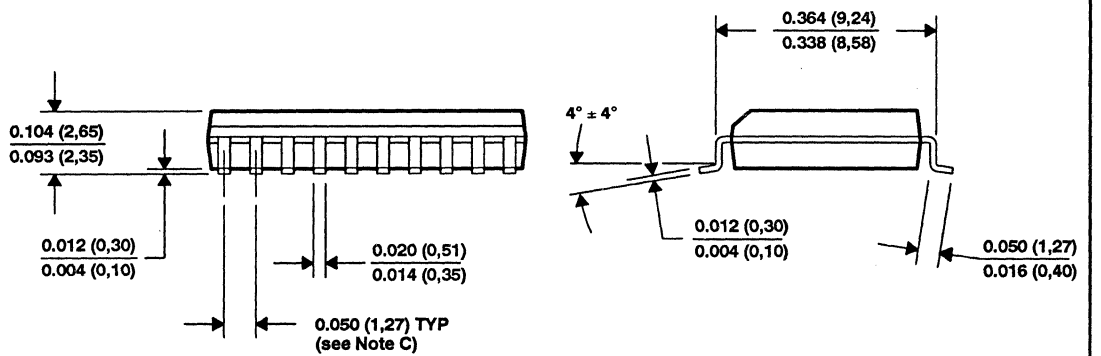
JULY 1993

DW/R-PDSO-G**
20-PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.602 (15,29)	0.696 (17,68)
A MAX	0.408 (10,36)	0.508 (12,90)	0.610 (15,49)	0.704 (17,88)



4040000/A–07/93

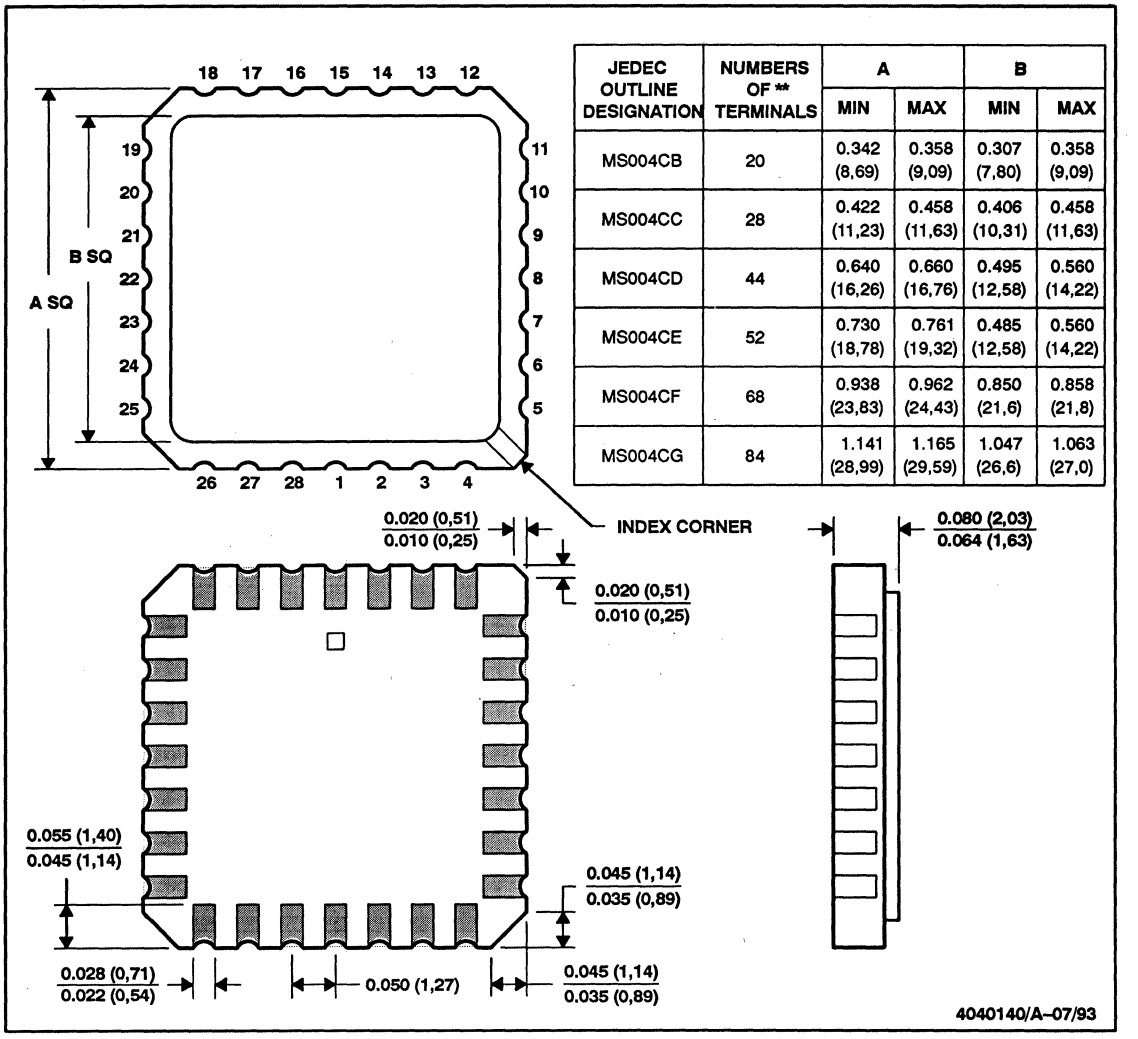
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.10 (0,25) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold flash or protrusion shall not exceed 0.006 (0,15).
F. Lead tips coplanar within ±0.004 (±0,10) exclusive of solder.

JULY 1993

FK/S-CQCC–N**

28 PIN SHOWN

CERAMIC CHIP CARRIER



JEDEC OUTLINE DESIGNATION	NUMBERS OF ** TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

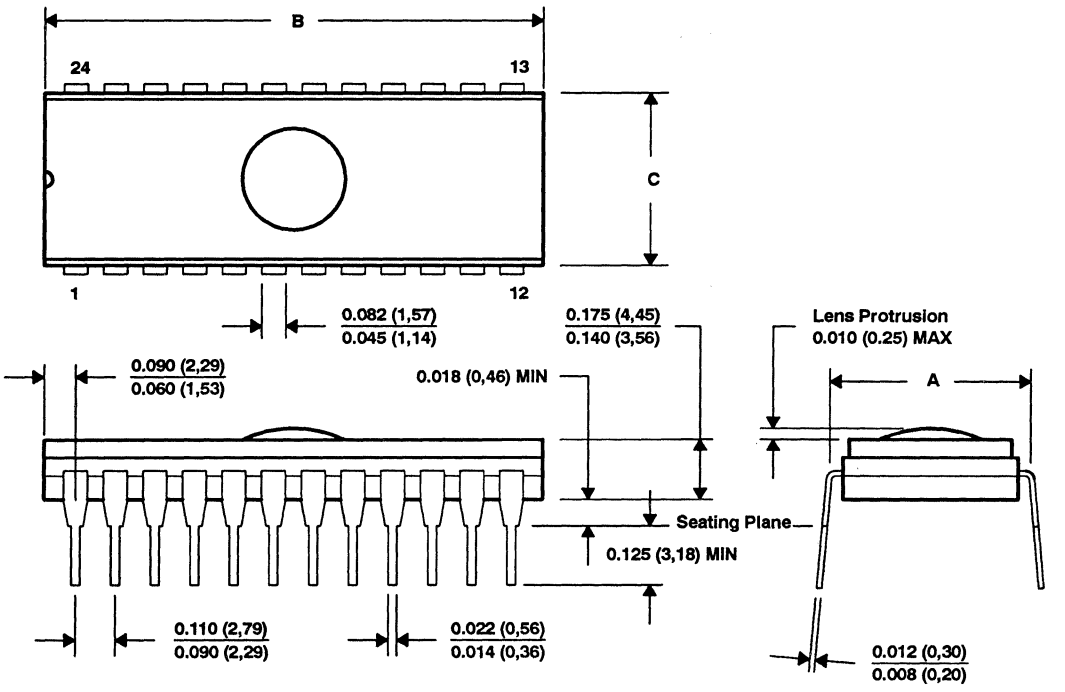
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Three–layer ceramic base with a metal lid and braze seal.
D. FK package terminal assignments conform to JEDEC Standards 1,2 and 11.
E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

JULY 1993

J/R-CDIP–T**

600 MIL CERAMIC DUAL IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS		24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/A–07/93

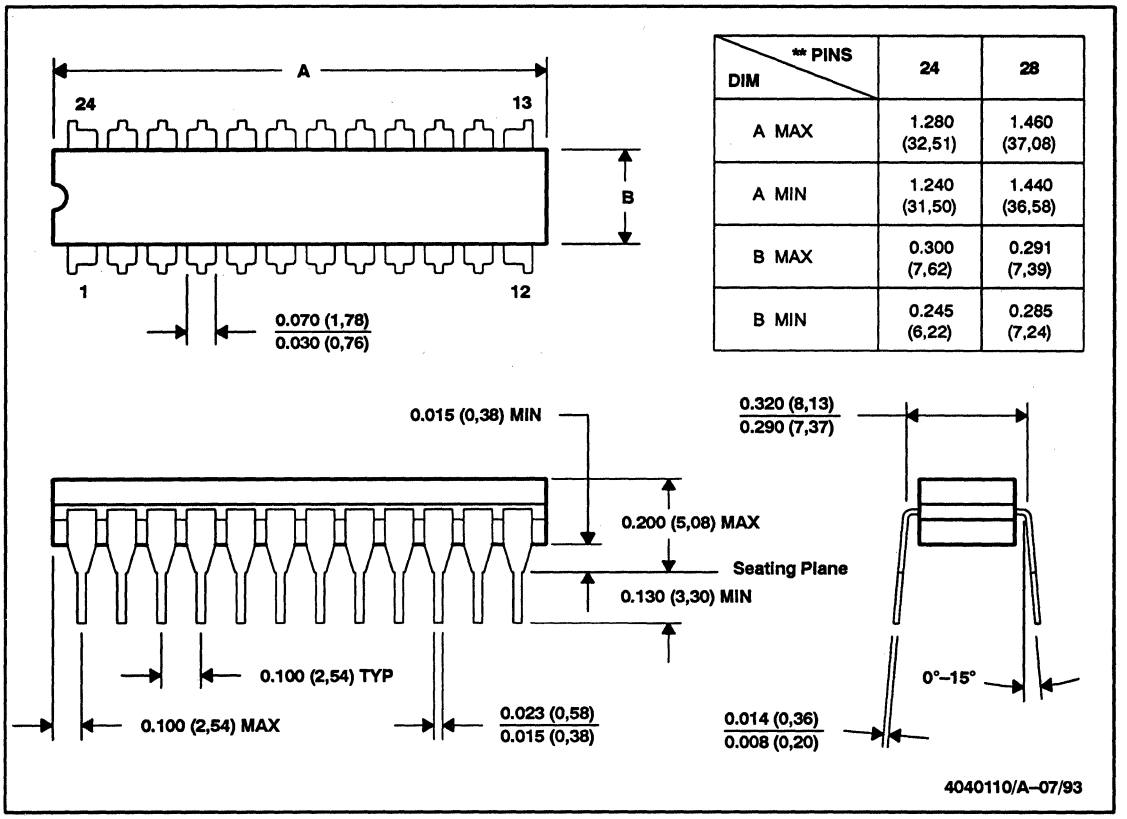
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

JULY 1993

JT/R-GDIP–T**

CERAMIC DUAL IN-LINE PACKAGE

24 PIN SHOWN



DIM \ ** PINS	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

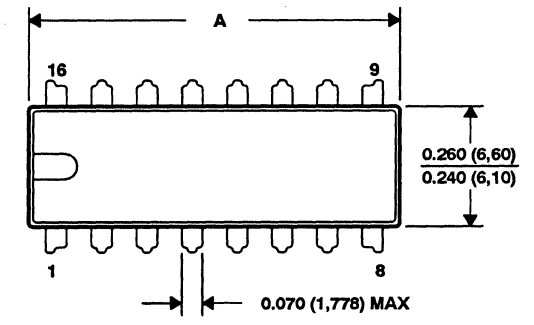
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is glass seal.

JULY 1993

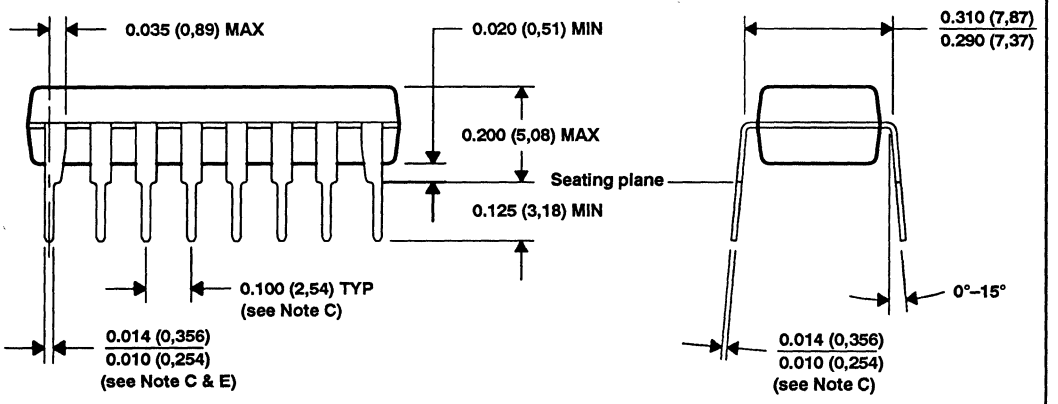
N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16-PIN SHOWN



DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)



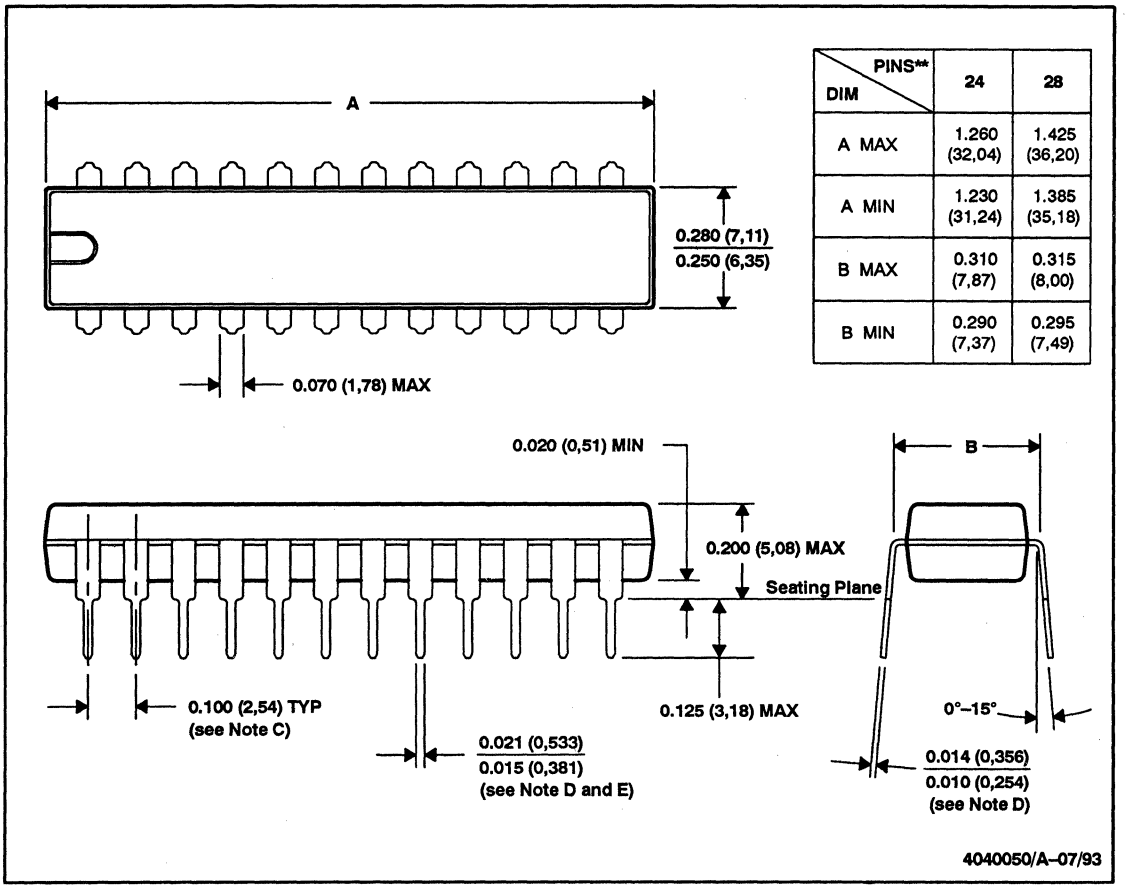
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder dipped leads.
E. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

JULY 1993

NT/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

24-PIN SHOWN



DIM \ PINS**	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

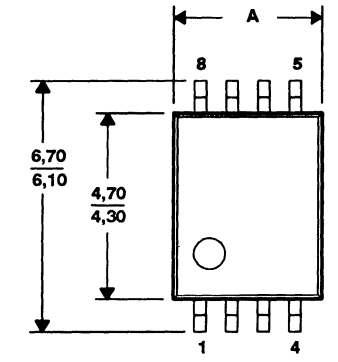
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder dipped leads.
E. For solder dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0,51) above seating plane.

JULY 1993

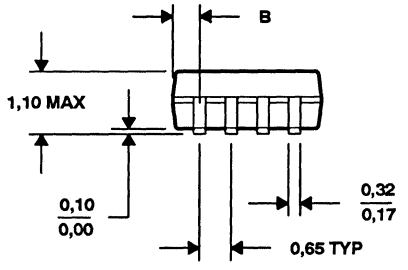
PW/R-PDSO-G**

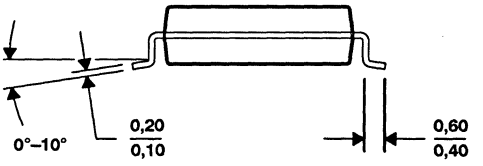
PLASTIC SMALL-OUTLINE PACKAGE

8-PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
B MAX	0,65	0,70	0,38	0,48	0,48	0,78





4040064/A–07/93

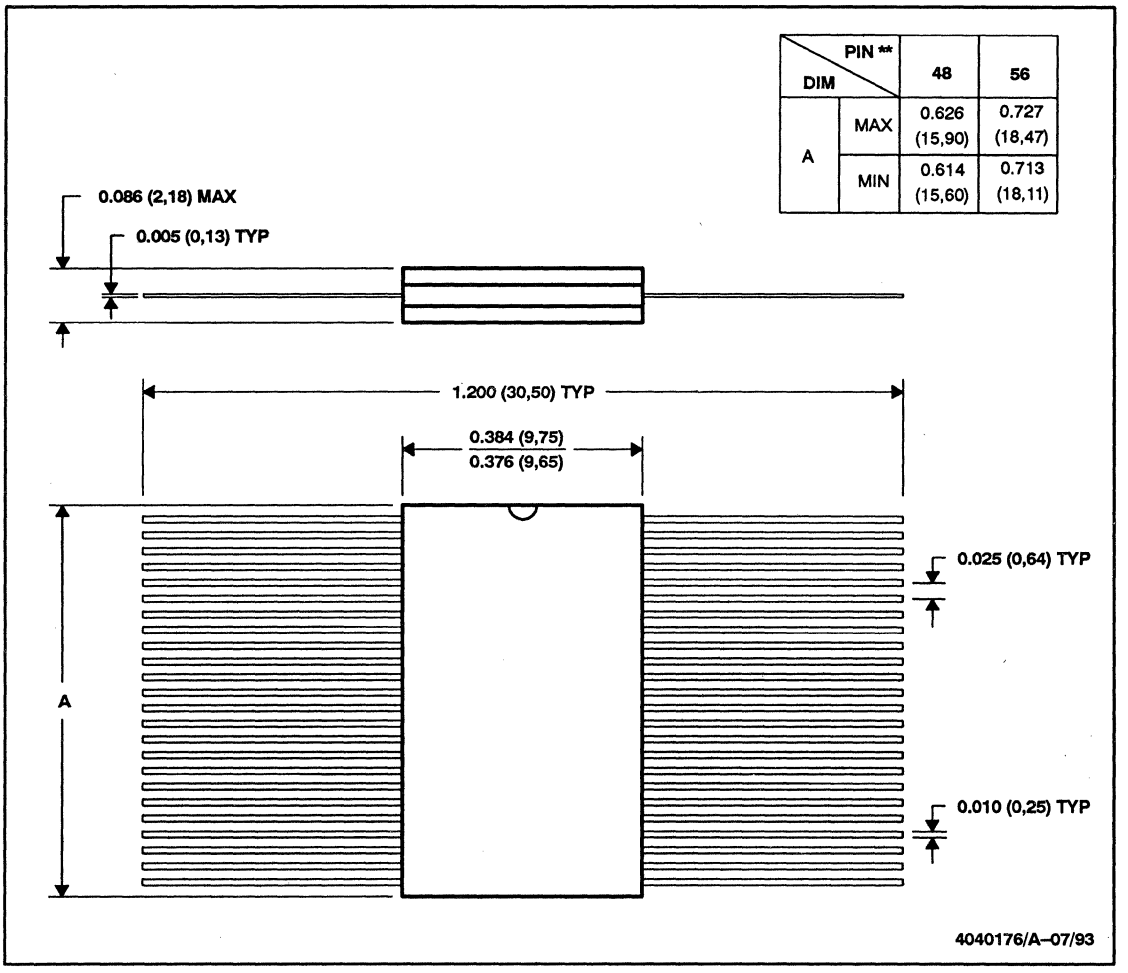
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

JULY 1993

WD/R-GDFP–F**

CERAMIC FLATPACK

48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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